Timberwolf Digital Signal Processor family, powered by *AcuEdge*™ Technology

Designed for IP and Security Cameras

ZL38050

Product Brief

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Description

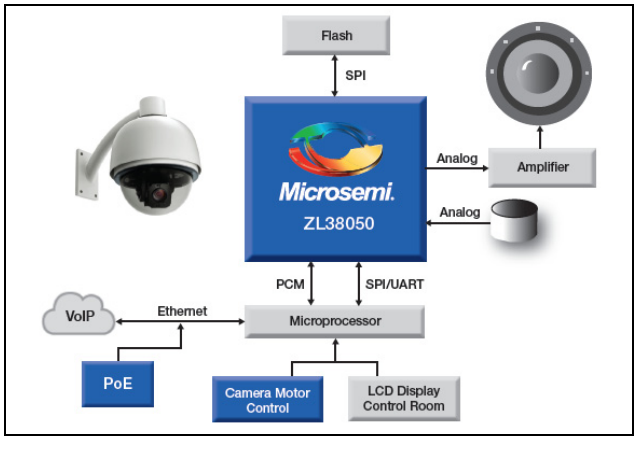
The ZL38050 is part of Microsemi's new Timberwolf audio processor family of products that feature the company's innovative *AcuEdge* acoustic technology, which is a set of highly-complex and integrated algorithms. These algorithms are incorporated into a powerful DSP platform that allow the user to extract intelligible information from the audio environment.

The Microsemi *AcuEdge* Technology ZL38050 device is ideal for IP and security camera applications. Its license-free, royalty-free intelligent audio Firmware (ZLS38050) provides Acoustic Echo Cancellation (AEC), Noise Reduction (NR) and a variety of other voice enhancements to improve both the intelligibility and subjective quality of voice in harsh acoustic environments.

Microsemi offers additional tools to speed up the product development cycle. The *MiTuner*™ ZLS38508 or ZLS38508LITE GUI software packages allow a user to interactively configure the ZL38050 device. The optional *MiTuner* ZLE38470BADA Automatic Tuning Kit provides automatic tuning and easy control for manual fine tuning adjustments.

Applications

- IP Cameras
- Security Cameras



Typical IP Security Camera Application

Ordering Information

Device OPN	Package	Packing
ZL38050LDF1	64-pin QFN (9x9)	Tape & Reel
ZL38050LDG1	64-pin QFN (9x9)	Tray
ZL38050UGB2	56-ball WLCSP (3.1x3.1)	

These packages meet RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

Microsemi *AcuEdge* Technology ZLS38050 Firmware

- Wideband and Narrowband Acoustic Echo Cancellation
- Full or Half duplex operation
- Supports long tail AEC (up to 256 ms) in both Narrowband and Wideband operation
- Howling detection/cancellation
  - Prevents oscillation in AEC audio path
- Non-linear echo cancellation provides higher tolerance for speaker distortions
- Advanced NR reduces background noise from the near-end speech signal using Psychoacoustic techniques
- Provisions for stereo audio mixing and stereo music record and playback (sample rate of 48 kHz) with 16 kHz voice processing
- Multi-tone generation
- Various encoding/decoding options:
  - 16-bit 2's complement (linear)
  - G.711 A/μ law
  - G.722
- Send and receive path equalizers
  - 16-band for Narrowband mode
  - 22-band for Wideband mode
- Comfort noise generation
- 48 kHz bypass mode
- Configurable Cross-Point Switch

Tools

- ZLK38000 Evaluation Kit
- *MiTuner*™ ZLS38508 and ZLS38508LITE GUI
- *MiTuner*™ ZLE38470BADA Automatic Tuning Kit

ZL38050 Hardware Features

- DSP with Voice Hardware Accelerators
- Dual ΔΣ 16-bit digital-to-analog converters (DAC)
  - Sampling up to 48 kHz and internal output drivers
  - Headphone amps capable of 4 single-ended or 2 differential outputs
  - 32 mW output drive power into 16 ohms
  - Impulse pop/click protection
- A single Digital Microphone input supporting up to 2 Microphones
- TDM port shared between PCM and Inter-IC Sound (I^2S)
  - Performs sample rate conversions
- SPI Slave port for host processor interface
- Master SPI port for serial Flash interface
- 14 General Purpose Input/Output (GPIO) pins
- General purpose UART port
- Boots from SPI, UART, or Flash allowing easy firmware updates
  - Can run unattended (controllerless), self-booting into a configured operational state
- Crystal-less operation (with a valid TDM clock)
- 2 low power modes controlled by reset
- Available in miniature Wafer Level Chip Scale Package

Performance

- AEC Tail Length: 256 ms
- AEC sampling rate: 8 and 16 kHz
- Single-Talk Weighted Terminal Coupling Loss (TCLw): > 60 dB
- Double-Talk TCLw: > 40 dB
- Double-Talk Attenuation: < 3 dB
- Noise reduction up to 30 dB

The *MiTuner*™ Automatic Tuning Kit and ZLS38508 MiTuner GUI

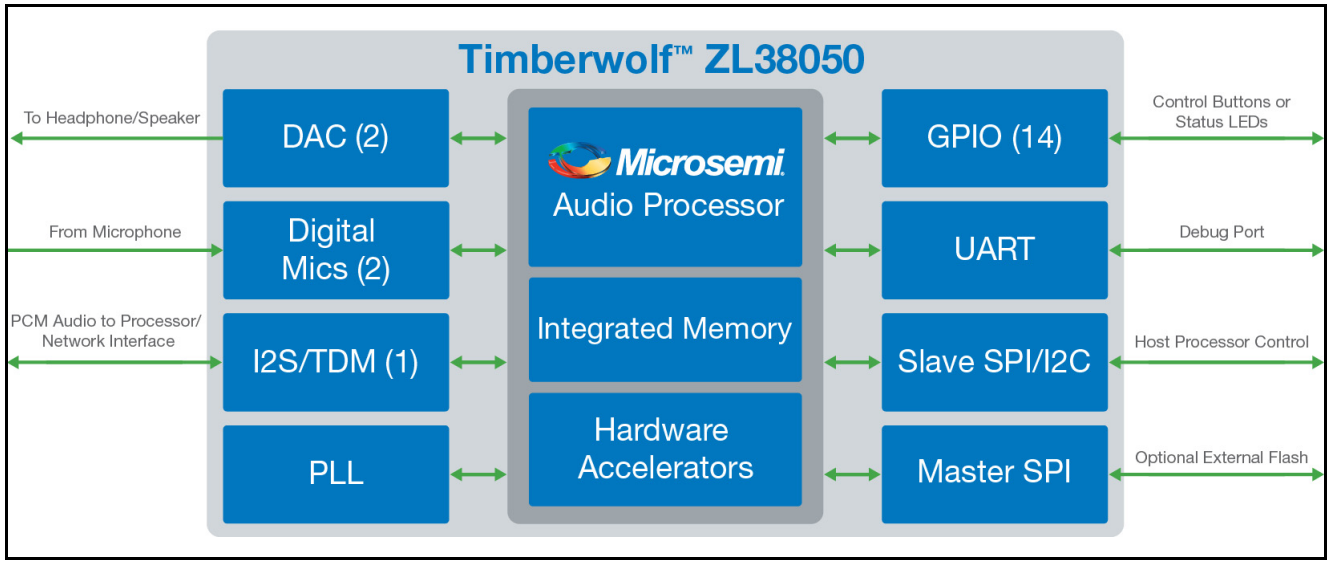
Microsemi's Automatic Tuning Kit provides Audio Interface Box hardware, Auto Tuning and Subjective Tuning software, and GUI support for tuning of Microsemi's *AcuEdge* Technology Audio Processors.

ZLS38508 software features:

- Allows tuning of key parameters of the system design
- Provides visual representations of the audio paths with drop-down menus to program parameters, allowing:
  - Control of the audio routing configuration
  - Programming of key building blocks in the transmit (Tx) and receive (Rx) audio paths
  - Setting analog and digital gains
- Configuration parameters allow users to “fine tune” the overall performance

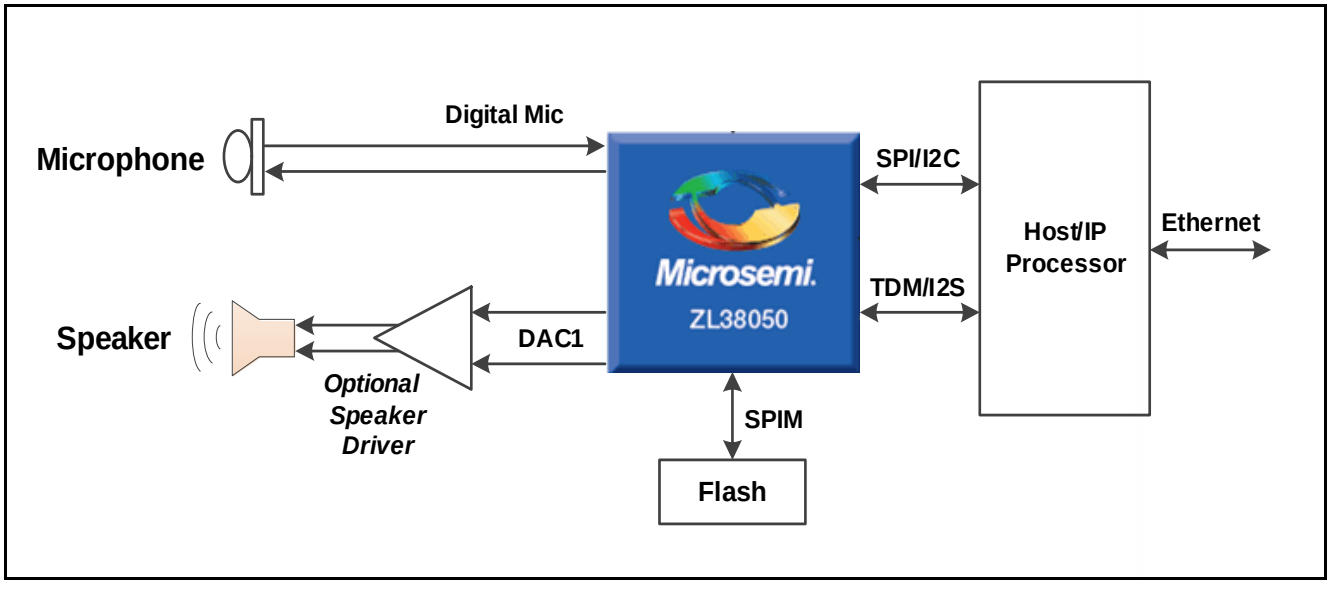
Device Block Diagram

The Microsemi ZL38050 Audio Processor powered by ZLS38050 *AcuEdge*™ Technology Firmware is ideal for providing high definition audio to IP cameras.



ZL38050 Audio Processor for IP and Security Cameras

Typical Application Block Diagram

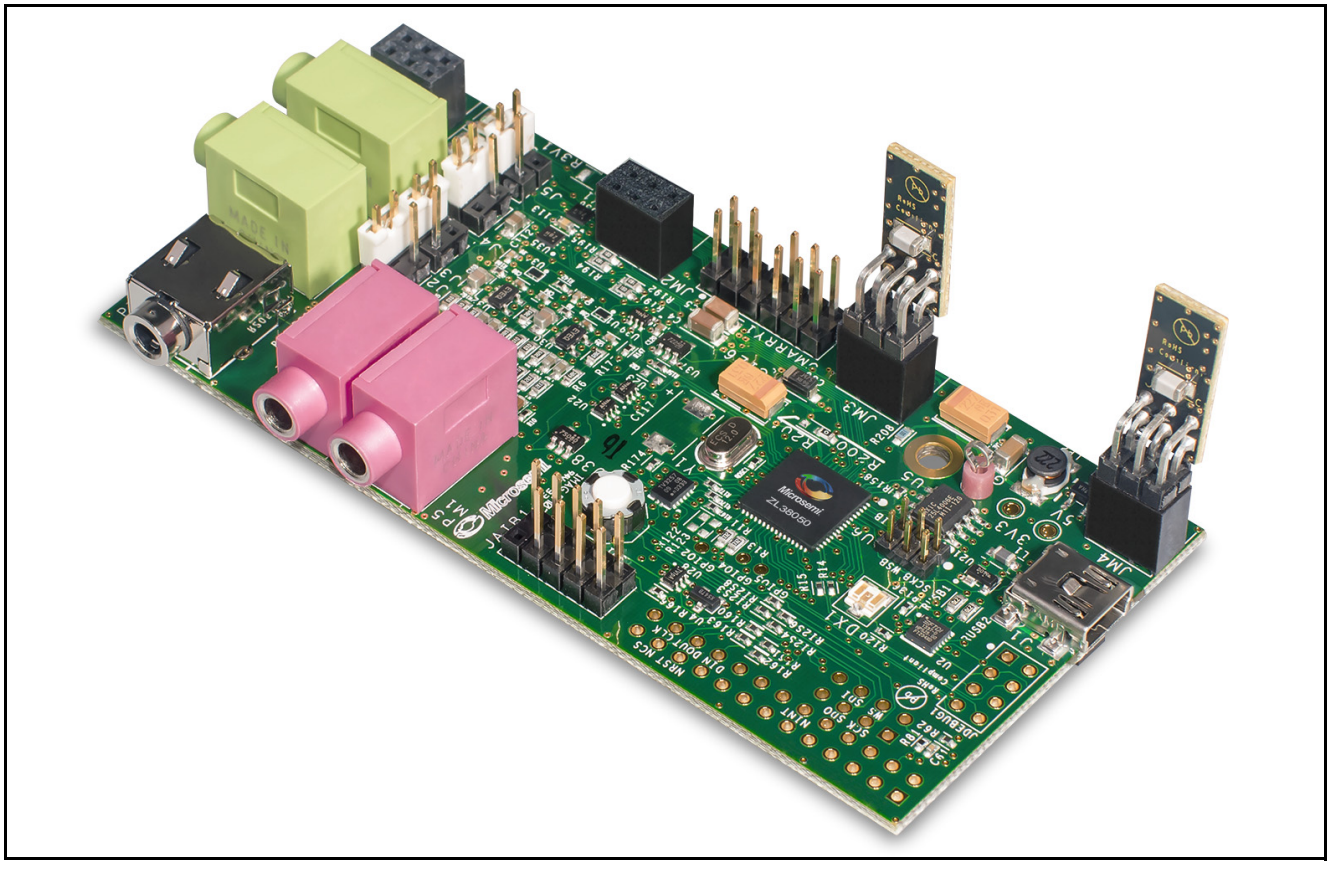


IP Camera HD Voice 2-way Audio Application

ZLK38000 Evaluation Kit

The ZLK38000 Evaluation Kit includes all the hardware necessary to operate the ZLE38000 Evaluation Board. The Evaluation Board provides a flexible platform to evaluate a ZL38050 Timberwolf Audio Processor device with *AcuEdge*™ Technology Firmware.

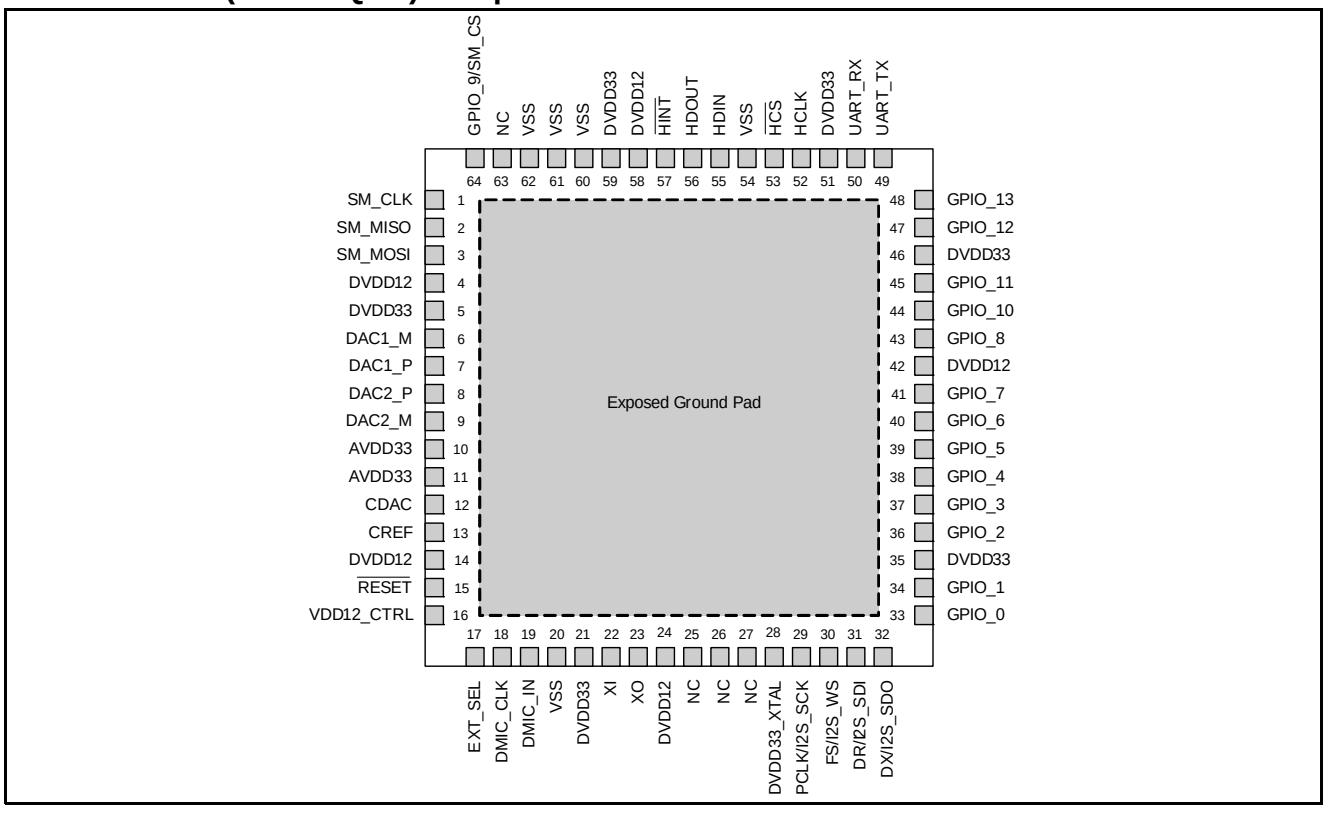
The ZLE38000 Evaluation Board provides a simple analog interface that can be connected to microphones and speakers to allow for subjective testing. The miniature size allows for easy mounting in an existing plastic enclosure.



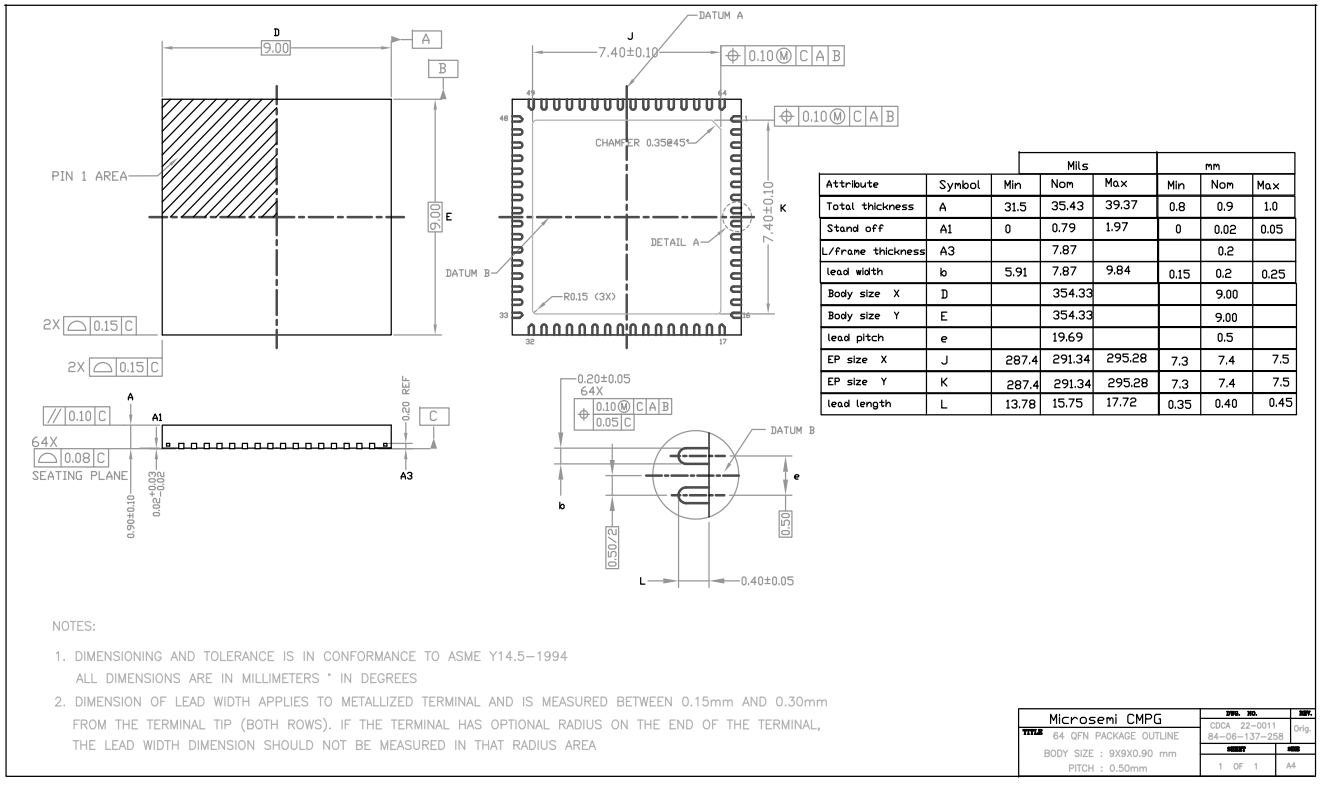
ZLE38000 Evaluation Board

Firmware Code for the ZL38050 can be downloaded into the Evaluation Board using the ZLS38000 Firmware Loader software. The ZLE38000 Evaluation Board can then be controlled using the *MiTuner*™ GUI Lite Software (ZLS38508LITE) or the full *MiTuner* GUI Software package (ZLS38508). Microsemi has developed automatic tuning capability into the full *MiTuner* GUI Software to further facilitate and shorten the design process. The ZLS38508 Software package consists of the *MiTuner* GUI Software and the Audio Interface Box (AIB) Evaluation Kit (ZLE38470BADA) hardware, together performing automatic tuning of the Timberwolf Audio Processor on the Evaluation Board or in a system design.

Device Pinout (64-Pin QFN) – Top View



Package Outline (64-Pin QFN)



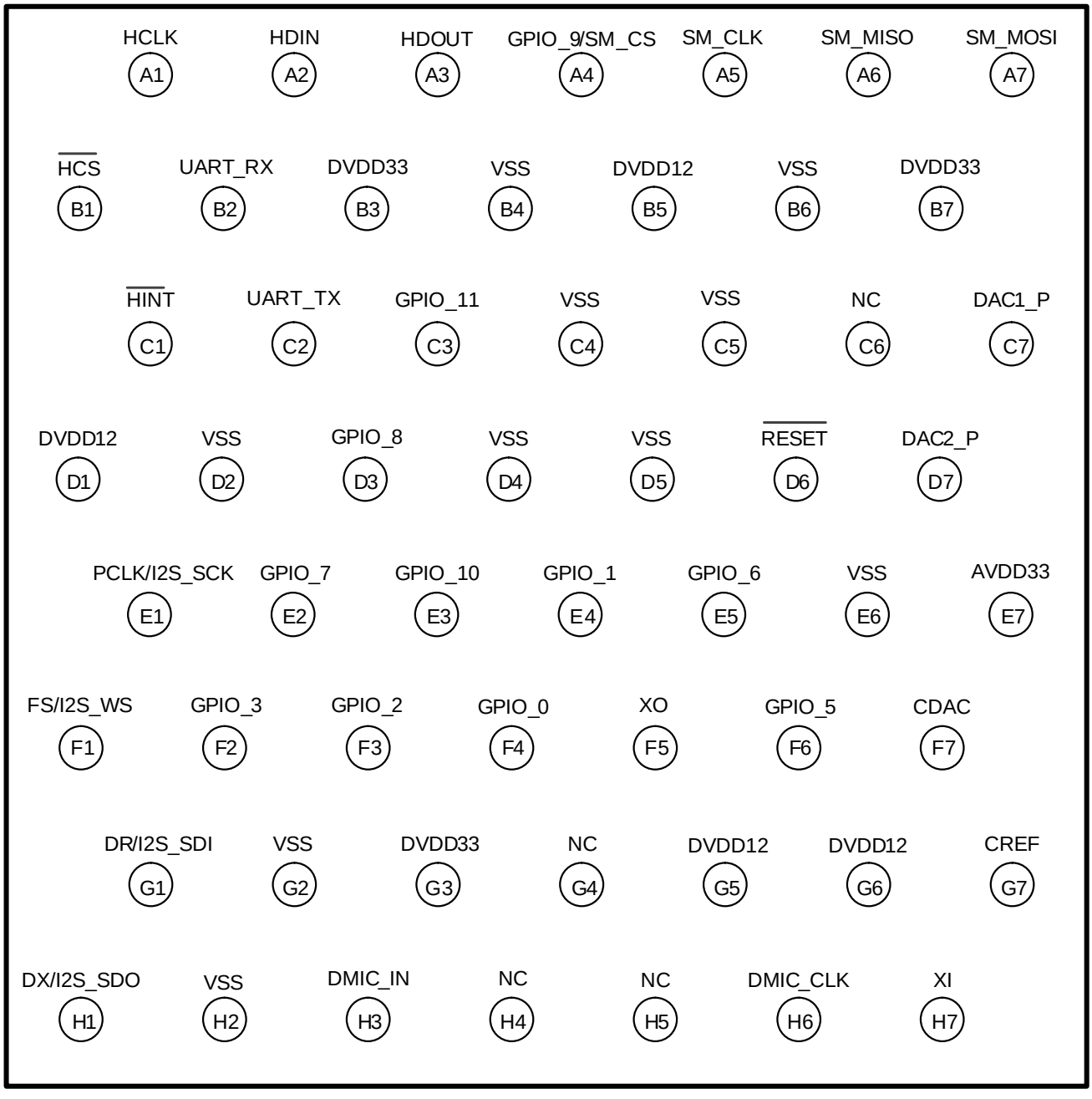
Attribute	Symbol	Mils			mm		
		Min	Nom	Max	Min	Nom	Max
Total thickness	A	31.5	35.43	39.37	0.8	0.9	1.0
Stand off	A1	0	0.79	1.97	0	0.02	0.05
L/frame thickness	A3		7.87			0.2	
lead width	b	5.91	7.87	9.84	0.15	0.2	0.25
Body size X	D		354.33			9.00	
Body size Y	E		354.33			9.00	
lead pitch	e		19.69			0.5	
EP size X	J	287.4	291.34	295.28	7.3	7.4	7.5
EP size Y	K	287.4	291.34	295.28	7.3	7.4	7.5
lead length	L	13.78	15.75	17.72	0.35	0.40	0.45

NOTES:

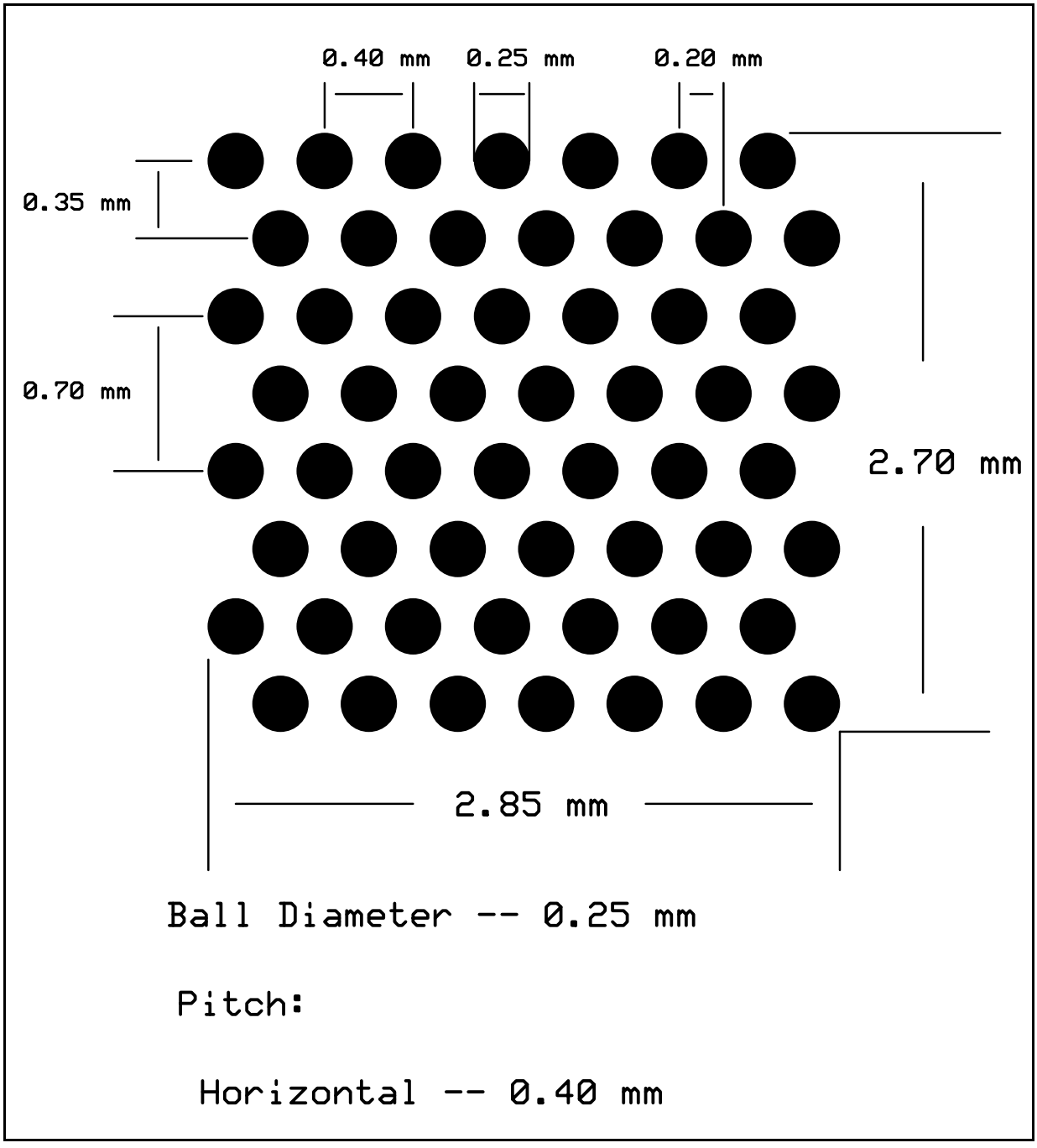
1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Microsemi CMPG
TITLE 64 QFN PACKAGE OUTLINE
BODY SIZE : 9X9X0.90 mm
PITCH : 0.50mm
DWG. NO. 0004 22-0011
84-06-137-258
REV. Orig.
SHEET 1 OF 1
SIZE A4

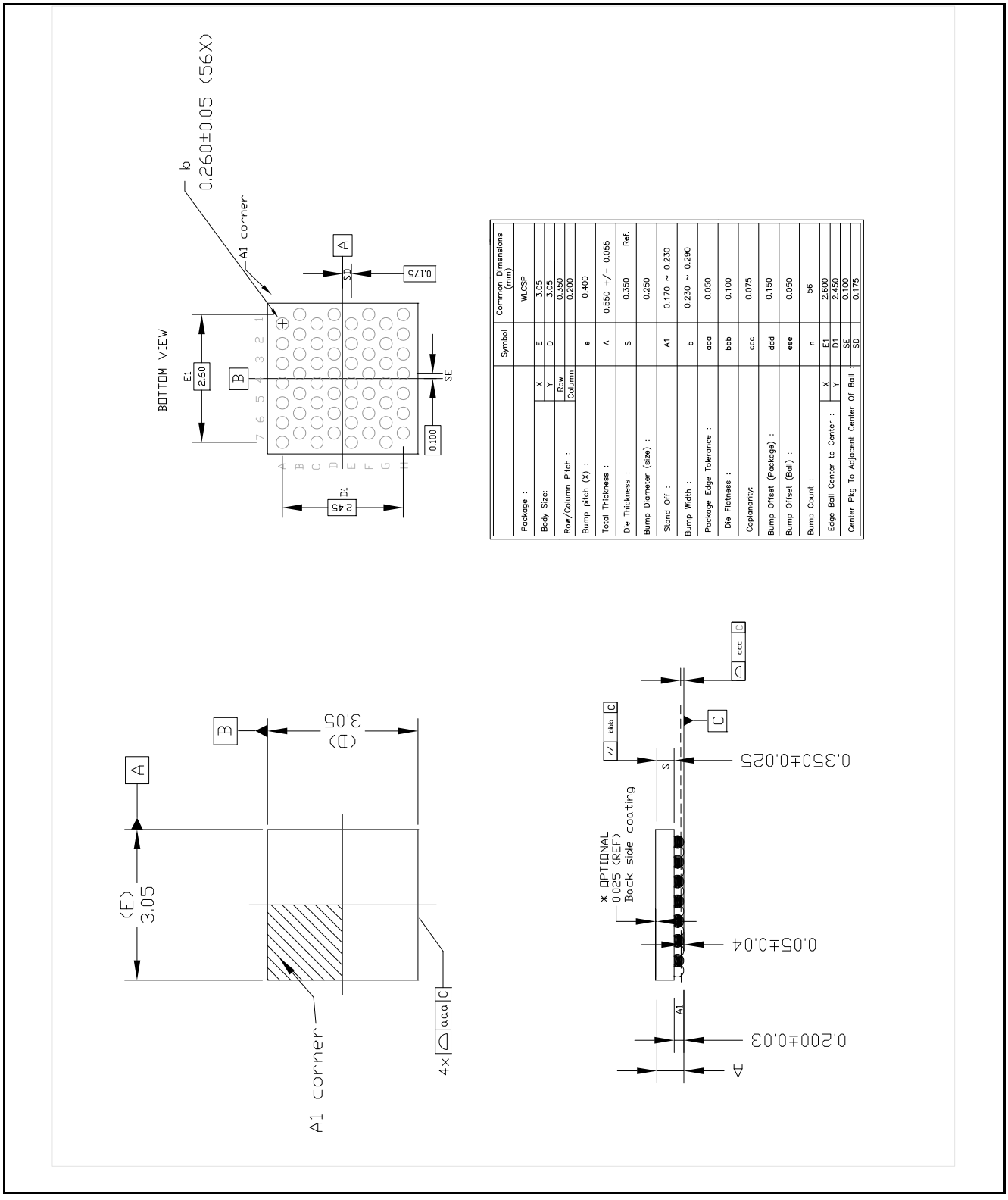
Device Pinout (56-Ball WLCSP) – Top View



Staggered Balls (56-Ball WLCSP) – Bottom View



Package Outline (56-Ball WLCSP)



Common Dimensions (mm)			Symbol	WLCSP
Package :				
Body Size:	X		E	3.05
	Y		D	3.05
Row/Column Pitch :	Row			0.350
	Column			0.200
Bump pitch (X) :			e	0.400
Total Thickness :			A	0.550 +/- 0.055
Die Thickness :			S	0.350 Ref.
Bump Diameter (size) :				0.250
Stand Off :			A1	0.170 ~ 0.230
Bump Width :			b	0.230 ~ 0.290
Package Edge Tolerance :			aaa	0.050
Die Flatness :			bbb	0.100
Coplanarity:			ccc	0.075
Bump Offset (Package) :			ddd	0.150
Bump Offset (Ball) :			eee	0.050
Bump Count :			n	56
Edge Ball Center to Center :	X		E1	2.600
	Y		D1	2.450
Center Pkg To Adjacent Center Of Ball :			SE	0.100
			SD	0.175

Device Pinout

QFN Pin #	WLCSP Ball	Name	Type	Description
15	D6	$\overline{\text{RESET}}$	Input	**Reset.** When low the device is in its reset state and all tristate outputs will be in a high impedance state. This input must be high for normal device operation. A 10 KΩ pull-up resistor is required on this node to DVDD33 if this pin is not continuously driven.

Table 1 - Reset Pin Description

QFN Pin #	WLCSP Ball	Name	Type	Description
6	–	DAC1_M	Output	**DAC 1 Minus Output.** This is the negative output signal of the differential amplifier of the DAC 1. *Not available on the WLCSP package.*
7	C7	DAC1_P	Output	**DAC 1 Plus Output.** This is the positive output signal of the differential amplifier of the DAC 1.
9	–	DAC2_M	Output	**DAC 2 Minus Output.** This is the negative output signal of the differential amplifier of the DAC 2. *Not available on the WLCSP package.*
8	D7	DAC2_P	Output	**DAC 2 Plus Output.** This is the positive output signal of the differential amplifier of DAC 2.
12	F7	CDAC	Output	**DAC Reference.** This node requires capacitive decoupling.
13	G7	CREF	Output	**Common Mode Reference.** This node requires capacitive decoupling.

Table 2 - DAC Pin Descriptions

QFN Pin #	WLCSP Ball	Name	Type	Description
18	H6	DMIC_CLK	Output	**Digital Microphone Clock Output.** Clock output for digital microphones and digital electret microphone pre-amplifier devices.
19	H3	DMIC_IN	Input	**Digital Microphone Input.** Stereo or mono digital microphone input. *Tie to VSS if unused.*

Table 3 - Microphone Pin Descriptions

The ZL38050 device has one TDM interface. The TDM block is capable of being a master or a slave. The port can be configured for Pulse-Code Modulation (PCM) or Inter-IC Sound (I^2S) operation. The port conforms to PCM, GCI, and I^2S timing protocols.

QFN Pin #	WLCSP Ball	Name	Type	Description
29	E1	PCLK/ I2S_SCK	Input/ Output	**PCM Port Clock (Input/Tristate Output).** PCLK is equal to the bit rate of signals DR/DX. In TDM master mode this clock is an output and in TDM slave mode this clock is an input. **I^2S Port Serial Clock (Input/Tristate Output).** This is the I^2S port bit clock. In I^2S master mode this clock is an output and drives the bit clock input of the external slave device's peripheral converters. In I^2S slave mode this clock is an input and is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I^2S slave mode. *A 100 KΩ pull-down resistor is required on this pin to VSS. If this pin is unused, tie the pin to VSS.* *When driving PCLK/I2S_SCK from a host, one of the following conditions must be satisfied:* *1. Host drives PCLK low during reset, or* *2. Host tri-states PCLK during reset (the 100 KΩ resistor will keep PCLK low), or* *3. Host drives PCLK at its normal frequency*
30	F1	FS/ I2S_WS	Input/ Output	**PCM Port Frame Pulse (Input/Tristate Output).** This is the TDM frame alignment reference. This signal is an input for applications where the PCM bus is frame aligned to an external frame signal (slave mode). In master mode this signal is a frame pulse output. **I^2S Port Word Select (Left/Right) (Input/Tristate Output**). This is the I^2S port left or right word select. In I^2S master mode word select is an output which drives the left/right input of the external slave device's peripheral converters. In I^2S slave mode this pin is an input which is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I^2S slave mode. *Tie this pin to VSS if unused.*
31	G1	DR/ I2S_SDI	Input	**PCM Port Serial Data Stream Input.** This serial data stream operates at PCLK data rates. **I^2S Port Serial Data Input.** This is the I^2S port serial data input. *Tie this pin to VSS if unused.*
32	H1	DX/ I2S_SDO	Output	**PCM Port Serial Data Stream Output.** This serial data stream operates at PCLK data rates. **I^2S Port Serial Data Output.** This is the I^2S port serial data output.

Table 4 - TDM and I^2S Ports Pin Description

The HBI port functions as a peripheral interface for an external controller, and supports access to the internal registers and memory of the device.

QFN Pin #	WLCSP Ball	Name	Type	Description
52	A1	HCLK	Input	**HBI SPI Slave Port Clock Input.** Clock input for the SPI Slave port. Maximum frequency = 25 MHz. This input should be tied to VSS in I^2C mode. *Tie this pin to VSS if unused.*
53	B1	$\overline{HCS}$	Input	**HBI SPI Slave Chip Select Input.** This active low chip select signal activates the SPI Slave port. **HBI I^2C Serial Clock Input.** This pin functions as the I2C_SCLK input in I^2C mode. A pull-up resistor is required on this node for I^2C operation. *Tie this pin to VSS if unused.*
55	A2	HDIN	Input	**HBI SPI Slave Port Data Input.** Data input signal for the SPI Slave port. This input selects the slave address in I^2C mode. *Tie this pin to VSS if unused.*
56	A3	HDOUT	Input/ Output	**HBI SPI Slave Port Data Output (Tristate Output).** Data output signal for the SPI Slave port. **HBI I^2C Serial Data (Input/Output).** This pin functions as the I2C_SDA I/O in I^2C mode. A pull-up resistor is required on this node for I^2C operation.
57	C1	$\overline{HINT}$	Output	**HBI Interrupt Output.** This output can be configured as either CMOS or open drain by the host.

Table 5 - HBI – SPI Slave Port Pin Descriptions

The Master SPI port functions as the interface to an external Flash device used to optionally Auto Boot and load the device's firmware and configuration record from external Flash memory..

QFN Pin #	WLCSP Ball	Name	Type	Description
1	A5	SM_CLK	Output	**Master SPI Port Clock (Tristate Output).** Clock output for the Master SPI port. Maximum frequency = 8 MHz.
2	A6	SM_MISO	Input	**Master SPI Port Data Input.** Data input signal for the Master SPI port.
3	A7	SM_MOSI	Output	**Master SPI Port Data Output (Tristate Output).** Data output signal for the Master SPI port.
64	A4	GPIO_9/ $\overline{SM\_CS}$	Input/ Output	**Master SPI Port Chip Select (Input Internal Pull-Up/Tristate Output).** Chip select output for the Master SPI port. Shared with GPIO_9.

Table 6 - Master SPI Port Pin Descriptions

The ZL38050 device incorporates a two-wire UART (Universal Asynchronous Receiver Transmitter) interface with a fixed 115.2K baud transfer rate, 8 data bits, 1 stop and no parity. The UART port can be used as a debug tool and is used for tuning purposes.

QFN Pin #	WLCSP Ball	Name	Type	Description
50	B2	UART_RX	Input	**UART (Input).** Receive serial data in. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.
49	C2	UART_TX	Output	**UART (Tristate Output).** Transmit serial data out. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.

Table 7 - UART Pin Description

GPIO ports can be used for interrupt and event reporting, fixed function control, bootstrap options, as well as being used for general purpose I/O for communication and controlling external devices.

QFN Pin #	WLCSP Ball	Name	Type	Description
33, 34, 36	F4, E4, F3	GPIO_[0:2]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signalling.
37, 38, 39, 40, 41, 43	F2, –, F6, E5, E2, D3	GPIO_[3:8]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signalling. *GPIO_4 is not available on the WLCSP package.*
64	A4	GPIO_9/ SM_CS	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** This pin can be configured as an input or output and is intended for low-frequency signalling. Alternate functionality with SM_CS.
44, 45, 47, 48	E3, C3, –, –	GPIO_ [10:13]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signalling. *GPIO_12 and GPIO_13 are not available on the WLCSP package.*

Table 8 - GPIO Pin Descriptions

The oscillator pins are connected to a 12.000 MHz crystal or clock oscillator which drives the device's internal PLL. Alternatively, PCLK can be used as the internal clock source.

QFN Pin #	WLCSP Ball	Name	Type	Description
22	H7	XI	Input	**Crystal Oscillator Input.**
23	F5	XO	Output	**Crystal Oscillator Output.**

Table 9 - Oscillator Pin Description

QFN Pin #	WLCSP Ball	Name	Type	Description
17	–	EXT_SEL	Input	**VDD +1.2 V Select.** Select external +1.2 V supply. Tie to DVDD33 if the +1.2 V supply is to be provided externally. Tie to VSS (0 V) if the +1.2 V supply is to be generated internally. *Not available on the WLCSP package.*
16	–	VDD12_CTRL	Output	**VDD +1.2 V Control.** Analog control line for the voltage regulator external FET when EXT_SEL is tied to VSS. When EXT_SEL is tied to DVDD33, the VDD12_CTRL pin becomes a CMOS output which can drive the shutdown input of an external LDO. *Not available on the WLCSP package.*
4,14, 24,42, 58	B5, D1, G5, G6	DVDD12	Power	**Core Supply.** Connect to a +1.2 V ±5% supply. Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.
5, 21,35, 46,51, 59	B3, B7, G3	DVDD33	Power	**Digital Supply.** Connect to a +3.3 V ±5% supply. Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.
28	–	DVDD33_ XTAL	Power	**Crystal Digital Supply.** For designs using a crystal or external oscillator, this pin must be connected to a +3.3 V supply source capable of delivering 10 mA. For designs that do not use a crystal or external oscillator this pin can be tied to VSS in order to save power. *Not available on the WLCSP package.*
10,11	E7	AVDD33	Power	**Analog Supply.** Connect to a +3.3 V ±5% supply. Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.
20, 54, 60, 61, 62	B4, B6, C4, C5, D2, D4, D5, E6, G2, H2	VSS	Ground	**Ground.** Connect to digital ground plane.
	–	Exposed Ground Pad	Ground	**Exposed Pad Substrate Connection.** Connect to VSS. This pad is at ground potential and must be soldered to the printed circuit board and connected via multiple vias to a heatsink area on the bottom of the board and to the internal ground plane. *Not available on the WLCSP package.*

Table 10 - Supply and Ground Pin Description

QFN Pin #	WLCSP Ball	Name	Type	Description
25, 26, 27, 63	C6, G4, H4, H5	NC		**No Connection.** These pins are to be left unconnected, do not use as a tie point.

Table 11 - No Connect Pin Description

For more information about all Microsemi products visit our website at www.microsemi.com

TECHNICAL DOCUMENTATION – NOT FOR RESALE

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