Comparative Analysis of 150W RF VDMOS Transistors for 100MHz Applications

Introduction

Four RF transistors, all rated for 150W and commonly used for industrial applications up to 100MHz, are evaluated and compared, they are: BLF177 from NXP Semiconductors, SD2941-10 from STMicroelectronics, and VRF151 and VRF152 from Microsemi Corporation Power Products Group (MPPG).

The maximum ratings and key parameters of these transistors are first compared and discussed. For the RF performance, all four transistors are load-pulled at 100MHz using a common test fixture as well as the same load-pull system at MPPG to eliminate uncertainties due to various application circuits and variable test conditions.

Through the current studies, we strive to demonstrate that devices from MPPG not only outperform others, but that MPPG also offers higher voltage versions of otherwise very similar device, i.e., VRF151, which is more versatile than others by operating the device at higher voltage around 60V to 65V for higher output power capabilities, or at 45V to 50V for improved ruggedness and reliability at similar output power level as others.

Maximum Ratings of the RF VDMOS Transistors

Maximum ratings of the four RF transistors under study are listed in Table 1. The importance and implication of these ratings are discussed in details next.

Table 1 · Maximum rating table for the 150W RF VDMOS transistors under study.

Maximum Rating Table						
Symbols	**Unit**	**Description**	**VRF152**	**BLF177**	**SD2941-10**	**VRF151**
$V_{(BR)DSS}$	[V]	Drain-Source Breakdown Voltage	130	125	130	170
$I_{D,max}$	[A]	Continuous Drain Current	20	16	20	16
$P_{D,max}$	[W]	Total Power Dissipation	300	220	389	300
$T_{j,max}$	[°C]	Junction Temperature	200	200	200	200
$V_{GS,max}$	[V]	Gate-Source Voltage	±40	±20	±20	±40

Drain-Source Breakdown Voltage - $V_{(BR)DSS}$

$V_{(BR)DSS}$ is primarily determined by the dopant concentration in the starting epitaxial wafer, onto which the RF MOSFETs are fabricated. The performance of the transistor is strongly influenced by the choice of the starting epitaxial wafer in three areas: 1) drain-source turn-on resistance $R_{DS(on)}$, 2) operating voltage $V_{DD(op)}$, and 3) ruggedness and long-term reliability of the device.

$R_{DS(on)}$ increases with $V_{(BR)DSS}$, and decreases with increasing die size. Figure 1 depicts the typical normalized relationship between $R_{DS(on)}$ and $V_{(BR)DSS}$ for MOSFETs. The effect of $R_{DS(on)}$ on RF performance will be discussed in more details in the next section. In short, lower $R_{DS(on)}$ is desirable for higher output power and efficiency.

The operating voltage $V_{DD(op)}$ is highly influenced by the circuit topology as well as the circuit design. As a rule of thumb for Class-A, B, AB, and C operations, the operating voltage is generally kept around one third of $V_{(BR)DSS}$. Applying this empirical rule, the operating voltage for VRF152, BLF177, and SD2941-10 is generally recommended around 45V-50V, while for VRF151, it can be operated at 55V-65V. Higher operating voltage enjoys the benefit of delivering more output power to a fixed load.

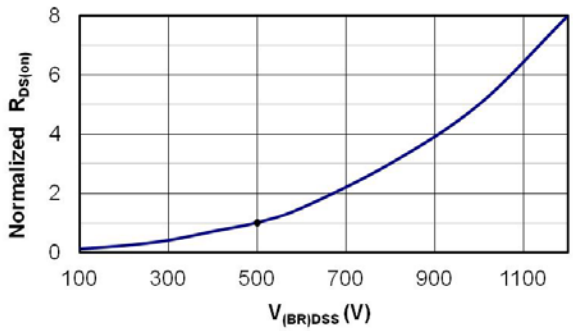

Figure 1 · Typical relationship between RDS(on) and V(BR)DSS normalized to 500V.

Device ruggedness is a measure of its survivability against mismatched loads, which results in elevated device junction temperature due to increased dissipation from reflected power. Although ruggedness and survivability are general, albeit vague terms, it is well understood that the device ruggedness can be improved by enhancing its thermal performance as well as lowering the operating output power into a fixed load - typically 50Ω. Thermal performance of the four transistors under study will be discussed in detail later.

In RF generator terminologies, the incident power is the power entering the load, of which some will be reflected back into the generator and the rest will be delivered to the load. If the generator and load are conjugate-matched, all the incident power will be delivered to such load. Since mismatched loads are often specified as the percentage reflection of the incident power, lowering the operating output power into the matched load effectively eases the severity of the mismatch specification, thus improves its ruggedness. For example, operating VRF151 at 60V offers 44% more output power (~216W) than operating the same device at 50V (~150W), therefore, for the same 33% reflection the reflected power are 70W vs. 50W for $V_{DD(op)}$ = 60V and 50V, respectively[1].

Devices with higher $V_{(BR)DSS}$ should be inherently more reliable as well if operated at the same operating voltage. This is due to the simple fact that the reverse breakdown of the MOSFET may weaken, or even destroy the device, and higher $V_{(BR)DSS}$ allows more headroom against voltage excursion caused by some uncontrollable events during operation. Therefore, VRF151 offers better long-term reliability than the others when operated at the same 45V to 50V.

In summary, the four RF transistors under study can be categorized into two groups by their recommended operating voltages: (A) $V_{DD(op)}$ = 45V-50V for VRF152, BLF177 and SD2941-10, and (B) $V_{DD(op)}$ = 45V-65V for VRF151. RF MOSFET with lower $V_{(BR)DSS}$ typically comes with lower $R_{DS(on)}$, while higher $V_{(BR)DSS}$ affords higher operating voltage as well as more rugged and reliable than devices with lower $V_{(BR)DSS}$.

Maximum Continuous Drain Current - $I_{D,max}$

All four RF transistors under study belong to a special class of MOSFET called vertical, doubly-diffused MOS, or VDMOS. The maximum current rating of a VDMOS transistor, $I_{D,max}$, is limited mostly by die size and $R_{DS(on)}$, and to a lesser extent, influenced by the device structure, layout design and fabrication processes. In fact, $R_{DS(on)}$ and die size are interdependent as $R_{DS(on)}$ goes down with increasing die sizes. Since $I_{D,max}$ is determined by running the MOSFET continuously, the self-heating effect is unavoidable such that the strong dependency of $R_{DS(on)}$ vs. temperature has to be taken into consideration. As shown in Figure 2, there is about 20% increase in $R_{DS(on)}$ for every 25°C temperature rise. If we neglect all the other factors except $R_{DS(on)}$ and $P_{D,max}$, $I_{D,max}$ can be estimated by running the transistor at rated power dissipation up to its rated temperature as

(1) $$\mathbf{I_{D,max}} = \sqrt{\frac{\mathbf{P_{D,max}}}{\mathbf{R_{DS(on)}(T_j = 200^o C)}}}$$

[1] *Ruggedness specifications are highly application dependent, examples of commonly adopted specifications are 1) withstand 33% reflection at full rated (incident) power for 10 minutes over all phase angles, and/or 2) withstand total (99%) reflection at 33% of rated (incident) power for 10 minutes over all phase angles. Note that the rated incident power becomes the rated output power into a matched load, and the phase angle specifies inductive or capacitive load conditions.*

where $R_{DS(on)}$ at T_j = 200°C can be estimated from Figure 2, i.e., $R_{DS(on)}$ increases 3.6 times from 25°C to 200°C. Table 2 lists both the estimated and reported $I_{D,max}$ values for the four transistors under study, which shows that Equation (1) is fairly accurate in predicting $I_{D,max}$ for MPPG devices since the temperature scaling factor of 3.6 is specific to MPPG's VDMOS technologies, while it understates BLF177's and overstates SD2941-10's temperature scaling factors. In fact, the temperature scaling factors can be estimated from the reported $I_{D,max}$ values for BLF177 and SD2941-10, respectively, as 16% and 25% increase in $R_{DS(on)}$ for every 25°C temperature rise, or factors of 2.9 and 4.9, respectively, from 25°C to 200°C.

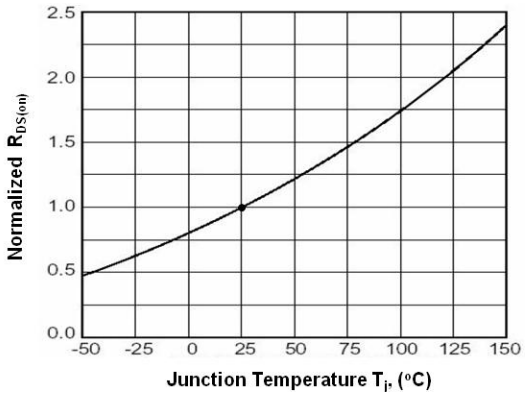

Figure 2 · Typical normalized relationship between RDS(on) and junction temperature Tj.

Table 2 · Reported and estimated ID,max by Equation (1).

Parameters	Unit	VRF152	BLF177	SD2941-10	VRF151
$P_{D,max}$ (from Table 1)	[W]	300	220	389	300
$R_{DS(on)}$ @25°C (from Table 4)	**[Ω]**	0.2	0.3	0.2	0.3
$R_{DS(on)}$ @200°C	**[Ω]**	0.72	1.08	0.72	1.08
$I_{D,max}$, Estimated	[A]	20.4	14.3	23.2	16.7
$I_{D,max}$, Reported	[A]	20	16	20	16

It is interesting to note that A) The difference in $I_{D,max}$ between VRF152 and VRF151 is mostly due to $R_{DS(on)}$, which can be attributed to the difference in breakdown voltages, $V_{(BR)DSS}$; and B) Although VRF152 and BLF177 have similar $V_{(BR)DSS}$, the fact that BLF177 has lower $I_{D,max}$ due to higher $R_{DS(on)}$ can be explained by its smaller die size, which will be discussed in more detail in the next section.

Total Power Dissipation - $P_{D,max}$

Total power dissipation is derived from two other parameters, they are: the maximum junction temperature $T_{j,max}$ and the junction-to-case thermal resistance of the device $R_{\theta JC}$. Conventionally, the package case temperature of 25°C is assumed in such calculation. By definition, the total power dissipation can be expressed as

(2) $$P_{D,max} = (T_{j,max} - 25^{o}C)/R_{\theta JC}$$

The estimated and reported $P_{D,max}$ for the four transistors under study are listed in Table 3 confirming that Equation (2) is the formula used in deriving the power rating. In short, all four transistors have ample thermal capabilities to dissipate partially or totally reflected power at 150W.

It should be noted that SD2941-10 uses a more expensive version of the SOE[2] package, i.e., the thermally enhanced M174 package, which is available to the other two manufacturers as well, who have deemed it unnecessary to further enhance the thermal capabilities of the device with the added costs. Finally, the 26% higher thermal capability of VRF152 compared to BLF177 can be attributed to the die size difference between these two devices, which will be discussed in the next section.

Table 3 · Reported and estimated PD,max by Equation (2).

Parameters	Unit	VRF152	BLF177	SD2941-10	VRF151
$T_{j,max}$ (from Table 1)	[°C]	200	200	200	200
$R_{\theta JC}$ (from Table 4)	[°C/W]	0.6	0.8	0.45	0.6
$P_{D,max}$, Estimated	[W]	292	219	389	292
$P_{D,max}$, Reported	[W]	300	220	389	300

Maximum Gate-Source Voltage - $V_{GS,max}$

$V_{GS,max}$ is a measure of the dielectric strength of the gate oxide against large gate voltage excursions. Higher $V_{GS,max}$ rating implies more rugged gate oxide construction. It is no accident that devices from MPPG are rated for the highest gate-source voltage in both polarities since MPPG's core strength is in high-voltage VDMOS device design and construction. In fact, MPPG is the only supplier among the three manufactures of VDMOS transistors, who also offers RF MOSFETs with 500V to 1200V breakdown voltages in its ARF family of transistor products.

It should be noted that it is not uncommon for a VDMOS transistor to experience a large voltage excursion at its gate during operation due to the feedback coupling capacitance, C_{rss}, which will be discussed in the next section. Therefore, higher $V_{GS,max}$ is desirable for additional headroom against such voltage excursions.

Key Parameters of the RF VDMOS Transistors

As part of the current analysis, transistor samples are first de-capsulated, and their die sizes are measured as shown in Figure 3. Since the die sizes and wire-bonding schemes of VRF151 and VRF152 are identical, only VRF152 is de-capsulated and shown. As seen from Figure 3, BLF177 has the smallest die area, followed by SD2941-10 and VRF151/VRF152. Also interesting to note is that BLF177 employs two MOSFET dies, while a single die is used in both SD2941-10 and VRF151/VRF152, respectively.

Table 3 lists the key parameters of the four RF transistors under study along with test conditions, under which these parameters were measured. It should be noted that common test conditions are listed in Table 3 unless they are tested under different conditions. Finally, only NXP reports $R_{DS(on)}$ directly on the datasheet, while $V_{DS(on)}$ is reported by MPPG and STMicroelectronics, which are then converted to $R_{DS(on)}$ by taking the ratio of $V_{DS(on)}$ and the fixed sensing drain current I_D.

Gate-Source Threshold Voltage - $V_{GS(th)}$

$V_{GS(th)}$ and $R_{DS(on)}$ are two of the most important parameters to consider if multiple MOSFETs are paralleled in an application for higher output power capacities. As shown in Figure 4, the gate-source threshold voltage of these RF MOSFETs decreases with increasing temperature, or a negative temperature coefficient, below the crossover point. If a few of these MOSFETs are paralleled in the application, the negative temperature coefficient promotes thermal runaway, i.e., a hotter device would be turned on more easily than others resulting in uncontrollable self-destruction.

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[2] ***S**tripline **O**pposed **E**mitter (SOE) Package - Originally developed by Motorola for bipolar transistors, SOE packages provides low inductance leads, which interfaces well with microstrip lines on circuit boards or substrates. The two emitter leads provide good collector-to-base isolation, as well as promote symmetry in board layout when combining devices to obtain higher output power. This package is also widely adopted for power MOSFETs with gate and drain leads in the place of base and collector leads, respectively, and two source leads in the place of emitter leads. There are two SOE package types, namely, stud-mounted and flange-mounted packages. Only the flange-mounted SOE packages are discussed in this Application Note.*

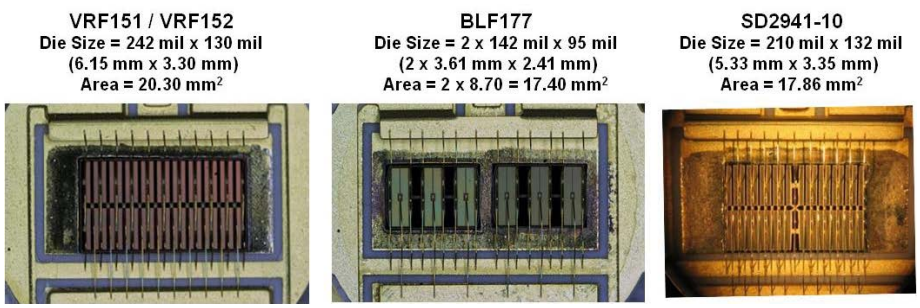

Figure 3 · De-capsulated RF VDMOS transistors under study with measured die sizes.

Table 4 · Key parameters table of the 150W RF VDMOS transistors under study.

Key Parameters Table								
Sym	**Unit**	**Description**		**VRF152**	**BLF177**	**SD2941-10**	**VRF151**	**Test Conditions**
A	[mm^2]	Die Size	Typ.	20.30	17.40	17.86	20.30	
$V_{GS(th)}$	[V]	Gate-Source Threshold Voltage	Min.	2.9	2.0	1.5	2.9	MSC: V_{DS} = 10V; I_D = 100mA. NXP: V_{DS} = 10V; I_D = 50mA. ST: V_{DS} = 10V; I_D = 250mA.
			Typ.	3.6			3.6	
			Max.	4.4	4.5	4.0	4.4	
$R_{DS(on)}$	[Ω]	Drain-Source On-State Resistance	Typ.	0.13	0.20		0.20	MSC/ST: V_{GS} = 10V; I_D = 10A. NXP: V_{GS} = 10V; I_D = 5A.
			Max.	0.20	0.30	0.20	0.30	
g_{fs}	[S]	Forward Transconductance	Min.	5.0	4.5	5.0	5.0	V_{DS} = 10V; I_D = 5A.
			Typ.	6.2	6.2	6.0		
I_{DSS}	[mA]	Drain-Source Leakage Current	Max.	0.05	2.5	0.05	1.0	MSC: V_{GS} = 0V; V_{DS} = 100V. NXP/ST: V_{GS} = 0V; V_{DS} = 50V.
I_{GSS}	[μA]	Gate-Source Leakage Current	Max.	1.0	1.0	0.25	1.0	MSC/NXP: V_{DS} = 0V; V_{GS} = ±20V. ST: VDS = 0V; VGS = 20V.
C_{iss}	[pF]	Input Capacitance	Typ.	383	480	415	375	V_{GS} = 0V; V_{DS} = 50V; f = 1MHz.
C_{oss}	[pF]	Output Capacitance	Typ.	215	190	236	200	V_{GS} = 0V; V_{DS} = 50V; f = 1MHz.
C_{rss}	[pF]	Reverse Transfer Capacitance	Typ.	20	14	17	12	V_{GS} = 0V; V_{DS} = 50V; f = 1MHz.
$R_{\theta JC}$	[°C/W]	Junction to Case Thermal Resistance	Max.	0.6	0.8	0.45	0.6	
f_T	GHz	Cutoff Frequency	Typ.	1.8	1.3	1.6	1.9	V_{DS}=10V (C_{iss}' are scaled to 10V)

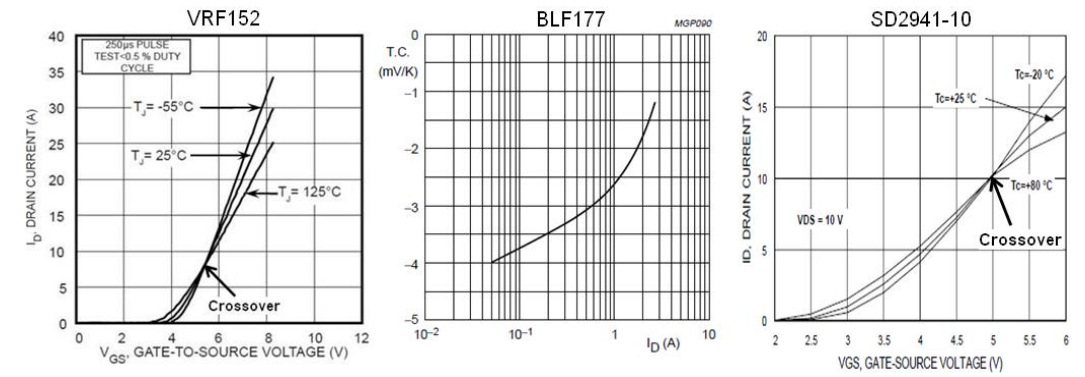

Figure 4 · Temperature dependency of the transfer characteristics.

It is desirable to have the crossover point at a lower drain current for a wider range of thermal stability in paralleled configurations. Among the four RF transistors under study, VRF151 and VRF152 have the lowest crossover point at about 8A compared to 10A for SD2941-10. Since only temperature coefficient is reported on BLF177's datasheet up to about 2.5A, it is too far away for accurate extrapolation to the point of vanishing temperature coefficient.

All four RF transistors can be ordered in matched $V_{GS(th)}$ groups, or bins, and their grouping and marking information are provided in Table 4. It is seen that VRF151 and VRF152 have the narrowest range of $V_{GS(th)}$ and the best group spacing, they are: 1.5V and 0.075V, respectively, while for BLF177 and SD2941-10, are 2.5V and 0.1V, respectively. Again, the narrower range and finer grouping of $V_{GS(th)}$ are both highly desirable when transistors are paralleled in the application.

Table 5 · VGS(th) grouping and marking codes for the RF VDMOS transistors under study.

$V_{GS(th)}$ Binning Group/Code																						
VRF151 / VRF152 (20 Bins, 0.075V Spacing)						BLF177 (25 Bins, 0.1V Spacing)						SD2941-10 (25 Bins, 0.1V Spacing)											
Bin	Range [V]		Bin	Range [V]		Bin	Range [V]		Bin	Range [V]		Bin	Range [V]		Bin	Range [V]		Bin	Range [V]			
A	2.900	2.975	R	3.875	3.950	A	2.00	2.10	O	3.30	3.40	AA	1.50	1.60	J	2.80	2.90					
B	2.975	3.050	S	3.950	4.025	B	2.10	2.20	P	3.40	3.50	BB	1.60	1.70	K	2.90	3.00					
C	3.050	3.125	T	4.025	4.100	C	2.20	2.30	Q	3.50	3.60	CC	1.70	1.80	L	3.00	3.10					
D	3.125	3.200	W	4.100	4.175	D	2.30	2.40	R	3.60	3.70	DD	1.80	1.90	M	3.10	3.20					
E	3.200	3.275	X	4.175	4.250	E	2.40	2.50	S	3.70	3.80	EE	1.90	2.00	N	3.20	3.30					
F	3.275	3.350	Y	4.250	4.325	F	2.50	2.60	T	3.80	3.90	A	2.00	2.10	P	3.30	3.40					
G	3.350	3.425	Z	4.325	4.400	G	2.60	2.70	U	3.90	4.00	B	2.10	2.20	Q	3.40	3.50					
H	3.425	3.500				H	2.70	2.80	V	4.00	4.10	C	2.20	2.30	R	3.50	3.60					
J	3.500	3.575				J	2.80	2.90	W	4.10	4.20	D	2.30	2.40	S	3.60	3.70					
K	3.575	3.650				K	2.90	3.00	X	4.20	4.30	E	2.40	2.50	T	3.70	3.80					
M	3.650	3.725				L	3.00	3.10	Y	4.30	4.40	F	2.50	2.60	U	3.80	3.90					
N	3.725	3.800				M	3.10	3.20	Z	4.40	4.50	G	2.60	2.70	V	3.90	4.00					
P	3.800	3.875				N	3.20	3.30				H	2.70	2.80								

Drain-Source On-State Resistance - $R_{DS(on)}$

It has been discussed in the last section that $R_{DS(on)}$ increases with $V_{(BR)DSS}$ and temperature, see Figure 1 and Figure 2, respectively; and decreases with die size. The relationship between $R_{DS(on)}$ and die size can also be influenced by the design as well as fabrication processes of the device. The $R_{DS(on)}$-$V_{(BR)DSS}$ trend can be seen clearly between VRF152 and VRF151 with different breakdown voltages. The lower $R_{DS(on)}$ of VRF152 compared to BLF177 reflects its bigger die size, while no such trend is observed between VRF152 and SD2941-10.

Discussed in the last section, $R_{DS(on)}$ is the determining factor for the current capacity of the device. As predicated by Equation (1), VRF152 and SD2941-10 both have higher current capability of 20A, while VRF151 and BLF177 are rated 4A lower due to their higher $R_{DS(on)}$.

Finally, It is interesting to note that VRF151 has the same $R_{DS(on)}$ as BLF177, while VRF151's $V_{(BR)DSS}$ is much higher than BLF177. Taking VRF151's lower $R_{\theta JC}$ into consideration, which will be discussed shortly, it implies that VRF151 can be operated at higher drain voltages for higher output power without compromising the long-term reliability of the device.

Forward Transconductance - g_{fs}

The forward transconductance, g_{fs}, is a static parameter determined by measuring the rate of change in drain current in response to the change in gate voltage at fixed drain-source voltage and drain current. It can be shown that there is a positive correlation between g_{fs} and the RF gain. Since RF gain depends on the application circuit as well as test conditions, it will be discussed in more detail when load-pull results are presented in the next section. For practical purposes, the forward transconductance of the four RF VDMOS transistors under study are very similar with the exception of BLF177, whose minimum g_{fs}, is 10% lower than the other three.

Leakage Currents - I_{GSS} & I_{DSS}

The gate-source leakage current I_{GSS}, measured in μA, are all very small for 150W power transistors, and the slightly smaller value for SD2941-10 really offers no measurable benefit in typical applications.

The differences in drain-source leakage currents, measured in mA, on the other hand, are not so subtle with BLF177 being 50 times more leaky than VRF152 and SD2941-10. More importantly, recognizing that drain-source leakage current grows exponentially with drain-source voltage, the I_{DSS} of VRF152 is measured at a V_{DS} of 100V, while both BLF177 and SD2941-10 are measured at 50V, therefore, VRF152 has the lowest I_{DSS} among the three RF transistors with similar $V_{(BR)DSS}$, and BLF177 is about two orders of magnitude more leaky than VRF152.

Input, Output and Reverse Transfer Capacitances - C_{iss}, C_{oss} & C_{rss}

As discussed in Appendix A, the capacitances of a VDMOS device can be represented by: (A) the terminal capacitances, C_{gs}, C_{ds} and C_{gd} commonly used in circuit analysis; (B) the measurable capacitances, C_{iss}, C_{oss} and C_{rss}; or (C) the physical capacitances, C_{ox1}, C_{ox2}, C_{drift} and C_{body}. The terminal and physical capacitances are illustrated in Figure 5.

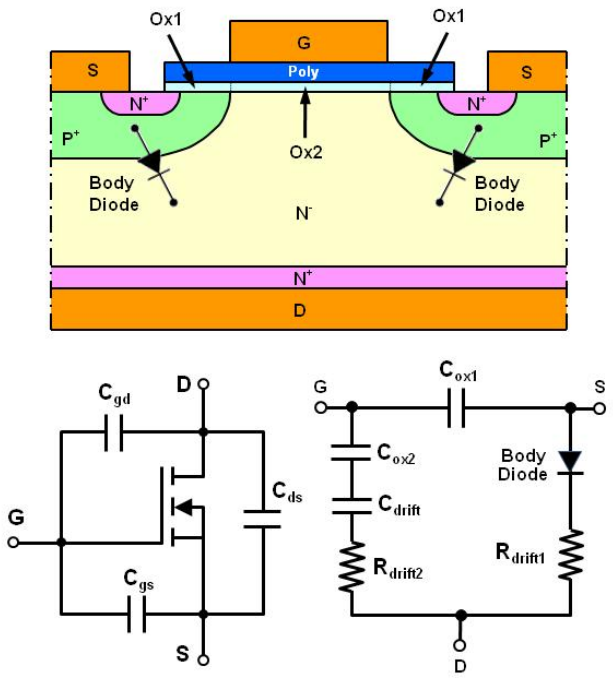

Figure 5 · Terminal and physical capacitances of a VDMOS device.

The terminal capacitances can be expressed in terms of measurable capacitances as well as physical capacitances such as

(3) $$\mathbf{C_{gs} = C_{iss} - C_{rss} = C_{ox1}}$$

(4) $$\mathbf{C_{ds} = C_{oss} - C_{rss} = C_{body}}$$

(5) $$\mathbf{C_{gd} = C_{rss} = \left(\frac{1}{C_{ox2}} + \frac{1}{C_{drift}} \right)^{-1}}$$

The gate-source capacitance, C_{gs}, is the capacitance of the gate oxide (ox1), which needs to be charged to turn on the MOSFET. C_{gs} can be readily obtained by subtracting C_{rss} from C_{iss}. The drain-source capacitance, C_{ds}, is the junction capacitance of the body diode, whose reverse breakdown voltage determines the drain-source breakdown voltage $V_{(BR)DSS}$ of the MOSFET. It should be noted that C_{gs} is relatively independent of the drain-source bias voltage V_{DS}, while C_{ds} strongly depends on V_{DS}. Similarly, C_{ds} is readily calculated by subtracting C_{rss} from C_{oss}. In amplifier operation, C_{ds} is seen as the reactance of its output impedance.

The gate-drain capacitance, C_{gd}, is the same capacitance as C_{rss} as measured, which consists of the stacked capacitances of the gate oxide (ox2) and the capacitance due to the space charge in the drift region under bias conditions. The gate-drain capacitance, C_{gd}, or the reverse transfer capacitance, C_{rss}, plays dual roles in the operation of the MOSFET: (A) it is the augmented "Miller" capacitance during turn-on of the MOSFET; and (B) it is responsible for the feedback or coupling between the input and output terminals of the MOSFET in a common-source configuration.

As shown in Figure 6, there are three distinctive segments in the charging curve of a typical MOSFET. The corresponding transients of gate-source voltage, drain-source voltage and current are also illustrated in the Figure 6. At t=0, the drain is already positively biased, and a constant gate voltage is suddenly connected to the gate with common source ground. Reacting to the applied gate signal, the gate-source voltage, V_{GS}, rises at a constant rate until t2. Within this period, V_{GS} first passes the threshold voltage $V_{GS(th)}$, hereafter the drain-source current increases rapidly from t1 to t2, while the drain-source voltage V_{DS} drops only slightly during the same period. During t2, both C_{gs} and C_{gd} are charged to the total amount of Q_{gs} until the so-called "Miller" plateau is reached at t2. Since C_{gs} is typically much larger than C_{gd}, most of charge goes to C_{gs} before t2.

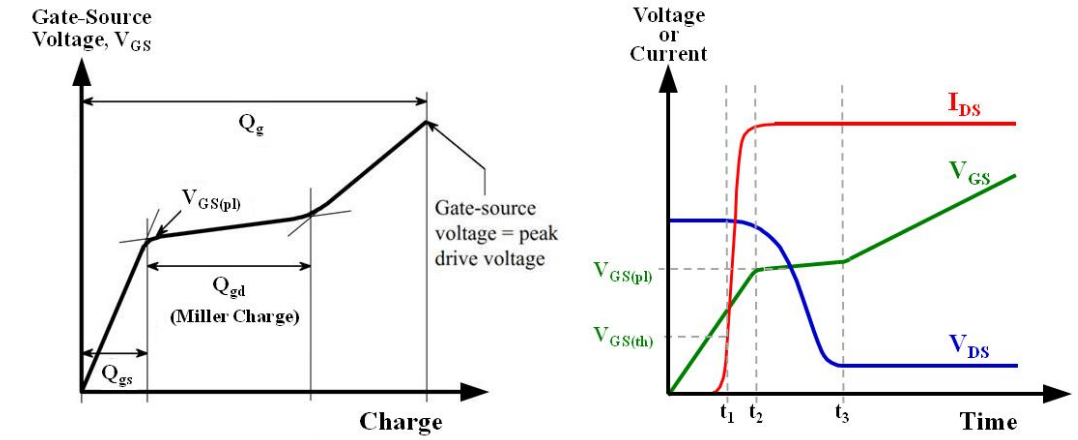

Figure 6 · Transient behavior and Miller effect during turn-on of MOSFET.

The Miller effect simply states that the coupling impedance between the input and output of a voltage amplifier is augmented by the gain of itself. As seen in Figure 6, the gain of the MOSFET reaches its peak at t2 when I_{DS} reaches its saturation point. At this point, C_{gd} begins its rapid ascension due to the Miller effect. It is this rapid rate of changing capacitance that results in a sudden increase in the observed capacitance at the gate, which is reflected by the gentler slope in the charging curve since the capacitance is inversely proportional to the slope of the charging curve. The partition of charge also reverses during this period since it is the rate of changing capacitance that dictates the draw of charge such that most charge is injected into C_{gd}.

The Miller plateau ends when the drain-source voltage reaches its on-state value, which is set by the product of I_{DS} and the on resistance of the MOSFET $R_{DS(on)}$. Beyond t3, the gain of the MOSFET saturates and no more increase of C_{gd} is possible such that the total capacitance seen at the gate is again the sum of two constant capacitances C_{gs} and C_{gd}, albeit a larger C_{gd} than before, thus a less steep slope.

In amplifier operation, the coupling between input and output is highly undesirable since it serves as a negative feedback resulting in less gain of the device, or "making it harder to drive", i.e., more input power and current are required for the same output power.

In summary, the desirable attributes of RF MOSFET capacitances include: (A) low C_{iss} (C_{gs}+C_{gd}) for fast turn-on, (B) low C_{rss} (C_{gd}) for less pronounced Miller effect as well as less negative feedback, and (C) low C_{ds} (C_{oss}-C_{rss}) for smaller size of output matching inductor or transformer.

The measurable capacitances of the four RF VDMOS transistors under study are plotted against the drain-source voltage in the same scale for clear comparison in Figures 7 and 8. Ranking of the measurable capacitances from the lowest to the highest values are: (A) C_{iss} - VRF151, VRF152, SD2941-10, and BLF177, (B) C_{oss} - BLF177, VRF151, VRF152, and SD2941-10, C) C_{rss} - VRF151, BLF177, SD2941-10, and VRF152.

The most significant differences among these four RF VDMOS transistors are: A) BLF177's C_{iss} is the worst by a large margin; B) To a less extent, SD2941-10 has the largest C_{oss} and VRF152 has the largest C_{rss}, and C) VRF151 ranks first in both C_{iss} and C_{rss} and second in C_{oss}.

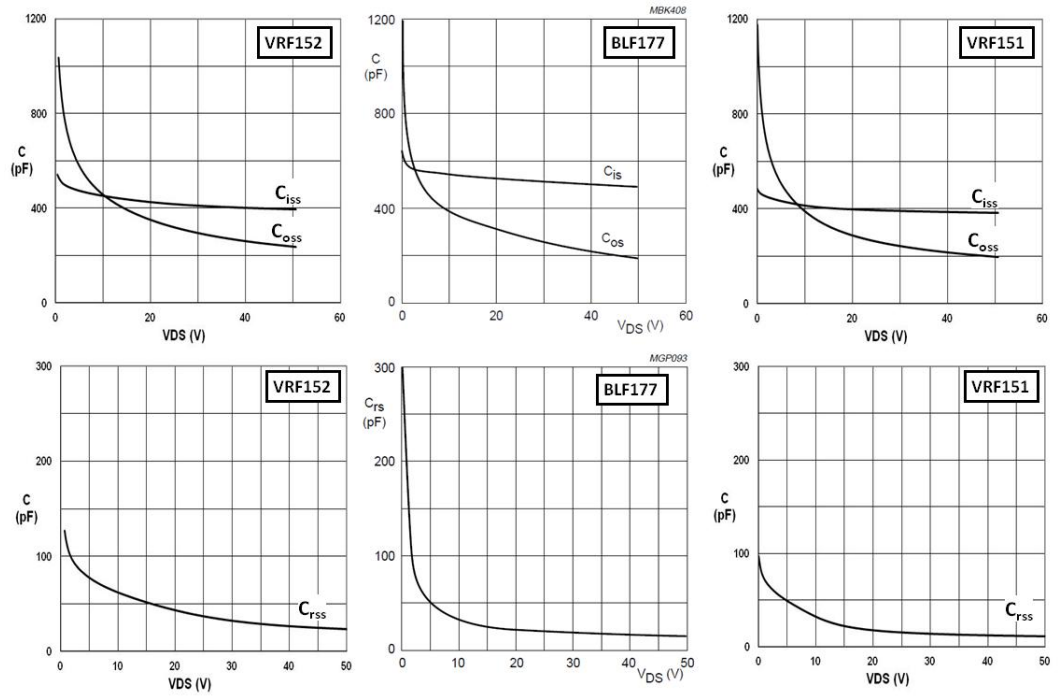

Figure 7 · Comparison of measurable capacitances between VRF152, BLF177 and VRF151.

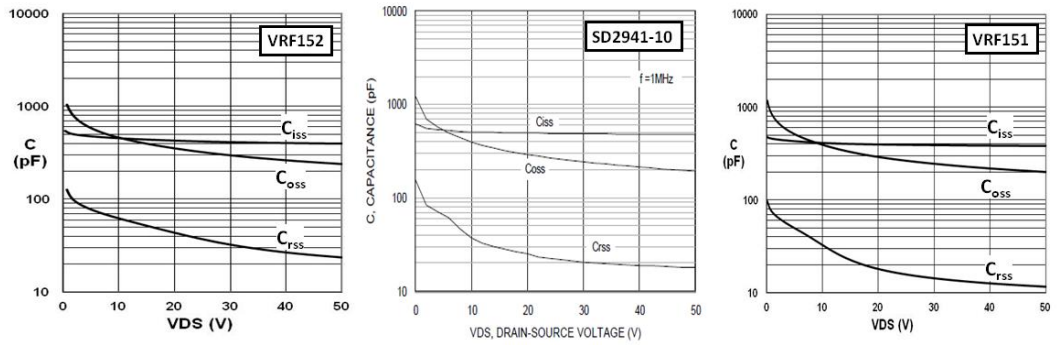

Figure 8 · Comparison of measurable capacitances between VRF152, SD2941-10 and VRF151.

Junction-to-Case Thermal Resistance - $R_{\theta JC}$

The junction-to-case thermal resistance is the limiting factor for the maximum power dissipation of the device, and is mostly determined by the properties of the material stack including the MOSFET and packaging materials. More specifically, the junction-to-case thermal resistance is the sum of the thermal resistance of each layer in the material stack such as

(6) $$\mathbf{R_{\theta JC}} = \sum_{\mathbf{i}} \frac{\mathbf{d_i}}{\mathbf{A_i k_i}}$$

where di, Ai and ki are, respectively, the thickness, area and thermal conductivity of the i^{th} layer in the material stack.

The same M174 package is adopted in VRF151, VRF152 and BLF177, while a thermally enhanced version of M174 is used for SD2941-10. As seen in Table 4, BLF177's $R_{\theta JC}$ is 33% larger than VRF151 and VRF152, which is mostly due to the difference in die sizes. SD2941-10 has a similar die size as BLF177, whose smaller thermal resistance is mostly due to the thermally enhanced, and a more expensive version of the M174 package. In fact, MPPG used to offer VRF151E, which adopts the same thermally enhanced M174 package. VRF151E has been obsoleted from MPPG's RF product offering since the power dissipation of the regular VRF151 is more than adequate in most applications, and the added cost could not be justified.

Transistor Cutoff Frequency - f_T

The cutoff frequency of a MOSFET is defined as the frequency at which its current gain becomes unity, or 0dB, and can be expressed as

$$\mathbf{f_T = \frac{g_{fs}}{2\pi\left(C_{gs} + C_{gd}\right)} = \frac{g_{fs}}{2\pi C_{iss}}} \quad (7)$$

Intuitively, (A) a higher starting gain at lower frequency is one of the prevailing conditions for higher fT, and the forward transconductance gfs is closely related to current gain at DC, and (B) the input capacitance C_{iss} limits fT since it takes longer to charge up a larger C_{iss} to turn on the MOSFET. From Table 4, it is seen that VRF151 and VRF152 have the highest fT at 1.9GHz and 1.8GHz, respectively, and BLF177's fT is the lowest at 1.3GHz.

RF Performance of the VDMOS Transistors

The RF performance of the four VDMOS transistors under study are evaluated and compared using the same load-pull system in a common water-cooled test fixture as shown in Figure 9. This load-pull system consists of a source tuner (LFT-013006 from Focus Microwave, 60-130MHz) and a load tuner (CCMT-101 also from Focus Microwave, 0.1-1.1GHz), which are both automatically controlled by software supplied by Focus Microwave. The load-pull test fixture comprises a socket for the M174 package, biasing circuit, quarter-wave transmission-line pre-matching circuits at both input (gate) and output (drain) terminals of the transistor, and N-type input and output connectors. The text fixture PCB is directly mounted on a copper heat-sink with forced cooling by a chiller. A thin layer of thermal grease is first applied onto the heat-sink surface in the M174 socket, and the DUT is then mounted onto the socket by mounting screws. Before the insertion of a new DUT, the residual grease in the socket is thoroughly wiped clean, and the grease application and DUT mounting are carefully carried out for consistency. The quarter-wave pre-match circuits are used to increase the impedance at the tuner for better accuracy, and their circuit contribution is de-embedded during the calibration of the load-pull system.

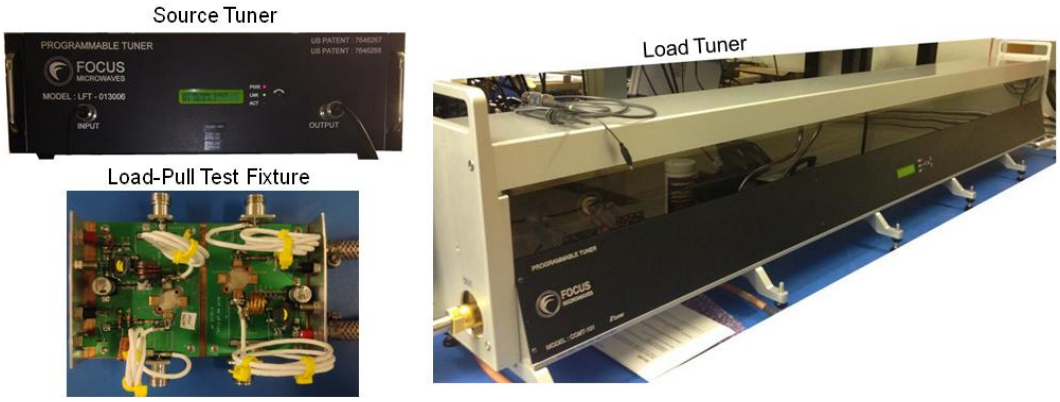

Figure 9 · The load-pull system and test fixture used in assessing the RF performance of the four RF VDMOS transistors under study.

In a fully automated load-pull system, the source and load tuners can be adjusted to search for impedance states that meet the preset load-pull objective. The load-pull objective can be a simple one such as the optimal states for (A) output power, (B) gain, (C) efficiency, or (D) linearity. If the load-pull objective is set loosely, e.g., setting output power below the maximum saturated power, multiple impedance states can be found, which forms a contour on the input and output Smith Charts. On the other hand, no impedance state will be found if the objective is set beyond the capability of the device. By setting the load-pull objective closer and closer to the capability of the device, these load-pull contours shrink to a single point, which represents the optimal impedance states for such objective. Composite load-pull object is also possible by assigning weights to the four simple objectives above. Finally, the source and load tuners are adjusted separately and iteratively with one tuner at a fixed impedance when the other is being adjusted until the desired impedance states are found.

The First Load-Pull Experiment - $P_{o,max}$ & PAE > 65%

In the first load-pull experiment, the load-pull objective is set for optimal output power with a minimum power added efficiency (PAE) of 65%. Two units of each of the four transistors under study are load-pulled at 100MHz in pulsed mode with 50% duty cycle, and cooled by water at 25°C. It should be noted that the impedance states are conventionally reported in terms of the input impedance of the transistor and load impedance presented to the transistor during load-pull. Table 6 lists the load-pull results of the first experiment for each of the two units of the four RF VDMOS transistors under study. Also listed in Table 6 are the average impedances of the two units of the four RF VDMOS transistors.

Table 6 · Optimal impedance states of the first load-pull experiment.

$P_{o,max}$/PAE > 65%		Z_{in}	Z_L
VRF151	DUT1	4.05 - j6.11	1.76 + j3.80
	DUT2	4.05 - j6.11	2.08 + j3.68
	AVE	4.05 - j6.11	1.92 + j3.74
VRF152	DUT1	2.86 - j6.71	2.13 + j3.93
	DUT2	2.86 - j6.71	2.13 + j3.93
	AVE	2.86 - j6.71	2.13 + j3.93
BLF177	DUT1	3.62 - j5.02	2.13 + j3.93
	DUT2	3.62 - j5.00	2.13 + j4.00
	AVE	3.62 - j5.00	2.13 + j3.97
SD2941-10	DUT1	4.14 - j6.07	2.23 + j3.47
	DUT2	4.14 - j6.07	2.23 + j3.47
	AVE	4.14 - j6.07	2.23 + j3.47

Power sweep experiments are also performed for each of the eight transistors at their respective optimal impedance states as listed in Table 6. Figures 10-12 show, respectively, the results of power sweep, gain vs. output power, and PAE vs. output power between VRF151/VRF152 and BLF177/SD2941-10. Key observations from the first load-pull experiment are in order:

(1) The RF performance of VRF152 and BLF177 closely resemble each other with noticeable difference in input impedance Z_{in} and slightly higher and flatter gain of VRF152 than BLF177.

(2) The RF performance of VRF151 and BLF177 closely resemble each other as well with noticeable difference in input impedance Z_{in}, slight difference in load impedance Z_L, and slightly higher gain and PAE of BLF177 than VRF151.

(3) The gain of SD-2941-10 is significantly lower as well as least flat among the four VDMOS transistors under study.

The variations in the resulting optimal load-pull impedance between two units of the same transistor is most significant in the load impedance of VRF151, however, the variations in power sweep results between the two units of the same transistor with similar optimal load-pull impedances are almost as significant as the former.

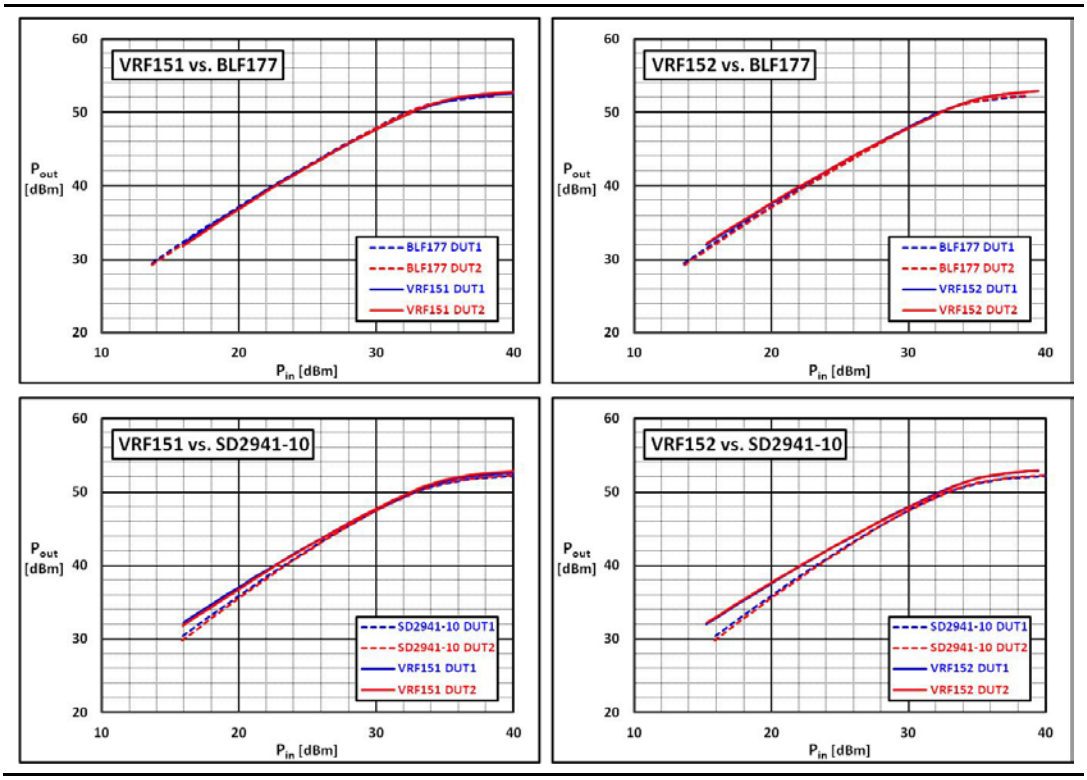

Figure 10 · Power sweep results of VRF151, VRF151, BLF177 and SD2941-10.

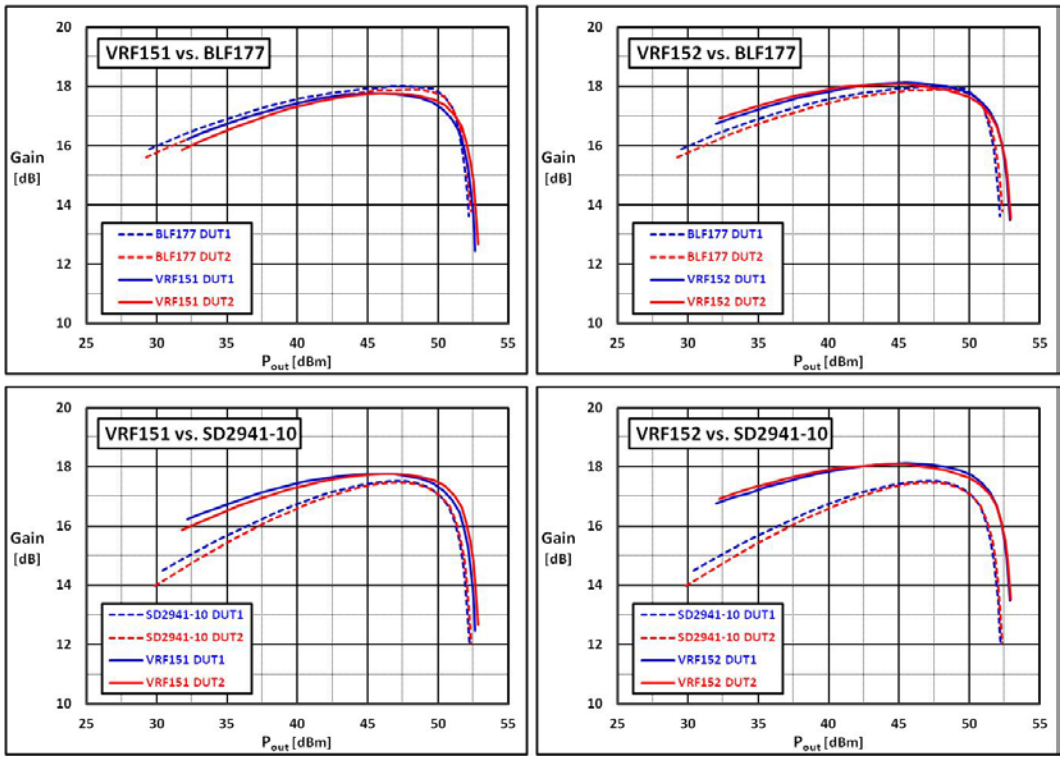

Figure 11 · Gain vs. output power results of VRF151, VRF152, BLF177 and SD2941-10.

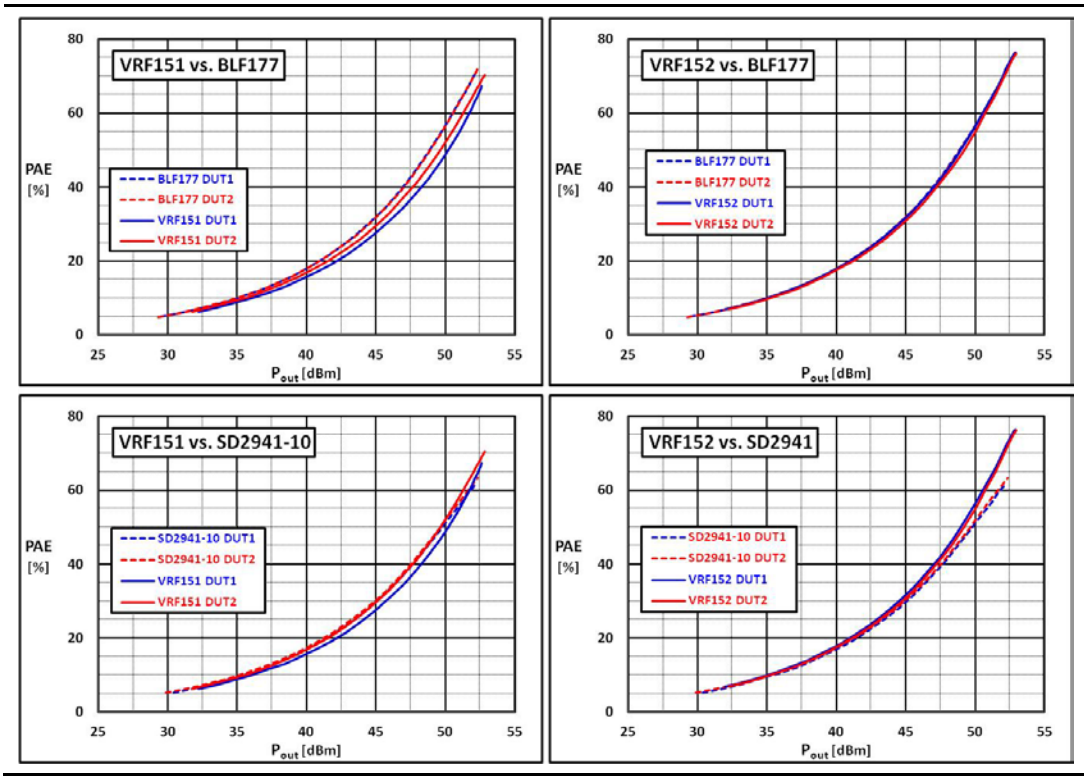

Figure 12 · PAE vs. ouptut power results of VRF151, VRF152, BLF177, and SD2941-10.

From the first load-pull experiment, it is seen that VRF151, VRF152 and BLF177 are interchangeable in a given RF power generator design since the load impedances are very close. The input impedances are noticeably different among these three transistors, which may impact the stability performance if one transistor is dropped into the circuit designed and optimized for another. Therefore, it is recommended that the input matching circuit be modified when replacing an incumbent transistor with another. The best way to assess the required circuit modification for a drop-in replacement is to examine the input and output matching circuits from de facto 50Ω standard to the input and output impedances of the transistors of interest.

Adopting the most simplistic L-network matching circuit, Figure 13 shows the input matching circuit design for the four transistors under consideration using the ADS simulator from Keysight (Agilent) Technologies, and Figure 14 shows the frequency responses of the input matching circuits. It should be noted that the quality (Q) factor for the inductors and capacitors used in the circuit simulation are, respectively, 50 and 250.

The input matching circuit parameters along with the insertion loss of the matching circuit at 100MHz are listed in Table 7. It is clear that the same input matching topology can be used for all the four transistors, while the optimal circuit parameters differ by 10% in inductance and 21% in capacitance.

The output matching circuits for all four transistors are also analyzed similarly using the L-network as the matching circuit. Figure 15 shows the output matching circuit design using the ADS simulator, and Figure 16 shows the frequency responses of the output matching circuits. Under the same matching topology, the output matching circuit parameters along with the insertion loss of the matching circuit at 100MHz are listed in Table 8. These output circuit matching parameters only differ by about 6% to 7% among the four transistors reflecting the fact that the optimal load impedances from the first load-pull experiment are very close among the four transistor under study.

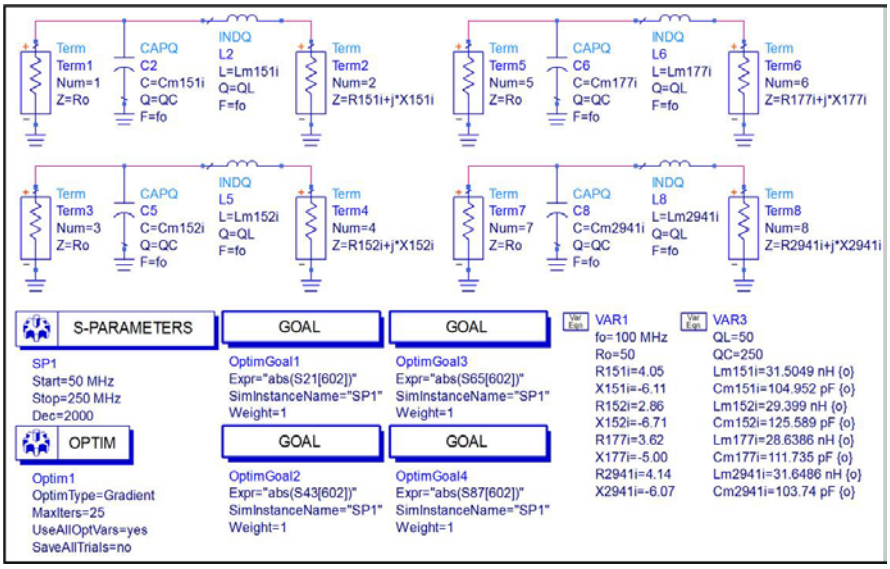

Figure 13 · Input matching circuit design for the first load-pull experiment using ADS simulator

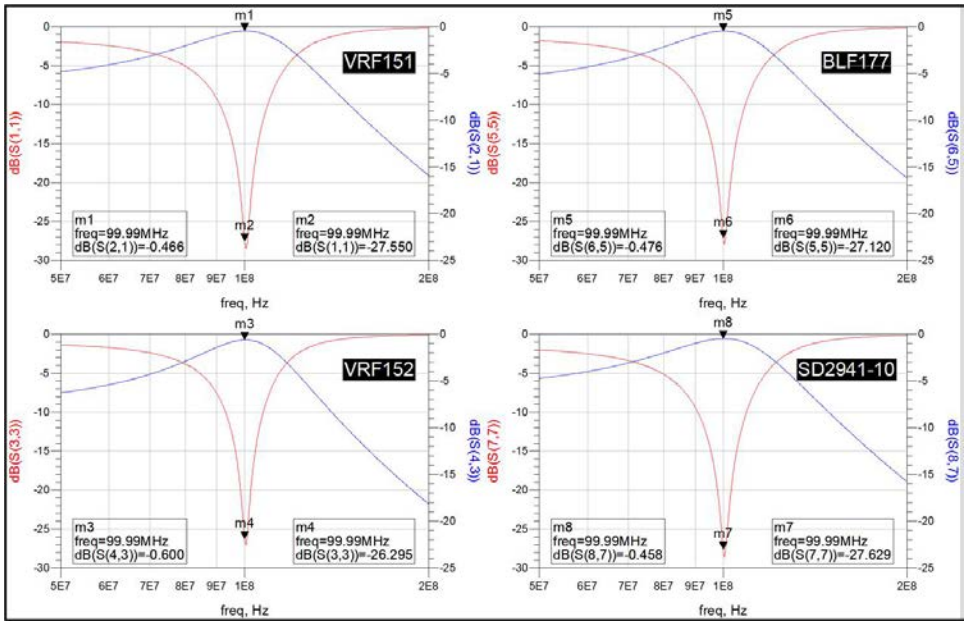

Figure 14 · Frequency responses of the input matching circuits for the first load-pull experiment.

Table 7 · Input matching circuit parameters and insertion loss at 100MHz for the first load-pull experiment.

P_{max}/PAE > 65%, Input Matching				
Transistor	**Z_{in}**	**L (nH)**	**C (pF)**	**IL (dB)**
VRF151	4.05 - j6.11	31.5	105.0	0.47
VRF152	2.86 - j6.71	29.4	125.6	0.60
BLF177	3.62 - j5.00	28.6	111.7	0.48
SD2941-10	4.14 - j6.07	31.6	103.7	0.46

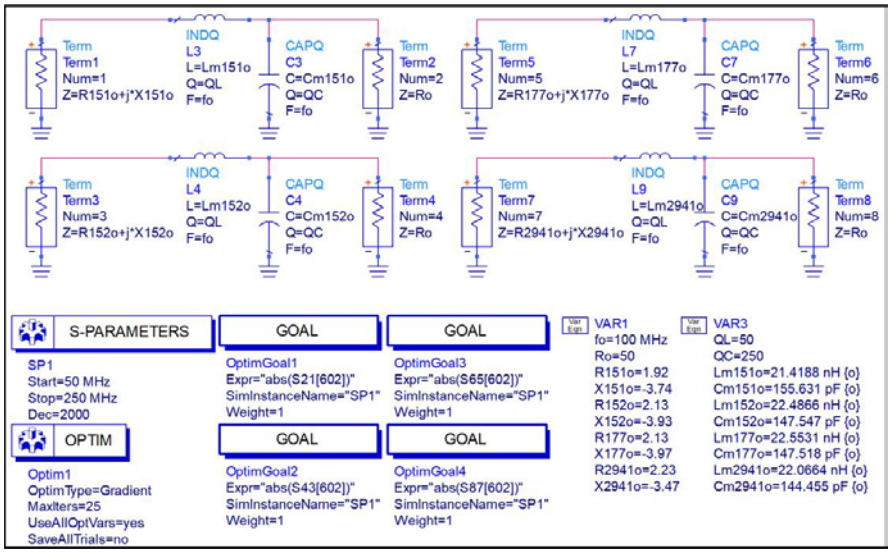

Figure 15 · Output matching circuit design for the first load-pull experiment using ADS simulator.

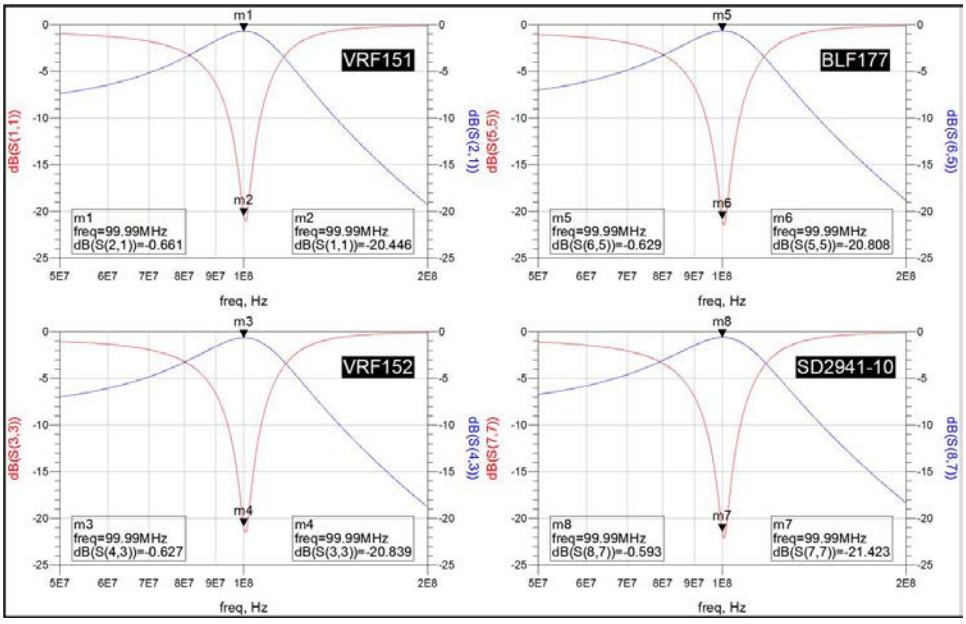

Figure 16 · Frequency responses of the output matching circuits for the first load-pull experiment.

Table 8 · Output matching circuit parameters and insertion loss at 100MHz for the first load-pull experiment.

	P_{max}/PAE > 65%, Output Matching			
Transistor	**Z_L**	**L (nH)**	**C (pF)**	**IL (dB)**
VRF151	1.92 + j3.74	21.4	155.6	0.66
VRF152	2.13 + j3.93	22.5	147.5	0.63
BLF177	2.13 + j3.97	22.6	147.5	0.62
SD2941-10	2.23 + j3.47	22.1	144.5	0.59

The Second Load-Pull Experiment - 100% $P_{o,max}$

To further assess the RF performance between VRF151, VRF152 and BLF177, a second load-pull experiment designed to search for the maximum output power at 100MHz in a pulsed mode operation with 20% duty cycle under active cooling by chilled water. It should be noted that SD2941-10 is dropped from this study due to its inferior RF performance.

The results of the second load-pull experiment are listed in Table 9. Unlike the first load-pull experiment, where only input impedances shows noticeable differences, variations in both input and load impedances are observed in the second load-pull experiment. The power sweep results of the three transistors at their respective optimal impedance states as listed in Table 9 are plotted in Figure 17. Again, the RF performance of these three transistors is fairly comparable with some noticeable differences in:

(A). The gain of BLF177 is slightly higher ~ 0.2 dB higher than VRF151 and 0.5 dB higher than VRF152,

(B). The PAE of VRF152 is the highest, which in part is due to its lower $R_{DS(on)}$ than the other two transistors.

The 1-dB compression point of VRF152 is the lowest, which implies the worst linearity performance among the three transistors.

Table 9 · Optimal impedance states of the second load-pull experiment.

100% P_{out}		Z_{in}	Z_L
VRF151	**DUT1**	2.54 - j3.45	3.28 + j1.78
VRF152	**DUT1**	2.45 - j3.42	2.36 + j2.07
BLF177	**DUT1**	3.67 - j3.72	3.05 + j1.75

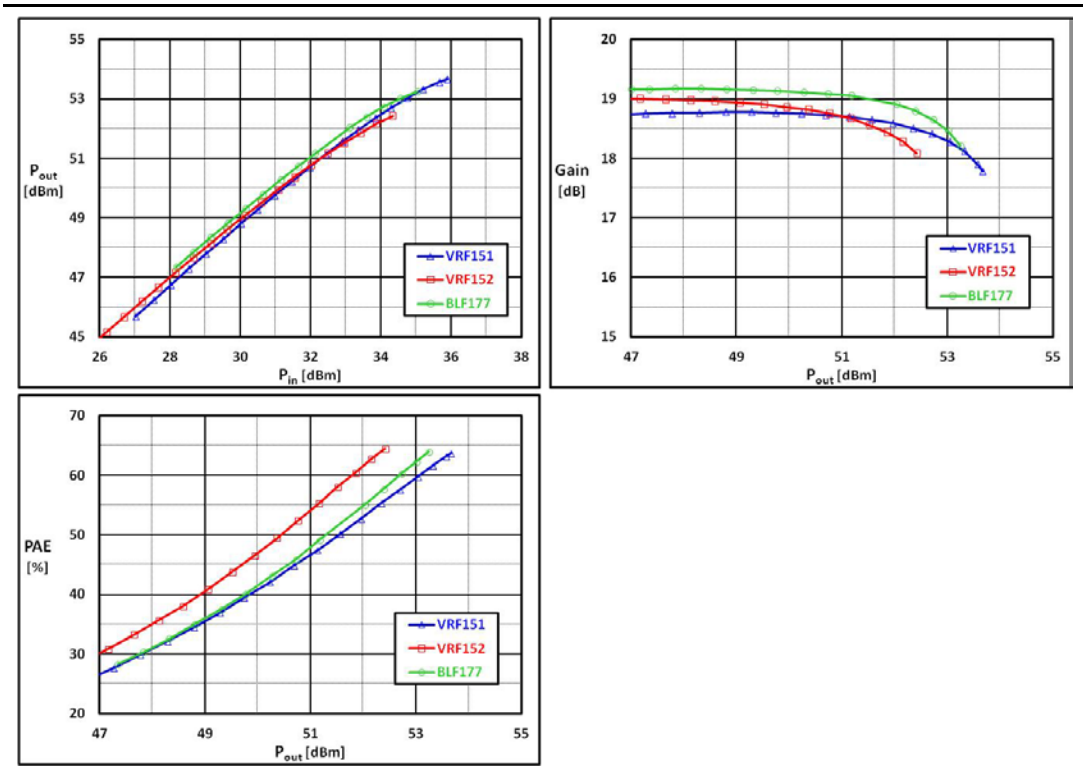

Figure 17 · Power sweep results of the second load-pull experiment.

Using the same L-network as the input/output matching circuits, the optimal impedances of the second load-pull experiment are also matched to the de facto 50Ω standard. The matching circuit parameter along with the insertion loss at 100MHz are listed in Tables 10 and 11, which indicates that a simple value change of matching components suffices to preserve the optimal performance of any of these three transistors when dropped into the circuit designed and optimized for the other.

Table 10 · Input matching circuit parameters and insertion loss at 100MHz for the second load-pull experiment.

100% P_{optm} , Input Matching				
Transistor	**Z_{in}**	**L (nH)**	**C (pF)**	**IL (dB)**
VRF151	2.54 - j3.45	23.0	135.1	0.55
VRF152	2.45 - j3.42	22.7	137.7	0.56
BLF177	3.67 - j3.72	26.6	111.3	0.44

Table 11 · Output matching circuit parameters and insertion loss at 100MHz for the second load-pull experiment.

100% P_{optm} , Output Matching				
Transistor	**Z_L**	**L (nH)**	**C (pF)**	**IL (dB)**
VRF151	3.28 + j1.78	22.4	118.9	0.43
VRF152	2.36 + j2.07	20.2	141.2	0.53
BLF177	3.05 + j1.75	21.8	123.6	0.45

It is also of interest to assess the RF performance if either VRF151 or VRF152 is dropped into the circuit designed and optimized for BLF177 without any circuit modification. Table 12 and 13 list the results of such exercises by presenting the optimal impedances for BLF177 to VRF151 and VRF152, respectively, and adjusting the input drive until the output power reaches the rated power of 150W.

Table 12 · Results of drop-in of VRF151 into the circuit optimized for BLF177 in the second load-pull experiment.

Device	**Z_{in}**	**Z_L**	**P_o (dBm) (~150W)**	**PAE (%)**	**Gain (dB)**	**P_{1dB} (dBm)**
BLF177	3.66 - j3.71	3.05 + j1.75	51.75	53.10	18.93	53.26
VRF151	2.54 - j3.45	3.28 + j1.78	51.70	55.23	19.64	53.70
VRF151 w BLF177 Z_{optm}	3.66 - j3.71	3.05 + j1.75	51.84	57.89	19.47	n/a

Table 13 · Results of drop-in of VRF152 into the circuit optimized for BLF177 in the second load-pull experiment.

Device	**Z_{in}**	**Z_L**	**P_o (dBm) (~150W)**	**PAE (%)**	**Gain (dB)**	**P_{1dB} (dBm)**
BLF177	3.66 - j3.71	3.05 + j1.75	51.75	53.10	18.93	53.26
VRF152	2.45 - j3.40	2.36 + j2.07	51.75	59.76	18.49	52.42
VRF152 w BLF177 Z_{optm}	3.66 -j3.71	3.05 + j1.75	51.78	55.43	18.25	n/a

Interestingly, the "drop-in" of VRF151 into the circuit optimized for BLF177 in the second load-pull experiment results in both higher gain and PAE than BLF177 in its own optimal circuit, which indicates that VRF151 and BLF177 are fairly interchangeable in their respectively optimized circuit without any change. For stability considerations, however, it is recommended that the input matching be modified to its own optimal impedance state for the broadest region of stability during operation.

Similar "drop-in" of VRF152 into the optimal circuit for BLF177 in the second load-pull experiment results in higher PAE but slightly lower gain than BLF177 in its own optimal circuit, which again indicates both VRF152 and BLF177 are also interchangeable. Again, modification on the input matching circuit is recommended for stability considerations.

Concluding Remarks

The maximum ratings and key parameters of the four RF VDMOS transistors under study are discussed and compared. For a quantitative analysis, ranking is assigned for each parameter according to its merit with a score of 4 assigned to the highest ranking transistor and progressively decreasing scores towards the lower rankings. A figure of merit (FM) is then computed for each transistor by averaging its score over the 14 categories included in the analysis. Table 14 lists the rankings of the 4 transistors in each of the 14 categories as well as the FM for each of the 4 transistors. It should be noted: (A) Instead of ranking the absolute value of $V_{GS(th),}$ the range and bin spacing are ranked since narrower range and spacing are both desirable as discussed earlier, (B) Although the test conditions for $V_{GS(th)}$, $R_{DS(on)}$, I_{DSS}, $R_{\theta JC}$ may not be identical among the four transistors, it wouldn't changed the rankings of these parameters had they been tested under the same conditions[3], and (C) The same rankings in $V_{(BR)DSS}$ and g_{fs} are given to BLF177 as SD2941-10 and VRF152 since the differences between them are small.

From Table 14, it is not surprising that VRF151 scores the highest figure of merit since it ranks first in eight and second in 6 categories out of the 14 parameters analyzed. On the other hand, BLF177 ranks poorly among the four RF VDMOS transistors under study, which only ranks first in 2 of the 14 parameters. Also, VRF152 is closely behind VRF151 followed by SD2941-10.

The RF performance of the four VDMOS transistors is also evaluated with the load-pull experiments. The load-pull results strongly suggest that VRF151 and VRF152 are interchangeable with BLF177. For best stability performance, it is recommended that the input matching circuit be optimized for the respective transistor, which often only involves a simple value change of the matching components in the same matching circuit topology. Interchanging with SD2941-10 is not recommended since its RF gain is significantly lower and least flat vs. output power than the other three transistors.

[3] For $V_{GS(th)}$, instead of absolute values, only range and group spacing are used in ranking, which are relatively independent of different sensing currents, at which $V_{GS(th)}$ is measured. For $R_{DS(on)}$, they are measured at different drain currents of 5A and 10A at a common gate-source voltage of 10V, which are in the linear region of the I_D-V_D curve well below saturation, where the variation in $R_{DS(on)}$ is very small. For I_{DSS}, both VRF151 and VRF152 are measured at higher drain-source voltage at 100V, and their assigned ranking would be the same had they were measured at a lower drain-source voltage of 50V. For $R_{\theta JC}$, whose measurement is very sensitive to the positioning of the thermal couple underneath the device, it is assumed the best practice as well as optimal values are reported by the manufacturers of these transistors.

Table 14 · Ranking and figure of merit of the four RF VDMOS transistors under study.

RF VDMOS Transistor		VRF151	VRF152	BLF177	SD2941-10
$V_{(BR)DSS}$	[V]	170	130	125	130
	Ranking	1	2	2	2
$I_{D,max}$	[A]	16	20	16	20
	Ranking	2	1	2	1
$P_{D,max}$	[W]	300	300	220	389
	Ranking	2	2	3	1
$V_{GS,max}$	[V]	±40	±40	±20	±20
	Ranking	1	1	2	2
$V_{GS(th)}$ Range	[V]	1.5	1.5	2.5	2.5
	Ranking	1	1	2	2
$V_{GS(th)}$ Bin Spacing	[V]	0.075	0.075	0.1	0.1
	Ranking	1	1	2	2
$R_{DS(on)}$	[W]	0.3	0.2	0.3	0.2
	Ranking	2	1	2	1
g_{fs}	[S]	5	5	4.5	5
	Ranking	1	1	1	1
I_{DSS}	[mA]	1	0.05	2.5	0.05
	Ranking	2	1	3	1
C_{iss}	[pF]	375	383	480	415
	Ranking	1	2	4	3
C_{oss}	[pF]	200	215	190	236
	Ranking	2	3	1	4
C_{rss}	[pF]	12	20	14	17
	Ranking	1	4	2	3
$R_{\theta JC}$	[°C/W]	0.6	0.6	0.8	0.45
	Ranking	2	2	3	1
f_T	[GHz]	1.9	1.8	1.3	1.6
	Ranking	1	2	4	3
Figure of Merit		3.6	3.3	2.6	3.1

Appendix A - Capacitances of a VDMOS Device

In device circuit models, capacitances of a transistor are conventionally specified as the capacitance between any of the two terminals of the transistor, as shown in Figure A1 for a VDMOS device. Although these terminal capacitances are useful in circuit analysis, they are very difficult to measure directly.

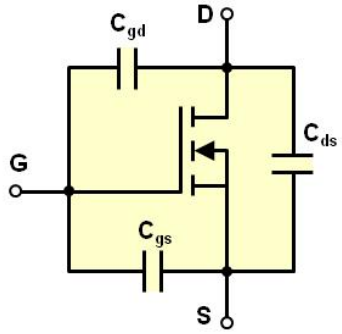

Figure A1 Capacitances of a VDMOS device.

The so-called input, output and reverse transfer capacitances, C_{iss}, C_{oss} and C_{rss}, on the other hand, are readily measurable. Figures A2 and A3 illustrate the circuits for measuring these capacitances. It is important to note that these capacitances are highly dependent on the bias voltage at the drain terminal, and such biasing circuit needs to be included in any of the measurement circuits.

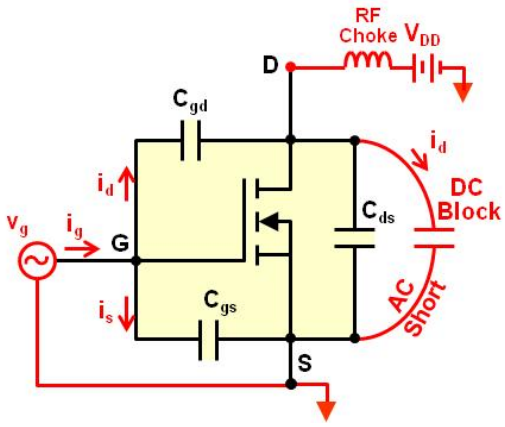

Figure A2 Measurement Circuit for C_{iss} and C_{rss}.

The input capacitance, C_{iss}, is defined as the capacitance between the gate and source terminals when the drain terminal is dynamically shorted to the source terminal. By properly placing the RF choking inductor and the DC blocking capacitor, the drain terminal is biased at V_{DD}, while no DC current is drawn from the DC source. In addition, the drain terminal is dynamically (AC) shorted to ground as shown in Figure A2. The input impedance and capacitance at the gate terminal are defined, respectively, as

(A1) $$\mathbf{Z}_{iss} = \mathbf{R}_{iss} + j\mathbf{X}_{iss} = \frac{\mathbf{v}_g}{\mathbf{i}_g}$$

(A2) $$\mathbf{C}_{iss} = \frac{-\mathbf{1}}{2\pi \mathbf{f}_o \mathbf{X}_{iss}}$$

From Figure A2, it can be seen that C_{iss} is the equivalent of C_{gs} and C_{gd} in parallel such as

(A3) $$\mathbf{C}_{iss} = \mathbf{C}_{gs} + \mathbf{C}_{gd}$$

Also from Figure A2, the reverse transfer impedance and capacitance at the same gate terminal are defined, respectively, as

(A4) $$\mathbf{Z_{rss} = R_{rss} + jX_{rss} = \frac{v_g}{i_d}}$$

(A5) $$\mathbf{C_{rss} = \frac{-1}{2\pi f_o X_{rss}}}$$

Note that the drain current, id, can be measured at the external current path dynamically shorting the drain and source terminals as shown in Figure A2, and C_{rss} is identical to C_{gd}, i.e.,

(A6) $$\mathbf{C_{rss} = C_{gd}}$$

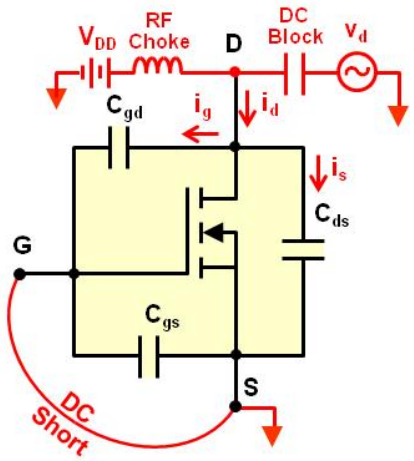

Figure A3 Measurement circuit for C_{oss}.

Finally, from Figure A3, the output capacitance is defined as the capacitance at the drain terminal when the gate terminal is shorted to the source terminal. Since the gate and source terminals are DC isolated internally, a simple DC short suffices in this case. The output impedance and capacitance at the drain terminal are defined, respectively, as

(A7) $$\mathbf{Z_{oss} = R_{oss} + jX_{oss} = \frac{v_d}{i_d}}$$

(A8) $$\mathbf{C_{oss} = \frac{-1}{2\pi f_o X_{oss}}}$$

As seen from Figure A3 C_{oss} is the equivalent of C_{ds} and C_{gd} in parallel such as

(A9) $$\mathbf{C_{oss} = C_{ds} + C_{gd}}$$

Moving beyond the terminal capacitances, C_{gs}, C_{ds} and C_{gd}, and measurable capacitances, C_{iss}, C_{oss} and C_{rss}, it is also insightful to see how these capacitances reside in the physical structure of a typical VDMOS device. Figure A4 shows a conceptual cross-section of a VDMOS device along with the DC bias conditions to activate the inversion channels for the electron current flow from source to drain terminals.

With the aid of Figure A5, the physical capacitors within the VDMOS structure can be readily identified: (A) The overlapped area between polysilicon and P-body and N-source regions forms the capacitor C_{ox1}, (B) The drain is connected to source via the drift region and the body diode at the P-body and N-drift junction, and (C) the gate and drain are connected via the capacitor C_{ox2}, which is the overlapped area between polysilicon and N-drift region, and a 2nd capacitor C_{drift}, which is formed due to the space-charge in the drift region when drain is positively biased. It should be noted that both C_{ox1} and C_{ox2} are relatively independent of the bias voltage at the drain, while both C_{drift} and C_{body} are strongly dependent on the drain bias voltage.

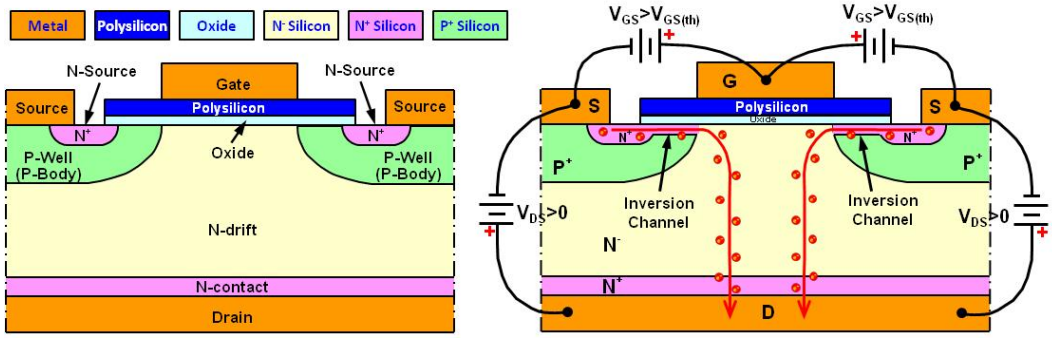

Figure A4 Conceptual cross-section of a typical VDMOS structure.

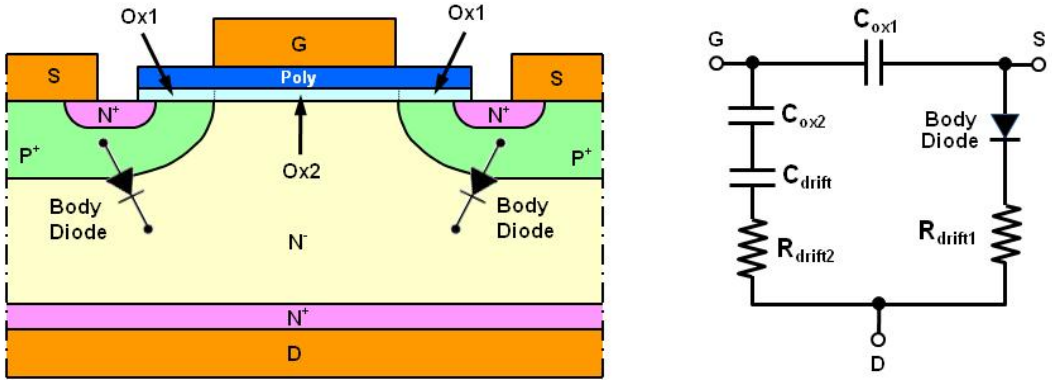

Figure A5 Cross-sectional view of the VDMOS capacitances.

Inspecting circuits in Figures A1 and A5, one quickly recognizes that

(A10) $$\mathbf{C_{gs} = C_{ox1}}$$

(A11) $$\mathbf{C_{gd} = \left(\frac{1}{C_{ox2}} + \frac{1}{C_{drift}} \right)^{-1}}$$

(A12) $$\mathbf{C_{ds} = C_{body}}$$

From Equations A3, A6, A9 and A10-A12, the measurable capacitances and physical capacitances can be linked via the following equations:

(A13) $$\mathbf{C_{iss} = C_{ox1} + \left(\frac{1}{C_{ox2}} + \frac{1}{C_{drift}} \right)^{-1}}$$

(A14) $$\mathbf{C_{oss} = C_{body} + \left(\frac{1}{C_{ox2}} + \frac{1}{C_{drift}} \right)^{-1}}$$

(A15) $$\mathbf{C_{rss} = \left(\frac{1}{C_{ox2}} + \frac{1}{C_{drift}} \right)^{-1}}$$

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The load-pull system at MPPG was set up by highly competent RF engineers, Dick Frey and John Soliday, with a combined RF transmitter/PA expertise of more than 60 years. Dick Frey designed and executed the first load-pull experiment, and John Soliday did the second one. This work simply is not possible without their expert contribution and consultation.

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