MR0014

Media Report

SmartFusion2 SoC FPGAs, IGLOO2, and RTG4 SerDes Transmission Media Report

February 2018

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Revision 3.0 is updated for changes related to RTG4 and follows the latest standards from Microsemi Technical Publications. This document is published in February 2018.

1.2 Revision 2.0

All the instances of 5.0 Gbps were removed in this revision.

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

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2 SerDes Transmission Report

This report focuses on the ability of SmartFusion®2 SoC FPGAs, IGLOO®2, and RTG4™ FPGAs to interconnect SerDes datastreams across different media and showcase the SerDes capability to deliver high-quality signaling using evaluation kits from Microsemi.

2.1 Introduction

The implementation of Serializer/Deserializer (SerDes) devices permit smaller area interconnections to be used that reduces the interference and EMI generated by legacy-wide parallel interfaces. Today, Microsemi offers SerDes devices that can transfer serial data at several gigabits per second (Gbps) over the backplane and cable mediums. These tests are not intended to provide exhaustive characterization information. The information is provided to show typical performance of the devices with the kits. This report summarizes the use of typical cable and backplane mediums with the SmartFusion2 SoC FPGA, IGLOO2, and RTG4 FPGA SerDes devices.

The experimentation highlighted in the document uses the IGLOO2 Evaluation Kit and RTG4 Development Kit. The boards allow connection to a SerDes lane through SMA connectors. These connectors are used throughout the experiment to interoperate with the test fixtures and the equipment. Tests were conducted using the IGLOO2 and RTG4 embedded SerDes test capabilities and SmartDebug SerDes access, to adjust and tune the SerDes devices.

Figure 1 IGLOO2 Evaluation Kit Board

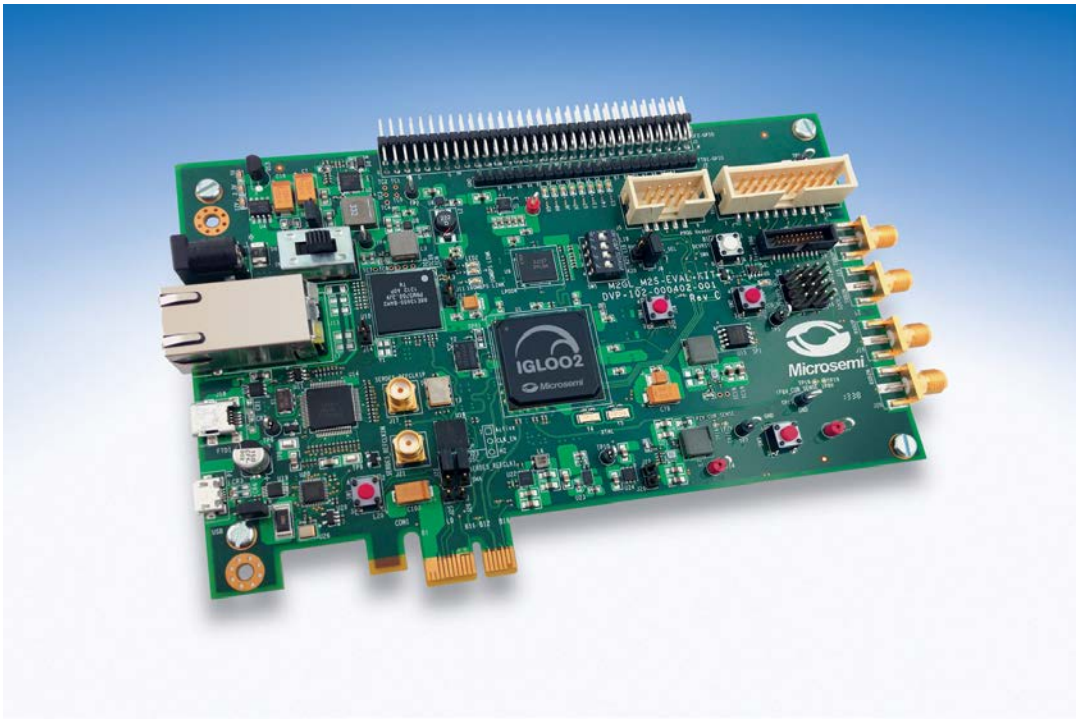
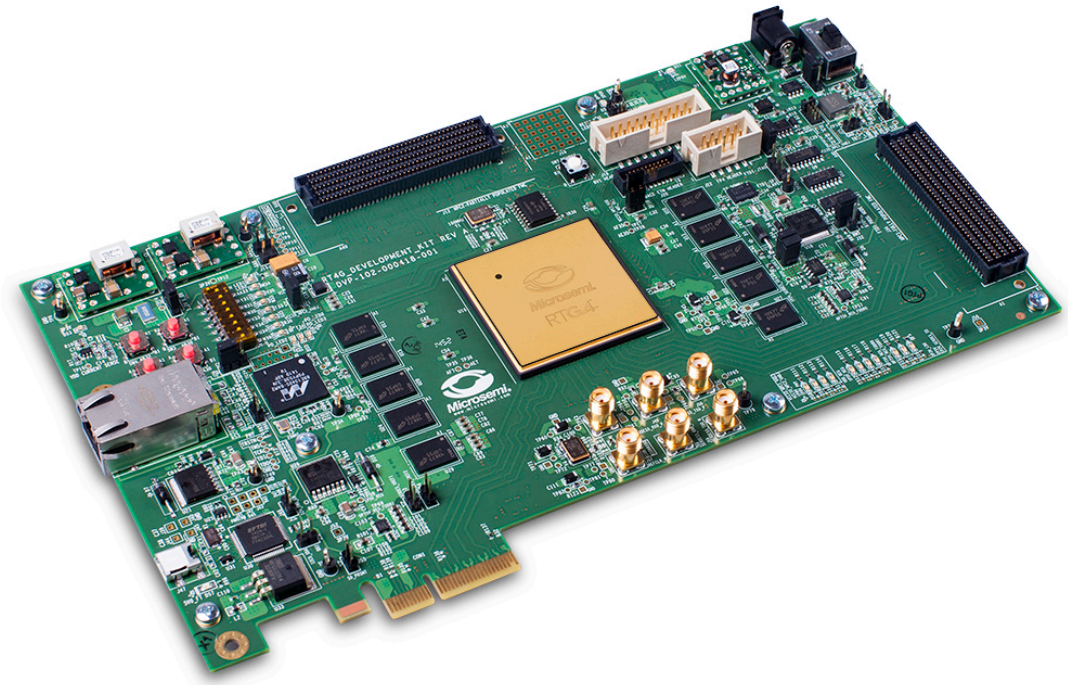


Figure 2 RTG4 Development Kit Board



The SmartFusion2/IGLOO2/RTG4 devices offer both transmit de-emphasis and receiver continuous-time linear equalization (CTLE) to overcome losses and improve the signal integrity. The transmit de-emphasis gives the user the option to configure the de-emphasis circuit to different levels, depending on the system requirements, that helps to improve the high-frequency signal waveform. The CTLE also offers a wide range of dynamic equalization to overcome board losses as signals are attenuated at the receiver. The CTLE tunings and transmit de-emphasis settings were used in all the tests specified in this report to highlight the signal integrity capabilities.

The following parameters were adjusted in the test:

- TX_PRE—Transmitter Pre-cursor de-emphasis
- TX_PST—Transmitter Post-cursor de-emphasis
- RX_AMP—Receiver equalization amplitude ratio
- RX_CUT—Receiver equalization cut-off frequency ratio

For more information, see the following user guides:

- UG0447: SmartFusion2/IGLOO2 SoC FPGA High Speed Serial User Guide
- UG0567: RTG4 SoC FPGA High Speed Serial User Guide

2.2 Network Cables

Ethernet cabling (specifically CAT5E/6/6A) is designed for ultra-low cost operations and is specified to work over relatively long distances for speeds up to a maximum of 1 Gbps. One of the key aspects for the success in real applications is that BASE-T transceivers have extra functionality that is absent in any SerDes-based FPGA or SoC devices. The extra functionality allows the BASE-T PHY devices to drive and receive signals with longer network cable installations.

The TIA/EIA–568A Commercial Building Telecommunications Cabling Standard defines the transmission requirements for commercial building telecommunication wiring. It classifies cabling into different categories based upon the attenuation and crosstalk losses over frequency. Twisted-pair cables are classified in different categories. Most differential signaling applications that require cabling utilize CAT5E, CAT6, and CAT6A cable at specified long distances (up to 1 Gbps). CAT5E is specified to operate at 100 MHz. CAT6 is categorized for 250 MHz while CAT6A is characterized to achieve 500 MHz with enhanced cross-talk immunity. These cables are all specified to operate at their specified speeds at lengths up to 100 meters. However, these cables can perform adequately when used for short distance point-to-point interconnections.

The report illustrates the performance of differential SerDes devices that use different clock-rate and different lengths of standard CAT5E, CAT6, and CAT6A cables between the serializer-transmitter and receiver-de-serializer. The setup uses an IGLOO2/RTG4 Evaluation Kit board equipped with SMA connectors. These connectors were cabled to a laboratory conversion PCB that translates the SMA connections to a standard RJ-45 connection.

The results are plotted as cable length versus data rate running at nominal voltage and room temperature. The test was performed using a single serial lane capable of running up to 3.125 Gbps and by transmitting PRBS7 data from the internal PRBS pattern generator from the serializer TX through the cable translator and network cable and back to the RX of the de-serializer. The data stream is checked for errors by the internal pattern checker. The data and clock should be properly recovered after being sent through the cable to avoid errors. Figure 1 and Figure 2 show the board setup.

The results show how increased cable lengths and cable types affect bit error rate, while varying the cable connections between the serializer and de-serializer. The SerDes PMA allows the tuning of TX de-emphasis and RX equalization to compensate for the different types of cable and length loss. The SerDes PMA tuning adjustments were used to optimize the cable link when necessary and when the cable length is increased, the performance degrades to a point where the link between the serializer and de-serializer is no longer usable, as shown in the following table.

Table 1 Network Cable Test Results Summary for SmartFusion2/IGLOO2

3 FT	**Cat6A**	**Cat6**	**Cat5**
1.25 Gbps	Pass	Pass	Pass
2.5 Gbps	Pass	Pass	Pass
3.125 Gbps	Pass	Pass	Pass
10 FT	**Cat6A**	**Cat6**	**Cat5**
1.25 Gbps	Pass	Pass	Pass
2.5 Gbps	Pass[1]	Pass[1]	Fail
3.125 Gbps	Pass[1]	Fail	Fail

20 FT	**Cat6A**	**Cat6**	**Cat5**
1.25 Gbps	Pass	Pass	Pass
2.5 Gbps	Pass[2]	Fail	Fail
3.125 Gbps	Pass[2]	Fail	Fail
35 FT	**Cat6A**	**Cat6**	**Cat5**
1.25 Gbps	Pass[2]	Fail	Fail
2.5 Gbps	Pass[2]	Fail	Fail
3.125 Gbps	Fail	Fail	Fail

PRBS7 pattern

1. TX_PST=0x19
2. TX_PST=0xA, RE_AMP=0x80, RE_CUT=0x80

Note: Default= TX_PRE=0x0, TX_PST=0x15, RE_AMP=0x0, RE_CUT=0x0

Table 2 Network Cable Test Results Summary for RTG4

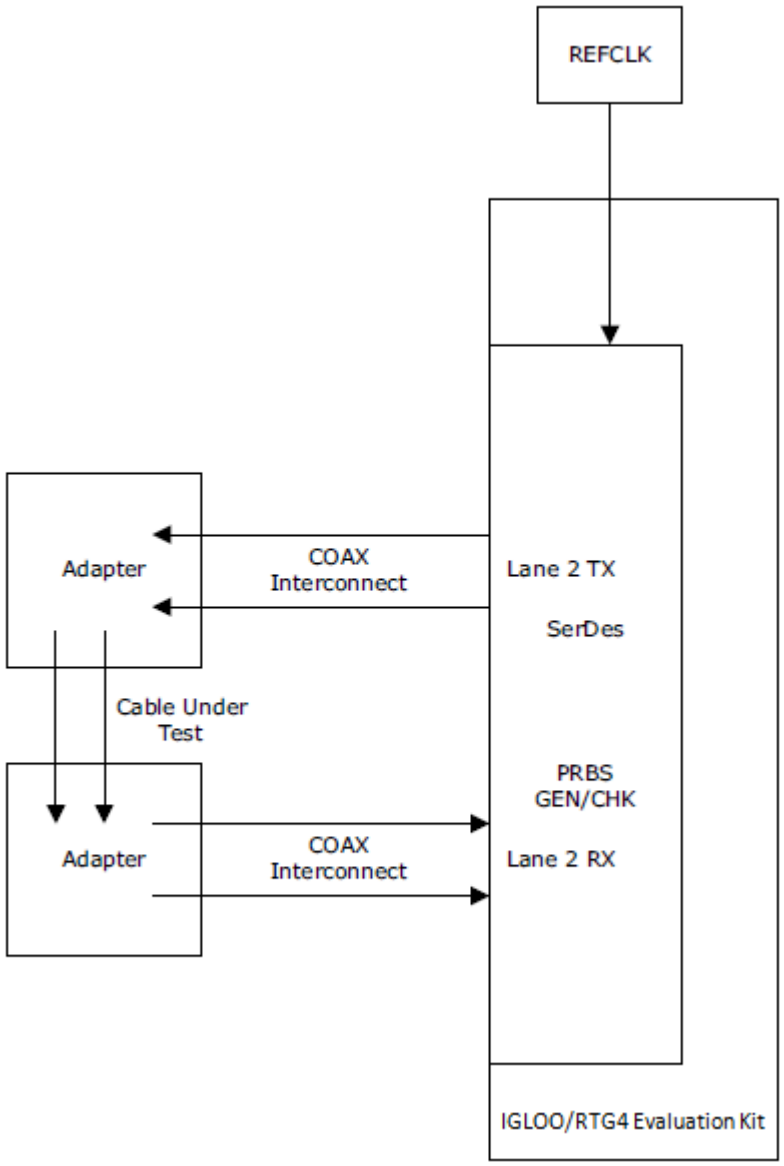
3 FT	**Cat6A**	**Cat6**	**Cat5**
1.25 Gbps	Pass	Pass	Pass
2.5 Gbps	Pass	Pass	Pass
3.125 Gbps	Pass	Pass	Pass
10 FT	**Cat6A**	**Cat6**	**Cat5**
1.25 Gbps	Pass	Pass	Pass
2.5 Gbps	Pass	Pass	Pass
3.125 Gbps	Pass	Fail	Fail
20 FT	**Cat6A**	**Cat6**	**Cat5**
1.25 Gbps	Pass	Pass	Pass
2.5 Gbps	Pass[1]	Pass[1]	Fail
3.125 Gbps	Pass[1]	Fail	Fail
35 FT	**Cat6A**	**Cat6**	**Cat5**
1.25 Gbps	Pass	Fail	Fail
2.5 Gbps	Pass[1]	Fail	Fail
3.125 Gbps	Fail	Fail	Fail

PRBS7 pattern

Default= TX_PRE=0x00, TX_PST=0x15,TX_AMP=0x80, RE_AMP=0x0, RE_CUT=0x0

1. TX_PST=0xA, RE_AMP=0x70, RE_CUT=0x4F

Figure 3 Network Cable Test Setup



In the laboratory experiment, the common CAT5E, CAT6, and CAT6A type cables were used to collect data. These cable types have a known composition and loss. The results shown in Table 1 can be used as a guide for the relative performance that can be achieved with similar and more expensive cable types.

2.3 Backplane

This section illustrates the SerDes high-speed backplane capabilities, through a series of laboratory tests. The Tyco Z-Pack TinMan Customer Evaluation Board was used to provide a realistic system implementation to show the SmartFusion2 SoC, IGLOO2, and RTG4 FPGA SerDes performance.

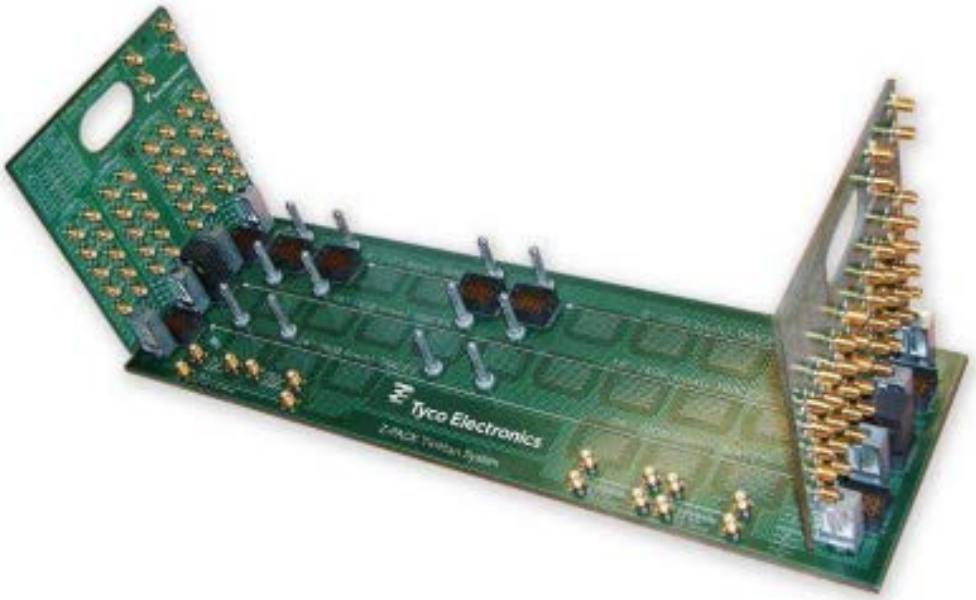
Tyco Electronics provides a variety of tools to aid customers in their design like SPICE single-line and multi-line models and S-parameter models.

2.3.1 Z-PACK TinMan Backplane Connectors

The z-pack Tinman backplane connectors are:

- Designed for high density and high-speed applications.
- Capable of supporting data rates up to 12.5 Gbps.
- Available in three versions— three, four, and five pair/column, respectively fitting 16.25 mm (.625")
- 20.32 mm (0.8"), and 25.4 mm (1") slot pitches.
- Density up to 52 high-speed signal lines per cm board space, in 25.4 mm (1") slot-pitch.
- Pin headers are available in four styles: open end, right end, left end, and dual closed end.
- Order Catalog 5-1773447-9, Z-PACK TinMan High Speed, High Density Backplane Connector. Website— http://www.tycoelectronics.com/ZPackTinMan.

Figure 4 Tyco Electronics Z-Pack TinMan Connector Test System



The following are the two different configuration experiments:

- Data-rate experiment— shows data rate limits measured for various FR4 path lengths.
- Eye diagram experiment— shows performance over a standard reference backplane.

The bit error rate and eye diagram measurements are used to evaluate link performance and margins. Error-free performance is observed through various backplane connections and over different operating conditions, for test intervals of several minutes. The effects and benefits of TX de-emphasis and RX equalization is highlighted in these experimentation.

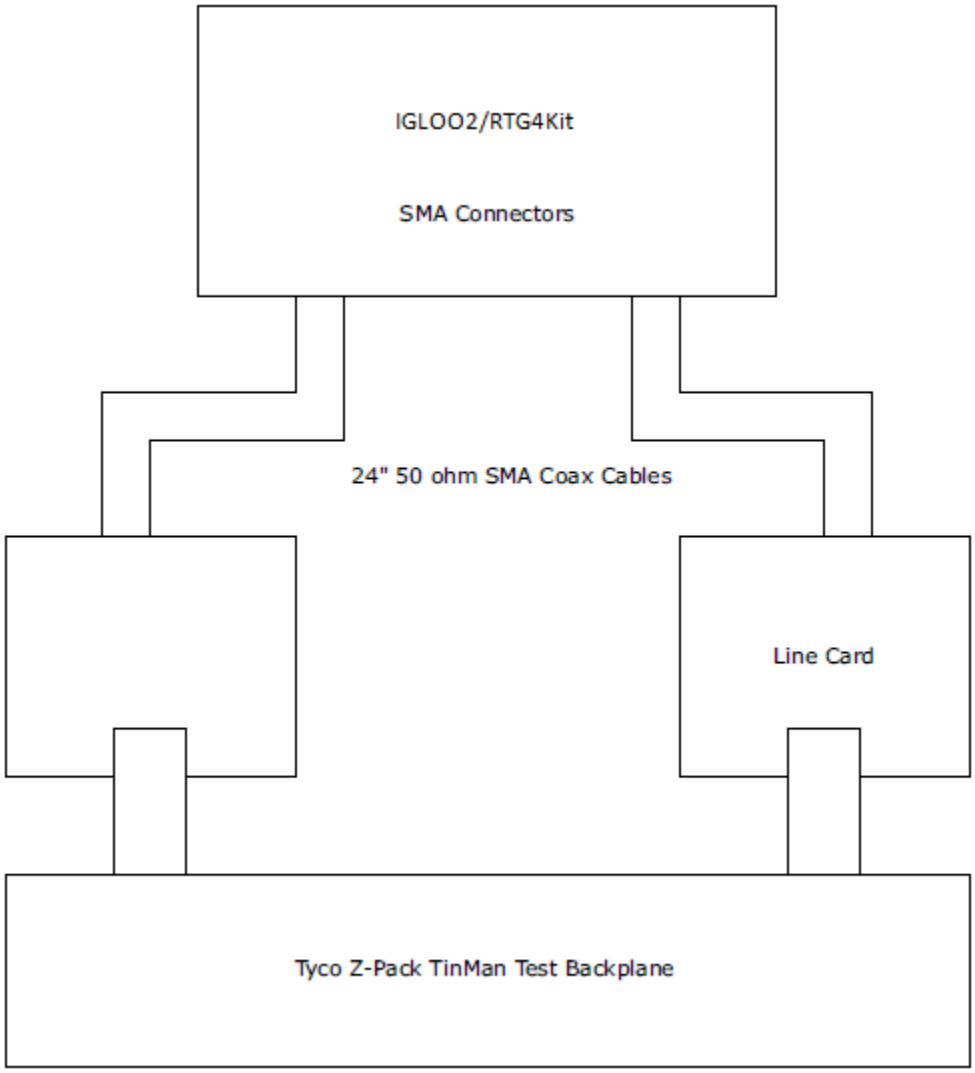
The following table shows the TinMan system trace lengths used for the experimentation.

Table 3 TinMan System Trace Lengths

Line Card Transmit Trace Length	Line Card Receive Trace Length	Backplane Trace Length	Total TinMan System Trace Length
5”	5”	1.5”	11.5”
5”	5”	4”	14”
5”	5”	8”	18”
5”	5”	16”	26”
5”	5”	24”	34”

The Tyco TinMan Evaluation Board includes multiple backplane routed trace lengths. The backplane also requires line cards at both ends of the link which include the 5" traces at both ends of the link, as well as the 5" routed paths on the Microsemi IGLOO2/RTG4 Kit and coax patch cables.

Figure 5 Data Rate Experiment Setup



The experiment was conducted with the IGLOO2/RTG4 Kit connecting the SerDes lane SMA connections to the RX and the TX SMA connectors on the TinMan line cards. SMA coax cables connected the line cards to the IGLOO2/RTG4 Kit. The TinMan line cards were inserted into the TinMan backplane at various length connections. A PRBS7 test pattern was transmitted by the SmartFusion2/IGLOO2/RTG4 internal generator and sent off-chip through the backplane and received back into the SmartFusion2/IGLOO2/RTG4 pattern checker. The data was monitored to be error-free for a period of time equal to 10×10–12 BER.

The following table shows the test results for the data rate experiment.

Table 4 Z-Pack TinMan Backplane Test Results

TinMan Backplane Topology	IGLOO2/SF2 Routing Length (RX/TX)	Cable Length of TX+ RX	TinMan Line Card Length (Both Ends)	Overall Total Routed Length	1.25 Gbps RE_AMP/ RE_CUT	2.5 Gbps RE_AMP/ RE_CUT	3.125 Gbps RE_AMP/RE_ CUT
5" No Connector	10"	16”		15”	0/0	0/0	0/0
4”	10”	16”	10”	24”	0/0	0/0	0/0
8”	10”	16”	10”	28”	0/0	0/0	0/0
16”	10”	16”	10”	36”	0/0	0/0	0x20/0
24”	10”	16”	10”	44”	0/0	0/0	0x20/0

PRBS7 pattern

Default= TX_PRE=0x0, TX_PST=0x15, RE_AMP=0x0, RE_CUT=0x0

Note: CTLE tuning is notated. The RE_AMP and RE_CUT setting are shown in the above table.

Table 5 Z-Pack TinMan Backplane Test Results

TinMan Backplane Topology	PCB routing on RTG4 Dev Kit length for TX+RX	Cable Length of TX+ RX	TinMan Line Card Length (Both Ends)	Overall Total Routed Length	1.25 Gbps RE_AMP/RE_ CUT	2.5 Gbps RE_AMP/RE _CUT	3.125 Gbps RE_AMP/RE _CUT
5" No Connector	3"	16”		8”	0/0	0/0	0/0
4"	3"	16"	10"	17”	0/0	0/0	0/0
8”	3”	16”	10”	21”	0/0	0/0	0/0
16”	3”	16”	10”	29”	0/0	0/0	0/0
24”	3”	16”	10”	37”	0/0	0/0	0x20/0

PRBS7 pattern

Default= TX_PRE=0x0, TX_PST=0x15, RE_AMP=0x0, RE_CUT=0x0

Note: CTLE tuning is notated. The RE_AMP and RE_CUT setting are shown in the above table.

2.4 Eye Diagram Measurements

Expected link performance can be relatively determined by viewing the receiver- end eye diagram. Eye diagrams were sampled at 1.25 Gbps, 2.5 Gbps, and 3.125 Gbps at varied de-emphasis settings. TX de-emphasis compensates for signal losses that occur at higher speeds and longer trace lengths. In general, adding de-emphasis increases the signal quality for an improved eye diagram. Figure 7 captures the data eye opening widths and peak-to-peak voltage swings. The resulting illustrations show captured eye diagrams with 36 inches trace length on the Z-Pack TinMan backplane. These diagrams show impacts of the varying de-emphasis adjustments compared to no de-emphasis tuning.

Figure 6 Eye Diagram Measurement Setup

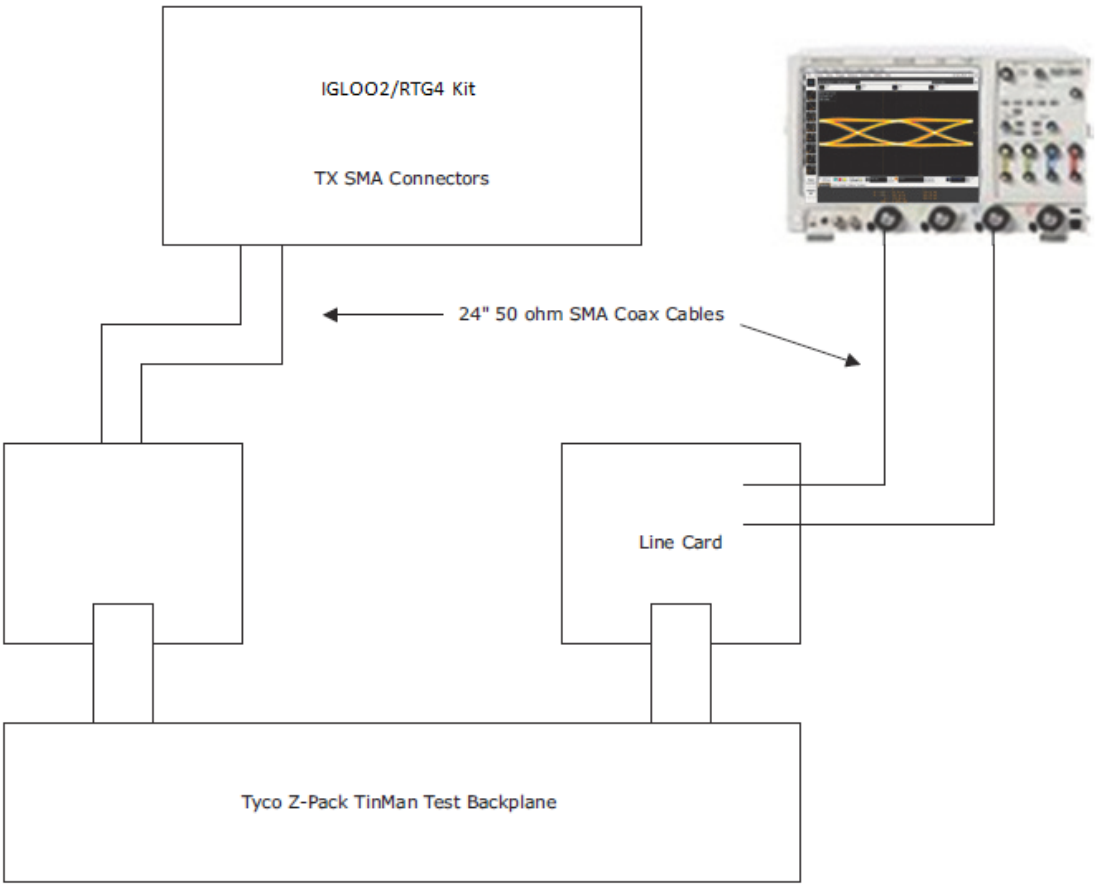
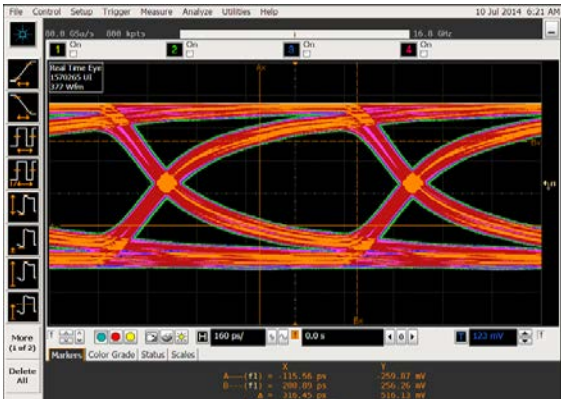
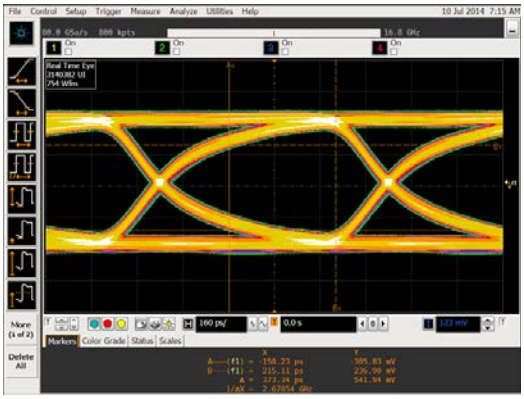
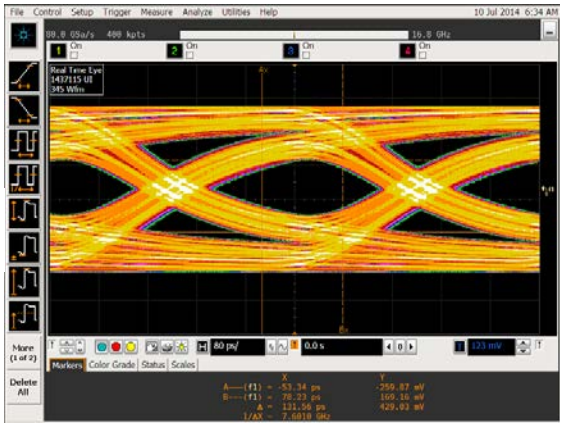
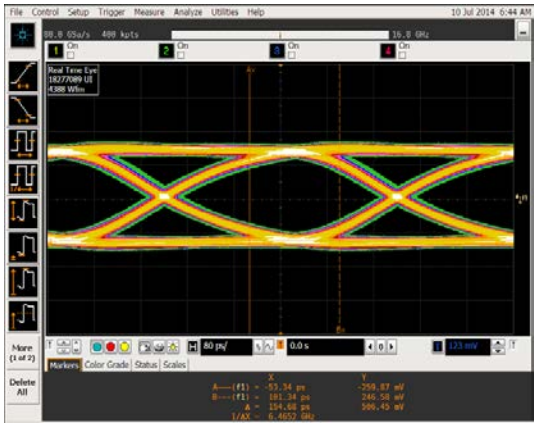


Figure 7 Eye Diagrams with 36” Total Routed Backplane Lengths for SmartFusion2/IGLOO2

	No De-emphasis	De-emphasis= TX_PST=0xa=-1.5 dB
1.25 Gbps		

	No De-emphasis	De-emphasis= TX_PST=0x1a= -4.5 dB
1.25 Gbps		

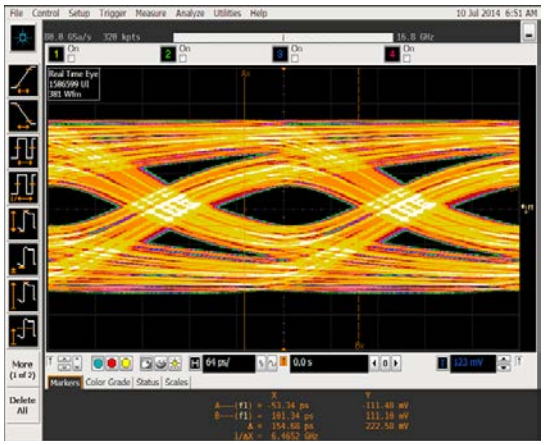
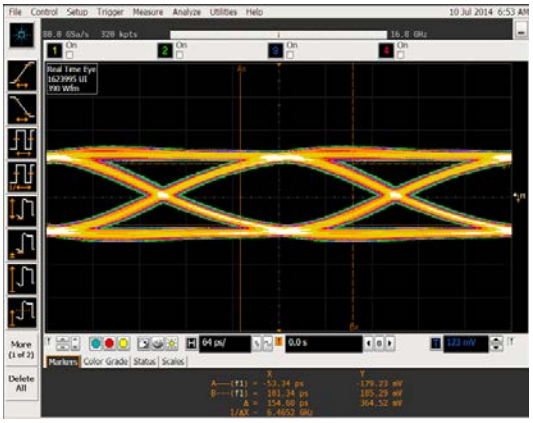
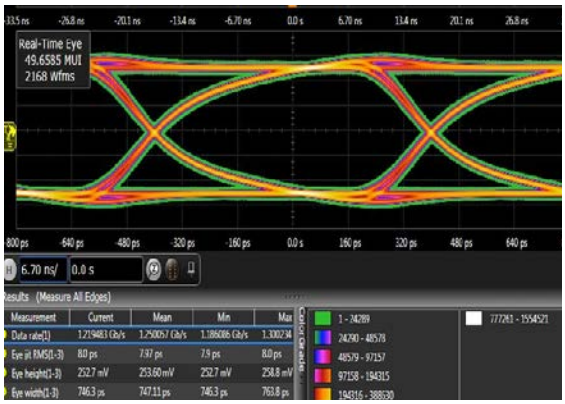
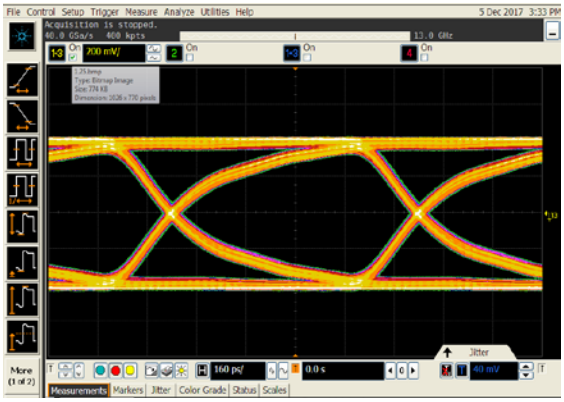
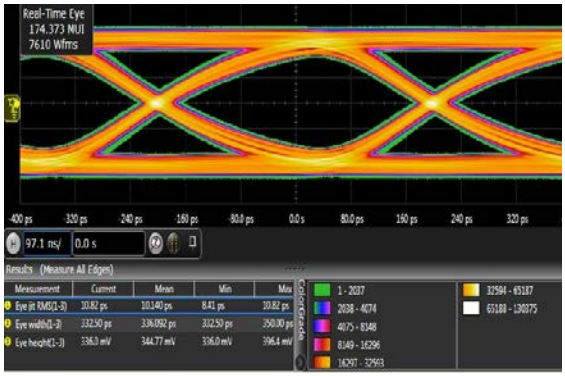
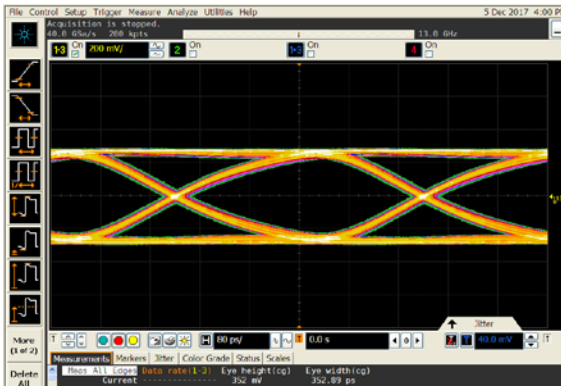
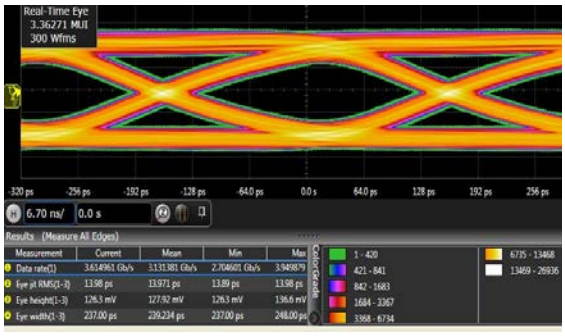
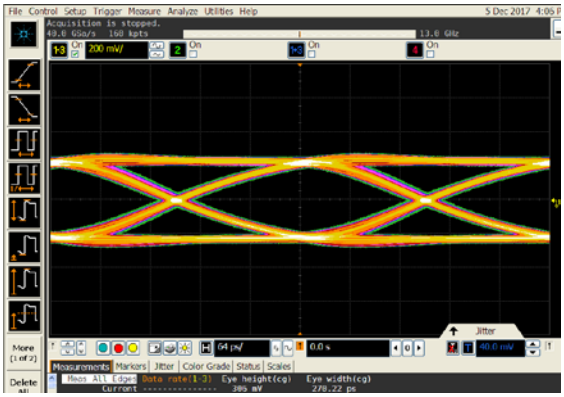
	No De-emphasis	De-emphasis= TX_PST=0x20= -6 dB
3.125 Gbps		

Figure 8 Eye Diagrams with 36” Total Routed Backplane Lengths for RTG4

	No De-emphasis	De-emphasis = TX_PST = 0xa = -1.5 dB
1.25 Gbps		
	No De-emphasis	De-emphasis = TX_PST = 0xa = -4.5 dB
2.5 Gbps		
	No De-emphasis	De-emphasis= TX_PST = 0xa = -6 dB
3.125 Gbps		

Note: 3.125 Gbps is available only in -1 SPD devices.

2.5 Conclusion

The details of this report demonstrate the ability of the SmartFusion®2 SoC, IGLOO®2, and RTG4™ FPGAs to interconnect SerDes datastreams across different media. The experiments showed the capability of the SerDes devices to deliver high-quality signaling over cable and backplane lengths at a broad range of data rates.

With careful system design, designers who optimize the SerDes interconnect using de-emphasis and CTLE equalization of the Microsemi SerDes devices will achieve reliable high-speed performance.

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