# UG0557
# User Guide
# SmartFusion2 SoC FPGA Advanced Development Kit

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Power Matters.

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# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 4.0

Information about the FTDI_JTAG_SEL signal was added. For more information, see Programming, page 19.

## 1.2 Revision 3.0

PCIe edge card ribbon cable was removed from the kit contents. For more information, see Kit Contents, page 2.

## 1.3 Revision 2.0

The following is a summary of the changes made in revision 2.0 of this document.

- Throughout the document, the part number was updated from M2S150-ADV-DEV-KIT-ES to M2S150-ADV-DEV-KIT (SAR 66855).
- Throughout the document, the device number was updated from M2S150T-1FCG1152ES to M2S150TS-1FCG1152 (SAR 66855).
- The MTD files link was updated. For more information, see Manufacturing Test, page 46 (SAR 60671 and 68260).
- Pin details were updated. For more information, see Validating Power Supply, page 46 (SAR 61171).
- Information about FMC connectors was updated. For more information, see FMC Connectors, page 25 (SAR 67950).

## 1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

# 2 Introduction

The RoHS-compliant SmartFusion®2 SoC FPGA Advanced Development Kit (M2S150-ADV-DEV-KIT) enables you to develop the following.

- Microprocessor applications
- Embedded ARM Cortex-M3 processor-based systems
- Motor control applications
- Industrial automation applications
- High-speed serial I/O applications
- Universal serial bus (USB) applications (with OTG support)

## 2.1 Kit Contents

The following table lists the contents of the SmartFusion2 Advanced Development Kit.

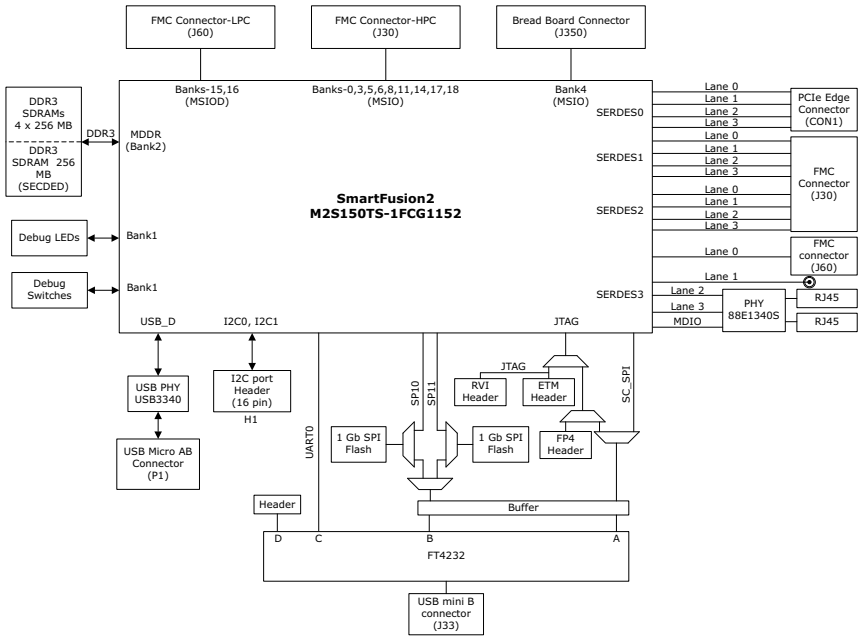
***Table 1 •*** **Kit Contents**

| Item | Quantity |
|---|---|
| SmartFusion2 Advanced Development Board with 150K LE M2S150TS-1FCG1152 device | 1 |
| USB A to Micro B cable | 1 |
| USB Micro A to A cable | 1 |
| USB A to Mini B cable | 1 |
| 12 V/5 A power adapter | 1 |

## 2.2 Block Diagram

The following figure is the block diagram of the SmartFusion2 Advanced Development Kit.

***Figure 1 •*** **SmartFusion2 Advanced Development Kit Block Diagram**



## 2.3 Web Resources

More information about the SmartFusion2 Advanced Development Kit is available at *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/smartfusion2/smartfusion2-advanced-development-kit#overview*.

## 2.4 Board Description

M2S150-ADV-DEV-KIT offers a full-featured development board for SmartFusion2 SoC FPGAs. The board integrates the following features on a single chip.

- Reliable flash-based FPGA fabric
- 166 MHz ARM Cortex-M3 processor
- Advanced security processing accelerators
- Digital signal processing (DSP) blocks
- Static random-access memory (SRAM)
- Embedded non-volatile memory (eNVM)
- High-performance communication interfaces

The SmartFusion2 Advanced Development Board has several standard interfaces including:

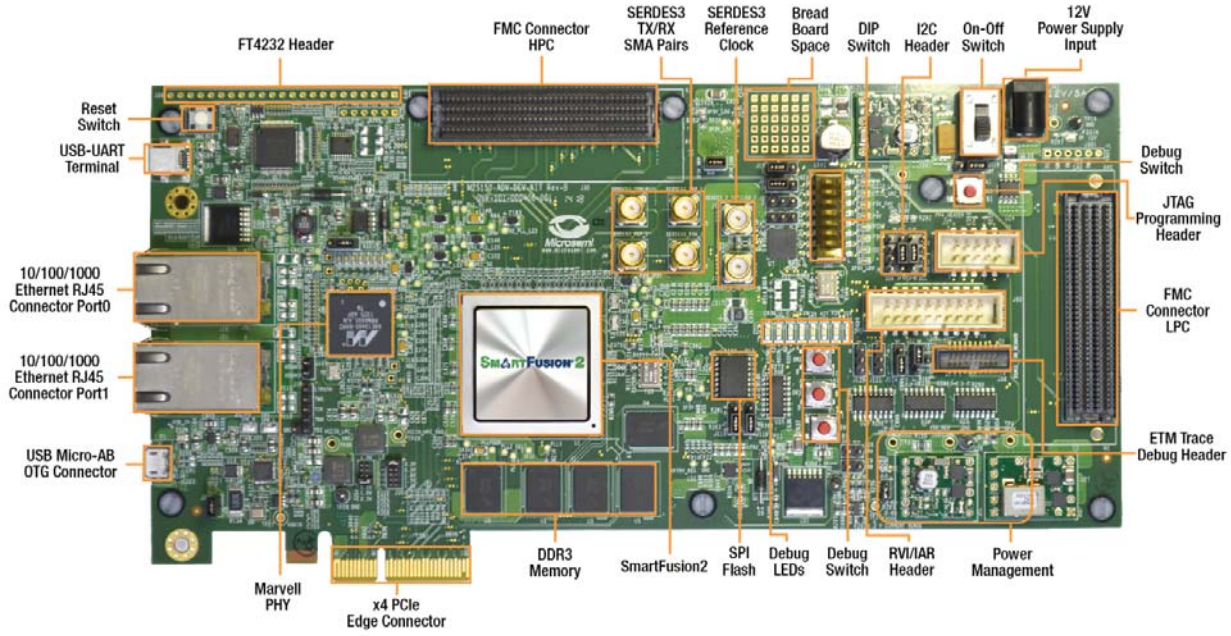
- USB
- x4 serializer and deserializer (SerDes)
- DDR3 memory
- JTAG
- Inter-integrated circuit (I2C)
- Serial peripheral interface (SPI)
- Universal asynchronous receiver/transmitter (UART)
- Dual gigabit Ethernet

The SmartFusion2 memory management system supports 1 GB (4 × 256 MB) on-board DDR3 memory for data storage, 256 MB DDR3 memory for error detection and correction (ECC-SECDED), and 2 GB (2 × 1 GB) memory for SPI flash devices. The SerDes block can be accessed using the PCIe edge connector, high-speed sub-miniature version-A (SMA) connectors, or an on-board FPGA mezzanine card (FMC) low pin count (LPC) connector (J60). Unused MSIOD signals are routed to the J60 connector from the SmartFusion2 device. Unused MSIO signals are routed to another on-board FMC connector—HPC (J30), and although the bread board connector (J350) space available for Bank 4 (MSIO) pins.

The SmartFusion2 device can be programmed through embedded FlashPro5. The Advanced Development Kit has the current measurement feature (see Current Measurement, page 11).

The following figure is a snapshot of the SmartFusion2 Advanced Development Board with its engineering silicon.

***Figure 2 •*** **SmartFusion2 Advanced Development Board**




## 2.5 Board Key Components

The following table lists key components of the SmartFusion2 Advanced Development Board.

***Table 2 •*** **SmartFusion2 Advanced Development Board Components**

| Name | Description |
|---|---|
| SmartFusion2 FPGA | M2S150TS-1FCG1152 FPGA with a hard Cortex-M3 processor. |
| DDR3 synchronous dynamic random access memory (SDRAM) | 4 × 256 MB (256 MB Micron DDR3 memories MT41K256M8DA-125 IT:K) for storing data, and 256 MB (1 × 256 MB Micron DDR3 memory MT41K256M8DA-125 IT:K) for storing ECC bits. |
| SPI flash | A 1-gigabit SPI flash (Micron N25Q00AA13GSF40G) connected to SPI port 0 of the SmartFusion2 microcontroller subsystem (MSS), and another 1-gigabit SPI flash (Micron N25Q00AA13GSF40G) connected to the SmartFusion2 fabric. |
| Ethernet | Two RJ45 connectors (Ethernet jacks with built-in magnetics) interfacing with a Marvell 10/100/1000 BASE-T physical layer (PHY) chip—88E1304S—in Serial Gigabit Media Independent Interface (SGMII) mode. The Marvell PHY device, in turn, interfaces with the Ethernet port of the SmartFusion2 MSS (on-chip MAC and external PHY). |
| RVI header | RVI header for application programming and debugging using Keil ULINK or IAR J-Link. |
| Embedded FlashPro5 | Embedded FlashPro5 for programming and debugging the SmartFusion2 FPGA using Microsemi tools. |
| Future Technology Devices International (FTDI) programmer | FTDI programmer interface (J33) to program the external SPI flash. An FTDI chip is also used to change the JTAG_SEL signal (*high* or *low*) remotely for switching between the RVI header and JTAG mode. |

***Table 2 •*** **SmartFusion2 Advanced Development Board Components *(continued)***

| | |
|---|---|
| Embedded Trace Macro (ETM) cell header | ETM header for debugging. |
| PCI Express (PCIe) edge connector | PCIe edge connector with four lanes. |
| Light-emitting diodes (LEDs) | Eight active-high LEDs connected to some of the user I/Os for debugging. |
| Push-button reset | Push-button system reset for the SmartFusion2 device. |
| Push-button switches | Four push-button switches for testing and navigation. |
| FMC HPC connector (J30) | High pin count FMC header to connect the external daughter boards. Connector array socket 400 pins (40 × 10), 1.27 mm pitch. Unused MSIO pins routed from the SmartFusion2 device to the J30 connector. |
| FMC LPC connector (J60) | Low pin count FMC header to connect the external daughter boards. Connector array socket 160 pins (40 × 4), 1.27 mm. Unused MSIOD pins routed from the SmartFusion2 device to the J60 connector. |
| USB interface | USB Micro-AB connector, interfacing with the high speed USB2.0 ULPI transceiver chip USB3320, which, in turn, interfaces with USB-D port of the SmartFusion2 MSS. |
| DS1818 3.3V EconoReset | A simple three-pin voltage monitor and power-on reset that holds reset for 150 ms for stabilization after power returns to tolerance. |
| OSC-100 | 100 MHz clock oscillator with differential output. |
| OSC-125 | 125 MHz clock oscillator with differential output. |
| OSC-50 | 50 MHz clock oscillator. |
| OSC-32 | 32.768 KHz low-power oscillator. |
| FT4232H | USB-to-quad serial ports in various configurations. |
| TPS3808G09DBVR | Supervisory circuit that monitors system voltage of 0.9 V, asserting an open-drain reset signal when the sense voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logical low. |
| I2C port header | 16-pin header available for I2C0 and I2C1 interfaces of the SmartFusion2 device. |

# 3 Installation and Settings

This section provides information about the software and hardware settings for the SmartFusion2 Advanced Development Kit.

## 3.1 Software Installation

Download and install the Microsemi Libero® SoC software v11.4 or later from the Microsemi website, and register for a free Gold license to the software. The Libero SoC v11.4 or later installer has FlashPro5 drivers. For instructions on how to install Libero SoC and SoftConsole, see *Libero Software Installation and Licensing Guide*.

For instructions on how to download and install Microsemi DirectCores, SGCores, and driver firmware cores, which must be installed on the PC where Libero SoC is installed, see *Installing IP Cores and Drivers User Guide*.

The SmartFusion2 FPGA is supported by the latest IAR Embedded Workbench from IAR Systems for ARM IP. It is also supported by the latest Keil MDK-ARM Microcontroller Advanced Development Kit.

## 3.2 Hardware Settings

This section provides information about default jumper settings, switches, LEDs, and DIP switches for the SmartFusion2 Advanced Development Kit.

### 3.2.1 Jumper Settings

Connect the jumpers with the default settings specified in the following table to evaluate the pre-programmed demo design.

***Table 3 •*** **Jumper Settings**

| Jumper | Description | Pin | Default Settings |
|---|---|---|---|
| **Power Supply** | | | |
| J123 | Jumper to select a core voltage (VDD_REG) of 1.0 V or 1.2 V. | Pin 1-2 for 1.0 V. | Open |
| | | Pin 2-3 for 1.2 V. | Close |
| J353 | Jumper to select a core voltage (VCCIO_HPC_VADJ) of 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2V. | Pin 1-2 for 3.3 V. | Closed |
| | | Pin 3-4 for 2.5 V. | Open |
| | | Pin 5-6 for 1.8 V. | Open |
| | | Pin 7-8 for 1.5 V. | Open |
| | | Pin 9-10 for 1.2 V. | Open |
| J354 | Jumper to select a core voltage (VCCIO_LPC_VADJ) of 2.5 V, 1.8 V, 1.5 V, or 1.2V. | Pin 1-2 for 2.5 V. | Closed |
| | | Pin 3-4 for 1.8 V. | Open |
| | | Pin 5-6 for 1.5 V. | Open |
| | | Pin 7-8 for 1.2 V. | Open |
| J116 | Jumpers to select either SW7 input or signal ENABLE_FT4232 from FT4232H chip. | Pin 1-2 for **SW7** switch selection. | Closed |
| | | Pin 2–3 for Enable_FT4232 signal control. | Open |

***Table 3 •*** **Jumper Settings *(continued)***

| | | | |
|---|---|---|---|
| **Clocks** | | | |
| J10 | Jumper to select switch-side MUX inputs of A or B to the line side. | Pin 1-2 (Input A to the line side) for external clock required to source the line side through FMC connector. | Open |
| | | Pin 2-3 (Input B to the line side) for external clock required to source the line side through SMA connectors. | Open |
| J9 | Jumper to select the output-enable control for the line side outputs. | Pin 1-2 (line-side output enabled). | Open |
| | | Pin 2-3 (line-side output disabled). | Open |
| J8 | Jumper to select the output-enable control for the line side outputs. | Pin 1-2 (line-side output enabled). | Closed |
| | | Pin 2-3 (line-side output disabled). | Open |
| J11 | Jumper to select switch-side MUX inputs of A or B to the line side. | Pin 1-2 (Input A to the line side), that is, on-board 125 MHz differential clock oscillator output is routed to line side. | Closed |
| | | Pin 2-3 (Input B to the line side), that is, on-board 100 MHz differential clock oscillator output is routed to line side. | Open |
| **Marvell PHY** | | | |
| J14 | Jumper to select either PHY_CONFIG1 or M2S_PHY_CONFIG1 for global hardware configuration (CONFIG[1]). | Pin 1-2 CONFIG [1] connects to P2_LED[2] pin of 88E1340S. | Open |
| | | Pin 2-3 CONFIG [1] connects to SmartFusion2 J8 pin (MSIO80NB3). | Open |
| J15 | Jumper to short AC test points for debugging. It is recommended not to connect this jumper; refer to the Marvell PHY Datasheet. | Two-pin header. | Open |
| J23 | Jumper to provide the VBUS supply to USB when used in host mode. | Two-pin header. | Open |
| **Programming** | | | |
| J32 | JTAG selection jumper to select RVI header or FP4 header for application debug. | Pin 1-2 FP4 for SoftConsole/FlashPro. | Closed |
| | | Pin 2-3 RVI for Keil ULINK or IAR J-Link. | Open |
| | | Pin 2-4 for JTAG_SEL pin to DD1 signal of FT4232H chip. | Open |
| J121 | Jumper to select FTDI JTAG or SPI slave programming. | Pin 1-2 for FTDI JTAG programming. | Closed |
| | | Pin 2-3 for FTDI SPI slave programming. | Open |
| J124 | Jumper to select JTAG programming via FP4 or FTDI. | Pin 1-2 for JTAG programming via FTDI. | Open |
| | | Pin 2-3 for JTAG programming via FP4. | Closed |
| J125 | Jumper to select FTDI SPI-0 or FTDI SPI-1 slave programming | Pin 1-2 for FTDI SPI-1 slave programming. | Open |
| | | Pin 2-3 for FTDI SPI-0 slave programming. | Open |

***Table 3 •*** **Jumper Settings *(continued)***

| | | | |
|---|---|---|---|
| J118 | Jumper to select programming SPI-0 flash through FTDI SPI-0 (Port-B) or SmartFusion2 SPI-0. | Pin 1-2 for programming SPI-0 flash via SmartFusion2 SPI-0. | Closed |
| | | Pin 2-3 for programming SPI-0 flash via FTDI SPI-0 (Port-B). J125 pin 2-3 must be shorted. | Open |
| J119 | Jumper to select programming SPI-1 flash through FTDI SPI (Port-B) or SmartFusion2 SPI-1. | Pin 1-2 for programming SPI-1 flash via SmartFusion2 SPI-1. | Closed |
| | | Pin 2-3 for programming SPI-1 flash via FTDI SPI (Port-B). J125 pin 1-2 must be shorted. | Open |

For locations of various jumpers and test points on the SmartFusion2 Advanced Development Board, see Figure 20, page 43 and Figure 21, page 44.

## 3.2.2 LEDs

The following table lists the power supply and Ethernet LEDs.

***Table 4 •*** **LEDs**

| LED | Description |
|---|---|
| DS26 | Indicates USB_5V supply |
| DS18 | Indicates 0P75V_REG supply |
| DS19 | Indicates 1P5V_REG supply |
| DS20 | Indicates VDD_REG supply |
| DS21 | Indicates 2P5V_LDO supply |
| DS22 | Indicates VCCIO_LPC_VADJ supply |
| DS23 | Indicates VCCIO_HPC_VADJ supply |
| DS24 | Indicates 1P0V_PHY supply |
| DS25 | Indicates 1P8V supply |
| DS28 | Indicates 3P3V_LDO supply |
| DS17 | Indicates 5P0V supply |
| DS29 | Indicates 3P3V supply |
| DS16 | Indicates 12P0V supply |
| DS27 | Indicates VSS_BUS supply |
| DS8 | Indicates that DS8 is connected to parallel LED output port 0 (P0_LED[0]) of Marvell PHY |
| DS9 | Indicates that DS9 is connected to parallel LED output port 0 (P0_LED[2]) of Marvell PHY |
| DS10 | Indicates that DS10 is connected to parallel LED output port 0 (P0_LED[3]) of Marvell PHY |
| DS14 | Indicates that DS14 is connected to parallel LED output port 1 (P1_LED[0]) of Marvell PHY |
| DS13 | Indicates that DS13 is connected to parallel LED output port 1 (P1_LED[1]) of Marvell PHY |
| DS12 | Indicates that DS12 is connected to parallel LED output port 1 (P1_LED[2]) of Marvell PHY |
| DS11 | Indicates that DS11 is connected to parallel LED output port 1 (P1_LED[3]) of Marvell PHY |

### 3.2.3 Test Points

The following table lists USB, ground, and other test points.

***Table 5 •*** **Test Points**

| Test Point | Description |
|---|---|
| TP20, TP33,TP16 | GND |
| TP7 | VDD_REG |
| TP12 | 12 V |
| TP11 | 5 V |
| TP4 | 3.3 V |
| TP29 | VCCIO_HPC_VADJ |
| TP28 | VCCIO_LPC_VADJ |
| TP30 | 3P3V_LDO |
| TP31 | 2P5V_LDO |
| TP9 | 1.5 V |
| TP10 | 0.75 V |
| TP14 | 1.8 V |
| TP27 | VDDIO for the USB device |
| TP24 | PHY 1.0 V |

## 3.3 Power Sources

The following table lists the key power supplies required for normal operation of the SmartFusion2 Advanced Development Kit.

***Table 6 •*** **I/O Voltage Rails**

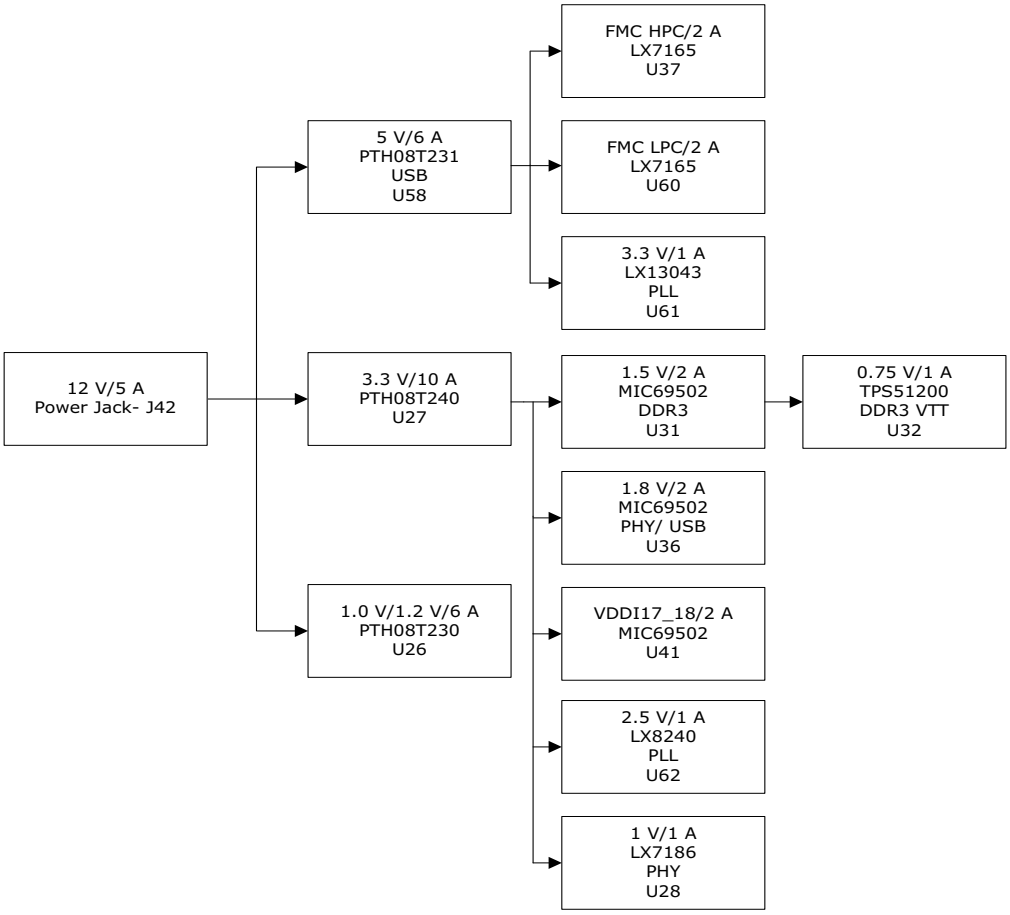
| SmartFusion2 Bank | I/O Rail | Voltage |
|---|---|---|
| Bank0 | VCCIO_HPC_VIO_B_M2S | 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V |
| Bank1 | 2P5V_LDO | 2.5 V |
| Bank2 | 1P5V_REG | 1.5 V |
| Bank3 | 3P3V | 3.3 V |
| Bank4 | 3P3V | 3.3 V |
| Bank5 | VCCIO_HPC_VIO_B_M2S | 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V |
| Bank6 | VCCIO_LPC_VADJ | 2.5 V, 1.8 V, 1.5 V, or 1.2 V |
| Bank7 | 3P3V | 3.3 V |
| Bank8 | VCCIO_LPC_VADJ | 2.5 V, 1.8 V, 1.5 V, or 1.2 V |
| Bank9 | 2P5V_LDO | 2.5 V |
| Bank10 | 2P5V_LDO | 2.5 V |
| Bank11 | VCCIO_HPC_VADJ | 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V |
| Bank12 | 2P5V_LDO | 2.5 V |
| Bank13 | 2P5V_LDO | 2.5 V |
| Bank14 | VCCIO_HPC_VADJ | 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V |

***Table 6 •*** **I/O Voltage Rails *(continued)***

| | | |
|---|---|---|
| Bank15 | VCCIO_LPC_VADJ | 2.5 V, 1.8 V, 1.5 V, or 1.2 V |
| Bank16 | VCCIO_LPC_VADJ | 2.5 V, 1.8 V, 1.5 V, or 1.2 V |
| Bank17 | VCCIO_HPC_VADJ | 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V |
| Bank18 | VCCIO_HPC_VADJ | 3.3 V, 2.5 V, 1.8 V, 1.5 V, or1.2 V |
| VDD | VDD_REG | 1.2 V or 1.0 V |
| VPP | 3P3V_VPP | 3.3 V |
| VREF1 | VREF1 | 0.75 V |
| VREF2 | 0P75V_VTT_REF | 0.75 V |
| SERDES_*x*_PLL_VDDA | PLL_SERDES*x*_VDDA | 3.3 V |
| SERDES_*x*_L01_VDDAPLL | SERDESx_VDDPLL | 2.5 V |
| SERDES_x_VDD | VDD_REG | 1.2 V or 1.0 V |

The following figure shows the voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, and 0.75 V) available in the SmartFusion2 Advanced Development Kit.

***Figure 3 •*** **Voltage Rails in SmartFusion2 Advanced Development Kit**



# 4 Key Components Description and Operation

This section describes the key component interfaces of the SmartFusion2 Advanced Development Kit. For device datasheets, go to *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/smartfusion2-kits*.

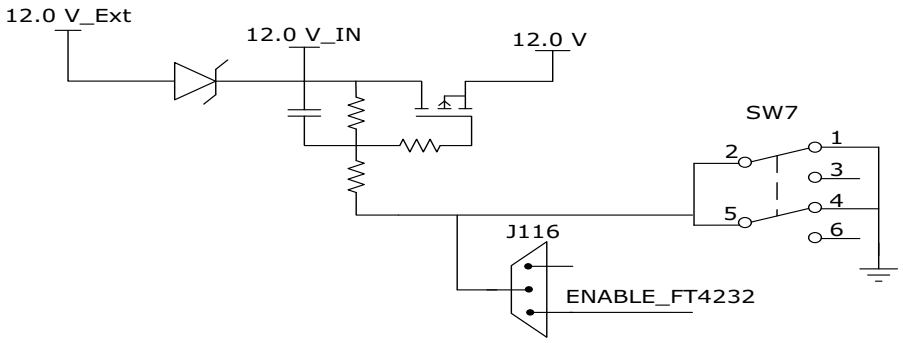
## 4.1 Powering Up the Board

The SmartFusion2 Advanced Development Board is powered using a 12 V external DC jack (12P0V_Ext), as shown in the following figure.

To power up the board:

1. Connect the 12 V power supply brick to the **J42** jumper to supply power to the board.
2. Switch ON the **SW7** power supply switch.

***Figure 4 •*** **Powering Up the Board**




## 4.2 Current Measurement

This section provides information about current sensing in various modes.

### 4.2.1 1.0 V or 1.2 V Current Sensing for Normal Operation

For applications that require current measurement, high-precision operational amplifier circuitry (U59 with gain 100) is provided on the board to measure the output voltage at the **TP17** test point.

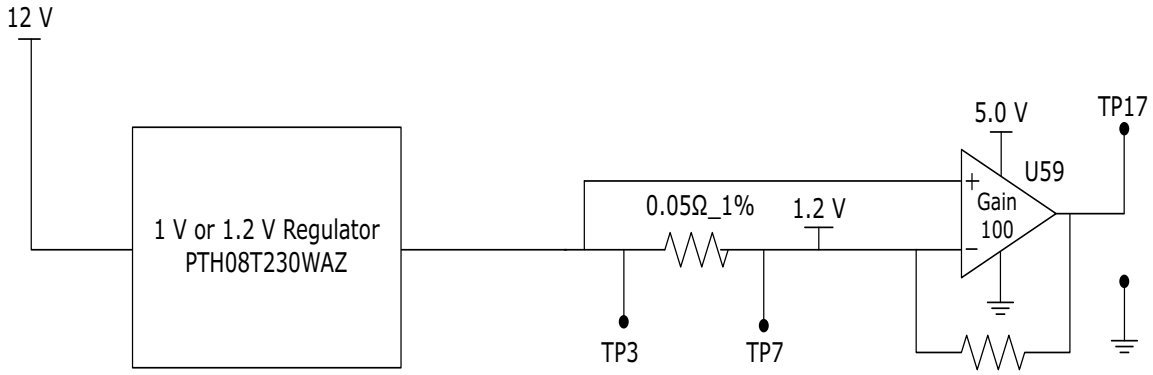
The following steps describe how to measure the core power.

1. Measure the output voltage ($V_{OUT}$) at TP17.
2. I = ($V_{OUT}$/5).
3. Core power consumed (P) = (1.2 V) × I.

For example, when the voltage measured across TP17 is 0.5 V, the core power consumed is 0.12 W.

The following figure shows the on-board core power measurement circuitry.

***Figure 5 •*** **Core Power Measurement Circuitry**




## 4.2.2 1.2 V Current Sensing for Flash*Freeze Mode

The SmartFusion2 device consumes very less power in Flash*Freeze mode. The voltage across the sense resistor (0.05 Ω) must be measured directly using a precision digital multimeter that can read sub-millivolts. The **TP16** and **TP17** test points can be used to directly measure the voltage across the 1.2 V sense resistor.

To convert the voltage measured across a sense resistor to power, use the following equation.

$$\text{Power} = \left(\frac{\text{voltage\_in\_millivolts}}{0.05}\right) \times 1.2$$

**Note:** Accuracy is ± 10%.

# 4.3 Memory Interface

Dedicated I/Os for MSS DDR and fabric DDR are available in the SmartFusion2 device.

## 4.3.1 DDR3 SDRAM

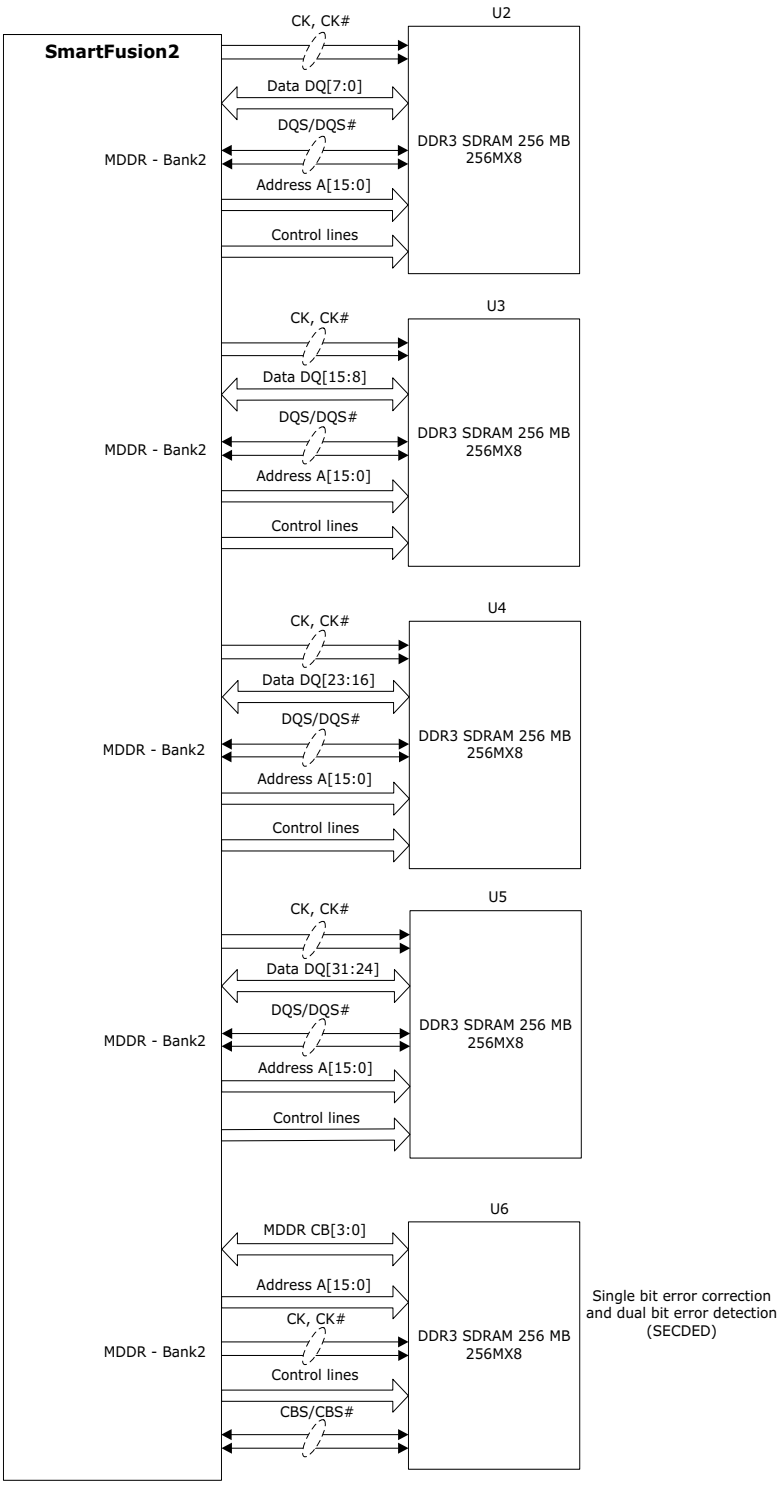
Four chips with 256 MB DDR3 memory are provided in the SmartFusion2 device as flexible volatile memory for user applications. Additionally, one chip with 256 MB DDR3 memory is provided for ECC. You can enable the SECDED feature using ECC. The DDR3 interface is implemented in Bank2.

DDR3 SDRAM specifications for the SmartFusion2 device are as follows.

- MT46H32M16LF: 32 Meg × 8 × 8 banks
- Density: 256 MB
- Clock rate: 800 MHz
- Data rate: DDR3 - 1600
- Total capacity: 1 GB across four chips

The following figure shows the SmartFusion2 memory interface.

***Figure 6 •*** **SmartFusion2 Memory Interface**




For more information, see the Board Level Schematics document (provided separately).

## 4.4 SerDes Interface

The SmartFusion2 Advanced Development Kit has x4 SerDes interfaces. The SerDes block can be accessed using the PCIe edge connector, high-speed sub-miniature version-A (SMA) connectors, and/or an on-board FPGA mezzanine card (FMC) low pin count (LPC) connector (J60).

**Note:** All SerDes TXD pairs (SERDES0, SERDES1, SERDES2, and SERDES3) are capacitively coupled to the SmartFusion2 device. Serial AC-coupling capacitors are used to provide common-mode voltage independence.

For more information, see the Board Level Schematics document (provided separately).

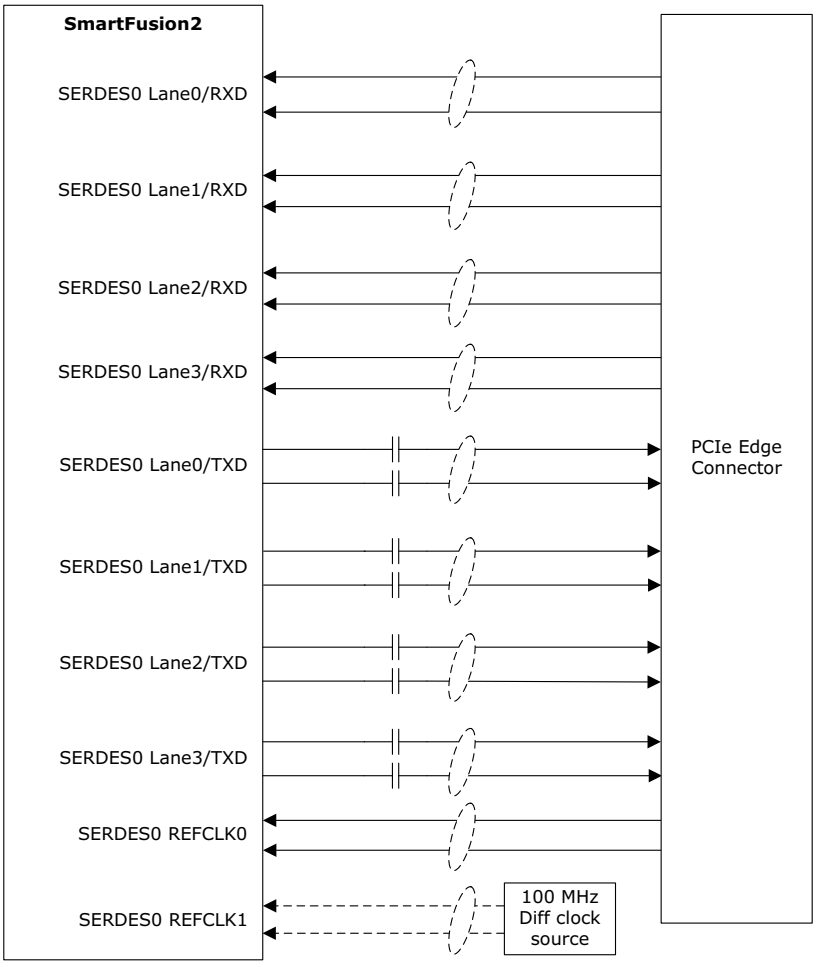
### 4.4.1 SERDES0 Interface

The SERDES0 interface (Lane 0,1, 2, or 3) is directly routed to the PCIe connector. The SerDes reference clocks are routed as follows.

- SERDES0 reference clock 0 is directly routed from the PCIe connector to the SmartFusion2 device.
- SERDES0 reference clock 1 is routed from the 100 MHz differential clock source (LVDS clock oscillator) through resistors.

The following figure shows the SERDES0 interface of the SmartFusion2 Advanced Development Board.

***Figure 7 •*** **SERDES0 Interface**




**Note:** Mount R977 and R978 to source the clock from 100 MHz differential oscillator to the SERDES0 REFCLK1.

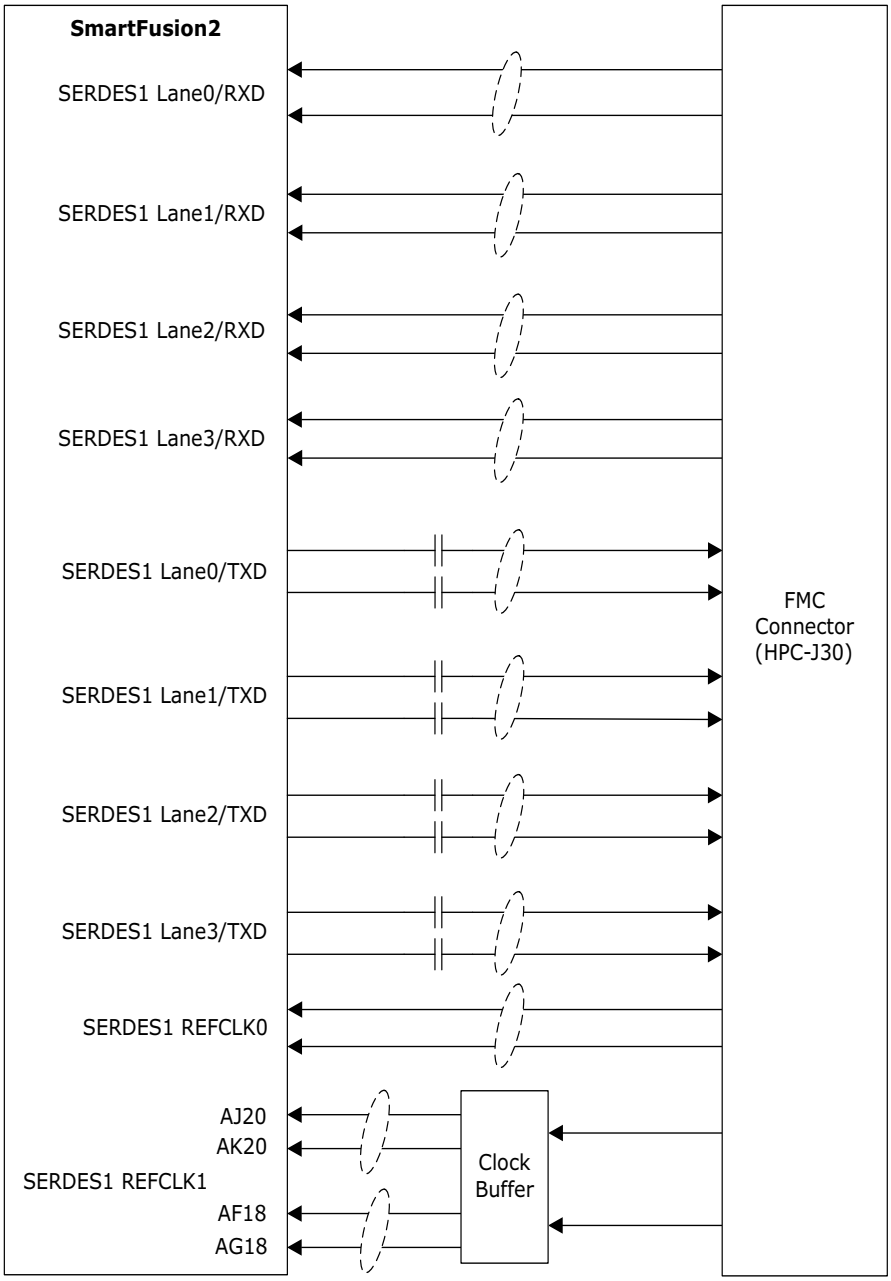
## 4.4.2 SERDES1 Interface

The SERDES1 interface (Lane 0, 1, 2, or 3) is routed to the FMC connector. The SerDes reference clocks are routed as follows.

- SERDES1 reference clock 0 is routed from the FMC connector.
- SERDES1 reference clock 1 is routed from the FMC connector through the clock buffer. The output of the clock buffer is additionally routed to SmartFusion2 Advanced Development Kit board pins AF18 and AG18.

The following figure shows the SERDES1 interface of the SmartFusion2 Advanced Development Board.

***Figure 8 •*** **SERDES1 Interface**



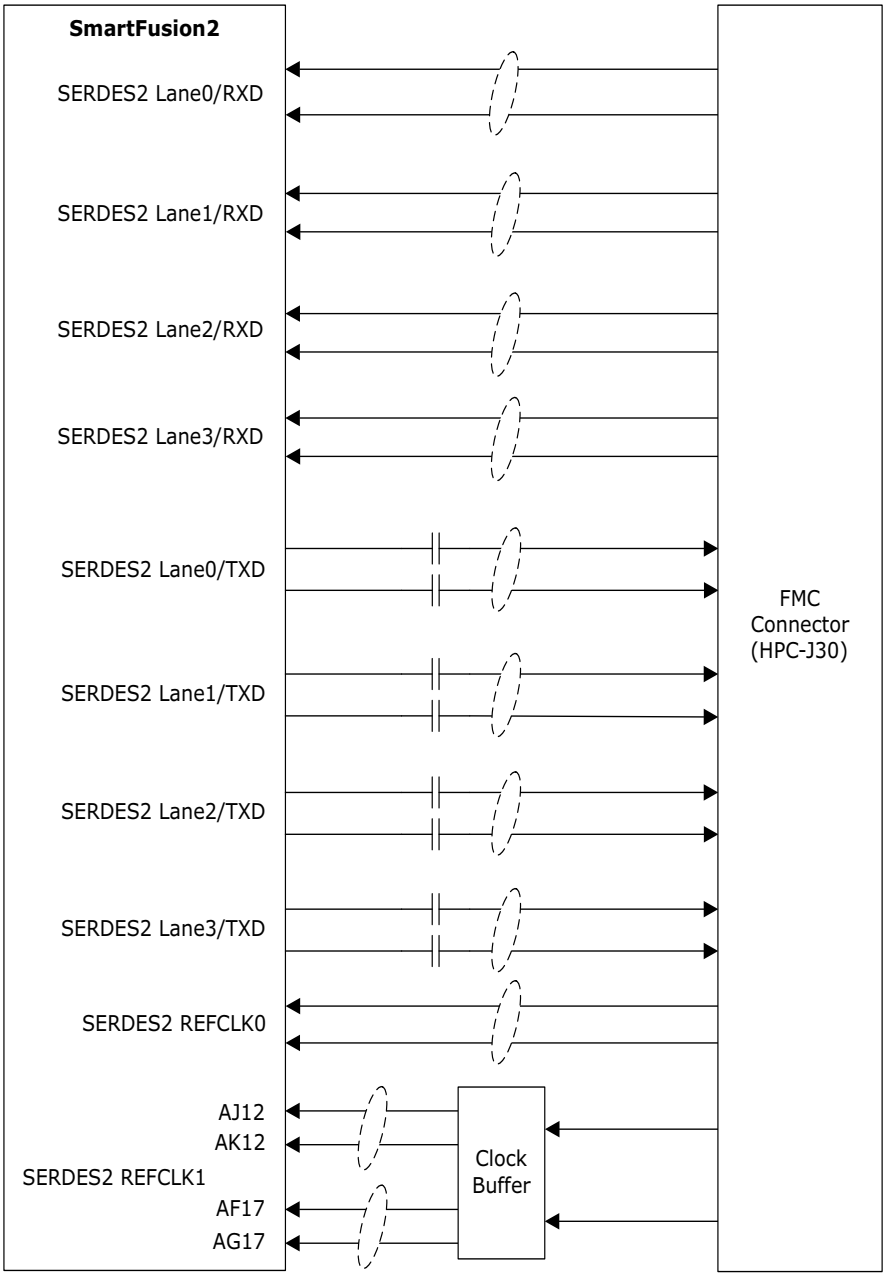
### 4.4.3 SERDES2 Interface

The SERDES2 interface (Lane 0, 1, 2, or 3) is routed to the FMC connector. The SerDes reference clocks are routed as follows.

- SERDES2 reference clock 0 is routed from the FMC connector.
- SERDES2 reference clock 1 is routed from the FMC connector through the clock buffer. The output of the clock buffer is additionally routed to SmartFusion2 Advanced Development Kit board pins AE17 and AF17.

The following figure shows the SERDES2 interface of the SmartFusion2 Advanced Development Board.

***Figure 9 •*** **SERDES2 Interface**



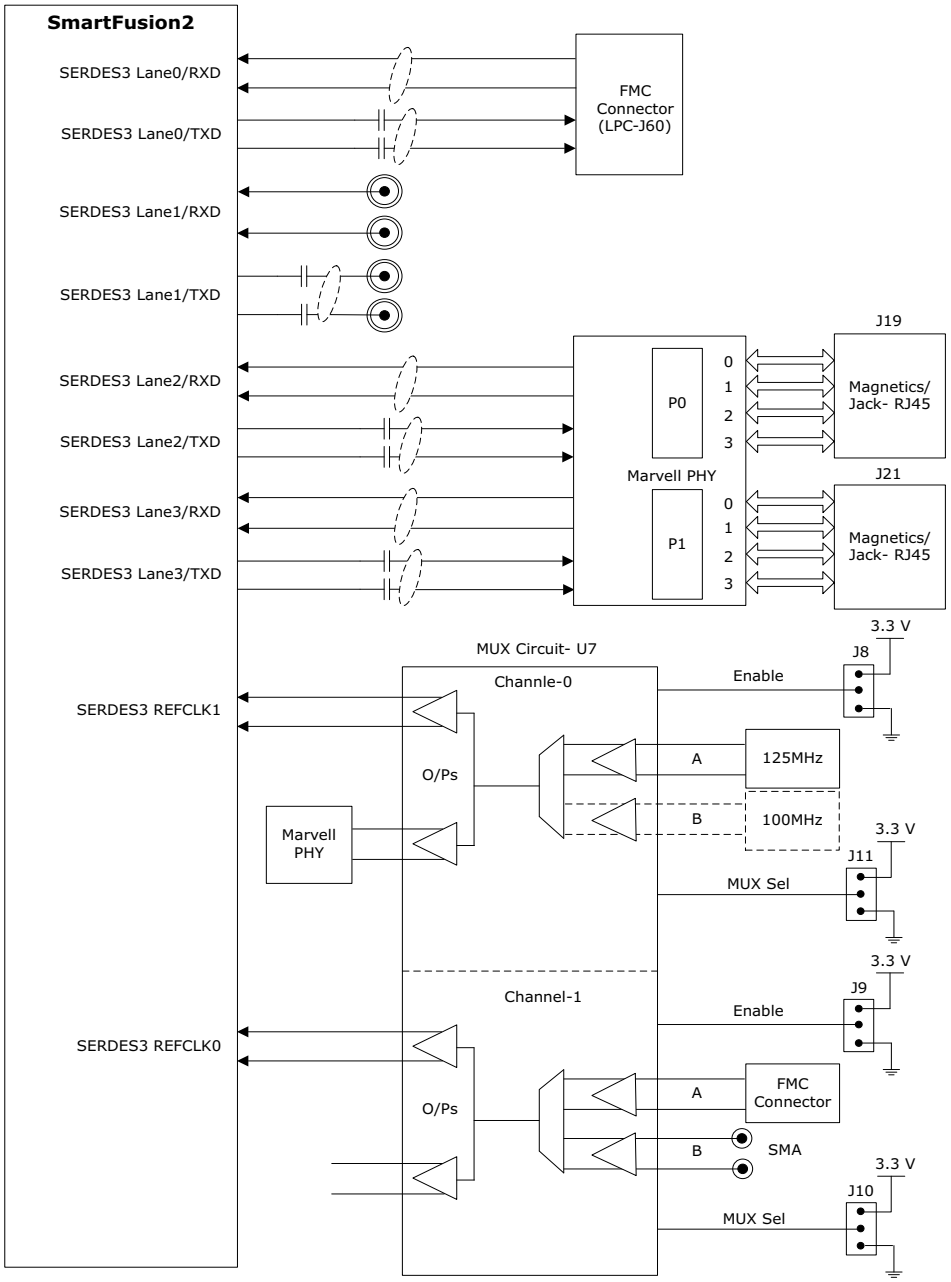
## 4.4.4 SERDES3 Interface

The SERDES3 lanes are connected as follows.

- Lane 0 is connected to the FMC connector.
- Lane 1 is connected to the SMA connectors.
- Lanes 2 and 3 are connected to the Marvell PHY device ports 0 and 1, respectively.
- SERDES3 reference clock 0 is connected from FMC connector or SMA connector through MUX.
- SERDES3 reference clock 1 is connected from 125 MHz or 100 MHz through MUX.

The following figure shows the SERDES3 interface of the SmartFusion2 Advanced Development Board.

***Figure 10 •*** **SERDES3 Interface**

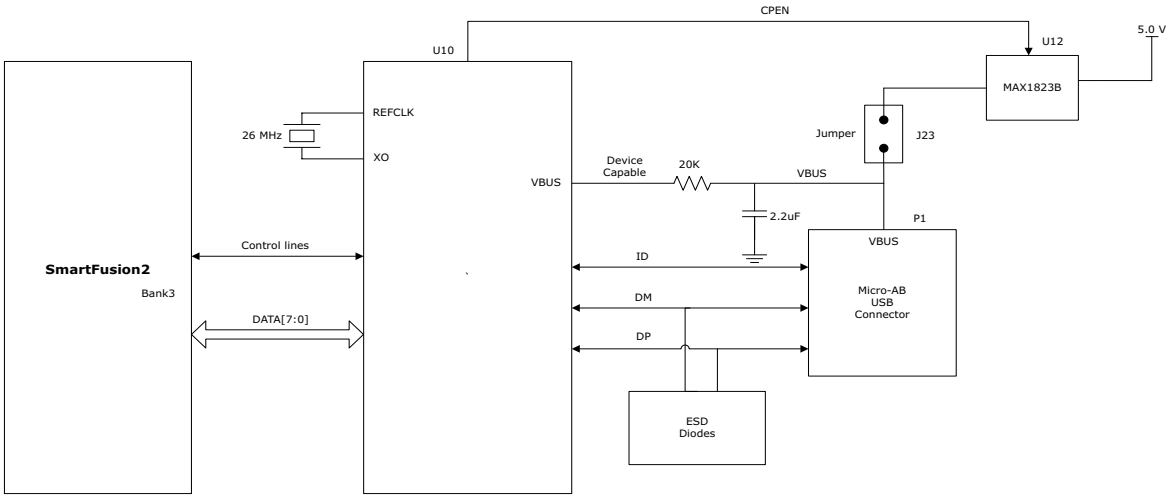


## 4.5 USB Interface

The following figure shows the USB interface of the SmartFusion2 Advanced Development Board. The SMSC USB3320 shown in the following figure is a high-speed USB 2.0 ULPI transceiver that provides the industry standard UTMI+ low pin interface to connect the USB transceiver to the link. CPEN (shown in the figure) is the external 5 V supply enable pin that controls the external VBUS power switch.

In the SmartFusion2 Advanced Development Kit, the USB interface can operate in host, device, and OTG modes. To use device mode, J23 can either be in open or shorted. To use host or OTG mode, pins 1 and 2 of the **J23** jumper must be closed.

***Figure 11 •*** **USB Interface**




For more information, see the Board Level Schematics document (provided separately).

## 4.6 Marvell PHY (88E1340S)

The SmartFusion2 Advanced Development Kit uses the on-board Marvell Alaska PHY device 88E1340S for Ethernet communications at 10 or 1000 Mbps. The device has four independent gigabit Ethernet transceivers; however, the board uses only two of these transceivers. Each transceiver performs all the PHY functions for 100BASE-TX and 1000BASE-T full-duplex or half-duplex Ethernet on a CAT5 twisted-pair cable. The PHY device is connected to a user-provided Ethernet cable through an RJ45 connector with built-in magnetics.

Device 88E1340S supports Quad SGMII for direct connection to a SmartFusion2 chip. It is configured through the CONFIG [3:0] and CLK_SEL [1:0] pins.

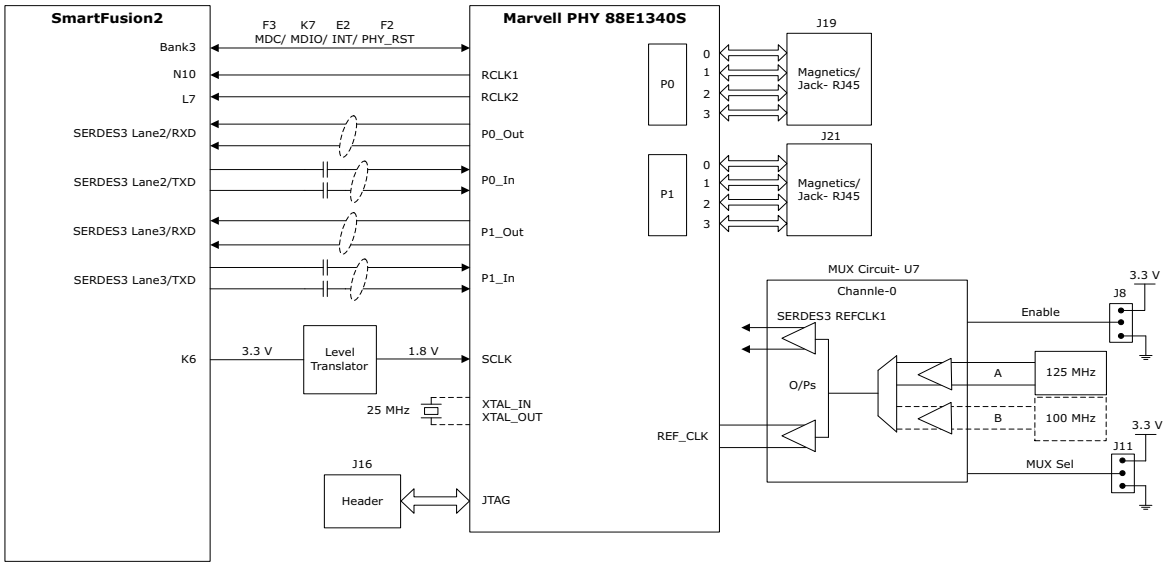
The CLK_SEL [1:0] pin is used to select the reference clock input. On the board, the status of the CLK_SEL0 pin is *high* and the status of the CLK_SEL1 pin is *low*. REF_CLK is a 125 MHz reference differential clock input (Y11). It consists of LVDS differential inputs with a 100 Ω differential internal termination resistor.

Key features of Marvell PHY 88E1340S are as follows.

- RCLK: Gigabit recovered clock
- SCLK: 25 MHz synchronous input reference clock
- Expected reference clock (REF_CLK) specifications:
  - Voltage level: 3.3 (± 0.3) V
  - Differential LVDS
    - Symmetry: 50% (± 10%)
    - Rise/fall time: Maximum 1 ns @ 20% to 80% of supply (3.3 V)
    - Output voltage levels: 0 = 0.90 minimum, 1.10 typical; 1 = 1.43 typical, 1.60 maximum
    - Differential output voltage: 247 mV minimum, 454 mV maximum

The following figure shows the SmartFusion2 Marvell PHY interface.

***Figure 12 •*** **Marvell PHY Interface**




For more information, see the Board Level Schematics document (provided separately).

# 4.7 Programming

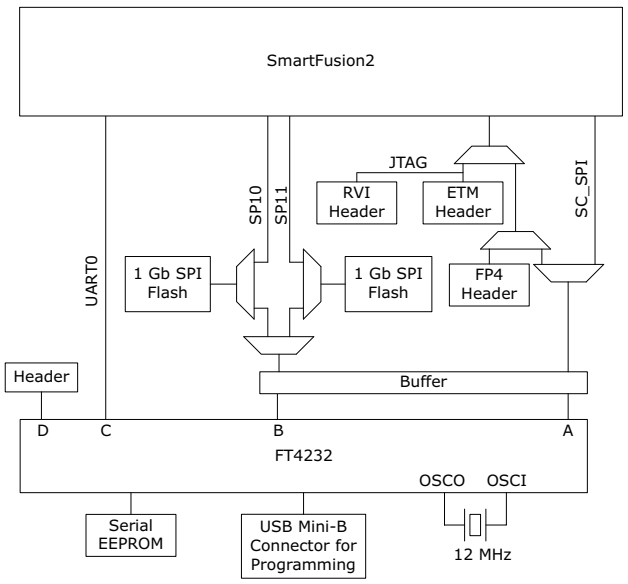
SmartFusion2 SoC FPGAs support multiple programming interfaces and can address a wide range of platform requirements. A SmartFusion2 device can be programmed through the JTAG and SPI interfaces.

The dedicated programming SPI port can operate in SPI slave or SPI master modes.

For more information, see *SmartFusion2 and IGLOO2 Programming User Guide*.

The following figure shows the programming interface of the SmartFusion2 Advanced Development Board.

***Figure 13 •*** **Programming Interface**



**JTAG_SEL:** The JTAG state machine is multiplexed with the CM3 debug port. JTAG_SEL is used to switch between JTAG programming (high) and CM3 debug (low). When using the CM3 debug port, an option is available to switch to serial wire debug port.

**RVI Header:** A 10 × 2 RVI header is provided on the board for debugging. This header allows plugging in the Keil ULINK debugger or IAR J-Link debugger to easily debug or configure the Cortex-M3 processor during board power-up.

**FTDI_JTAG_SEL:** The SmartFusion2 device on the Advanced Development Kit can be programmed either using the JTAG header or the RVI header. FTDI_JTAG_SEL is used to switch between programming the device using the JTAG header (high) or the RVI header (low).

**FLASH_GOLDEN_N:** This signal is always tied high to the 3.3V VCCIO_HPC_VADJ supply. It indicates that the SPI is in slave mode.

**FlashPro4 Programming Header:** The SmartFusion2 device on this Advanced Development Kit can be programmed using a FlashPro4 programmer. In addition, SoftConsole uses FlashPro4 for software debugging.

The following table lists jumpers to be selected for various types of programming.

***Table 7 •*** **Programming Jumper Selection**

| J121 | J124 | J125 | J32 | Function |
|---|---|---|---|---|
| X | X | X | L | IAR debugging |
| X | L | X | H | FP4 JTAG programming |
| H | H | X | H | FTDI JTAG programming (embedded FlashPro5 programming) |
| L | X | X | H | FTDI SPI slave programming |
| X | X | L | X | FTDI SPI-0 programming |
| X | X | H | X | FTDI SPI-1 programming |

For more information, see the Board Level Schematics document (provided separately).

## 4.8 FTDI Interface

The FT4232H chip is a USB 2.0 high-speed (480 Mbps) to UART/MPSSE interface with the following key features.

- Single-chip USB-to-quad serial ports in various configurations
- Entire USB protocol handled on the chip without requiring USB-specific firmware programming
- USB 2.0 high-speed (480 Mbps) and full-speed (12 Mbps) compatibility
- Two MPSSEs on channel A and channel B to simplify synchronous serial protocol (USB to JTAG, I2C, SPI, or bit-bang) design
- Fully assisted hardware handshaking and X-On/X-Off software handshaking
- +1.8 V (chip core) and +3.3 V I/O interfacing with +5 V tolerance

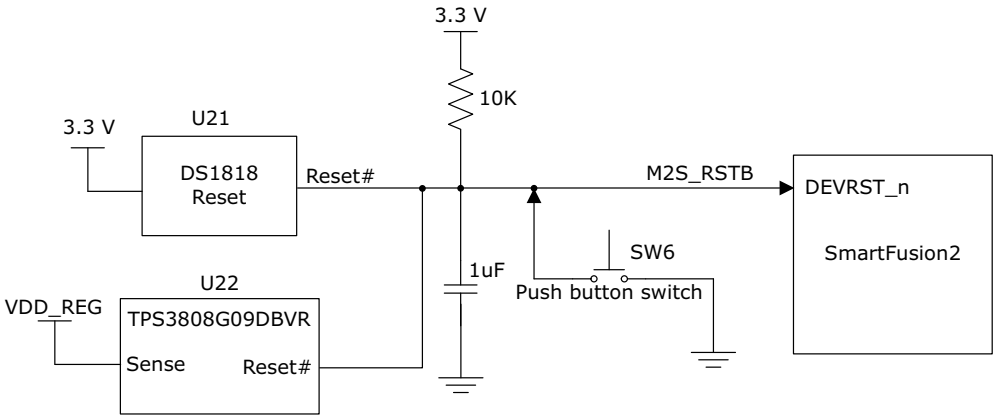
## 4.9 System Reset

The M2S_RSTB signal (active-low) is generated by the **SW6** push-button switch, or by the U21 (DS1818) or U22 (TPS3808G09) chips. DEVRST_N is an input-only reset pad that allows assertion of a full reset to the chip at any time.

DS1818 maintains reset till 150 milliseconds after the 3.3 V supply returns to intolerance. The TPS3808G09DBVR device monitors the voltage at the VDD_REG terminal. If the voltage at this terminal sense-drops below the threshold voltage of 0.9 V, the M2S_RSTB signal is asserted.

The following figure shows the system reset interface of the SmartFusion2 Advanced Development Board.

***Figure 14 •*** **System Reset Interface**




For more information, see the Board Level Schematics document (provided separately).

# 4.10 Clock Sources

This section provides information about the clock sources available in the SmartFusion2 Advanced Development Kit.

## 4.10.1 50 MHz Clock Oscillator

A 50 MHz clock oscillator with an accuracy of +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock.

An on-chip SmartFusion2 PLL can be configured to generate a wide range of high-precision clock frequencies.

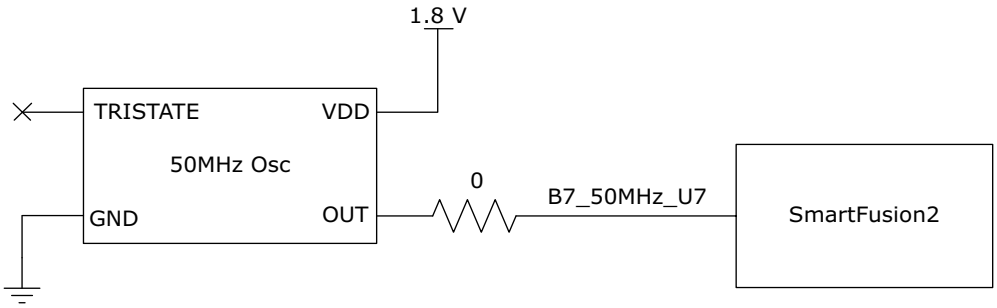
The following table provides package and pin details of the 50 MHz oscillator.

***Table 8 •*** **50 MHz Clock**

| SmartFusion2 Advanced Development Kit Pin Name | SmartFusion2 Package Number | SmartFusion2 Device Pin Name |
|---|---|---|
| 50MHZ_SECLK_B4_P1 | P1 | MSIO39PB4/CCC_NE0_CLKI1 |

The following figure shows the 50 MHz clock oscillator interface.

***Figure 15 •*** **50 MHz Clock Oscillator Interface**




For more information, see the Board Level Schematics document (provided separately).

### 4.10.2 100 MHz Clock Oscillator

A 100 MHz LVDS clock oscillator operating at 3.3 V with an accuracy of +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric M1 and N1 pins.

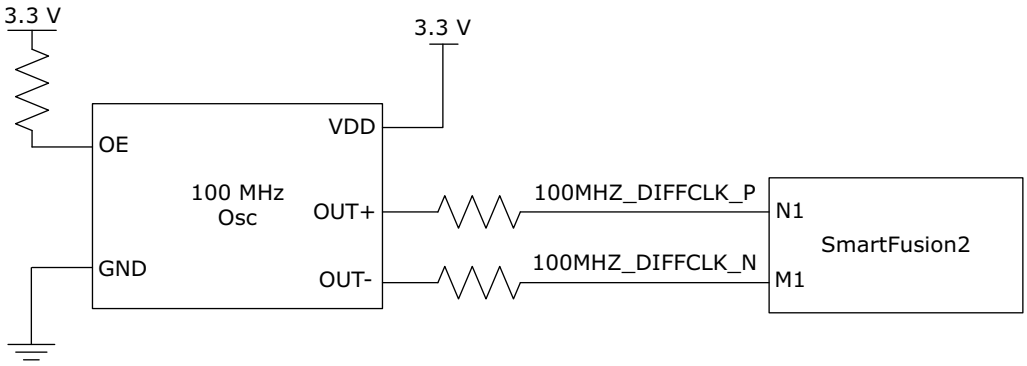
The following table provides package and pin details of the 100 MHz oscillator.

***Table 9 •*** **100 MHz Clock**

| SmartFusion2 Advanced Development Kit Pin Name | SmartFusion2 Package Pin Number | SmartFusion2 Device Pin Name |
|---|---|---|
| 100MHZ_DIFFCLK_P | N1 | MSIO40PB4/CCC_NE1_CLKI1 |
| 100MHZ_DIFFCLK_N | M1 | MSIO40NB4 |

The following figure shows the 100 MHz clock oscillator interface.

***Figure 16 •*** **100 MHz Clock Oscillator Interface**




For more information, see the Board Level Schematics document (provided separately).

## 4.11 User Interface

The SmartFusion2 Advanced Development Board UI has user LEDs as well as push-button switches.

### 4.11.1 User LEDs

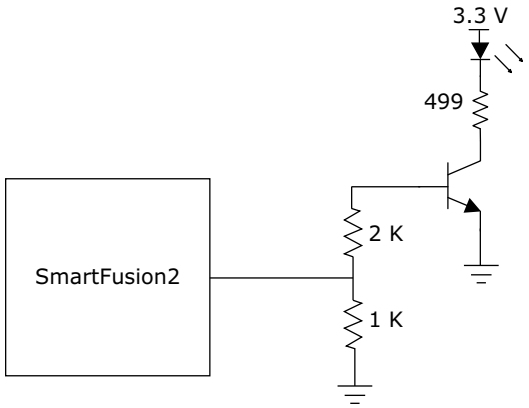
The board has eight active-high LEDs connected to the SmartFusion2 device that can be used to debug applications. The following table lists the on-board user LEDs.

***Table 10 •*** **LEDs**

| SmartFusion2 Advanced Development Board Pin | SmartFusion2 Package Pin Number | SmartFusion2 Device Pin Name |
|---|---|---|
| DS0 | D26 | DDRIO149PB1/FDDR_DQS2 |
| DS1 | F26 | DDRIO150PB1/FDDR_DQ18 |
| DS2 | A27 | DDRIO148PB1/FDDR_DM_RDQS2 |
| DS3 | C26 | DDRIO149NB1/FDDR_DQS2_N |
| DS4 | C28 | DDRIO151PB1/FDDR_DQ16 |
| DS5 | B27 | DDRIO148NB1/FDDR_DQ20 |
| DS6 | C27 | DDRIO151NB1/FDDR_DQ17 |
| DS7 | E26 | DDRIO150NB1/FDDR_DQ19 |

The following figure shows the LED interface of the SmartFusion2 Advanced Development Board.

***Figure 17 •*** **LED Interface**




For more information, see the Board Level Schematics document (provided separately).

## 4.11.2 Push-Button Switches

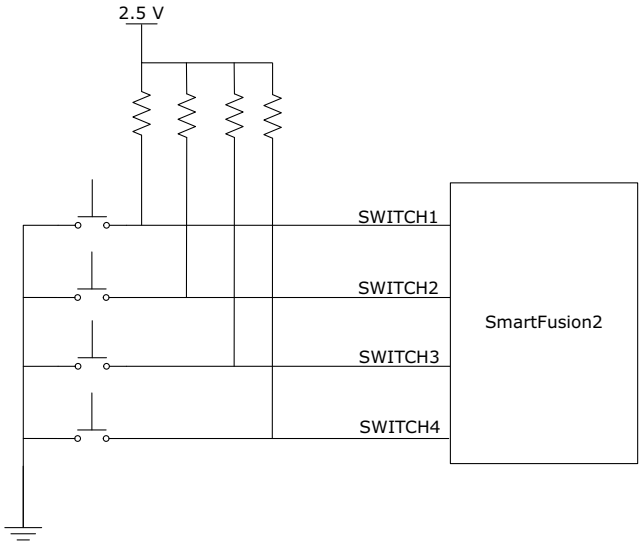
The SmartFusion2 Advanced Development Kit comes with five push-button tactile switches that are connected to the SmartFusion2 device. The following table lists the on-board push-button switches.

***Table 11 •*** **Push-Button Switches**

| SmartFusion2 Advanced Development Board Pin | SmartFusion2 Package Pin Number | SmartFusion2 Device Pin Name |
|---|---|---|
| SWITCH1 | J25 | DDRIO156PB1/FDDR_DQ10 |
| SWITCH2 | H25 | DDRIO156NB1/FDDR_DQ11 |
| SWITCH3 | J24 | DDRIO157PB1/FDDR_DQ8 |
| SWITCH4 | H23 | DDRIO157NB1/FDDR_DQ9 |
| SW6 | AE5 | System Reset |

The following figure shows the switches interface of the SmartFusion2 Advanced Development Board.

***Figure 18 •*** **Switches Interface**




For more information, see the Board Level Schematics document (provided separately).

## 4.11.3 Slide Switches - DPDT

The **SW7** switch powers the device ON or OFF switch from the +12 V external DC jack (J42).

## 4.11.4 DIP Switch - SPST

The **SW5** DIP switch has eight connections to the SmartFusion2 device.

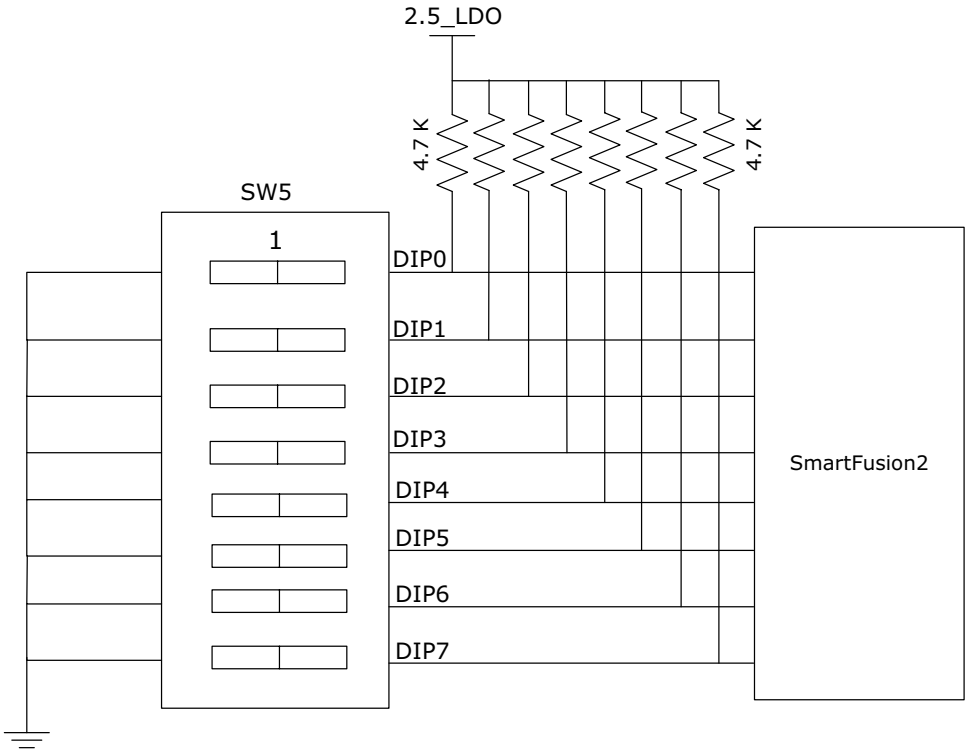
The following table lists the on-board DIP switches.

***Table 12 •*** **DIP Switches**

| SmartFusion2 Advanced Development Board Pin | SmartFusion2 Package Pin Number | SmartFusion2 Device Pin Name |
|---|---|---|
| DIP0 | F25 | DDRIO152PB1/FDDR_DQ14 |
| DIP1 | G25 | DDRIO152NB1/FDDR_DQ15 |
| DIP2 | J23 | DDRIO153PB1/FDDR_DQ12 |
| DIP3 | J22 | DDRIO153NB1/FDDR_DQ13 |
| DIP4 | G27 | DDRIO154PB1/FDDR_TMATCH_0_IN |
| DIP5 | H27 | DDRIO154NB1/FDDR_DM_RDQS1 |
| DIP6 | F23 | DDRIO155PB1/FDDR_DQS1 |
| DIP7 | G23 | DDRIO155NB1/FDDR_DQS1_N |

The following figure shows the SPST interface of the SmartFusion2 Advanced Development Board.

***Figure 19 •*** **SPST Interface**




For more information, see the Board Level Schematics document (provided separately).

## 4.11.5 FMC Connectors

SmartFusion2 Advanced Development Kit has HPC (J30) and LPC (J60) FMC connectors on the board for connecting the daughter cards to enable future expansion of interfaces.

### 4.11.5.1 FMC HPC Connector (J30)

The SmartFusion2 MSIOs from banks 0, 3, 5, 6, 8, 11, 14, 17, and 18, and the SERDES1 and SERDES2 signals are routed to the FMC connector for the application to be developed.

If the FMC daughter board is designed according to VITA standards, Bank0 and Bank5 I/Os draw power from the FMC daughter board. If it is not designed according to VITA standards, these I/Os can be powered from the on-board U37 regulator, by mounting an R1216 resistor.

The following table provides the FMC HPC header pinout details.

***Table 13 •*** **FMC HPC Connector (J30) Pinout**

| FMC Pin Number-J30 | FMC Net Name | SmartFusion2 Pin Number | SmartFusion2 Pin name |
|---|---|---|---|
| A1 | GND | | |
| A2 | FMC_HPC_SERDES2_RXD2_P | AM13 | SERDES_2_RXD2_P |
| A3 | FMC_HPC_SERDES2_RXD2_N | AL13 | SERDES_2_RXD2_N |
| A4 | GND | | |
| A5 | GND | | |
| A6 | FMC_HPC_SERDES2_RXD1_P | AM15 | SERDES_2_RXD1_P |
| A7 | FMC_HPC_SERDES2_RXD1_N | AL15 | SERDES_2_RXD1_N |
| A8 | GND | | |
| A9 | GND | | |
| A10 | FMC_HPC_SERDES2_RXD0_P | AM17 | SERDES_2_RXD0_P |
| A11 | FMC_HPC_SERDES2_RXD0_N | AL17 | SERDES_2_RXD0_N |
| A12 | GND | | |
| A13 | GND | | |
| A14 | FMC_HPC_SERDES1_RXD3_P | AL19 | SERDES_1_RXD3_P |
| A15 | FMC_HPC_SERDES1_RXD3_N | AM19 | SERDES_1_RXD3_N |
| A16 | GND | | |
| A17 | GND | | |
| A18 | FMC_HPC_SERDES1_RXD2_P | AL21 | SERDES_1_RXD2_P |
| A19 | FMC_HPC_SERDES1_RXD2_N | AM21 | SERDES_1_RXD2_N |
| A20 | GND | | |
| A21 | GND | | |
| A22 | FMC_HPC_SERDES2_TXD2_P | AN12 | SERDES_2_TXD2_P |
| A23 | FMC_HPC_SERDES2_TXD2_N | AP12 | SERDES_2_TXD2_N |
| A24 | GND | | |
| A25 | GND | | |
| A26 | FMC_HPC_SERDES2_TXD1_P | AN14 | SERDES_2_TXD1_P |
| A27 | FMC_HPC_SERDES2_TXD1_N | AP14 | SERDES_2_TXD1_N |

***Table 13 •*** **FMC HPC Connector (J30) Pinout *(continued)***

| | | | |
|---|---|---|---|
| A28 | GND | | |
| A29 | GND | | |
| A30 | FMC_HPC_SERDES2_TXD0_P | AN16 | SERDES_2_TXD0_P |
| A31 | FMC_HPC_SERDES2_TXD0_N | AP16 | SERDES_2_TXD0_N |
| A32 | GND | | |
| A33 | GND | | |
| A34 | FMC_HPC_SERDES1_TXD3_P | AP18 | SERDES_1_TXD3_P |
| A35 | FMC_HPC_SERDES1_TXD3_N | AN18 | SERDES_1_TXD3_N |
| A36 | GND | | |
| A37 | GND | | |
| A38 | FMC_HPC_SERDES1_TXD2_P | AP20 | SERDES_1_TXD2_P |
| A39 | FMC_HPC_SERDES1_TXD2_N | AN20 | SERDES_1_TXD2_N |
| A40 | GND | | |
| B1 | NC | | |
| B2 | GND | | |
| B3 | GND | | |
| B4 | NC | | |
| B5 | NC | | |
| B6 | GND | | |
| B7 | GND | | |
| B8 | NC | | |
| B9 | NC | | |
| B10 | GND | | |
| B11 | GND | | |
| B12 | FMC_HPC_SERDES1_RXD0_P | AL25 | SERDES_1_RXD0_P |
| B13 | FMC_HPC_SERDES1_RXD0_N | AM25 | SERDES_1_RXD0_N |
| B14 | GND | | |
| B15 | GND | | |
| B16 | FMC_HPC_SERDES1_RXD1_P | AL23 | SERDES_1_RXD1_P |
| B17 | FMC_HPC_SERDES1_RXD1_N | AM23 | SERDES_1_RXD1_N |
| B18 | GND | | |
| B19 | GND | | |
| B20 | FMC_HPC_SERDES1_REFCLK0_P | AJ22 | MSIOD271PB12/SERDES_1_REFCLK0_P |
| B21 | FMC_HPC_SERDES1_REFCLK0_N | AK22 | MSIOD271NB12/SERDES_1_REFCLK0_N |
| B22 | GND | | |
| B23 | GND | | |
| B24 | NC | | |
| B25 | NC | | |
| B26 | GND | | |

***Table 13 •*** **FMC HPC Connector (J30) Pinout *(continued)***

| | | | |
|---|---|---|---|
| B27 | GND | | |
| B28 | NC | | |
| B29 | NC | | |
| B30 | GND | | |
| B31 | GND | | |
| B32 | FMC_HPC_SERDES1_TXD0_P | AP24 | SERDES_1_TXD0_P |
| B33 | FMC_HPC_SERDES1_TXD0_N | AN24 | SERDES_1_TXD0_N |
| B34 | GND | | |
| B35 | GND | | |
| B36 | FMC_HPC_SERDES1_TXD1_P | AP22 | SERDES_1_TXD1_P |
| B37 | FMC_HPC_SERDES1_TXD1_N | AN22 | SERDES_1_TXD1_N |
| B38 | GND | | |
| B39 | GND | | |
| B40 | NC | | |
| C1 | GND | | |
| C2 | FMC_HPC_SERDES2_TXD3_P | AN10 | SERDES_2_TXD3_P |
| C3 | FMC_HPC_SERDES2_TXD3_N | AP10 | SERDES_2_TXD3_N |
| C4 | GND | | |
| C5 | GND | | |
| C6 | FMC_HPC_SERDES2_RXD3_P | AM11 | SERDES_2_RXD3_P |
| C7 | FMC_HPC_SERDES2_RXD3_N | AL11 | SERDES_2_RXD3_N |
| C8 | GND | | |
| C9 | GND | | |
| C10 | HPC_LA06_M32_191P_B18 | M32 | MSIO191PB18 |
| C11 | HPC_LA06_M31_191N_B18 | M31 | MSIO191NB18 |
| C12 | GND | | |
| C13 | GND | | |
| C14 | HPC_LA10_T23_206P_B17 | T23 | MSIO206PB17 |
| C15 | HPC_LA10_T24_206N_B17 | T24 | MSIO206NB17 |
| C16 | GND | | |
| C17 | GND | | |
| C18 | HPC_LA14_P29_198P_B17 | P29 | MSIO198PB17 |
| C19 | HPC_LA14_P28_198N_B17 | P28 | MSIO198NB17 |
| C20 | GND | | |
| C21 | GND | | |
| C22 | HPC_LA18_CC_U29_215P_B17 | U29 | MSIO215PB17/CCC_NW1_CLKI0 |
| C23 | HPC_LA18_CC_U30_215N_B17 | U30 | MSIO215NB17 |
| C24 | GND | | |
| C25 | GND | | |

***Table 13 •*** **FMC HPC Connector (J30) Pinout *(continued)***

| | | | |
|---|---|---|---|
| C26 | HPC_LA27_P34_208P_B17 | P34 | MSIO208PB17 |
| C27 | HPC_LA27_N34_208N_B17 | N34 | MSIO208NB17 |
| C28 | GND | | |
| C29 | GND | | |
| C30 | I2C0_SCL | K10 | MSIO81NB3/I2C_0_SCL/GPIO_31_B/USB_DATA1_C |
| C31 | I2C0_SDA | K9 | MSIO81PB3/I2C_0_SDA/GPIO_30_B/USB_DATA0_C |
| C32 | GND | | |
| C33 | GND | | |
| C34 | GND | | |
| C35 | 12P0V | | |
| C36 | GND | | |
| C37 | 12P0V | | |
| C38 | GND | | |
| C39 | 3P3V | | |
| C40 | GND | | |
| D1 | HPC_PG_C2M_H6_77N_B3 | H6 | MSIO77NB3/MMUART_0_DSR/GPIO_20_B |
| D2 | GND | | |
| D3 | GND | | |
| D4 | FMC_HPC_SERDES2_REFCLK0_P | AK14 | MSIOD277PB10/SERDES_2_REFCLK0_P |
| D5 | FMC_HPC_SERDES2_REFCLK0_N | AJ14 | MSIOD277NB10/SERDES_2_REFCLK0_N |
| D6 | GND | | |
| D7 | GND | | |
| D8 | HPC_LA01_CC_U27_216P_B17 | U27 | MSIO216PB17/CCC_NW0_CLKI0 |
| D9 | HPC_LA01_CC_U26_216N_B17 | U26 | MSIO216NB17 |
| D10 | GND | | |
| D11 | HPC_LA05_N23_186P_B18 | N23 | MSIO186PB18 |
| D12 | HPC_LA05_N24_186N_B18 | N24 | MSIO186NB18 |
| D13 | GND | | |
| D14 | HPC_LA09_R23_200P_B17 | R23 | MSIO200PB17 |
| D15 | HPC_LA09_R24_200N_B17 | R24 | MSIO200NB17 |
| D16 | GND | | |
| D17 | HPC_LA13_R26_202P_B17 | R26 | MSIO202PB17 |
| D18 | HPC_LA13_R25_202N_B17 | R25 | MSIO202NB17 |
| D19 | GND | | |
| D20 | HPC_LA17_CC_U31_213P_B17 | U31 | MSIO213PB17/GB6/CCC_NW1_CLKI1 |
| D21 | HPC_LA17_CC_U32_213N_B17 | U32 | MSIO213NB17 |
| D22 | GND | | |
| D23 | HPC_LA23_T33_212P_B17 | T33 | MSIO212PB17 |

***Table 13 •*** **FMC HPC Connector (J30) Pinout *(continued)***

| | | | |
|---|---|---|---|
| D24 | HPC_LA23_T32_212N_B17 | T32 | MSIO212NB17 |
| D25 | GND | | |
| D26 | HPC_LA26_L33_190P_B18 | L33 | MSIO190PB18 |
| D27 | HPC_LA26_L32_190N_B18 | L32 | MSIO190NB18 |
| D28 | GND | | |
| D29 | HPC_TCK | | |
| D30 | HPC_TDI | | |
| D31 | HPC_TDO | | |
| D32 | 3P3V | | |
| D33 | HPC_TMS | | |
| D34 | HPC_TRST_L | | |
| D35 | GND | | |
| D36 | 3P3V | | |
| D37 | GND | | |
| D38 | 3P3V | | |
| D39 | GND | | |
| D40 | 3P3V | | |
| E1 | GND | | |
| E2 | HPC_HA01_CC_AF16_276P_B11 | AF16 | MSIO276PB11/GB11/VCCC_SE0_CLKI |
| E3 | HPC_HA01_CC_AG16_276N_B11 | AG16 | MSIO276NB11 |
| E4 | GND | | |
| E5 | GND | | |
| E6 | HPC_HA05_AA3_17P_B6 | AA3 | MSIO17PB6 |
| E7 | HPC_HA05_AA2_17N_B6 | AA2 | MSIO17NB6 |
| E8 | GND | | |
| E9 | HPC_HA09_AJ2_285P_B8 | AJ2 | MSIO285PB8 |
| E10 | HPC_HA09_AH3_285N_B8 | AH3 | MSIO285NB8 |
| E11 | GND | | |
| E12 | HPC_HA13_AH6_283P_B8 | AH6 | MSIO283PB8 |
| E13 | HPC_HA13_AH5_283N_B8 | AH5 | MSIO283NB8 |
| E14 | GND | | |
| E15 | HPC_HA16_AG7_284P_B8 | AG7 | MSIO284PB8 |
| E16 | HPC_HA16_AF7_284N_B8 | AF7 | MSIO284NB8 |
| E17 | GND | | |
| E18 | HPC_HA20_AB8_8P_B6 | AB8 | MSIO8PB6 |
| E19 | HPC_HA20_AB7_8N_B6 | AB7 | MSIO8NB6 |
| E20 | GND | | |
| E21 | HPC_HB03_W1_20P_B5 | W1 | MSIO20PB5 |
| E22 | HPC_HB03_W2_20N_B5 | W2 | MSIO20NB5 |

***Table 13 •*** **FMC HPC Connector (J30) Pinout *(continued)***

| | | | |
|---|---|---|---|
| E23 | GND | | |
| E24 | HPC_HB05_Y2_19P_B5 | Y2 | MSIO19PB5 |
| E25 | HPC_HB05_Y1_19N_B5 | Y1 | MSIO19NB5 |
| E26 | GND | | |
| E27 | HPC_HB09_V4_30P_B5 | V4 | MSIO30PB5/USB_DATA0_B |
| E28 | HPC_HB09_V5_30N_B5 | V5 | MSIO30NB5/USB_DATA1_B |
| E29 | GND | | |
| E30 | HPC_HB13_U2_29P_B5 | U2 | MSIO29PB5/USB_STP_B |
| E31 | HPC_HB13_U3_29N_B5 | U3 | MSIO29NB5/USB_NXT_B |
| E32 | GND | | |
| E33 | HPC_HB19_H31_175P_B0 | H31 | MSIO175PB0 |
| E34 | HPC_HB19_G31_175N_B0 | G31 | MSIO175NB0 |
| E35 | GND | | |
| E36 | HPC_HB21_L25_174P_B0 | L25 | MSIO174PB0 |
| E37 | HPC_HB21_L26_174N_B0 | L26 | MSIO174NB0 |
| E38 | GND | | |
| E39 | VCCIO_HPC_VADJ | | |
| E40 | GND | | |
| F1 | HPC_PG_M2C_J6_78P_B3 | J6 | MSIO78PB3/MMUART_0_RI/GPIO_21_B |
| F2 | GND | | |
| F3 | GND | | |
| F4 | HPC_HA00_CC_AJ4_282P_B8 | AJ4 | MSIO282PB8/VCCC_SE1_CLKI |
| F5 | HPC_HA00_CC_AJ3_282N_B8 | AJ3 | MSIO282NB8 |
| F6 | GND | | |
| F7 | HPC_HA04_AG3_287P_B8 | AG3 | MSIO287PB8 |
| F8 | HPC_HA04_AG4_287N_B8 | AG4 | MSIO287NB8 |
| F9 | GND | | |
| F10 | HPC_HA08_AD1_9P_B6 | AD1 | MSIO9PB6 |
| F11 | HPC_HA08_AC1_9N_B6 | AC1 | MSIO9NB6 |
| F12 | GND | | |
| F13 | HPC_HA12_AE4_4P_B6 | AE4 | MSIO4PB6 |
| F14 | HPC_HA12_AD4_4N_B6 | AD4 | MSIO4NB6 |
| F15 | GND | | |
| F16 | HPC_HA15_AA7_15P_B6 | AA7 | MSIO15PB6 |
| F17 | HPC_HA15_Y7_15N_B6 | Y7 | MSIO15NB6 |
| F18 | GND | | |
| F19 | HPC_HA19_AB10_11P_B6 | AB10 | MSIO11PB6 |
| F20 | HPC_HA19_AA10_11N_B6 | AA10 | MSIO11NB6 |
| F21 | GND | | |

***Table 13 •*** **FMC HPC Connector (J30) Pinout *(continued)***

| | | | |
|---|---|---|---|
| F22 | HPC_HB02_V1_26P_B5 | V1 | MSIO26PB5/GPIO_27_A |
| F23 | HPC_HB02_U1_26N_B5 | U1 | MSIO26NB5/GPIO_28_A |
| F24 | GND | | |
| F25 | HPC_HB04_W3_25P_B5 | W3 | MSIO25PB5 |
| F26 | HPC_HB04_V3_25N_B5 | V3 | MSIO25NB5 |
| F27 | GND | | |
| F28 | HPC_HB08_Y6_18P_B5 | Y6 | MSIO18PB5 |
| F29 | HPC_HB08_Y5_18N_B5 | Y5 | MSIO18NB5 |
| F30 | GND | | |
| F31 | HPC_HB12_W8_27P_B5 | W8 | MSIO27PB5 |
| F32 | HPC_HB12_W9_27N_B5 | W9 | MSIO27NB5/USB_DATA7_B |
| F33 | GND | | |
| F34 | HPC_HB16_Y12_21P_B5 | Y12 | MSIO21PB5 |
| F35 | HPC_HB16_Y11_21N_B5 | Y11 | MSIO21NB5 |
| F36 | GND | | |
| F37 | HPC_HB20_W12_28P_B5 | W12 | MSIO28PB5/USB_XCLK_B |
| F38 | HPC_HB20_W11_28N_B5 | W11 | MSIO28NB5/USB_DIR_B |
| F39 | GND | | |
| F40 | VCCIO_HPC_VADJ | | |
| G1 | GND | | |
| G2 | HPC_CLK1_M2C_AH28_267P_B14 | AH28 | MSIO267PB14/CCC_SW0_CLKI2 |
| G3 | HPC_CLK1_M2C_AG27_267N_B14 | AG27 | MSIO267NB14 |
| G4 | GND | | |
| G5 | GND | | |
| G6 | HPC_LA00_CC_U23_214P_B17 | U23 | MSIO214PB17/GB2/CCC_NW0_CLKI1 |
| G7 | HPC_LA00_CC_U24_214N_B17 | U24 | MSIO214NB17 |
| G8 | GND | | |
| G9 | HPC_LA03_N32_201P_B17 | N32 | MSIO201PB17 |
| G10 | HPC_LA03_N31_201N_B17 | N31 | MSIO201NB17 |
| G11 | GND | | |
| G12 | HPC_LA08_M25_181P_B18 | M25 | MSIO181PB18 |
| G13 | HPC_LA08_M24_181N_B18 | M24 | MSIO181NB18 |
| G14 | GND | | |
| G15 | HPC_LA12_M27_183P_B18 | M27 | MSIO183PB18 |
| G16 | HPC_LA12_M26_183N_B18 | M26 | MSIO183NB18 |
| G17 | GND | | |
| G18 | HPC_LA16_T28_209P_B17 | T28 | MSIO209PB17 |
| G19 | HPC_LA16_T27_209N_B17 | T27 | MSIO209NB17 |
| G20 | GND | | |

***Table 13 •*** **FMC HPC Connector (J30) Pinout *(continued)***

| | | | |
|---|---|---|---|
| G21 | HPC_LA20_R31_205P_B17 | R31 | MSIO205PB17 |
| G22 | HPC_LA20_R30_205N_B17 | R30 | MSIO205NB17 |
| G23 | GND | | |
| G24 | HPC_LA22_R33_207P_B17 | R33 | MSIO207PB17 |
| G25 | HPC_LA22_R32_207N_B17 | R32 | MSIO207NB17 |
| G26 | GND | | |
| G27 | HPC_LA25_M34_197P_B17 | M34 | MSIO197PB17 |
| G28 | HPC_LA25_L34_197N_B17 | L34 | MSIO197NB17 |
| G29 | GND | | |
| G30 | HPC_LA29_J34_194P_B18 | J34 | MSIO194PB18 |
| G31 | HPC_LA29_J33_194N_B18 | J33 | MSIO194NB18 |
| G32 | GND | | |
| G33 | HPC_LA31_H34_196P_B18 | H34 | MSIO196PB18 |
| G34 | HPC_LA31_G34_196N_B18 | G34 | MSIO196NB18 |
| G35 | GND | | |
| G36 | HPC_LA33_E33_176P_B18 | E33 | MSIO176PB18 |
| G37 | HPC_LA33_D33_176N_B18 | D33 | MSIO176NB18 |
| G38 | GND | | |
| G39 | VCCIO_HPC_VADJ | | |
| G40 | GND | | |
| H1 | N36608719 | | |
| H2 | HPC_PRSNT_M2CL_J7_78N_B3 | J7 | MSIO78NB3/MMUART_0_DCD/GPIO_22_B |
| H3 | GND | | |
| H4 | HPC_CLK0_M2C_AJ6_281P_B8 | AJ6 | MSIO281PB8/GB15/VCCC_SE1_CLKI |
| H5 | HPC_CLK0_M2C_AJ5_281N_B8 | AJ5 | MSIO281NB8 |
| H6 | GND | | |
| H7 | HPC_LA02_K31_179P_B18 | K31 | MSIO179PB18 |
| H8 | HPC_LA02_K30_179N_B18 | K30 | MSIO179NB18 |
| H9 | GND | | |
| H10 | HPC_LA04_L30_182P_B18 | L30 | MSIO182PB18 |
| H11 | HPC_LA04_L29_182N_B18 | L29 | MSIO182NB18 |
| H12 | GND | | |
| H13 | HPC_LA07_P23_192P_B18 | P23 | MSIO192PB18 |
| H14 | HPC_LA07_P24_192N_B18 | P24 | MSIO192NB18 |
| H15 | GND | | |
| H16 | HPC_LA11_T30_210P_B17 | T30 | MSIO210PB17 |
| H17 | HPC_LA11_T29_210N_B17 | T29 | MSIO210NB17 |
| H18 | GND | | |
| H19 | HPC_LA15_M30_188P_B18 | M30 | MSIO188PB18 |

***Table 13 •*** **FMC HPC Connector (J30) Pinout *(continued)***

| | | | |
|---|---|---|---|
| H20 | HPC_LA15_M29_188N_B18 | M29 | MSIO188NB18 |
| H21 | GND | | |
| H22 | HPC_LA19_P31_199P_B17 | P31 | MSIO199PB17 |
| H23 | HPC_LA19_P30_199N_B17 | P30 | MSIO199NB17 |
| H24 | GND | | |
| H25 | HPC_LA21_P33_203P_B17 | P33 | MSIO203PB17 |
| H26 | HPC_LA21_N33_203N_B17 | N33 | MSIO203NB17 |
| H27 | GND | | |
| H28 | HPC_LA24_K33_187P_B18 | K33 | MSIO187PB18 |
| H29 | HPC_LA24_K32_187N_B18 | K32 | MSIO187NB18 |
| H30 | GND | | |
| H31 | HPC_LA28_H33_184P_B18 | H33 | MSIO184PB18 |
| H32 | HPC_LA28_H32_184N_B18 | H32 | MSIO184NB18 |
| H33 | GND | | |
| H34 | HPC_LA30_F34_185P_B18 | F34 | MSIO185PB18 |
| H35 | HPC_LA30_F33_185N_B18 | F33 | MSIO185NB18 |
| H36 | GND | | |
| H37 | HPC_LA32_D34_180P_B18 | D34 | MSIO180PB18 |
| H38 | HPC_LA32_C34_180N_B18 | C34 | MSIO180NB18 |
| H39 | GND | | |
| H40 | VCCIO_HPC_VADJ | | |
| J1 | GND | | |
| J2 | HPC_CLK3_M2C_P | AK12 | MSIOD278PB10/SERDES_2_REFCLK1_P |
| J2 | HPC_CLK3_M2C_P | AE17 | MSIO275PB11/VCCC_SE0_CLKI |
| J3 | HPC_CLK3_M2C_N | AJ12 | MSIOD278NB10/SERDES_2_REFCLK1_N |
| J3 | HPC_CLK3_M2C_N | AF17 | MSIO275NB11 |
| J4 | GND | | |
| J5 | GND | | |
| J6 | HPC_HA03_AA4_12P_B6 | AA4 | MSIO12PB6 |
| J7 | HPC_HA03_AA5_12N_B6 | AA5 | MSIO12NB6 |
| J8 | GND | | |
| J9 | HPC_HA07_AC3_10P_B6 | AC3 | MSIO10PB6 |
| J10 | HPC_HA07_AB3_10N_B6 | AB3 | MSIO10NB6 |
| J11 | GND | | |
| J12 | HPC_HA11_AD3_5P_B6 | AD3 | MSIO5PB6 |
| J13 | HPC_HA11_AD2_5N_B6 | AD2 | MSIO5NB6 |
| J14 | GND | | |
| J15 | HPC_HA14_AG6_286P_B8 | AG6 | MSIO286PB8 |
| J16 | HPC_HA14_AG5_286N_B8 | AG5 | MSIO286NB8 |

***Table 13 •*** **FMC HPC Connector (J30) Pinout *(continued)***

| | | | |
|---|---|---|---|
| J17 | GND | | |
| J18 | HPC_HA18_AC9_3P_B6 | AC9 | MSIO3PB6 |
| J19 | HPC_HA18_AC8_3N_B6 | AC8 | MSIO3NB6 |
| J20 | GND | | |
| J21 | HPC_HA22_AA8_13P_B6 | AA8 | MSIO13PB6 |
| J22 | HPC_HA22_AA9_13N_B6 | AA9 | MSIO13NB6 |
| J23 | GND | | |
| J24 | HPC_HB01_R1_32P_B5 | R1 | MSIO32PB5/USB_DATA4_B |
| J25 | HPC_HB01_R2_32N_B5 | R2 | MSIO32NB5/USB_DATA5_B |
| J26 | GND | | |
| J27 | HPC_HB07_Y4_24P_B5 | Y4 | MSIO24PB5 |
| J28 | HPC_HB07_W4_24N_B5 | W4 | MSIO24NB5 |
| J29 | GND | | |
| J30 | HPC_HB11_W6_23P_B5 | W6 | MSIO23PB5 |
| J31 | HPC_HB11_W7_23N_B5 | W7 | MSIO23NB5 |
| J32 | GND | | |
| J33 | HPC_HB15_V9_34P_B5 | V9 | MSIO34PB5 |
| J34 | HPC_HB15_V10_34N_B5 | V10 | MSIO34NB5 |
| J35 | GND | | |
| J36 | HPC_HB18_T2_31P_B5 | T2 | MSIO31PB5/USB_DATA2_B |
| J37 | HPC_HB18_T3_31N_B5 | T3 | MSIO31NB5/USB_DATA3_B |
| J38 | GND | | |
| J39 | VCCIO_HPC_VIO_B_M2C_FMC | | |
| J40 | GND | | |
| K1 | N36626276 | | |
| K2 | GND | | |
| K3 | GND | | |
| K4 | HPC_CLK2_M2C_P | AJ20 | MSIOD272PB12/SERDES_1_REFCLK1_P |
| K4 | HPC_CLK2_M2C_P | AF18 | MSIO274PB11/CCC_SW1_CLKI2 |
| K5 | HPC_CLK2_M2C_N | AK20 | MSIOD272NB12/SERDES_1_REFCLK1_N |
| K5 | HPC_CLK2_M2C_N | AG18 | MSIO274NB11/CCC_SW1_CLKI3 |
| K6 | GND | | |
| K7 | HPC_HA02_AB2_16P_B6 | AB2 | MSIO16PB6 |
| K8 | HPC_HA02_AB1_16N_B6 | AB1 | MSIO16NB6 |
| K9 | GND | | |
| K10 | HPC_HA06_AC5_6P_B6 | AC5 | MSIO6PB6 |
| K11 | HPC_HA06_AC4_6N_B6 | AC4 | MSIO6NB6 |
| K12 | GND | | |
| K13 | HPC_HA10_AE6_288P_B8 | AE6 | MSIO288PB8 |

***Table 13 •*** **FMC HPC Connector (J30) Pinout *(continued)***

| | | | |
|---|---|---|---|
| K14 | HPC_HA10_AF5_288N_B8 | AF5 | MSIO288NB8 |
| K15 | GND | | |
| K16 | HPC_HA17_CC_AJ29_268P_B14 | AJ29 | MSIO268PB14/GB3/CCC_SW0_CLKI3 |
| K17 | HPC_HA17_CC_AJ28_268N_B14 | AJ28 | MSIO268NB14 |
| K18 | GND | | |
| K19 | HPC_HA21_AA12_14P_B6 | AA12 | MSIO14PB6 |
| K20 | HPC_HA21_AA11_14N_B6 | AA11 | MSIO14NB6 |
| K21 | GND | | |
| K22 | HPC_HA23_AB5_7P_B6 | AB5 | MSIO7PB6 |
| K23 | HPC_HA23_AB6_7N_B6 | AB6 | MSIO7NB6 |
| K24 | GND | | |
| K25 | HPC_HB00_CC_F32_172P_B0 | F32 | MSIO172PB0/GB0/CCC_NW0_CLKI3 |
| K26 | HPC_HB00_CC_E32_172N_B0 | E32 | MSIO172NB0 |
| K27 | GND | | |
| K28 | HPC_HB06_CC_J29_170P_B0 | J29 | MSIO170PB0/CCC_NW1_CLKI3 |
| K29 | HPC_HB06_CC_J28_170N_B0 | J28 | MSIO170NB0 |
| K30 | GND | | |
| K31 | HPC_HB10_Y10_22P_B5 | Y10 | MSIO22PB5 |
| K32 | HPC_HB10_Y9_22N_B5 | Y9 | MSIO22NB5 |
| K33 | GND | | |
| K34 | HPC_HB14_V6_33P_B5 | V6 | MSIO33PB5/USB_DATA6_B |
| K35 | HPC_HB14_U6_33N_B5 | U6 | MSIO33NB5 |
| K36 | GND | | |
| K37 | HPC_HB17_CC_U5_37P_B5 | U5 | MSIO37PB5/GB9/VCCC_SE0_CLKI |
| K38 | HPC_HB17_CC_T5_37N_B5 | T5 | MSIO37NB5 |
| K39 | GND | | |
| K40 | VCCIO_HPC_VIO_B_M2C_FMC | | |

### 4.11.5.2 FMC LPC Connector (J60)

The SmartFusion2 MSIODs from banks 15 and 16 and the SERFDES3 lane 0 signals are routed to the FMC connector for the application to be developed.

The following table provides the FMC LPC header pinout details.

***Table 14 •*** **FMC LPC Connector (J60) Pinout**

| FMC Pin Number - J60 | FMC Net Name | SmartFusion2 Pin Number | SmartFusion2 Pin Name |
|---|---|---|---|
| C1 | GND | | |
| C2 | FMC_LPC_SERDES3_TXD0_P | AN8 | SERDES_3_TXD0_P |
| C3 | FMC_LPC_SERDES3_TXD0_N | AP8 | SERDES_3_TXD0_N |
| C4 | GND | | |
| C5 | GND | | |
| C6 | FMC_LPC_SERDES3_RXD0_P | AM9 | SERDES_3_RXD0_P |
| C7 | FMC_LPC_SERDES3_RXD0_N | AL9 | SERDES_3_RXD0_N |
| C8 | GND | | |
| C9 | GND | | |
| C10 | LPC_LA06_AF33_248P_B15 | AF33 | MSIOD248PB15 |
| C11 | LPC_LA06_AE33_248N_B15 | AE33 | MSIOD248NB15 |
| C12 | GND | | |
| C13 | GND | | |
| C14 | LPC_LA10_AE30_250P_B15 | AE30 | MSIOD250PB15 |
| C15 | LPC_LA10_AD30_250N_B15 | AD30 | MSIOD250NB15 |
| C16 | GND | | |
| C17 | GND | | |
| C18 | LPC_LA14_W23_227P_B16 | W23 | MSIOD227PB16 |
| C19 | LPC_LA14_W24_227N_B16 | W24 | MSIOD227NB16 |
| C20 | GND | | |
| C21 | GND | | |
| C22 | LPC_LA18_CC_AA32_228P_B16 | AA32 | MSIOD228PB16 |
| C23 | LPC_LA18_CC_Y32_228N_B16 | Y32 | MSIOD228NB16 |
| C24 | GND | | |
| C25 | GND | | |
| C26 | LPC_LA27_V29_223P_B16 | V29 | MSIOD223PB16 |
| C27 | LPC_LA27_V28_223N_B16 | V28 | MSIOD223NB16 |
| C28 | GND | | |
| C29 | GND | | |
| C30 | I2C1_SCL | T8 | MSIO45NB4/I2C_1_SCL/GPIO_1_A/USB_DATA4_A |
| C31 | I2C1_SDA | T9 | MSIO45PB4/I2C_1_SDA/GPIO_0_A/USB_DATA3_A |

***Table 14 •*** **FMC LPC Connector (J60) Pinout *(continued)***

| | | | |
|---|---|---|---|
| C32 | GND | | |
| C33 | GND | | |
| C34 | GND | | |
| C35 | 12P0V | | |
| C36 | GND | | |
| C37 | 12P0V | | |
| C38 | GND | | |
| C39 | 3P3V | | |
| C40 | GND | | |
| D1 | LPC_PGC2M_N12_71P_B3 | N12 | MSIO71PB3/MMUART_1_RTS/GPIO_11_B |
| D2 | GND | | |
| D3 | GND | | |
| D4 | FMC_LPC_SERDES3_REFCLK0_P | AJ10 | MSIOD279PB9/SERDES_3_REFCLK0_P |
| D5 | FMC_LPC_SERDES3_REFCLK0_N | AK10 | MSIOD279NB9/SERDES_3_REFCLK0_N |
| D6 | GND | | |
| D7 | GND | | |
| D8 | LPC_LA01_CC_W34_219P_B16 | W34 | MSIOD219PB16/CCC_SW1_CLKI0 |
| D9 | LPC_LA01_CC_V34_219N_B16 | V34 | MSIOD219NB16 |
| D10 | GND | | |
| D11 | LPC_LA05_W29_226P_B16 | W29 | MSIOD226PB16 |
| D12 | LPC_LA05_W30_226N_B16 | W30 | MSIOD226NB16 |
| D13 | GND | | |
| D14 | LPC_LA09_Y28_231P_B16 | Y28 | MSIOD231PB16 |
| D15 | LPC_LA09_W28_231N_B16 | W28 | MSIOD231NB16 |
| D16 | GND | | |
| D17 | LPC_LA13_AC24_258P_B15 | AC24 | MSIOD258PB15 |
| D18 | LPC_LA13_AC23_258N_B15 | AC23 | MSIOD258NB15 |
| D19 | GND | | |
| D20 | LPC_LA17_CC_V23_220P_B16 | V23 | MSIOD220PB16/CCC_SW0_CLKI0 |
| D21 | LPC_LA17_CC_V24_220N_B16 | V24 | MSIOD220NB16 |
| D22 | GND | | |
| D23 | LPC_LA23_AG32_252P_B15 | AG32 | MSIOD252PB15 |
| D24 | LPC_LA23_AF32_252N_B15 | AF32 | MSIOD252NB15 |
| D25 | GND | | |
| D26 | LPC_LA26_V27_222P_B16 | V27 | MSIOD222PB16 |
| D27 | LPC_LA26_V26_222N_B16 | V26 | MSIOD222NB16 |
| D28 | GND | | |

***Table 14 •*** **FMC LPC Connector (J60) Pinout *(continued)***

| | | | |
|---|---|---|---|
| D29 | LPC_TCK | | |
| D30 | LPC_TDI | | |
| D31 | LPC_TDO | | |
| D32 | 3P3V | | |
| D33 | LPC_TMS | | |
| D34 | LPC_TRST_L | | |
| D35 | GND | | |
| D36 | 3P3V | | |
| D37 | GND | | |
| D38 | 3P3V | | |
| D39 | GND | | |
| D40 | 3P3V | | |
| G1 | GND | | |
| G2 | LPC_CLK1_M2C_U34_217P_B16 | U34 | MSIOD217PB16/GB5/CCC_SW1_CLKI1 |
| G3 | LPC_CLK1_M2C_T34_217N_B16 | T34 | MSIOD217NB16 |
| G4 | GND | | |
| G5 | GND | | |
| G6 | LPC_LA00_CC_Y33_224P_B16 | Y33 | MSIOD224PB16 |
| G7 | LPC_LA00_CC_W33_224N_B16 | W33 | MSIOD224NB16 |
| G8 | GND | | |
| G9 | LPC_LA03_AC34_232P_B16 | AC34 | MSIOD232PB16 |
| G10 | LPC_LA03_AB34_232N_B16 | AB34 | MSIOD232NB16 |
| G11 | GND | | |
| G12 | LPC_LA08_AC32_233P_B16 | AC32 | MSIOD233PB16 |
| G13 | LPC_LA08_AC33_233N_B16 | AC33 | MSIOD233NB16 |
| G14 | GND | | |
| G15 | LPC_LA12_W26_229P_B16 | W26 | MSIOD229PB16 |
| G16 | LPC_LA12_W25_229N_B16 | W25 | MSIOD229NB16 |
| G17 | GND | | |
| G18 | LPC_LA16_Y23_234P_B16 | Y23 | MSIOD234PB16 |
| G19 | LPC_LA16_Y24_234N_B16 | Y24 | MSIOD234NB16 |
| G20 | GND | | |
| G21 | LPC_LA20_AF27_257P_B15 | AF27 | MSIOD257PB15 |
| G22 | LPC_LA20_AE27_257N_B15 | AE27 | MSIOD257NB15 |
| G23 | GND | | |
| G24 | LPC_LA22_AG34_244P_B15 | AG34 | MSIOD244PB15 |
| G25 | LPC_LA22_AF34_244N_B15 | AF34 | MSIOD244NB15 |
| G26 | GND | | |

***Table 14 •*** **FMC LPC Connector (J60) Pinout *(continued)***

| | | | |
|---|---|---|---|
| G27 | LPC_LA25_AH33_255P_B15 | AH33 | MSIOD255PB15 |
| G28 | LPC_LA25_AH34_255N_B15 | AH34 | MSIOD255NB15 |
| G29 | GND | | |
| G30 | LPC_LA29_AC27_245P_B15 | AC27 | MSIOD245PB15 |
| G31 | LPC_LA29_AB27_245N_B15 | AB27 | MSIOD245NB15 |
| G32 | GND | | |
| G33 | LPC_LA31_AB24_251P_B15 | AB24 | MSIOD251PB15 |
| G34 | LPC_LA31_AB23_251N_B15 | AB23 | MSIOD251NB15 |
| G35 | GND | | |
| G36 | LPC_LA33_AD24_261P_B15 | AD24 | MSIOD261PB15 |
| G37 | LPC_LA33_AD25_261N_B15 | AD25 | MSIOD261NB15 |
| G38 | GND | | |
| G39 | VCCIO_LPC_VADJ | | |
| G40 | GND | | |
| H1 | N36478604 | | |
| H2 | LPC_PRSNTM2CL_N11_71N_B3 | N11 | MSIO71NB3/MMUART_1_DTR/GPIO_12_B |
| H3 | GND | | |
| H4 | LPC_CLK0_M2C_V32_218P_B16 | V32 | MSIOD218PB16/GB1/CCC_SW0_CLKI1 |
| H5 | LPC_CLK0_M2C_V33_218N_B16 | V33 | MSIOD218NB16 |
| H6 | GND | | |
| H7 | LPC_LA02_AA33_225P_B16 | AA33 | MSIOD225PB16 |
| H8 | LPC_LA02_AA34_225N_B16 | AA34 | MSIOD225NB16 |
| H9 | GND | | |
| H10 | LPC_LA04_AD33_239P_B16 | AD33 | MSIOD239PB16 |
| H11 | LPC_LA04_AD34_239N_B16 | AD34 | MSIOD239NB16 |
| H12 | GND | | |
| H13 | LPC_LA07_AE31_247P_B15 | AE31 | MSIOD247PB15 |
| H14 | LPC_LA07_AE32_247N_B15 | AE32 | MSIOD247NB15 |
| H15 | GND | | |
| H16 | LPC_LA11_AF30_254P_B15 | AF30 | MSIOD254PB15 |
| H17 | LPC_LA11_AG31_254N_B15 | AG31 | MSIOD254NB15 |
| H18 | GND | | |
| H19 | LPC_LA15_AF28_256P_B15 | AF28 | MSIOD256PB15 |
| H20 | LPC_LA15_AE28_256N_B15 | AE28 | MSIOD256NB15 |
| H21 | GND | | |
| H22 | LPC_LA19_AG30_260P_B15 | AG30 | MSIOD260PB15 |
| H23 | LPC_LA19_AF29_260N_B15 | AF29 | MSIOD260NB15 |
| H24 | GND | | |

***Table 14 •*** **FMC LPC Connector (J60) Pinout *(continued)***

| | | | |
|---|---|---|---|
| H25 | LPC_LA21_W31_221P_B16 | W31 | MSIOD221PB16 |
| H26 | LPC_LA21_V31_221N_B16 | V31 | MSIOD221NB16 |
| H27 | GND | | |
| H28 | LPC_LA24_AD28_249P_B15 | AD28 | MSIOD249PB15 |
| H29 | LPC_LA24_AD29_249N_B15 | AD29 | MSIOD249NB15 |
| H30 | GND | | |
| H31 | LPC_LA28_AB25_246P_B15 | AB25 | MSIOD246PB15 |
| H32 | LPC_LA28_AB26_246N_B15 | AB26 | MSIOD246NB15 |
| H33 | GND | | |
| H34 | LPC_LA30_AC25_253P_B15 | AC25 | MSIOD253PB15 |
| H35 | LPC_LA30_AC26_253N_B15 | AC26 | MSIOD253NB15 |
| H36 | GND | | |
| H37 | LPC_LA32_AE26_259P_B15 | AE26 | MSIOD259PB15 |
| H38 | LPC_LA32_AD26_259N_B15 | AD26 | MSIOD259NB15 |
| H39 | GND | | |
| H40 | VCCIO_LPC_VADJ | | |

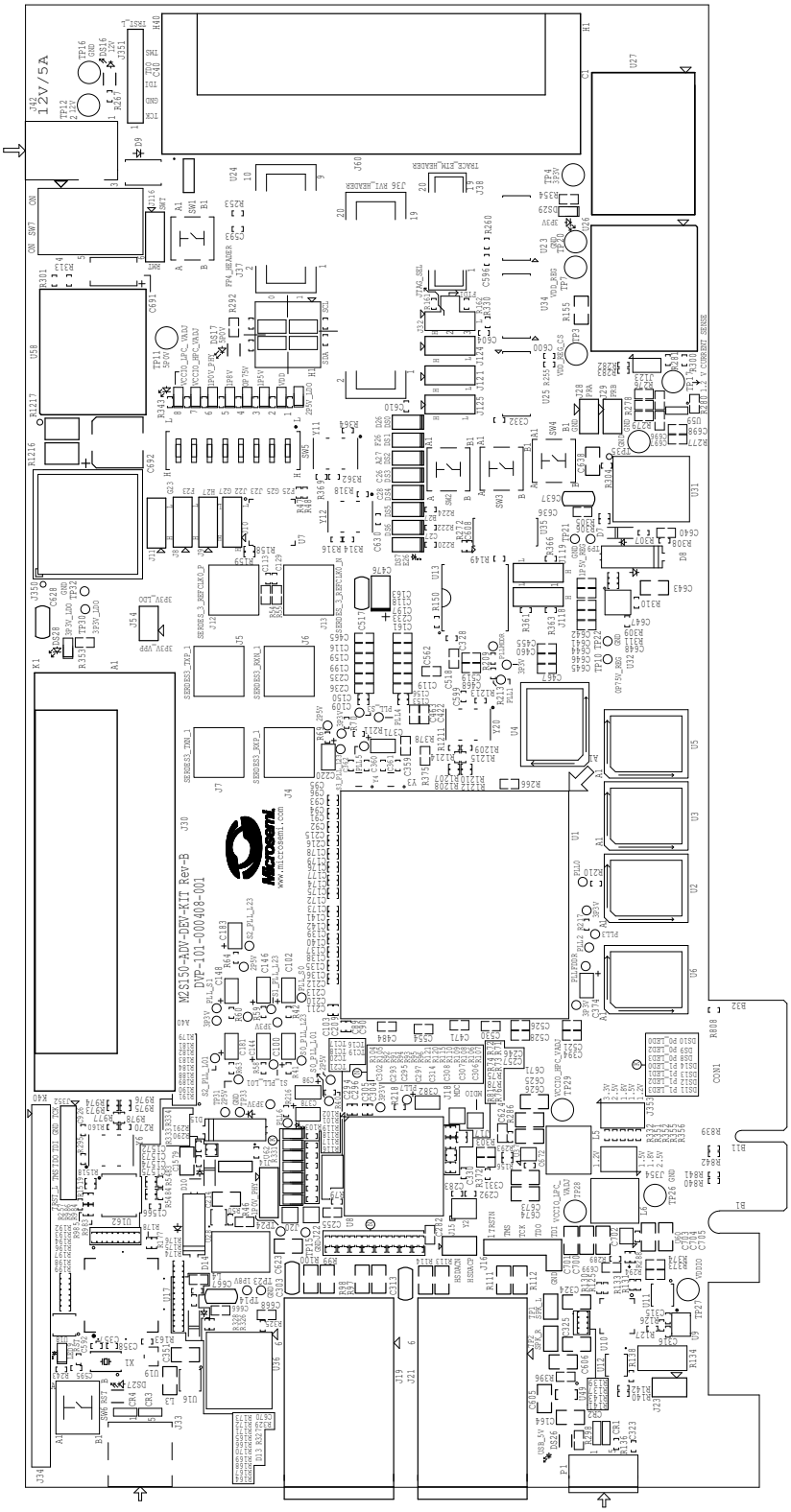
# 5 Pin List

The SmartFusion2 Advanced Development Kit uses an M2S150TS-1FCG1152 device. For a list of all package pins in this device, see *SmartFusion2 FC1152 Pinouts*.

# 6 Board Components Placement

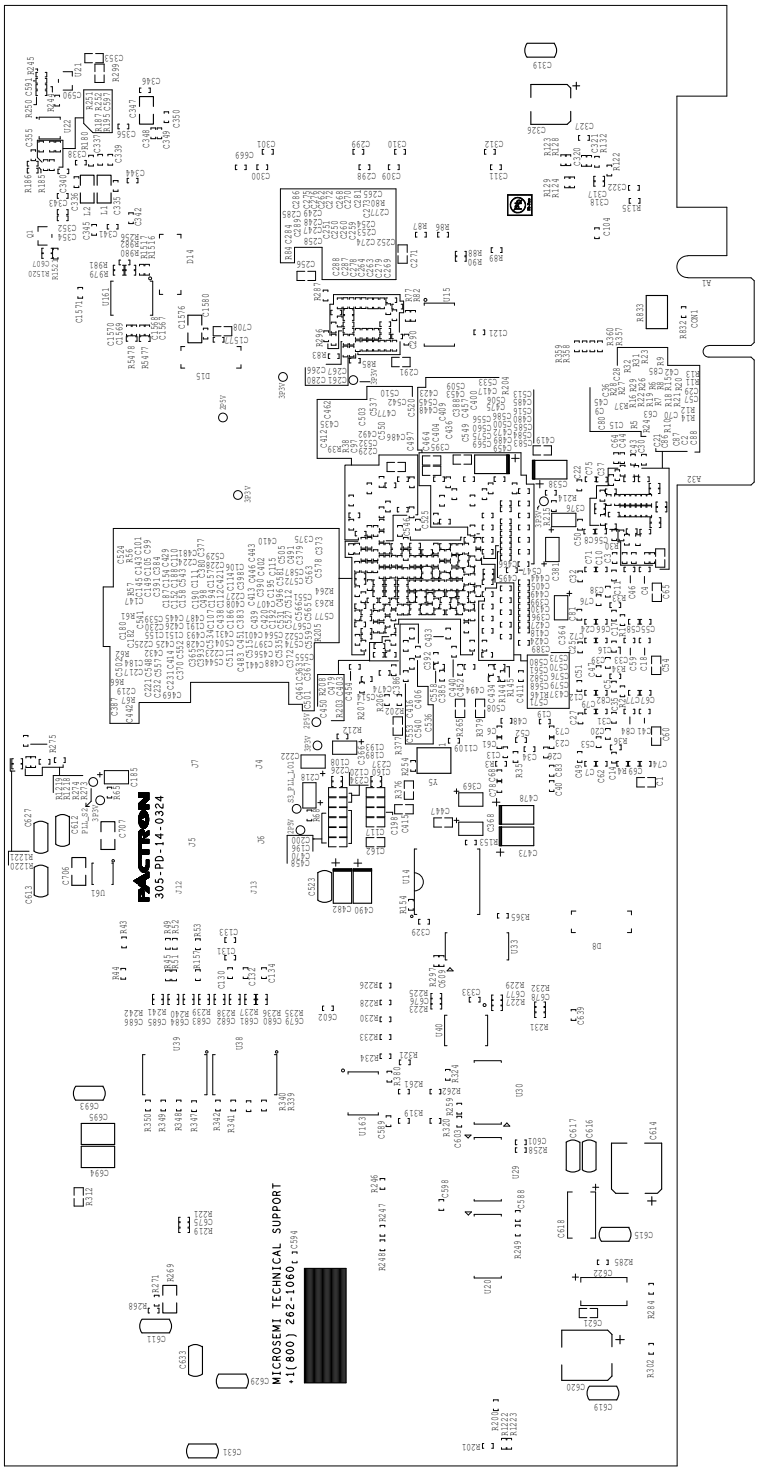
The following figure shows the placement of various components on the SmartFusion2 Advanced Development Kit silkscreen.

***Figure 20 •*** **Silkscreen Top View**



The following figure shows the bottom view of the SmartFusion2 Advanced Development Kit silkscreen.

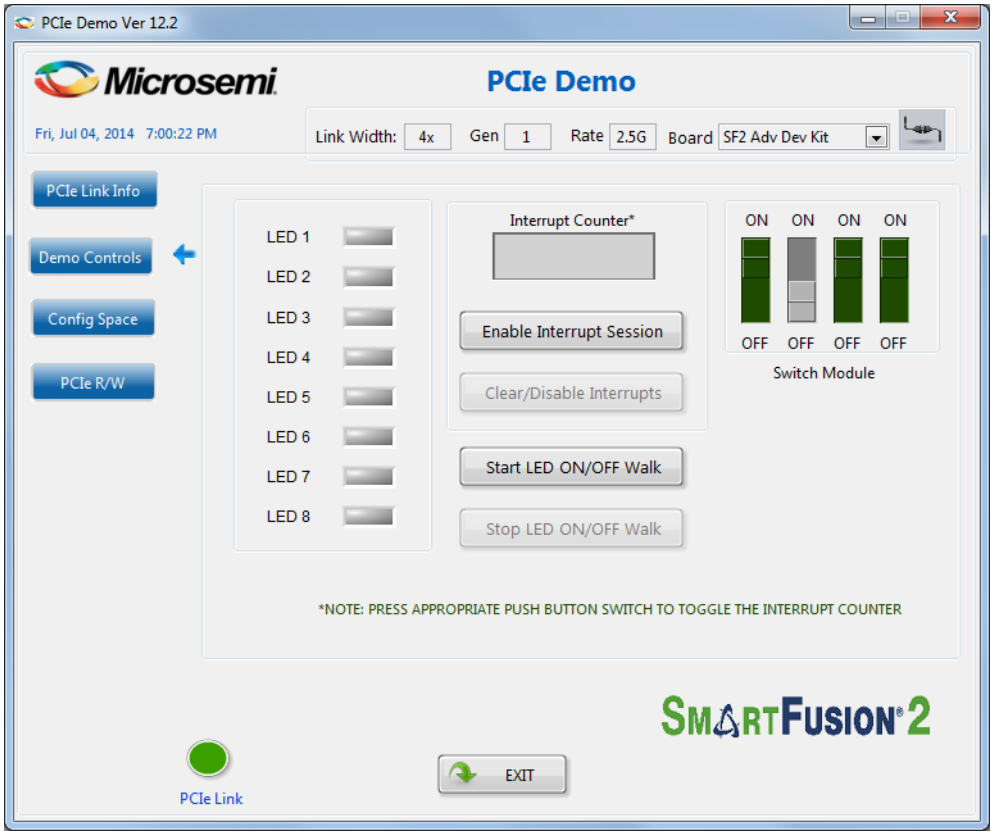
***Figure 21 •*** **Silkscreen Bottom View**



# 7 Demo Design

The SmartFusion2 M2S150-ADV-DEV-KIT comes with a preloaded PCIe control plane design. to demonstrate the PCIe interface of the SmartFusion2 device. The following figure shows the PCIe demo design window.

***Figure 22 •*** **PCIe Demo Design Window**




For more information about running the demo design, see *SmartFusion2 SoC FPGA PCIe Control Plane Demo Guide for Advanced Development Kit*.

# 8 Manufacturing Test

The M2S150-ADV-DEV-KIT device contains a manufacturing test program that can be run to verify the functionality of the board. This program contains a list of options that can be run as diagnostics. After Tera Term is set up and the board is powered up, various tests that can be performed on the board are displayed (see Figure 29, page 51). One or more tests can then be selected from the list of available tests.

Before testing the SmartFusion2 Advanced Development Board:

- Download `SEC_KIT_MTD_top.stp` file from *http://www.microsemi.com/document-portal/doc_download/134344-smartfusion2-advanced-development-kit-mtd*.
- Download and install the FTD drivers from *http://www.ftdichip.com/Drivers/D2XX.htm*.

## 8.1 Programming M2S150-ADV-DEV-KIT

This section provides information about validating the power supply and programming the M2S150-ADV-DEV-KIT for the manufacturing test.

### 8.1.1 Validating Power Supply

To test and validate the power supply to the board:

1. Connect the following jumpers on the SmartFusion2 Advanced Development Board.
   - Short the **J116** jumper to position 1-2.
   - Short the **J123** jumper to position 2-3.
   - Short the **J353** jumper to position 1-2.
   - Short the **J354** jumper to position 1-2.
   - Short the **J54** jumper to position 1-2.

**Note:** Before making the jumper connections, switch OFF the **SW7** power supply switch.

2. Connect the 12 V/5 A power supply brick to the **J42** jumper.
3. Switch ON the **SW7** power supply switch.

### 8.1.2 Programming the FPGA Using Embedded FlashPro5

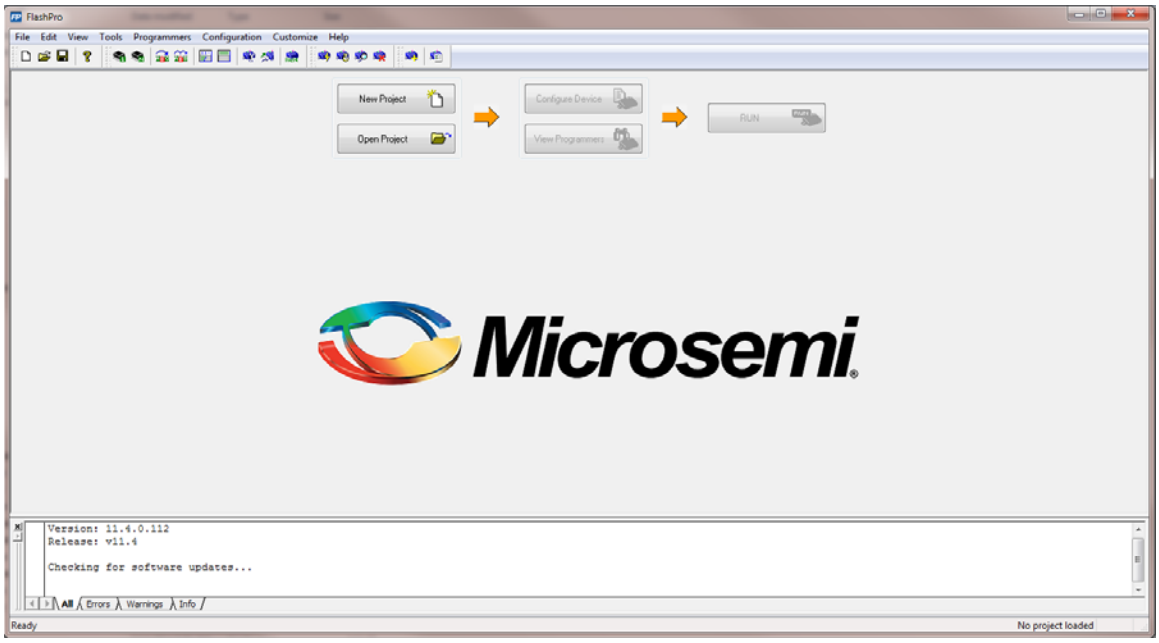
The M2S150-ADV-DEV-KIT has an embedded FlashPro5 programmer; therefore, an external programmer is not required to program the SmartFusion2 device. The device can be programmed using the embedded FlashPro5, provided the FlashPro software is installed on the host PC.

**Note:** The board can also be programmed using FlashPro4. To program the board using FlashPro4, connect the FlashPro4 header to the **J37** connector, and change the position of the **J124** jumper to pin 2-3.

To program the device using embedded FlashPro5:

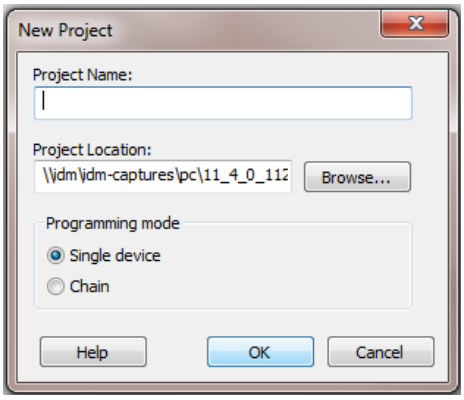
1. Connect the following jumpers on the SmartFusion2 Advanced Development Board:
   - Short the **J124** jumper to position 1-2.
   - Short the **J121** jumper to position 1-2.
   - Short the **J32** jumper to position 1-2.
2. Connect one end of the mini USB to Type A USB cable to the **J33** jumper, and other end to the USB port of the host PC.
3. Launch the FlashPro v11.4 software.

***Figure 23 •*** **FlashPro Window**



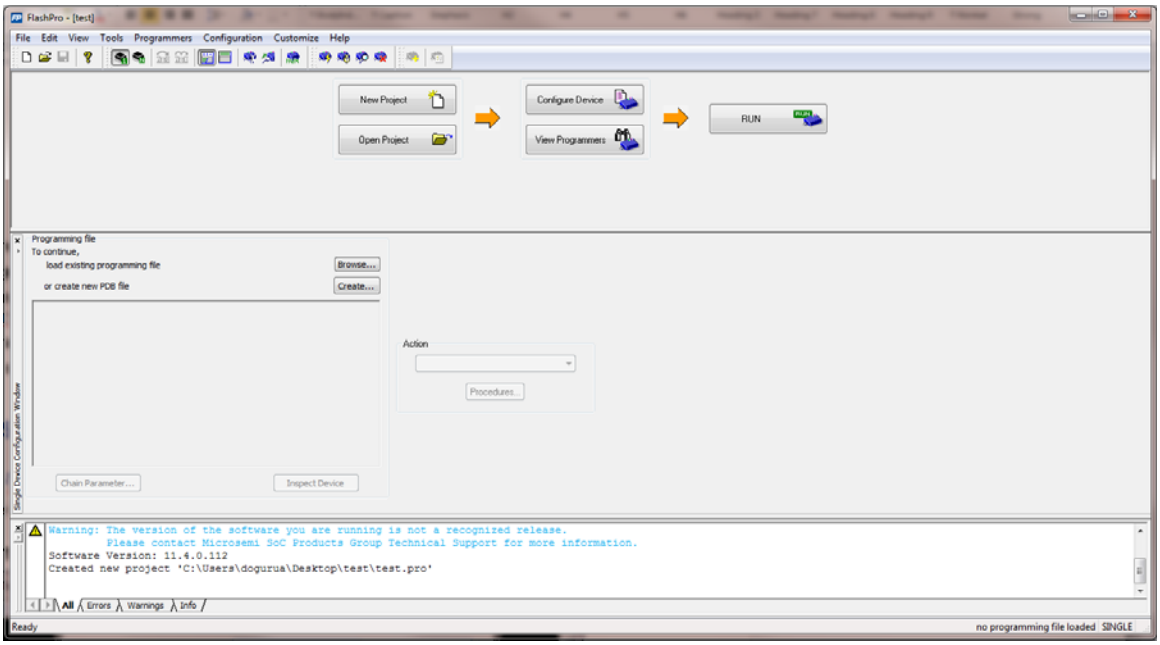

4. Click **New Project** to create a new project.
5. In the **New Project** window, do the following, and click **OK**.
   - Enter a project name.
   - Select **Single device** as the programming mode.

***Figure 24 •*** **New Project Window**




6. Click **Configure Device**.

***Figure 25 •*** **Configuring the Device**




7. Click **Browse,** and select the `SEC_KIT_MTD_top.stp` file from the **Load Programming File** window.
8. Click **Program** to program the device.
9. Press the **SW4** switch.
   The corresponding DS7 LED starts glowing, indicating that the device is programmed successfully.

## 8.2 Running the Manufacturing Test

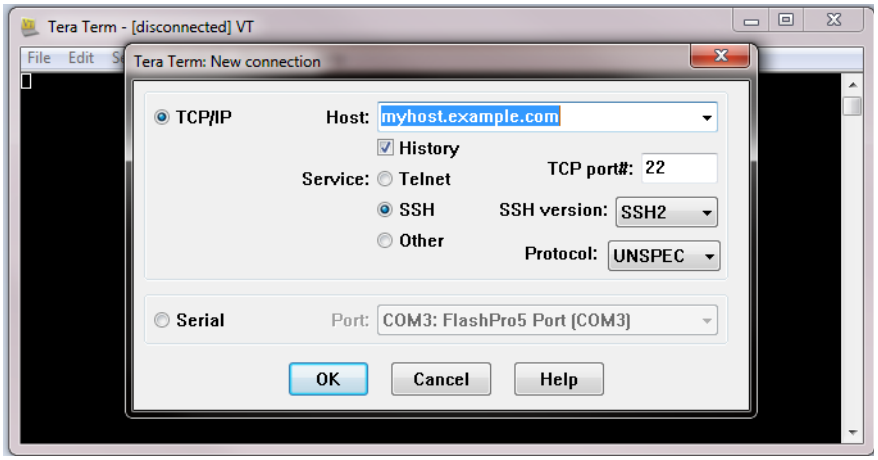
This section describes how to run the manufacturing test for the SmartFusion2 Advanced Development Board.

### 8.2.1 Setting Up Tera Term

To set up Tera Term for the manufacturing test:

1. Connect one end of the mini USB to Type A USB cable to **J33,** and other end to the USB port of the host PC.
2. Launch **Tera Term** from the Start menu.

***Figure 26 •*** **Tera Term New Connection Window**

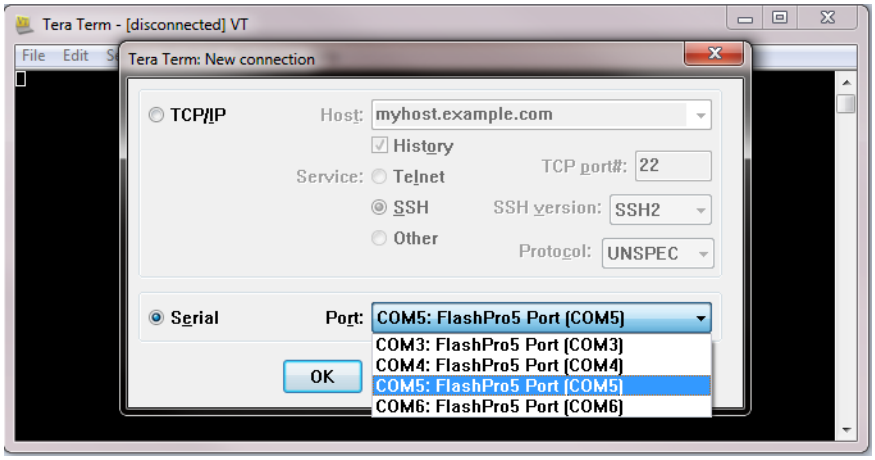



3. Select the **Serial** radio button.
4. Select a port from the **Port** drop-down list, and click **OK**.

**Notes:**

- When using a USB cable for Tera Term communication, four FlashPro5 COM ports are available in the **Port** drop-down list, as shown in the following figure. Select the third FlashPro5 COM port to establish the connection with the host PC.
- If FlashPro5 drivers are not installed properly, the drop-down list does not list FlashPro5 COM ports.

***Figure 27 •*** **Tera Term New Connection Window**




5. On the **Tera Term Serial port setup** window, select the COM port to establish connection with the host PC, and enter the following Tera Term settings.
   - Baud rate = 57600
   - Data = 8 bit
   - Parity = none
   - Stop = 1 bit
   - Flow control = none

***Figure 28 •*** **Tera Term Serial Port Setup Window**


6. Click **OK**.

## 8.2.2 Setting Up Jumpers

The following table specifies the jumper settings required to perform various tests on the SmartFusion2 Advanced Development Board.

***Table 15 •*** **Jumper Settings for Manufacturing Test**

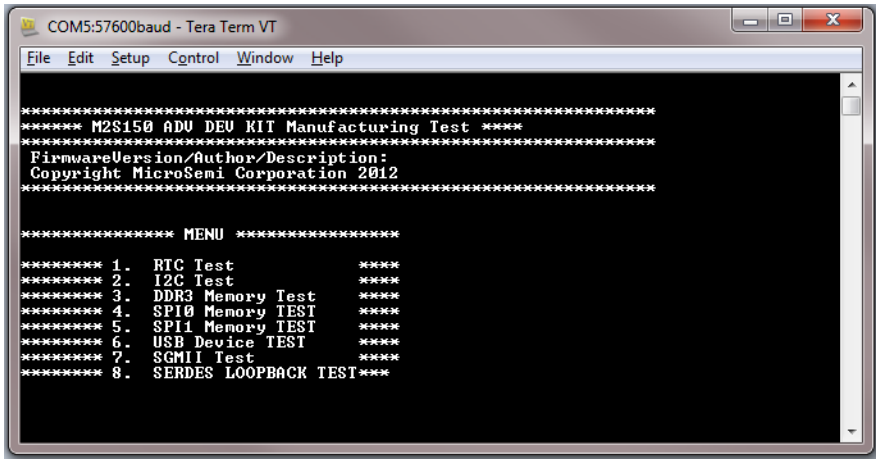
| Interface | Jumper Settings |
|---|---|
| RTC test | |
| I2C test | On header (H1), short 10-6 and 11-7. |
| DDR3 memory test | |
| SPI0 memory test | Short J118 pin 1-2. |
| SPI1 memory test | Short J119 pin 1-2. |
| USB device test | Connect Micro B to P1, and connect the other end of the cable to the host PC (type A). This cable is required for testing on board USB device interface. |
| | Short J23 pin 1-2. |
| SGMII test | Connect an Ethernet cable to J19, and connect other end of the cable to the 1 Gbps Ethernet switch or network. |
| | Short J11 pin 1-2. |
| | Short J8 pin 1-2. |
| | Short J14 pin 1-2. |
| SerDes loopback test | Connect J4 to J5 and J6 to J7 using an SMA-to-SMA cable. |
| | Loopback cable (5 Gbps data rate). |
| | Short J11 pin 1-2. |
| | Short J8 pin 1-2. |

### 8.2.3 Running the Test

After the device is programmed and the jumper settings are applied, follow these steps to run the manufacturing test.

1. Press the **SW6** reset switch on the M2S150-ADV-DEV-KIT board to reset the board and begin the tests.
   When the setup is completed, all tests are listed in the HyperTerminal window, as shown in the following figure.

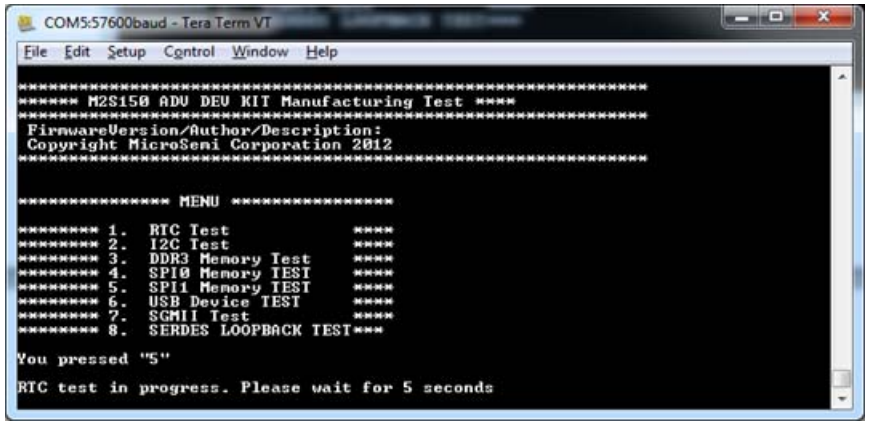
***Figure 29 •*** **Test Menu**




If the list of tests does not appear, press the **SW6** reset switch again. If the list still does not appear, then check all the jumpers and Tera Term settings.

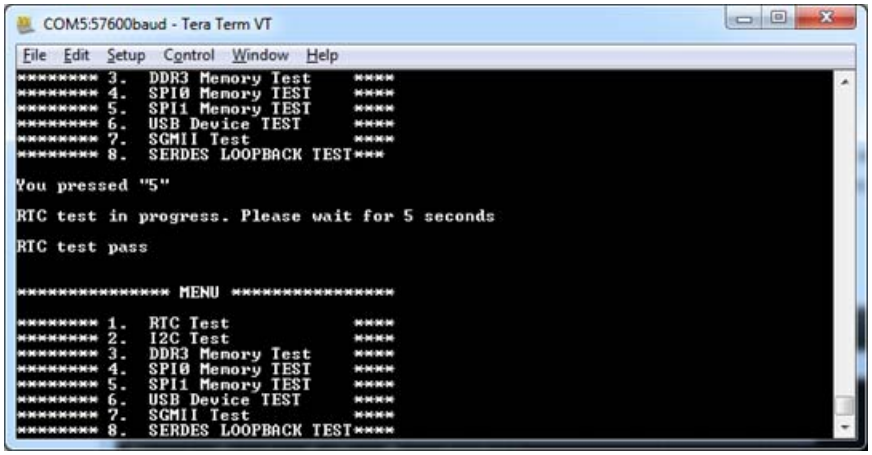
2. Press **1** to run the RTC test.
   The following message appears.

***Figure 30 •*** **Running RTC Test**



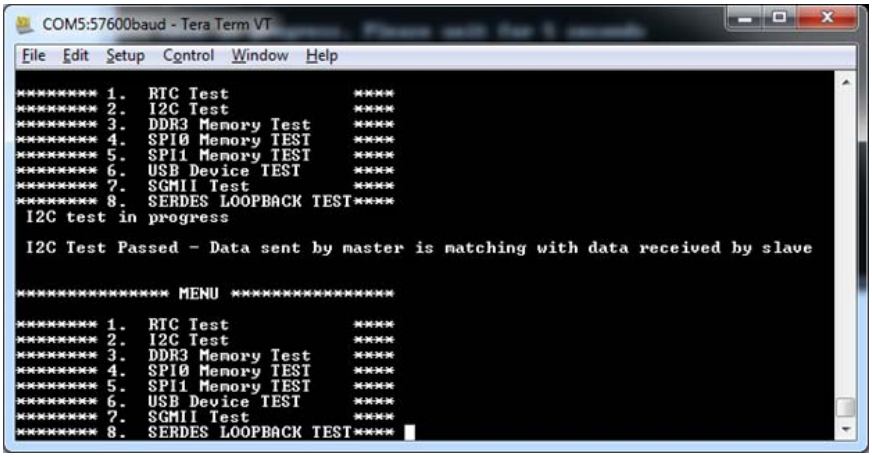
When the test is passed, the following message appears.

***Figure 31 •*** **RTC Test Passed**



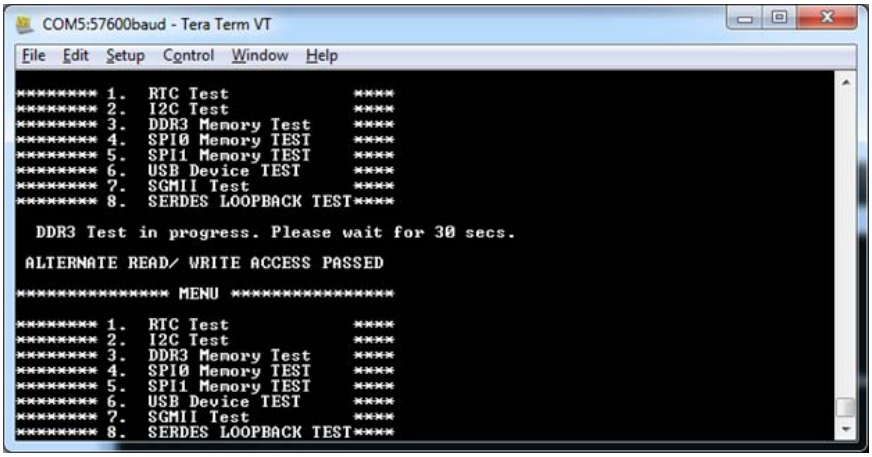

3. Press **2** to run the I2C loopback test. Wait for five seconds for the test to be run. When the test is passed, the following message appears.

***Figure 32 •*** **I2C Test Passed**



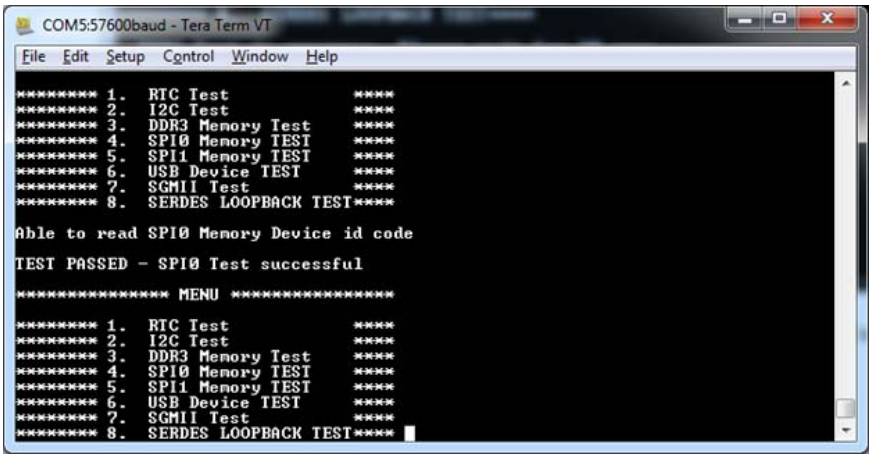

4. Press **3** to run the DDR3 memory test. Wait for 30 seconds for the test to be run. When the test is passed, the following message appears.

***Figure 33 •*** **DDR3 Memory Test Passed**



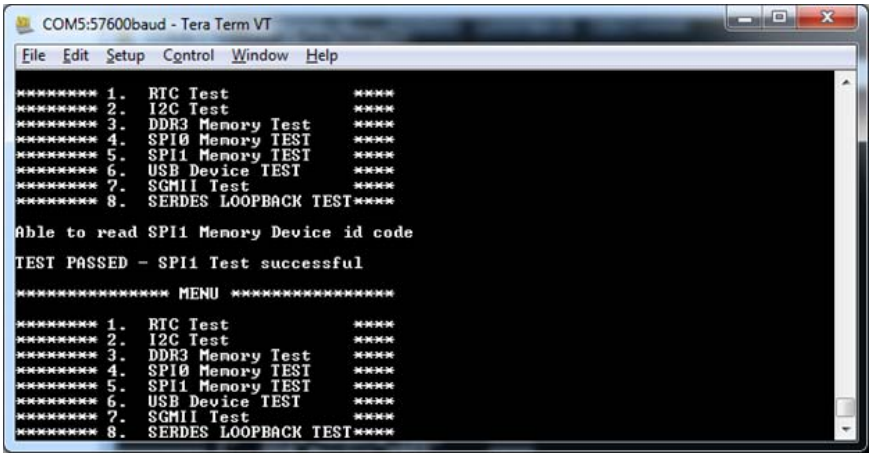
5. Press **4** to run the SPI0 memory test.
   When the test is passed, the following message appears.

***Figure 34 •*** **SPI0 Memory Test Passed**



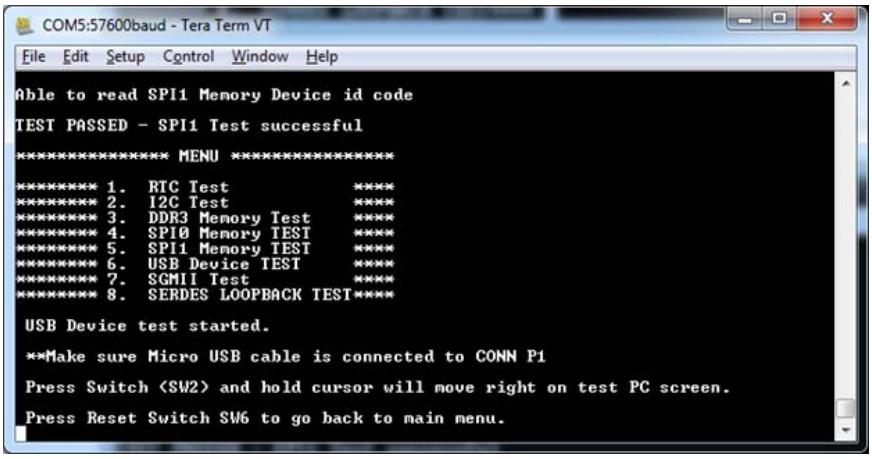

6. Press **5** to run the SPI1 memory test.
   When the test is passed, the following message is appears.

***Figure 35 •*** **SPI1 Memory Test Passed**



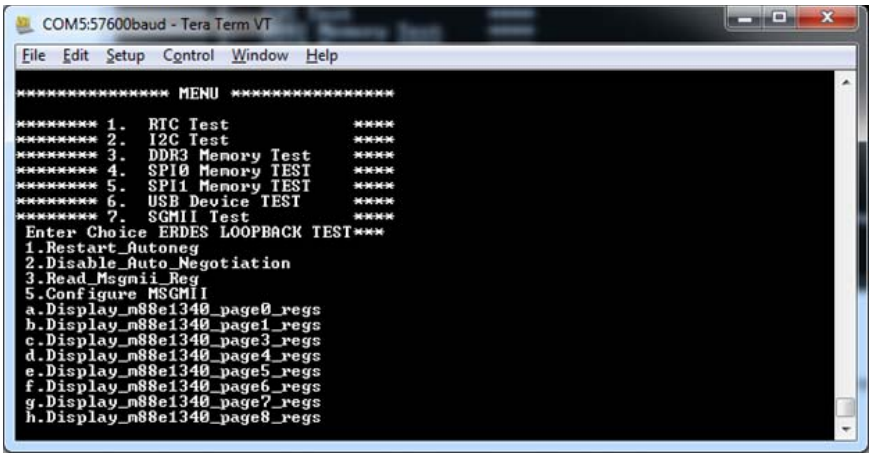

7. Press **6** to run the USB device test.
   When the test begins, the following message appears.

***Figure 36 •*** **USB Device Test Passed**



8. Press and hold the **SW2** switch on the board, and observe the mouse cursor moving to the right side.
9. Press **SW6** reset switch go back to the main menu.
10. Press **7** to run the SGMII test.
    When the test begins, the DS1 LED is OFF. The DS10 LED starts glowing, and the DS8 LED starts blinking. The following message appears.

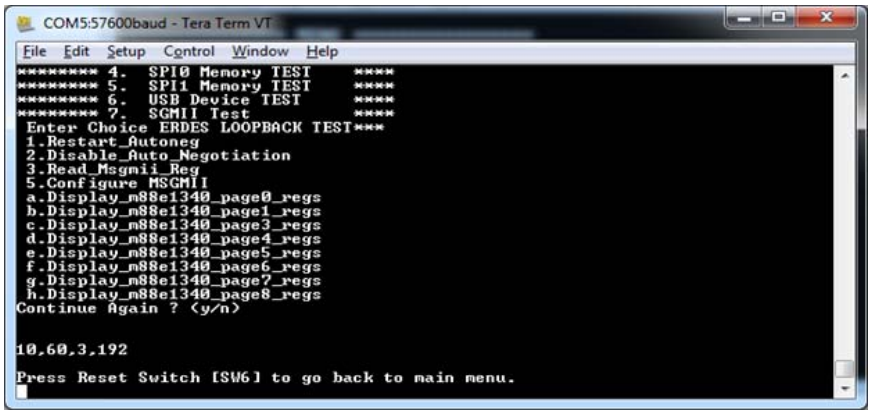
***Figure 37 •*** **SGMII Test**




**Note:** If this message is not displayed, or if DS10 and DS8 LEDs do not blink, switch ON and OFF the **SW7** power supply switch on the board, and run the DDR3 test by pressing 3.

11. Press **7** to repeat the SGMII test.
    A confirmation message is displayed,
12. Press **n** twice.
    When the test is passed, the IP address of the host PC is displayed, as shown in the following figure.

***Figure 38 •*** **SGMII Test Passed**

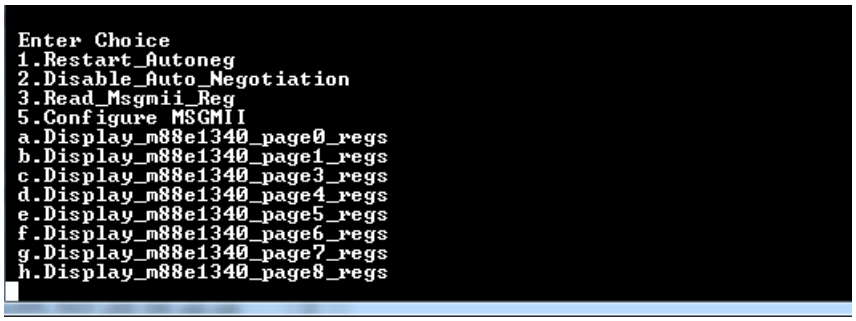



**Note:** IP address may vary from one PC to the other PC.

13. Press the **SW6** reset switch on the board to go back to the main menu.

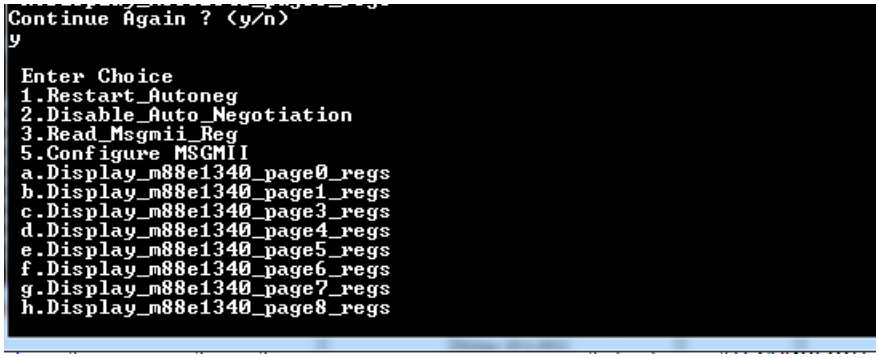
14. If the IP address is not displayed, perform the following steps to get the IP address.
    i. Press **7** to run the SGMII test.

***Figure 39 •*** **SGMII Debug Test**



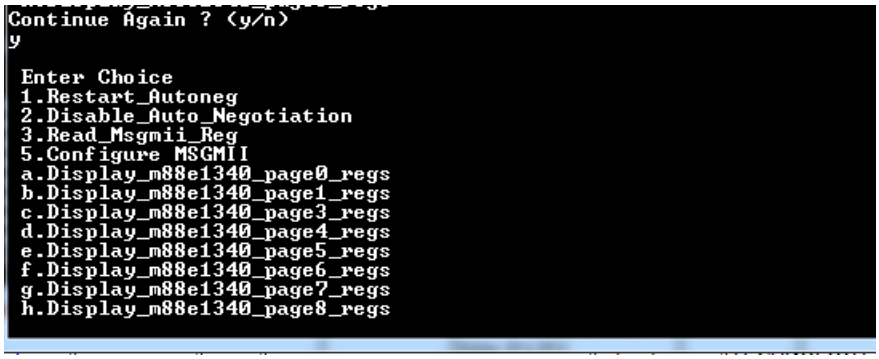

    ii. Press **1** to restart auto-negotiation, and press **y** to continue.

***Figure 40 •*** **SGMII Debug Test**



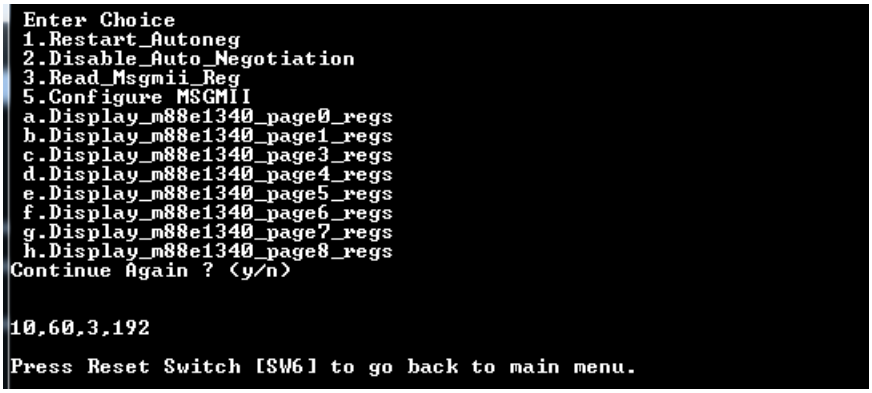

    iii. Press **2** to disable auto-negotiation, and press **y** to continue.

***Figure 41 •*** **SGMII Debug Test**



iv. Press **n** twice to not repeat the action and to get the IP address, as shown in the following figure.

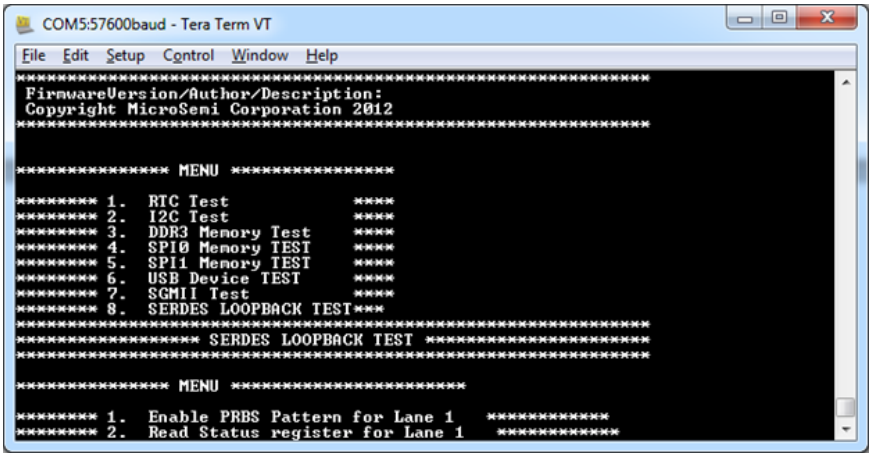
***Figure 42 •*** **SGMII Debug Test Passed**




15. Press **SW6** to go back to the main menu.
16. Press **8** to run the SerDes loopback test.

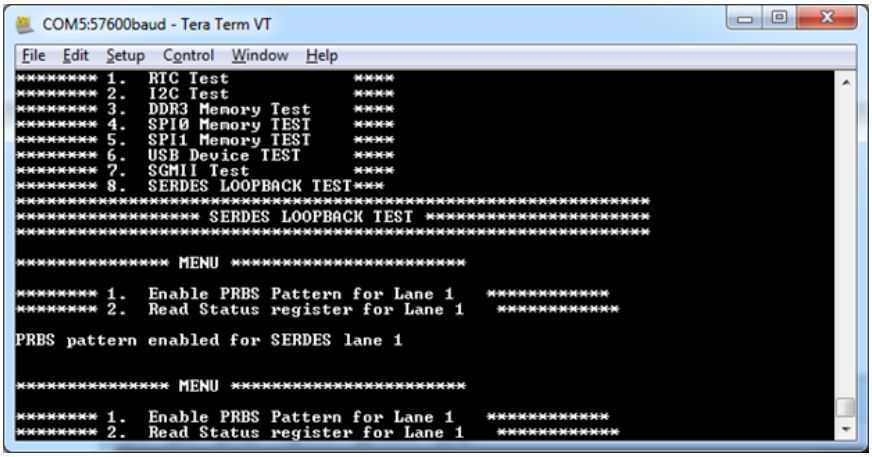
**Note:** Ensure that the loopback cable is connected. (See Setting Up Jumpers, page 50.)

***Figure 43 •*** **SerDes Loopback Test**



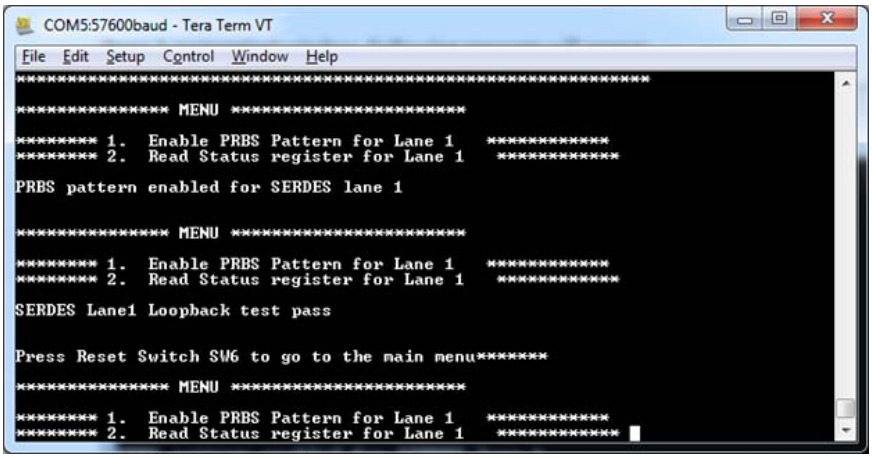

17. Press 1 to enable PRBS pattern for Lane 1.

***Figure 44 •*** **SerDes Loopback Test - Enabling PRBS Pattern for Lane 1**



18. Press **2** to read the status register for Lane 1.
    When the test is passed, the following message appears.

***Figure 45 •*** **SerDes Loopback Passed**




19. Press the **SW6** reset switch to go back to the main menu.