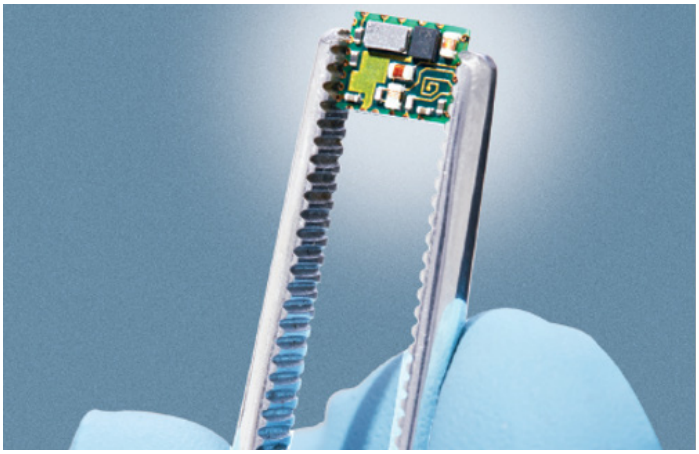
Miniaturization: Embedded SiP Technology

Advanced Packaging Services

Summary

Our embedded System-In-Package (SiP) technology provides unparalleled miniaturization in a proven and robust package capable of meeting the most stringent quality requirements.



Website: https://www.microchip.com/en-us/products/services/advanced-packaging

Email: Info-Caldicot@microchip.com

We have developed a technology for embedding components between PCB laminations that enables them to occupy a near-zero area. This allows you to reduce the size of your device or maintain its size while delivering additional functionality.

Our embedded die technology offers quality, reliability and security, enabling practical implementations of SiPs that offer a real-estate savings of up to 70% versus the original PCB area.

Capabilities

- Compatible components can be embedded
  - Flip chip, wire bond, packaged part, passives
- 3D die stacking
- Low tooling cost
- Inbuilt RF screening
- Internal interconnect
- Custom package design
- MIL-standard for implantable devices compatible

What Can We Offer You?

Markets

Our embedded SiP technology is used in, but is not limited to, these markets:

- Medical
- Security
- Military
- Industrial sensing

Customer benefits

- Significant size reduction
- Increased security against counterfeiting
- Reduced signal path loss
- Robustness against vibration
- High reliability
- Adaptable package to meet your board requirements
- Low cost of entry
- Fast turnaround time
- Flexible size and shape; any package size available
- Scalable manufacturing process
- Component traceability and planning

Module Parameters	
Minimum Substrate Thickness	450 µm Core (assumes 4 copper layers and minimum 75 µm die thickness)
Minimum Feature Size	75 µm
Minimum Module XY Size	Die XY Dimensions +1.4 mm
Encapsulation	Yes
Traceability	Yes
Embedded Components	Yes
Smd Components on Top Layer	Yes
Packaging	JEDEC Tray or Tape and Reel
Footprint	Land Grid Array (LGA)

Test Group	Test Standard	Result
Moisture Sensitivity Preconditioning:	JESD22-A113F, IPC/JEDEC J-STD-020 Level 2a	
Temperature Cycling	−40°C to +60°C, 5 cycles	✓
Bake	125°C for 24 hours	
Moisture Soak	120 hours, 60°C/60% RH	
3× Reflow	JESD22-A113F	
Thermal stress:		
Low Temperature Storage	−40°C, 72h	✓
High Temperature Storage	125°C, 72h	
Temperature Cycling	MIL-STD-883 Method 1010, Condition B, −55°C to +125°C, 20 cycles	
Mechanical stress:		
Mechanical Shock	MIL-STD-883 Method 2002, Condition B, 5 shocks, 1500g	✓
Mechanical Vibration	MIL-STD-883 Method 2007, Condition A, 20–2000 Hz, 20G	
Constant Acceleration	MIL-STD-883 Method 2001, 10,000G	
Steady state life testing:		
Low and High Temperature Testing	0°C, 55°C	✓
HTOL	125°C, 1000 hours	
Exposure:		
Resistance to solvents	MIL-STD-883 Method 2016	✓
ESD	MIL-883 Method 3015, 1000V HBM	
Assembly:		
Component shear	MIL-STD-883 Method 2019/2011	✓
External Physical Dimensions	MIL-883 Method 2016	
Solderability	MIL-STD-883 Method 2003.8/2022.2	
Ionic cleanliness	IPC-TM-650	