AC406

Application Note
Configuring IGLOO2 and SmartFusion2 Devices for Safety-Critical Applications

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 7.0

The following changes are made in revision 7.0 of this document:

- Information about Device Identification and Programming Considerations, page 27 was added.
- Information about Isolating unused MSS/HPMS/FDDR/SerDes Blocks, page 16 was added.
- Information about lock-bits file was updated. See How to Set System Registers Write-Protection Bits, page 11.
- Information about Protecting MSS/HPMS Configuration in SmartFusion2/IGLOO2 Devices, page 5 was updated.
- Information in Figure 1, page 3 and Figure 2, page 4 was updated.
- Appendix: Configuration of Unused IP Blocks, page 37 was added.

1.2 Revision 6.0

The following changes are made in revision 6.0 of this document:

- Title of the section, MSS Configurator to Set System Registers Write-Protection Bits is changed to How to Set System Registers Write-Protection Bits, page 11
- Added content on how to write-protect system registers using Configure Register Lock Bits option available in the Libero design flow. For more information, see How to Set System Registers Write-Protection Bits, page 11

1.3 Revision 5.0

Updated a note in revision 5.0 of this document. For more information, see Isolating MSS/HPMS/FDDR/SERDESIF BlocksProtecting the SERDES, MDDR and FDDR Configuration, page 15.

1.4 Revision 4.0

Updated a note and added a note in revision 4.0 of this document. For more information, see Isolating MSS/HPMS/FDDR/SERDESIF BlocksProtecting the SERDES, MDDR and FDDR Configuration, page 15.

1.5 Revision 3.0

Updated the document for Libero SoC v11.5 software release changes in revision 3.0 of this document.

1.6 Revision 2.0

Updated the document for Libero SoC v11.4 software release changes in revision 2.0 of this document.

1.7 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Overview

This application note explains the SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA features that require customer action for implementing safety-critical designs.

2.1 Introduction

Designers intending to deploy integrated circuits in safety-critical applications need to understand the effects of atmospheric radiation.The single event upset (SEU) phenomenon was first discovered in 1979 by Intel and Bell Labs as failures in dynamic random-access memory (DRAMs). SEU is attributed to stray alpha particles or neutrons changing the contents of storage elements such as registers and memory cells. In aviation applications, the operational altitudes have a higher neutron flux. However, the SEU phenomenon has increasingly become a concern at sea level as well. The continuous drive to smaller node processes reduces the charge at each base cell. Therefore, the likelihood of SEU errors at sea level has increased. These SEU errors are of concern to designers of safety-critical systems.

The next generation Microsemi SmartFusion2 SoC FPGAs and IGLOO2 FPGAs are the only devices that address fundamental requirements for advanced security, high reliability and low power in safety-critical industrial, military, aviation, communications, and medical applications.

2.2 References

Following are the references used in this document:

- *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*
- *UG0451: IGLOO2 and SmartFusion2 Programming User Guide*
- *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*
- *AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note*
- *Single Event Effects*

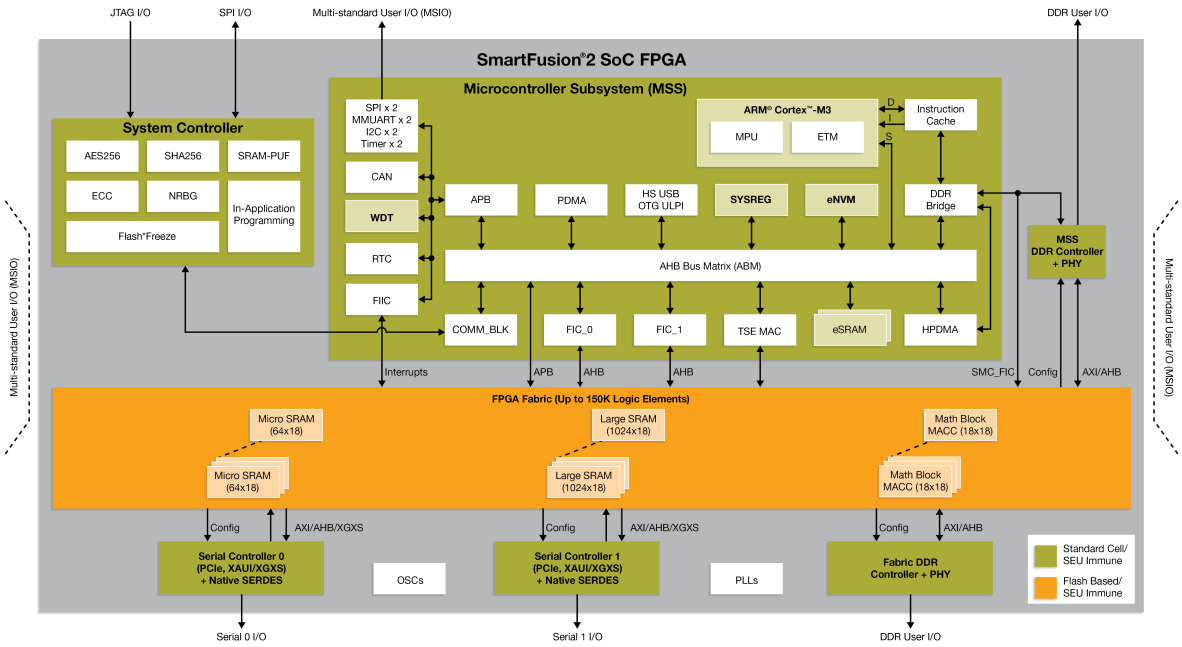
3 Configuring SmartFusion2 and IGLOO2 Devices for Safety-Critical Applications

SmartFusion2 and IGLOO2 devices integrate various hard IP blocks and FPGA fabric on a single die. The key elements of these devices include microcontroller subsystem (MSS) in case of SmartFusion2 devices or high performance memory subsystem (HPMS) in case of IGLOO2 devices, FPGA fabric, double data rate (DDR) memory controllers, and high-speed transceiver lanes. SmartFusion2 and IGLOO2 devices do not require an external configuration device, reducing the component count and improving reliability.

The following figure shows the architectural block diagram of SmartFusion2 devices. The green blocks are hardwired standard cell ASIC parts on the die. These blocks are immunize from SEU's aside from the soft status/control registers within the block. There is no SEU sensitive configuration logic behind those parts.

The orange block is the FPGA fabric. The FPGA fabric configuration is built on a flash-based SEU immune technology. Internal device Interconnects to the standard cell blocks through FPGA routing resources. Standard cell block inputs tied inactive (high or low) via the FPGA fabric are SEU immune and can keep those interface inactive when resources are unused.

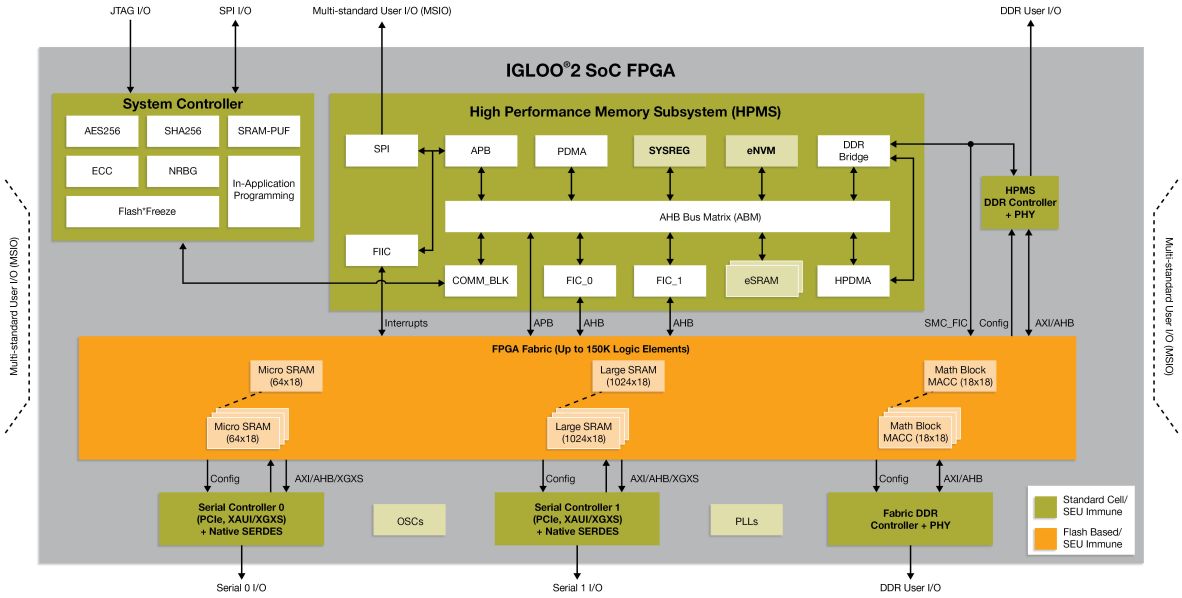
Figure 1 • **SmartFusion2 Architectural Block Diagram**



The following image shows the architectural block diagram of IGLOO2 devices. The green blocks are hardwired standard cell ASIC parts on the die. These blocks are immunize from SEU's aside from the soft status/control registers within the block. There is no SEU sensitive configuration logic behind those parts.

The orange block is the FPGA fabric. The FPGA fabric configuration is built on a flash-based SEU immune technology. Internal device Interconnects to the standard cell blocks through FPGA routing resources. Standard cell block inputs tied inactive (high or low) via the FPGA fabric are SEU immune and can keep those interface inactive when resources are unused.

Figure 2 • **IGLOO2 Architectural Block Diagram**



The SmartFusion2 and IGLOO2 device families address critical high-reliability requirements with the following features:

- SEU immune FPGA fabric configuration
- SEU immune hard IP blocks (MSS/HPMS/FDDR, and SERDESIFs) configuration
- SEU immune I/O configuration
- SEU protected memories
- Hard 667 Mbps DDR2/3 controllers with single error correction and double error detection (SECDED) protection

SmartFusion2 and IGLOO2 devices have dedicated flash cells to configure the FPGA fabric, hard IP blocks, and IOMUXes. These flash cells are programmed at the time of device programming and cannot be changed during run-time.The bits programmed into these flash cells are referred to as flash bits throughout the remainder of the document. These flash bits are proven to be SEU immune with zero failure in time (FIT) rate due to the high voltage charge level required to reprogram the flash cell. A common Flash cell technology is utilized in both the FPGA fabric and MSS/HPMS/DDR/SerDes configuration bits. Consequently, there radiation sensitivity is the same. For more information about SEU, see *Single Event Effects* web page.

SmartFusion2/IGLOO2 devices include a variety of built-in functionality that can be enabled or disabled to provide the functions required for an application. Designers implementing safety-critical designs using SmartFusion2 SoC /IGLOO2 FPGAs have the option of disabling certain built-in features or let Libero SoC software configure any unused resource (configuration can be verified via unused resources configuration report) if these features are not required in the design.

SmartFusion2 and IGLOO2 devices support write-protection, activated through “lock” bits, for MSS/HPMS configuration registers, FDDR configuration registers, SERDESIF configuration registers, and MSS IOMUX configuration registers. The write-protection feature enables immunity against SEUs and unintentional writes to the configuration registers.

This application note describes the methodology used to isolate critical functions in SmartFusion2 SoC FPGAs and IGLOO2 FPGAs for design assurance purposes in the safety-critical applications.

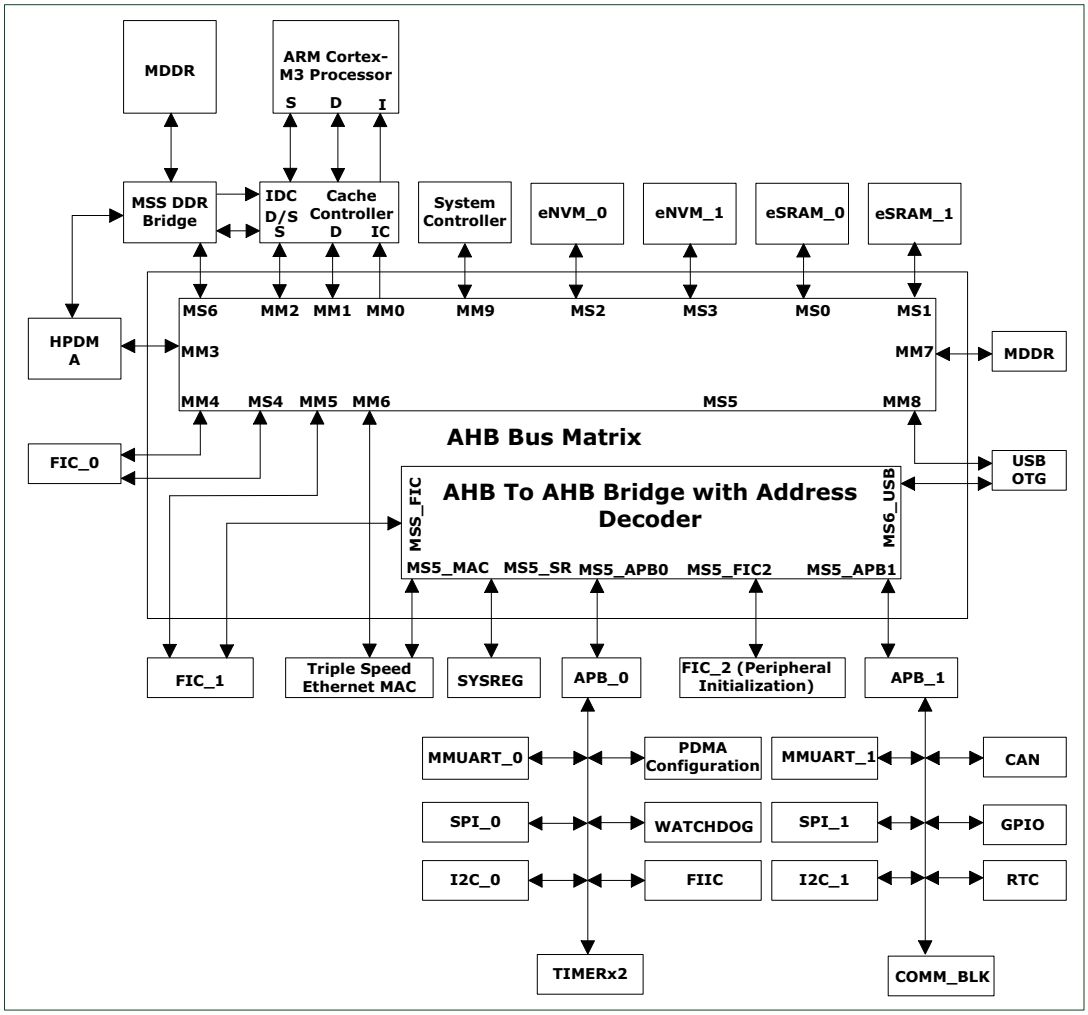
Note: All unused user I/Os are tri-stated with internal weak pull-up resistors.

3.1 Protecting MSS/HPMS Configuration in SmartFusion2/IGLOO2 Devices

SmartFusion2 devices integrate a MSS ASIC block. The MSS consists of multiple hard IP blocks such as, ARM Cortex-M3 processor subsystem, embedded memories, direct memory access (DMA) engines, communication peripherals, timers, and DDR memory controller. See *UG0331: SmartFusion2 Microcontroller Subsystem User Guide* for more information.

The following figure shows the SmartFusion2 MSS block diagram:

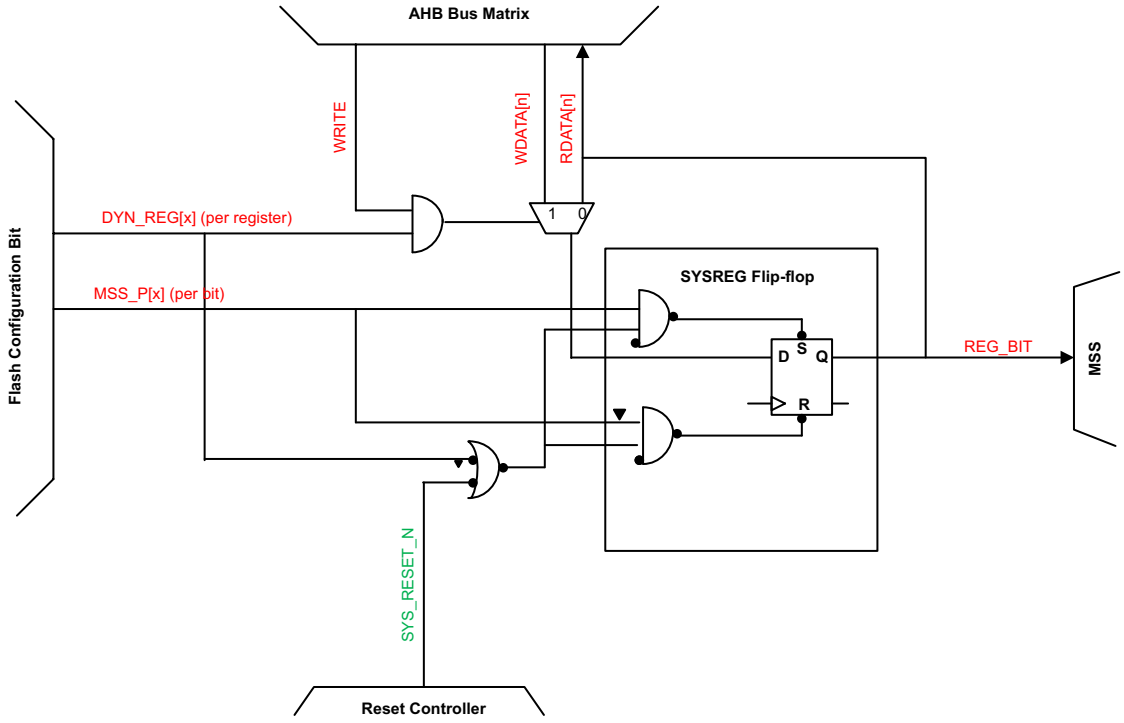
Figure 3 • **SmartFusion2 MSS Block Diagram**



The state of the MSS sub-blocks is controlled by system registers (SYSREG). System registers are initialized by the user-configurable flash bits at power-up. After initialization, the system registers' content can be protected from SEUs or unintended run-time writes by enabling the write-protection feature associated with system registers. The write-protection feature of system registers is set by user-configurable flash bits. Write protection can be assigned to all bits in a register, to a specific field in a register, or to each specific bit in a register.

The following figure shows the system register schematic.

Figure 4 • **System Register Schematic**



If a write-protection flash bit (DYN_REG[x]) is set, then the associated SYSREG flip-flop is held in continuous reset or preset depending upon its initialization flash bit value (MSS_P[x]). Therefore, even if there is an SEU hit on the SYSREG flip-flop, the SYSREG flip-flop immediately goes back to the initialized flash bit value. See How to Set System Registers Write-Protection Bits, page 11 for more information.

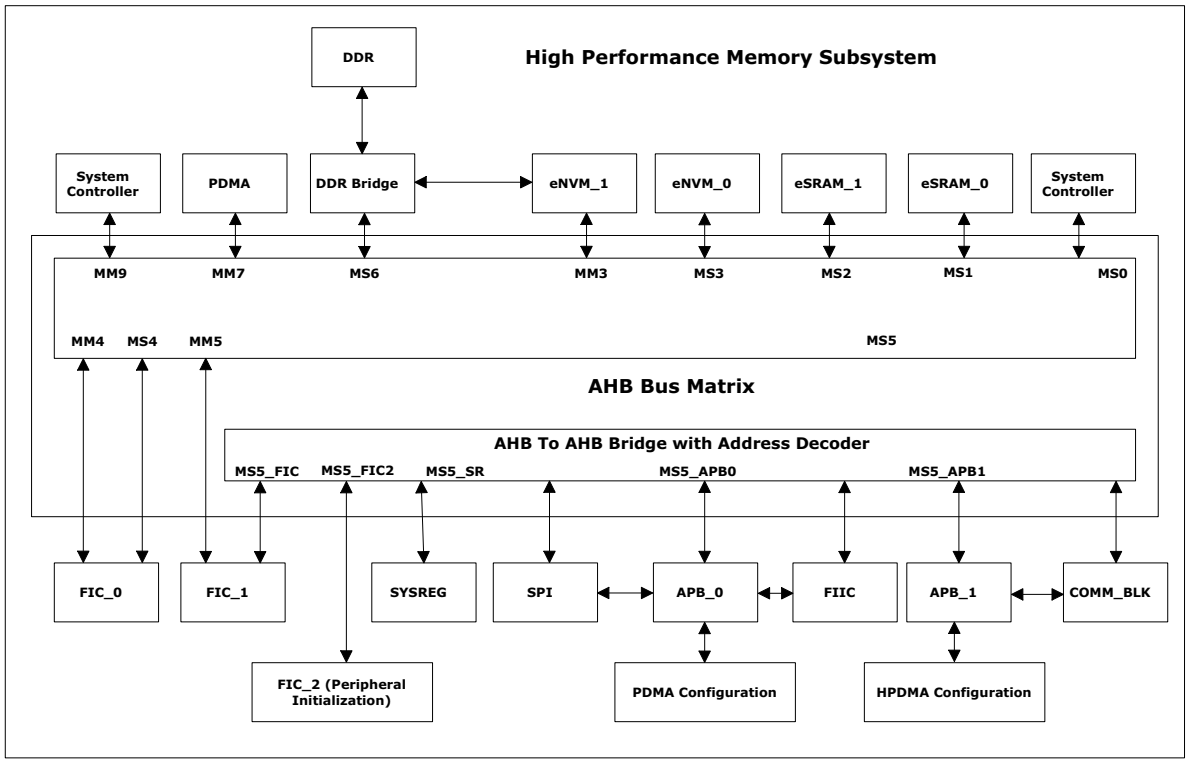
The system registers content can be read back at run-time (using the Cortex-M3 processor or fabric logic) to ensure that system registers are initialized properly and they have not changed over time. It is required to enable at least one of the fabric interface controllers (FIC) to read the SYSREG content from the FPGA fabric.

See the Fabric Interface Controller chapter of *UG0331: SmartFusion2 Microcontroller Subsystem User Guide* for more information on how to interface a fabric master to MSS to read the SYSREG address space.

IGLOO2 devices integrate a hardened HPMS. The HPMS consists of multiple hard IP blocks such as embedded memories, direct memory access (DMA) engines, communication peripherals, and DDR memory controller. See *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide* for more information.

The following figure shows the IGLOO2 HPMS block diagram.

Figure 5 • **IGLOO2 HPMS Block Diagram**



The state of the HPMS sub-blocks is controlled by system registers (SYSREG). System registers are initialized by the user-configurable flash bits at power-up. After initialization, the system registers' content can be protected from SEUs or unintended run-time writes by enabling the write-protection feature associated with system registers. The write-protection feature of system registers is set by user-configurable flash bits. Write protection can be assigned to all bits in a register, to a specific field in a register, or to each specific bit in a register. See How to Set System Registers Write-Protection Bits, page 11 for more information. In IGLOO2, the system registers content can be read back at run-time, using fabric logic to ensure that system registers are initialized properly and they have not changed over time. It is required to enable at least one of the fabric interface controllers (FIC) to read the SYSREG content from the FPGA fabric.

See the Fabric Interface Controller chapter of *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide* for more information about how to interface a fabric master to HPMS to read the SYSREG address space.

3.1.1 Using SmartFusion2 MSS Configurator to Disable Unused MSS Features

If the MSS is used in a system design, it is still possible to disable the various sub-blocks that are not used. The MSS sub-blocks can be held in reset from power-up by configuring the flash bits associated with the following system registers — SOFT_RESET_CR, CC_CR, and WDOG_CR. It is also required to enable the write protection to protect the configuration from SEUs or unintended writes.

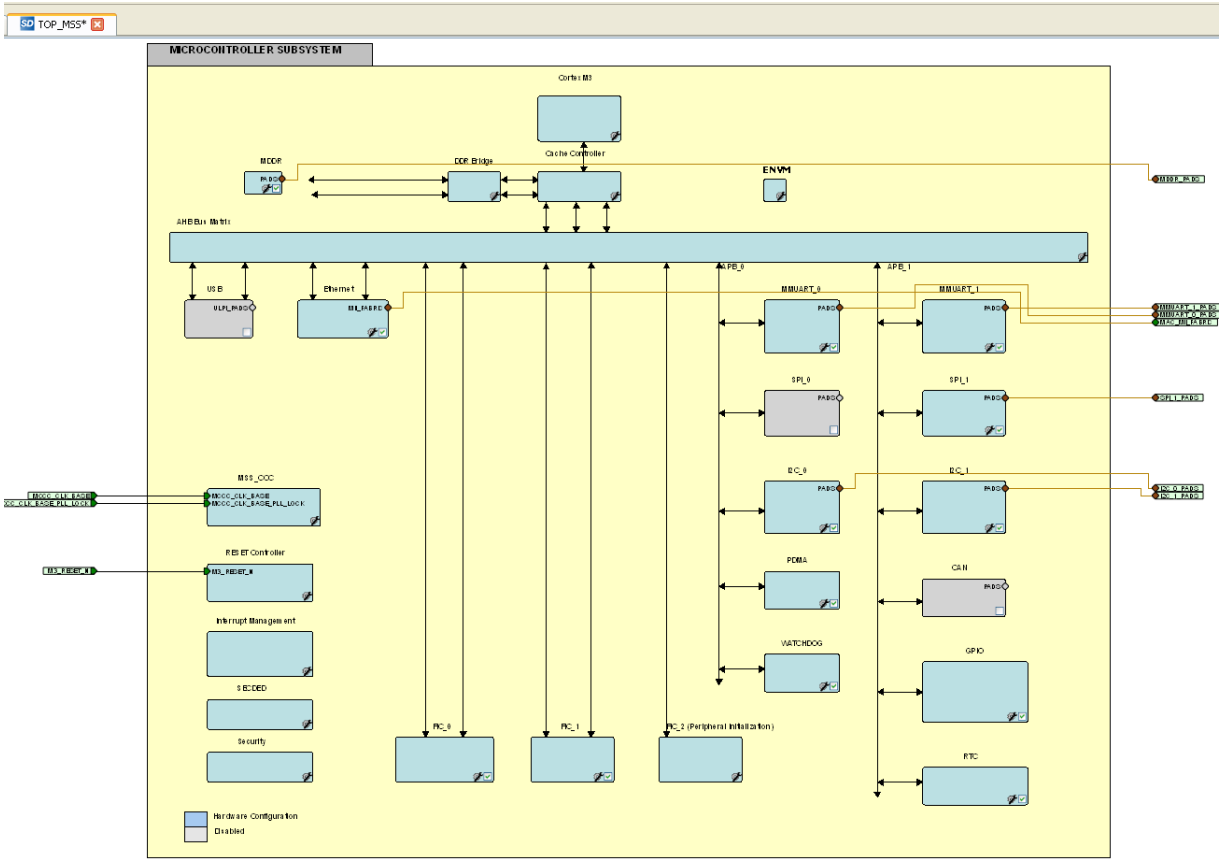
There are a full set of MSS system registers that can be optionally write protected. The SOFT_RESET_CR, CC_CR, and WDOG_CR registers should be considered as a minimum to write-lock. See Appendix: System Register Description, page 29 for bit definitions of SOFT_RESET_CR, CC_CR, and WDOG_CR registers. The user should understand the use and need of any register bit under consideration to lock. See *UG0331: SmartFusion2 Microcontroller Subsystem User* Guide for

information about the full set of system control registers. All registers listed as RW-P have write protection capability.

The SmartFusion2 MSS Configurator allows enabling or disabling and configuring of each MSS sub-block according to the user's application requirements.

The following figure shows the SmartFusion2 MSS Configurator window:

Figure 6 • **SmartFusion2 MSS Configurator**



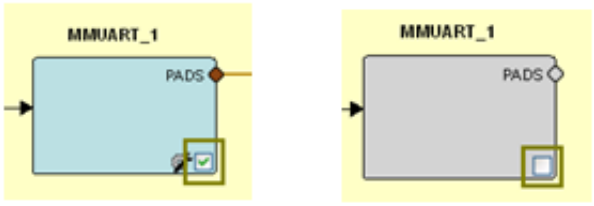
The SmartFusion2 MSS Configurator allows enabling or disabling of the following sub-blocks

- Cache Controller
- MDDR Controller
- USB Controller
- Ethernet MAC
- MMUART_0 and MMUART_1
- SPI_0 and SPI_1
- I2C_0 and I2C_1
- PDMA
- CAN
- Watchdog Timer
- GPIO
- FIC_0 and FIC_1

The following figure shows how to disable the MSS sub-blocks by selecting the check box provided in the lower-right corner of the sub-blocks. At the time of device programming, Libero SoC software programs the SOFT_RESET_CR system register with the appropriate values based on the enable or disable configuration in the MSS Configurator.

The following figure shows how to disable unused MSS sub-blocks:

Figure 7 • **Disabling Unused MSS Sub blocks**



Disabling a sub-block causes it to be held in reset when the device is powered up. While most of the MSS sub-block states can be configured through MSS configurator, the following blocks are not provided in MSS configurator to select their state:

- HPDMA
- Timers
- COMM_BLK
- DMA
- Embedded memories (eNVM_0, eNVM_1, eSRAM_0, eSRAM_1)

The DMA, high-performance DMA (HPDMA), and Timers are not in reset by default. However, these IP blocks require further configuration to be active. The COMM_BLK and embedded memories are active from power-up to support System Controller functions including device certificate read and SmartDebug support.

Note: There is no flash bit to disable the real time clock (RTC). Microsemi recommends masking the RTC wakeup interrupt to the Cortex-M3 processor and FPGA fabric by un-checking the RTC sub-block in the MSS configurator. RTC wakeup interrupt masking is done through flash bits, and can be protected from SEUs by enabling write protection to the RTC_WAKEUP_CR system register.

3.1.2 Using IGLOO2 MSS Configurator to Disable Unused HPMS Features

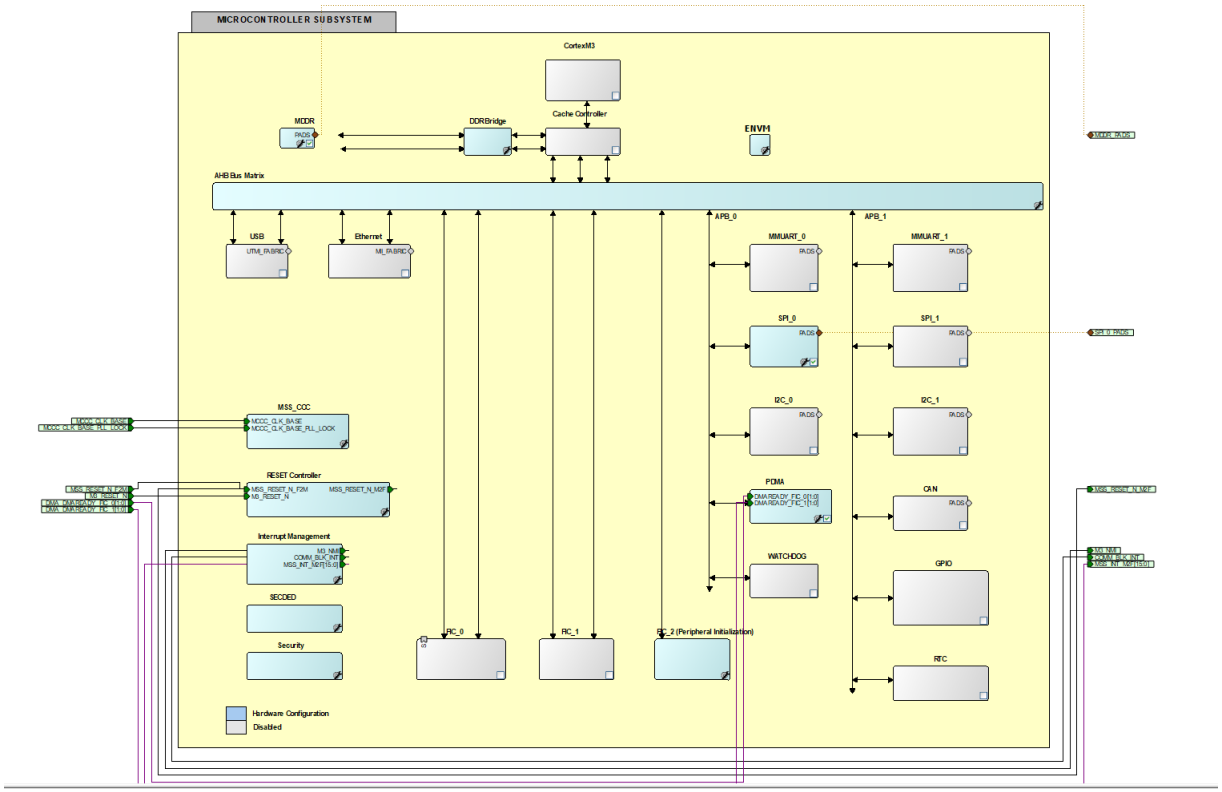
If the HPMS is used in a system design, it is still possible to disable the various sub-blocks that are not used. The HPMS sub-blocks can be held in reset from power-up by configuring the flash bits associated with the HPMS SOFT_RESET_CR. It is also required to enable the write protection to protect the configuration from SEUs or unintended writes.

There are a full set of HPMS system registers that can be optionally write protected. The SOFT_RESET_CR register should be considered as a minimum to write-lock. See Appendix: System Register Description, page 29, for bit definitions of HPMS SOFT_RESET_CR register. The user should understand the use and need of any register bit under consideration to lock. The HPMS block is the same ASIC block as the SmartFusion2 MSS. See *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide* for information about the full set of system control registers. All registers listed as RW-P have write protection capability.

The IGLOO2 MSS Configurator allows enabling or disabling and configuring of each HPMS sub-block according to the user's application requirements.

The following figure shows the IGLOO2 MSS Configurator.

Figure 8 • **IGLOO2 MSS Configurator**



The IGLOO2 MSS Configurator allows enabling or disabling of the following sub-blocks.

- MDDR Controller
- SPI_0
- PDMA
- FIC_0 and FIC_1

Note: The other IP blocks shown in the GUI are not available in IGLOO2 and are automatically placed into reset by the Libero SoC Software tool.

At the time of device programming, Libero SoC software programs the SOFT_RESET_CR system register with the appropriate values based on the enable or disable configuration in the MSS Configurator.

Disabling a sub-block causes it to be held in reset when the device is powered up. While most of the HPMS sub-block states can be configured through MSS configurator, the following blocks are not available in MSS configurator to select their state:

- HPDMA
- Timers
- COMM_BLK
- DMA
- Embedded memories (eNVM_0, eNVM_1, eSRAM_0, eSRAM_1)

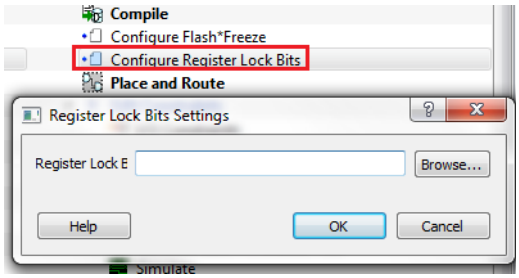
The DMA, high-performance DMA (HPDMA), and Timers are not in reset by default. However, these IP blocks require further configuration to be active. The COMM_BLK and embedded memories are active from power-up to support System Controller functions including device certificate read and SmartDebug support.

3.1.3 How to Set System Registers Write-Protection Bits

The **Configure Register Lock Bits** option available in the Libero SoC Design Flow is used to write-protect or lock the MSS, SERDES, and FDDR system registers to prevent them from being overwritten by masters that have access to these registers. Register write-protection bits or lock bits are set in a text (*.txt) file, which is then imported into the SmartFusion2 project. From the **Design Flow** window, click

Configure Register Lock Bits option to open the configurator. Click **Browse** to navigate to the text file (*.txt) that contains the register lock bits settings (see the following figure). The Libero SoC software generates the configuration data for write-protection flash bits based on user inputs.These flash bits are programmed at the time of device programming.

Figure 9 • **Register Lock Bit Settings**



3.1.3.1 Lock Bit File

An initial, default lock bit file will be generated by clicking **Generate FPGA Array Data** in the

Design Flow window.

The default file located at `<proj_location>/designer/<root>/<root>_init_config_lock_bits.txt` can be used to make the required changes.

The lock bits default configuration is unlocked. It is the user's responsibility to determine, which locks are desired and modify the locks bits file accordingly.

Starting in Libero SoC software v12.3, the lock-bits file will include all available lock-bits in the selected device.

Note: Save the file using a different name if you modify the text file to set the lock bits.

3.1.3.2 Lock Bit File Syntax

A valid entry in the lock bit configuration file is defined as a <lock_parameters> < lock bit value> pair format.

The lock parameters are structured as follows:

- Lock bits syntax for a register: <Physical block name>_<register name>_LOCK
- Lock bits syntax for a specific field: <Physical block name>_<register name>_<field name>_LOCK
- The following are the physical block names (varies with device family and die):
  - MSS
  - FDDR
  - SERDES_IF_x (where x is 0,1,2,3 to indicate the physical SERDES location) for SmartFusion2 M2S010/025/050/150 devices
  - SERDES_IF2 for SmartFusion2 M2S060/090 devices (only one SERDES block per device)
- Set the lock bit value to 1 to indicate that the register can be written to (unlocked) and to 0 to indicate that the register cannot be written to (locked)

Note: Lines starting with # or ; are comments. Empty lines are allowed in the lock bit configuration file.

The following figure shows the lock bit configuration file:

Figure 10 • **Lock Bit Configuration File**

```
# Register Lock Bits Configuration File for MSS, SERDES(s) and Fabric DDR
# Microsemi Corporation - Microsemi Libero Software Release v11.7 SP1 (Version 11.7.1.2)
# Date: Tue Mar 29 13:24:54 2016

# sb_sb_0/sb_sb_MSS_0/MSS_ADLIB_INST/INST_MSS_050_IP
 MSS_ESRAM_CONFIG_LOCK                          0
 MSS_ESRAM_MAX_LAT_LOCK                         1
 MSS_DDR_CONFIG_LOCK                            1
 MSS_ENVM_CONFIG_LOCK                           0
 MSS_ENVM_REMAP_BASE_LOCK                       1
 MSS_ENVM_FAB_REMAP_LOCK                        1
 MSS_CC_CONFIG_LOCK                             0
 MSS_CC_CACHEREGION_LOCK                        1
 MSS_CC_LOCKBASEADDR_LOCK                       1
 MSS_CC_FLUSHINDX_LOCK                          0
 MSS_DDRB_BUF_TIMER_LOCK                        1
 MSS_DDRB_NB_ADR_LOCK                           1
 MSS_DDRB_NB_SIZE_LOCK                          0
 MSS_DDRB_CONFIG_LOCK                           1
 MSS_EDAC_ENABLE_LOCK                           1
 MSS_MASTER_WEIGHT_CONFIG0_LOCK                 1
 MSS_MASTER_WEIGHT_CONFIG1_LOCK                 1
 MSS_SOFT_INTERRUPT_LOCK                        1
 MSS_SOFTRESET_ENVM0_SOFTRESET_LOCK             1
 MSS_SOFTRESET_ENVM1_SOFTRESET_LOCK             1
 MSS_SOFTRESET_ESRAM0_SOFTRESET_LOCK            1
 MSS_SOFTRESET_ESRAM1_SOFTRESET_LOCK            1
 MSS_SOFTRESET_MAC_SOFTRESET_LOCK               1
 MSS_SOFTRESET_PDMA_SOFTRESET_LOCK              1
 MSS_SOFTRESET_TIMER_SOFTRESET_LOCK             1
 MSS_SOFTRESET_MMUART0_SOFTRESET_LOCK           1
 MSS_SOFTRESET_MMUART1_SOFTRESET_LOCK           1
 MSS_SOFTRESET_G4SPI0_SOFTRESET_LOCK            1
 MSS_SOFTRESET_G4SPI1_SOFTRESET_LOCK            1
 MSS_SOFTRESET_I2C0_SOFTRESET_LOCK              1
 MSS_SOFTRESET_I2C1_SOFTRESET_LOCK              1
 MSS_SOFTRESET_CAN_SOFTRESET_LOCK               1
 MSS_SOFTRESET_USB_SOFTRESET_LOCK               1
 MSS_SOFTRESET_COMBLK_SOFTRESET_LOCK            1
 MSS_SOFTRESET_FPGA_SOFTRESET_LOCK              1
 MSS_SOFTRESET_HPDMA_SOFTRESET_LOCK             1
 MSS_SOFTRESET_FIC32_0_SOFTRESET_LOCK           1
 MSS_SOFTRESET_FIC32_1_SOFTRESET_LOCK           1
 MSS_SOFTRESET_MSS_GPIO_SOFTRESET_LOCK          1
 MSS_SOFTRESET_MSS_GPOUT_7_0_SOFT_RESET_LOCK    1
 MSS_SOFTRESET_MSS_GPOUT_15_8_SOFT_RESET_LOCK   1
 MSS_SOFTRESET_MSS_GPOUT_23_16_SOFT_RESET_LOCK  1
 MSS_SOFTRESET_MSS_GPOUT_31_24_SOFT_RESET_LOCK  1
 MSS_SOFTRESET_MDDR_CTLR_SOFTRESET_LOCK         1
 MSS_SOFTRESET_MDDR_FIC64_SOFTRESET_LOCK        1
 MSS_M3_CONFIG_LOCK                             1
```

3.1.3.3 Locking and Unlocking a Register

A register can be locked or unlocked by setting the appropriate lock bit value in the lock bit configuration.`txt` file.

1. Browse to locate the lock bit configuration.`txt` file.
2. Do one or both of the following:
   - Set the lock bit value to 0 for the registers you want to lock.
   - Set the lock bit value to 1 for the registers you want to unlock.
3. Save the file, and import the file into the project (**Design Flow** window > **Configure Register Lock Bits**), see Figure 9, page 11.
4. Regenerate the bitstream.

Note: Changing the content of the lock-bits file does not invalidate place-and-route. However, you must regenerate the FPGA array data and regenerate the bitstream for lock bit changes to take effect. The current state of lock bits can be seen in the regenerated lock bits file that is recreated during the **Generate FPGA Array Data**.

See the System Register Block chapter of *UG0331: SmartFusion2 Microcontroller Subsystem User Guide* for more information on system registers.

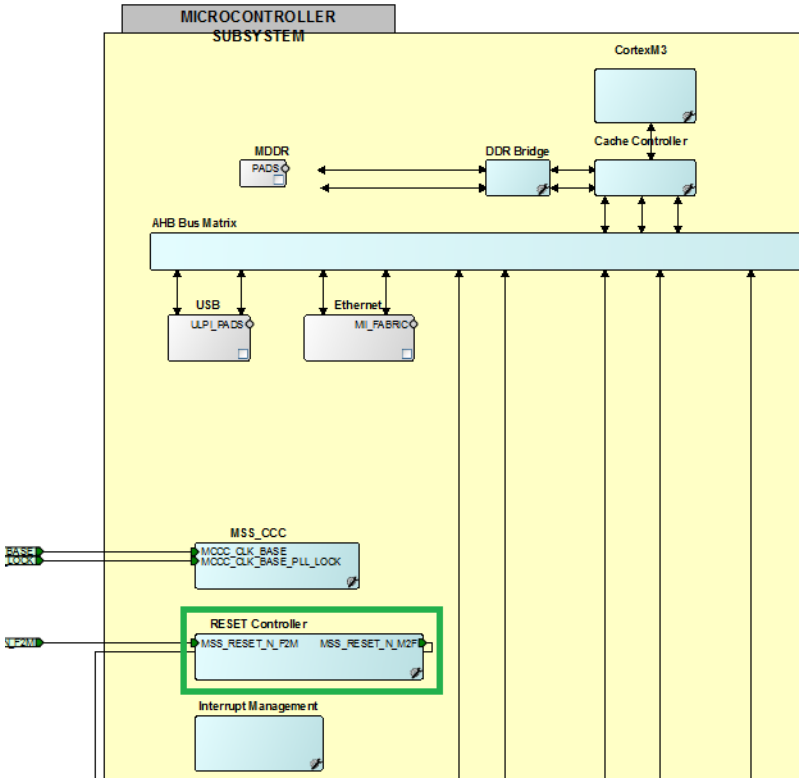
3.1.3.4 Keeping the Cortex-M3 Processor in Reset

In SmartFusion2 devices, the system controller keeps the Cortex-M3 processor in reset during device initialization. The state of the Cortex-M3 processor after device initialization is defined by the M3_RESET_N signal. The Cortex-M3 processor can be held in reset while the FPGA is powered by tying the M3_RESET_N signal to 0. The M3_RESET_N signal must be exposed to the FPGA fabric to tie it to 0. Tying the M3_RESET_N signal to '0' in the fabric means that the M3_RESET_N signal is directly driven from a flash bit and immune to SEUs.

The reset controller block in the MSS configurator GUI allows the user to access the M3_RESET_N signal via the FPGA fabric.

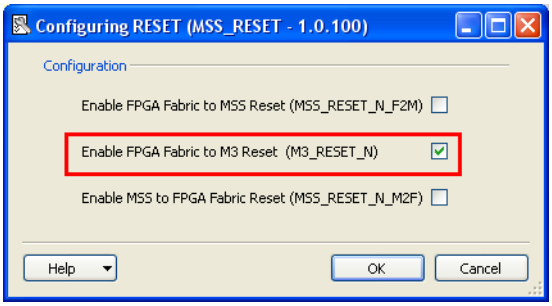
Double-click the RESET controller sub-block (Figure 11, page 13) of the MSS configurator to launch MSS RESET controller configurator.

Figure 11 • **Launching MSS RESET Controller Configurator**



The following figure shows how to configure the RESET controller sub-block to expose the M3_RESET_N signal to the FPGA fabric:

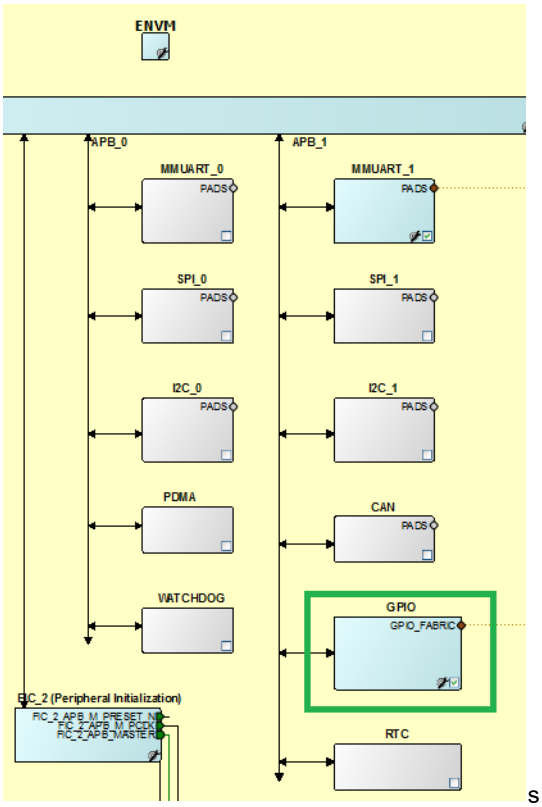
Figure 12 • **Exposing M3_RESET_N to FPGA Fabric**



The following steps describe how to monitor the state of the Cortex-M3 processor from the FPGA fabric using GPIOs:

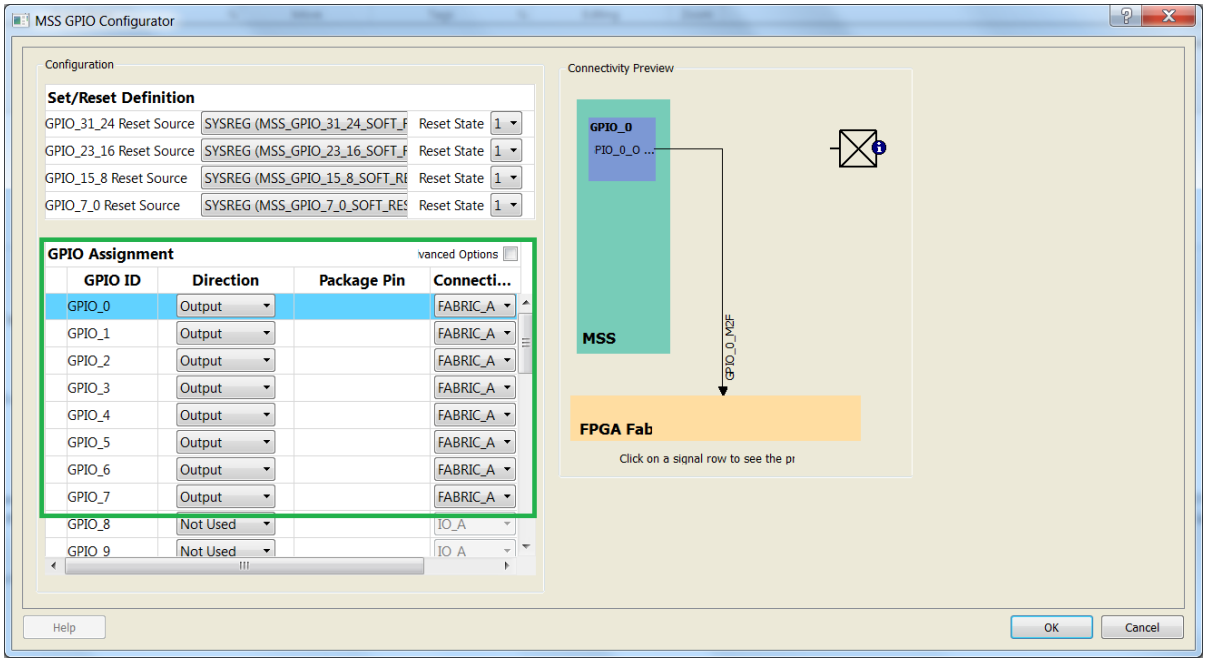
1. In the Libero project, double-click the GPIO sub-block (see, Figure 11, page 13) of the MSS configurator to launch the MSS GPIO configurator.

Figure 13 • **Launching MSS GPIO Configurator**



2. In the MSS GPIO configurator, configure several MSS GPIOs as outputs by selecting **Output** as **Direction** from the drop-down list, as shown in Figure 14, page 15.
3. Promote the configured MSS GPIOs to FPGA fabric by selecting **Fabric_A** from the drop-down list, as shown in Figure 14, page 15.

Figure 14 • **MSS GPIO Configuration**



4. Build a Cortex-M3 executable application program to drive a known pattern on these MSS GPIOs. For more information about how to build an Cortex-M3 executable application program using Microsemi tools, see *TU0546: SoftConsole v4.0 and Libero SoC v11.7 Tutorial*.
5. Add a data storage client to the eNVM with the preceding MSS GPIO application program as its content. This application program is automatically executed when the Cortex-M3 processor is out of reset. For information about how to add a eNVM data storage client, see *AC426: Implementing Production Release Mode Programming for SmartFusion2 Application Note*.
6. During device run-time, monitor these MSS GPIOs from FPGA fabric logic. If any activity is detected on these MSS GPIOs, it indicates that the Cortex-M3 processor is not in reset, and the design must take action as required.

In IGLOO2 devices, the Cortex-M3 device is disabled at the factory by programming the M3_ALLOWED flash bit = 0. This permanently disables the Cortex-M3 in IGLOO2 devices. When an IGLOO2 device is targeted in the Libero SoC software tool, the M3_DISABLE flash bit is set to 1 and the M3_RESET_N signal is tied to 0 in the FPGA fabric through a flash bit. This ensures the Cortex-M3 is non-operable in the IGLOO2 devices. Verification that the M3 is disabled can be obtained by reading the device information through JTAG which reports the state of the M3_ALLOWED bit. Starting in Libero SoC software v12.3, the state of the configured M3_ALLOWED flash bit can be read over JTAG using the DEVICE_INFO STAPL file action provided that the MSS is not in reset (MSS_RESET_N_F2M = 1).

3.2 Protecting the SerDes, MDDR, and FDDR Configuration

The SerDes, MDDR and FDDR IP blocks have system configuration registers. These registers are loaded at power-up by a bus master in the design (Cortex-M3, CoreABC, CoreConfigMaster). These registers have write protection capability to protect the configuration from SEUs or unintended writes. Because these registers are loaded at power-up, the write protection should not be enabled to any of the system configuration registers that are configured to a value not equal to the register reset value. Enabling the write-protection will prevent the bus master from modifying the register. The specific registers loaded at power-up can be found in the generated <ip name>_init_abc.txt file located in the IP blocks folder under component/work directory.

See Appendix: System Register Description, page 29, for definitions of SerDes, MDDR, and FDDR configuration registers.

If the user desires to lock any of these registers, see How to Set System Registers Write-Protection Bits, page 11 for description about how to set write-protection bits.

3.3 Isolating unused MSS/HPMS/FDDR/SerDes Blocks

Any unused hard IP blocks (MSS in SmartFusion2, HPMS in IGLOO2, FDDR, and SERDESIF's) can be isolated from rest of the FPGA. If any of the available hard IP blocks are not used in a design (not instantiated by the user), then Libero SoC software automatically configures them into a state where they are isolated from impacting any other part of the device. This is achieved by Libero SoC software asserting all instantiated IP internal soft reset bits, configuring all IP sub-block soft register bits and hard driving critical IP inputs. The driven IP inputs are directly driven from SEU immune flash bits. The IP outputs and bus interfaces are not available for connection by the end user effectively isolating the IP block from the reset of the FPGA. All soft register bits have an associated, flash-based, lock bit that can be set by the user to ensure that the soft register bits cannot be changed by an SEU event.

An exception to this configuration is the MSS in SmartFusion2 or HPMS in IGLOO2. These blocks are not completely disabled when un-instantiated. These IP blocks have a subset of modules that remain active to support device programming. Part of the device programming algorithm is to verify the device type, which is located in a device certificate programmed into the device during the manufacturing process. In order for the system controller to read this certificate, the eNVM and COMBLOCK need to be enabled and the MSS/HPMS not in hard reset (MSS_RESET_N_F2M deasserted). This is the default configuration when the MSS/HPMS is not instantiated in the user design, so no user configuration is required.

Note: The Cortex-M3 is not required for device type verification or device programming, it is held in hard, SEU protected reset if the MSS is not instantiated in the design.

Starting in the Libero SoC software v12.3, an enhanced report file (<design>_init_config.txt) is generated which reports the register settings and input signal configuration of all instantiated and un-instantiated IP blocks. Additionally, enhancements are made to the lock bits file (<design>_init_config_lock_bits.txt) which reports all registers in the device that have an available lock bit. All lock bits are set to inactive, the user can optionally enable these write-protection bits to provide additional assurance that the register bits will not change state. It is recommended that users only lock bits on IP blocks that are not used in the design. IP blocks used in a design can have register bits actively changed while in use so locking them is not recommended.

If desired, a user can validate that the Libero SoC software tool configured their unused IP blocks as expected by comparing their <design>_init_config.txt design output to what is provided in the output file in Appendix: Configuration of Unused IP Blocks, page 38.

With un-instantiated IP configured by the Libero SoC tool along with activation of the lock bits, these IP blocks will not interfere with the operation of the FPGA and are SEU protected for configuration changes. With this level of protection, there is no need for the user to actively monitor these blocks. The recommendation is to not instantiate unused IP blocks and set the lock bits for these unused IP blocks to active state.

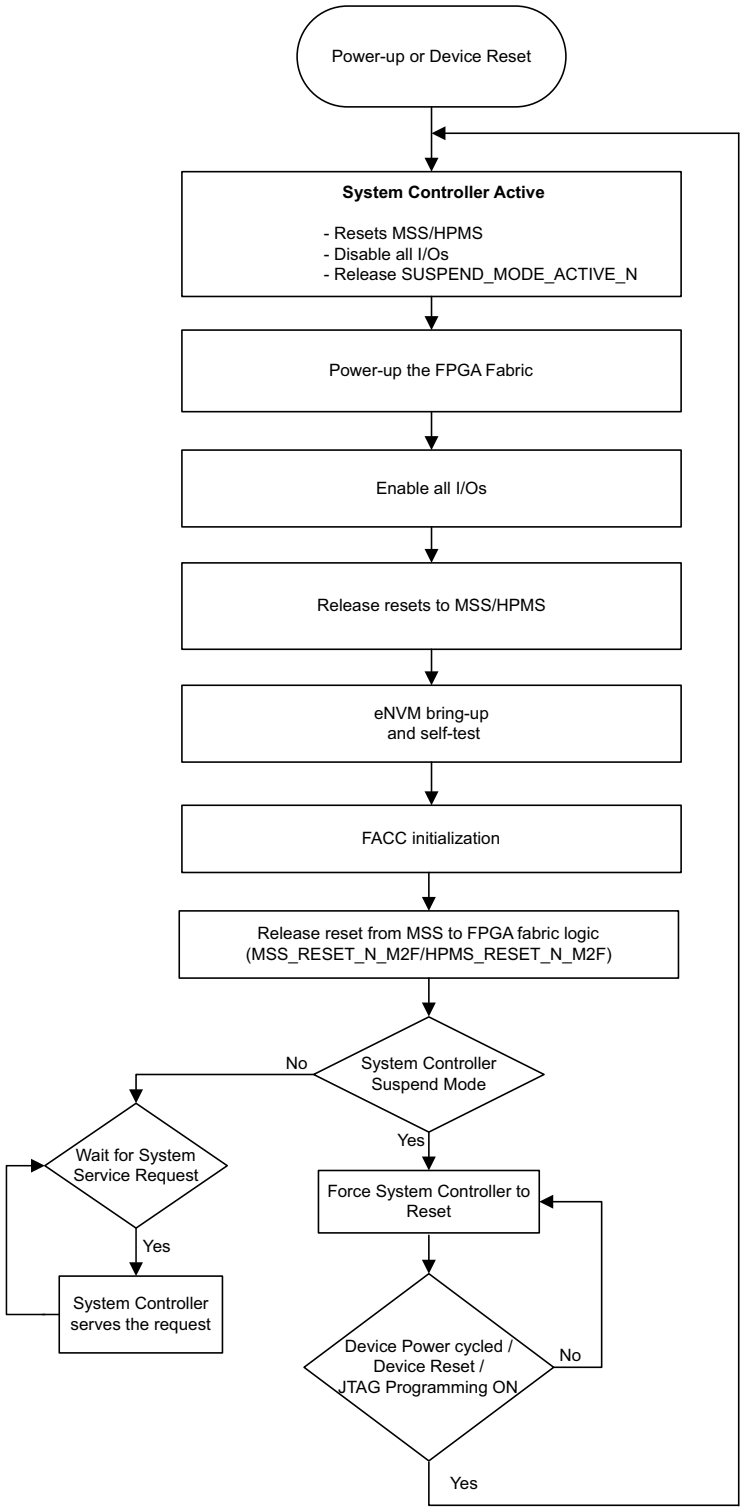
Note: In cases where certain IP block interfaces are not used, the associated hard device I/O pins need to be configured properly, see *AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note* for more information.

3.4 Isolating System Controller

In SmartFusion2 and IGLOO2 devices, the system controller manages device initialization, programming operations, and handles the system service requests. After power-on-reset or device reset (DEVRST_N) events, the system controller performs the initialization sequence of the I/O banks, FPGA fabric, and MSS or HPMS.

The following figure shows the flow chart of sequence of operations performed by the system controller:

Figure 15 • **Device Initialization Sequence Performed by System Controller**



The system controller can be held in suspend mode after the completion of device initialization to protect the device from unintended device programming or zeroization of the device due to SEUs.

The system controller suspend mode is designed to provide an SEU immune reset state for the system controller. The system controller reset generation circuitry is designed with a triple modular redundancy (TMR) self-refreshing latch to provide SEU immunity. In this mode, the system controller is held in reset while its output ports to the rest of the system are forced to known and well-determined states.

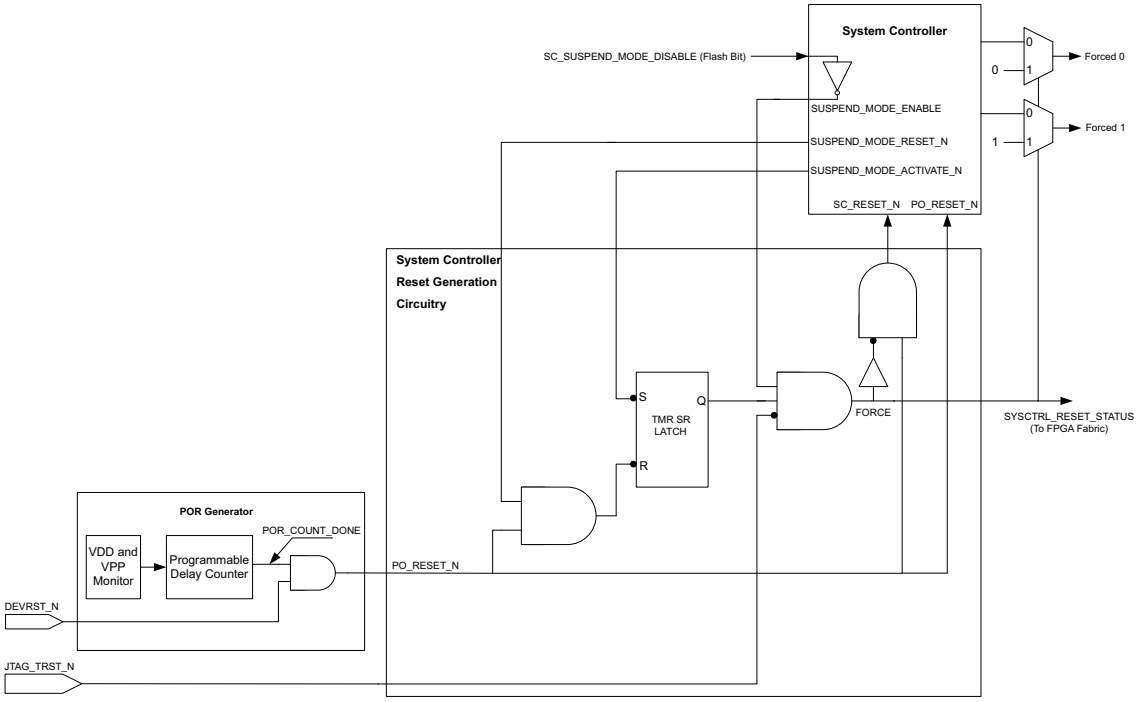
System controller suspend mode is controlled by a flash bit (SC_SUSPEND_MODE_DISABLE), which is set during device programming, and is not accessible either by external pin or from within the design. It is only accessed by the programming file loaded into the device, during programming. Since the SC_SUSPEND_MODE_DISABLE control bit is stored in a flash cell, it is immune to SEUs.

- If SC_SUSPEND_MODE_DISABLE = 1, the system controller suspend mode is disabled.
- If SC_SUSPEND_MODE_DISABLE = 0, the system controller suspend mode is enabled.

In system controller suspend mode, the system controller is held in a reset state and cannot provide any system services such as Flash*Freeze service, cryptographic services, or programming services. The Libero SoC software tool bit that corresponds to SC_SUSPEND_MODE_DISABLE is the SYSTEM_CONTROLLER_SUSPEND_MODE bit that can be controlled using the GUI or through a tcl command, see Enabling System Controller Suspend Mode Using Libero SoC Software, page 20.

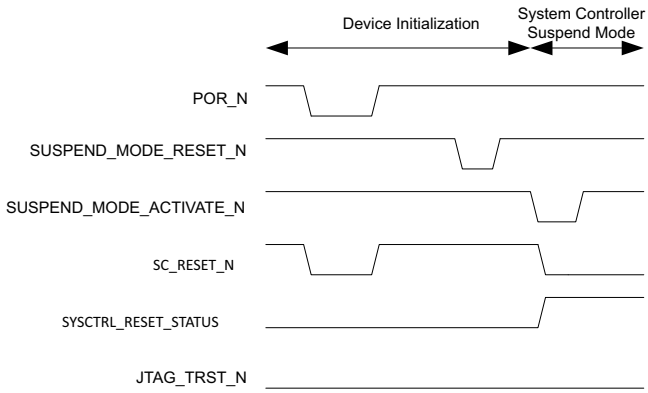
The following figure shows the system controller reset generation circuitry.

Figure 16 • **System Controller Reset Generation Circuitry**



The following figure shows the activation sequence for the system controller suspend mode.

Figure 17 • **System Controller Suspend Mode Activation after Device Initialization**



The system controller becomes active if the device is power-cycled or if a hard reset (DEVRST_N) is applied, but it returns to suspend mode after the initialization cycle is completed. To restore normal operation, the device must be reprogrammed with the system controller suspend mode turned off

(SC_SUSPEND_MODE_DISABLE = 1).

After the device has entered the suspend mode, the system controller is held in reset and cannot respond to the reprogramming requests. To facilitate reprogramming of the device, the JTAG_TRST_N pin is used to gate the internal FORCE signal and releases the system controller from reset. In an avionics environment, JTAG_TRST_N must be held asserted to prevent JTAG circuitry from affecting the I/Os due to SEUs. Releasing JTAG_TRST_N puts the system controller out of reset and allows the device to be reprogrammed.

When a programming mode instruction is loaded, the system controller sends a pulse on SUSPEND_MODE_RESET_N to clear the TMR latch so that the device can re-execute a normal boot sequence after programming is completed.

Reprogramming via the system controller SPI (SC_SPI) interface is also possible. However, JTAG_TRST_N must be controlled by the external host.

As shown in Figure 16, page 18 the state of the system controller can be monitored by the FPGA fabric logic by reading the state of the SYSCTRL_RESET_STATUS signal.

- If SYSCTRL_RESET_STATUS = 1, the system controller suspend mode is enabled.
- If SYSCTRL_RESET_STATUS = 0, the system controller suspend mode is disabled.

Note: The SYSCTRL_RESET_STATUS signal is available in all SmartFusion2 and IGLOO2 devices except M2S050 and M2GL050 variants.

For information on system controller reset status monitoring, see Monitoring System Controller Reset Status from FPGA Fabric, page 23.

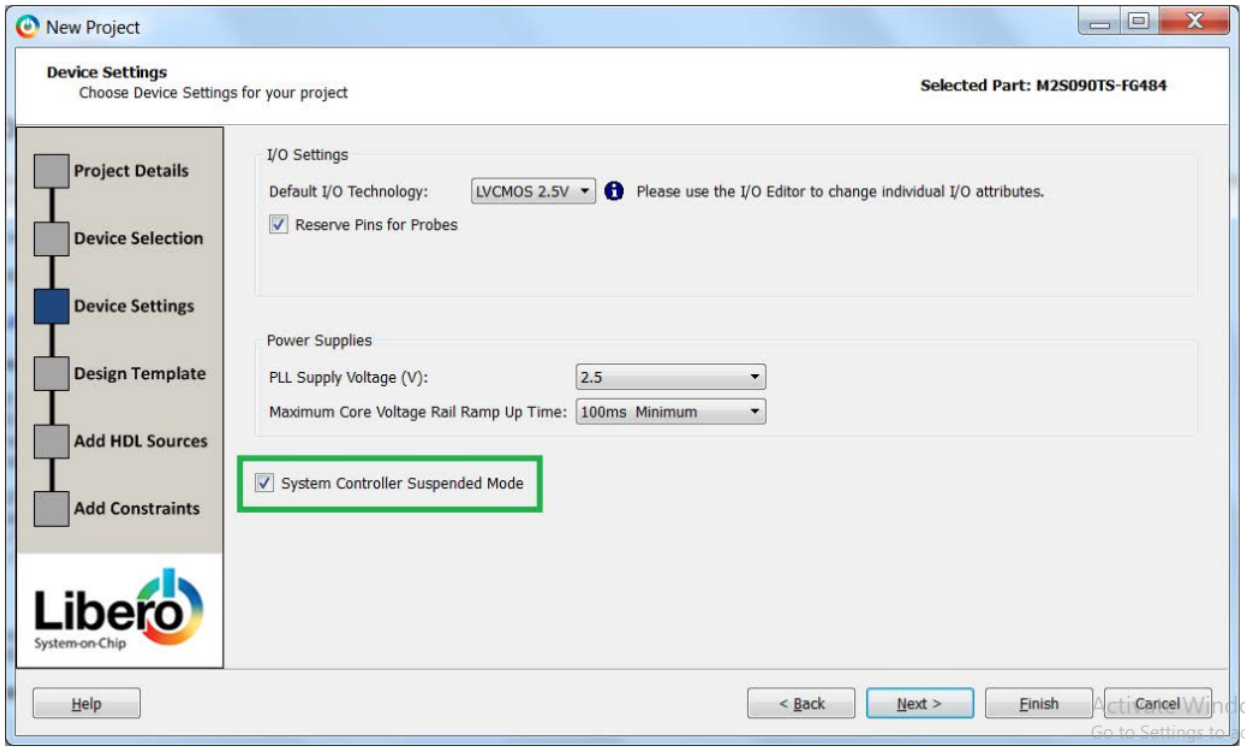
Note: To keep the system controller in suspend mode, the FLASH_GOLDEN_N pin must be tied to high at power-up or during assertion of the device reset pin (DEVRST_N). If the FLASH_GOLDEN_N pin is set to low at power-up or during assertion of the DEVRST_N pin, the device enters the auto-programming mode. For more information on auto-programming mode, see *UG0451: IGLOO2 and SmartFusion2 Programming User Guide*.

3.4.1 Enabling System Controller Suspend Mode Using Libero SoC Software

The system controller suspend mode feature can be configured (enabled/disabled) using the Libero SoC software in the following two ways:

- At the time of project creation, select the **System Controller Suspended Mode** check box in the **New Project- Device Settings** page as shown in the following figure.

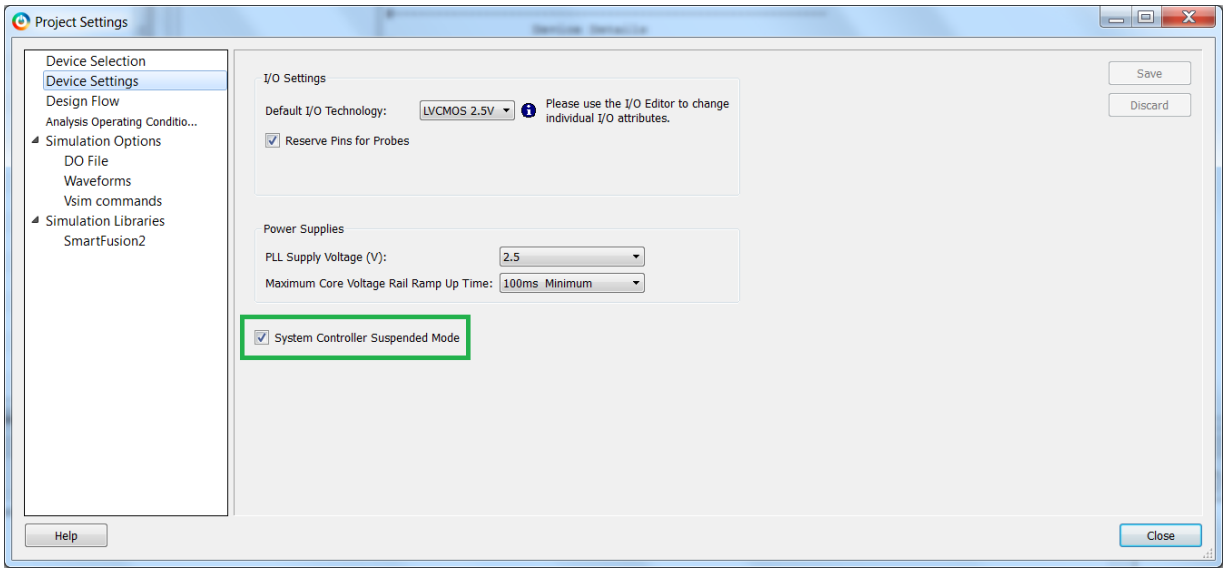
Figure 18 • **Enabling System Controller Suspend Mode in New Project- Device Settings Page**



This can also be accomplished by adding the switch -adv_options {SYSTEM_CONTROLLER_SUSPEND_MODE:1} to the "new_project" tcl command.

- In an existing project, the system controller suspend mode can be enabled by selecting the **System Controller Suspended Mode** check box under **Device Settings** of the **Project Settings** window as shown in the following figure.

Figure 19 • **Enabling System Controller Suspend Mode in Project Settings Window**



The programming file generated with this configuration sets the suspend mode flash bit (SC_SUSPEND_MODE_DISABLE = 1) when the device is programmed.

This can also be accomplished by adding the switch -adv_options {SYSTEM_CONTROLLER_SUSPEN_MODE:1} to the "set_device" tcl command

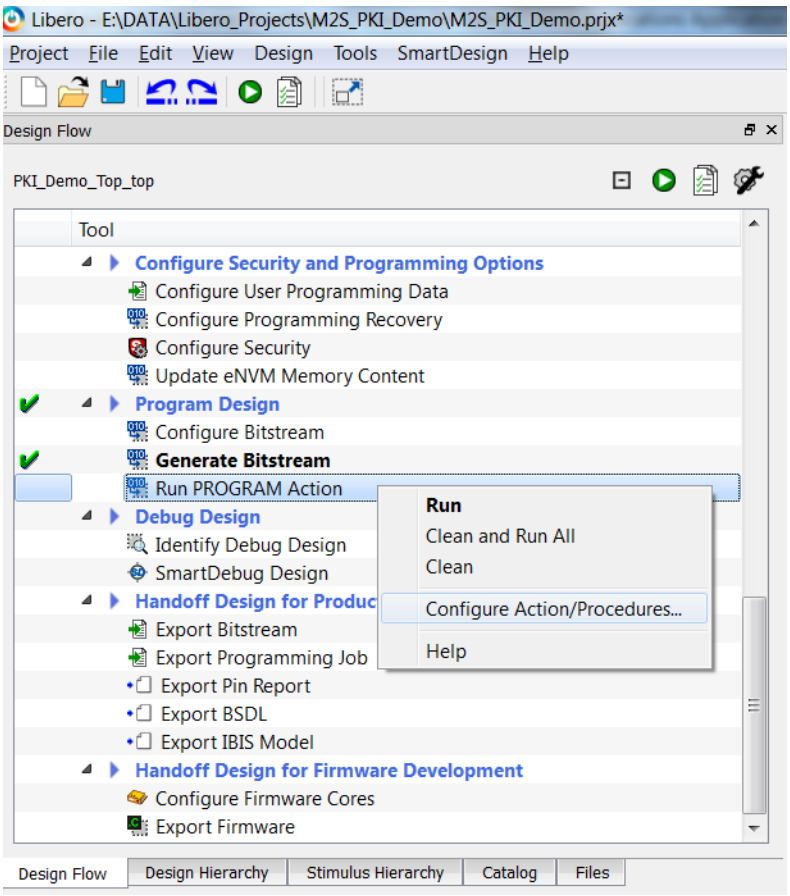
Note: Changing the state of the system controller suspend mode does not invalidate place-and-route. User only needs to regenerate the programming bitstream.

3.4.2 Reading the State of System Controller Suspend Mode Flash Bit through JTAG

The state of the system controller suspend mode flash bit can be read through JTAG by running DEVICE_INFO programming action using the Libero SoC software. Following are the steps to run the DEVICE_INFO programming action:

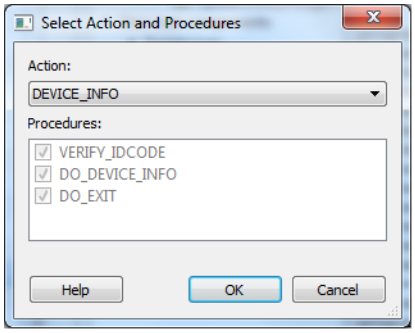
1. Right-click **Run PROGRAM Action** in the **Design Flow** tab of Libero SoC software, and select **Configure Action/Procedures**, as shown in the following figure.

Figure 20 • **Selecting Configure Action/Procedures**



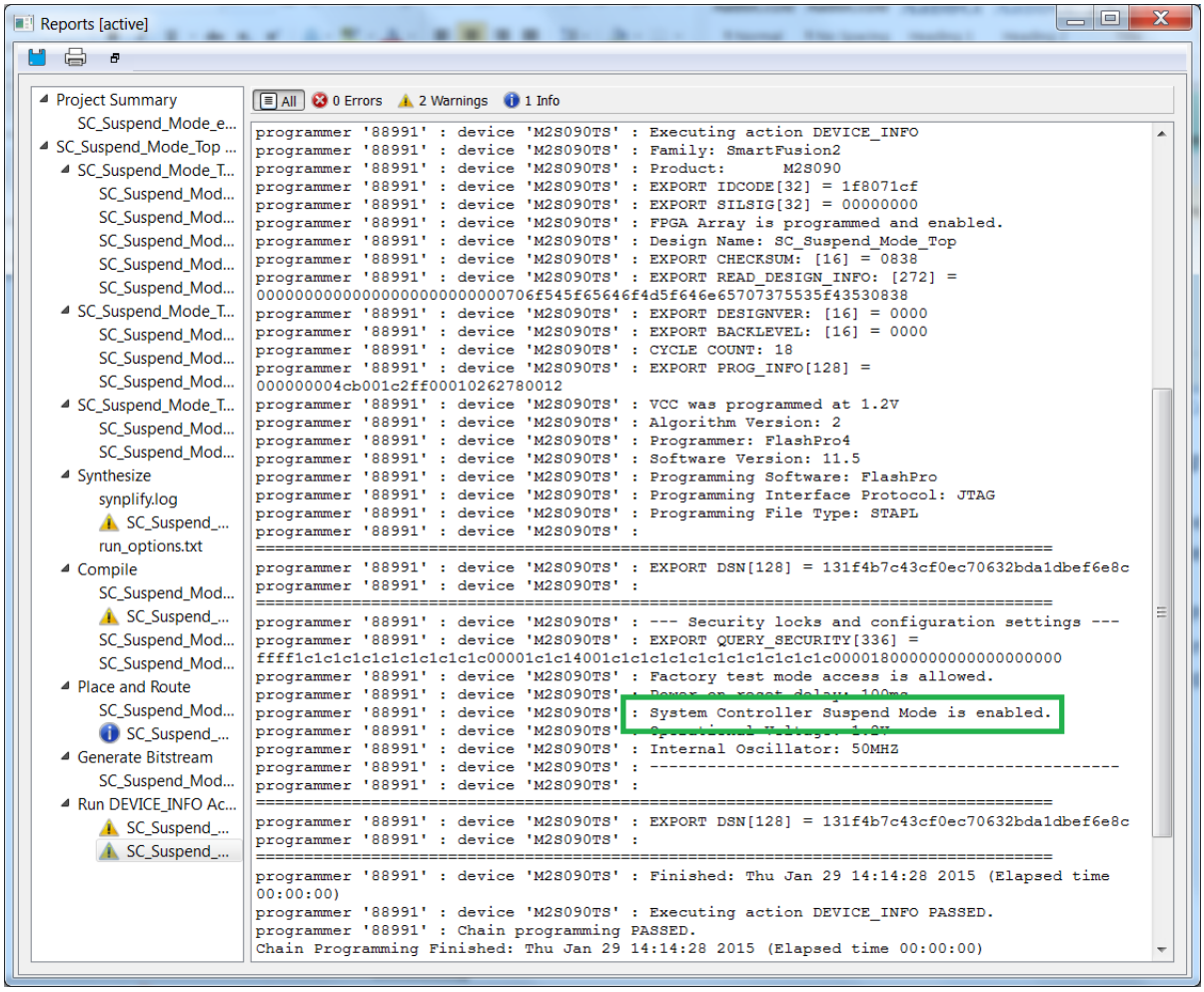
2. In the **Select Action and Procedures** dialog box, select **DEVICE_INFO** as Action, and click **OK**, as shown in the following figure.

Figure 21 • **Selecting DEVICE_INFO Action**



3. Right-click **Run PROGRAM Action** in the **Design Flow** tab and select **Run**. After the successful completion of this action, the system controller suspend mode status is displayed in the **Reports** window, as shown in the following figure.

Figure 22 • **System Controller Suspend Mode Status in Reports Window**



3.4.3 Monitoring System Controller Reset Status from FPGA Fabric

At run-time, the status of the system controller can be monitored from the FPGA fabric using **System Controller Reset Status (SYSCTRL_RESET_STATUS)** macro.

To monitor the system controller reset status, drag-and-drop the **SYSCTRL_RESET_STATUS** macro from the **Catalog** window on to Libero SoC software canvas, as shown in Figure 23, page 24 and Figure 24, page 24.

The RESET_STATUS port from the macro can be connected to the fabric logic to monitor the system controller reset status.

- If RESET_STATUS = 1, the system controller suspend mode is enabled.
- If RESET_STATUS = 0, the system controller suspend mode is disabled.

Figure 23 • **Catalog Window**

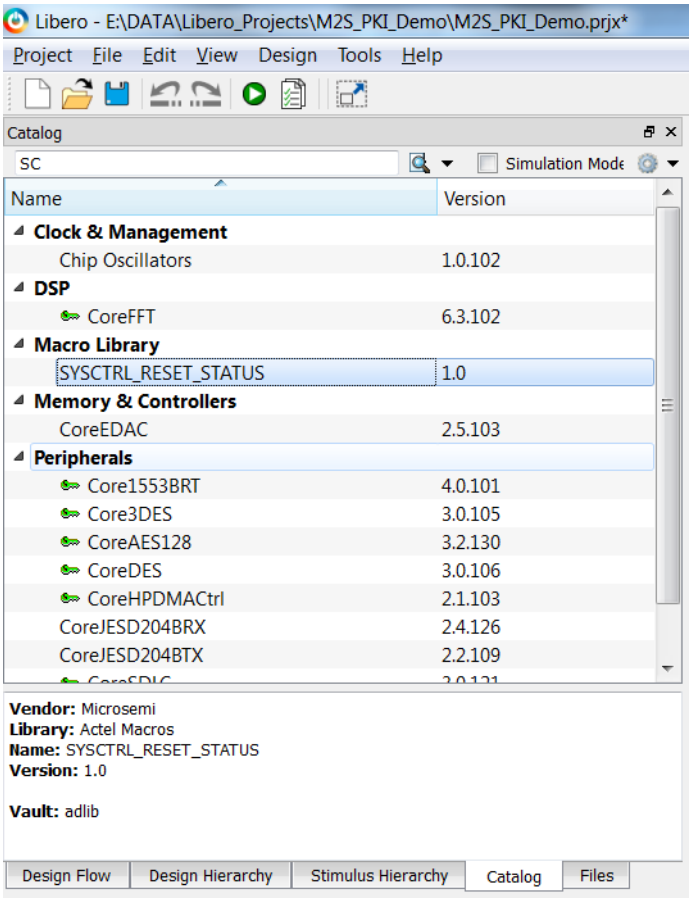
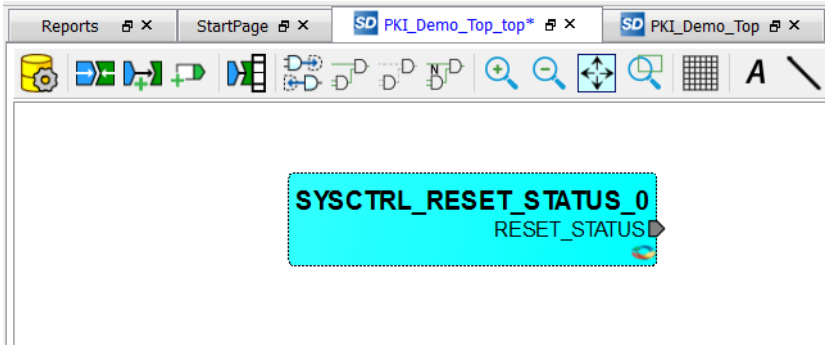


Figure 24 • **System Controller Reset Status Macro**



3.5 Configuring SmartDebug circuits for Safety-Critical Applications

3.5.1 SmartDebug Architecture

SmartFusion2 and IGLOO2 devices contain additional logic to support design debug. SmartDebug circuitry supports the following debug capabilities:

- Live Probe
- Active Probe
- Fabric RAM Block access
- eNVM read access
- Fabric Hardware Breakpoint (FHB)
- SerDes debug

The SmartDebug circuitry is mastered by the embedded System Controller which is controlled by commands over the JTAG interface. The system controller converts JTAG commands to various bus accesses to control the SmartDebug logic.

3.5.2 SmartDebug Avionics Radiation Exposure and Mitigation

The underlying SmartDebug circuitry is implemented primarily by hard ASIC logic. The exception being the Fabric Hardware Breakpoints where the logic is implemented in FPGA fabric logic. The ASIC logic is mainly asynchronous logic with some amount of synchronous logic. Adhering to the recommendations provided as follows hold the majority of synchronous logic in reset, minimizing any deleterious effects due to radiation expose for avionics applications. The remaining asynchronous logic would require multiple SET events to result in an unwanted SmartDebug access. This is due to the bus style architecture required to access these circuits. To minimize the impact of Avionics radiation exposure, it is recommended to disable and/or minimizing the SmartDebug circuitry by considering the following:

1. Enable the System Controller suspend mode. In this configuration, the system controller is driven into asynchronous reset. In this state, the controller cannot initiate an access to the SmartDebug circuity due to an SEU/T event. In this mode, the System Controller reset output holds the majority of the SmartDebug target co-located logic in reset.
2. Disable the Fabric Hardware Breakpoints (FHB). This removes the circuitry from the FPGA fabric, reducing SEU/T footprint of the design proportionally.
3. Reserve the two available Live Probe pins and do not use them as user I/O.

Note: When the system controller is in suspend mode, it cannot provide any system services such as Flash*Freeze, cryptographic services and programming services.

Any upsets in SmartDebug circuitry are covered by default in MCHP SEU reports, which show overall SEU rates at levels acceptable or better for aviation applications.

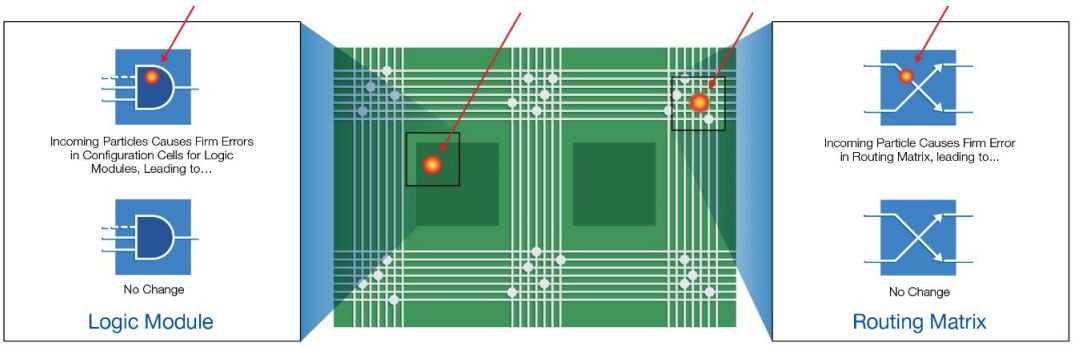
3.6 Radiation Considerations and Single Event Effects (SEE)

Malfunctions in Integrated Circuits (ICs) due to radiation effects (single event effects) from high energy neutrons at ground level and high altitudes are a major concern for safety-critical applications. Configuration upsets in FPGAs are problematic because the configuration memory must remain static and error free during all the operating hours of the device for correct operation. Any upset will be persistent until the device is powered-down or the cell is reprogrammed correctly. If an upset occurs in the erroneous state, the logic or routing of the FPGA fabric will be wrong, potentially causing not just a single wrong data value, but a string of wrong results until it is fixed. This may require a full system reboot. Attempts to mitigate configuration upsets in SRAM FPGAs are extremely complex. Typically, they require dual-redundant FPGAs with an external controller, which periodically searches for configuration errors in each SRAM FPGA and initiates a fail-over from primary to secondary FPGA while reprogramming of the primary FPGA takes place. This presumes that the system will not be detrimentally affected by the bad data produced by the FPGA during the period that the configuration SEU is undetected. It also presumes that the system can tolerate the subsequent loss of processing while the fail-over from primary to secondary takes place.

IGLOO2 FPGA and SmartFusion2 SoC FPGA configuration is SEE immune because of the non-volatile technology, unlike the configuration memory in SRAM-based FPGAs, which can flip state due to neutron hits. Neutron and alpha radiation do not have adverse effects on the configuration of Microchip's flash-based FPGAs. Microchip offers extremely reliable FPGAs for many applications, including military, aerospace, industrial control, medical, automotive, networking, and communications.

- Microchip's flash-based FPGAs are not susceptible to configuration loss due to single event errors (SEE) caused by alpha or neutron radiation
- No SEE mitigation techniques for configuration upsets are required in Microchip FPGAs, reducing overall system cost (maintaining low overall system cost)
- Microchip FPGAs maintain system integrity at high altitudes and at sea level

Figure 25 • **Microchip FPGAs configuration is immune to upsets**



3.6.1 Radiation exposure of IOMUX

The hard communications IP blocks available in the MSS/HPMS have I/O interfaces that can be optionally routed to FPGA I/O pins or to the FPGA fabric. The selection of the connection is made by the user when configuring the MSS via the Libero SoC software MSS/HPMS GUI interfaces. There are IOMUX structures implemented in the device to statically control this configuration at device power-up. The IOMUX is controlled by registers automatically loaded at power-up. These registers are protected by lock-bits that can be set to protect these registers from changing state due to SEU event. There is a small but non-zero chance that the IOMUX control could be affected by a SET event resulting in possibility of the communications block I/O temporarily glitching. Device I/Os that are connected to/from the FPGA fabric are not exposed to this potential issue. This phenomenon has not been observed in radiation testing but cannot be completely ruled out. Designers using these IP blocks should be aware of this possibility. The MSS/HPMS IP blocks with IOMUX structures are—CAN, Ethernet, GPIO, I2C_0/1, MMUART_0/1, SPI_0/1, USB.

3.6.2 Neutron Radiation Test Results Summary

To get Neutron SEE reports on Microchip's different product family of FPGAs, see *https://www.microsemi.com/product-directory/reliability/4883-see#documents*

Or

Download *IGLOO2 and SmartFusion2 Report*.

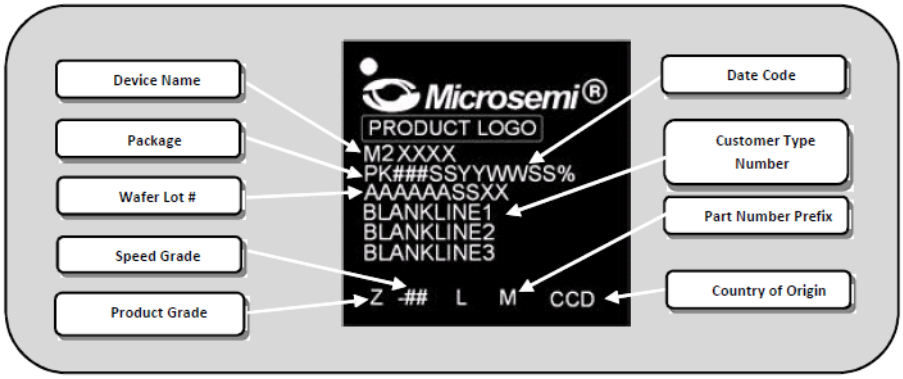
3.7 Device Identification and Programming Considerations

This section provides information to identify SmartFusion2/IGLOO2 devices visually and electronically. Device Programming information is also provided.

3.7.1 Device Identification

Microsemi SmartFusion2/IGLOO2 devices have external labeling to distinguish devices. The following figure shows the device labeling format.

Figure 26 • **Device Labeling Format**



Device information can also be obtained electronically over JTAG. Execution of the STP file DEVICE_INFO action over JTAG returns the following information:

- **Device Family**: SmartFusion2 | IGLOO2
- **Product ID**: M2S150 | 090 |060 | 050 |025 | 010 | 005
  M2GL150 | 090 |060 | 050 |025 | 010 | 005
- **Feature Activation M3_ALLOWED**: 0(M3 disabled) | 1 (M3 enabled)
- **Device Serial Number**: Unique 128 bit value

During the manufacture flow, IGOO2 devices have their M3_ALLOWED flash bit programmed to 0 and verified. An X.509 device certificate is then injected into the device to certify the device family and product identification. Once complete, the physical device labeling is added.

The user is required to generate a STP programming file using Libero SoC software. There are no specific Libero SoC software tool configurations required to properly generate a STP programming file.

3.7.2 Device Programming

SmartFusion2/IGLOO2 devices can be programmed only with an encrypted bitstream. The Libero SoC software tool generates only encrypted bitstreams to protect the user design IP. The encrypted bitstream is decrypted on-the-fly during programming and will only successfully program if the decryption is successful and authenticated. The Libero SoC software tool can generate an encrypted STP file using the ‘Export Bitstream’ feature of the Libero SoC software tool. No tool settings required if the user is generating a STP file encrypted with the default key.

To take full advantage of device information reporting and device validation prior to JTAG programming, Microsemi recommends the use of a STP programming file.

Execution of the JTAG ‘PROGRAM’ action JTAG programs the device. Before the device programs, the STP action compares the device density read from the device to the STP file device density. If there is a match, then the process continues. The process then reads the device certificate to determine if the

device is a SmartFusion2 (M2S) device or an IGLOO2 (M2GL) device. Once determined, programming continues as follows:

Table 1 • **Device Programming**

Bitstream Target	Device	Program Action	Comment
M2S	M2S	Device programmed	
M2S	M2GL	Device not programmed	Illegal because M3 is not enabled in M2GL devices
M2GL	M2GL	Device programmed	
M2GL	M2S	Device Programmed	This is legal because M2GL a subset of M2S

The preceding validation checks are automatic, which are available in the STP file. No user configuration is required to generate a STP file containing these device checks.

3.8 Conclusion

SmartFusion2 SoC FPGAs and IGLOO2 FPGAs provide several advantages to the designers of safety-critical systems. The inherent immunity of the flash technology to terrestrial and atmospheric radiation effects makes the devices suitable for safety-critical applications in industrial control, medical, aviation, and military applications. The high reliability of tried-and-trusted 65 nm flash brings more assurance. Flexibility of SmartFusion2 and IGLOO2 devices comes from its embedded system controller and hard IP blocks. To minimize the effects of radiation on SmartFusion2/IGLOO2 devices, follow the recommendations detailed in this application note.

4 Appendix: System Register Description

4.1 MSS SYSREG Configuration Registers

The following table is a list of SYSREG configuration registers to be used to hold MSS blocks in reset for safety-critical avionics applications. For a complete list of all MSS system registers, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*

4.1.1 MSS Software Reset Control Register

Note: The reset state of a bit depends on resource that is enabled or disabled. See the user design <root>_init_config.xml file to view the reset value for these bits.

Table 2 • **SOFT_RESET_CR**

Bit Number	Name	Description
[31:27]	Reserved	Reserved
26	MDDR_FIC64_SOFTRESET	0: Releases DDR_FIC controller from reset. 1: Keeps DDR_FIC controller in reset.
25	MDDR_CTLR_SOFTRESET	0: Releases MDDR controller from reset. 1: Keeps MMDR controller in reset.
24	MSS_GPOUT_31_24_SOFTRESET	0: Releases GPIO_OUT[31:24] from reset. 1: Keeps GPIO_OUT[31:24] in reset.
23	MSS_GPOUT_23_16_SOFTRESET	0: Releases GPIO_OUT[23:16] from reset. 1: Keeps GPIO_OUT[23:16] in reset.
22	MSS_GPOUT_15_8_SOFTRESET	0: Releases GPIO_OUT[15:8] from reset. 1: Keeps GPIO_OUT[15:8] in reset.
21	MSS_GPOUT_7_0_SOFTRESET	0: Releases GPIO_OUT[7:0] from reset. 1: Keeps GPIO_OUT[7:0] in reset.
20	MSS_GPIO_SOFTRESET	0:Releases the GPIO from reset, as long as it isn't being held in reset by some other means. 1: Keeps the GPIO to be held in reset. Asserting this soft reset bit holds APB register, GPIO input, interrupt generation logic in reset. GPIO OUT logic is not affected by this reset.
19	FIC32_1_SOFTRESET	0: Releases FIC _1 from reset. 1: Keeps FIC_1 in reset.
18	FIC32_0_SOFTRESET	0: Releases FIC _0 from reset. 1: Keeps FIC_0 in reset.
17	HPDMA_SOFTRESET	0: Releases HPDMA from reset. 1: Keeps HPDMA n reset.
16	FPGA_SOFTRESET	0: Releases FPGA from reset (MSS_M2F_RESET_N) 1: Keeps FPGA in reset (MSS_M2F_RESET_N)
15	COMBLK_SOFTRESET	0: Releases COMM_BLK from reset. 1: Keeps COMMUNICTIONK BLOCK (COMM_BLK) in reset.
14	USB_SOFTRESET	0: Releases USB from reset. 1: Keeps USB in reset.
13	CAN_SOFTRESET	0: Releases CAN from reset. 1: Keeps CAN in reset.

Table 2 • **SOFT_RESET_CR** ***(continued)***

Bit Number	Name	Description
12	I2C1_SOFTRESET	0: Releases I2C_1 from reset. 1: Keeps I2C_1 in reset.
11	I2C0_SOFTRESET	0: Releases I2C_0 from reset. 1: Keeps I2C_0 in reset.
10	SPI1_SOFTRESET	0: Releases SPI1 from reset. 1: Keeps SPI1 in reset.
9	SPI0_SOFTRESET	0: Releases SPI0 from reset. 1: Keeps SPI0in reset.
8	MMUART1_SOFTRESET	0: Releases MMUART_1 from reset. 1: Keeps MMUART_1 in reset.
7	MMUART0_SOFTRESET	0: Releases MMUART_0 from reset. 1: Keeps MMUART_0 in reset.
6	TIMER_SOFTRESET	0: Releases the system timer from reset. 1: Keeps the system timer in reset.
5	PDMA_SOFTRESET	0: Releases the PDMA from reset. 1: Keeps the PDMA in reset.
4	MAC_SOFTRESET	0: Releases the Ethernet MAC from reset. 1: Keeps the Ethernet MAC in reset.
3	ESRAM1_SOFTRESET	0: Releases the ESRAM_1 memory controller from reset. 1: Keeps the ESRAM_1 memory controller in reset.
2	ESRAM0_SOFTRESET	0: Releases the ESRAM_0 memory controller from reset. 1: Keeps the ESRAM_0 memory controller in reset.
1	ENVM1_SOFTRESET	0: Releases the ENVM_1memory controller from reset. 1: Keeps the ENVM_1 memory controller in reset.
0	ENVM0_SOFTRESET	0: Releases the ENVM_0 memory controller from reset. 1: Keeps the ENVM_0 memory controller in reset.

4.1.2 MSS M3 Cache Control Register

Note: The reset state of a bit depends on the resource that is enabled or disabled. See the user design <root>_init_config.xml file to view the reset value for these bits.

Table 3 • **CC_CR**

Bit Number	Name	Reset Value	Description
[31:3]	Reserved	0	Reserved
2	CC_CACHE_LOCK	0	This signal allows the cache lock to be enabled. The allowed values are: 0: Cache lock disabled 1: Cache lock enabled
1	CC_SBUS_WR_MODE	0	This signal allows debug mode SBUS writes to cache memory to be enabled. The allowed values are: 0: Debug mode SBUS write disabled 1: Debug mode SBUS write enabled
0	CC_CACHE_ENB	0	This signal allows the cache to be disabled. The allowed values are: 0: Cache disabled 1: Cache enabled

4.1.3 MSS Watchdog Timer Control Register

Note: The reset state of a bit depends on the resource that is enabled or disabled. See the user design <root>_init_config.xml file to view the reset value for these bits.

Table 4 • **WDOG_CR**

Bit Number	Name	Description
[31:2]	Reserved	Reserved
1	WDOGMODE	This bit is the reset/interrupt mode selection bit from the system register. This value can be read from the WDOGCONTROL register within the WatchDog module.
0	WDOGENABLE	This is the enable bit for the Watchdog module. The status of this bit can be monitored in the WDOGENABLE register within the WatchDog module.

4.2 HPMS SYSREG Configuration Registers

The following is a list of SYSREG configuration registers to be used to hold HPMS blocks in reset for safety-critical avionics applications. For a complete list of all HPMS system registers, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide.*

4.2.1 HPMS Software Reset Control Register

Note: The reset state of a bit depends on the resource that is enabled or disabled. See the user design <root>_init_config.xml file to view the reset value for these bits.

Table 5 • **HPMS Software Reset Control Register**

Bit Number	Name	Description
(31:27]	Reserved	
26	MDDR_DDRFIC_SOFTRESET	'0: Releases DDR_FIC controller from reset 1: Keeps DDR_FIC controller in reset.
25	MDDR_CTLR_SOFTRESET	0: Releases MDDR controller from reset 1: Keeps MMDR controller in reset.
(24:20]*	Reserved	
19	FIC_1_SOFTRESET	0: Releases FIC _1 from reset 1: Keeps FIC_1 in reset
18	FIC_O_SOFTRESET	0: Releases FIC _0 from reset 1: Keeps FIC _O in reset
17	HPDMA_SOFTRESET	0: Releases HPDMA from reset 1: Keeps HPDMA n reset
16	FPGA_SOFTRESET	0: Releases FPGA from reset (MSS_M2F_RESET_N) 1: Keeps FPGA in reset (MSS_M2F_RESET_N)
15	COMBLK_SOFTRESET	0: Releases COMM_BLK from reset 1: Keeps COMMUNICATION BLOCK (COMM_BLK) in reset
(14:10]*	Reserved	
9	SPI_SOFTRESET	0: Releases SPI from reset 1: Keeps SPI in reset
(8:6]*	Reserved	
5	PDMA_SOFTRESET	0: Releases the PDMA from reset 1: Keeps the PDMA in reset
4*	Reserved	
3	ESRAM1_SOFTRESET	0: Releases the eSRAM_1 memory controller from reset 1: Keeps the eSRAM_1 memory controller in reset
2	ESRAMO_SOFTRESET	0: Releases the eSRAM_0 memory controller from reset. 1: Keeps the eSRAM_0 memory controller in reset.
1	ENVM1_SOFTRESET	0: Releases the eNVM_1memory controller from reset 1: Keeps the eNVM_1 memory controller in reset
0	ENVMO_SOFTRESET	0: Releases the eNVM_0 memory controller from reset. 1: Keeps the eNVM_O memory controller in reset

Note: **:* The IP blocks associated with these bits are unavailable in IGLOO2 devices. Libero SoC software forces all these bits = 1 to keep the IP blocks in reset. For safety critical applications, it is recommended to set the lock bit associated with these bits.

4.3 FDDR SYSREG Configuration Registers

The following table lists the FDDR SYSREG Configuration Registers. These registers are located in the FDDR IP block. See *UG0446 SmartFusion2 and IGLOO2 High Speed DDR Interfaces* for more information about each bit of these registers.

Table 6 • **FDDR SYSREG**

Register Name	Address Offset	Register Type	Flash	Reset Source	Description
PLL_CONFIG_LOW_1	0x500	RW	P	PRESETN	Comes from SYSREG. Controls the corresponding configuration input of the FPLL.
PLL_CONFIG_LOW_2	0x504	RW	P	PRESETN	Comes from SYSREG. Controls the corresponding configuration input of the FPLL.
PLL_CONFIG_HIGH	0x508	RW	P	PRESETN	Comes from SYSREG. Controls the corresponding configuration input of the FPLL.
FDDR_FACC_CLK_EN	Ox50C	RW	P	PRESETN	Enables the clock to the DDR memory controller.
FDDR_FACC_MUX_CONFIG	0x510	RW	P	PRESETN	Selects the standby glitch-free multiplexers within the fabric alignment clock controller (FACC).
FDDR_FACC_DIVISOR_RATIO	0x514	RW	P	PRESETN	Selects the ratio between CLK_A and CLK_DDR_FIC.
PLL_DELAY_LINE_SEL	Ox518	RW	P	PRESETN	Selects the delay values to be added to the FPLL.
FDDR_SOFT_RESET	0x51 C	RW	P	PRESETN	Soft reset register for FDDR
FDDR_IO_CALIB	0x520	RW	P	PRESETN	Configurations register for DDRIO calibration block
FDDR_INTERRUPT_ENABLE	0x524	RW	P	PRESETN	Interrupt enable register
F_AXI_AHB_MODE_SEL	0x528	RW	P	PRESETN	Selects AXI/AHB interface in the fabric.
PHY_SELF_REF_EN	0x52C	RW	P	PRESETN	Automatic calibration lock is enabled.
FDDR_FAB_PLL_CLK_SR	0x530	RO	-	PRESETN	Indicates the lock status of the fabric_ PLL.
FDDR_FPLL_CLK_SR	0x534	RO	-	PRESETN	Indicates the lock status of the fabric PLL.
FDDR_INTERRUPT_SR	Ox53C	RO	-	PRESETN	Interrupt status register
FDDR_IO_CALIB_SR	0x544	RO	-	PRESETN	I/O calibration status register
FDDR_FATC_RESET	0x548	RW	P	PRESETN	Reset to fabric portion of the fabric alignment test circuit

4.4 MDDR SYSREG Configuration Registers

The following table lists the MDDR SYSREG Configuration Registers. These registers are located in the MSS/HPMS IP blocks. See *UG0331: SmartFusion2 Microcontroller Subsystem User Guide* or *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide* for more information about each bit of these registers.

Table 7 • **SYSREG Configuration Register Summary**

Register Name	Register Type	Flash Write Protect	Reset Source	Description
MDDR_CR	RW-P	Register	PORESET_N	MDDR Configuration register
MDDR JO_CALIB_CR	RW-P	Register	PORESET_N	MDDR I/O Calibration Control register
HPMSDDR_PLL_STATUS_LOW_CR	RW-P	Register	CC_RESET_N	Used to control the corresponding configuration input of the MPLL
HPMSDDR_PLL_STATUS_HIGH_CR	RW-P	Register	CC_RESET_N	Used to control the corresponding configuration input of the MPLL register
HPMSDDR_FACC1_CR	RW-P	Field	CC_RESET_N	HPMS DDR Fabric Alignment Clock Controller 1 Configuration register
HPMSDDR_FACC2_CR	RW-P	Field	CC_RESET_N	HPMS DDR Fabric Alignment Clock Controller 2 Configuration register
HPMSDDR_CLK_CALIB_STATUS	RW-P	Register	SYSRESET_N	Used to start an FPGA fabric calibration test circuit
DDRB_CR	RW-P	Register	SYSRESET_N	HPMS DDR bridge configuration register
HPMSDDR_PLL_STATUS	RO	-	-	HPMS DDR PLL Status register
MDDR_IO_CALIB_STATUS	RO	-	PORESET_N	DDR I/O Calibration Status register
HPMSDDR_CLK_CALIB_STATUS	RO	-	SYSRESET_N	HPMS DDR Clock Calibration register
SOFT_RESET_CR	RW-P	Bit	SYSRESET_N	Soft reset control register

4.5 SerDes SYSREG Configuration Registers

The following table lists the SerDes SYSREG Configuration Registers. These registers are located in the SerDes IP block. See *UG0447 SmartFusion2 and IGLOO2 High-Speed Serial Interfaces User Guide* for more information about each bit of these registers.

Table 8 • **SERDESIF System Registers**

Register Name	Address Offset	Register Type	Description
SYSTEM_SER_PLL_CONFIG_LOW	0x00	R/W	Sets SERDES PLL(SPLL) configuration bits (LSBs)
SYSTEM_SER_PLL_CONFIG_HIGH	0x04	R/W	Sets SPLL configuration bits (MSBs)
SYSTEM_SERDESIF_SOFT_RESET	0x08	R/W	PCIe controller, XAUI, and SERDES lanes soft RESET
SYSTEM_SER_INTERRUPT_ENABLE	0x0C	R/W	SPLL lock interrupt enable
SYSTEM_CONFIG(CONFIG2)_AXI_AHBRIDGE	0X10	R/W	Defines whether AXI3/AHB master interface is implemented on the master interface to fabric
SYSTEM_CONFIG(CONFIG2)_ECC_INTR_ENABLE 0x14	0X14	R/W	Sets ECC enable and ECC interrupt enable for PCIe memories
Reserved	0x18	R/W	Reserved
Reserved	0x1C	R/W	Reserved
SYSTEM_CONFIG(CONFIG2)_PCIE_PM	0x20	R/W	Used to inform the configuration space, the slot power, PHY reference clock, and Power mode.
SYSTEM_CONFIG_PHY_MODE_0	0x24	R/W	Selects the protocol default settings of the PHY
SYSTEM_CONFIG_PHY_MODE_1	0x 28	R/W	Selects PCS mode, link to lane settings.
SYSTEM_CONFIG_PHY_MODE_2	0x2C	R/W	Sets the equalization calibration performed by the PMA control logic of the lane or use the calibration result of adjacent lane.
SYSTEM_CONFIG(CONFIG2)_PCIE_0	0x30	R/W	Defines PCIe vendor ID and device ID for PCIe identification registers.
SYSTEM_CONFIG(CONFIG2)_PCIE_1	0x34	R/W	Defines PCIe subsystem vendor ID and subsystem device ID for PCIe identification registers.
SYSTEM_CONFIG(CONFIG2)_PCIE_2	0x38	R/W	Defines PCIe subsystem revision ID and class code
SYSTEM_CONFIG(CONFIG2)_PCIE_3	0x3C	R/W	Sets PCIe link speed
SYSTEM_CONFIG(CONFIG2)_BAR_SIZE_0_1	0x40	R/W	Sets BARO and BAR1 of PCIe core register map
SYSTEM CONFIG(CONFIG2)_BAR_SIZ E_ 2_ 3	0x44	R/W	Sets BAR2 and BAR3 of PCIe core register map
SYSTEM_CONFIG(CONFIG2)_BAR_SIZ E_4_5	0x48	R/W	Sets BAR4 and BARS of PCIe core register map
SYSTEM_SER_CLK_STATUS	0x4C	R/O	This register describes SPLL lock information.

Table 8 • **SERDESIF System Registers *(continued)***

Register Name	Address Offset	Register Type	Description
Reserved	0x50	R/O	-
Reserved	0x54	R/O	-
SYSTEM _ SER_ INTERRUPT	0x58	R/O	SPLL/FPLL lock interrupt
SYSTEM_SERDESIF(SERDESIF2)_INTR_STATUS	0x5C	R/O	SECDED interrupt status for PCIe memories
Reserved	0x60	-	-
SYSTEM_REFCLK_SEL	0x64	R/W	Reference clock selection for the four lanes of PMA
SYSTEM_PCLK_SEL	0x68	R/W	SERDESIF clock selection
SYSTEM_EPCS_RSTN_SEL	0x6C	R/W	EPCS reset signal selection from fabric
SYSTEM_CHIP_ENABLES	0x70	R/O	GEN2 enable for PCIe
SYSTEM_SERDES_TEST_OUT	0x74	R/O	Status Test out output of PCIe PHY
Reserved	0x78	R/W	Reserved
SYSTEM_RC_OSC_SPLL_REFCLK_SEL	0x7C	R/W	Reference clock selection for SPLL
SYSTEM_SPREAD_SPECTRUM_CLK	0x80	R/W	Spread spectrum clocking configuration
SYSTEM_CONF(CONF2)_AXI_MSTR_WNDW_0	0x84	R/W	PCIe AXI3-master window0 configuration register -0
SYSTEM_CONF(CONF2)_AXI_MSTR_WNDW_1	0x88	R/W	PCIe AXI3-master window0 configuration register -2
SYSTEM_CONF(CONF2)_AXI_MSTR_WNDW_2	0x8C	R/W	PCIe AXI3-master window0 configuration register -2
SYSTEM_CONF(CONF2)_AXI_MSTR_WNDW_3	0x90	R/W	PCIe AXI3-master window0 configuration register -3
SYSTEM CONF(CONF2)_AXI_SLV_WN DW_0	0x94	R/W	PCIe AXI3-slave window0 configuration register - 0
SYSTEM_CONF(CONF2)_AXI_SLV_WN DW_1	0x98	R/W	PCIe AXI3-slave window0 configuration register - 1
SYSTEM_CONF(CONF2)_AXI_SLV_WNDW_2	0X9C	R/W	PCIe AXI3-slave window0 configuration register - 2
SYSTEM_CONF(CONF2)_AXI_SLV_WNDW_3	0AX0	R/W	PCIe AXI3-slave window0 configuration register - 4
SYSTEM_DESKEW_CONFIG	0xA4	R/W	PLL REF clock DESKEW register
SYSTEM_ DEBUG_MODE_KEY	0xA8	R/W	Enables/Disables APB bus to monitor PCIE test pins
SYSTEM_ADVCONFIG(ADVCONFIG2)	0xB4	R/W	-
SYSTEM_ ADVSTATUS(ADVSTATUS2)	0xB8	R/0	Indicates the reset phase of the PCIE controller
SYSTEM_ ENHANCEMENT	0xC8	R/W	M2S/M2GL060 and M2S/M2GL090 devices only

5 Appendix: Configuration of Unused IP Blocks

The following table lists the unused configuration of IP blocks in SmartFusion2and IGLOO2 devices. Configuration Report for MSS, SERDES (s), Fabric DDR, and Fabric CCC (s).

Table 9 • **CCC-NE0 (Unused)**

Register	Field	INIT	Value
FCCC_RFDIV_CR	RFDIV[7:0]	INIT[7:0]	8'h0
FCCC_FBDIV_CR0	FBDIV[7:0]	INIT[15:8]	8'h0
FCCC_FBDIV_CR1	FBDIV[13:8]	INIT[21:16]	6'h0
FCCC_GPD0_CR	GPDIV[7:0]	INIT[29:22]	8'h0
FCCC_GPD1_CR	GPDIV[7:0]	INIT[37:30]	8'h0
FCCC_GPD2_CR	GPDIV[7:0]	INIT[45:38]	8'h0
FCCC_GPD3_CR	GPDIV[7:0]	INIT[53:46]	8'h0
FCCC_RFMUX_CR	SELRF[3:0]	INIT[57:54]	4'h0
FCCC_FBMUX_CR	SELFB[3:0]	INIT[61:58]	4'h0
FCCC_GPMUX0_CR	SEL_GPMUX0[4:0]	INIT[66:62]	5'h0
FCCC_GPMUX1_CR	SEL_GPMUX1[4:0]	INIT[71:67]	5'h0
FCCC_GPMUX2_CR	SEL_GPMUX2[4:0]	INIT[76:72]	5'h0
FCCC_GPMUX3_CR	SEL_GPMUX3[4:0]	INIT[81:77]	5'h0
FCCC_NGMUX0_CR0	SELGL[4:0]	INIT[86:82]	5'h0
FCCC_NGMUX0_CR1	SELGL[9:5]	INIT[91:87]	5'h0
FCCC_NGMUX1_CR0	SELGL[14:10]	INIT[96:92]	5'h0
FCCC_NGMUX1_CR1	SELGL[19:15]	INIT[101:97]	5'h0
FCCC_NGMUX2_CR0	SELGL[24:20]	INIT[106:102]	5'h0
FCCC_NGMUX2_CR1	SELGL[29:25]	INIT[111:107]	5'h0
FCCC_NGMUX3_CR0	SELGL[34:30]	INIT[116:112]	5'h0
FCCC_NGMUX3_CR1	SELGL[39:35]	INIT[121:117]	5'h0
FCCC_GPD0_SYNC_CR	RESET_GENEN[0]	INIT[122:122]	1'h0
FCCC_GPD1_SYNC_CR	RESET_GENEN[1]	INIT[123:123]	1'h0
FCCC_GPD2_SYNC_CR	RESET_GENEN[2]	INIT[124:124]	1'h0
FCCC_GPD3_SYNC_CR	RESET_GENEN[3]	INIT[125:125]	1'h0
FCCC_RFMUX_CR	INVRF[3:0]	INIT[131:126]	6'h0
FCCC_PDLY_CR	SEL_PLL_DLINE[5:0]	INIT[137:132]	6'h0
FCCC_PDLY_CR	RF_DLINE	INIT[138:138]	1'h0
FCCC_PLL_CR0	LOCKWIN[2:0]	INIT[141:139]	3'h0
FCCC_PLL_CR1	LOCKCNT[3:0]	INIT[145:142]	4'h0
FCCC_PLL_CR7	DIVQ[2:0]	INIT[148:146]	3'h0
FCCC_PLL_CR5	MODE32K	INIT[149:149]	1'h0

Table 9 • **CCC-NE0 (Unused)** ***(continued)***

Register	Field	INIT	Value
FCCC_PLL_CR5	MODE_1V2	INIT[150:150]	1'h0
FCCC_PLL_CR5	MODE_3V3	INIT[151:151]	1'h0
FCCC_PLL_CR6	FSE	INIT[152:152]	1'h0
FCCC_PLL_CR4	SSE	INIT[153:153]	1'h0
FCCC_PLL_CR3	SSMD[1:0]	INIT[155:154]	2'h0
FCCC_PLL_CR2	SSMF[4:0]	INIT[160:156]	5'h0
FCCC_PLL_CR8	DIVR[5:0]	INIT[166:161]	6'h0
FCCC_PLL_CR9	DIVF[5:0]	INIT[174:167]	8'h0
FCCC_PLL_CR10	RANGE	INIT[178:175]	4'h0
FCCC_GPMUX0_CR	NOPIPE_SYNCRST0	INIT[179:179]	1'h0
FCCC_GPMUX1_CR	NOPIPE_SYNCRST1	INIT[180:180]	1'h0
FCCC_GPMUX2_CR	NOPIPE_SYNCRST2	INIT[181:181]	1'h0
FCCC_GPMUX3_CR	NOPIPE_SYNCRST3	INIT[182:182]	1'h0
FCCC_GPD0_SYNC_CR	SRESET_GENEN[0]	INIT[183:183]	1'h0
FCCC_GPD1_SYNC_CR	SRESET_GENEN[1]	INIT[184:184]	1'h0
FCCC_GPD2_SYNC_CR	SRESET_GENEN[2]	INIT[185:185]	1'h0
FCCC_GPD3_SYNC_CR	SRESET_GENEN[3]	INIT[186:186]	1'h0
FCCC_GPDS_SYNC_CR	SW_RESYNC_GPD	INIT[187:187]	1'h0
FCCC_GPMUX0_CR	INV_GPMUX0	INIT[188:188]	1'h0
FCCC_GPMUX1_CR	INV_GPMUX1	INIT[189:189]	1'h0
FCCC_GPMUX2_CR	INV_GPMUX2	INIT[190:190]	1'h0
FCCC_GPMUX3_CR	INV_GPMUX3	INIT[191:191]	1'h0
RESERVED_0	RESERVED[0]	INIT[192:192]	1'h0
RESERVED_0	RESERVED[1]	INIT[193:193]	1'h0
FCCC_GPD0_SYNC_CR	GPD_MODE_N[0]	INIT[194:194]	1'h0
FCCC_GPD1_SYNC_CR	GPD_MODE_N[1]	INIT[195:195]	1'h0
FCCC_GPD2_SYNC_CR	GPD_MODE_N[2]	INIT[196:196]	1'h0
FCCC_GPD3_SYNC_CR	GPD_MODE_N[3]	INIT[197:197]	1'h0
FCCC_NGMUX0_CR1	SELOUT_0	INIT[198:198]	1'h0
FCCC_NGMUX1_CR1	SELOUT_1	INIT[199:199]	1'h0
FCCC_NGMUX2_CR1	SELOUT_2	INIT[200:200]	1'h0
FCCC_NGMUX3_CR1	SELOUT_3	INIT[201:201]	1'h0
RESERVED_1	RESERVED[7:0]	INIT[209:202]	8'h0

Table 10 • **CCC-NE1 (Unused)**

Register	Field	INIT	Value
FCCC_RFDIV_CR	RFDIV[7:0]	INIT[7:0]	8'h0
FCCC_FBDIV_CR0	FBDIV[7:0]	INIT[15:8]	8'h0
FCCC_FBDIV_CR1	FBDIV[13:8]	INIT[21:16]	6'h0
FCCC_GPD0_CR	GPDIV[7:0]	INIT[29:22]	8'h0
FCCC_GPD1_CR	GPDIV[7:0]	INIT[37:30]	8'h0
FCCC_GPD2_CR	GPDIV[7:0]	INIT[45:38]	8'h0
FCCC_GPD3_CR	GPDIV[7:0]	INIT[53:46]	8'h0
FCCC_RFMUX_CR	SELRF[3:0]	INIT[57:54]	4'h0
FCCC_FBMUX_CR	SELFB[3:0]	INIT[61:58]	4'h0
FCCC_GPMUX0_CR	SEL_GPMUX0[4:0]	INIT[66:62]	5'h0
FCCC_GPMUX1_CR	SEL_GPMUX1[4:0]	INIT[71:67]	5'h0
FCCC_GPMUX2_CR	SEL_GPMUX2[4:0]	INIT[76:72]	5'h0
FCCC_GPMUX3_CR	SEL_GPMUX3[4:0]	INIT[81:77]	5'h0
FCCC_NGMUX0_CR0	SELGL[4:0]	INIT[86:82]	5'h0
FCCC_NGMUX0_CR1	SELGL[9:5]	INIT[91:87]	5'h0
FCCC_NGMUX1_CR0	SELGL[14:10]	INIT[96:92]	5'h0
FCCC_NGMUX1_CR1	SELGL[19:15]	INIT[101:97]	5'h0
FCCC_NGMUX2_CR0	SELGL[24:20]	INIT[106:102]	5'h0
FCCC_NGMUX2_CR1	SELGL[29:25]	INIT[111:107]	5'h0
FCCC_NGMUX3_CR0	SELGL[34:30]	INIT[116:112]	5'h0
FCCC_NGMUX3_CR1	SELGL[39:35]	INIT[121:117]	5'h0
FCCC_GPD0_SYNC_CR	RESET_GENEN[0]	INIT[122:122]	1'h0
FCCC_GPD1_SYNC_CR	RESET_GENEN[1]	INIT[123:123]	1'h0
FCCC_GPD2_SYNC_CR	RESET_GENEN[2]	INIT[124:124]	1'h0
FCCC_GPD3_SYNC_CR	RESET_GENEN[3]	INIT[125:125]	1'h0
FCCC_RFMUX_CR	INVRF[3:0]	INIT[131:126]	6'h0
FCCC_PDLY_CR	SEL_PLL_DLINE[5:0]	INIT[137:132]	6'h0
FCCC_PDLY_CR	RF_DLINE	INIT[138:138]	1'h0
FCCC_PLL_CR0	LOCKWIN[2:0]	INIT[141:139]	3'h0
FCCC_PLL_CR1	LOCKCNT[3:0]	INIT[145:142]	4'h0
FCCC_PLL_CR7	DIVQ[2:0]	INIT[148:146]	3'h0
FCCC_PLL_CR5	MODE32K	INIT[149:149]	1'h0
FCCC_PLL_CR5	MODE_1V2	INIT[150:150]	1'h0
FCCC_PLL_CR5	MODE_3V3	INIT[151:151]	1'h0
FCCC_PLL_CR6	FSE	INIT[152:152]	1'h0
FCCC_PLL_CR4	SSE	INIT[153:153]	1'h0
FCCC_PLL_CR3	SSMD[1:0]	INIT[155:154]	2'h0

Table 10 • **CCC-NE1 (Unused)** ***(continued)***

Register	Field	INIT	Value
FCCC_PLL_CR2	SSMF[4:0]	INIT[160:156]	5'h0
FCCC_PLL_CR8	DIVR[5:0]	INIT[166:161]	6'h0
FCCC_PLL_CR9	DIVF[5:0]	INIT[174:167]	8'h0
FCCC_PLL_CR10	RANGE	INIT[178:175]	4'h0
FCCC_GPMUX0_CR	NOPIPE_SYNCRST0	INIT[179:179]	1'h0
FCCC_GPMUX1_CR	NOPIPE_SYNCRST1	INIT[180:180]	1'h0
FCCC_GPMUX2_CR	NOPIPE_SYNCRST2	INIT[181:181]	1'h0
FCCC_GPMUX3_CR	NOPIPE_SYNCRST3	INIT[182:182]	1'h0
FCCC_GPD0_SYNC_CR	SRESET_GENEN[0]	INIT[183:183]	1'h0
FCCC_GPD1_SYNC_CR	SRESET_GENEN[1]	INIT[184:184]	1'h0
FCCC_GPD2_SYNC_CR	SRESET_GENEN[2]	INIT[185:185]	1'h0
FCCC_GPD3_SYNC_CR	SRESET_GENEN[3]	INIT[186:186]	1'h0
FCCC_GPDS_SYNC_CR	SW_RESYNC_GPD	INIT[187:187]	1'h0
FCCC_GPMUX0_CR	INV_GPMUX0	INIT[188:188]	1'h0
FCCC_GPMUX1_CR	INV_GPMUX1	INIT[189:189]	1'h0
FCCC_GPMUX2_CR	INV_GPMUX2	INIT[190:190]	1'h0
FCCC_GPMUX3_CR	INV_GPMUX3	INIT[191:191]	1'h0
RESERVED_0	RESERVED[0]	INIT[192:192]	1'h0
RESERVED_0	RESERVED[1]	INIT[193:193]	1'h0
FCCC_GPD0_SYNC_CR	GPD_MODE_N[0]	INIT[194:194]	1'h0
FCCC_GPD1_SYNC_CR	GPD_MODE_N[1]	INIT[195:195]	1'h0
FCCC_GPD2_SYNC_CR	GPD_MODE_N[2]	INIT[196:196]	1'h0
FCCC_GPD3_SYNC_CR	GPD_MODE_N[3]	INIT[197:197]	1'h0
FCCC_NGMUX0_CR1	SELOUT_0	INIT[198:198]	1'h0
FCCC_NGMUX1_CR1	SELOUT_1	INIT[199:199]	1'h0
FCCC_NGMUX2_CR1	SELOUT_2	INIT[200:200]	1'h0
FCCC_NGMUX3_CR1	SELOUT_3	INIT[201:201]	1'h0
RESERVED_1	RESERVED[7:0]	INIT[209:202]	8'h0

Table 11 • **CCC-NW0 (Unused)**

Register	Field	INIT	Value
FCCC_RFDIV_CR	RFDIV[7:0]	INIT[7:0]	8'h0
FCCC_FBDIV_CR0	FBDIV[7:0]	INIT[15:8]	8'h0
FCCC_FBDIV_CR1	FBDIV[13:8]	INIT[21:16]	6'h0
FCCC_GPD0_CR	GPDIV[7:0]	INIT[29:22]	8'h0
FCCC_GPD1_CR	GPDIV[7:0]	INIT[37:30]	8'h0
FCCC_GPD2_CR	GPDIV[7:0]	INIT[45:38]	8'h0
FCCC_GPD3_CR	GPDIV[7:0]	INIT[53:46]	8'h0
FCCC_RFMUX_CR	SELRF[3:0]	INIT[57:54]	4'h0
FCCC_FBMUX_CR	SELFB[3:0]	INIT[61:58]	4'h0
FCCC_GPMUX0_CR	SEL_GPMUX0[4:0]	INIT[66:62]	5'h0
FCCC_GPMUX1_CR	SEL_GPMUX1[4:0]	INIT[71:67]	5'h0
FCCC_GPMUX2_CR	SEL_GPMUX2[4:0]	INIT[76:72]	5'h0
FCCC_GPMUX3_CR	SEL_GPMUX3[4:0]	INIT[81:77]	5'h0
FCCC_NGMUX0_CR0	SELGL[4:0]	INIT[86:82]	5'h0
FCCC_NGMUX0_CR1	SELGL[9:5]	INIT[91:87]	5'h0
FCCC_NGMUX1_CR0	SELGL[14:10]	INIT[96:92]	5'h0
FCCC_NGMUX1_CR1	SELGL[19:15]	INIT[101:97]	5'h0
FCCC_NGMUX2_CR0	SELGL[24:20]	INIT[106:102]	5'h0
FCCC_NGMUX2_CR1	SELGL[29:25]	INIT[111:107]	5'h0
FCCC_NGMUX3_CR0	SELGL[34:30]	INIT[116:112]	5'h0
FCCC_NGMUX3_CR1	SELGL[39:35]	INIT[121:117]	5'h0
FCCC_GPD0_SYNC_CR	RESET_GENEN[0]	INIT[122:122]	1'h0
FCCC_GPD1_SYNC_CR	RESET_GENEN[1]	INIT[123:123]	1'h0
FCCC_GPD2_SYNC_CR	RESET_GENEN[2]	INIT[124:124]	1'h0
FCCC_GPD3_SYNC_CR	RESET_GENEN[3]	INIT[125:125]	1'h0
FCCC_RFMUX_CR	INVRF[3:0]	INIT[131:126]	6'h0
FCCC_PDLY_CR	SEL_PLL_DLINE[5:0]	INIT[137:132]	6'h0
FCCC_PDLY_CR	RF_DLINE	INIT[138:138]	1'h0
FCCC_PLL_CR0	LOCKWIN[2:0]	INIT[141:139]	3'h0
FCCC_PLL_CR1	LOCKCNT[3:0]	INIT[145:142]	4'h0
FCCC_PLL_CR7	DIVQ[2:0]	INIT[148:146]	3'h0
FCCC_PLL_CR5	MODE32K	INIT[149:149]	1'h0
FCCC_PLL_CR5	MODE_1V2	INIT[150:150]	1'h0
FCCC_PLL_CR5	MODE_3V3	INIT[151:151]	1'h0
FCCC_PLL_CR6	FSE	INIT[152:152]	1'h0
FCCC_PLL_CR4	SSE	INIT[153:153]	1'h0
FCCC_PLL_CR3	SSMD[1:0]	INIT[155:154]	2'h0

Table 11 • **CCC-NW0 (Unused)** ***(continued)***

Register	Field	INIT	Value
FCCC_PLL_CR2	SSMF[4:0]	INIT[160:156]	5'h0
FCCC_PLL_CR8	DIVR[5:0]	INIT[166:161]	6'h0
FCCC_PLL_CR9	DIVF[5:0]	INIT[174:167]	8'h0
FCCC_PLL_CR10	RANGE	INIT[178:175]	4'h0
FCCC_GPMUX0_CR	NOPIPE_SYNCRST0	INIT[179:179]	1'h0
FCCC_GPMUX1_CR	NOPIPE_SYNCRST1	INIT[180:180]	1'h0
FCCC_GPMUX2_CR	NOPIPE_SYNCRST2	INIT[181:181]	1'h0
FCCC_GPMUX3_CR	NOPIPE_SYNCRST3	INIT[182:182]	1'h0
FCCC_GPD0_SYNC_CR	SRESET_GENEN[0]	INIT[183:183]	1'h0
FCCC_GPD1_SYNC_CR	SRESET_GENEN[1]	INIT[184:184]	1'h0
FCCC_GPD2_SYNC_CR	SRESET_GENEN[2]	INIT[185:185]	1'h0
FCCC_GPD3_SYNC_CR	SRESET_GENEN[3]	INIT[186:186]	1'h0
FCCC_GPDS_SYNC_CR	SW_RESYNC_GPD	INIT[187:187]	1'h0
FCCC_GPMUX0_CR	INV_GPMUX0	INIT[188:188]	1'h0
FCCC_GPMUX1_CR	INV_GPMUX1	INIT[189:189]	1'h0
FCCC_GPMUX2_CR	INV_GPMUX2	INIT[190:190]	1'h0
FCCC_GPMUX3_CR	INV_GPMUX3	INIT[191:191]	1'h0
RESERVED_0	RESERVED[0]	INIT[192:192]	1'h0
RESERVED_0	RESERVED[1]	INIT[193:193]	1'h0
FCCC_GPD0_SYNC_CR	GPD_MODE_N[0]	INIT[194:194]	1'h0
FCCC_GPD1_SYNC_CR	GPD_MODE_N[1]	INIT[195:195]	1'h0
FCCC_GPD2_SYNC_CR	GPD_MODE_N[2]	INIT[196:196]	1'h0
FCCC_GPD3_SYNC_CR	GPD_MODE_N[3]	INIT[197:197]	1'h0
FCCC_NGMUX0_CR1	SELOUT_0	INIT[198:198]	1'h0
FCCC_NGMUX1_CR1	SELOUT_1	INIT[199:199]	1'h0
FCCC_NGMUX2_CR1	SELOUT_2	INIT[200:200]	1'h0
FCCC_NGMUX3_CR1	SELOUT_3	INIT[201:201]	1'h0
RESERVED_1	RESERVED[7:0]	INIT[209:202]	8'h0

Table 12 • **CCC-NW1 (Unused)**

Register	Field	INIT	Value
FCCC_RFDIV_CR	RFDIV[7:0]	INIT[7:0]	8'h0
FCCC_FBDIV_CR0	FBDIV[7:0]	INIT[15:8]	8'h0
FCCC_FBDIV_CR1	FBDIV[13:8]	INIT[21:16]	6'h0
FCCC_GPD0_CR	GPDIV[7:0]	INIT[29:22]	8'h0
FCCC_GPD1_CR	GPDIV[7:0]	INIT[37:30]	8'h0
FCCC_GPD2_CR	GPDIV[7:0]	INIT[45:38]	8'h0
FCCC_GPD3_CR	GPDIV[7:0]	INIT[53:46]	8'h0
FCCC_RFMUX_CR	SELRF[3:0]	INIT[57:54]	4'h0
FCCC_FBMUX_CR	SELFB[3:0]	INIT[61:58]	4'h0
FCCC_GPMUX0_CR	SEL_GPMUX0[4:0]	INIT[66:62]	5'h0
FCCC_GPMUX1_CR	SEL_GPMUX1[4:0]	INIT[71:67]	5'h0
FCCC_GPMUX2_CR	SEL_GPMUX2[4:0]	INIT[76:72]	5'h0
FCCC_GPMUX3_CR	SEL_GPMUX3[4:0]	INIT[81:77]	5'h0
FCCC_NGMUX0_CR0	SELGL[4:0]	INIT[86:82]	5'h0
FCCC_NGMUX0_CR1	SELGL[9:5]	INIT[91:87]	5'h0
FCCC_NGMUX1_CR0	SELGL[14:10]	INIT[96:92]	5'h0
FCCC_NGMUX1_CR1	SELGL[19:15]	INIT[101:97]	5'h0
FCCC_NGMUX2_CR0	SELGL[24:20]	INIT[106:102]	5'h0
FCCC_NGMUX2_CR1	SELGL[29:25]	INIT[111:107]	5'h0
FCCC_NGMUX3_CR0	SELGL[34:30]	INIT[116:112]	5'h0
FCCC_NGMUX3_CR1	SELGL[39:35]	INIT[121:117]	5'h0
FCCC_GPD0_SYNC_CR	RESET_GENEN[0]	INIT[122:122]	1'h0
FCCC_GPD1_SYNC_CR	RESET_GENEN[1]	INIT[123:123]	1'h0
FCCC_GPD2_SYNC_CR	RESET_GENEN[2]	INIT[124:124]	1'h0
FCCC_GPD3_SYNC_CR	RESET_GENEN[3]	INIT[125:125]	1'h0
FCCC_RFMUX_CR	INVRF[3:0]	INIT[131:126]	6'h0
FCCC_PDLY_CR	SEL_PLL_DLINE[5:0]	INIT[137:132]	6'h0
FCCC_PDLY_CR	RF_DLINE	INIT[138:138]	1'h0
FCCC_PLL_CR0	LOCKWIN[2:0]	INIT[141:139]	3'h0
FCCC_PLL_CR1	LOCKCNT[3:0]	INIT[145:142]	4'h0
FCCC_PLL_CR7	DIVQ[2:0]	INIT[148:146]	3'h0
FCCC_PLL_CR5	MODE32K	INIT[149:149]	1'h0
FCCC_PLL_CR5	MODE_1V2	INIT[150:150]	1'h0
FCCC_PLL_CR5	MODE_3V3	INIT[151:151]	1'h0
FCCC_PLL_CR6	FSE	INIT[152:152]	1'h0
FCCC_PLL_CR4	SSE	INIT[153:153]	1'h0
FCCC_PLL_CR3	SSMD[1:0]	INIT[155:154]	2'h0

Table 12 • **CCC-NW1 (Unused)** ***(continued)***

Register	Field	INIT	Value
FCCC_PLL_CR2	SSMF[4:0]	INIT[160:156]	5'h0
FCCC_PLL_CR8	DIVR[5:0]	INIT[166:161]	6'h0
FCCC_PLL_CR9	DIVF[5:0]	INIT[174:167]	8'h0
FCCC_PLL_CR10	RANGE	INIT[178:175]	4'h0
FCCC_GPMUX0_CR	NOPIPE_SYNCRST0	INIT[179:179]	1'h0
FCCC_GPMUX1_CR	NOPIPE_SYNCRST1	INIT[180:180]	1'h0
FCCC_GPMUX2_CR	NOPIPE_SYNCRST2	INIT[181:181]	1'h0
FCCC_GPMUX3_CR	NOPIPE_SYNCRST3	INIT[182:182]	1'h0
FCCC_GPD0_SYNC_CR	SRESET_GENEN[0]	INIT[183:183]	1'h0
FCCC_GPD1_SYNC_CR	SRESET_GENEN[1]	INIT[184:184]	1'h0
FCCC_GPD2_SYNC_CR	SRESET_GENEN[2]	INIT[185:185]	1'h0
FCCC_GPD3_SYNC_CR	SRESET_GENEN[3]	INIT[186:186]	1'h0
FCCC_GPDS_SYNC_CR	SW_RESYNC_GPD	INIT[187:187]	1'h0
FCCC_GPMUX0_CR	INV_GPMUX0	INIT[188:188]	1'h0
FCCC_GPMUX1_CR	INV_GPMUX1	INIT[189:189]	1'h0
FCCC_GPMUX2_CR	INV_GPMUX2	INIT[190:190]	1'h0
FCCC_GPMUX3_CR	INV_GPMUX3	INIT[191:191]	1'h0
RESERVED_0	RESERVED[0]	INIT[192:192]	1'h0
RESERVED_0	RESERVED[1]	INIT[193:193]	1'h0
FCCC_GPD0_SYNC_CR	GPD_MODE_N[0]	INIT[194:194]	1'h0
FCCC_GPD1_SYNC_CR	GPD_MODE_N[1]	INIT[195:195]	1'h0
FCCC_GPD2_SYNC_CR	GPD_MODE_N[2]	INIT[196:196]	1'h0
FCCC_GPD3_SYNC_CR	GPD_MODE_N[3]	INIT[197:197]	1'h0
FCCC_NGMUX0_CR1	SELOUT_0	INIT[198:198]	1'h0
FCCC_NGMUX1_CR1	SELOUT_1	INIT[199:199]	1'h0
FCCC_NGMUX2_CR1	SELOUT_2	INIT[200:200]	1'h0
FCCC_NGMUX3_CR1	SELOUT_3	INIT[201:201]	1'h0
RESERVED_1	RESERVED[7:0]	INIT[209:202]	8'h0

Table 13 • **CCC-SE0 (Unused)**

Register	Field	INIT	Value
FCCC_RFDIV_CR	RFDIV[7:0]	INIT[7:0]	8'h0
FCCC_FBDIV_CR0	FBDIV[7:0]	INIT[15:8]	8'h0
FCCC_FBDIV_CR1	FBDIV[13:8]	INIT[21:16]	6'h0
FCCC_GPD0_CR	GPDIV[7:0]	INIT[29:22]	8'h0
FCCC_GPD1_CR	GPDIV[7:0]	INIT[37:30]	8'h0
FCCC_GPD2_CR	GPDIV[7:0]	INIT[45:38]	8'h0
FCCC_GPD3_CR	GPDIV[7:0]	INIT[53:46]	8'h0
FCCC_RFMUX_CR	SELRF[3:0]	INIT[57:54]	4'h0
FCCC_FBMUX_CR	SELFB[3:0]	INIT[61:58]	4'h0
FCCC_GPMUX0_CR	SEL_GPMUX0[4:0]	INIT[66:62]	5'h0
FCCC_GPMUX1_CR	SEL_GPMUX1[4:0]	INIT[71:67]	5'h0
FCCC_GPMUX2_CR	SEL_GPMUX2[4:0]	INIT[76:72]	5'h0
FCCC_GPMUX3_CR	SEL_GPMUX3[4:0]	INIT[81:77]	5'h0
FCCC_NGMUX0_CR0	SELGL[4:0]	INIT[86:82]	5'h0
FCCC_NGMUX0_CR1	SELGL[9:5]	INIT[91:87]	5'h0
FCCC_NGMUX1_CR0	SELGL[14:10]	INIT[96:92]	5'h0
FCCC_NGMUX1_CR1	SELGL[19:15]	INIT[101:97]	5'h0
FCCC_NGMUX2_CR0	SELGL[24:20]	INIT[106:102]	5'h0
FCCC_NGMUX2_CR1	SELGL[29:25]	INIT[111:107]	5'h0
FCCC_NGMUX3_CR0	SELGL[34:30]	INIT[116:112]	5'h0
FCCC_NGMUX3_CR1	SELGL[39:35]	INIT[121:117]	5'h0
FCCC_GPD0_SYNC_CR	RESET_GENEN[0]	INIT[122:122]	1'h0
FCCC_GPD1_SYNC_CR	RESET_GENEN[1]	INIT[123:123]	1'h0
FCCC_GPD2_SYNC_CR	RESET_GENEN[2]	INIT[124:124]	1'h0
FCCC_GPD3_SYNC_CR	RESET_GENEN[3]	INIT[125:125]	1'h0
FCCC_RFMUX_CR	INVRF[3:0]	INIT[131:126]	6'h0
FCCC_PDLY_CR	SEL_PLL_DLINE[5:0]	INIT[137:132]	6'h0
FCCC_PDLY_CR	RF_DLINE	INIT[138:138]	1'h0
FCCC_PLL_CR0	LOCKWIN[2:0]	INIT[141:139]	3'h0
FCCC_PLL_CR1	LOCKCNT[3:0]	INIT[145:142]	4'h0
FCCC_PLL_CR7	DIVQ[2:0]	INIT[148:146]	3'h0
FCCC_PLL_CR5	MODE32K	INIT[149:149]	1'h0
FCCC_PLL_CR5	MODE_1V2	INIT[150:150]	1'h0
FCCC_PLL_CR5	MODE_3V3	INIT[151:151]	1'h0
FCCC_PLL_CR6	FSE	INIT[152:152]	1'h0
FCCC_PLL_CR4	SSE	INIT[153:153]	1'h0
FCCC_PLL_CR3	SSMD[1:0]	INIT[155:154]	2'h0

Table 13 • **CCC-SE0 (Unused)** ***(continued)***

Register	Field	INIT	Value
FCCC_PLL_CR2	SSMF[4:0]	INIT[160:156]	5'h0
FCCC_PLL_CR8	DIVR[5:0]	INIT[166:161]	6'h0
FCCC_PLL_CR9	DIVF[5:0]	INIT[174:167]	8'h0
FCCC_PLL_CR10	RANGE	INIT[178:175]	4'h0
FCCC_GPMUX0_CR	NOPIPE_SYNCRST0	INIT[179:179]	1'h0
FCCC_GPMUX1_CR	NOPIPE_SYNCRST1	INIT[180:180]	1'h0
FCCC_GPMUX2_CR	NOPIPE_SYNCRST2	INIT[181:181]	1'h0
FCCC_GPMUX3_CR	NOPIPE_SYNCRST3	INIT[182:182]	1'h0
FCCC_GPD0_SYNC_CR	SRESET_GENEN[0]	INIT[183:183]	1'h0
FCCC_GPD1_SYNC_CR	SRESET_GENEN[1]	INIT[184:184]	1'h0
FCCC_GPD2_SYNC_CR	SRESET_GENEN[2]	INIT[185:185]	1'h0
FCCC_GPD3_SYNC_CR	SRESET_GENEN[3]	INIT[186:186]	1'h0
FCCC_GPDS_SYNC_CR	SW_RESYNC_GPD	INIT[187:187]	1'h0
FCCC_GPMUX0_CR	INV_GPMUX0	INIT[188:188]	1'h0
FCCC_GPMUX1_CR	INV_GPMUX1	INIT[189:189]	1'h0
FCCC_GPMUX2_CR	INV_GPMUX2	INIT[190:190]	1'h0
FCCC_GPMUX3_CR	INV_GPMUX3	INIT[191:191]	1'h0
RESERVED_0	RESERVED[0]	INIT[192:192]	1'h0
RESERVED_0	RESERVED[1]	INIT[193:193]	1'h0
FCCC_GPD0_SYNC_CR	GPD_MODE_N[0]	INIT[194:194]	1'h0
FCCC_GPD1_SYNC_CR	GPD_MODE_N[1]	INIT[195:195]	1'h0
FCCC_GPD2_SYNC_CR	GPD_MODE_N[2]	INIT[196:196]	1'h0
FCCC_GPD3_SYNC_CR	GPD_MODE_N[3]	INIT[197:197]	1'h0
FCCC_NGMUX0_CR1	SELOUT_0	INIT[198:198]	1'h0
FCCC_NGMUX1_CR1	SELOUT_1	INIT[199:199]	1'h0
FCCC_NGMUX2_CR1	SELOUT_2	INIT[200:200]	1'h0
FCCC_NGMUX3_CR1	SELOUT_3	INIT[201:201]	1'h0
RESERVED_1	RESERVED[7:0]	INIT[209:202]	8'h0

Table 14 • **CCC-SE1 (Unused)**

Register	Field	INIT	Value
FCCC_RFDIV_CR	RFDIV[7:0]	INIT[7:0]	8'h0
FCCC_FBDIV_CR0	FBDIV[7:0]	INIT[15:8]	8'h0
FCCC_FBDIV_CR1	FBDIV[13:8]	INIT[21:16]	6'h0
FCCC_GPD0_CR	GPDIV[7:0]	INIT[29:22]	8'h0
FCCC_GPD1_CR	GPDIV[7:0]	INIT[37:30]	8'h0
FCCC_GPD2_CR	GPDIV[7:0]	INIT[45:38]	8'h0
FCCC_GPD3_CR	GPDIV[7:0]	INIT[53:46]	8'h0
FCCC_RFMUX_CR	SELRF[3:0]	INIT[57:54]	4'h0
FCCC_FBMUX_CR	SELFB[3:0]	INIT[61:58]	4'h0
FCCC_GPMUX0_CR	SEL_GPMUX0[4:0]	INIT[66:62]	5'h0
FCCC_GPMUX1_CR	SEL_GPMUX1[4:0]	INIT[71:67]	5'h0
FCCC_GPMUX2_CR	SEL_GPMUX2[4:0]	INIT[76:72]	5'h0
FCCC_GPMUX3_CR	SEL_GPMUX3[4:0]	INIT[81:77]	5'h0
FCCC_NGMUX0_CR0	SELGL[4:0]	INIT[86:82]	5'h0
FCCC_NGMUX0_CR1	SELGL[9:5]	INIT[91:87]	5'h0
FCCC_NGMUX1_CR0	SELGL[14:10]	INIT[96:92]	5'h0
FCCC_NGMUX1_CR1	SELGL[19:15]	INIT[101:97]	5'h0
FCCC_NGMUX2_CR0	SELGL[24:20]	INIT[106:102]	5'h0
FCCC_NGMUX2_CR1	SELGL[29:25]	INIT[111:107]	5'h0
FCCC_NGMUX3_CR0	SELGL[34:30]	INIT[116:112]	5'h0
FCCC_NGMUX3_CR1	SELGL[39:35]	INIT[121:117]	5'h0
FCCC_GPD0_SYNC_CR	RESET_GENEN[0]	INIT[122:122]	1'h0
FCCC_GPD1_SYNC_CR	RESET_GENEN[1]	INIT[123:123]	1'h0
FCCC_GPD2_SYNC_CR	RESET_GENEN[2]	INIT[124:124]	1'h0
FCCC_GPD3_SYNC_CR	RESET_GENEN[3]	INIT[125:125]	1'h0
FCCC_RFMUX_CR	INVRF[3:0]	INIT[131:126]	6'h0
FCCC_PDLY_CR	SEL_PLL_DLINE[5:0]	INIT[137:132]	6'h0
FCCC_PDLY_CR	RF_DLINE	INIT[138:138]	1'h0
FCCC_PLL_CR0	LOCKWIN[2:0]	INIT[141:139]	3'h0
FCCC_PLL_CR1	LOCKCNT[3:0]	INIT[145:142]	4'h0
FCCC_PLL_CR7	DIVQ[2:0]	INIT[148:146]	3'h0
FCCC_PLL_CR5	MODE32K	INIT[149:149]	1'h0
FCCC_PLL_CR5	MODE_1V2	INIT[150:150]	1'h0
FCCC_PLL_CR5	MODE_3V3	INIT[151:151]	1'h0
FCCC_PLL_CR6	FSE	INIT[152:152]	1'h0
FCCC_PLL_CR4	SSE	INIT[153:153]	1'h0
FCCC_PLL_CR3	SSMD[1:0]	INIT[155:154]	2'h0

Table 14 • **CCC-SE1 (Unused)** ***(continued)***

Register	Field	INIT	Value
FCCC_PLL_CR2	SSMF[4:0]	INIT[160:156]	5'h0
FCCC_PLL_CR8	DIVR[5:0]	INIT[166:161]	6'h0
FCCC_PLL_CR9	DIVF[5:0]	INIT[174:167]	8'h0
FCCC_PLL_CR10	RANGE	INIT[178:175]	4'h0
FCCC_GPMUX0_CR	NOPIPE_SYNCRST0	INIT[179:179]	1'h0
FCCC_GPMUX1_CR	NOPIPE_SYNCRST1	INIT[180:180]	1'h0
FCCC_GPMUX2_CR	NOPIPE_SYNCRST2	INIT[181:181]	1'h0
FCCC_GPMUX3_CR	NOPIPE_SYNCRST3	INIT[182:182]	1'h0
FCCC_GPD0_SYNC_CR	SRESET_GENEN[0]	INIT[183:183]	1'h0
FCCC_GPD1_SYNC_CR	SRESET_GENEN[1]	INIT[184:184]	1'h0
FCCC_GPD2_SYNC_CR	SRESET_GENEN[2]	INIT[185:185]	1'h0
FCCC_GPD3_SYNC_CR	SRESET_GENEN[3]	INIT[186:186]	1'h0
FCCC_GPDS_SYNC_CR	SW_RESYNC_GPD	INIT[187:187]	1'h0
FCCC_GPMUX0_CR	INV_GPMUX0	INIT[188:188]	1'h0
FCCC_GPMUX1_CR	INV_GPMUX1	INIT[189:189]	1'h0
FCCC_GPMUX2_CR	INV_GPMUX2	INIT[190:190]	1'h0
FCCC_GPMUX3_CR	INV_GPMUX3	INIT[191:191]	1'h0
RESERVED_0	RESERVED[0]	INIT[192:192]	1'h0
RESERVED_0	RESERVED[1]	INIT[193:193]	1'h0
FCCC_GPD0_SYNC_CR	GPD_MODE_N[0]	INIT[194:194]	1'h0
FCCC_GPD1_SYNC_CR	GPD_MODE_N[1]	INIT[195:195]	1'h0
FCCC_GPD2_SYNC_CR	GPD_MODE_N[2]	INIT[196:196]	1'h0
FCCC_GPD3_SYNC_CR	GPD_MODE_N[3]	INIT[197:197]	1'h0
FCCC_NGMUX0_CR1	SELOUT_0	INIT[198:198]	1'h0
FCCC_NGMUX1_CR1	SELOUT_1	INIT[199:199]	1'h0
FCCC_NGMUX2_CR1	SELOUT_2	INIT[200:200]	1'h0
FCCC_NGMUX3_CR1	SELOUT_3	INIT[201:201]	1'h0
RESERVED_1	RESERVED[7:0]	INIT[209:202]	8'h0

Table 15 • **CCC-SW0 (Unused)**

Register	Field	INIT	Value
FCCC_RFDIV_CR	RFDIV[7:0]	INIT[7:0]	8'h0
FCCC_FBDIV_CR0	FBDIV[7:0]	INIT[15:8]	8'h0
FCCC_FBDIV_CR1	FBDIV[13:8]	INIT[21:16]	6'h0
FCCC_GPD0_CR	GPDIV[7:0]	INIT[29:22]	8'h0
FCCC_GPD1_CR	GPDIV[7:0]	INIT[37:30]	8'h0
FCCC_GPD2_CR	GPDIV[7:0]	INIT[45:38]	8'h0
FCCC_GPD3_CR	GPDIV[7:0]	INIT[53:46]	8'h0
FCCC_RFMUX_CR	SELRF[3:0]	INIT[57:54]	4'h0
FCCC_FBMUX_CR	SELFB[3:0]	INIT[61:58]	4'h0
FCCC_GPMUX0_CR	SEL_GPMUX0[4:0]	INIT[66:62]	5'h0
FCCC_GPMUX1_CR	SEL_GPMUX1[4:0]	INIT[71:67]	5'h0
FCCC_GPMUX2_CR	SEL_GPMUX2[4:0]	INIT[76:72]	5'h0
FCCC_GPMUX3_CR	SEL_GPMUX3[4:0]	INIT[81:77]	5'h0
FCCC_NGMUX0_CR0	SELGL[4:0]	INIT[86:82]	5'h0
FCCC_NGMUX0_CR1	SELGL[9:5]	INIT[91:87]	5'h0
FCCC_NGMUX1_CR0	SELGL[14:10]	INIT[96:92]	5'h0
FCCC_NGMUX1_CR1	SELGL[19:15]	INIT[101:97]	5'h0
FCCC_NGMUX2_CR0	SELGL[24:20]	INIT[106:102]	5'h0
FCCC_NGMUX2_CR1	SELGL[29:25]	INIT[111:107]	5'h0
FCCC_NGMUX3_CR0	SELGL[34:30]	INIT[116:112]	5'h0
FCCC_NGMUX3_CR1	SELGL[39:35]	INIT[121:117]	5'h0
FCCC_GPD0_SYNC_CR	RESET_GENEN[0]	INIT[122:122]	1'h0
FCCC_GPD1_SYNC_CR	RESET_GENEN[1]	INIT[123:123]	1'h0
FCCC_GPD2_SYNC_CR	RESET_GENEN[2]	INIT[124:124]	1'h0
FCCC_GPD3_SYNC_CR	RESET_GENEN[3]	INIT[125:125]	1'h0
FCCC_RFMUX_CR	INVRF[3:0]	INIT[131:126]	6'h0
FCCC_PDLY_CR	SEL_PLL_DLINE[5:0]	INIT[137:132]	6'h0
FCCC_PDLY_CR	RF_DLINE	INIT[138:138]	1'h0
FCCC_PLL_CR0	LOCKWIN[2:0]	INIT[141:139]	3'h0
FCCC_PLL_CR1	LOCKCNT[3:0]	INIT[145:142]	4'h0
FCCC_PLL_CR7	DIVQ[2:0]	INIT[148:146]	3'h0
FCCC_PLL_CR5	MODE32K	INIT[149:149]	1'h0
FCCC_PLL_CR5	MODE_1V2	INIT[150:150]	1'h0
FCCC_PLL_CR5	MODE_3V3	INIT[151:151]	1'h0
FCCC_PLL_CR6	FSE	INIT[152:152]	1'h0
FCCC_PLL_CR4	SSE	INIT[153:153]	1'h0
FCCC_PLL_CR3	SSMD[1:0]	INIT[155:154]	2'h0

Table 15 • **CCC-SW0 (Unused)** ***(continued)***

Register	Field	INIT	Value
FCCC_PLL_CR2	SSMF[4:0]	INIT[160:156]	5'h0
FCCC_PLL_CR8	DIVR[5:0]	INIT[166:161]	6'h0
FCCC_PLL_CR9	DIVF[5:0]	INIT[174:167]	8'h0
FCCC_PLL_CR10	RANGE	INIT[178:175]	4'h0
FCCC_GPMUX0_CR	NOPIPE_SYNCRST0	INIT[179:179]	1'h0
FCCC_GPMUX1_CR	NOPIPE_SYNCRST1	INIT[180:180]	1'h0
FCCC_GPMUX2_CR	NOPIPE_SYNCRST2	INIT[181:181]	1'h0
FCCC_GPMUX3_CR	NOPIPE_SYNCRST3	INIT[182:182]	1'h0
FCCC_GPD0_SYNC_CR	SRESET_GENEN[0]	INIT[183:183]	1'h0
FCCC_GPD1_SYNC_CR	SRESET_GENEN[1]	INIT[184:184]	1'h0
FCCC_GPD2_SYNC_CR	SRESET_GENEN[2]	INIT[185:185]	1'h0
FCCC_GPD3_SYNC_CR	SRESET_GENEN[3]	INIT[186:186]	1'h0
FCCC_GPDS_SYNC_CR	SW_RESYNC_GPD	INIT[187:187]	1'h0
FCCC_GPMUX0_CR	INV_GPMUX0	INIT[188:188]	1'h0
FCCC_GPMUX1_CR	INV_GPMUX1	INIT[189:189]	1'h0
FCCC_GPMUX2_CR	INV_GPMUX2	INIT[190:190]	1'h0
FCCC_GPMUX3_CR	INV_GPMUX3	INIT[191:191]	1'h0
RESERVED_0	RESERVED[0]	INIT[192:192]	1'h0
RESERVED_0	RESERVED[1]	INIT[193:193]	1'h0
FCCC_GPD0_SYNC_CR	GPD_MODE_N[0]	INIT[194:194]	1'h0
FCCC_GPD1_SYNC_CR	GPD_MODE_N[1]	INIT[195:195]	1'h0
FCCC_GPD2_SYNC_CR	GPD_MODE_N[2]	INIT[196:196]	1'h0
FCCC_GPD3_SYNC_CR	GPD_MODE_N[3]	INIT[197:197]	1'h0
FCCC_NGMUX0_CR1	SELOUT_0	INIT[198:198]	1'h0
FCCC_NGMUX1_CR1	SELOUT_1	INIT[199:199]	1'h0
FCCC_NGMUX2_CR1	SELOUT_2	INIT[200:200]	1'h0
FCCC_NGMUX3_CR1	SELOUT_3	INIT[201:201]	1'h0
RESERVED_1	RESERVED[7:0]	INIT[209:202]	8'h0

Table 16 • **CCC-SW1 (Unused)**

Register	Field	INIT	Value
FCCC_RFDIV_CR	RFDIV[7:0]	INIT[7:0]	8'h0
FCCC_FBDIV_CR0	FBDIV[7:0]	INIT[15:8]	8'h0
FCCC_FBDIV_CR1	FBDIV[13:8]	INIT[21:16]	6'h0
FCCC_GPD0_CR	GPDIV[7:0]	INIT[29:22]	8'h0
FCCC_GPD1_CR	GPDIV[7:0]	INIT[37:30]	8'h0
FCCC_GPD2_CR	GPDIV[7:0]	INIT[45:38]	8'h0
FCCC_GPD3_CR	GPDIV[7:0]	INIT[53:46]	8'h0
FCCC_RFMUX_CR	SELRF[3:0]	INIT[57:54]	4'h0
FCCC_FBMUX_CR	SELFB[3:0]	INIT[61:58]	4'h0
FCCC_GPMUX0_CR	SEL_GPMUX0[4:0]	INIT[66:62]	5'h0
FCCC_GPMUX1_CR	SEL_GPMUX1[4:0]	INIT[71:67]	5'h0
FCCC_GPMUX2_CR	SEL_GPMUX2[4:0]	INIT[76:72]	5'h0
FCCC_GPMUX3_CR	SEL_GPMUX3[4:0]	INIT[81:77]	5'h0
FCCC_NGMUX0_CR0	SELGL[4:0]	INIT[86:82]	5'h0
FCCC_NGMUX0_CR1	SELGL[9:5]	INIT[91:87]	5'h0
FCCC_NGMUX1_CR0	SELGL[14:10]	INIT[96:92]	5'h0
FCCC_NGMUX1_CR1	SELGL[19:15]	INIT[101:97]	5'h0
FCCC_NGMUX2_CR0	SELGL[24:20]	INIT[106:102]	5'h0
FCCC_NGMUX2_CR1	SELGL[29:25]	INIT[111:107]	5'h0
FCCC_NGMUX3_CR0	SELGL[34:30]	INIT[116:112]	5'h0
FCCC_NGMUX3_CR1	SELGL[39:35]	INIT[121:117]	5'h0
FCCC_GPD0_SYNC_CR	RESET_GENEN[0]	INIT[122:122]	1'h0
FCCC_GPD1_SYNC_CR	RESET_GENEN[1]	INIT[123:123]	1'h0
FCCC_GPD2_SYNC_CR	RESET_GENEN[2]	INIT[124:124]	1'h0
FCCC_GPD3_SYNC_CR	RESET_GENEN[3]	INIT[125:125]	1'h0
FCCC_RFMUX_CR	INVRF[3:0]	INIT[131:126]	6'h0
FCCC_PDLY_CR	SEL_PLL_DLINE[5:0]	INIT[137:132]	6'h0
FCCC_PDLY_CR	RF_DLINE	INIT[138:138]	1'h0
FCCC_PLL_CR0	LOCKWIN[2:0]	INIT[141:139]	3'h0
FCCC_PLL_CR1	LOCKCNT[3:0]	INIT[145:142]	4'h0
FCCC_PLL_CR7	DIVQ[2:0]	INIT[148:146]	3'h0
FCCC_PLL_CR5	MODE32K	INIT[149:149]	1'h0
FCCC_PLL_CR5	MODE_1V2	INIT[150:150]	1'h0
FCCC_PLL_CR5	MODE_3V3	INIT[151:151]	1'h0
FCCC_PLL_CR6	FSE	INIT[152:152]	1'h0
FCCC_PLL_CR4	SSE	INIT[153:153]	1'h0
FCCC_PLL_CR3	SSMD[1:0]	INIT[155:154]	2'h0

Table 16 • **CCC-SW1 (Unused)** ***(continued)***

Register	Field	INIT	Value
FCCC_PLL_CR2	SSMF[4:0]	INIT[160:156]	5'h0
FCCC_PLL_CR8	DIVR[5:0]	INIT[166:161]	6'h0
FCCC_PLL_CR9	DIVF[5:0]	INIT[174:167]	8'h0
FCCC_PLL_CR10	RANGE	INIT[178:175]	4'h0
FCCC_GPMUX0_CR	NOPIPE_SYNCRST0	INIT[179:179]	1'h0
FCCC_GPMUX1_CR	NOPIPE_SYNCRST1	INIT[180:180]	1'h0
FCCC_GPMUX2_CR	NOPIPE_SYNCRST2	INIT[181:181]	1'h0
FCCC_GPMUX3_CR	NOPIPE_SYNCRST3	INIT[182:182]	1'h0
FCCC_GPD0_SYNC_CR	SRESET_GENEN[0]	INIT[183:183]	1'h0
FCCC_GPD1_SYNC_CR	SRESET_GENEN[1]	INIT[184:184]	1'h0
FCCC_GPD2_SYNC_CR	SRESET_GENEN[2]	INIT[185:185]	1'h0
FCCC_GPD3_SYNC_CR	SRESET_GENEN[3]	INIT[186:186]	1'h0
FCCC_GPDS_SYNC_CR	SW_RESYNC_GPD	INIT[187:187]	1'h0
FCCC_GPMUX0_CR	INV_GPMUX0	INIT[188:188]	1'h0
FCCC_GPMUX1_CR	INV_GPMUX1	INIT[189:189]	1'h0
FCCC_GPMUX2_CR	INV_GPMUX2	INIT[190:190]	1'h0
FCCC_GPMUX3_CR	INV_GPMUX3	INIT[191:191]	1'h0
RESERVED_0	RESERVED[0]	INIT[192:192]	1'h0
RESERVED_0	RESERVED[1]	INIT[193:193]	1'h0
FCCC_GPD0_SYNC_CR	GPD_MODE_N[0]	INIT[194:194]	1'h0
FCCC_GPD1_SYNC_CR	GPD_MODE_N[1]	INIT[195:195]	1'h0
FCCC_GPD2_SYNC_CR	GPD_MODE_N[2]	INIT[196:196]	1'h0
FCCC_GPD3_SYNC_CR	GPD_MODE_N[3]	INIT[197:197]	1'h0
FCCC_NGMUX0_CR1	SELOUT_0	INIT[198:198]	1'h0
FCCC_NGMUX1_CR1	SELOUT_1	INIT[199:199]	1'h0
FCCC_NGMUX2_CR1	SELOUT_2	INIT[200:200]	1'h0
FCCC_NGMUX3_CR1	SELOUT_3	INIT[201:201]	1'h0
RESERVED_1	RESERVED[7:0]	INIT[209:202]	8'h0

Table 17 • **HPMS/MDDR (Unused)**

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
ESRAM_CONFIG	SW_CC_ESRAMFWREMAP	INIT[147:147]	1'h0	INIT[0]	1
ESRAM_CONFIG	SW_CC_ESRAM1FWREMAP	INIT[148:148]	1'h0	INIT[0]	1
ESRAM_MAX_LAT	SW_MAX_LAT_ESRAM0	INIT[151:149]	3'b001	INIT[1]	1
ESRAM_MAX_LAT	SW_MAX_LAT_ESRAM1	INIT[154:152]	3'b001	INIT[1]	1
DDR_CONFIG	SW_CC_DDRFWREMAP	INIT[155:155]	1'h0	INIT[2]	1
ENVM_CONFIG	SW_ENVMREMAPSIZE	INIT[160:156]	5'b10001	INIT[3]	1
ENVM_CONFIG	NV_FREQRNG	INIT[168:161]	8'h07	INIT[3]	1
ENVM_CONFIG	NV_DPD0	INIT[169:169]	1'h0	INIT[3]	1
ENVM_CONFIG	NV_DPD1	INIT[170:170]	1'h0	INIT[3]	1
ENVM_CONFIG	ENVM_PERSIST	INIT[171:171]	1'h0	INIT[3]	1
ENVM_CONFIG	ENVM_SENSE_ON	INIT[172:172]	1'h0	INIT[3]	1
ENVM_REMAP_BASE	SW_ENVMREMAPBASE	INIT[191:173]	19'h00000	INIT[4]	1
ENVM_FAB_REMAP	SW_ENVMFABREMAPBASE	INIT[210:192]	19'h0	INIT[5]	1
CC_CONFIG	CC_CACHE_ENB	INIT[211:211]	1'h0	INIT[6]	1
CC_CONFIG	CC_SBUS_WR_MODE	INIT[212:212]	1'h0	INIT[6]	1
CC_CONFIG	CC_CACHE_LOCK	INIT[213:213]	1'h0	INIT[6]	1
CC_CACHEREGION	CC_CACHE_REGION	INIT[217:214]	4'h0	INIT[7]	1
CC_LOCKBASEADDR	CC_LOCK_BASEADD	INIT[236:218]	19'h0	INIT[8]	1
CC_FLUSHINDX	CC_FLUSH_INDEX	INIT[242:237]	6'h0	INIT[9]	1
DDRB_BUF_TIMER	DDRB_TIMER	INIT[252:243]	10'h3FF	INIT[10]	1
DDRB_NB_ADR	DDRB_NB_ADDR	INIT[268:253]	16'hA000	INIT[11]	1
DDRB_NB_SIZE	DDRB_NB_SZ	INIT[272:269]	4'h1	INIT[12]	1
DDRB_CONFIG	DDRB_DS_WEN	INIT[273:273]	1'h1	INIT[13]	1
DDRB_CONFIG	DDRB_DS_REN	INIT[274:274]	1'h1	INIT[13]	1
DDRB_CONFIG	DDRB_HPD_WEN	INIT[275:275]	1'h1	INIT[13]	1
DDRB_CONFIG	DDRB_HPD_REN	INIT[276:276]	1'h1	INIT[13]	1
DDRB_CONFIG	DDRB_SW_WEN	INIT[277:277]	1'h1	INIT[13]	1
DDRB_CONFIG	DDRB_SW_REN	INIT[278:278]	1'h1	INIT[13]	1
DDRB_CONFIG	DDRB_IDC_EN	INIT[279:279]	1'h1	INIT[13]	1
DDRB_CONFIG	DDRB_BUF_SZ	INIT[280:280]	1'h1	INIT[13]	1
DDRB_CONFIG	DDR_DS_MAP	INIT[284:281]	4'h0	INIT[13]	1
DDRB_CONFIG	DDR_HPD_MAP	INIT[288:285]	4'h0	INIT[13]	1
DDRB_CONFIG	DDR_SW_MAP	INIT[292:289]	4'h0	INIT[13]	1
DDRB_CONFIG	DDR_IDC_MAP	INIT[296:293]	4'h0	INIT[13]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
EDAC_ENABLE	ESRAM0_EDAC_EN	INIT[297:297]	1'h0	INIT[14]	1
EDAC_ENABLE	ESRAM1_EDAC_EN	INIT[298:298]	1'h0	INIT[14]	1
EDAC_ENABLE	CC_EDAC_EN	INIT[299:299]	1'h0	INIT[14]	1
EDAC_ENABLE	MAC_EDAC_TX_EN	INIT[300:300]	1'h0	INIT[14]	1
EDAC_ENABLE	MAC_EDAC_RX_EN	INIT[301:301]	1'h0	INIT[14]	1
EDAC_ENABLE	USB_EDAC_EN	INIT[302:302]	1'h0	INIT[14]	1
EDAC_ENABLE	CAN_EDAC_EN	INIT[303:303]	1'h0	INIT[14]	1
MASTER_WEIGHT_CONFIG0	SW_WEIGHT_IC	INIT[308:304]	5'h1	INIT[15]	1
MASTER_WEIGHT_CONFIG0	SW_WEIGHT_S	INIT[313:309]		INIT[15]	1
MASTER_WEIGHT_CONFIG0	SW_WEIGHT_GIGE	INIT[318:314]	5'h1	INIT[15]	1
MASTER_WEIGHT_CONFIG0	SW_WEIGHT_FAB_0	INIT[323:319]	5'h1	INIT[15]	1
MASTER_WEIGHT_CONFIG0	SW_WEIGHT_FAB_1	INIT[328:324]	5'h1	INIT[15]	1
MASTER_WEIGHT_CONFIG0	SW_WEIGHT_PDMA	INIT[333:329]	5'h1	INIT[15]	1
MASTER_WEIGHT_CONFIG1	SW_WEIGHT_HPDMA	INIT[338:334]	5'h1	INIT[16]	1
MASTER_WEIGHT_CONFIG1	SW_WEIGHT_USB	INIT[343:339]	5'h1	INIT[16]	1
MASTER_WEIGHT_CONFIG1	SW_WEIGHT_G	INIT[348:344]	5'h1	INIT[16]	1
SOFT_INTERRUPT	SOFTINTERRUPT	INIT[349:349]	1'h0	INIT[17]	1
SOFTRESET	ENVM0_SOFTRESET	INIT[350:350]	1'h0	INIT[18]	1
SOFTRESET	ENVM1_SOFTRESET	INIT[351:351]	1'h0	INIT[19]	1
SOFTRESET	ESRAM0_SOFTRESET	INIT[352:352]	1'h0	INIT[20]	1
SOFTRESET	ESRAM1_SOFTRESET	INIT[353:353]	1'h0	INIT[21]	1
SOFTRESET	MAC_SOFTRESET	INIT[354:354]	1'h1	INIT[22]	1
SOFTRESET	PDMA_SOFTRESET	INIT[355:355]	1'h0	INIT[23]	1
SOFTRESET	TIMER_SOFTRESET	INIT[356:356]	1'h0	INIT[24]	1
SOFTRESET	MMUART0_SOFTRESET	INIT[357:357]	1'h1	INIT[25]	1
SOFTRESET	MMUART1_SOFTRESET	INIT[358:358]	1'h1	INIT[26]	1
SOFTRESET	G4SPI0_SOFTRESET	INIT[359:359]	1'h1	INIT[27]	1
SOFTRESET	G4SPI1_SOFTRESET	INIT[360:360]	1'h1	INIT[28]	1
SOFTRESET	I2C0_SOFTRESET	INIT[361:361]	1'h1	INIT[29]	1
SOFTRESET	I2C1_SOFTRESET	INIT[362:362]	1'h1	INIT[30]	1
SOFTRESET	CAN_SOFTRESET	INIT[363:363]	1'h1	INIT[31]	1
SOFTRESET	USB_SOFTRESET	INIT[364:364]	1'h1	INIT[32]	1
SOFTRESET	COMBLK_SOFTRESET	INIT[365:365]	1'h0	INIT[33]	1
SOFTRESET	FPGA_SOFTRESET	INIT[366:366]	1'h1	INIT[34]	1
SOFTRESET	HPDMA_SOFTRESET	INIT[367:367]	1'h0	INIT[35]	1
SOFTRESET	FIC32_0_SOFTRESET	INIT[368:368]	1'h1	INIT[36]	1
SOFTRESET	FIC32_1_SOFTRESET	INIT[369:369]	1'h1	INIT[37]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
SOFTRESET	MSS_GPIO_SOFTRESET	INIT[370:370]	1'h1	INIT[38]	1
SOFTRESET	MSS_GPOUT_7_0_SOFT_RESET	INIT[371:371]	1'h1	INIT[39]	1
SOFTRESET	MSS_GPOUT_15_8_SOFT_RESET	INIT[372:372]	1'h1	INIT[40]	1
SOFTRESET	MSS_GPOUT_23_16_SOFT_RESET	INIT[373:373]	1'h1	INIT[41]	1
SOFTRESET	MSS_GPOUT_31_24_SOFT_RESET	INIT[374:374]	1'h1	INIT[42]	1
SOFTRESET	MDDR_CTLR_SOFTRESET	INIT[375:375]	1'h1	INIT[43]	1
SOFTRESET	MDDR_FIC64_SOFTRESET	INIT[376:376]	1'h1	INIT[44]	1
M3_CONFIG	STCALIB250	INIT[402:377]	26'h2000000	INIT[45]	1
M3_CONFIG	STCLK_DIVISOR	INIT[404:403]	2'b11	INIT[45]	1
M3_CONFIG	M3_MPU_DISABLE	INIT[405:405]	1'h0	INIT[45]	1
FAB_IF	FAB0_AHB_BYPASS	INIT[406:406]	1'h0	INIT[46]	1
FAB_IF	FAB1_AHB_BYPASS	INIT[407:407]	1'h0	INIT[46]	1
FAB_IF	FAB0_AHB_MODE	INIT[408:408]	1'h0	INIT[46]	1
FAB_IF	FAB1_AHB_MODE	INIT[409:409]	1'h0	INIT[46]	1
FAB_IF	SW_FIC_REG_SEL	INIT[415:410]	6'h38	INIT[46]	1
LOOPBACK_CTRL	MSS_MMUARTLOOPBACK	INIT[416:416]	1'h0	INIT[47]	1
LOOPBACK_CTRL	MSS_SPILOOPBACK	INIT[417:417]	1'h0	INIT[47]	1
LOOPBACK_CTRL	MSS_I2CLOOPBACK	INIT[418:418]	1'h0	INIT[47]	1
LOOPBACK_CTRL	MSS_GPIOLOOPBACK	INIT[419:419]	1'h0	INIT[47]	1
GPIO_SYSRESET_SEL	MSS_GPIO_7_0_SYSRESET_SEL	INIT[420:420]	1'h0	INIT[48]	1
GPIO_SYSRESET_SEL	MSS_GPIO_15_8_SYSRESET_SEL	INIT[421:421]	1'h0	INIT[48]	1
GPIO_SYSRESET_SEL	MSS_GPIO_23_16_SYSRESET_SEL	INIT[422:422]	1'h0	INIT[48]	1
GPIO_SYSRESET_SEL	MSS_GPIO_31_24_SYSRESET_SEL	INIT[423:423]	1'h0	INIT[48]	1
GPIN_SRC_SEL	MSS_GPINSOURCE	INIT[455:424]	32'h0	INIT[49]	1
MDDR_CONFIG	MDDR_CONFIG_LOCAL	INIT[456:456]	1'h0	INIT[50]	1
MDDR_CONFIG	SDR_MODE	INIT[457:457]	1'h0	INIT50[]	1
MDDR_CONFIG	F_AXI_AHB_MODE	INIT[458:458]	1'h0	INIT[50]	1
MDDR_CONFIG	PHY_SELF_REF_EN	INIT[459:459]	1'h0	INIT[50]	1
USB_IO_INPUT_SEL	USB_IO_INPUT_SEL	INIT[461:460]	2'h0	INIT[51]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
PERIPH_CLOCK_MUX_SEL	SPI0_SCK_FAB_SEL	INIT[462:462]	1'h0	INIT[52]	1
PERIPH_CLOCK_MUX_SEL	SPI1_SCK_FAB_SEL	INIT[463:463]	1'h0	INIT[52]	1
PERIPH_CLOCK_MUX_SEL	TRACECLK_DIV2_SEL	INIT[464:464]	1'h0	INIT[52]	1
WDOGCONFIG	G4_TESTWDOGENABLE	INIT[465:465]	1'h0	INIT[53]	1
WDOGCONFIG	G4_TESTWDOGMODE	INIT[466:466]	1'h0	INIT[53]	1
MDDR_IO_CALIB	PCODE	INIT[472:467]	6'h0	INIT[54]	1
MDDR_IO_CALIB	NCODE	INIT[478:473]	6'h0	INIT[54]	1
MDDR_IO_CALIB	CALIB_TRIM	INIT[479:479]	1'h0	INIT[54]	1
SPARE_OUT	MSS_SPARE_OUT	INIT[495:480]	16'h0	INIT[55]	1
EDAC_INT_ENABLE	ESRAM0_EDAC_1E_EN	INIT[496:496]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	ESRAM0_EDAC_2E_EN	INIT[497:497]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	ESRAM1_EDAC_1E_EN	INIT[498:498]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	ESRAM1_EDAC_2E_EN	INIT[499:499]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	CC_EDAC_1E_EN	INIT[500:500]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	CC_EDAC_2E_EN	INIT[501:501]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	MAC_EDAC_TX_1E_EN	INIT[502:502]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	MAC_EDAC_TX_2E_EN	INIT[503:503]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	MAC_EDAC_RX_1E_EN	INIT[504:504]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	MAC_EDAC_RX_2E_EN	INIT[505:505]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	USB_EDAC_1E_EN	INIT[506:506]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	USB_EDAC_2E_EN	INIT[507:507]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	CAN_EDAC_1E_EN	INIT[508:508]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	CAN_EDAC_2E_EN	INIT[509:509]	1'h0	INIT[56]	1
EDAC_INT_ENABLE	MDDR_ECC_INT_EN	INIT[510:510]	1'h0	INIT[56]	1
USB_CONFIG	USB_UTMI_SEL	INIT[511:511]	1'h0	INIT[57]	1
USB_CONFIG	USB_DDR_SELECT	INIT[512:512]	1'h0	INIT[57]	1
ESRAM_PIPELINE_CONFIG	ESRAM_PIPELINE_ENABLE	INIT[513:513]	1'h1	INIT[58]	1
MSS_INTERRUPT_ENABLE	SW_INTERRUPT_EN	INIT[520:514]	7'h7F	INIT[59]	1
MSS_INTERRUPT_ENABLE	CC_INTERRUPT_EN	INIT[523:521]	3'h7	INIT[59]	1
MSS_INTERRUPT_ENABLE	DDRB_INTERRUPT_EN	INIT[533:524]	10'h3FF	INIT[59]	1
RTC_WAKEUP_CONFIG	RTC_WAKEUP_M3_EN	INIT[534:534]	1'h0	INIT[60]	1
RTC_WAKEUP_CONFIG	RTC_WAKEUP_FAB_EN	INIT[535:535]	1'h0	INIT[60]	1
RTC_WAKEUP_CONFIG	RTC_WAKEUP_G4C_EN	INIT[536:536]	1'h0	INIT[60]	1
MAC_CONFIG	ETH_LINE_SPEED	INIT[538:537]	2'h0	INIT[61]	1
MAC_CONFIG	ETH_PHY_MODE	INIT[541:539]	3'h0	INIT[61]	1
MAC_CONFIG	RGMII_TXC_DELAY_SEL	INIT[545:542]	4'h0	INIT[61]	1
MSSDDR_PLL_STATUS_LOW	FACC_PLL_DIVR	INIT[551:546]	6'h1	INIT[62]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
MSSDDR_PLL_STATUS_LOW	FACC_PLL_DIVF	INIT[561:552]	10'h2	INIT[62]	1
MSSDDR_PLL_STATUS_LOW	FACC_PLL_DIVQ	INIT[564:562]	3'h2	INIT[62]	1
MSSDDR_PLL_STATUS_LOW	FACC_PLL_RANGE	INIT[568:565]	4'h0	INIT[62]	1
MSSDDR_PLL_STATUS_LOW	FACC_PLL_LOCKWIN	INIT[571:569]	3'h0	INIT[62]	1
MSSDDR_PLL_STATUS_LOW	FACC_PLL_LOCKCNT	INIT[575:572]	4'h0	INIT[62]	1
MSSDDR_PLL_STATUS_HIGH	FACC_PLL_BYPASS	INIT[576:576]	1'h0	INIT[63]	1
MSSDDR_PLL_STATUS_HIGH	FACC_PLL_MODE_1V2	INIT[577:577]	1'h1	INIT[63]	1
MSSDDR_PLL_STATUS_HIGH	FACC_PLL_MODE_3V3	INIT[578:578]	1'h0	INIT[63]	1
MSSDDR_PLL_STATUS_HIGH	FACC_PLL_FSE	INIT[579:579]	1'h0	INIT[63]	1
MSSDDR_PLL_STATUS_HIGH	FACC_PLL_PD	INIT[580:580]	1'h1	INIT[63]	1
MSSDDR_PLL_STATUS_HIGH	FACC_PLL_SSE	INIT[581:581]	1'h0	INIT[63]	1
MSSDDR_PLL_STATUS_HIGH	FACC_PLL_SSMD	INIT[583:582]	2'h0	INIT[63]	1
MSSDDR_PLL_STATUS_HIGH	FACC_PLL_SSMF	INIT[588:584]	5'h0	INIT[63]	1
MSSDDR_FACC_CONFIG_1	DIVISOR_A	INIT[590:589]	2'h0	INIT[64]	1
MSSDDR_FACC_CONFIG_1	APB0_DIVISOR	INIT[593:591]	3'h0	INIT[65]	1
MSSDDR_FACC_CONFIG_1	APB1_DIVISOR	INIT[596:594]	3'h0	INIT[66]	1
MSSDDR_FACC_CONFIG_1	DDR_CLK_EN	INIT[597:597]	1'h0	INIT[67]	1
MSSDDR_FACC_CONFIG_1	FCLK_DIVISOR	INIT[600:598]	3'h0	INIT[68]	1
MSSDDR_FACC_CONFIG_1	FACC_GLMUX_SEL	INIT[601:601]	1'h1	INIT[69]	1
MSSDDR_FACC_CONFIG_1	FIC32_0_DIVISOR	INIT[604:602]	3'h0	INIT[70]	1
MSSDDR_FACC_CONFIG_1	FIC32_1_DIVISOR	INIT[607:605]	3'h0	INIT[71]	1
MSSDDR_FACC_CONFIG_1	FIC64_DIVISOR	INIT[610:608]	3'h0	INIT[72]	1
MSSDDR_FACC_CONFIG_1	BASE_DIVISOR	INIT[613:611]	3'h0	INIT[73]	1
MSSDDR_FACC_CONFIG_1	PERSIST_CC	INIT[614:614]	1'h1	INIT[74]	1
MSSDDR_FACC_CONFIG_1	CONTROLLER_PLL_INIT	INIT[615:615]	1'h0	INIT[75]	1
MSSDDR_FACC_CONFIG_1	FACC_FAB_REF_SEL	INIT[616:616]	1'h0	INIT[76]	1
MSSDDR_FACC_CONFIG_2	RTC_CLK_SEL	INIT[618:617]	2'h0	INIT[77]	1
MSSDDR_FACC_CONFIG_2	FACC_SRC_SEL	INIT[621:619]	3'h0	INIT[78]	1
MSSDDR_FACC_CONFIG_2	FACC_PRE_SRC_SEL	INIT[622:622]	1'h0	INIT[79]	1
MSSDDR_FACC_CONFIG_2	FACC_STANDBY_SEL	INIT[625:623]	3'h4	INIT[80]	1
MSSDDR_FACC_CONFIG_2	MSS_25_50MHZ_EN	INIT[626:626]	1'h1	INIT[81]	1
MSSDDR_FACC_CONFIG_2	MSS_1MHZ_EN	INIT[627:627]	1'h1	INIT[82]	1
MSSDDR_FACC_CONFIG_2	MSS_CLK_ENVM_EN	INIT[628:628]	1'h1	INIT[83]	1
MSSDDR_FACC_CONFIG_2	MSS_XTAL_EN	INIT[629:629]	1'h1	INIT[84]	1
MSSDDR_FACC_CONFIG_2	MSS_XTAL_RTC_EN	INIT[630:630]	1'h1	INIT[85]	1
PLL_LOCK_EN	MPLL_LOCK_EN	INIT[631:631]	1'h0	INIT[86]	1
PLL_LOCK_EN	MPLL_LOCK_LOST_EN	INIT[632:632]	1'h0	INIT[86]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
PLL_LOCK_EN	FAB_PLL_LOCK_EN	INIT[633:633]	1'h0	INIT[86]	1
PLL_LOCK_EN	FAB_PLL_LOCK_LOST_EN	INIT[634:634]	1'h0	INIT[86]	1
MSSDDR_CLK_CALIB_CONFIG	FAB_CALIB_START	INIT[635:635]	1'h0	INIT[87]	1
PLL_DELAY_LINE_SEL	PLL_REF_DEL_SEL	INIT[637:636]	2'h0	INIT[88]	1
PLL_DELAY_LINE_SEL	PLL_FB_DEL_SEL	INIT[639:638]	2'h0	INIT[88]	1
MAC_STAT_CLRONRD	MAC_STAT_CLRONRD	INIT[640:640]	1'h1	INIT[89]	
WDOGLOAD	G4_TESTWDOGLOAD	INIT[666:641]	26'h1800000	N/A	N/A
WDOGMVRP	G4_TESTWDOGMVRP	INIT[698:667]	32'hFFFFFFFF	N/A	N/A
USERCONFIG0	CONFIG_REG0	INIT[730:699]	32'h0	N/A	N/A
USERCONFIG1	CONFIG_REG1	INIT[762:731]	32'h0	N/A	N/A
USERCONFIG2	CONFIG_REG2	INIT[794:763]	32'h0	N/A	N/A
USERCONFIG3	CONFIG_REG3	INIT[826:795]	32'h0	N/A	N/A
FAB_PROT_SIZE	SW_PROTREGIONSIZE	INIT[831:827]	5'b11110	N/A	N/A
FAB_PROT_BASE	SW_PROTREGIONBASE	INIT[863:832]	32'h0	N/A	N/A
MSS_GPIO_DEF	MSS_GPIO_7_0_DEF	INIT[864:864]	1'h1	N/A	N/A
MSS_GPIO_DEF	MSS_GPIO_15_8_DEF	INIT[865:865]	1'h1	N/A	N/A
MSS_GPIO_DEF	MSS_GPIO_23_16_DEF	INIT[866:866]	1'h1	N/A	N/A
MSS_GPIO_DEF	MSS_GPIO_31_24_DEF	INIT[867:867]	1'h1	N/A	N/A
IOMUXCELL_0_CONFIG	MSS_IOMUXSEL0	INIT[868:868]	1'h0	INIT[90]	1
IOMUXCELL_0_CONFIG	MSS_IOMUXSEL1	INIT[869:869]	1'h0	INIT[90]	1
IOMUXCELL_0_CONFIG	MSS_IOMUXSEL2	INIT[870:870]	1'h0	INIT[90]	1
IOMUXCELL_0_CONFIG	MSS_IOMUXSEL3	INIT[871:871]	1'h0	INIT[90]	1
IOMUXCELL_0_CONFIG	MSS_IOMUXSEL4UPPER	INIT[872:872]	1'h0	INIT[90]	1
IOMUXCELL_0_CONFIG	MSS_IOMUXSEL4MID	INIT[873:873]	1'h0	INIT[90]	1
IOMUXCELL_0_CONFIG	MSS_IOMUXSEL4LOWER	INIT[874:874]	1'h0	INIT[90]	1
IOMUXCELL_0_CONFIG	MSS_IOMUXSEL5UPPER	INIT[875:875]	1'h0	INIT[90]	1
IOMUXCELL_0_CONFIG	MSS_IOMUXSEL5MID	INIT[876:876]	1'h0	INIT[90]	1
IOMUXCELL_0_CONFIG	MSS_IOMUXSEL5LOWER	INIT[877:877]	1'h0	INIT[90]	1
IOMUXCELL_1_CONFIG	MSS_IOMUXSEL0	INIT[878:878]	1'h0	INIT[91]	1
IOMUXCELL_1_CONFIG	MSS_IOMUXSEL1	INIT[879:879]	1'h0	INIT[91]	1
IOMUXCELL_1_CONFIG	MSS_IOMUXSEL2	INIT[880:880]	1'h0	INIT[91]	1
IOMUXCELL_1_CONFIG	MSS_IOMUXSEL3	INIT[881:881]	1'h0	INIT[91]	1
IOMUXCELL_1_CONFIG	MSS_IOMUXSEL4UPPER	INIT[882:882]	1'h0	INIT[91]	1
IOMUXCELL_1_CONFIG	MSS_IOMUXSEL4MID	INIT[883:883]	1'h0	INIT[91]	1
IOMUXCELL_1_CONFIG	MSS_IOMUXSEL4LOWER	INIT[884:884]	1'h0	INIT[91]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_1_CONFIG	MSS_IOMUXSEL5UPPER	INIT[885:885]	1'h0	INIT[91]	1
IOMUXCELL_1_CONFIG	MSS_IOMUXSEL5MID	INIT[886:886]	1'h0	INIT[91]	1
IOMUXCELL_1_CONFIG	MSS_IOMUXSEL5LOWER	INIT[887:887]	1'h0	INIT[91]	1
IOMUXCELL_2_CONFIG	MSS_IOMUXSEL0	INIT[888:888]	1'h0	INIT[92]	1
IOMUXCELL_2_CONFIG	MSS_IOMUXSEL1	INIT[889:889]	1'h0	INIT[92]	1
IOMUXCELL_2_CONFIG	MSS_IOMUXSEL2	INIT[890:890]	1'h0	INIT[92]	1
IOMUXCELL_2_CONFIG	MSS_IOMUXSEL3	INIT[891:891]	1'h0	INIT[92]	1
IOMUXCELL_2_CONFIG	MSS_IOMUXSEL4UPPER	INIT[892:892]	1'h0	INIT[92]	1
IOMUXCELL_2_CONFIG	MSS_IOMUXSEL4MID	INIT[893:893]	1'h0	INIT[92]	1
IOMUXCELL_2_CONFIG	MSS_IOMUXSEL4LOWER	INIT[894:894]	1'h0	INIT[92]	1
IOMUXCELL_2_CONFIG	MSS_IOMUXSEL5UPPER	INIT[895:895]	1'h0	INIT[92]	1
IOMUXCELL_2_CONFIG	MSS_IOMUXSEL5MID	INIT[896:896]	1'h0	INIT[92]	1
IOMUXCELL_2_CONFIG	MSS_IOMUXSEL5LOWER	INIT[897:897]	1'h0	INIT[92]	1
IOMUXCELL_3_CONFIG	MSS_IOMUXSEL0	INIT[898:898]	1'h0	INIT[93]	1
IOMUXCELL_3_CONFIG	MSS_IOMUXSEL1	INIT[899:899]	1'h0	INIT[93]	1
IOMUXCELL_3_CONFIG	MSS_IOMUXSEL2	INIT[900:900]	1'h0	INIT[93]	1
IOMUXCELL_3_CONFIG	MSS_IOMUXSEL3	INIT[901:901]	1'h0	INIT[93]	1
IOMUXCELL_3_CONFIG	MSS_IOMUXSEL4UPPER	INIT[902:902]	1'h0	INIT[93]	1
IOMUXCELL_3_CONFIG	MSS_IOMUXSEL4MID	INIT[903:903]	1'h0	INIT[93]	1
IOMUXCELL_3_CONFIG	MSS_IOMUXSEL4LOWER	INIT[904:904]	1'h0	INIT[93]	1
IOMUXCELL_3_CONFIG	MSS_IOMUXSEL5UPPER	INIT[905:905]	1'h0	INIT[93]	1
IOMUXCELL_3_CONFIG	MSS_IOMUXSEL5MID	INIT[906:906]	1'h0	INIT[93]	1
IOMUXCELL_3_CONFIG	MSS_IOMUXSEL5LOWER	INIT[907:907]	1'h0	INIT[93]	1
IOMUXCELL_4_CONFIG	MSS_IOMUXSEL0	INIT[908:908]	1'h0	INIT[94]	1
IOMUXCELL_4_CONFIG	MSS_IOMUXSEL1	INIT[909:909]	1'h0	INIT[94]	1
IOMUXCELL_4_CONFIG	MSS_IOMUXSEL2	INIT[910:910]	1'h0	INIT[94]	1
IOMUXCELL_4_CONFIG	MSS_IOMUXSEL3	INIT[911:911]	1'h0	INIT[94]	1
IOMUXCELL_4_CONFIG	MSS_IOMUXSEL4UPPER	INIT[912:912]	1'h0	INIT[94]	1
IOMUXCELL_4_CONFIG	MSS_IOMUXSEL4MID	INIT[913:913]	1'h0	INIT[94]	1
IOMUXCELL_4_CONFIG	MSS_IOMUXSEL4LOWER	INIT[914:914]	1'h0	INIT[94]	1
IOMUXCELL_4_CONFIG	MSS_IOMUXSEL5UPPER	INIT[915:915]	1'h0	INIT[94]	1
IOMUXCELL_4_CONFIG	MSS_IOMUXSEL5MID	INIT[916:916]	1'h0	INIT[94]	1
IOMUXCELL_4_CONFIG	MSS_IOMUXSEL5LOWER	INIT[917:917]	1'h0	INIT[94]	1
IOMUXCELL_5_CONFIG	MSS_IOMUXSEL0	INIT[918:918]	1'h0	INIT[95]	1
IOMUXCELL_5_CONFIG	MSS_IOMUXSEL1	INIT[919:919]	1'h0	INIT[95]	1
IOMUXCELL_5_CONFIG	MSS_IOMUXSEL2	INIT[920:920]	1'h0	INIT[95]	1
IOMUXCELL_5_CONFIG	MSS_IOMUXSEL3	INIT[921:921]	1'h0	INIT[95]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_5_CONFIG	MSS_IOMUXSEL4UPPER	INIT[922:922]	1'h0	INIT[95]	1
IOMUXCELL_5_CONFIG	MSS_IOMUXSEL4MID	INIT[923:923]	1'h0	INIT[95]	1
IOMUXCELL_5_CONFIG	MSS_IOMUXSEL4LOWER	INIT[924:924]	1'h0	INIT[95]	1
IOMUXCELL_5_CONFIG	MSS_IOMUXSEL5UPPER	INIT[925:925]	1'h0	INIT[95]	1
IOMUXCELL_5_CONFIG	MSS_IOMUXSEL5MID	INIT[926:926]	1'h0	INIT[95]	1
IOMUXCELL_5_CONFIG	MSS_IOMUXSEL5LOWER	INIT[927:927]	1'h0	INIT[95]	1
IOMUXCELL_6_CONFIG	MSS_IOMUXSEL0	INIT[928:928]	1'h0	INIT[96]	1
IOMUXCELL_6_CONFIG	MSS_IOMUXSEL1	INIT[929:929]	1'h0	INIT[96]	1
IOMUXCELL_6_CONFIG	MSS_IOMUXSEL2	INIT[930:930]	1'h0	INIT[96]	1
IOMUXCELL_6_CONFIG	MSS_IOMUXSEL3	INIT[931:931]	1'h0	INIT[96]	1
IOMUXCELL_6_CONFIG	MSS_IOMUXSEL4UPPER	INIT[932:932]	1'h0	INIT[96]	1
IOMUXCELL_6_CONFIG	MSS_IOMUXSEL4MID	INIT[933:933]	1'h0	INIT[96]	1
IOMUXCELL_6_CONFIG	MSS_IOMUXSEL4LOWER	INIT[934:934]	1'h0	INIT[96]	1
IOMUXCELL_6_CONFIG	MSS_IOMUXSEL5UPPER	INIT[935:935]	1'h0	INIT[96]	1
IOMUXCELL_6_CONFIG	MSS_IOMUXSEL5MID	INIT[936:936]	1'h0	INIT[96]	1
IOMUXCELL_6_CONFIG	MSS_IOMUXSEL5LOWER	INIT[937:937]	1'h0	INIT[96]	1
IOMUXCELL_7_CONFIG	MSS_IOMUXSEL0	INIT[938:938]	1'h0	INIT[97]	1
IOMUXCELL_7_CONFIG	MSS_IOMUXSEL1	INIT[939:939]	1'h0	INIT[97]	1
IOMUXCELL_7_CONFIG	MSS_IOMUXSEL2	INIT[940:940]	1'h0	INIT[97]	1
IOMUXCELL_7_CONFIG	MSS_IOMUXSEL3	INIT[941:941]	1'h0	INIT[97]	1
IOMUXCELL_7_CONFIG	MSS_IOMUXSEL4UPPER	INIT[942:942]	1'h0	INIT[97]	1
IOMUXCELL_7_CONFIG	MSS_IOMUXSEL4MID	INIT[943:943]	1'h0	INIT[97]	1
IOMUXCELL_7_CONFIG	MSS_IOMUXSEL4LOWER	INIT[944:944]	1'h0	INIT[97]	1
IOMUXCELL_7_CONFIG	MSS_IOMUXSEL5UPPER	INIT[945:945]	1'h0	INIT[97]	1
IOMUXCELL_7_CONFIG	MSS_IOMUXSEL5MID	INIT[946:946]	1'h0	INIT[97]	1
IOMUXCELL_7_CONFIG	MSS_IOMUXSEL5LOWER	INIT[947:947]	1'h0	INIT[97]	1
IOMUXCELL_8_CONFIG	MSS_IOMUXSEL0	INIT[948:948]	1'h0	INIT[98]	1
IOMUXCELL_8_CONFIG	MSS_IOMUXSEL1	INIT[949:949]	1'h0	INIT[98]	1
IOMUXCELL_8_CONFIG	MSS_IOMUXSEL2	INIT[950:950]	1'h0	INIT[98]	1
IOMUXCELL_8_CONFIG	MSS_IOMUXSEL3	INIT[951:951]	1'h0	INIT[98]	1
IOMUXCELL_8_CONFIG	MSS_IOMUXSEL4UPPER	INIT[952:952]	1'h0	INIT[98]	1
IOMUXCELL_8_CONFIG	MSS_IOMUXSEL4MID	INIT[953:953]	1'h0	INIT[98]	1
IOMUXCELL_8_CONFIG	MSS_IOMUXSEL4LOWER	INIT[954:954]	1'h0	INIT[98]	1
IOMUXCELL_8_CONFIG	MSS_IOMUXSEL5UPPER	INIT[955:955]	1'h0	INIT[98]	1
IOMUXCELL_8_CONFIG	MSS_IOMUXSEL5MID	INIT[956:956]	1'h0	INIT[98]	1
IOMUXCELL_8_CONFIG	MSS_IOMUXSEL5LOWER	INIT[957:957]	1'h0	INIT[98]	1
IOMUXCELL_9_CONFIG	MSS_IOMUXSEL0	INIT[958:958]	1'h0	INIT[99]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_9_CONFIG	MSS_IOMUXSEL1	INIT[959:959]	1'h0	INIT[99]	1
IOMUXCELL_9_CONFIG	MSS_IOMUXSEL2	INIT[960:960]	1'h0	INIT[99]	1
IOMUXCELL_9_CONFIG	MSS_IOMUXSEL3	INIT[961:961]	1'h0	INIT[99]	1
IOMUXCELL_9_CONFIG	MSS_IOMUXSEL4UPPER	INIT[962:962]	1'h0	INIT[99]	1
IOMUXCELL_9_CONFIG	MSS_IOMUXSEL4MID	INIT[963:963]	1'h0	INIT[99]	1
IOMUXCELL_9_CONFIG	MSS_IOMUXSEL4LOWER	INIT[964:964]	1'h0	INIT[99]	1
IOMUXCELL_9_CONFIG	MSS_IOMUXSEL5UPPER	INIT[965:965]	1'h0	INIT[99]	1
IOMUXCELL_9_CONFIG	MSS_IOMUXSEL5MID	INIT[966:966]	1'h0	INIT[99]	1
IOMUXCELL_9_CONFIG	MSS_IOMUXSEL5LOWER	INIT[967:967]	1'h0	INIT[99]	1
IOMUXCELL_10_CONFIG	MSS_IOMUXSEL0	INIT[968:968]	1'h0	INIT[100]	1
IOMUXCELL_10_CONFIG	MSS_IOMUXSEL1	INIT[969:969]	1'h0	INIT[100]	1
IOMUXCELL_10_CONFIG	MSS_IOMUXSEL2	INIT[970:970]	1'h0	INIT[100]	1
IOMUXCELL_10_CONFIG	MSS_IOMUXSEL3	INIT[971:971]	1'h0	INIT[100]	1
IOMUXCELL_10_CONFIG	MSS_IOMUXSEL4UPPER	INIT[972:972]	1'h0	INIT[100]	1
IOMUXCELL_10_CONFIG	MSS_IOMUXSEL4MID	INIT[973:973]	1'h0	INIT[100]	1
IOMUXCELL_10_CONFIG	MSS_IOMUXSEL4LOWER	INIT[974:974]	1'h0	INIT[100]	1
IOMUXCELL_10_CONFIG	MSS_IOMUXSEL5UPPER	INIT[975:975]	1'h0	INIT[100]	1
IOMUXCELL_10_CONFIG	MSS_IOMUXSEL5MID	INIT[976:976]	1'h0	INIT[100]	1
IOMUXCELL_10_CONFIG	MSS_IOMUXSEL5LOWER	INIT[977:977]	1'h0	INIT[100]	1
IOMUXCELL_11_CONFIG	MSS_IOMUXSEL0	INIT[978:978]	1'h0	INIT[101]	1
IOMUXCELL_11_CONFIG	MSS_IOMUXSEL1	INIT[979:979]	1'h0	INIT[101]	1
IOMUXCELL_11_CONFIG	MSS_IOMUXSEL2	INIT[980:980]	1'h0	INIT[101]	1
IOMUXCELL_11_CONFIG	MSS_IOMUXSEL3	INIT[981:981]	1'h0	INIT[101]	1
IOMUXCELL_11_CONFIG	MSS_IOMUXSEL4UPPER	INIT[982:982]	1'h0	INIT[101]	1
IOMUXCELL_11_CONFIG	MSS_IOMUXSEL4MID	INIT[983:983]	1'h0	INIT[101]	1
IOMUXCELL_11_CONFIG	MSS_IOMUXSEL4LOWER	INIT[984:984]	1'h0	INIT[101]	1
IOMUXCELL_11_CONFIG	MSS_IOMUXSEL5UPPER	INIT[985:985]	1'h0	INIT[101]	1
IOMUXCELL_11_CONFIG	MSS_IOMUXSEL5MID	INIT[986:986]	1'h0	INIT[101]	1
IOMUXCELL_11_CONFIG	MSS_IOMUXSEL5LOWER	INIT[987:987]	1'h0	INIT[101]	1
IOMUXCELL_12_CONFIG	MSS_IOMUXSEL0	INIT[988:988]	1'h0	INIT[102]	1
IOMUXCELL_12_CONFIG	MSS_IOMUXSEL1	INIT[989:989]	1'h0	INIT[102]	1
IOMUXCELL_12_CONFIG	MSS_IOMUXSEL2	INIT[990:990]	1'h0	INIT[102]	1
IOMUXCELL_12_CONFIG	MSS_IOMUXSEL3	INIT[991:991]	1'h0	INIT[102]	1
IOMUXCELL_12_CONFIG	MSS_IOMUXSEL4UPPER	INIT[992:992]	1'h0	INIT[102]	1
IOMUXCELL_12_CONFIG	MSS_IOMUXSEL4MID	INIT[993:993]	1'h0	INIT[102]	1
IOMUXCELL_12_CONFIG	MSS_IOMUXSEL4LOWER	INIT[994:994]	1'h0	INIT[102]	1
IOMUXCELL_12_CONFIG	MSS_IOMUXSEL5UPPER	INIT[995:995]	1'h0	INIT[102]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_12_CONFIG	MSS_IOMUXSEL5MID	INIT[996:996]	1'h0	INIT[102]	1
IOMUXCELL_12_CONFIG	MSS_IOMUXSEL5LOWER	INIT[997:997]	1'h0	INIT[102]	1
IOMUXCELL_13_CONFIG	MSS_IOMUXSEL0	INIT[998:998]	1'h0	INIT[103]	1
IOMUXCELL_13_CONFIG	MSS_IOMUXSEL1	INIT[999:999]	1'h0	INIT[103]	1
IOMUXCELL_13_CONFIG	MSS_IOMUXSEL2	INIT[1000:1000]	1'h0	INIT[103]	1
IOMUXCELL_13_CONFIG	MSS_IOMUXSEL3	INIT[1001:1001]	1'h0	INIT[103]	1
IOMUXCELL_13_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1002:1002]	1'h0	INIT[103]	1
IOMUXCELL_13_CONFIG	MSS_IOMUXSEL4MID	INIT[1003:1003]	1'h0	INIT[103]	1
IOMUXCELL_13_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1004:1004]	1'h0	INIT[103]	1
IOMUXCELL_13_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1005:1005]	1'h0	INIT[103]	1
IOMUXCELL_13_CONFIG	MSS_IOMUXSEL5MID	INIT[1006:1006]	1'h0	INIT[103]	1
IOMUXCELL_13_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1007:1007]	1'h0	INIT[103]	1
IOMUXCELL_14_CONFIG	MSS_IOMUXSEL0	INIT[1008:1008]	1'h0	INIT[104]	1
IOMUXCELL_14_CONFIG	MSS_IOMUXSEL1	INIT[1009:1009]	1'h0	INIT[104]	1
IOMUXCELL_14_CONFIG	MSS_IOMUXSEL2	INIT[1010:1010]	1'h0	INIT[104]	1
IOMUXCELL_14_CONFIG	MSS_IOMUXSEL3	INIT[1011:1011]	1'h0	INIT[104]	1
IOMUXCELL_14_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1012:1012]	1'h0	INIT[104]	1
IOMUXCELL_14_CONFIG	MSS_IOMUXSEL4MID	INIT[1013:1013]	1'h0	INIT[104]	1
IOMUXCELL_14_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1014:1014]	1'h0	INIT[104]	1
IOMUXCELL_14_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1015:1015]	1'h0	INIT[104]	1
IOMUXCELL_14_CONFIG	MSS_IOMUXSEL5MID	INIT[1016:1016]	1'h0	INIT[104]	1
IOMUXCELL_14_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1017:1017]	1'h0	INIT[104]	1
IOMUXCELL_15_CONFIG	MSS_IOMUXSEL0	INIT[1018:1018]	1'h0	INIT[105]	1
IOMUXCELL_15_CONFIG	MSS_IOMUXSEL1	INIT[1019:1019]	1'h0	INIT[105]	1
IOMUXCELL_15_CONFIG	MSS_IOMUXSEL2	INIT[1020:1020]	1'h0	INIT[105]	1
IOMUXCELL_15_CONFIG	MSS_IOMUXSEL3	INIT[1021:1021]	1'h0	INIT[105]	1
IOMUXCELL_15_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1022:1022]	1'h0	INIT[105]	1
IOMUXCELL_15_CONFIG	MSS_IOMUXSEL4MID	INIT[1023:1023]	1'h0	INIT[105]	1
IOMUXCELL_15_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1024:1024]	1'h0	INIT[105]	1
IOMUXCELL_15_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1025:1025]	1'h0	INIT[105]	1
IOMUXCELL_15_CONFIG	MSS_IOMUXSEL5MID	INIT[1026:1026]	1'h0	INIT[105]	1
IOMUXCELL_15_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1027:1027]	1'h0	INIT[105]	1
IOMUXCELL_16_CONFIG	MSS_IOMUXSEL0	INIT[1028:1028]	1'h0	INIT[106]	1
IOMUXCELL_16_CONFIG	MSS_IOMUXSEL1	INIT[1029:1029]	1'h0	INIT[106]	1
IOMUXCELL_16_CONFIG	MSS_IOMUXSEL2	INIT[1030:1030]	1'h0	INIT[106]	1
IOMUXCELL_16_CONFIG	MSS_IOMUXSEL3	INIT[1031:1031]	1'h0	INIT[106]	1
IOMUXCELL_16_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1032:1032]	1'h0	INIT[106]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_16_CONFIG	MSS_IOMUXSEL4MID	INIT[1033:1033]	1'h0	INIT[106]	1
IOMUXCELL_16_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1034:1034]	1'h0	INIT[106]	1
IOMUXCELL_16_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1035:1035]	1'h0	INIT[106]	1
IOMUXCELL_16_CONFIG	MSS_IOMUXSEL5MID	INIT[1036:1036]	1'h0	INIT[106]	1
IOMUXCELL_16_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1037:1037]	1'h0	INIT[106]	1
IOMUXCELL_17_CONFIG	MSS_IOMUXSEL0	INIT[1038:1038]	1'h0	INIT[107]	1
IOMUXCELL_17_CONFIG	MSS_IOMUXSEL1	INIT[1039:1039]	1'h0	INIT[107]	1
IOMUXCELL_17_CONFIG	MSS_IOMUXSEL2	INIT[1040:1040]	1'h0	INIT[107]	1
IOMUXCELL_17_CONFIG	MSS_IOMUXSEL3	INIT[1041:1041]	1'h0	INIT[107]	1
IOMUXCELL_17_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1042:1042]	1'h0	INIT[107]	1
IOMUXCELL_17_CONFIG	MSS_IOMUXSEL4MID	INIT[1043:1043]	1'h0	INIT[107]	1
IOMUXCELL_17_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1044:1044]	1'h0	INIT[107]	1
IOMUXCELL_17_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1045:1045]	1'h0	INIT[107]	1
IOMUXCELL_17_CONFIG	MSS_IOMUXSEL5MID	INIT[1046:1046]	1'h0	INIT[107]	1
IOMUXCELL_17_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1047:1047]	1'h0	INIT[107]	1
IOMUXCELL_18_CONFIG	MSS_IOMUXSEL0	INIT[1048:1048]	1'h0	INIT[108]	1
IOMUXCELL_18_CONFIG	MSS_IOMUXSEL1	INIT[1049:1049]	1'h0	INIT[108]	1
IOMUXCELL_18_CONFIG	MSS_IOMUXSEL2	INIT[1050:1050]	1'h0	INIT[108]	1
IOMUXCELL_18_CONFIG	MSS_IOMUXSEL3	INIT[1051:1051]	1'h0	INIT[108]	1
IOMUXCELL_18_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1052:1052]	1'h0	INIT[108]	1
IOMUXCELL_18_CONFIG	MSS_IOMUXSEL4MID	INIT[1053:1053]	1'h0	INIT[108]	1
IOMUXCELL_18_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1054:1054]	1'h0	INIT[108]	1
IOMUXCELL_18_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1055:1055]	1'h0	INIT[108]	1
IOMUXCELL_18_CONFIG	MSS_IOMUXSEL5MID	INIT[1056:1056]	1'h0	INIT[108]	1
IOMUXCELL_18_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1057:1057]	1'h0	INIT[108]	1
IOMUXCELL_19_CONFIG	MSS_IOMUXSEL0	INIT[1058:1058]	1'h0	INIT[109]	1
IOMUXCELL_19_CONFIG	MSS_IOMUXSEL1	INIT[1059:1059]	1'h0	INIT[109]	1
IOMUXCELL_19_CONFIG	MSS_IOMUXSEL2	INIT[1060:1060]	1'h0	INIT[109]	1
IOMUXCELL_19_CONFIG	MSS_IOMUXSEL3	INIT[1061:1061]	1'h0	INIT[109]	1
IOMUXCELL_19_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1062:1062]	1'h0	INIT[109]	1
IOMUXCELL_19_CONFIG	MSS_IOMUXSEL4MID	INIT[1063:1063]	1'h0	INIT[109]	1
IOMUXCELL_19_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1064:1064]	1'h0	INIT[109]	1
IOMUXCELL_19_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1065:1065]	1'h0	INIT[109]	1
IOMUXCELL_19_CONFIG	MSS_IOMUXSEL5MID	INIT[1066:1066]	1'h0	INIT[109]	1
IOMUXCELL_19_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1067:1067]	1'h0	INIT[109]	1
IOMUXCELL_20_CONFIG	MSS_IOMUXSEL0	INIT[1068:1068]	1'h0	INIT[110]	1
IOMUXCELL_20_CONFIG	MSS_IOMUXSEL1	INIT[1069:1069]	1'h0	INIT[110]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_20_CONFIG	MSS_IOMUXSEL2	INIT[1070:1070]	1'h0	INIT[110]	1
IOMUXCELL_20_CONFIG	MSS_IOMUXSEL3	INIT[1071:1071]	1'h0	INIT[110]	1
IOMUXCELL_20_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1072:1072]	1'h0	INIT[110]	1
IOMUXCELL_20_CONFIG	MSS_IOMUXSEL4MID	INIT[1073:1073]	1'h0	INIT[110]	1
IOMUXCELL_20_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1074:1074]	1'h0	INIT[110]	1
IOMUXCELL_20_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1075:1075]	1'h0	INIT[110]	1
IOMUXCELL_20_CONFIG	MSS_IOMUXSEL5MID	INIT[1076:1076]	1'h0	INIT[110]	1
IOMUXCELL_20_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1077:1077]	1'h0	INIT[110]	1
IOMUXCELL_21_CONFIG	MSS_IOMUXSEL0	INIT[1078:1078]	1'h0	INIT[111]	1
IOMUXCELL_21_CONFIG	MSS_IOMUXSEL1	INIT[1079:1079]	1'h0	INIT[111]	1
IOMUXCELL_21_CONFIG	MSS_IOMUXSEL2	INIT[1080:1080]	1'h0	INIT[111]	1
IOMUXCELL_21_CONFIG	MSS_IOMUXSEL3	INIT[1081:1081]	1'h0	INIT[111]	1
IOMUXCELL_21_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1082:1082]	1'h0	INIT[111]	1
IOMUXCELL_21_CONFIG	MSS_IOMUXSEL4MID	INIT[1083:1083]	1'h0	INIT[111]	1
IOMUXCELL_21_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1084:1084]	1'h0	INIT[111]	1
IOMUXCELL_21_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1085:1085]	1'h0	INIT[111]	1
IOMUXCELL_21_CONFIG	MSS_IOMUXSEL5MID	INIT[1086:1086]	1'h0	INIT[111]	1
IOMUXCELL_21_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1087:1087]	1'h0	INIT[111]	1
IOMUXCELL_22_CONFIG	MSS_IOMUXSEL0	INIT[1088:1088]	1'h0	INIT[112]	1
IOMUXCELL_22_CONFIG	MSS_IOMUXSEL1	INIT[1089:1089]	1'h0	INIT[112]	1
IOMUXCELL_22_CONFIG	MSS_IOMUXSEL2	INIT[1090:1090]	1'h0	INIT[112]	1
IOMUXCELL_22_CONFIG	MSS_IOMUXSEL3	INIT[1091:1091]	1'h0	INIT[112]	1
IOMUXCELL_22_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1092:1092]	1'h0	INIT[112]	1
IOMUXCELL_22_CONFIG	MSS_IOMUXSEL4MID	INIT[1093:1093]	1'h0	INIT[112]	1
IOMUXCELL_22_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1094:1094]	1'h0	INIT[112]	1
IOMUXCELL_22_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1095:1095]	1'h0	INIT[112]	1
IOMUXCELL_22_CONFIG	MSS_IOMUXSEL5MID	INIT[1096:1096]	1'h0	INIT[112]	1
IOMUXCELL_22_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1097:1097]	1'h0	INIT[112]	1
IOMUXCELL_23_CONFIG	MSS_IOMUXSEL0	INIT[1098:1098]	1'h0	INIT[113]	1
IOMUXCELL_23_CONFIG	MSS_IOMUXSEL1	INIT[1099:1099]	1'h0	INIT[113]	1
IOMUXCELL_23_CONFIG	MSS_IOMUXSEL2	INIT[1100:1100]	1'h0	INIT[113]	1
IOMUXCELL_23_CONFIG	MSS_IOMUXSEL3	INIT[1101:1101]	1'h0	INIT[113]	1
IOMUXCELL_23_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1102:1102]	1'h0	INIT[113]	1
IOMUXCELL_23_CONFIG	MSS_IOMUXSEL4MID	INIT[1103:1103]	1'h0	INIT[113]	1
IOMUXCELL_23_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1104:1104]	1'h0	INIT[113]	1
IOMUXCELL_23_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1105:1105]	1'h0	INIT[113]	1
IOMUXCELL_23_CONFIG	MSS_IOMUXSEL5MID	INIT[1106:1106]	1'h0	INIT[113]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_23_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1107:1107]	1'h0	INIT[113]	1
IOMUXCELL_24_CONFIG	MSS_IOMUXSEL0	INIT[1108:1108]	1'h0	INIT[114]	1
IOMUXCELL_24_CONFIG	MSS_IOMUXSEL1	INIT[1109:1109]	1'h0	INIT[114]	1
IOMUXCELL_24_CONFIG	MSS_IOMUXSEL2	INIT[1110:1110]	1'h0	INIT[114]	1
IOMUXCELL_24_CONFIG	MSS_IOMUXSEL3	INIT[1111:1111]	1'h0	INIT[114]	1
IOMUXCELL_24_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1112:1112]	1'h0	INIT[114]	1
IOMUXCELL_24_CONFIG	MSS_IOMUXSEL4MID	INIT[1113:1113]	1'h0	INIT[114]	1
IOMUXCELL_24_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1114:1114]	1'h0	INIT[114]	1
IOMUXCELL_24_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1115:1115]	1'h0	INIT[114]	1
IOMUXCELL_24_CONFIG	MSS_IOMUXSEL5MID	INIT[1116:1116]	1'h0	INIT[114]	1
IOMUXCELL_24_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1117:1117]	1'h0	INIT[114]	1
IOMUXCELL_25_CONFIG	MSS_IOMUXSEL0	INIT[1118:1118]	1'h0	INIT[115]	1
IOMUXCELL_25_CONFIG	MSS_IOMUXSEL1	INIT[1119:1119]	1'h0	INIT[115]	1
IOMUXCELL_25_CONFIG	MSS_IOMUXSEL2	INIT[1120:1120]	1'h0	INIT[115]	1
IOMUXCELL_25_CONFIG	MSS_IOMUXSEL3	INIT[1121:1121]	1'h0	INIT[115]	1
IOMUXCELL_25_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1122:1122]	1'h0	INIT[115]	1
IOMUXCELL_25_CONFIG	MSS_IOMUXSEL4MID	INIT[1123:1123]	1'h0	INIT[115]	1
IOMUXCELL_25_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1124:1124]	1'h0	INIT[115]	1
IOMUXCELL_25_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1125:1125]	1'h0	INIT[115]	1
IOMUXCELL_25_CONFIG	MSS_IOMUXSEL5MID	INIT[1126:1126]	1'h0	INIT[115]	1
IOMUXCELL_25_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1127:1127]	1'h0	INIT[115]	1
IOMUXCELL_26_CONFIG	MSS_IOMUXSEL0	INIT[1128:1128]	1'h0	INIT[116]	1
IOMUXCELL_26_CONFIG	MSS_IOMUXSEL1	INIT[1129:1129]	1'h0	INIT[116]	1
IOMUXCELL_26_CONFIG	MSS_IOMUXSEL2	INIT[1130:1130]	1'h0	INIT[116]	1
IOMUXCELL_26_CONFIG	MSS_IOMUXSEL3	INIT[1131:1131]	1'h0	INIT[116]	1
IOMUXCELL_26_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1132:1132]	1'h0	INIT[116]	1
IOMUXCELL_26_CONFIG	MSS_IOMUXSEL4MID	INIT[1133:1133]	1'h0	INIT[116]	1
IOMUXCELL_26_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1134:1134]	1'h0	INIT[116]	1
IOMUXCELL_26_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1135:1135]	1'h0	INIT[116]	1
IOMUXCELL_26_CONFIG	MSS_IOMUXSEL5MID	INIT[1136:1136]	1'h0	INIT[116]	1
IOMUXCELL_26_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1137:1137]	1'h0	INIT[116]	1
IOMUXCELL_27_CONFIG	MSS_IOMUXSEL0	INIT[1138:1138]	1'h0	INIT[117]	1
IOMUXCELL_27_CONFIG	MSS_IOMUXSEL1	INIT[1139:1139]	1'h0	INIT[117]	1
IOMUXCELL_27_CONFIG	MSS_IOMUXSEL2	INIT[1140:1140]	1'h0	INIT[117]	1
IOMUXCELL_27_CONFIG	MSS_IOMUXSEL3	INIT[1141:1141]	1'h0	INIT[117]	1
IOMUXCELL_27_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1142:1142]	1'h0	INIT[117]	1
IOMUXCELL_27_CONFIG	MSS_IOMUXSEL4MID	INIT[1143:1143]	1'h0	INIT[117]	1

Table 17 • **HPMS/MDDR (Unused) *(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_27_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1144:1144]	1'h0	INIT[117]	1
IOMUXCELL_27_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1145:1145]	1'h0	INIT[117]	1
IOMUXCELL_27_CONFIG	MSS_IOMUXSEL5MID	INIT[1146:1146]	1'h0	INIT[117]	1
IOMUXCELL_27_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1147:1147]	1'h0	INIT[117]	1
IOMUXCELL_28_CONFIG	MSS_IOMUXSEL0	INIT[1148:1148]	1'h0	INIT[118]	1
IOMUXCELL_28_CONFIG	MSS_IOMUXSEL1	INIT[1149:1149]	1'h0	INIT[118]	1
IOMUXCELL_28_CONFIG	MSS_IOMUXSEL2	INIT[1150:1150]	1'h0	INIT[118]	1
IOMUXCELL_28_CONFIG	MSS_IOMUXSEL3	INIT[1151:1151]	1'h0	INIT[118]	1
IOMUXCELL_28_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1152:1152]	1'h0	INIT[118]	1
IOMUXCELL_28_CONFIG	MSS_IOMUXSEL4MID	INIT[1153:1153]	1'h0	INIT[118]	1
IOMUXCELL_28_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1154:1154]	1'h0	INIT[118]	1
IOMUXCELL_28_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1155:1155]	1'h0	INIT[118]	1
IOMUXCELL_28_CONFIG	MSS_IOMUXSEL5MID	INIT[1156:1156]	1'h0	INIT[118]	1
IOMUXCELL_28_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1157:1157]	1'h0	INIT[118]	1
IOMUXCELL_29_CONFIG	MSS_IOMUXSEL0	INIT[1158:1158]	1'h0	INIT[119]	1
IOMUXCELL_29_CONFIG	MSS_IOMUXSEL1	INIT[1159:1159]	1'h0	INIT[119]	1
IOMUXCELL_29_CONFIG	MSS_IOMUXSEL2	INIT[1160:1160]	1'h0	INIT[119]	1
IOMUXCELL_29_CONFIG	MSS_IOMUXSEL3	INIT[1161:1161]	1'h0	INIT[119]	1
IOMUXCELL_29_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1162:1162]	1'h0	INIT[119]	1
IOMUXCELL_29_CONFIG	MSS_IOMUXSEL4MID	INIT[1163:1163]	1'h0	INIT[119]	1
IOMUXCELL_29_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1164:1164]	1'h0	INIT[119]	1
IOMUXCELL_29_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1165:1165]	1'h0	INIT[119]	1
IOMUXCELL_29_CONFIG	MSS_IOMUXSEL5MID	INIT[1166:1166]	1'h0	INIT[119]	1
IOMUXCELL_29_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1167:1167]	1'h0	INIT[119]	1
IOMUXCELL_30_CONFIG	MSS_IOMUXSEL0	INIT[1168:1168]	1'h0	INIT[120]	1
IOMUXCELL_30_CONFIG	MSS_IOMUXSEL1	INIT[1169:1169]	1'h0	INIT[120]	1
IOMUXCELL_30_CONFIG	MSS_IOMUXSEL2	INIT[1170:1170]	1'h0	INIT[120]	1
IOMUXCELL_30_CONFIG	MSS_IOMUXSEL3	INIT[1171:1171]	1'h0	INIT[120]	1
IOMUXCELL_30_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1172:1172]	1'h0	INIT[120]	1
IOMUXCELL_30_CONFIG	MSS_IOMUXSEL4MID	INIT[1173:1173]	1'h0	INIT[120]	1
IOMUXCELL_30_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1174:1174]	1'h0	INIT[120]	1
IOMUXCELL_30_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1175:1175]	1'h0	INIT[120]	1
IOMUXCELL_30_CONFIG	MSS_IOMUXSEL5MID	INIT[1176:1176]	1'h0	INIT[120]	1
IOMUXCELL_30_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1177:1177]	1'h0	INIT[120]	1
IOMUXCELL_31_CONFIG	MSS_IOMUXSEL0	INIT[1178:1178]	1'h0	INIT[121]	1
IOMUXCELL_31_CONFIG	MSS_IOMUXSEL1	INIT[1179:1179]	1'h0	INIT[121]	1
IOMUXCELL_31_CONFIG	MSS_IOMUXSEL2	INIT[1180:1180]	1'h0	INIT[121]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_31_CONFIG	MSS_IOMUXSEL3	INIT[1181:1181]	1'h0	INIT[121]	1
IOMUXCELL_31_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1182:1182]	1'h0	INIT[121]	1
IOMUXCELL_31_CONFIG	MSS_IOMUXSEL4MID	INIT[1183:1183]	1'h0	INIT[121]	1
IOMUXCELL_31_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1184:1184]	1'h0	INIT[121]	1
IOMUXCELL_31_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1185:1185]	1'h0	INIT[121]	1
IOMUXCELL_31_CONFIG	MSS_IOMUXSEL5MID	INIT[1186:1186]	1'h0	INIT[121]	1
IOMUXCELL_31_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1187:1187]	1'h0	INIT[121]	1
IOMUXCELL_32_CONFIG	MSS_IOMUXSEL0	INIT[1188:1188]	1'h0	INIT[122]	1
IOMUXCELL_32_CONFIG	MSS_IOMUXSEL1	INIT[1189:1189]	1'h0	INIT[122]	1
IOMUXCELL_32_CONFIG	MSS_IOMUXSEL2	INIT[1190:1190]	1'h0	INIT[122]	1
IOMUXCELL_32_CONFIG	MSS_IOMUXSEL3	INIT[1191:1191]	1'h0	INIT[122]	1
IOMUXCELL_32_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1192:1192]	1'h0	INIT[122]	1
IOMUXCELL_32_CONFIG	MSS_IOMUXSEL4MID	INIT[1193:1193]	1'h0	INIT[122]	1
IOMUXCELL_32_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1194:1194]	1'h0	INIT[122]	1
IOMUXCELL_32_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1195:1195]	1'h0	INIT[122]	1
IOMUXCELL_32_CONFIG	MSS_IOMUXSEL5MID	INIT[1196:1196]	1'h0	INIT[122]	1
IOMUXCELL_32_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1197:1197]	1'h0	INIT[122]	1
IOMUXCELL_33_CONFIG	MSS_IOMUXSEL0	INIT[1198:1198]	1'h0	INIT[123]	1
IOMUXCELL_33_CONFIG	MSS_IOMUXSEL1	INIT[1199:1199]	1'h0	INIT[123]	1
IOMUXCELL_33_CONFIG	MSS_IOMUXSEL2	INIT[1200:1200]	1'h0	INIT[123]	1
IOMUXCELL_33_CONFIG	MSS_IOMUXSEL3	INIT[1201:1201]	1'h0	INIT[123]	1
IOMUXCELL_33_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1202:1202]	1'h0	INIT[123]	1
IOMUXCELL_33_CONFIG	MSS_IOMUXSEL4MID	INIT[1203:1203]	1'h0	INIT[123]	1
IOMUXCELL_33_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1204:1204]	1'h0	INIT[123]	1
IOMUXCELL_33_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1205:1205]	1'h0	INIT[123]	1
IOMUXCELL_33_CONFIG	MSS_IOMUXSEL5MID	INIT[1206:1206]	1'h0	INIT[123]	1
IOMUXCELL_33_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1207:1207]	1'h0	INIT[123]	1
IOMUXCELL_34_CONFIG	MSS_IOMUXSEL0	INIT[1208:1208]	1'h0	INIT[124]	1
IOMUXCELL_34_CONFIG	MSS_IOMUXSEL1	INIT[1209:1209]	1'h0	INIT[124]	1
IOMUXCELL_34_CONFIG	MSS_IOMUXSEL2	INIT[1210:1210]	1'h0	INIT[124]	1
IOMUXCELL_34_CONFIG	MSS_IOMUXSEL3	INIT[1211:1211]	1'h0	INIT[124]	1
IOMUXCELL_34_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1212:1212]	1'h0	INIT[124]	1
IOMUXCELL_34_CONFIG	MSS_IOMUXSEL4MID	INIT[1213:1213]	1'h0	INIT[124]	1
IOMUXCELL_34_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1214:1214]	1'h0	INIT[124]	1
IOMUXCELL_34_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1215:1215]	1'h0	INIT[124]	1
IOMUXCELL_34_CONFIG	MSS_IOMUXSEL5MID	INIT[1216:1216]	1'h0	INIT[124]	1
IOMUXCELL_34_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1217:1217]	1'h0	INIT[124]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_35_CONFIG	MSS_IOMUXSEL0	INIT[1218:1218]	1'h0	INIT[125]	1
IOMUXCELL_35_CONFIG	MSS_IOMUXSEL1	INIT[1219:1219]	1'h0	INIT[125]	1
IOMUXCELL_35_CONFIG	MSS_IOMUXSEL2	INIT[1220:1220]	1'h0	INIT[125]	1
IOMUXCELL_35_CONFIG	MSS_IOMUXSEL3	INIT[1221:1221]	1'h0	INIT[125]	1
IOMUXCELL_35_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1222:1222]	1'h0	INIT[125]	1
IOMUXCELL_35_CONFIG	MSS_IOMUXSEL4MID	INIT[1223:1223]	1'h0	INIT[125]	1
IOMUXCELL_35_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1224:1224]	1'h0	INIT[125]	1
IOMUXCELL_35_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1225:1225]	1'h0	INIT[125]	1
IOMUXCELL_35_CONFIG	MSS_IOMUXSEL5MID	INIT[1226:1226]	1'h0	INIT[125]	1
IOMUXCELL_35_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1227:1227]	1'h0	INIT[125]	1
IOMUXCELL_36_CONFIG	MSS_IOMUXSEL0	INIT[1228:1228]	1'h0	INIT[126]	1
IOMUXCELL_36_CONFIG	MSS_IOMUXSEL1	INIT[1229:1229]	1'h0	INIT[126]	1
IOMUXCELL_36_CONFIG	MSS_IOMUXSEL2	INIT[1230:1230]	1'h0	INIT[126]	1
IOMUXCELL_36_CONFIG	MSS_IOMUXSEL3	INIT[1231:1231]	1'h0	INIT[126]	1
IOMUXCELL_36_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1232:1232]	1'h0	INIT[126]	1
IOMUXCELL_36_CONFIG	MSS_IOMUXSEL4MID	INIT[1233:1233]	1'h0	INIT[126]	1
IOMUXCELL_36_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1234:1234]	1'h0	INIT[126]	1
IOMUXCELL_36_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1235:1235]	1'h0	INIT[126]	1
IOMUXCELL_36_CONFIG	MSS_IOMUXSEL5MID	INIT[1236:1236]	1'h0	INIT[126]	1
IOMUXCELL_36_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1237:1237]	1'h0	INIT[126]	1
IOMUXCELL_37_CONFIG	MSS_IOMUXSEL0	INIT[1238:1238]	1'h0	INIT[127]	1
IOMUXCELL_37_CONFIG	MSS_IOMUXSEL1	INIT[1239:1239]	1'h0	INIT[127]	1
IOMUXCELL_37_CONFIG	MSS_IOMUXSEL2	INIT[1240:1240]	1'h0	INIT[127]	1
IOMUXCELL_37_CONFIG	MSS_IOMUXSEL3	INIT[1241:1241]	1'h0	INIT[127]	1
IOMUXCELL_37_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1242:1242]	1'h0	INIT[127]	1
IOMUXCELL_37_CONFIG	MSS_IOMUXSEL4MID	INIT[1243:1243]	1'h0	INIT[127]	1
IOMUXCELL_37_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1244:1244]	1'h0	INIT[127]	1
IOMUXCELL_37_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1245:1245]	1'h0	INIT[127]	1
IOMUXCELL_37_CONFIG	MSS_IOMUXSEL5MID	INIT[1246:1246]	1'h0	INIT[127]	1
IOMUXCELL_37_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1247:1247]	1'h0	INIT[127]	1
IOMUXCELL_38_CONFIG	MSS_IOMUXSEL0	INIT[1248:1248]	1'h0	INIT[128]	1
IOMUXCELL_38_CONFIG	MSS_IOMUXSEL1	INIT[1249:1249]	1'h0	INIT[128]	1
IOMUXCELL_38_CONFIG	MSS_IOMUXSEL2	INIT[1250:1250]	1'h0	INIT[128]	1
IOMUXCELL_38_CONFIG	MSS_IOMUXSEL3	INIT[1251:1251]	1'h0	INIT[128]	1
IOMUXCELL_38_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1252:1252]	1'h0	INIT[128]	1
IOMUXCELL_38_CONFIG	MSS_IOMUXSEL4MID	INIT[1253:1253]	1'h0	INIT[128]	1
IOMUXCELL_38_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1254:1254]	1'h0	INIT[128]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_38_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1255:1255]	1'h0	INIT[128]	1
IOMUXCELL_38_CONFIG	MSS_IOMUXSEL5MID	INIT[1256:1256]	1'h0	INIT[128]	1
IOMUXCELL_38_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1257:1257]	1'h0	INIT[128]	1
IOMUXCELL_39_CONFIG	MSS_IOMUXSEL0	INIT[1258:1258]	1'h0	INIT[129]	1
IOMUXCELL_39_CONFIG	MSS_IOMUXSEL1	INIT[1259:1259]	1'h0	INIT[129]	1
IOMUXCELL_39_CONFIG	MSS_IOMUXSEL2	INIT[1260:1260]	1'h0	INIT[129]	1
IOMUXCELL_39_CONFIG	MSS_IOMUXSEL3	INIT[1261:1261]	1'h0	INIT[129]	1
IOMUXCELL_39_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1262:1262]	1'h0	INIT[129]	1
IOMUXCELL_39_CONFIG	MSS_IOMUXSEL4MID	INIT[1263:1263]	1'h0	INIT[129]	1
IOMUXCELL_39_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1264:1264]	1'h0	INIT[129]	1
IOMUXCELL_39_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1265:1265]	1'h0	INIT[129]	1
IOMUXCELL_39_CONFIG	MSS_IOMUXSEL5MID	INIT[1266:1266]	1'h0	INIT[129]	1
IOMUXCELL_39_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1267:1267]	1'h0	INIT[129]	1
IOMUXCELL_40_CONFIG	MSS_IOMUXSEL0	INIT[1268:1268]	1'h0	INIT[130]	1
IOMUXCELL_40_CONFIG	MSS_IOMUXSEL1	INIT[1269:1269]	1'h0	INIT[130]	1
IOMUXCELL_40_CONFIG	MSS_IOMUXSEL2	INIT[1270:1270]	1'h0	INIT[130]	1
IOMUXCELL_40_CONFIG	MSS_IOMUXSEL3	INIT[1271:1271]	1'h0	INIT[130]	1
IOMUXCELL_40_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1272:1272]	1'h0	INIT[130]	1
IOMUXCELL_40_CONFIG	MSS_IOMUXSEL4MID	INIT[1273:1273]	1'h0	INIT[130]	1
IOMUXCELL_40_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1274:1274]	1'h0	INIT[130]	1
IOMUXCELL_40_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1275:1275]	1'h0	INIT[130]	1
IOMUXCELL_40_CONFIG	MSS_IOMUXSEL5MID	INIT[1276:1276]	1'h0	INIT[130]	1
IOMUXCELL_40_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1277:1277]	1'h0	INIT[130]	1
IOMUXCELL_41_CONFIG	MSS_IOMUXSEL0	INIT[1278:1278]	1'h0	INIT[131]	1
IOMUXCELL_41_CONFIG	MSS_IOMUXSEL1	INIT[1279:1279]	1'h0	INIT[131]	
IOMUXCELL_41_CONFIG	MSS_IOMUXSEL2	INIT[1280:1280]	1'h0	INIT[131]	1
IOMUXCELL_41_CONFIG	MSS_IOMUXSEL3	INIT[1281:1281]	1'h0	INIT[131]	1
IOMUXCELL_41_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1282:1282]	1'h0	INIT[131]	1
IOMUXCELL_41_CONFIG	MSS_IOMUXSEL4MID	INIT[1283:1283]	1'h0	INIT[131]	1
IOMUXCELL_41_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1284:1284]	1'h0	INIT[131]	1
IOMUXCELL_41_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1285:1285]	1'h0	INIT[131]	1
IOMUXCELL_41_CONFIG	MSS_IOMUXSEL5MID	INIT[1286:1286]	1'h0	INIT[131]	1
IOMUXCELL_41_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1287:1287]	1'h0	INIT[131]	1
IOMUXCELL_42_CONFIG	MSS_IOMUXSEL0	INIT[1288:1288]	1'h0	INIT[132]	1
IOMUXCELL_42_CONFIG	MSS_IOMUXSEL1	INIT[1289:1289]	1'h0	INIT[132]	1
IOMUXCELL_42_CONFIG	MSS_IOMUXSEL2	INIT[1290:1290]	1'h0	INIT[132]	1
IOMUXCELL_42_CONFIG	MSS_IOMUXSEL3	INIT[1291:1291]	1'h0	INIT[132]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_42_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1292:1292]	1'h0	INIT[132]	1
IOMUXCELL_42_CONFIG	MSS_IOMUXSEL4MID	INIT[1293:1293]	1'h0	INIT[132]	1
IOMUXCELL_42_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1294:1294]	1'h0	INIT[132]	1
IOMUXCELL_42_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1295:1295]	1'h0	INIT[132]	1
IOMUXCELL_42_CONFIG	MSS_IOMUXSEL5MID	INIT[1296:1296]	1'h0	INIT[132]	1
IOMUXCELL_42_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1297:1297]	1'h0	INIT[132]	1
IOMUXCELL_43_CONFIG	MSS_IOMUXSEL0	INIT[1298:1298]	1'h0	INIT[133]	1
IOMUXCELL_43_CONFIG	MSS_IOMUXSEL1	INIT[1299:1299]	1'h0	INIT[133]	1
IOMUXCELL_43_CONFIG	MSS_IOMUXSEL2	INIT[1300:1300]	1'h0	INIT[133]	1
IOMUXCELL_43_CONFIG	MSS_IOMUXSEL3	INIT[1301:1301]	1'h0	INIT[133]	1
IOMUXCELL_43_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1302:1302]	1'h0	INIT[133]	1
IOMUXCELL_43_CONFIG	MSS_IOMUXSEL4MID	INIT[1303:1303]	1'h0	INIT[133]	1
IOMUXCELL_43_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1304:1304]	1'h0	INIT[133]	1
IOMUXCELL_43_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1305:1305]	1'h0	INIT[133]	1
IOMUXCELL_43_CONFIG	MSS_IOMUXSEL5MID	INIT[1306:1306]	1'h0	INIT[133]	1
IOMUXCELL_43_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1307:1307]	1'h0	INIT[133]	1
IOMUXCELL_44_CONFIG	MSS_IOMUXSEL0	INIT[1308:1308]	1'h0	INIT[134]	1
IOMUXCELL_44_CONFIG	MSS_IOMUXSEL1	INIT[1309:1309]	1'h0	INIT[134]	1
IOMUXCELL_44_CONFIG	MSS_IOMUXSEL2	INIT[1310:1310]	1'h0	INIT[134]	1
IOMUXCELL_44_CONFIG	MSS_IOMUXSEL3	INIT[1311:1311]	1'h0	INIT[134]	1
IOMUXCELL_44_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1312:1312]	1'h0	INIT[134]	1
IOMUXCELL_44_CONFIG	MSS_IOMUXSEL4MID	INIT[1313:1313]	1'h0	INIT[134]	1
IOMUXCELL_44_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1314:1314]	1'h0	INIT[134]	1
IOMUXCELL_44_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1315:1315]	1'h0	INIT[134]	1
IOMUXCELL_44_CONFIG	MSS_IOMUXSEL5MID	INIT[1316:1316]	1'h0	INIT[134]	1
IOMUXCELL_44_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1317:1317]	1'h0	INIT[134]	1
IOMUXCELL_45_CONFIG	MSS_IOMUXSEL0	INIT[1318:1318]	1'h0	INIT[135]	1
IOMUXCELL_45_CONFIG	MSS_IOMUXSEL1	INIT[1319:1319]	1'h0	INIT[135]	1
IOMUXCELL_45_CONFIG	MSS_IOMUXSEL2	INIT[1320:1320]	1'h0	INIT[135]	1
IOMUXCELL_45_CONFIG	MSS_IOMUXSEL3	INIT[1321:1321]	1'h0	INIT[135]	1
IOMUXCELL_45_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1322:1322]	1'h0	INIT[135]	1
IOMUXCELL_45_CONFIG	MSS_IOMUXSEL4MID	INIT[1323:1323]	1'h0	INIT[135]	1
IOMUXCELL_45_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1324:1324]	1'h0	INIT[135]	1
IOMUXCELL_45_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1325:1325]	1'h0	INIT[135]	1
IOMUXCELL_45_CONFIG	MSS_IOMUXSEL5MID	INIT[1326:1326]	1'h0	INIT[135]	1
IOMUXCELL_45_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1327:1327]	1'h0	INIT[135]	1
IOMUXCELL_46_CONFIG	MSS_IOMUXSEL0	INIT[1328:1328]	1'h0	INIT[136]	1

Table 17 • **HPMS/MDDR (Unused) *(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_46_CONFIG	MSS_IOMUXSEL1	INIT[1329:1329]	1'h0	INIT[136]	1
IOMUXCELL_46_CONFIG	MSS_IOMUXSEL2	INIT[1330:1330]	1'h0	INIT[136]	1
IOMUXCELL_46_CONFIG	MSS_IOMUXSEL3	INIT[1331:1331]	1'h0	INIT[136]	1
IOMUXCELL_46_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1332:1332]	1'h0	INIT[136]	1
IOMUXCELL_46_CONFIG	MSS_IOMUXSEL4MID	INIT[1333:1333]	1'h0	INIT[136]	1
IOMUXCELL_46_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1334:1334]	1'h0	INIT[136]	1
IOMUXCELL_46_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1335:1335]	1'h0	INIT[136]	1
IOMUXCELL_46_CONFIG	MSS_IOMUXSEL5MID	INIT[1336:1336]	1'h0	INIT[136]	1
IOMUXCELL_46_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1337:1337]	1'h0	INIT[136]	1
IOMUXCELL_47_CONFIG	MSS_IOMUXSEL0	INIT[1338:1338]	1'h0	INIT[137]	1
IOMUXCELL_47_CONFIG	MSS_IOMUXSEL1	INIT[1339:1339]	1'h0	INIT[137]	1
IOMUXCELL_47_CONFIG	MSS_IOMUXSEL2	INIT[1340:1340]	1'h0	INIT[137]	1
IOMUXCELL_47_CONFIG	MSS_IOMUXSEL3	INIT[1341:1341]	1'h0	INIT[137]	1
IOMUXCELL_47_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1342:1342]	1'h0	INIT[137]	1
IOMUXCELL_47_CONFIG	MSS_IOMUXSEL4MID	INIT[1343:1343]	1'h0	INIT[137]	1
IOMUXCELL_47_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1344:1344]	1'h0	INIT[137]	1
IOMUXCELL_47_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1345:1345]	1'h0	INIT[137]	1
IOMUXCELL_47_CONFIG	MSS_IOMUXSEL5MID	INIT[1346:1346]	1'h0	INIT[137]	1
IOMUXCELL_47_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1347:1347]	1'h0	INIT[137]	1
IOMUXCELL_48_CONFIG	MSS_IOMUXSEL0	INIT[1348:1348]	1'h0	INIT[138]	1
IOMUXCELL_48_CONFIG	MSS_IOMUXSEL1	INIT[1349:1349]	1'h0	INIT[138]	1
IOMUXCELL_48_CONFIG	MSS_IOMUXSEL2	INIT[1350:1350]	1'h0	INIT[138]	1
IOMUXCELL_48_CONFIG	MSS_IOMUXSEL3	INIT[1351:1351]	1'h0	INIT[138]	1
IOMUXCELL_48_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1352:1352]	1'h0	INIT[138]	1
IOMUXCELL_48_CONFIG	MSS_IOMUXSEL4MID	INIT[1353:1353]	1'h0	INIT[138]	1
IOMUXCELL_48_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1354:1354]	1'h0	INIT[138]	1
IOMUXCELL_48_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1355:1355]	1'h0	INIT[138]	1
IOMUXCELL_48_CONFIG	MSS_IOMUXSEL5MID	INIT[1356:1356]	1'h0	INIT[138]	1
IOMUXCELL_48_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1357:1357]	1'h0	INIT[138]	1
IOMUXCELL_49_CONFIG	MSS_IOMUXSEL0	INIT[1358:1358]	1'h0	INIT[139]	1
IOMUXCELL_49_CONFIG	MSS_IOMUXSEL1	INIT[1359:1359]	1'h0	INIT[139]	1
IOMUXCELL_49_CONFIG	MSS_IOMUXSEL2	INIT[1360:1360]	1'h0	INIT[139]	1
IOMUXCELL_49_CONFIG	MSS_IOMUXSEL3	INIT[1361:1361]	1'h0	INIT[139]	1
IOMUXCELL_49_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1362:1362]	1'h0	INIT[139]	1
IOMUXCELL_49_CONFIG	MSS_IOMUXSEL4MID	INIT[1363:1363]	1'h0	INIT[139]	1
IOMUXCELL_49_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1364:1364]	1'h0	INIT[139]	1
IOMUXCELL_49_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1365:1365]	1'h0	INIT[139]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_49_CONFIG	MSS_IOMUXSEL5MID	INIT[1366:1366]	1'h0	INIT[139]	1
IOMUXCELL_49_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1367:1367]	1'h0	INIT[139]	1
IOMUXCELL_50_CONFIG	MSS_IOMUXSEL0	INIT[1368:1368]	1'h0	INIT[140]	1
IOMUXCELL_50_CONFIG	MSS_IOMUXSEL1	INIT[1369:1369]	1'h0	INIT[140]	1
IOMUXCELL_50_CONFIG	MSS_IOMUXSEL2	INIT[1370:1370]	1'h0	INIT[140]	1
IOMUXCELL_50_CONFIG	MSS_IOMUXSEL3	INIT[1371:1371]	1'h0	INIT[140]	1
IOMUXCELL_50_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1372:1372]	1'h0	INIT[140]	1
IOMUXCELL_50_CONFIG	MSS_IOMUXSEL4MID	INIT[1373:1373]	1'h0	INIT[140]	1
IOMUXCELL_50_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1374:1374]	1'h0	INIT[140]	1
IOMUXCELL_50_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1375:1375]	1'h0	INIT[140]	1
IOMUXCELL_50_CONFIG	MSS_IOMUXSEL5MID	INIT[1376:1376]	1'h0	INIT[140]	1
IOMUXCELL_50_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1377:1377]	1'h0	INIT[140]	1
IOMUXCELL_51_CONFIG	MSS_IOMUXSEL0	INIT[1378:1378]	1'h0	INIT[141]	1
IOMUXCELL_51_CONFIG	MSS_IOMUXSEL1	INIT[1379:1379]	1'h0	INIT[141]	1
IOMUXCELL_51_CONFIG	MSS_IOMUXSEL2	INIT[1380:1380]	1'h0	INIT[141]	1
IOMUXCELL_51_CONFIG	MSS_IOMUXSEL3	INIT[1381:1381]	1'h0	INIT[141]	1
IOMUXCELL_51_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1382:1382]	1'h0	INIT[141]	1
IOMUXCELL_51_CONFIG	MSS_IOMUXSEL4MID	INIT[1383:1383]	1'h0	INIT[141]	1
IOMUXCELL_51_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1384:1384]	1'h0	INIT[141]	1
IOMUXCELL_51_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1385:1385]	1'h0	INIT[141]	1
IOMUXCELL_51_CONFIG	MSS_IOMUXSEL5MID	INIT[1386:1386]	1'h0	INIT[141]	1
IOMUXCELL_51_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1387:1387]	1'h0	INIT[141]	1
IOMUXCELL_52_CONFIG	MSS_IOMUXSEL0	INIT[1388:1388]	1'h0	INIT[142]	1
IOMUXCELL_52_CONFIG	MSS_IOMUXSEL1	INIT[1389:1389]	1'h0	INIT[142]	1
IOMUXCELL_52_CONFIG	MSS_IOMUXSEL2	INIT[1390:1390]	1'h0	INIT[142]	1
IOMUXCELL_52_CONFIG	MSS_IOMUXSEL3	INIT[1391:1391]	1'h0	INIT[142]	1
IOMUXCELL_52_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1392:1392]	1'h0	INIT[142]	1
IOMUXCELL_52_CONFIG	MSS_IOMUXSEL4MID	INIT[1393:1393]	1'h0	INIT[142]	1
IOMUXCELL_52_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1394:1394]	1'h0	INIT[142]	1
IOMUXCELL_52_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1395:1395]	1'h0	INIT[142]	1
IOMUXCELL_52_CONFIG	MSS_IOMUXSEL5MID	INIT[1396:1396]	1'h0	INIT[142]	1
IOMUXCELL_52_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1397:1397]	1'h0	INIT[142]	1
IOMUXCELL_53_CONFIG	MSS_IOMUXSEL0	INIT[1398:1398]	1'h0	INIT[143]	1
IOMUXCELL_53_CONFIG	MSS_IOMUXSEL1	INIT[1399:1399]	1'h0	INIT[143]	1
IOMUXCELL_53_CONFIG	MSS_IOMUXSEL2	INIT[1400:1400]	1'h0	INIT[143]	1
IOMUXCELL_53_CONFIG	MSS_IOMUXSEL3	INIT[1401:1401]	1'h0	INIT[143]	1
IOMUXCELL_53_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1402:1402]	1'h0	INIT[143]	1

Table 17 • **HPMS/MDDR (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
IOMUXCELL_53_CONFIG	MSS_IOMUXSEL4MID	INIT[1403:1403]	1'h0	INIT[143]	1
IOMUXCELL_53_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1404:1404]	1'h0	INIT[143]	1
IOMUXCELL_53_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1405:1405]	1'h0	INIT[143]	1
IOMUXCELL_53_CONFIG	MSS_IOMUXSEL5MID	INIT[1406:1406]	1'h0	INIT[143]	1
IOMUXCELL_53_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1407:1407]	1'h0	INIT[143]	1
IOMUXCELL_54_CONFIG	MSS_IOMUXSEL0	INIT[1408:1408]	1'h0	INIT[144]	1
IOMUXCELL_54_CONFIG	MSS_IOMUXSEL1	INIT[1409:1409]	1'h0	INIT[144]	1
IOMUXCELL_54_CONFIG	MSS_IOMUXSEL2	INIT[1410:1410]	1'h0	INIT[144]	1
IOMUXCELL_54_CONFIG	MSS_IOMUXSEL3	INIT[1411:1411]	1'h0	INIT[144]	1
IOMUXCELL_54_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1412:1412]	1'h0	INIT[144]	1
IOMUXCELL_54_CONFIG	MSS_IOMUXSEL4MID	INIT[1413:1413]	1'h0	INIT[144]	1
IOMUXCELL_54_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1414:1414]	1'h0	INIT[144]	1
IOMUXCELL_54_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1415:1415]	1'h0	INIT[144]	1
IOMUXCELL_54_CONFIG	MSS_IOMUXSEL5MID	INIT[1416:1416]	1'h0	INIT[144]	1
IOMUXCELL_54_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1417:1417]	1'h0	INIT[144]	1
IOMUXCELL_55_CONFIG	MSS_IOMUXSEL0	INIT[1418:1418]	1'h0	INIT[145]	1
IOMUXCELL_55_CONFIG	MSS_IOMUXSEL1	INIT[1419:1419]	1'h0	INIT[145]	1
IOMUXCELL_55_CONFIG	MSS_IOMUXSEL2	INIT[1420:1420]	1'h0	INIT[145]	1
IOMUXCELL_55_CONFIG	MSS_IOMUXSEL3	INIT[1421:1421]	1'h0	INIT[145]	1
IOMUXCELL_55_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1422:1422]	1'h0	INIT[145]	1
IOMUXCELL_55_CONFIG	MSS_IOMUXSEL4MID	INIT[1423:1423]	1'h0	INIT[145]	1
IOMUXCELL_55_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1424:1424]	1'h0	INIT[145]	1
IOMUXCELL_55_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1425:1425]	1'h0	INIT[145]	1
IOMUXCELL_55_CONFIG	MSS_IOMUXSEL5MID	INIT[1426:1426]	1'h0	INIT[145]	1
IOMUXCELL_55_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1427:1427]	1'h0	INIT[145]	1
IOMUXCELL_56_CONFIG	MSS_IOMUXSEL0	INIT[1428:1428]	1'h0	INIT[146]	1
IOMUXCELL_56_CONFIG	MSS_IOMUXSEL1	INIT[1429:1429]	1'h0	INIT[146]	1
IOMUXCELL_56_CONFIG	MSS_IOMUXSEL2	INIT[1430:1430]	1'h0	INIT[146]	1
IOMUXCELL_56_CONFIG	MSS_IOMUXSEL3	INIT[1431:1431]	1'h0	INIT[146]	1
IOMUXCELL_56_CONFIG	MSS_IOMUXSEL4UPPER	INIT[1432:1432]	1'h0	INIT[146]	1
IOMUXCELL_56_CONFIG	MSS_IOMUXSEL4MID	INIT[1433:1433]	1'h0	INIT[146]	1
IOMUXCELL_56_CONFIG	MSS_IOMUXSEL4LOWER	INIT[1434:1434]	1'h0	INIT[146]	1
IOMUXCELL_56_CONFIG	MSS_IOMUXSEL5UPPER	INIT[1435:1435]	1'h0	INIT[146]	1
IOMUXCELL_56_CONFIG	MSS_IOMUXSEL5MID	INIT[1436:1436]	1'h0	INIT[146]	1
IOMUXCELL_56_CONFIG	MSS_IOMUXSEL5LOWER	INIT[1437:1437]	1'h0	INIT[146]	1

Note: Lock Value (*) = 0, disables modification of the Register field.

Table 18 • **FDDR (Unused)**

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
PLL_CONFIG_LOW_1	PLL_REF_DIVISOR	INIT[33:28]	6'h1	INIT[0]	1
PLL_CONFIG_LOW_1	PLL_FEEDBACK_DIVISOR	INIT[43:34]	10'h2	INIT[1]	1
PLL_CONFIG_LOW_2	PLL_OUTPUT_DIVISOR	INIT[46:44]	3'h2	INIT[2]	1
PLL_CONFIG_LOW_2	PLL_RESET	INIT[47:47]	1'h1	INIT[3]	1
PLL_CONFIG_HIGH	PLL_FILTER_RANGE	INIT[51:48]	4'h9	INIT[4]	1
PLL_CONFIG_HIGH	PLL_LOCKWIN	INIT[54:52]	3'h0	INIT[5]	1
PLL_CONFIG_HIGH	PLL_LOCKCNT	INIT[58:55]	4'hF	INIT[6]	1
PLL_CONFIG_HIGH	PLL_BYPASS	INIT[59:59]	1'h1	INIT[7]	1
PLL_CONFIG_HIGH	PLL_MODE_1V2	INIT[60:60]	1'h1	INIT[8]	1
PLL_CONFIG_HIGH	PLL_MODE_3V3	INIT[61:61]	1'h0	INIT[9]	1
PLL_CONFIG_HIGH	PLL_FSE	INIT[62:62]	1'h0	INIT[10]	1
PLL_CONFIG_HIGH	PLL_PD	INIT[63:63]	1'h1	INIT[11]	1
FDDR_FACC_CLK_EN	DDR_CLK_EN	INIT[64:64]	1'h1	INIT[12]	1
FDDR_FACC_MUX_CONFIG	FACC_STANDBY_SEL	INIT[67:65]	3'h0	INIT[13]	1
FDDR_FACC_MUX_CONFIG	FACC_SRC_SEL	INIT[70:68]	3'h0	INIT[14]	1
FDDR_FACC_MUX_CONFIG	FACC_PRE_SRC_SEL	INIT[71:71]	1'h0	INIT[15]	1
FDDR_FACC_MUX_CONFIG	FACC_GLMUX_SEL	INIT[72:72]	1'h1	INIT[16]	1
FDDR_FACC_MUX_CONFIG	FACC_FAB_REF_SEL	INIT[73:73]	1'h0	INIT[17]	1
FDDR_FACC_DIVISOR_RATIO	FIC64_DIVISOR	INIT[76:74]	3'h0	INIT[18]	1
FDDR_FACC_DIVISOR_RATIO	DIVISOR_A	INIT[78:77]	2'h0	INIT[19]	1
FDDR_FACC_DIVISOR_RATIO	BASE_DIVISOR	INIT[81:79]	3'h0	INIT[20]	1
PLL_DELAY_LINE_SEL	PLL_REF_DEL_SEL	INIT[83:82]	2'h0	INIT[21]	1
PLL_DELAY_LINE_SEL	PLL_FB_DEL_SEL	INIT[85:84]	2'h0	INIT[21]	1
FDDR_SOFT_RESET	FDDR_CTLR_SOFTRESET	INIT[86:86]	1'h1	INIT[22]	1
FDDR_SOFT_RESET	FDDR_FIC64_SOFTRESET	INIT[87:87]	1'h1	INIT[23]	1
FDDR_IO_CALIB	PCODE	INIT[93:88]	6'h0	INIT[24]	1
FDDR_IO_CALIB	NCODE	INIT[99:94]	6'h0	INIT[24]	1
FDDR_IO_CALIB	CALIB_START	INIT[100:100]	1'h0	INIT[24]	1
FDDR_IO_CALIB	CALIB_LOCK	INIT[101:101]	1'h0	INIT[24]	1
FDDR_IO_CALIB	CALIB_TRIM	INIT[102:102]	1'h0	INIT[24]	1
FDDR_INTERRUPT_ENABLE	FPLL_LOCK_INT_ENABLE	INIT[103:103]	1'h0	INIT[25]	1
FDDR_INTERRUPT_ENABLE	FPLL_LOCKLOST_INT_ENABLE	INIT[104:104]	1'h0	INIT[25]	1
FDDR_INTERRUPT_ENABLE	FABRIC_PLL_LOCK_INT_ENABLE	INIT[105:105]	1'h0	INIT[25]	1
FDDR_INTERRUPT_ENABLE	FABRIC_PLL_LOCKLOST_INT_ENABLE	INIT[106:106]	1'h0	INIT[25]	1
FDDR_INTERRUPT_ENABLE	FDDR_ECC_INT_ENABLE	INIT[107:107]	1'h0	INIT[25]	1

Table 18 • **FDDR (Unused) *(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
FDDR_INTERRUPT_ENABLE	IO_CALIB_INT_ENABLE	INIT[108:108]	1'h0	INIT[25]	1
FDDR_INTERRUPT_ENABLE	FIC64_INT_ENABLE	INIT[109:109]	1'h0	INIT[25]	1
F_AXI_AHB_MODE_SEL	F_AXI_AHB_MODE	INIT[110:110]	1'h0	INIT[26]	1
PHY_SELF_REF_EN	PHY_SELF_REF_EN	INIT[111:111]	1'h0	INIT[27]	1

Note: Lock Value (*) = 0, disables modification of the Register field.

Table 19 • **PCIE0 (Unused)**

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
SER_PLL_CONFIG_LOW	PLL_REF_DIVISOR	INIT[85:80]	6'h1	INIT[0]	1
SER_PLL_CONFIG_LOW	PLL_FEEDBACK_DIVISOR	INIT[95:86]	10'h2	INIT[1]	1
SER_PLL_CONFIG_LOW	PLL_OUTPUT_DIVISOR	INIT[98:96]	3'h2	INIT[2]	1
SER_PLL_CONFIG_HIGH	PLL_FILTER_RANGE	INIT[102:99]	4'h9	INIT[3]	1
SER_PLL_CONFIG_HIGH	PLL_LOCKWIN	INIT[105:103]	3'h0	INIT[4]	1
SER_PLL_CONFIG_HIGH	PLL_LOCKCNT	INIT[109:106]	4'hF	INIT[5]	1
SER_PLL_CONFIG_HIGH	PLL_RESET	INIT[110:110]	1'h1	INIT[6]	1
SER_PLL_CONFIG_HIGH	PLL_BYPASS	INIT[111:111]	1'h1	INIT[7]	1
SER_PLL_CONFIG_HIGH	PLL_MODE_1V2	INIT[112:112]	1'h1	INIT[8]	1
SER_PLL_CONFIG_HIGH	PLL_MODE_3V3	INIT[113:113]	1'h0	INIT[9]	1
SER_PLL_CONFIG_HIGH	PLL_FSE	INIT[114:114]	1'h0	INIT[10]	1
SER_PLL_CONFIG_HIGH	PLL_PD	INIT[115:115]	1'h0	INIT[11]	1
SERDESIF_SOFT_RESET	PCIE_CTLR_SOFTRESET	INIT[116:116]	1'h1	INIT[12]	1
SERDESIF_SOFT_RESET	XAUI_CTRL_SOFTRESET	INIT[117:117]	1'h1	INIT[13]	1
SERDESIF_SOFT_RESET	SERDES_LANE0_SOFTRESET	INIT[118:118]	1'h1	INIT[14]	1
SERDESIF_SOFT_RESET	SERDES_LANE1_SOFTRESET	INIT[119:119]	1'h1	INIT[15]	1
SERDESIF_SOFT_RESET	SERDES_LANE2_SOFTRESET	INIT[120:120]	1'h1	INIT[16]	1
SERDESIF_SOFT_RESET	SERDES_LANE3_SOFTRESET	INIT[121:121]	1'h1	INIT[17]	1
SER_INTERRUPT_ENABLE	SPLL_LOCK_INT_ENABLE	INIT[122:122]	1'h0	INIT[18]	1
SER_INTERRUPT_ENABLE	SPLL_LOCKLOST_INT_ENABLE	INIT[123:123]	1'h0	INIT[18]	1
SER_INTERRUPT_ENABLE	FPLL_LOCK_INT_ENABLE	INIT[124:124]	1'h0	INIT[18]	1
SER_INTERRUPT_ENABLE	FPLL_LOCKLOST_INT_ENABLE	INIT[125:125]	1'h0	INIT[18]	1
CONFIG_AXI_AHB_BRIDGE	CFGR_AXI_AHB_MASTER	INIT[126:126]	1'h1	INIT[19]	1
CONFIG_AXI_AHB_BRIDGE	CFGR_AXI_AHB_SLAVE	INIT[127:127]	1'h1	INIT[20]	1
CONFIG_ECC_INTR_ENABLE	CFGR_PCIE_ECC_EN	INIT[130:128]	3'h7	INIT[21]	1
CONFIG_ECC_INTR_ENABLE	CFGR_PCIE_ECC_INTR_EN	INIT[133:131]	3'h7	INIT[22]	1

Table 19 • **PCIE0 (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
CONFIG_TEST_IN	CONFIG_TEST_IN	INIT[165:134]	32'h0	INIT[23]	1
TEST_OUT_READ_ADDR	TEST_OUT_READ_ADDR	INIT[170:166]	5'h0	INIT[24]	1
CONFIG_PCIE_PM	CFGR_SLOT_CONFIG	INIT[171:171]	1'h0	INIT[25]	1
CONFIG_PCIE_PM	CFGR_PM_AUX_PWR	INIT[172:172]	1'h0	INIT[26]	1
CONFIG_PCIE_PM	CFGR_L2_P2_ENABLE	INIT[173:173]	1'h0	INIT[27]	1
CONFIG_PCIE_PM	CFGR_TX_SWING	INIT[174:174]	1'h0	INIT[28]	1
CONFIG_PHY_MODE_0	CONFIG_PHY_MODE	INIT[190:175]	16'h5555	INIT[29]	1
CONFIG_PHY_MODE_1	CONFIG_ECPS_SEL	INIT[194:191]	4'h0	INIT[30]	1
CONFIG_PHY_MODE_1	CONFIG_LINKK2LANE	INIT[198:195]	4'hF	INIT[31]	1
CONFIG_PHY_MODE_1	CONFIG_REG_LANE_SEL	INIT[202:199]	4'hF	INIT[32]	1
CONFIG_PHY_MODE_2	CONFIG_REXT_SEL	INIT[210:203]	8'h0	INIT[33]	1
CONFIG_PCIE_0	PCIE_VENDOR_ID	INIT[226:211]	16'h0	INIT[34]	1
CONFIG_PCIE_0	PCIE_DEVICE_ID	INIT[242:227]	16'h0	INIT[35]	1
CONFIG_PCIE_1	PCIE_SUB_VENDOR_ID	INIT[258:243]	16'h0	INIT[36]	1
CONFIG_PCIE_1	PCIE_SUB_DEVICE_ID	INIT[274:259]	16'h0	INIT[37]	1
CONFIG_PCIE_2	PCIE_REV_ID	INIT[290:275]	16'h0	INIT[38]	1
CONFIG_PCIE_2	PCIE_CLASS_CODE	INIT[306:291]	16'h0	INIT[39]	1
CONFIG_PCIE_3	K_BRIDGE_SPEED	INIT[307:307]	1'h0	INIT[40]	1
CONFIG_PCIE_3	K_BRIDGE_EMPH	INIT[308:308]	1'h0	INIT[41]	1
CONFIG_PCIE_3	K_BRIDGE_SPEC_REV	INIT[310:309]	2'h0	INIT[42]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_CONTROL_0	INIT[314:311]	4'h0	INIT[43]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_SIZE_0	INIT[319:315]	4'h0	INIT[44]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_CONTROL_1	INIT[323:320]	4'h0	INIT[45]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_SIZE_1	INIT[328:324]	5'h0	INIT[46]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_CONTROL_2	INIT[332:329]	4'h0	INIT[47]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_SIZE_2	INIT[337:333]	5'h0	INIT[48]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_CONTROL_3	INIT[341:338]	4'h0	INIT[49]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_SIZE_3	INIT[346:342]	5'h0	INIT[50]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_CONTROL_4	INIT[350:347]	4'h0	INIT[51]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_SIZE_4	INIT[355:351]	5'h0	INIT[52]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_CONTROL_5	INIT[359:356]	4'h0	INIT[53]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_SIZE_5	INIT[364:360]	5'h0	INIT[54]	1
REFCLK_SEL	LANE01_REFCLK_SEL	INIT[366:365]	2'h0	INIT[55]	1
REFCLK_SEL	LANE23_REFCLK_SEL	INIT[368:367]	2'h0	INIT[56]	1
PCLK_SEL	PCIE_CORECLK_SEL	INIT[370:369]	2'h0	INIT[57]	1
PCLK_SEL	PIPE_PCLKIN_LANE01_SEL	INIT[372:371]	2'h0	INIT[58]	1
PCLK_SEL	PIPE_PCLKIN_LANE23_SEL	INIT[374:373]	2'h0	INIT[59]	1

Table 19 • **PCIE0 (Unused) *(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
ECPS_RSTN_SEL	FABRIC_EPCS_RSTN_SEL	INIT[378:375]	4'h0	INIT[60]	1
MBIST_CLK_SEL	MBIST_CLK_SEL	INIT[379:379]	1'h0	INIT[61]	1
SERDES_FATC_RESET	FATC_RESET	INIT[380:380]	1'h1	INIT[62]	1
RC_OSC_SPLL_REFCLK_SEL	RC_OSC_REFCLK_SEL	INIT[381:381]	1'h1	INIT[63]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSE	INIT[382:382]	1'h0	INIT[64]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSMD	INIT[384:383]	2'h0	INIT[65]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSMF	INIT[389:385]	5'h0	INIT[66]	1
CONF_AXI_MSTR_WNDW_0	CONF_AXI_MSTR_WNDW_0	INIT[421:390]	32'h0	INIT[67]	1
CONF_AXI_MSTR_WNDW_1	CONF_AXI_MSTR_WNDW_1	INIT[453:422]	32'h0	INIT[68]	1
CONF_AXI_MSTR_WNDW_2	CONF_AXI_MSTR_WNDW_2	INIT[485:454]	32'h0	INIT[69]	1
CONF_AXI_MSTR_WNDW_3	CONF_AXI_MSTR_WNDW_3	INIT[489:486]	4'h0	INIT[70]	1
CONF_AXI_SLV_WNDW_0	CONF_AXI_SLV_WNDW_0	INIT[521:490]	32'h0	INIT[71]	1
CONF_AXI_SLV_WNDW_1	CONF_AXI_SLV_WNDW_1	INIT[553:522]	32'h0	INIT[72]	1
CONF_AXI_SLV_WNDW_2	CONF_AXI_SLV_WNDW_2	INIT[585:554]	32'h0	INIT[73]	1
CONF_AXI_SLV_WNDW_3	CONF_AXI_SLV_WNDW_3	INIT[588:586]	3'h0	INIT[74]	1
DESKEW_CONFIG	DESKEW_PLL_REF_CLK	INIT[590:589]	2'h0	INIT[75]	1
DESKEW_CONFIG	DESKEW_PLL_FDB_CLK	INIT[592:591]	2'h0	INIT[76]	1
DEBUG_MODE_KEY	DEBUG_MODE_KEY	INIT[600:593]	8'h0	INIT[77]	1
ATSPEED_CLK_SEL	ATSPEED_CLK_SEL	INIT[601:601]	1'h0	INIT[78]	1
EXTRA_BITS	EXTRA_BITS	INIT[609:602]	8'h0F	INIT[79]	1

Note: Lock Value (*) = 0, disables modification of the Register field.

Table 20 • **PCIE1 (Unused)**

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
SER_PLL_CONFIG_LOW	PLL_REF_DIVISOR	INIT[85:80]	6'h1	INIT[0]	1
SER_PLL_CONFIG_LOW	PLL_FEEDBACK_DIVISOR	INIT[95:86]	10'h2	INIT[1]	1
SER_PLL_CONFIG_LOW	PLL_OUTPUT_DIVISOR	INIT[98:96]	3'h2	INIT[2]	1
SER_PLL_CONFIG_HIGH	PLL_FILTER_RANGE	INIT[102:99]	4'h9	INIT[3]	1
SER_PLL_CONFIG_HIGH	PLL_LOCKWIN	INIT[105:103]	3'h0	INIT[4]	1
SER_PLL_CONFIG_HIGH	PLL_LOCKCNT	INIT[109:106]	4'hF	INIT[5]	1
SER_PLL_CONFIG_HIGH	PLL_RESET	INIT[110:110]	1'h1	INIT[6]	1
SER_PLL_CONFIG_HIGH	PLL_BYPASS	INIT[111:111]	1'h1	INIT[7]	1
SER_PLL_CONFIG_HIGH	PLL_MODE_1V2	INIT[112:112]	1'h1	INIT[8]	1
SER_PLL_CONFIG_HIGH	PLL_MODE_3V3	INIT[113:113]	1'h0	INIT[9]	1
SER_PLL_CONFIG_HIGH	PLL_FSE	INIT[114:114]	1'h0	INIT[10]	1

Table 20 • **PCIE1 (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
SER_PLL_CONFIG_HIGH	PLL_PD	INIT[115:115]	1'h0	INIT[11]	1
SERDESIF_SOFT_RESET	PCIE_CTLR_SOFTRESET	INIT[116:116]	1'h1	INIT[12]	1
SERDESIF_SOFT_RESET	XAUI_CTRL_SOFTRESET	INIT[117:117]	1'h1	INIT[13]	1
SERDESIF_SOFT_RESET	SERDES_LANE0_SOFTRESET	INIT[118:118]	1'h1	INIT[14]	1
SERDESIF_SOFT_RESET	SERDES_LANE1_SOFTRESET	INIT[119:119]	1'h1	INIT[15]	1
SERDESIF_SOFT_RESET	SERDES_LANE2_SOFTRESET	INIT[120:120]	1'h1	INIT[16]	1
SERDESIF_SOFT_RESET	SERDES_LANE3_SOFTRESET	INIT[121:121]	1'h1	INIT[17]	1
SER_INTERRUPT_ENABLE	SPLL_LOCK_INT_ENABLE	INIT[122:122]	1'h0	INIT[18]	1
SER_INTERRUPT_ENABLE	SPLL_LOCKLOST_INT_ENABLE	INIT[123:123]	1'h0	INIT[18]	1
SER_INTERRUPT_ENABLE	FPLL_LOCK_INT_ENABLE	INIT[124:124]	1'h0	INIT[18]	1
SER_INTERRUPT_ENABLE	FPLL_LOCKLOST_INT_ENABLE	INIT[125:125]	1'h0	INIT[18]	1
CONFIG_AXI_AHB_BRIDGE	CFGR_AXI_AHB_MASTER	INIT[126:126]	1'h1	INIT[19]	1
CONFIG_AXI_AHB_BRIDGE	CFGR_AXI_AHB_SLAVE	INIT[127:127]	1'h1	INIT[20]	1
CONFIG_ECC_INTR_ENABLE	CFGR_PCIE_ECC_EN	INIT[130:128]	3'h7	INIT[21]	1
CONFIG_ECC_INTR_ENABLE	CFGR_PCIE_ECC_INTR_EN	INIT[133:131]	3'h7	INIT[22]	1
CONFIG_TEST_IN	CONFIG_TEST_IN	INIT[165:134]	32'h0	INIT[23]	1
TEST_OUT_READ_ADDR	TEST_OUT_READ_ADDR	INIT[170:166]	5'h0	INIT[24]	1
CONFIG_PCIE_PM	CFGR_SLOT_CONFIG	INIT[171:171]	1'h0	INIT[25]	1
CONFIG_PCIE_PM	CFGR_PM_AUX_PWR	INIT[172:172]	1'h0	INIT[26]	1
CONFIG_PCIE_PM	CFGR_L2_P2_ENABLE	INIT[173:173]	1'h0	INIT[27]	1
CONFIG_PCIE_PM	CFGR_TX_SWING	INIT[174:174]	1'h0	INIT[28]	1
CONFIG_PHY_MODE_0	CONFIG_PHY_MODE	INIT[190:175]	16'h5555	INIT[29]	1
CONFIG_PHY_MODE_1	CONFIG_ECPS_SEL	INIT[194:191]	4'h0	INIT[30]	1
CONFIG_PHY_MODE_1	CONFIG_LINKK2LANE	INIT[198:195]	4'hF	INIT[31]	1
CONFIG_PHY_MODE_1	CONFIG_REG_LANE_SEL	INIT[202:199]	4'hF	INIT[32]	1
CONFIG_PHY_MODE_2	CONFIG_REXT_SEL	INIT[210:203]	8'h0	INIT[33]	1
CONFIG_PCIE_0	PCIE_VENDOR_ID	INIT[226:211]	16'h0	INIT[34]	1
CONFIG_PCIE_0	PCIE_DEVICE_ID	INIT[242:227]	16'h0	INIT[35]	1
CONFIG_PCIE_1	PCIE_SUB_VENDOR_ID	INIT[258:243]	16'h0	INIT[36]	1
CONFIG_PCIE_1	PCIE_SUB_DEVICE_ID	INIT[274:259]	16'h0	INIT[37]	1
CONFIG_PCIE_2	PCIE_REV_ID	INIT[290:275]	16'h0	INIT[38]	1
CONFIG_PCIE_2	PCIE_CLASS_CODE	INIT[306:291]	16'h0	INIT[39]	1
CONFIG_PCIE_3	K_BRIDGE_SPEED	INIT[307:307]	1'h0	INIT[40]	1
CONFIG_PCIE_3	K_BRIDGE_EMPH	INIT[308:308]	1'h0	INIT[41]	1
CONFIG_PCIE_3	K_BRIDGE_SPEC_REV	INIT[310:309]	2'h0	INIT[42]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_CONTROL_0	INIT[314:311]	4'h0	INIT[43]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_SIZE_0	INIT[319:315]	5'h0	INIT[44]	1

Table 20 • **PCIE1 (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_CONTROL_1	INIT[323:320]	4'h0	INIT[45]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_SIZE_1	INIT[328:324]	5'h0	INIT[46]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_CONTROL_2	INIT[332:329	4'h0	INIT[47]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_SIZE_2	INIT[337:333]	5'h0	INIT[48]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_CONTROL_3	INIT[341:338]	4'h0	INIT[49]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_SIZE_3	INIT[346:342]	5'h0	INIT[50]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_CONTROL_4	INIT[350:347]	4'h0	INIT[51]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_SIZE_4	INIT[355:351]	5'h0	INIT[52]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_CONTROL_5	INIT[359:356]	4'h0	INIT[53]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_SIZE_5	INIT[364:360]	5'h0	INIT[54]	1
REFCLK_SEL	LANE01_REFCLK_SEL	INIT[366:365]	2'h0	INIT[55]	1
REFCLK_SEL	LANE23_REFCLK_SEL	INIT[368:367]	2'h0	INIT[56]	1
PCLK_SEL	PCIE_CORECLK_SEL	INIT[370:369]	2'h0	INIT[57]	1
PCLK_SEL	PIPE_PCLKIN_LANE01_SEL	INIT[372:371]	2'h0	INIT[58]	1
PCLK_SEL	PIPE_PCLKIN_LANE23_SEL	INIT[374:373]	2'h0	INIT[59]	1
ECPS_RSTN_SEL	FABRIC_EPCS_RSTN_SEL	INIT[378:375]	4'h0	INIT[60]	1
MBIST_CLK_SEL	MBIST_CLK_SEL	INIT[379:379]	1'h0	INIT[61]	1
SERDES_FATC_RESET	FATC_RESET	INIT[380:380]	1'h1	INIT[62]	1
RC_OSC_SPLL_REFCLK_SEL	RC_OSC_REFCLK_SEL	INIT[381:381]	1'h1	INIT[63]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSE	INIT[382:382]	1'h0	INIT[64]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSMD	INIT[384:383]	2'h0	INIT[65]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSMF	INIT[389:385]	5'h0	INIT[66]	1
CONF_AXI_MSTR_WNDW_0	CONF_AXI_MSTR_WNDW_0	INIT[421:390]	32'h0	INIT[67]	1
CONF_AXI_MSTR_WNDW_1	CONF_AXI_MSTR_WNDW_1	INIT[453:422]	32'h0	INIT[68]	1
CONF_AXI_MSTR_WNDW_2	CONF_AXI_MSTR_WNDW_2	INIT[485:454]	32'h0	INIT[69]	1
CONF_AXI_MSTR_WNDW_3	CONF_AXI_MSTR_WNDW_3	INIT[489:486]	4'h0	INIT[70]	1
CONF_AXI_SLV_WNDW_0	CONF_AXI_SLV_WNDW_0	INIT[521:490]	32'h0	INIT[71]	1
CONF_AXI_SLV_WNDW_1	CONF_AXI_SLV_WNDW_1	INIT[553:522]	32'h0	INIT[72]	1
CONF_AXI_SLV_WNDW_2	CONF_AXI_SLV_WNDW_2	INIT[585:554]	32'h0	INIT[73]	1
CONF_AXI_SLV_WNDW_3	CONF_AXI_SLV_WNDW_3	INIT[588:586]	3'h0	INIT[74]	1
DESKEW_CONFIG	DESKEW_PLL_REF_CLK	INIT[590:589]	2'h0	INIT[75]	1
DESKEW_CONFIG	DESKEW_PLL_FDB_CLK	INIT[592:591]	2'h0	INIT[76]	1
DEBUG_MODE_KEY	DEBUG_MODE_KEY	INIT[600:593]	8'h0	INIT[77]	1
ATSPEED_CLK_SEL	ATSPEED_CLK_SEL	INIT[601:601]	1'h0	INIT[78]	1
EXTRA_BITS	EXTRA_BITS	INIT[609:602]	8'h0F	INIT[79]	1

Note: Lock Value (*) = 0, disables modification of the Register field.

Table 21 • **PCIE2 (Unused)**

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
SER_PLL_CONFIG_LOW	PLL_REF_DIVISOR	INIT[85:80]	6'h1	INIT[0]	1
SER_PLL_CONFIG_LOW	PLL_FEEDBACK_DIVISOR	INIT[95:86]	10'h2	INIT[1]	1
SER_PLL_CONFIG_LOW	PLL_OUTPUT_DIVISOR	INIT[98:96]	3'h2	INIT[2]	1
SER_PLL_CONFIG_HIGH	PLL_FILTER_RANGE	INIT[102:99]	4'h9	INIT[3]	1
SER_PLL_CONFIG_HIGH	PLL_LOCKWIN	INIT[105:103]	3'h0	INIT[4]	1
SER_PLL_CONFIG_HIGH	PLL_LOCKCNT	INIT[109:106]	4'hF	INIT[5]	1
SER_PLL_CONFIG_HIGH	PLL_RESET	INIT[110:110]	1'h1	INIT[6]	1
SER_PLL_CONFIG_HIGH	PLL_BYPASS	INIT[111:111]	1'h1	INIT[7]	1
SER_PLL_CONFIG_HIGH	PLL_MODE_1V2	INIT[112:112]	1'h1	INIT[8]	1
SER_PLL_CONFIG_HIGH	PLL_MODE_3V3	INIT[113:113]	1'h0	INIT[9]	1
SER_PLL_CONFIG_HIGH	PLL_FSE	INIT[114:114]	1'h0	INIT[10]	1
SER_PLL_CONFIG_HIGH	PLL_PD	INIT[115:115]	1'h0	INIT[11]	1
SERDESIF_SOFT_RESET	PCIE_CTLR_SOFTRESET	INIT[116:116]	1'h1	INIT[12]	1
SERDESIF_SOFT_RESET	XAUI_CTRL_SOFTRESET	INIT[117:117]	1'h1	INIT[13]	1
SERDESIF_SOFT_RESET	SERDES_LANE0_SOFTRESET	INIT[118:118]	1'h1	INIT[14]	1
SERDESIF_SOFT_RESET	SERDES_LANE1_SOFTRESET	INIT[119:119]	1'h1	INIT[15]	1
SERDESIF_SOFT_RESET	SERDES_LANE2_SOFTRESET	INIT[120:120]	1'h1	INIT[16]	1
SERDESIF_SOFT_RESET	SERDES_LANE3_SOFTRESET	INIT[121:121]	1'h1	INIT[17]	1
SER_INTERRUPT_ENABLE	SPLL_LOCK_INT_ENABLE	INIT[122:122]	1'h0	INIT[18]	1
SER_INTERRUPT_ENABLE	SPLL_LOCKLOST_INT_ENABLE	INIT[123:123]	1'h0	INIT18[]	1
SER_INTERRUPT_ENABLE	FPLL_LOCK_INT_ENABLE	INIT[124:124]	1'h0	INIT[18]	1
SER_INTERRUPT_ENABLE	FPLL_LOCKLOST_INT_ENABLE	INIT[125:125]	1'h0	INIT[18]	1
CONFIG_AXI_AHB_BRIDGE	CFGR_AXI_AHB_MASTER	INIT[126:126]	1'h1	INIT[19]	1
CONFIG_AXI_AHB_BRIDGE	CFGR_AXI_AHB_SLAVE	INIT[127:127]	1'h1	INIT[20]	1
CONFIG_ECC_INTR_ENABLE	CFGR_PCIE_ECC_EN	INIT[130:128]	3'h7	INIT[21]	1
CONFIG_ECC_INTR_ENABLE	CFGR_PCIE_ECC_INTR_EN	INIT[133:131]	3'h7	INIT[22]	1
CONFIG_TEST_IN	CONFIG_TEST_IN	INIT[165:134]	32'h0	INIT[23]	1
TEST_OUT_READ_ADDR	TEST_OUT_READ_ADDR	INIT[170:166]	5'h0	INIT[24]	1
CONFIG_PCIE_PM	CFGR_SLOT_CONFIG	INIT[171:171]	1'h0	INIT[25]	1
CONFIG_PCIE_PM	CFGR_PM_AUX_PWR	INIT[172:172]	1'h0	INIT[26]	1
CONFIG_PCIE_PM	CFGR_L2_P2_ENABLE	INIT[173:173]	1'h0	INIT[27]	1
CONFIG_PCIE_PM	CFGR_TX_SWING	INIT[174:174]	1'h0	INIT[28]	1
CONFIG_PHY_MODE_0	CONFIG_PHY_MODE	INIT[190:175]	16'h5555	INIT[29]	1
CONFIG_PHY_MODE_1	CONFIG_ECPS_SEL	INIT[194:191]	4'h0	INIT[30]	1
CONFIG_PHY_MODE_1	CONFIG_LINKK2LANE	INIT[198:195]	4'hF	INIT[31]	1
CONFIG_PHY_MODE_1	CONFIG_REG_LANE_SEL	INIT[202:199]	4'hF	INIT[32]	1

Table 21 • **PCIE2 (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
CONFIG_PHY_MODE_2	CONFIG_REXT_SEL	INIT[210:203]	8'h0	INIT[33]	1
CONFIG_PCIE_0	PCIE_VENDOR_ID	INIT[226:211]	16'h0	INIT[34]	1
CONFIG_PCIE_0	PCIE_DEVICE_ID	INIT[242:227]	16'h0	INIT[35]	1
CONFIG_PCIE_1	PCIE_SUB_VENDOR_ID	INIT[258:243]	16'h0	INIT[36]	1
CONFIG_PCIE_1	PCIE_SUB_DEVICE_ID	INIT[274:259]	16'h0	INIT[37]	1
CONFIG_PCIE_2	PCIE_REV_ID	INIT[290:275]	16'h0	INIT[38]	1
CONFIG_PCIE_2	PCIE_CLASS_CODE	INIT[306:291]	16'h0	INIT[39]	1
CONFIG_PCIE_3	K_BRIDGE_SPEED	INIT[307:307]	1'h0	INIT[40]	1
CONFIG_PCIE_3	K_BRIDGE_EMPH	INIT[308:308]	1'h0	INIT[41]	1
CONFIG_PCIE_3	K_BRIDGE_SPEC_REV	INIT[310:309]	2'h0	INIT[42]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_CONTROL_0	INIT[314:311]	4'h0	INIT[43]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_SIZE_0	INIT[319:315]	5'h0	INIT[44]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_CONTROL_1	INIT[323:320]	4'h0	INIT[45]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_SIZE_1	INIT[328:324]	5'h0	INIT[46]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_CONTROL_2	INIT[332:329]	4'h0	INIT[47]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_SIZE_2	INIT[337:333]	5'h0	INIT[48]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_CONTROL_3	INIT[341:338]	4'h0	INIT[49]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_SIZE_3	INIT[346:342]	5'h0	INIT[50]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_CONTROL_4	INIT[350:347]	4'h0	INIT[51]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_SIZE_4	INIT[355:351]	5'h0	INIT[52]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_CONTROL_5	INIT[359:356]	4'h0	INIT[53]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_SIZE_5	INIT[364:360]	5'h0	INIT[54]	1
REFCLK_SEL	LANE01_REFCLK_SEL	INIT[366:365]	2'h0	INIT[55]	1
REFCLK_SEL	LANE23_REFCLK_SEL	INIT[368:367]	2'h0	INIT[56]	1
PCLK_SEL	PCIE_CORECLK_SEL	INIT[370:369]	2'h0	INIT[57]	1
PCLK_SEL	PIPE_PCLKIN_LANE01_SEL	INIT[372:371]	2'h0	INIT[58]	1
PCLK_SEL	PIPE_PCLKIN_LANE23_SEL	INIT[374:373]	2'h0	INIT[59]	1
ECPS_RSTN_SEL	FABRIC_EPCS_RSTN_SEL	INIT[378:375]	4'h0	INIT[60]	1
MBIST_CLK_SEL	MBIST_CLK_SEL	INIT[379:379]	1'h0	INIT[61]	1
SERDES_FATC_RESET	FATC_RESET	INIT[380:380]	1'h1	INIT[62]	1
RC_OSC_SPLL_REFCLK_SEL	RC_OSC_REFCLK_SEL	INIT[381:381]	1'h1	INIT[63]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSE	INIT[382:382]	1'h0	INIT[64]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSMD	INIT[384:383]	2'h0	INIT[65]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSMF	INIT[389:385]	5'h0	INIT[66]	1
CONF_AXI_MSTR_WNDW_0	CONF_AXI_MSTR_WNDW_0	INIT[421:390]	32'h0	INIT[67]	1
CONF_AXI_MSTR_WNDW_1	CONF_AXI_MSTR_WNDW_1	INIT[453:422]	32'h0	INIT[68]	1
CONF_AXI_MSTR_WNDW_2	CONF_AXI_MSTR_WNDW_2	INIT[485:454]	32'h0	INIT[69]	1

Table 21 • **PCIE2 (Unused) *(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
CONF_AXI_MSTR_WNDW_3	CONF_AXI_MSTR_WNDW_3	INIT[489:486]	4'h0	INIT[70]	1
CONF_AXI_SLV_WNDW_0	CONF_AXI_SLV_WNDW_0	INIT[521:490]	32'h0	INIT[71]	1
CONF_AXI_SLV_WNDW_1	CONF_AXI_SLV_WNDW_1	INIT[553:522]	32'h0	INIT[72]	1
CONF_AXI_SLV_WNDW_2	CONF_AXI_SLV_WNDW_2	INIT[585:554]	32'h0	INIT[73]	1
CONF_AXI_SLV_WNDW_3	CONF_AXI_SLV_WNDW_3	INIT[588:586]	3'h0	INIT[74]	1
DESKEW_CONFIG	DESKEW_PLL_REF_CLK	INIT[590:589]	2'h0	INIT[75]	1
DESKEW_CONFIG	DESKEW_PLL_FDB_CLK	INIT[592:591]	2'h0	INIT[76]	1
DEBUG_MODE_KEY	DEBUG_MODE_KEY	INIT[600:593]	8'h0	INIT[77]	1
ATSPEED_CLK_SEL	ATSPEED_CLK_SEL	INIT[601:601]	1'h0	INIT[78]	1
EXTRA_BITS	EXTRA_BITS	INIT[609:602]	8'h0F	INIT[79]	1

Note: Lock Value (*) = 0, disables modification of the Register field.

Table 22 • **PCIE3 (Unused)**

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
SER_PLL_CONFIG_LOW	PLL_REF_DIVISOR	INIT[85:80]	6'h1	INIT[0]	1
SER_PLL_CONFIG_LOW	PLL_FEEDBACK_DIVISOR	INIT[95:86]	10'h2	INIT[1]	1
SER_PLL_CONFIG_LOW	PLL_OUTPUT_DIVISOR	INIT[98:96]	3'h2	INIT[2]	1
SER_PLL_CONFIG_HIGH	PLL_FILTER_RANGE	INIT[102:99]	4'h9	INIT[3]	1
SER_PLL_CONFIG_HIGH	PLL_LOCKWIN	INIT[105:103]	3'h0	INIT[4]	1
SER_PLL_CONFIG_HIGH	PLL_LOCKCNT	INIT[109:106]	4'hF	INIT[5]	1
SER_PLL_CONFIG_HIGH	PLL_RESET	INIT[110:110]	1'h1	INIT[6]	1
SER_PLL_CONFIG_HIGH	PLL_BYPASS	INIT[111:111]	1'h1	INIT[7]	1
SER_PLL_CONFIG_HIGH	PLL_MODE_1V2	INIT[112:112]	1'h1	INIT[8]	1
SER_PLL_CONFIG_HIGH	PLL_MODE_3V3	INIT[113:113]	1'h0	INIT[9]	1
SER_PLL_CONFIG_HIGH	PLL_FSE	INIT[114:114]	1'h0	INIT[10]	1
SER_PLL_CONFIG_HIGH	PLL_PD	INIT[115:115]	1'h0	INIT[11]	1
SERDESIF_SOFT_RESET	PCIE_CTLR_SOFTRESET	INIT[116:116]	1'h1	INIT[12]	1
SERDESIF_SOFT_RESET	XAUI_CTRL_SOFTRESET	INIT[117:117]	1'h1	INIT[13]	1
SERDESIF_SOFT_RESET	SERDES_LANE0_SOFTRESET	INIT[118:118]	1'h1	INIT[14]	1
SERDESIF_SOFT_RESET	SERDES_LANE1_SOFTRESET	INIT[119:119]	1'h1	INIT[15]	1
SERDESIF_SOFT_RESET	SERDES_LANE2_SOFTRESET	INIT[120:120]	1'h1	INIT[16]	1
SERDESIF_SOFT_RESET	SERDES_LANE3_SOFTRESET	INIT[121:121]	1'h1	INIT[17]	1
SER_INTERRUPT_ENABLE	SPLL_LOCK_INT_ENABLE	INIT[122:122]	1'h0	INIT[18]	1
SER_INTERRUPT_ENABLE	SPLL_LOCKLOST_INT_ENABLE	INIT[123:123]	1'h0	INIT18[]	1
SER_INTERRUPT_ENABLE	FPLL_LOCK_INT_ENABLE	INIT[124:124]	1'h0	INIT[18]	1

Table 22 • **PCIE3 (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
SER_INTERRUPT_ENABLE	FPLL_LOCKLOST_INT_ENABLE	INIT[125:125]	1'h0	INIT[18]	1
CONFIG_AXI_AHB_BRIDGE	CFGR_AXI_AHB_MASTER	INIT[126:126]	1'h1	INIT[19]	1
CONFIG_AXI_AHB_BRIDGE	CFGR_AXI_AHB_SLAVE	INIT[127:127]	1'h1	INIT[20]	1
CONFIG_ECC_INTR_ENABLE	CFGR_PCIE_ECC_EN	INIT[130:128]	3'h7	INIT[21]	1
CONFIG_ECC_INTR_ENABLE	CFGR_PCIE_ECC_INTR_EN	INIT[133:131]	3'h7	INIT[22]	1
CONFIG_TEST_IN	CONFIG_TEST_IN	INIT[165:134]	32'h0	INIT[23]	1
TEST_OUT_READ_ADDR	TEST_OUT_READ_ADDR	INIT[170:166]	5'h0	INIT[24]	1
CONFIG_PCIE_PM	CFGR_SLOT_CONFIG	INIT[171:171]	1'h0	INIT[25]	1
CONFIG_PCIE_PM	CFGR_PM_AUX_PWR	INIT[172:172]	1'h0	INIT[26]	1
CONFIG_PCIE_PM	CFGR_L2_P2_ENABLE	INIT[173:173]	1'h0	INIT[27]	1
CONFIG_PCIE_PM	CFGR_TX_SWING	INIT[174:174]	1'h0	INIT[28]	1
CONFIG_PHY_MODE_0	CONFIG_PHY_MODE	INIT[190:175]	16'h5555	INIT[29]	1
CONFIG_PHY_MODE_1	CONFIG_ECPS_SEL	INIT[194:191]	4'h0	INIT[30]	1
CONFIG_PHY_MODE_1	CONFIG_LINKK2LANE	INIT[198:195]	4'hF	INIT[31]	1
CONFIG_PHY_MODE_1	CONFIG_REG_LANE_SEL	INIT[202:199]	4'hF	INIT[32]	1
CONFIG_PHY_MODE_2	CONFIG_REXT_SEL	INIT[210:203]	8'h0	INIT[33]	1
CONFIG_PCIE_0	PCIE_VENDOR_ID	INIT[226:211]	16'h0	INIT[34]	1
CONFIG_PCIE_0	PCIE_DEVICE_ID	INIT[242:227]	16'h0	INIT[35]	1
CONFIG_PCIE_1	PCIE_SUB_VENDOR_ID	INIT[258:243]	16'h0	INIT[36]	1
CONFIG_PCIE_1	PCIE_SUB_DEVICE_ID	INIT[274:259]	16'h0	INIT[37]	1
CONFIG_PCIE_2	PCIE_REV_ID	INIT[290:275]	16'h0	INIT[38]	1
CONFIG_PCIE_2	PCIE_CLASS_CODE	INIT[306:291]	16'h0	INIT[39]	1
CONFIG_PCIE_3	K_BRIDGE_SPEED	INIT[307:307]	1'h0	INIT[40]	1
CONFIG_PCIE_3	K_BRIDGE_EMPH	INIT[308:308]	1'h0	INIT[41]	1
CONFIG_PCIE_3	K_BRIDGE_SPEC_REV	INIT[310:309]	2'h0	INIT[42]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_CONTROL_0	INIT[314:311]	4'h0	INIT[43]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_SIZE_0	INIT[319:315]	5'h0	INIT[44]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_CONTROL_1	INIT[323:320]	4'h0	INIT[45]	1
CONFIG_BAR_SIZE_0_1	CONFIG_BAR_SIZE_1	INIT[328:324]	5'h0	INIT[46]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_CONTROL_2	INIT[332:329]	4'h0	INIT[47]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_SIZE_2	INIT[337:333]	5'h0	INIT[48]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_CONTROL_3	INIT[341:338]	4'h0	INIT[49]	1
CONFIG_BAR_SIZE_2_3	CONFIG_BAR_SIZE_3	INIT[346:342]	5'h0	INIT[50]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_CONTROL_4	INIT[350:347]	4'h0	INIT[51]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_SIZE_4	INIT[355:351]	5'h0	INIT[52]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_CONTROL_5	INIT[359:356]	4'h0	INIT[53]	1
CONFIG_BAR_SIZE_3_4	CONFIG_BAR_SIZE_5	INIT[364:360]	5'h0	INIT[54]	1

Table 22 • **PCIE3 (Unused)** ***(continued)***

Register	Field	INIT	Value	Lock INIT	Lock Value (*)
REFCLK_SEL	LANE01_REFCLK_SEL	INIT[366:365]	2'h0	INIT[55]	1
REFCLK_SEL	LANE23_REFCLK_SEL	INIT[368:367]	2'h0	INIT[56]	1
PCLK_SEL	PCIE_CORECLK_SEL	INIT[370:369]	2'h0	INIT[57]	1
PCLK_SEL	PIPE_PCLKIN_LANE01_SEL	INIT[372:371]	2'h0	INIT[58]	1
PCLK_SEL	PIPE_PCLKIN_LANE23_SEL	INIT[374:373]	2'h0	INIT[59]	1
ECPS_RSTN_SEL	FABRIC_EPCS_RSTN_SEL	INIT[378:375]	4'h0	INIT[60]	1
MBIST_CLK_SEL	MBIST_CLK_SEL	INIT[379:379]	1'h0	INIT[61]	1
SERDES_FATC_RESET	FATC_RESET	INIT[380:380]	1'h1	INIT[62]	1
RC_OSC_SPLL_REFCLK_SEL	RC_OSC_REFCLK_SEL	INIT[381:381]	1'h1	INIT[63]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSE	INIT[382:382]	1'h0	INIT[64]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSMD	INIT[384:383]	2'h0	INIT[65]	1
SPREAD_SPECTRUM_CLK	PLL_SERDESIF_SSMF	INIT[389:385]	5'h0	INIT[66]	1
CONF_AXI_MSTR_WNDW_0	CONF_AXI_MSTR_WNDW_0	INIT[421:390]	32'h0	INIT[67]	1
CONF_AXI_MSTR_WNDW_1	CONF_AXI_MSTR_WNDW_1	INIT[453:422]	32'h0	INIT[68]	1
CONF_AXI_MSTR_WNDW_2	CONF_AXI_MSTR_WNDW_2	INIT[485:454]	32'h0	INIT[69]	1
CONF_AXI_MSTR_WNDW_3	CONF_AXI_MSTR_WNDW_3	INIT[489:486]	4'h0	INIT[70]	1
CONF_AXI_SLV_WNDW_0	CONF_AXI_SLV_WNDW_0	INIT[521:490]	32'h0	INIT[71]	1
CONF_AXI_SLV_WNDW_1	CONF_AXI_SLV_WNDW_1	INIT[553:522]	32'h0	INIT[72]	1
CONF_AXI_SLV_WNDW_2	CONF_AXI_SLV_WNDW_2	INIT[585:554]	32'h0	INIT[73]	1
CONF_AXI_SLV_WNDW_3	CONF_AXI_SLV_WNDW_3	INIT[588:586]	3'h0	INIT[74]	1
DESKEW_CONFIG	DESKEW_PLL_REF_CLK	INIT[590:589]	2'h0	INIT[75]	1
DESKEW_CONFIG	DESKEW_PLL_FDB_CLK	INIT[592:591]	2'h0	INIT[76]	1
DEBUG_MODE_KEY	DEBUG_MODE_KEY	INIT[600:593]	8'h0	INIT[77]	1
ATSPEED_CLK_SEL	ATSPEED_CLK_SEL	INIT[601:601]	1'h0	INIT[78]	1
EXTRA_BITS	EXTRA_BITS	INIT[609:602]	8'h0F	INIT[79]	1

Note: Lock Value (*) = 0, disables modification of the Register field.

Table 23 • **HPMS Security Setting (Unused)**

Register	Field	ACT_UBITS	Value	Lock ACT_UBITS	Lock Value (*)
MM0_1_2_MS0_ALLOWED_R	MM0_1_2_MS0_ALLOWED_R	ACT_UBITS [0:0]	1'h1	N/A	N/A
MM0_1_2_MS1_ALLOWED_R	MM0_1_2_MS1_ALLOWED_R	ACT_UBITS [1:1]	1'h1	N/A	N/A
MM0_1_2_MS2_ALLOWED_R	MM0_1_2_MS2_ALLOWED_R	ACT_UBITS [2:2]	1'h1	N/A	N/A
MM0_1_2_MS3_ALLOWED_R	MM0_1_2_MS3_ALLOWED_R	ACT_UBITS [3:3]	1'h1	N/A	N/A
MM0_1_2_MS6_ALLOWED_R	MM0_1_2_MS6_ALLOWED_R	ACT_UBITS [4:4]	1'h1	N/A	N/A
MM0_1_2_MS0_ALLOWED_W	MM0_1_2_MS0_ALLOWED_W	ACT_UBITS [5:5]	1'h1	N/A	N/A
MM0_1_2_MS1_ALLOWED_W	MM0_1_2_MS1_ALLOWED_W	ACT_UBITS [6:6]	1'h1	N/A	N/A
MM0_1_2_MS2_ALLOWED_W	MM0_1_2_MS2_ALLOWED_W	ACT_UBITS [7:7]	1'h1	N/A	N/A
MM0_1_2_MS3_ALLOWED_W	MM0_1_2_MS3_ALLOWED_W	ACT_UBITS [8:8]	1'h1	N/A	N/A
MM0_1_2_MS6_ALLOWED_W	MM0_1_2_MS6_ALLOWED_W	ACT_UBITS [9:9]	1'h1	N/A	N/A
MM4_5_FIC64_MS0_ALLOWED_R	MM4_5_FIC64_MS0_ALLOWED_R	ACT_UBITS [10:10]	1'h1	N/A	N/A
MM4_5_FIC64_MS1_ALLOWED_R	MM4_5_FIC64_MS1_ALLOWED_R	ACT_UBITS [11:11]	1'h1	N/A	N/A
MM4_5_FIC64_MS2_ALLOWED_R	MM4_5_FIC64_MS2_ALLOWED_R	ACT_UBITS [12:12]	1'h1	N/A	N/A
MM4_5_FIC64_MS3_ALLOWED_R	MM4_5_FIC64_MS3_ALLOWED_R	ACT_UBITS [13:13]	1'h1	N/A	N/A
MM4_5_FIC64_MS6_ALLOWED_R	MM4_5_FIC64_MS6_ALLOWED_R	ACT_UBITS [14:14]	1'h1	N/A	N/A
MM4_5_FIC64_MS0_ALLOWED_W	MM4_5_FIC64_MS0_ALLOWED_W	ACT_UBITS [15:15]	1'h1	N/A	N/A
MM4_5_FIC64_MS1_ALLOWED_W	MM4_5_FIC64_MS1_ALLOWED_W	ACT_UBITS [16:16]	1'h1	N/A	N/A
MM4_5_FIC64_MS2_ALLOWED_W	MM4_5_FIC64_MS2_ALLOWED_W	ACT_UBITS [17:17]	1'h1	N/A	N/A
MM4_5_FIC64_MS3_ALLOWED_W	MM4_5_FIC64_MS3_ALLOWED_W	ACT_UBITS [18:18]	1'h1	N/A	N/A
MM4_5_FIC64_MS6_ALLOWED_W	MM4_5_FIC64_MS6_ALLOWED_W	ACT_UBITS [19:19]	1'h1	N/A	N/A
MM3_6_7_8_MS0_ALLOWED_R	MM3_6_7_8_MS0_ALLOWED_R	ACT_UBITS [20:20]	1'h1	N/A	N/A

Table 23 • **HPMS Security Setting (Unused)** ***(continued)***

Register	Field	ACT_UBITS	Value	Lock ACT_UBITS	Lock Value (*)
MM3_6_7_8_MS1_ALLOWED_R	MM3_6_7_8_MS1_ALLOWED_R	ACT_UBITS [21:21]	1'h1	N/A	N/A
MM3_6_7_8_MS2_ALLOWED_R	MM3_6_7_8_MS2_ALLOWED_R	ACT_UBITS [22:22]	1'h1	N/A	N/A
MM3_6_7_8_MS3_ALLOWED_R	MM3_6_7_8_MS3_ALLOWED_R	ACT_UBITS [23:23]	1'h1	N/A	N/A
MM3_6_7_8_MS6_ALLOWED_R	MM3_6_7_8_MS6_ALLOWED_R	ACT_UBITS [24:24]	1'h1	N/A	N/A
MM3_6_7_8_MS0_ALLOWED_W	MM3_6_7_8_MS0_ALLOWED_W	ACT_UBITS [25:25]	1'h1	N/A	N/A
MM3_6_7_8_MS1_ALLOWED_W	MM3_6_7_8_MS1_ALLOWED_W	ACT_UBITS [26:26]	1'h1	N/A	N/A
MM3_6_7_8_MS2_ALLOWED_W	MM3_6_7_8_MS2_ALLOWED_W	ACT_UBITS [27:27]	1'h1	N/A	N/A
MM3_6_7_8_MS3_ALLOWED_W	MM3_6_7_8_MS3_ALLOWED_W	ACT_UBITS [28:28]	1'h1	N/A	N/A
MM3_6_7_8_MS6_ALLOWED_W	MM3_6_7_8_MS6_ALLOWED_W	ACT_UBITS [29:29]	1'h1	N/A	N/A
MM9_MS0_ALLOWED_R	MM9_MS0_ALLOWED_R	ACT_UBITS [30:30]	1'h1	N/A	N/A
MM9_MS1_ALLOWED_R	MM9_MS1_ALLOWED_R	ACT_UBITS [31:31]	1'h1	N/A	N/A
MM9_MS2_ALLOWED_R	MM9_MS2_ALLOWED_R	ACT_UBITS [32:32]	1'h1	N/A	N/A
MM9_MS3_ALLOWED_R	MM9_MS3_ALLOWED_R	ACT_UBITS [33:33]	1'h1	N/A	N/A
MM9_MS6_ALLOWED_R	MM9_MS6_ALLOWED_R	ACT_UBITS [34:34]	1'h1	N/A	N/A
MM9_MS0_ALLOWED_W	MM9_MS0_ALLOWED_W	ACT_UBITS [35:35]	1'h1	N/A	N/A
MM9_MS1_ALLOWED_W	MM9_MS1_ALLOWED_W	ACT_UBITS [36:36]	1'h1	N/A	N/A
MM9_MS2_ALLOWED_W	MM9_MS2_ALLOWED_W	ACT_UBITS [37:37]	1'h1	N/A	N/A
MM9_MS3_ALLOWED_W	MM9_MS3_ALLOWED_W	ACT_UBITS [38:38]	1'h1	N/A	N/A
MM9_MS6_ALLOWED_W	MM9_MS6_ALLOWED_W	ACT_UBITS [39:39]	1'h1	N/A	N/A
NVM0_LOWER_M3ACCESS	NVM0_LOWER_M3ACCESS	ACT_UBITS [40:40]	1'h1	N/A	N/A
NVM0_LOWER_FABRIC_ACCESS	NVM0_LOWER_FABRIC_ACCESS	ACT_UBITS [41:41]	1'h1	N/A	N/A
NVM0_LOWER_OTHERS_ACCESS	NVM0_LOWER_OTHERS_ACCES	ACT_UBITS [42:42]	1'h1	N/A	N/A

Table 23 • **HPMS Security Setting (Unused) *(continued)***

Register	Field	ACT_UBITS	Value	Lock ACT_UBITS	Lock Value (*)
NVM0_LOWER_ALLOWED	NVM0_LOWER_ALLOWED	ACT_UBITS [43:43]	1'h1	N/A	N/A
NVM0_UPPER_M3ACCESS	NVM0_UPPER_M3ACCESS	ACT_UBITS [44:44]	1'h1	N/A	N/A
NVM0_UPPER_FABRIC_ACCESS	NVM0_UPPER_FABRIC_ACCESS	ACT_UBITS [45:45]	1'h1	N/A	N/A
NVM0_UPPER_OTHERS_ACCESS	NVM0_UPPER_OTHERS_ACCESS	ACT_UBITS [46:46]	1'h1	N/A	N/A
NVM0_UPPER_ALLOWED	NVM0_UPPER_ALLOWED	ACT_UBITS [47:47]	1'h1	N/A	N/A
NVM1_LOWER_M3ACCESS	NVM1_LOWER_M3ACCESS	ACT_UBITS [48:48]	1'h1	N/A	N/A
NVM1_LOWER_FABRIC_ACCESS	NVM1_LOWER_FABRIC_ACCESS	ACT_UBITS [49:49]	1'h1	N/A	N/A
NVM1_LOWER_OTHERS_ACCESS	NVM1_LOWER_OTHERS_ACCES	ACT_UBITS [50:50]	1'h1	N/A	N/A
NVM1_LOWER_ALLOWED	NVM1_LOWER_ALLOWED	ACT_UBITS [51:51]	1'h1	N/A	N/A
NVM1_UPPER_M3ACCESS	NVM1_UPPER_M3ACCESS	ACT_UBITS [52:52]	1'h1	N/A	N/A
NVM1_UPPER_FABRIC_ACCESS	NVM1_UPPER_FABRIC_ACCESS	ACT_UBITS [53:53]	1'h1	N/A	N/A
NVM1_UPPER_OTHERS_ACCESS	NVM1_UPPER_OTHERS_ACCESS	ACT_UBITS [54:54]	1'h1	N/A	N/A
NVM1_UPPER_ALLOWED	NVM1_UPPER_ALLOWED	ACT_UBITS [55:55]	1'h1	N/A	N/A

Note: Lock Value (*) = 0, disables modification of the Register field.

Table 24 • **System controller/M3 Settings**

Function	Enabled
System controller suspended mode	No
M3	No

Table 25 • **CCC-SW0 (Unused pin tie-off)**

Input Pin3	Tie-Off
PLL_POWERDOWN_N	0
PRESET_N	1
NGMUX0_ARST_N	1
NGMUX1_ARST_N	1
NGMUX2_ARST_N	1
NGMUX3_ARST_N	1
PLL_ARST_N	1
GPD0_ARST_N	1
GPD1_ARST_N	1
GPD2_ARST_N	1
GPD3_ARST_N	1
CLK0	1
CLK1	1
CLK2	1
CLK3	1
PCLK	1

Table 26 • **CCC-SW1 (Unused pin tie-off)**

Input Pin	Tie-Off
PLL_POWERDOWN_N	0
PRESET_N	1
NGMUX0_ARST_N	1
NGMUX1_ARST_N	1
NGMUX2_ARST_N	1
NGMUX3_ARST_N	1
PLL_ARST_N	1
GPD0_ARST_N	1
GPD1_ARST_N	1
GPD2_ARST_N	1
GPD3_ARST_N	1
CLK0	1
CLK1	1
CLK2	1
CLK3	1
PCLK	1

Table 27 • CCC-SE0 (Unused pin tie-off)

Input Pin	Tie-Off
PLL_POWERDOWN_N	0
PRESET_N	1
NGMUX0_ARST_N	1
NGMUX1_ARST_N	1
NGMUX2_ARST_N	1
NGMUX3_ARST_N	1
PLL_ARST_N	1
GPD0_ARST_N	1
GPD1_ARST_N	1
GPD2_ARST_N	1
GPD3_ARST_N	1
CLK0	1
CLK1	1
CLK2	1
CLK3	1
PCLK	1

Table 28 • CCC-SE1 (Unused pin tie-off)

Input Pin	Tie-Off
PLL_POWERDOWN_N	0
PRESET_N	1
NGMUX0_ARST_N	1
NGMUX1_ARST_N	1
NGMUX2_ARST_N	1
NGMUX3_ARST_N	1
PLL_ARST_N	1
GPD0_ARST_N	1
GPD1_ARST_N	1
GPD2_ARST_N	1
GPD3_ARST_N	1
CLK0	1
CLK1	1
CLK2	1
CLK3	1
PCLK	1

Table 29 • **CCC-NW0 (Unused pin tie-off)**

Input Pin	Tie-Off
PLL_POWERDOWN_N	0
PRESET_N	1
NGMUX0_ARST_N	1
NGMUX1_ARST_N	1
NGMUX2_ARST_N	1
NGMUX3_ARST_N	1
PLL_ARST_N	1
GPD0_ARST_N	1
GPD1_ARST_N	1
GPD2_ARST_N	1
GPD3_ARST_N	1
CLK0	1
CLK1	1
CLK2	1
CLK3	1
PCLK	1

Table 30 • **CCC-NW1 (Unused pin tie-off)**

Input Pin	Tie-Off
PLL_POWERDOWN_N	0
PRESET_N	1
NGMUX0_ARST_N	1
NGMUX1_ARST_N	1
NGMUX2_ARST_N	1
NGMUX3_ARST_N	1
PLL_ARST_N	1
GPD0_ARST_N	1
GPD1_ARST_N	1
GPD2_ARST_N	1
GPD3_ARST_N	1
CLK0	1
CLK1	1
CLK2	1
CLK3	1
PCLK	1

Table 31 • **CCC-NE0 (Unused pin tie-off)**

Input Pin	Tie-Off
PLL_POWERDOWN_N	0
PRESET_N	1
NGMUX0_ARST_N	1
NGMUX1_ARST_N	1
NGMUX2_ARST_N	1
NGMUX3_ARST_N	1
PLL_ARST_N	1
GPD0_ARST_N	1
GPD1_ARST_N	1
GPD2_ARST_N	1
GPD3_ARST_N	1
CLK0	1
CLK1	1
CLK2	1
CLK3	1
PCLK	1

Table 32 • **CCC-NE1 (Unused pin tie-off)**

Input Pin	Tie-Off
PLL_POWERDOWN_N	0
PRESET_N	1
NGMUX0_ARST_N	1
NGMUX1_ARST_N	1
NGMUX2_ARST_N	1
NGMUX3_ARST_N	1
PLL_ARST_N	1
GPD0_ARST_N	1
GPD1_ARST_N	1
GPD2_ARST_N	1
GPD3_ARST_N	1
CLK0	1
CLK1	1
CLK2	1
CLK3	1
PCLK	1

Table 33 • **FDDR (Unused pin tie-off)**

Input Pin	Tie-Off
PRESET_N	0
FPGA_FDDR_ARESET_N	1
CLK_BASE	1
PCLK	1

Table 34 • **HPMS/MDDR (Unused pin tie-off)**

Input Pin	Tie-Off
FAB_M3_RESET_N	0
USER_MSS_GPIO_RESET_N	0
FPGA_MDDR_ARESET_N	0
PRESET_N	0
USER_MSS_RESET_N	1
CLK_BASE	1
GTX_CLKPF	1
I2C0_BCLK	1
I2C1_BCLK	1
RX_CLKPF	1
SPI0_CLK_IN	1
SPI1_CLK_IN	1
TX_CLKPF	1
XCLK_FAB	1
CLK_MDDR_APB	1

Table 35 • **PCIE0 (Unused pin tie-off)**

Input Pin	Tie-Off
SERDESIF_CORE_RESET_N	0
SERDESIF_PHY_RESET_N	0
APB_RSTN	0
EPCS_PWRDN[1:0]	11
EPCS_RSTN[1:0]	11
PERST_N	1
APB_CLK	1
CLK_BASE	1
FAB_REF_CLK	1
XAUI_FB_CLK	1
FAB_REF_CLK	1

Table 36 • **PCIE1 (Unused pin tie-off)**

Input Pin	Tie-Off
SERDESIF_CORE_RESET_N	0
SERDESIF_PHY_RESET_N	0
APB_RSTN	0
EPCS_PWRDN[1:0]	11
EPCS_RSTN[1:0]	11
PERST_N	1
APB_CLK	1
CLK_BASE	1
FAB_REF_CLK	1
XAUI_FB_CLK	1
FAB_REF_CLK	1

Table 37 • **PCIE2 (Unused pin tie-off)**

Input Pin	Tie-Off
SERDESIF_CORE_RESET_N	0
SERDESIF_PHY_RESET_N	0
APB_RSTN	0
EPCS_PWRDN[1:0]	11
EPCS_RSTN[1:0]	11
PERST_N	1
APB_CLK	1
CLK_BASE	1
FAB_REF_CLK	1
XAUI_FB_CLK	1
FAB_REF_CLK	1

Table 38 • **PCIE3 (Unused pin tie-off)**

Input Pin	Tie-Off
SERDESIF_CORE_RESET_N	0
SERDESIF_PHY_RESET_N	0
APB_RSTN	0
EPCS_PWRDN[1:0]	11
EPCS_RSTN[1:0]	11
PERST_N	1
APB_CLK	1
CLK_BASE	1
FAB_REF_CLK	1
XAUI_FB_CLK	1
FAB_REF_CLK	1