# Timing Analysis of RTAX-S/SL/DSP Design Using Libero IDE v9.2

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## Introduction

This application note describes timing data enhancements for RTAX™-S/SL/DSP designs in Libero® IDE v9.2. It also provides general guidance for performing static timing analysis of the RTAX-S/SL/DSP design using the SmartTime tool in Libero IDE v9.2.

SmartTime is a gate-level static timing analysis tool for Microsemi® FGPAs that assists you to perform complete timing analysis. It also ensures that the designs meet all timing constraints and that they operate at a desired speed with the right amount of margin across all operating conditions. SmartTime Timing Analyzer has two default analysis views: Maximum Delay Analysis and Minimum Delay Analysis. Maximum Delay Analysis, also known as setup check, calculates the maximum delay analysis under worst-case operating conditions. Minimum Delay Analysis, also known as hold check, calculates the minimum delay analysis under best-case operating conditions. You can also change the operating condition in SmartTime and run timing analysis for other operating conditions. This application note has been written with an assumption that you are familiar with timing analysis using SmartTime tool in Libero IDE. Refer to *SmartTime User Guide* for more information on using the SmartTime tool.

You need not run analysis again on most of the existing RTAX-S/SL/DSP designs using Libero IDE v9.2 due to the timing improvement in Libero IDE v9.2. Designs that do not require analysis to be repeated are the typical synchronous designs that use only the hard-wired clocks (H-clock) or routed clocks (R-clock) for clock network with no combinatorial logic, or regular routing in the clock network. For these type of designs, the setup time will be worst during the maximum delay analysis under the worst-case operating conditions, and the hold time will be worst during the minimum delay analysis under best-case operating conditions. SmartTime default analysis view covers these two corners (Maximum Delay Analysis view shows worst case setup and Minimum Delay Analysis view shows the best case hold setup).

On the other hand, the timing improvement in Libero IDE v9.2 might impact designs with complex clocking schemes, such as gated clocks that use regular routing resources in the clock path. These type of designs might have worst-case slack on non-default corners, meaning the setup time will be worst under best-case conditions, or the hold time will be worst under worst-case conditions. For these type of designs, you need to run maximum and minimum analysis using the default and non-default corners.

Note: The general recommendation for RTAX-S/SL/DSP designs is to perform timing analysis in all four corners. General guidance for four-corner timing analysis will be provided in this application note.

# Timing Delays in Static Timing Analysis Tool

During timing analysis, the setup check involves comparing the latest data arrival time with the earliest data required time. The hold check involves comparing the earliest data arrival time with the latest data required time. The latest data arrival time is obtained by calculating the longest path delay to get to the timing check point. The earliest data required time is obtained by calculating the shortest clock insertion delay to get to the timing check point.The setup check uses EQ 1 and EQ 2:

Longest data path = Σ Tmax (data path)

*EQ 1*

Shortest clock path = Σ Tmin (clock path)

*EQ 2*

The hold check uses EQ 3 and EQ 4:

Longest clock path = Σ Tmax (clock path)

*EQ 3*

Shortest data path = Σ Tmin (data path)

*EQ 4*

To calculate the clock path and data path delays for longest or shortest path, you must set the appropriate combinations of process, voltage, and temperature to allow timing variation across various corners. Even for a given operating conditions of PVT (P = Process, V = Voltage, T = Temperature), each component on a timing path represents a delay variation between a maximum delay (Tmax) and a minimum delay (Tmin). These variations as shown in Figure 1, are due to the static approach of timing analysis, the dynamic context, and other modeling considerations are unknown. During dynamic simulation, all the input conditions of a logic are known and a proper timing model can be applied; whereas during static analysis, only the worst and best configurations are used to check for potential timing violations. During timing check, the latest data arrival or required time is computed and the timing analysis tool is expected to use Tmax of each component on the timing path. Similarly, Tmin is used in the computation of the earliest arrival or required time. Tmin is a conservative calculation of the lower bound of a propagation delay, considering the delay distribution of a component under specific operating conditions.

Note: Both Tmin and Tmax vary each time a new set of operating conditions is chosen for analysis.

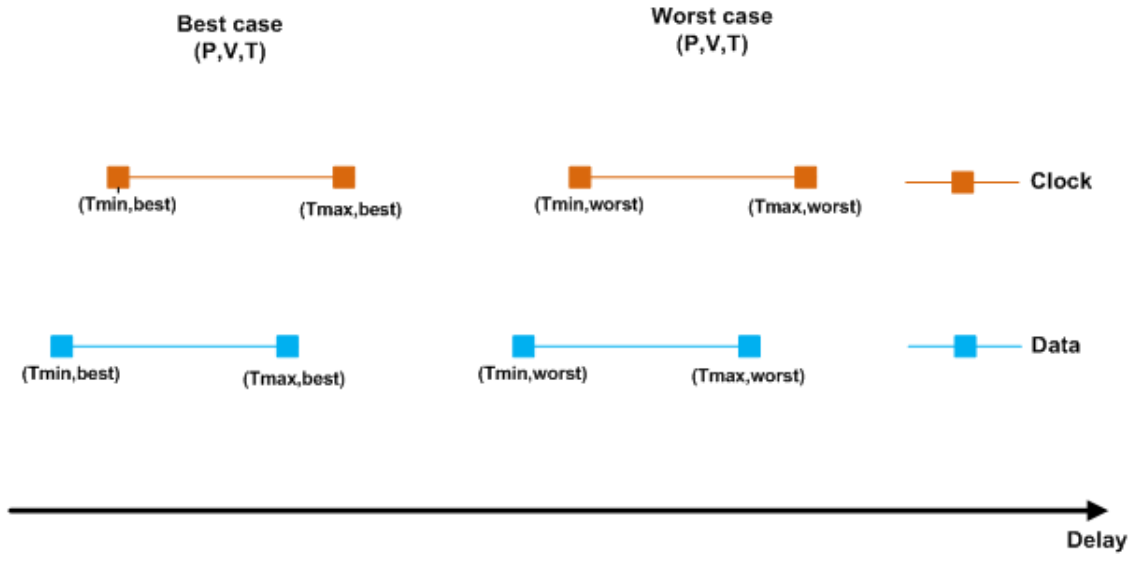



***Figure 1* • Timing Delays Under Various Conditions**

Another consideration is related to the process variation when analyzing multiple dies for a given speed grade. For a specific timing check, both the arrival and required times are computed using either the slowest die for a worst-case analysis or the fastest die for a best-case analysis. But in both the cases, delays involved in a given timing check, such as external setup and hold, are computed considering the variation on the same die.

The static timing analysis tool is expected to use the appropriate Tmax and Tmin for setup and hold calculation. However, traditionally, the FPGA static timing analysis tools are mainly focused on worst case scenarios and require you to add margin for other corners. Microsemi's SmartTime timing analysis tool uses Tmin value for calculating the arrival or required time since Libero v6.3. In Libero IDE v9.2, this model is improved, therefore allowing accurate modeling for both the maximum and minimum timing analysis corners.

# Timing Enhancements in Libero IDE v9.2

SmartTime in Libero IDE v9.2 contains several updates in timing number and calculation compared to SmartTime in Libero IDE v9.1 SP5. These changes are for Axcelerator and RTAX-S/SL/DSP families only. The timing data and timing calculation changes in Libero IDE v9.2 are:

- SmartTime in Libero IDE v9.2 uses Tmin on data path for the worst case hold check
- SmartTime in Libero IDE v9.2 uses fastest silicon timing number for the best case setup check
- The value of Tmin is improved (it reduces the spread between Tmin and Tmax values)

Table 1 summarizes the enhancements in Libero IDE v9.2 compared to Libero IDE v9.1SP5.

***Table 1 •*** **Enhancement in Libero IDE v9.2 Compared to Libero IDE v9.1SP5**

| | | Libero IDE v9.1 SP5 | | Libero IDE v9.2 | |
|---|---|---|---|---|---|
| | | **Best Case** | **Worst Case** | **Best Case** | **Worst Case** |
| Setup | data | Tmax | Tmax | Tmax | Tmax |
| | clock | Tmax | Tmax | Tmax | Tmax |
| | Speed-grade | User setting | User setting | Fastest | User setting |
| Hold | data | Tmin | Tmax | Tmin | Tmin |
| | clock | Tmax | Tmax | Tmax | Tmax |
| | Speed-grade | Fastest | User setting | Fastest | User setting |

Note: Tmin has not been introduced for the clock delay during maximum delay analysis (setup check) for a couple of reasons:

- Microsemi recommends using a dedicated global resource for the clock. A global resource has very low skew and hence very low variation. Microsemi has done internal testing on silicon and found that the variation of clock path delay is very low compared to regular routing delay.
- The Tmax on a data path is sufficiently conservative to cover small variations on the clock network delay. Generating Tmin on a clock network would have added the risk of many false violations for maximum delay analysis (setup check).

# Impact of Libero IDE v9.2 Timing Enhancement on Existing Designs

The timing enhancement in Libero IDE v9.2 does not require you to rerun timing analysis on typical synchronous designs. Figure 2 shows the clocking scheme for these typical designs.

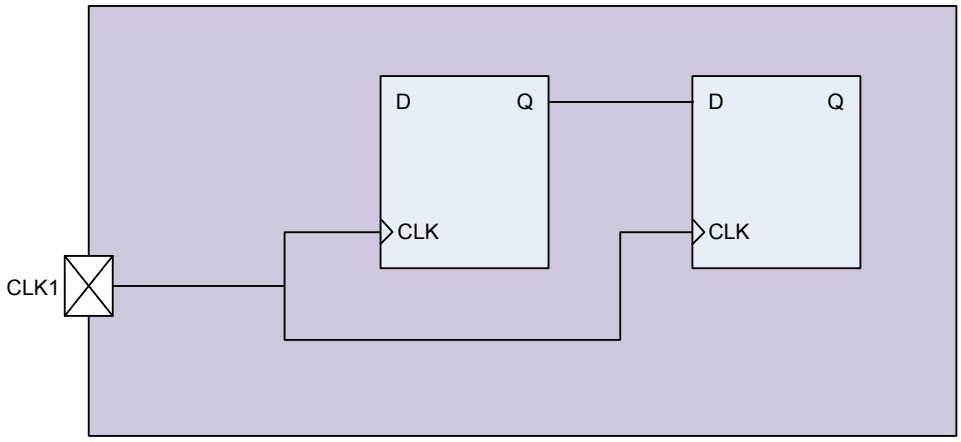
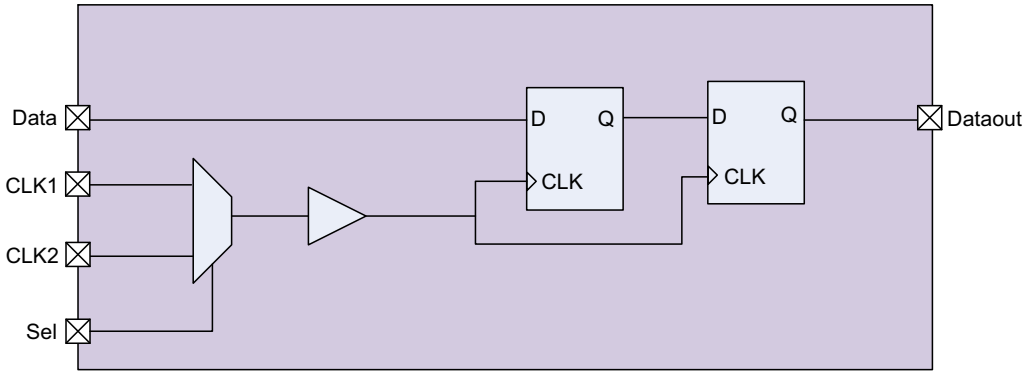



***Figure 2* • Clocking Scheme in Typical Design**

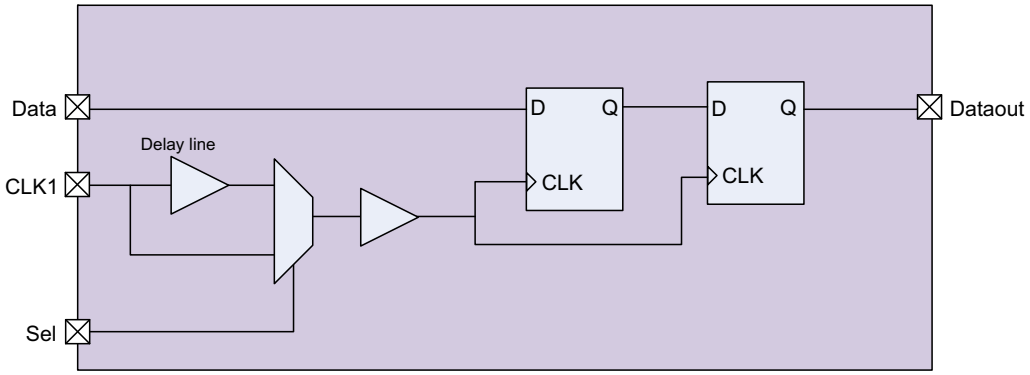
On the other hand, if you have a design with a complex clocking scheme, as previously mentioned, then it is recommended to re-run the timing analysis on all four corners and verifying your design using Libero IDE v9.2.

Figure 3 on page 5 shows an example of complex clocking. In general, it is recommended for all designs to run timing analysis on all the four corners:

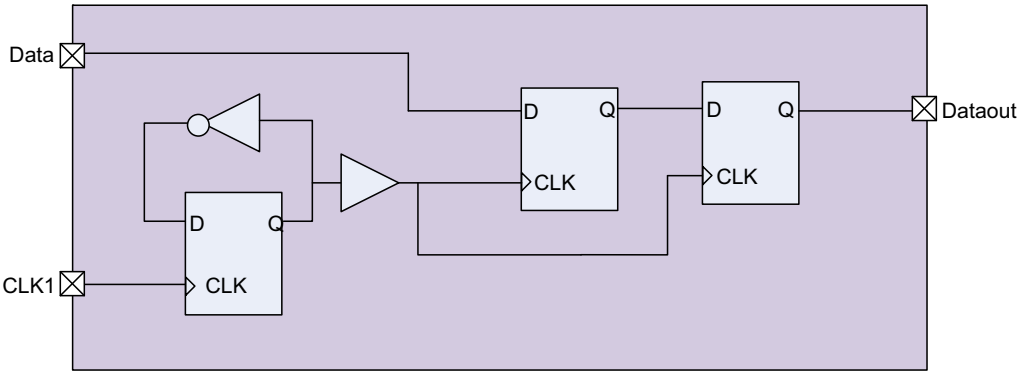
- setup check for worst case,
- setup check for best case,
- hold check for best case and
- hold check for worst case




Complex Clocking Scheme Scenario1




Complex Clocking Scheme Scenario2




Complex Clocking Scheme Scenario3

***Figure 3* • Complex Clocking Scheme**

Note that your design might have multiple clocks and you might have some paths which cross the clock domains. These designs normally have worst-case slack on the two default corners. However, the user must follow the standard practice used for cross clock domain paths and to make sure the data is passed from one clock domain to other clock domain properly. By default, SmartTime does not include the cross-clock domain path during timing analysis for RTAX-S/SL/DSP devices. You need to enable the cross-clock domain paths to run timing analysis on these cross-clock domain paths using SmartTime.

Refer to Inter-Clock Domain Analysis in *AC379: Advanced Static Timing Analysis Using SmartTime* Application Note for details.

# Timing Analysis on All Four Corners

This section describes the detail procedure for the four-corner timing analysis on a synchronous design. SmartTime default analysis view shows setup analysis for the worst-case operating condition and hold analysis for the best-case operating conditions. You need to change the setting in SmartTime to run analysis on the other corners.

The following sections describe how to change the operating condition in SmartTime and run timing analysis for all four corners using the GUI. In addition, it explains the timing data used during the four-corner timing analysis and explains how SmartTime performs the calculations.

Note: The four-corner analysis can also be accomplished by running a series of commands in tool command language (TCL).

"Appendix- A: TCL Script Example Showing Four Corner Analysis" on page 20 shows a simple TCL example that runs four corner timing analysis and reports the violation in a design. This is a very quick way to check timing analysis provided you have applied all the required timing constraints.

Figure 4 shows a simple synchronous design that is used to illustrate the various timing checks. There are four types of timing paths in a synchronous design:

- Input to Register: External setup and external hold calculation is used for this type of path.
- Register to Register: Register to register setup and hold calculation is used for this type of path.
- Register to Output: Clock-to-Output calculation is used for this type of path.
- Input-to-Output: Input to output is used for this type of path.

SmartTime GUI shows all the four timing path types as the default path in Figure 5.

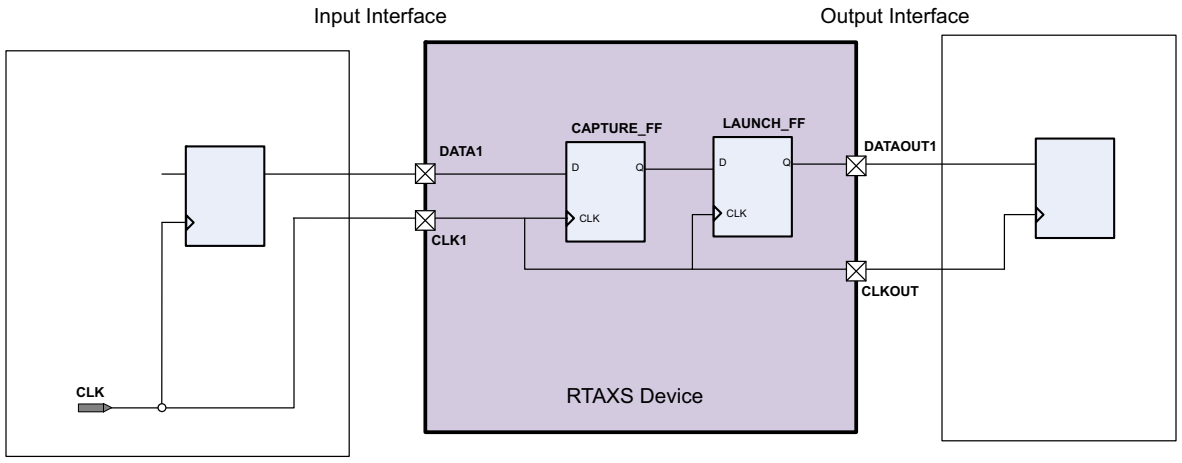



***Figure 4* • Simple Synchronous Design**

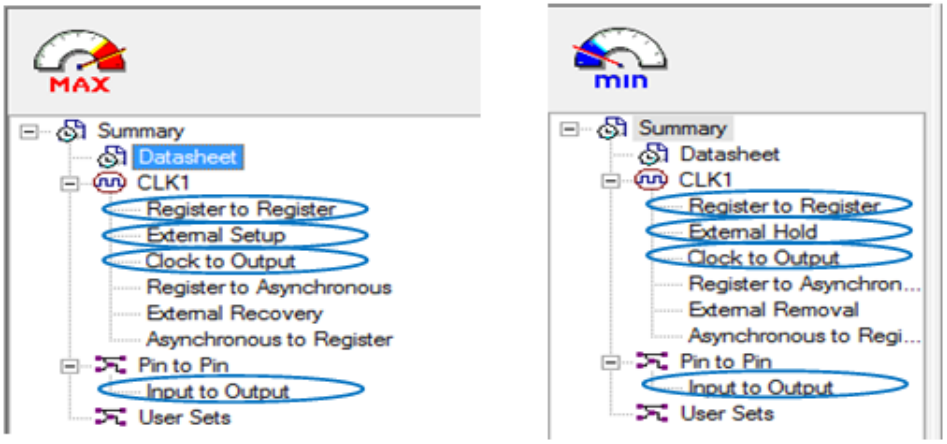



***Figure 5* • External Setup and External Hold and Clock-to-Output in SmartTime GUI**

The following steps are required before performing timing analysis:

1. Set the desired temperature and voltage conditions (operating ranges) in the Device Selection Wizard as shown in Figure 6.

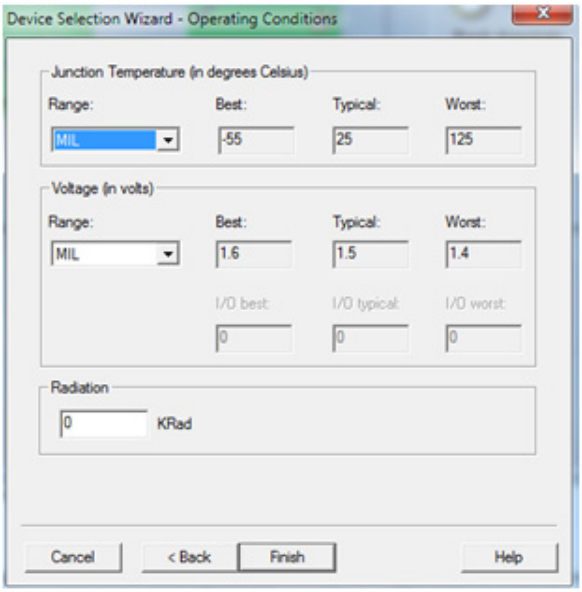



***Figure 6* • Setting Conditions in the Device Selection Wizard**

2. Apply the appropriate timing constraint. You can use the following SDC or use the GUI to apply the constraints.

```
create_clock  -name { CLK1 } -period 12.500 -waveform { 0.000 6.250  }  { CLK1  }
set_input_delay 0.000 -clock { CLK1 }  [get_ports { DATA1 }]
set_max_delay 2.500 -from [get_ports { DATA1 }]  -to [get_clocks {CLK1}]
set_min_delay 2.000 -from [get_ports { DATA1 }]  -to [get_clocks {CLK1}]
set_output_delay 0.000 -clock { CLK1 }  [get_ports { DATAOUT1 }]
set_max_delay 2.500 -from [get_clocks {CLK1}]  -to [get_ports { DATAOUT1 }]
set_min_delay 2.000 -from [get_clocks {CLK1}]  -to [get_ports { DATAOUT1 }]
```

The following sections describe in detail the steps for four-corner analysis of timing paths and modeling of Tmin and Tmax in each situation. Delays from a real implementation of the design shown in Figure 4 are used on a RTAX-S/SL/DSP device with -1 speed grade.

## Input to Register Path Timing Analysis

This section describes the timing check calculation for input to register path. This is done usually with external setup and external hold calculation.

To calculate the external setup or hold time, timing analysis involves the shortest and longest paths between DATA1 and CAPTURE_FF:D, as well as the shortest and longest paths between CLK and CAPTURE_FF:CLK. Both the rising edge and the falling edge data-path propagation must be evaluated. In addition, the analysis is also performed under two operating condition sets, best case and worst case.

External hold calculation under best and worst case condition is shown in EQ 5 and EQ 6:

ExtHold_best = Tmax,best(clk) – Tmin,best(data) – FF_Hold

*EQ 5*

ExtHold_worst = Tmax,worst(clk) – Tmin,worst(data) – FF_Hold

*EQ 6*

External setup calculation under best and worst case condition is shown in EQ 7 and EQ :

ExtSetup_best = Tmax,best(data) – Tmin,best(clk) + FF_Setup

*EQ 7*

ExtSetup_worst = Tmax,worst(data) – Tmin,worst(clk) + FF_Setup

SmartTime, by default, shows the analysis and calculation for ExtHold_best and ExtSetup_worst. To calculate ExtHold_worst and ExtSetup_best, you need to apply the appropriate conditions in SmartTime. For the typical design, the slack will be worst for ExtHold_best and ExtSetup_worst, and the SmartTime default setting will show the analysis results. For complex clocking designs, you need to look at the slack for all four conditions. The following section shows the steps for applying the appropriate setting to calculate all the four conditions.

### *External Hold Calculation under Best-Case Conditions*

To calculate external hold under best-case conditions, use the Minimum Delay Analysis capability in SmartTime, which directly applies EQ 5 by computing Tmax,best(clk) and Tmin,best(data). Under the best case conditions, SmartTime Minimum Delay Analysis does the following:

- Assumes that the silicon die being analyzed is the fastest possible, regardless of the requested speed grade. Allows a conservative calculation for a STD speed grade part. Note that the customer can receive -1 speed grade part even though they order –STD. Microsemi does not guarantee that the shipping part cannot be faster silicon than ordered.
- Computes Tmax and Tmin on every component along the clock path (Tmax) and the data path (Tmin).

The flow and the numeric results for this example are shown below:

1. Ensure that the minimum delay analysis is set to **BEST**, as shown in Figure 7. This is usually the default setting.

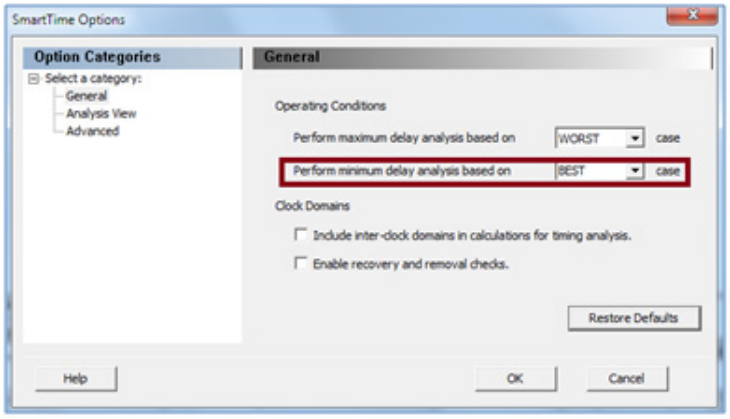



***Figure 7* • Default External Setup Calculation by SmartTime**

2. In Minimum Delay Analysis view, get the external hold time, as shown in Figure 8.

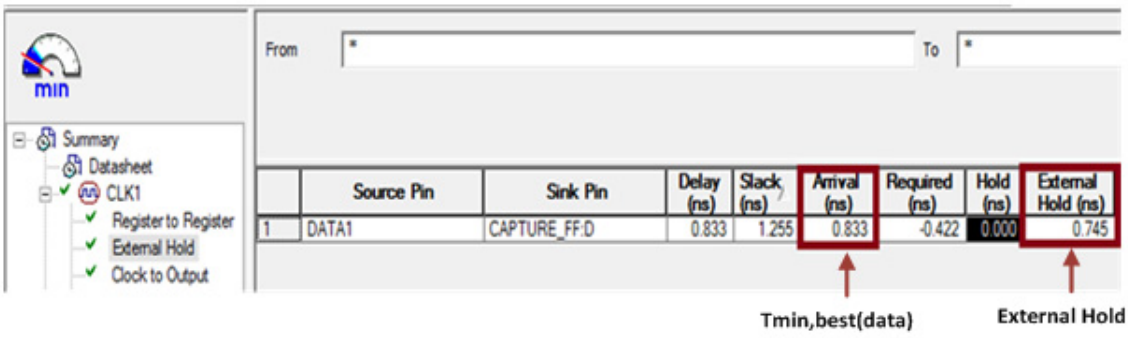



***Figure 8* • SmartTime Best Case Setup Analysis**

As shown in GUI, SmartTime does the calculation and displays the result for calculating the external hold time. You are not required to do any manual calculation. However for reference, EQ 8 shows the calculation for the external hold time under the best-case condition:

External hold time under best case =Tmax,best(clk) – Tmin,best(data) – FF_Hold

= 1.578 – 0.833 – 0 = 0.745

*EQ 8*

The Tmin,best(data) value is shown in the GUI as 0.833 ns. The Tmax,best(clk) value can be derived from the required time (-0.422ns) and the external hold constraint (2ns) =2+ (-0.422)=1.578 ns.

Table 2 tabulates the result.

***Table 2* • Minimum Best Data and Maximum Best-Clock Values**

| | Minimum Best | Maximum Best | Minimum Worst | Maximum Worst |
|---|---|---|---|---|
| Data | 0.833 | | | |
| Clock | | 1.578 | | |

## External Hold Calculation Under Worst-Case Conditions

Under worst-case conditions, SmartTime minimum delay analysis:

- Assumes that the silicon die being analyzed is the one at the slowest speed specified by the speed grade requested in the device selection wizard.
- Computes Tmax and Tmin on every component along the clock path (Tmax) and the data path (Tmin).

Minimum delay analysis capability in SmartTime directly applies EQ 6 on page 8 by computing Tmax,worst(clk) and Tmin,worst(data). The steps and the numeric results for this example are shown below:

1. Keep the same temperature and voltage settings in the **Device Selection Wizard**.
2. Open the **SmartTime Options** window and set **Perform minimum delay analysis based on** to **WORST** case conditions, as shown in Figure 9.

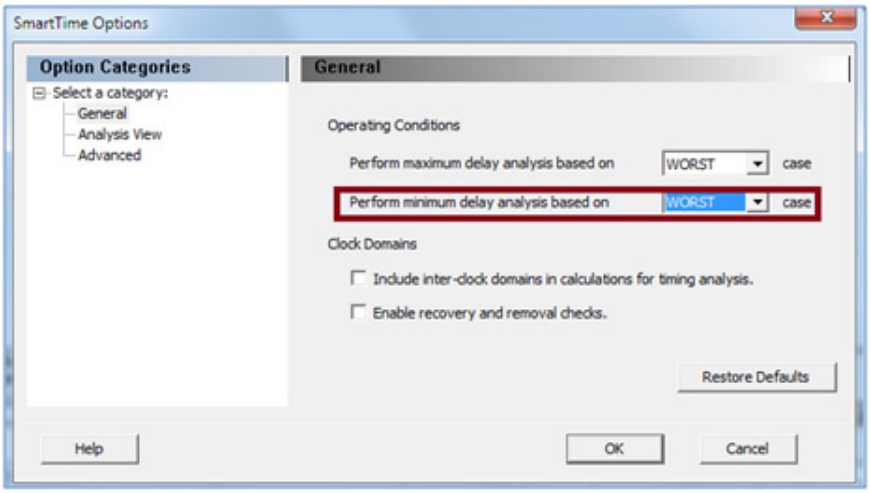



***Figure 9* • SmartTime Setting for Worst Case Hold Analysis**

3. In minimum delay analysis view, get the external hold time, as shown in Figure 10.

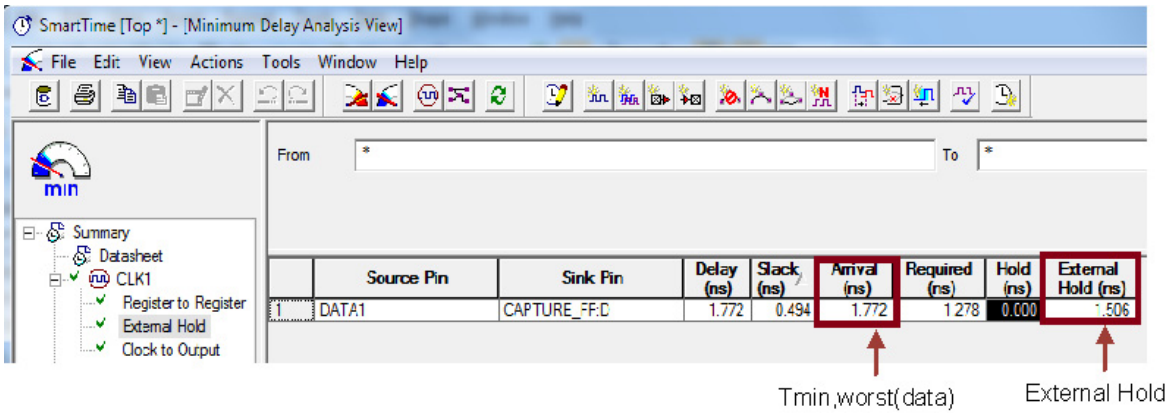



***Figure 10* • SmartTime Worst Case Hold Analysis**

SmartTime does the calculation and displays the result and you are not required to do any manual calculation. However for reference, EQ 9 shows the calculation for the external hold time under best case:

External hold time for the worst-case condition:

= Tmax,worst(clk) – Tmin,worst (data) – FF_Hold

= 3.278 – 1.772 – 0 = 1.506

*EQ 9*

The Tmin,worst (data) value is shown in GUI (Arrival column) and the Tmax,worst(clk) value can be derived from the required time (1.278 ns) and the external setup constraint(2ns) =2 + 1.278=3.278 ns. Table 3 tabulates the results.

***Table 3 •*** **Minimum Worst Data and Maximum Worst-Clock Values**

| | Minimum Best | Maximum Best | Minimum Worst | Maximum Worst |
|---|---|---|---|---|
| Data | 0.833 | | 1.772 | |
| Clock | | 1.578 | | 3.278 |

## External Setup Calculation under Worst-Case Conditions

To calculate the external setup under worst-case conditions, use the Maximum Delay Analysis capability in SmartTime. SmartTime computes the external setup time under worst case and displays the result. However, SmartTime does not use EQ  on page 8. SmartTime uses Tmax, worst(data) for calculation. However, Tmin,worst(clock) is not used for the clock delay. Instead, SmartTime computes and uses Tmax,worst(clock) as explained in “Timing enhancements in Libero v9.2” section. Adding Tmin,worst(clock) in the calculation would have produced an extremely conservative timing requirement with a high probability for multiple false violations.

The following steps describe the external setup calculation as currently implemented in SmartTime:

1. Keep the same temperature and voltage settings in the **Device Selection Wizard**.
2. Open the **SmartTime Options** window and set **Perform maximum delay analysis based on** options to **WORST** case conditions, as shown in Figure 11.

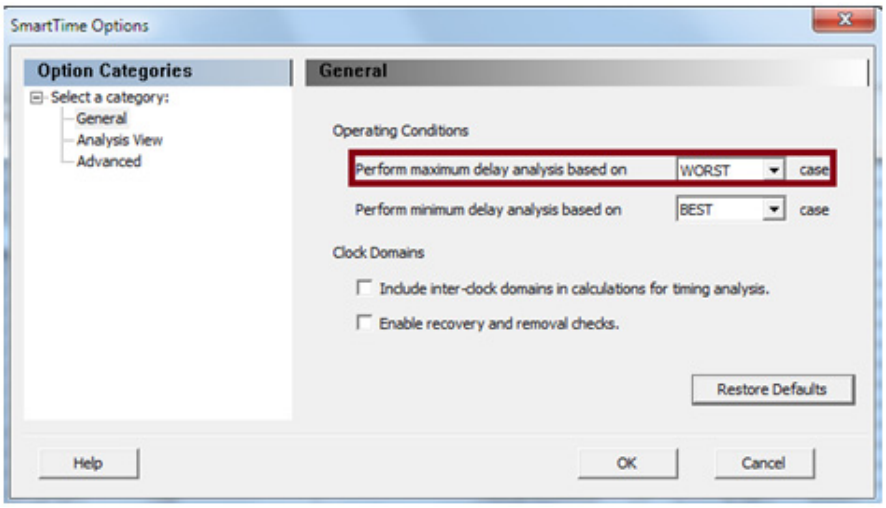



***Figure 11 •*** **SmartTime Setting for Worst Case Setup Analysis**

3. In the Maximum Delay Analysis view, get the external setup time, as shown in Figure 12.

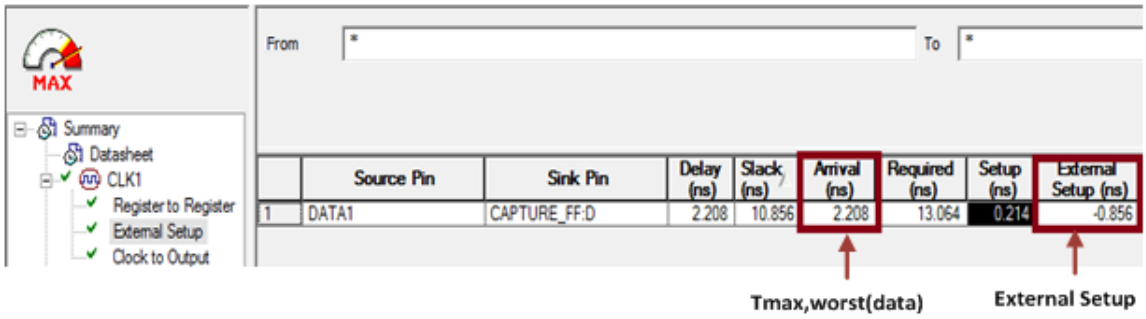



***Figure 12 •*** **SmartTime Worst Case Setup Analysis**

Again, SmartTime does the calculation and displays the results and you are not required to do any manual calculation.

External Setup time for worst case:

=Tmax,worst(data) – Tmax,worst(clk) + FF_Setup

= 2.208 – 3.278 + 0.214 = –0.856

*EQ 10*

The Tmax,worst(data) value is shown in GUI and the Tmax,worst(clk) is the same as Tmin,worst(clock) because for the purpose of timing check (external setup), the clock variation is small, and Tmax and worst(data) has enough built-in margin.

Table 4 tabulates the results.

***Table 4 •*** **Maximum Worst Data and Minimum Worst-Clock Values**

| | Minimum Best | Maximum Best | Minimum Worst | Maximum Worst |
|---|---|---|---|---|
| Data | 0.833 | | 1.772 | 2.208 |
| Clock | | 1.578 | 3.278 | 3.278 |

## External Setup Calculation under Best-Case Conditions

Continue to use the maximum delay analysis capability in SmartTime.

1. Open the **SmartTime Options** window and set **Perform maximum delay analysis based on** options to **BEST** case conditions, as shown in the Figure 13.

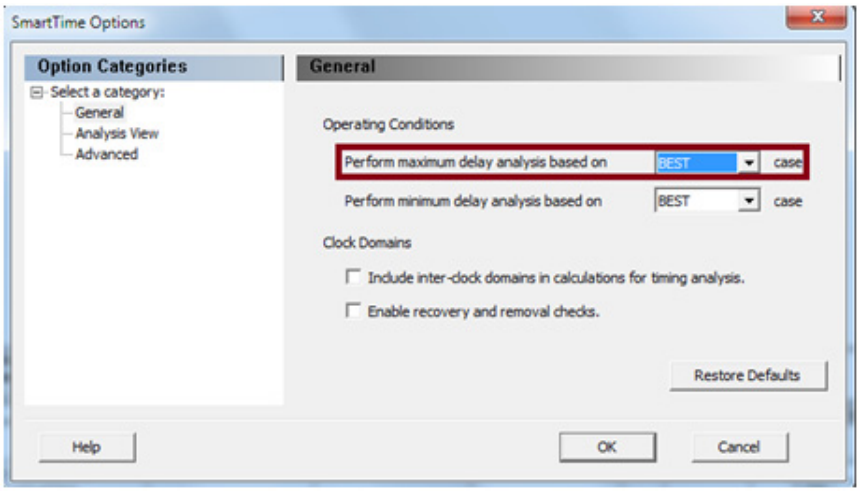



***Figure 13* • SmartTime Setting for Best-Case Setup Analysis**

2. In the Maximum Delay Analysis view, get the external setup time, as shown in the Figure 14.

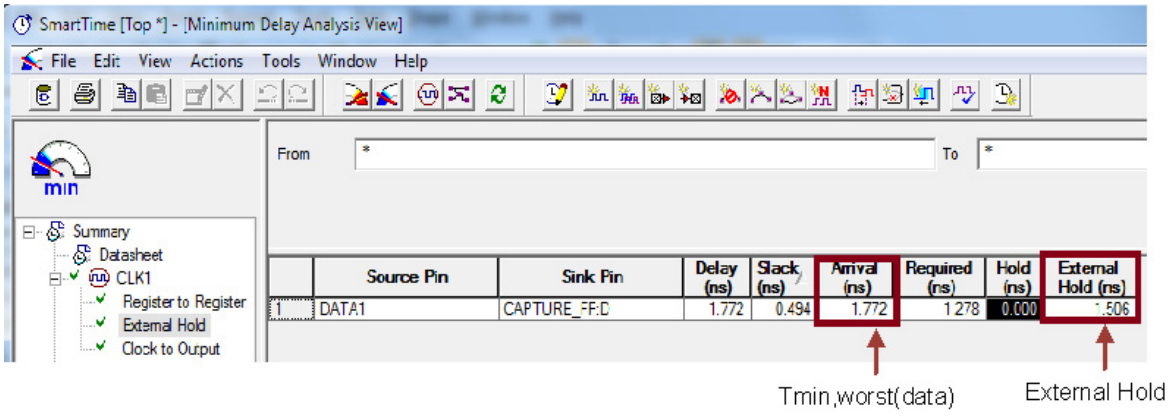



***Figure 14* • SmartTime Setting for Worst-Case Hold Analysis**

External Setup time for best case

=Tmax,best(data) – Tmin,best(clk) + FF_Setup

= 1.052 – 1.578 + 0.103 = –0.423

*EQ 11*

The Tmax,best(data) value is shown in GUI and the Tmin,best(clk) is same as Tmin,best(clk) because for timing check (external setup), clock variation is small and Tmax,best(data) has enough built-in margin.

The final minimum and maximum delay for data and clock under various conditions for the external setup are shown in Table 5:

***Table 5 •*** **Minimum Worst Data and Maximum Worst-Clock Values for Libero IDE v9.2**

| | Minimum Best | Maximum Best | Minimum Worst | Maximum Worst |
|---|---|---|---|---|
| Data | 0.833 | 1.052 | 1.772 | 2.208 |
| Clock | 1.578 | 1.578 | 3.278 | 3.278 |

Table 6 shows the Tmax and Tmin for clock and data Libero IDE v9.1 SP5:

***Table 6 •*** **Minimum Worst Data and Maximum Worst-Clock Values for Libero IDE v9.1 SP5**

| | Minimum Best | Maximum Best | Minimum Worst | Maximum Worst |
|---|---|---|---|---|
| Data | 0.791 | 1.234 | 2.164 | 2.208 |
| Clock | 1.802 | 1.578 | 3.278 | 3.278 |

Table 7 shows the external setup and external hold time for the same design using Libero IDE v9.2 and Libero v9.1 SP5. As you can see the external hold time is worst for the best case and external setup time is worst for worst case in both Libero v9.1 SP5 and Libero IDE v9.2, as expected for a typical design.

***Table 7 •*** **External Setup and Hold Time Using a Typical Design in Libero IDE v9.2 and Libero IDE v9.1 SP5**

| | Libero IDE v9.2 | Libero IDE v9.1 SP5 |
|---|---|---|
| External Hold time for best case | 0.745 | 0.787 |
| External Hold time for worst case | 1.506 | 1.114 |
| External Setup time for worst case | –0.856 | –0.856 |
| External Setup time for best case | –0.423 | -0.451 |

## Register to Register Path Timing Analysis

The maximum and minimum delay analysis for the register to register path can be done using a similar procedure as the external setup and hold path timing analysis.

Table 8 shows the register to register path setup and hold time for the same design using Libero IDE v9.2 and Libero IDE v9.1 SP5.

***Table 8 •*** **Slack for Reg-Reg Path Using a Typical Design in Libero IDE v9.2 and Libero IDE v9.1 SP5**

| | Libero IDE v9.2 | Libero IDE v9.1 SP5 |
|---|---|---|
| Slack calculation for best case reg-reg hold | 0.705 | 0.65 |
| Slack calculation for worst case reg-reg hold | 1.525 | 2.009 |
| Slack calculation for worst case reg-reg setup | 10.237 | 10.237 |
| Slack calculation for best case reg-reg setup | 11.401 | 11.279 |

Again, it can be seen that the hold time is worst for the best case and setup time is worst for worst case in both Libero IDE v9.1 SP5 and Libero IDE v9.2.

## Register to Output Path Timing Analysis

This section describes the timing check calculation for register to output path, which is also known as Clock-to-Output path. The Clock-to-Output path set is also shown as a default path set in the SmartTime GUI. Using the appropriate conditions, you can find the minimum and maximum delay for Clock-to-Output.

The Clock-to-Output calculation can be two types:

- Clock-to-Output for regular synchronous design
- Clock-to-Output for source synchronous designs

### *Clock-to-Output for Regular Synchronous Designs*

For a synchronous design, the Clock-to-Output path in SmartTime shows the best and worst case Clock-to-Output delay.

### *Clock-to-Output Calculation under Best-Case Conditions*

To calculate best Clock-to-Output, use the minimum delay analysis capability in SmartTime to calculate Tmin,best(data).

1. Ensure that the setting for minimum delay analysis is set to **BEST,** as shown in the Figure 7 on page 9. This is usually the default in **SmartTime Options** window.
2. In the Minimum Delay Analysis view, examine the **Clock-to-Output** path set to get Tmin, best(data), as shown in Figure 15.

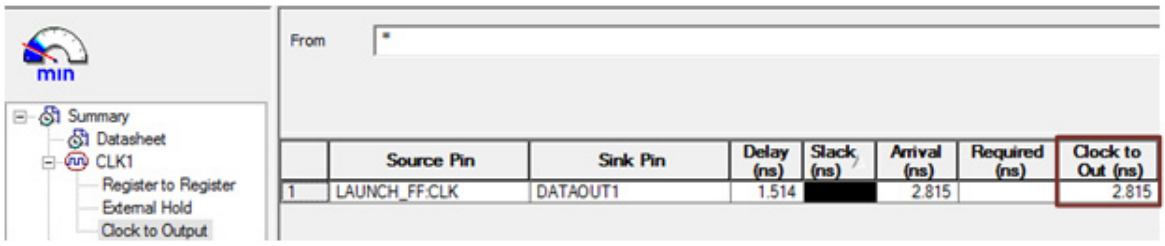



***Figure 15* • SmartTime Showing Clock-to-Output Delay for Minimum Delay Analysis**

### *Clock-to-Output Calculation under Worst-Case Condition*

To calculate the worst Clock-to-Output, use the Maximum Delay Analysis capability in SmartTime to calculate Tmax,worst(data):

1. Ensure that the setting for Maximum Delay Analysis and Minimum Delay Analysis is set to **WORST**.
2. In Maximum Delay Analysis view, examine the Clock-to-Output path set to get Tmax,worst(datapath), as shown in Figure 16.

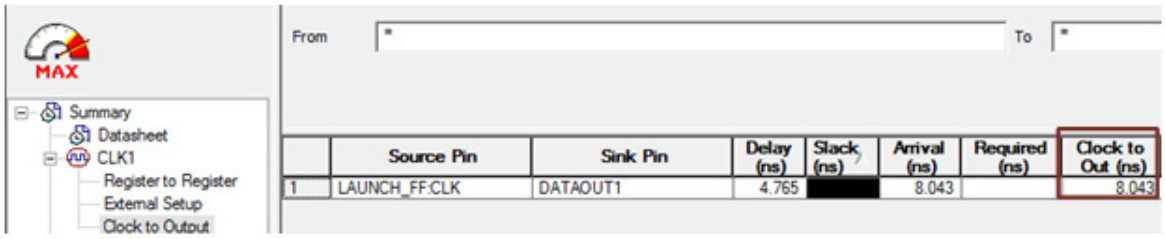



***Figure 16* • SmartTime Showing Clock-to-Output Delay for Maximum Delay Analysis**

## Clock-to-Output for Source Synchronous Designs

For a source synchronous design, the clock is also passed to I/O and the timing checks involve calculating Clock-to-Output delay with respect to clock output. Therefore, delay can be used for performing timing analysis on the other chip. To run setup and hold analysis on a source – synchronous design, refer to the *Source-Synchronous Clock Designs: Timing Constraints and Analysis* application note.

Following equations can be used for calculating the minimum and maximum timing delay for Clock-to-Output with respect to the clock output:

The best and worst Clock-to-Output delay with respect to clock output is shown in EQ 12 and EQ 13:

Best_clk_to_out wrt clkout = Tmin,best (datapath) – Tmax,best(clockpth)

*EQ 12*

Worst_clk_to_out wrt clkout = Tmax,worst(datapath) – Tmin,worst(clockpth)

*EQ 13*

## Clock-to-Output Calculation under Best-Case Conditions

To calculate best Clock-to-Output, use the minimum delay analysis capability in SmartTime to calculate Tmin,best(data), and use maximum delay analysis capability in SmartTime to calculate Tmax,best(clk), and apply EQ 12.

The flow and the numeric results for the example are shown below:

1. Ensure that the setting for Minimum Delay Analysis is set to **BEST** (Figure 7 on page 9). This is usually the default in **SmartTime Options** window.
2. In the Minimum Delay Analysis view, examine the **Clock to Out** path set to get Tmin, best (data), as shown in Figure 17.

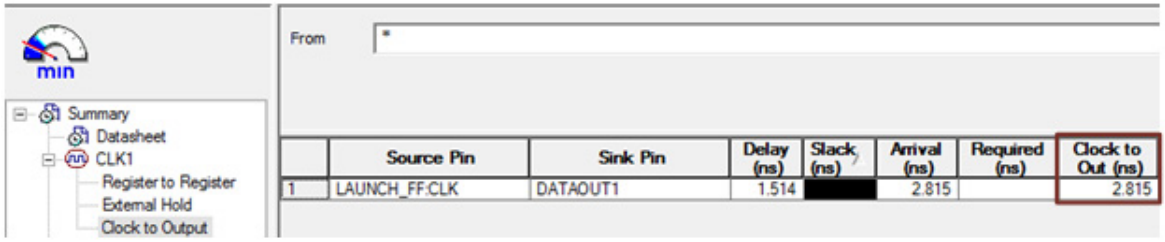
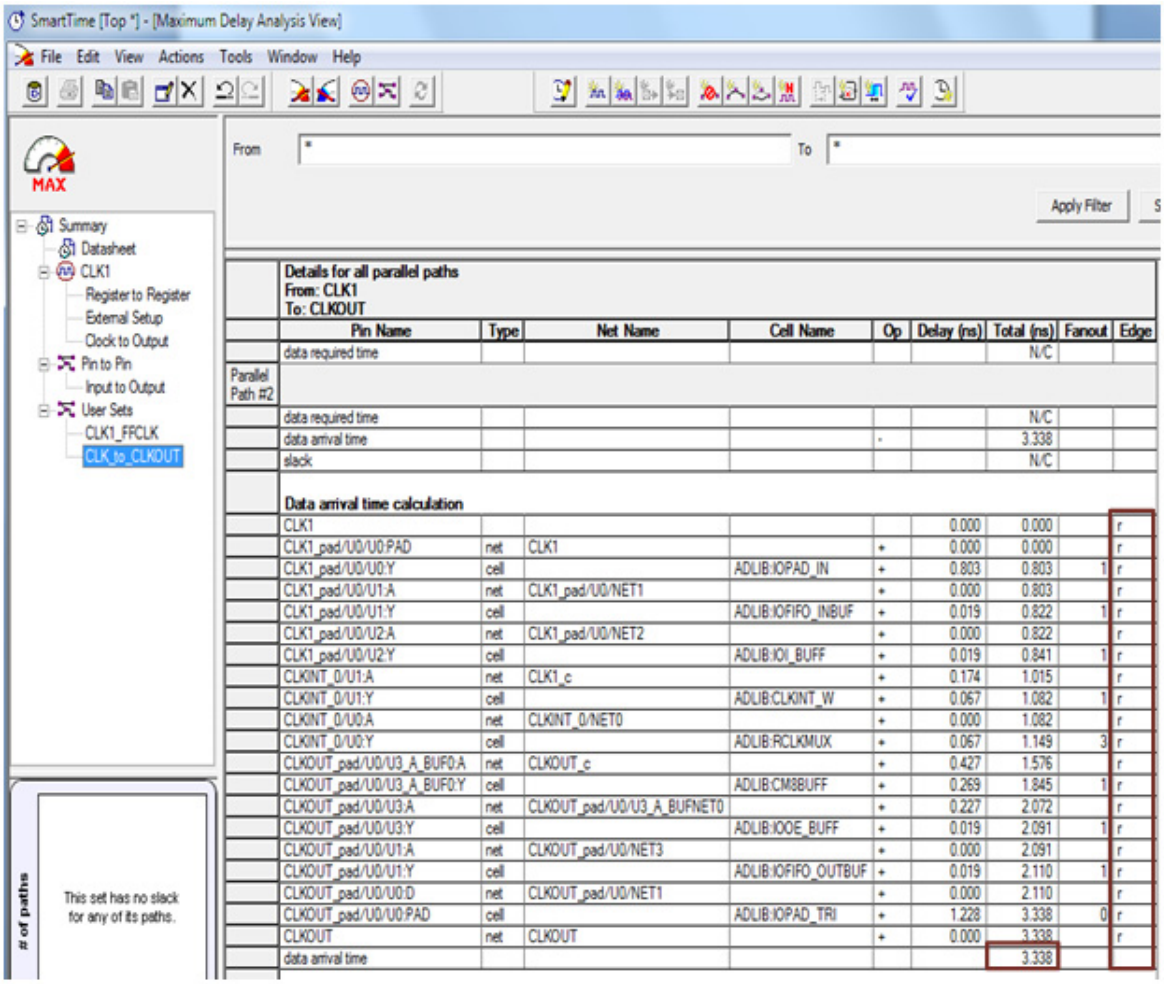



***Figure 17* • SmartTime Showing Clock-to-Output Delay for Minimum Delay Analysis**

3. Create a custom path set from the CLK port to the clock out pin, CLKOUT; name it the CLK_to_CLKOUT path set.
4. Open the **SmartTime Options** window and set **Perform maximum delay analysis based on** to **BEST** case conditions.

5. In the Maximum Delay Analysis view, get Tmax,best(clk) from the CLK_to_CLKOUT path set, as shown in the Figure 18. Ensure that you extract the same edge as the clock path in the external setup, standard calculation. If the correct edge is not there, change the options in SmartTime to show more than one parallel path.




**Details for all parallel paths**
**From: CLK1**
**To: CLKOUT**

| | Pin Name | Type | Net Name | Cell Name | Op | Delay (ns) | Total (ns) | Fanout | Edge |
|---|---|---|---|---|---|---|---|---|---|
| | data required time | | | | | | N/C | | |
| Parallel Path #2 | | | | | | | | | |
| | data required time | | | | | | N/C | | |
| | data arrival time | | | | - | | 3.338 | | |
| | slack | | | | | | N/C | | |
| | **Data arrival time calculation** | | | | | | | | |
| | CLK1 | | | | | 0.000 | 0.000 | | r |
| | CLK1_pad/U0/U0:PAD | net | CLK1 | | + | 0.000 | 0.000 | | r |
| | CLK1_pad/U0/U0:Y | cell | | ADLIB:IOPAD_IN | + | 0.803 | 0.803 | 1 | r |
| | CLK1_pad/U0/U1:A | net | CLK1_pad/U0/NET1 | | + | 0.000 | 0.803 | | r |
| | CLK1_pad/U0/U1:Y | cell | | ADLIB:IOFIFO_INBUF | + | 0.019 | 0.822 | 1 | r |
| | CLK1_pad/U0/U2:A | net | CLK1_pad/U0/NET2 | | + | 0.000 | 0.822 | | r |
| | CLK1_pad/U0/U2:Y | cell | | ADLIB:IOI_BUFF | + | 0.019 | 0.841 | 1 | r |
| | CLKINT_0/U1:A | net | CLK1_c | | + | 0.174 | 1.015 | | r |
| | CLKINT_0/U1:Y | cell | | ADLIB:CLKINT_W | + | 0.067 | 1.082 | 1 | r |
| | CLKINT_0/U0:A | net | CLKINT_0/NET0 | | + | 0.000 | 1.082 | | r |
| | CLKINT_0/U0:Y | cell | | ADLIB:RCLKMUX | + | 0.067 | 1.149 | 3 | r |
| | CLKOUT_pad/U0/U3_A_BUF0:A | net | CLKOUT_c | | + | 0.427 | 1.576 | | r |
| | CLKOUT_pad/U0/U3_A_BUF0:Y | cell | | ADLIB:CM8BUFF | + | 0.269 | 1.845 | 1 | r |
| | CLKOUT_pad/U0/U3:A | net | CLKOUT_pad/U0/U3_A_BUFNET0 | | + | 0.227 | 2.072 | | r |
| | CLKOUT_pad/U0/U3:Y | cell | | ADLIB:IOOE_BUFF | + | 0.019 | 2.091 | 1 | r |
| | CLKOUT_pad/U0/U1:A | net | CLKOUT_pad/U0/NET3 | | + | 0.000 | 2.091 | | r |
| | CLKOUT_pad/U0/U1:Y | cell | | ADLIB:IOFIFO_OUTBUF | + | 0.019 | 2.110 | 1 | r |
| | CLKOUT_pad/U0/U0:D | net | CLKOUT_pad/U0/NET1 | | + | 0.000 | 2.110 | | r |
| | CLKOUT_pad/U0/U0:PAD | cell | | ADLIB:IOPAD_TRI | + | 1.228 | 3.338 | 0 | r |
| | CLKOUT | net | CLKOUT | | + | 0.000 | 3.338 | | r |
| | data arrival time | | | | | | 3.338 | | |

***Figure 18* • SmartTime Showing CLK to CLKOUT Delay in Max Delay Analysis**

The minimum Clock-to-Output delay with respect to clock output is shown in EQ 14:

Best_clk_to_out wrt clkout = Tmin,best(datapath) – Tmax,best(clockpath) = 2.815– 3.338 = –0.523 ns

*EQ 14*

## CLK_OUT Calculation under Worst-Case Conditions

To calculate worst Clock-to-Output, use the Maximum Delay Analysis capability in SmartTime to calculate Tmax,worst(datapath) and use the Minimum Delay Analysis capability in SmartTime to calculate Tmin,worst(clk), and apply EQ 13. The flow and the numeric results for the example are shown below:

1. Ensure that the setting for Maximum Delay Analysis and Minimum Delay Analysis is set to **WORST**.
2. In the Maximum Delay Analysis view, examine the **Clock to Out** path set to get Tmax,worst(datapath), as shown in Figure 19.

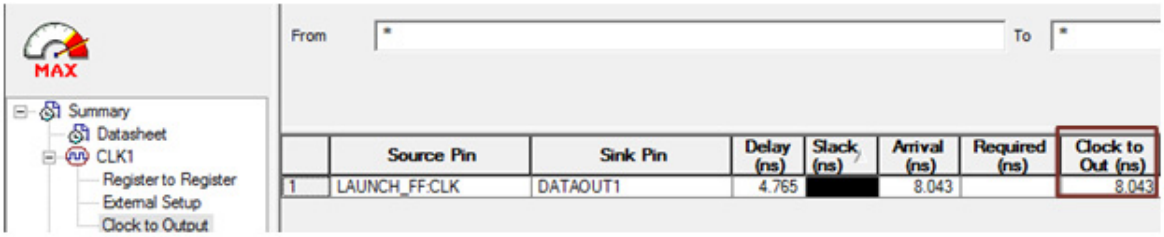



***Figure 19* • SmartTime Showing Clock-to-Output Delay for Maximum Delay Analysis**

3. In the Minimum Delay Analysis view, get Tmin,best(clk) from the CLK_to_CLKOUT path set (Figure 20). Ensure that you extract the same edge as the clock path in the external setup standard calculation. If the correct edge is not there, change the options in SmartTime to show more than one parallel path.

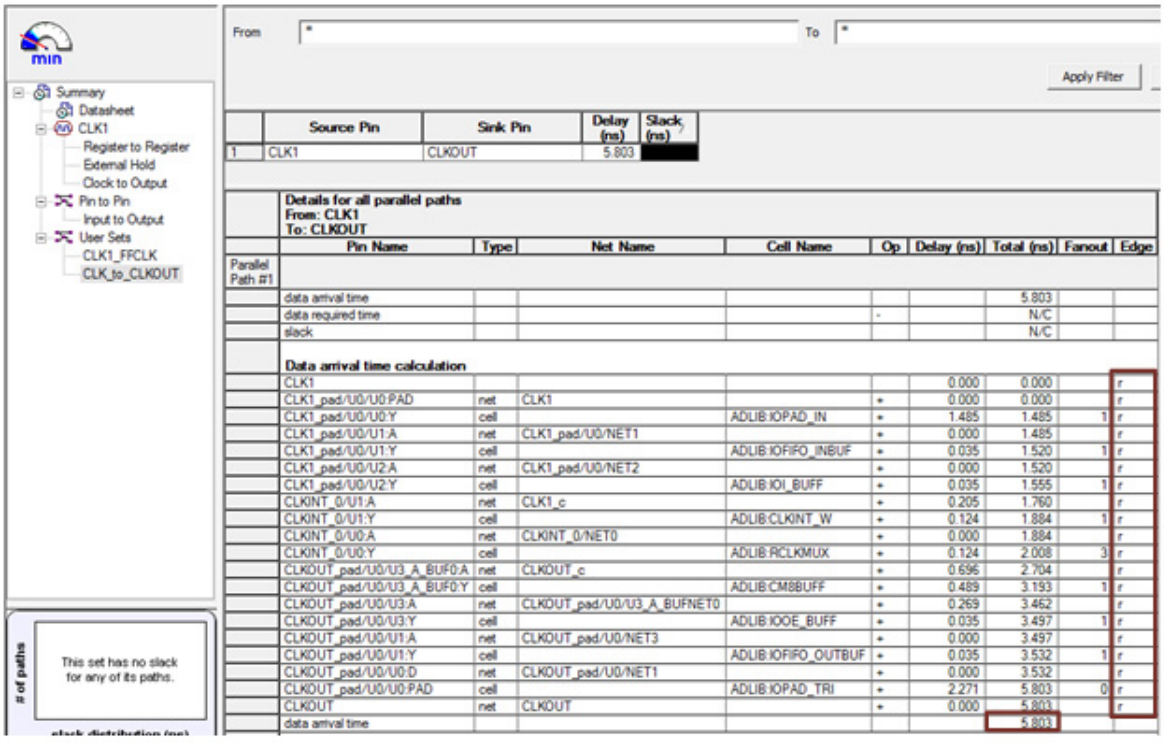



***Figure 20* • SmartTime Showing CLK to CLKOUT Delay in Minimum Delay Window**

The worst Clock-to-Output delay with respect to clock output is shown in EQ 15:

Worst_clk_to_out wrt clkout = Tmax,worst(datapath) – Tmin,worst(clockpth) = 8.043 – 5.803 = 2.24 ns

*EQ 15*

### Input-to-Output Path Timing Analysis

The design example used in the application note does not has any input-to-output path, so the calculation is not shown here in the application note.

## Conclusion

This application note describes the timing improvement in Libero IDE v9.2 and its impact on various types of RTAX-S/SL/DSP designs. You should only need to re-run timing analysis using Libero IDE v9.2 for complex clocking scheme designs. For new designs, Libero IDE v9.2 is recommended as it has improved timing data in maximum delay analysis, which will result in better performance than previous Libero versions.

This application note also shows detail steps for performing four corner analysis on various types of timing paths. It is recommended to run four-corner analysis on all RTAX-S/SL/DSP designs.

Finally, you should follow the design guidelines below for RTAX-S/SL/DSP FPGA:

- Use H-clocks to the maximum extent.
- Use R-clocks only when all H-clocks resources are used or when you need clock to drive combinatorial logic or I/Os.
- Avoid using combinatorial logic in clock network or minimize the regular routing in clock network. If clock network has combinatorial logic, you must use the maximum and minimum setup and hold analysis as shown in this application note.
- Constrain your design for a proper timing analysis.

# Appendix- A: TCL Script Example Showing Four Corner Analysis

```
file delete -force reports
file mkdir reports

st_set_options -max_opcond worst -min_opcond best
report -type “datasheet” -format “TEXT” {./reports/datasheet_b_w.txt}
report -type “timing_violations” -format “TEXT” -analysis “max” -use_slack_threshold \
“yes” -slack_threshold 0.00 - limit_max_paths “no” -max_paths 5 -max_expanded_paths 0
{./reports/timing_violations_max_b_w.txt}
report -type “timing_violations” -format “TEXT” -analysis “min” -use_slack_threshold \
“yes” - slack_threshld 0.00 -limit_max_paths "no" -max_paths 5 -max_expanded_paths 0
{./reports/timing_violations_min_b_w.txt}

st_set_options -max_opcond best -min_opcond worst
report -type “datasheet” -format “TEXT” {./reports/datasheet_w_b.txt}
report -type “timing_violations” -format “TEXT” -analysis “max” -use_slack_threshold \
“yes” -slack_threshold 0.00 - limit_max_paths “no” -max_paths 5 -max_expanded_paths 0
{./reports/timing_violations_max_w_b.txt}
report -type “timing_violations” -format “TEXT” -analysis “min” -use_slack_threshold \
“yes” -slack_threshold 0.00 - limit_max_paths “no” -max_paths 5 -max_expanded_paths 0
{./reports/timing_violations_min_w_b.txt}

st_set_options -max_opcond worst -min_opcond worst
report -type “datasheet” -format “TEXT” {./reports/datasheet_w_w.txt}
report -type “timing_violations” -format “TEXT” -analysis “max” -use_slack_threshold \
“yes” -slack_threshold 0.00 - limit_max_paths “no” -max_paths 5 -max_expanded_paths 0
{./reports/timing_violations_max_w_w.txt}
report -type “timing_violations” -format “TEXT” -analysis “min” -use_slack_threshold \
“yes” -slack_threshold 0.00 - limit_max_paths “no” -max_paths 5 -max_expanded_paths 0
{./reports/timing_violations_min_w_w.txt}

st_set_options -max_opcond best -min_opcond best
report -type “datasheet” -format “TEXT” {./reports/datasheet_b_b.txt}
report -type “timing_violations” -format “TEXT” -analysis “max” -use_slack_threshold \
“yes” -slack_threshold 0.00 - limit_max_paths “no” -max_paths 5 -max_expanded_paths 0
{./reports/timing_violations_max_b_b.txt}
report -type “timing_violations” -format “TEXT” -analysis “min” -use_slack_threshold \
“yes” -slack_threshold 0.00 - limit_max_paths “no” -max_paths 5 -max_expanded_paths 0
{./reports/timing_violations_min_b_b.txt}
```

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