Libero SoC v11.2 SP1 Release Notes

Libero SoC v11.2 SP1 is an incremental Service Pack that can be installed over Libero SoC v11.2.

Libero SoC v11.2 is a comprehensive software suite for designing with Microsemi's SmartFusion2 and SmartFusion SoC FPGAs, and IGLOO2, IGLOO, ProASIC3 and Fusion FPGA families.

Visit the Documents tab on your device page at www.microsemi.com to obtain silicon Datasheets, Silicon User's Guides, Tutorials and Application Notes.

Development Kits and Starter Kits are available from the Microsemi website.

Contents

Supported Families

IGLOO2, SmartFusion2, SmartFusion, Fusion, ProASIC3, ProASIC3E, ProASIC3L, IGLOO, IGLOOe, IGLOO+

SmartFusion2 Device Support

M2S150, M2S150T, M2S150TS, M2S150S	1152 FC
M2S100, M2S100T, M2S100TS, M2S100S	1152 FC
M2S090, M2S090T, M2S090TS, M2S090S	676 FBGA *(New),* 484 FBGA *(New)*
M2S050, M2S050T, M2S050TS, M2S050S	400 VF, 484 FBGA, 896 FBGA, 325 FCSBGA *(New)*
M2S025, M2S025T, M2S025TS, M2S025S	400 VF, 484 FBGA
M2S010, M2S010T, M2S010TS, M2S010S	400 VF, 484 FBGA
M2S005, M2S005S	400 VF, 484 FBGA

IGLOO2 Device Support

M2GL150, M2GL150T, M2GL150TS, M2GL150S	1152 FC
M2GL100, M2GL100T, M2GL100TS, M2GL100S	1152 FC
M2GL090, M2GL090T, M2GL090TS, M2GL090S	676 FBGA *(New),* 484 FBGA *(New)*
M2GL050, M2GL050T, M2GL050TS, M2GL050S	400 VF, 484 FBGA, 896 FBGA, 325 FCSBGA *(New)*
M2GL025, M2GL025T, M2GL025TS, M2GL025S	400 VF, 484 FBGA
M2GL010, M2GL010T, M2GL010TS, M2GL010S	400 VF, 484 FBGA
M2GL005, M2GL005S	400 VF, 484 FBGA

Programming Support for SmartFusion2 and IGLOO2

Programming file generation is enabled for these devices.

SmartFusion2

M2S050, M2S050S, M2S050T, M2S050TS
M2S025, M2S025S, M2S025T, M2S025TS
M2S010, M2S010S, M2S010T, M2S010TS
M2S005, M2S005S
M2S050T_ES

IGLOO2

M2GL050, M2GL050S, M2GL050T, M2GL050TS
M2GL025, M2GL025S, M2GL025T, M2GL025TS
M2GL010, M2GL010S, M2GL010T, M2GL010TS
M2GL005, M2GL005S

What's New Libero SoC v11.2 SP1

New Device Support

IGLOO2

484 FBGA for M2GL090, M2GL090T, M2GL090TS and M2GL090S
325 FCSBGA for M2GL050, M2GL050T, M2GL050TS and M2GL050S

Die	Package	Speed	Ranges	Gold License
M2GL050	325 FCSBGA	STD	COM, IND, Custom	Yes
M2GL050	325 FCSBGA	-1	COM, IND, Custom	Yes
M2GL050S	325 FCSBGA	-1	IND, Custom	No
M2GL050T	325 FCSBGA	STD	COM, IND, Custom	Yes
M2GL050T	325 FCSBGA	-1	COM, IND, Custom	Yes
M2GL050TS	325 FCSBGA	-1	IND, Custom	No
M2GL090	484 FBGA	STD	COM, IND, MIL, Custom	No
M2GL090	484 FBGA	-1	COM, IND, Custom	No
M2GL090S	484 FBGA	-1	IND, Custom	No
M2GL090T	484 FBGA	STD	COM, IND, Custom	No
M2GL090T	484 FBGA	-1	COM, IND, Custom	No
M2GL090TS	484 FBGA	-1	IND, Custom	No

SmartFusion2

484 FBGA for M2S090, M2S090T, M2S090TS and M2S090S
325 FCSBGA for M2S050, M2S050T, M2S050TS and M2S050S

Die	Package	Speed	Ranges	Gold License
M2S050	325 FCSBGA	STD	COM, IND, Custom	Yes
M2S050	325 FCSBGA	-1	COM, IND, Custom	Yes
M2S050S	325 FCSBGA	-1	IND, Custom	No
M2S050T	325 FCSBGA	STD	COM, IND, Custom	Yes
M2S050T	325 FCSBGA	-1	COM, IND, Custom	Yes
M2S050TS	325 FCSBGA	-1	IND, Custom	No
M2S090	484 FBGA	STD	COM, IND, MIL, Custom	No
M2S090	484 FBGA	-1	COM, IND, Custom	No
M2S090S	484 FBGA	-1	IND, Custom	No
M2S090T	484 FBGA	STD	COM, IND, Custom	No
M2S090T	484 FBGA	-1	COM, IND, Custom	No
M2S090TS	484 FBGA	-1	IND, Custom	No

Important Known and Fixed Issues

High Speed Serial Interfaces Configurator incorrect generation (SAR 52677, SAR 52967)

This known issue impacts both SmartFusion2 and IGLOO2 SERDESIF behavior.

For several protocol combinations the SERDESIF Configurator GUI incorrectly programs a particular register. This results in the link to not operate correctly at the physical level. This impacts both the actual device as well as the RTL simulation.

This issue will be found on any PCIe x1 development for the IGLOO2 Evaluation Kit.

It is possible for the user to modify the programming of the incorrect register and alleviate the problem. This can be accomplished by performing an "Edit Registers…". Select the "Edit Registers…" button in the SERDESIF Configurator GUI. Locate the SYSTEM_CONFIG_PHY_MODE_1 register. The table below provides the correct value for the invalid configurations. Modify the SYSTEM_CONFIG_PHY_MODE_1 register to the correct value and generate the component.

Protocol 1	Protocol 2	SYSTEM_CONFIG _PHY_MODE_0	SYSTEM_CONFIG _PHY_MODE_1	11.2 & 11.2 SP1
PCIe x1	None	0xFFF0	0xF1E	Invalid
PCIe x2	None	0xFF00	0xF3C	Invalid
PCIe x4	None	0x0000	0xFF0	Valid
EPCS x1 1.25G	None	0xFFF4	0xF0F	Invalid
EPCS x2 1.25G	None	0xFF44	0xF0F	Invalid
EPCS x4 1.25G	None	0x4444	0xF0F	Invalid
EPCS x1 2.5G	None	0xFFF3	0xF0F	Invalid
EPCS x2 2.5G	None	0xFF33	0xF0F	Invalid
EPCS x4 2.5G	None	0x3333	0xF0F	Invalid
SGMII x1	None	0x4FFF	0xF0F	Invalid
XAUI	None	0x1111	0xF0F	Invalid
PCIe x1	EPCS x1 1.25G	0x4FF0	0xF1E	Invalid
PCIe x2	EPCS x1 1.25G	0x4F00	0xF3C	Invalid
PCIe x1	EPCS x2 1.25G	0x44F0	0xF1E	Invalid
PCIe x2	EPCS x2 1.25G	0x4400	0xF3C	Invalid
PCIe x1	EPCS x1 2.5G	0x3FF0	0xF1E	Invalid
PCIe x2	EPCS x1 2.5G	0x33F0	0xF3C	Invalid
PCIe x1	EPCS x2 2.5G	0x33F0	0xF1E	Invalid
PCIe x2	EPCS x2 2.5G	0x3300	0xF3C	Invalid
PCIe x1	SGMII x1	0x4FF0	0xF1E	Invalid
PCIe x2	SGMII x1	0x4F00	0xF3C	Invalid
PCIe x1	PCIe x1	0xF0F0	0xF5A	Invalid
PCIe x2	PCIe x1	0xF000	0xF78	Invalid
PCIe x1	PCIe x2	0x00F0	0xFD2	Invalid
PCIe x2	PCIe x2	0x0000	0xFF0	Valid

This issue will be resolved in the 11.2 SP2 release of Libero SoC

325 FCSBGA Packages and SERDES lane limitations

In Libero SoC v11.2 SP1 the following protocols are supported:

- PCIe x1
- EPCS x1 and x2 (x2 is a special case where you MUST use the x4 mode to get to lane 0 and 2)

Only lanes 0 and 2 are bonded in this package. See the datasheet for a detailed package description.

There are no restrictions in the configurator today. There are no design rules in Compile to prevent unsupported configurations from passing.

MIL Temp Removed from 400 VF, 676 FBGA & 896 FBGA packages

Military Temperature for all SmartFusion2 and IGLOO2 packages was introduced in V11.2. Subsequently, we decided to offer MIL Temp only for 484 FBGA and 1152 FC packages.

If you started a design using Libero SoC v11.2 and selected MIL Temp for any 400 VF, 676 FBGA or 896 FBGA package, when you open the project in Libero SoC v11.2 SP1 the software will crash. Please contact soc_tech@microsemi.com for instructions on how to modify your project so that it can be opened in the current release.

SmartFusion2 & IGLOO2 SmartDesigns using the ULPI:USB_C option will revert to pre-generated state.

SAR 52873 – SmartDesign generates incorrect IOMUX configuration, which causes a silicon failure.

For designs created using Libero SoC v11.2 or earlier releases where the ULPI:USB_C option was selected in SmartDesign, the IOMUX configuration was not generated correctly and will not work in silicon. In Libero SoC v11.2 SP1 when you open this design the software will detect the problem and your design state will be shown to be pre-SmartDesign generation.

M2S150 and M2GL150 designs using unsupported attributes will revert to pre-Compile state.

SAR 53285 – M2S150 and M2GL150 designs created using Libero SoC v11.2 or earlier releases may not work on silicon.

In previous releases the software allows you to select attributes that are not supported for the 150 devices. When a 150 design is opened using Libero SoC v11.2 SP2 it will be invalided to a pre-Compile state.

Introduced in Libero SoC v11.2

Updating your design to Libero SoC v11.2

Regenerate programming files

SmartFusion2 designs created with pre-v11.2 software for the M2S025, M2S010 & M2S005 devices may need to be updated using Libero SoC v11.2.

In earlier releases, the RTC inside the MSS does not use the clock from the correct XTL.

Libero SoC v11.2 automatically detects if this scenario exists in your design and invalidates the programming file. You must regenerate the programming file.

IGLOO2 and SmartFusion2 System Builder Port/BIF Name Changes

The System Builder Interface has been optimized for clarity and simplicity. In Libero SoC v11.2 the names of some System Builder Pins, Pin Groups, and Bus Interfaces for System Builder Blocks have changed from previous releases. In addition to changing some port names, extraneous reset ports have been removed, and ports have been added to support new features.

If you are migrating a project created with a pre-11.2 release and your design contains a System Builder Block, read the relevant document below to understand the changes and updates required to continue with your System Builder design using Libero SoC v11.2.

- **IGLOO2 System Builder Port/BIF Name Changes**
- **SmartFusion2 System Builder Port/BIF Name Changes**

New Programming Support

Programming file generation is enabled for IGLOO2 M2GL005 and M2GL005S.

SmartFusion2 and IGLOO2 programming file generation on Linux is enabled.

New Device Support

IGLOO2 676 FBGA for M2GL090, M2GL090T, M2GL090TS and M2GL090S.

SmartFusion2 676 FBGA for M2S090, M2S090T, M2S090TS and M2S090S.

Industrial Temperature devices are now available in Standard speed grade.

Military Temperature devices are now available for SmartFusion2 and IGLOO2.

MIL devices will be offered for all 484 FBGA and 1152 FC packages.
Do not select MIL for other packages. This will be removed in the next release.

Software Enhancements

Compile time decreased up to 50% for the largest SmartFusion2 and IGLOO2 devices

Block Design Flow for SmartFusion2 and IGLOO2

Block Flow is a bottom-up design methodology that enables you to use design blocks (“Components” in generic terms) as building blocks for your top-level design. These building blocks may already have completed layout and been optimized for timing and power performance for a specific Microsemi device. Using these blocks as part of your top level design can reduce design time and improve timing and power performance.

- You can focus on the timing of critical blocks and ensure the timing across the blocks meets requirements before proceeding to integrate your blocks at the top level.
- Changes in other blocks have no impact on your own block; you can re-use your block without re-optimizing for timing closure.
- The block can be re-used in multiple designs.
- Shorter verification time; you must re-verify only the portion of the design that has changed.

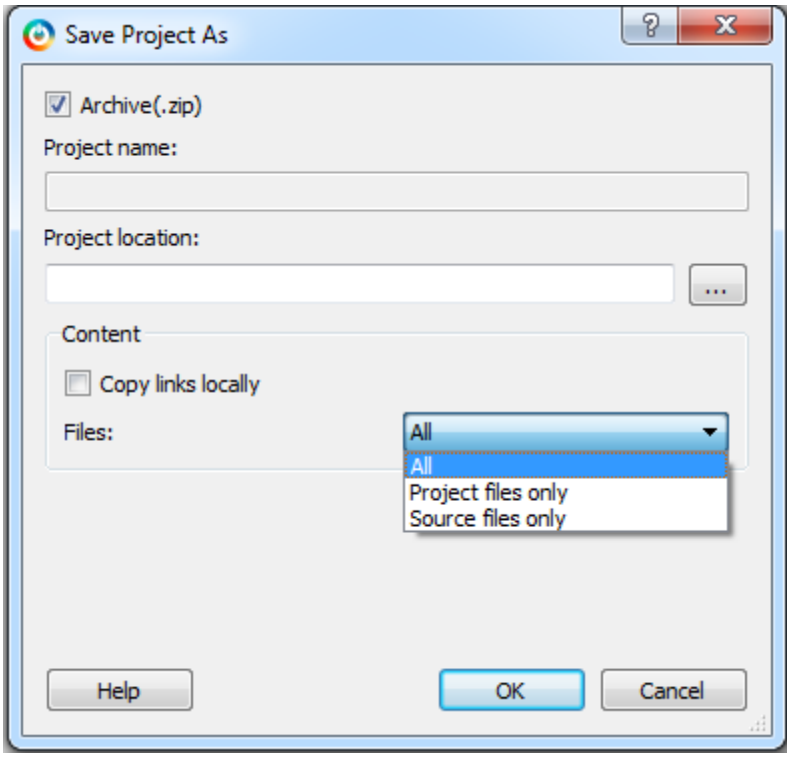
Enhanced Support for Version Control Tools

Libero now retains the directories that contain the source repository metadata information (such as *.svn, *.cvs) in the project so that they can be safely checked in and out of your configuration management system.

Libero Project Archiving

You can archive your Libero Project and select the type of files to be archived. The existing **Save Project As** functionality, which creates a copy of the opened project, is extended to include an Archive option in **Save Project As** dialog box.

Save Project As dialog box has a checkbox to Archive the Project.



Archive Checkbox functionality:

- Archive checkbox ON (checked):
  a) Project Name field is disabled; project is archived with the same name as the opened project at the specified location.
  b) Project is Archived and no copy is created.
- Archive checkbox OFF (unchecked):
  a) Save as functionality is identical to previous Libero SoC software.

SmartPower

SmartFusion2 and IGLOO2 Power Reports are now aligned with Datasheet nomenclature regarding the silicon status of Preliminary, Advance and Production.

Worst-case Analysis Support for Process Variations

Process variation is the naturally occurring variation in the attributes of transistors (length, widths, oxide thickness etc.) when integrated circuits are fabricated.

In previous releases SmartPower only supported voltage and temperature variations, now it also supports process variations. SmartPower now enables you to analyze power for worst-case process variations. Worse-case analysis is now supported for all – process, voltage and temperature [PVT].

Thermal Support

FPGA reliability, functionality and performance are influenced by operating junction temperature as it contributes to power to a large extent. To analyze the effect of junction temperature on device power, Microsemi SmartPower and Power Calculator now support pre-defined Heat Sink models, parameters for custom Heat Sink, Air Flow and Board Thermal models.

Updated Power Spreadsheet

SmartFusion2 and IGLOO2 Power Calculators have been updated with Thermal support and support for worse-case process variations.

SmartTime

Silicon-verified timing for M2S050/M2GL050 v1.2 COM & IND.

Updated M2S005/M2GL005 MSS timing data.

Design-specific IBIS models for SmartFusion2 and IGLOO2

M2S010 VF400
M2S050 VF400
M2S050T FG896

Synplify Pro ME - See Synplify Pro ME Release Notes for More Information

MACC DOTP support

Incremental Flow synthesis (Compile Points in Synplify Pro)

SmartDebug SERDES Analysis

A new view built into the SmartDebug application allows access to a SERDES specific interface when a SERDESIF block is found in the design. This interface provides the user with the following features.

- PMA Analysis
  - PRBS pattern generation and checking for near and far loopback
  - Loopback tests
- SERDES Lane status
- TCL script execution for SERDES memory map access

eNVM Serialization Support in Programming

- Program unique data into each device programmed (i.e. serial numbers, encryption keys).
- Serialization content can be configured by a file or by using auto increment.
  - Auto_increment (limited to 64-bit unsigned decimal)
  - Read_from_file
    - DEC (limited to 64-bit unsigned decimal)
    - HEX (no limit, can span multiple pages)

System Builder

FIC0 Fabric Master Subsystem is Now Editable in IGLOO2 System Builder

Fabric slaves of type AHBLite/APB3 can be added to this subsystem.

Dual Master Support for SmartFusion2 and IGLOO2

Dual master support added to the FIC0/1 Fabric master subsystems in both SmartFusion2 and IGLOO2 System Builder. Both the masters should be AHBLite. Multi-master support up to four masters is planned for a future release.

SPI_0 Support Added

The MSS/HPMS provides a SPI master/slave for interfacing to an external SPI flash memory or SPI device. Supported has been added to use this SPI port. In IGLOO2 the user is responsible for providing the fabric master via the FIC to utilize the SPI port.

PCIe Hot Reset and L2/P2 (Low Power States) Fixes for System Builder Designs for All Devices

These fixes are automatically enabled when SERDES is marked as used in the System Builder.

Low Power States

- L2 and P2 are low power states for the Link and PHY interface in a PCI Express (PCIe) system. A power management component in a PCIe system will control exit from the L2/P2 state. Part of the sequence when emerging from the low power state involves assertion and release of the PCI Express Reset (PERST#, or PERST_N in our implementation). In pre-v11.2 software, the PERST_N functionality is not implemented correctly in the SERDES block.

Hot Reset

- A hot reset is typically a software generated reset that is propagated downstream to all devices in the PCIe system. In pre-v11.2 software there is a problem in the handling of a hot reset in the SERDES block. The problem has been corrected to ensure that a hot reset of the SERDES interface occurs when necessary.

Resolved Issues

Issues Fixed in v11.2 SP1

SAR 52658 – Run Program action in the Libero will not program eNVM after adding a serialization client

SAR 51423 - Serialization file generation may take a long time

SAR 52873 – SmartDesign generates incorrect IOMUX configuration, which causes a silicon failure.

For designs created using Libero SoC v11.2 or earlier releases where the ULPI:USB_C option was selected in SmartDesign, the IOMUX configuration was not generated correctly and will not work in silicon. In Libero SoC v11.2 SP1 when you open this design the software will detect the problem and your design state will be shown to be pre-SmartDesign generation.

SAR 53285 – M2S150 and M2GL150 designs created using Libero SoC v11.2 or earlier releases may not work on silicon.

In previous releases the software allows you to select attributes that are not supported for the 150 devices. When a 150 design is opened using Libero SoC v11.2 SP2 it will be invalided to a pre-Compile state.

Issues Fixed in v11.2

SAR 51150 – For M2S025/010 designs the RTC does not use the clock from the correct xtal.

SAR 52131 - After changing the device in Libero, Generate Programming Data causes a crash.

SAR 41668 – SW Update Check window opens in full screen; cannot see buttons.

SAR 42954 - Not all remote cores are visible in the Catalog after switching to a new vault.

SAR 46334 – Ordering of PDC files may be incorrect after using ChipPlanner.

SAR 49693 - Changing the default I/O technology in Project Settings requires re-Compile.

SAR 50580 - SERDES configurator does not retain values for certain registers.

SAR 43095 - In the Domain Browser of the Analysis window, Edit Clock for a Generated Clock does not open the Edit Clock dialog box.

SAR 51055 – Programming with a programming file that does not contain the fabric erases the design name and checksum.

SAR 47535 – Multiple dialog windows should not open for Programmer Settings, Update eNVM Memory Content and Device I/O States.

Customer Reported SARs fixed in v11.2

Refer to your Technical Support Hotline Case Number to determine if it has been fixed in this release. The case number and SAR are listed below.

SAR	Case	Component	Summary
9264	1-32337637	SmartTime	DCF Warning Message is confusing
41824	493642-1025686476	Design Flow	Changing Preferred HDL option is not generating correct Designer block HDL file.
42626	493642-1076190772	Constraints Flow	Working design loses constraints on import and so fails to work.
43395	493642-1146559358	Design Hierarchy	Create Symbol option missing.
41668	493642-1260467609	Project Manager	SW Update check window appears at full screen size.
36596	493642-1260467609	Project Manager	When Vault Preference is set to Automatic Download, application startup is slow.
47886	493642-1327092690	HDL	Erroneous message for Check HDL.
48043	493642-1339354137	Precision RTL	Precision RTL cannot handle obfuscated Verilog files.
49829	493642-1353632775	VHDL Library	Incorrect RAM VHDL Simulation Model.
48673	493642-1355056818	SmartTime	TCL -select_clock_domains option ignored.
49151	493642-1363710309	Synthesis	SmartHeap Library Out of memory error.
49909	493642-1419960315 493642-1490639721	SmartDesign	Core with default name "newCore" prevents adding other cores.
51092	493642-1420984529	SynplifyPro	Expression does not match type std_ulogic.
50052	493642-1421750463	Power Calculator	Device Selection broken in Excel 2010 (Excel 2007 is OK).
50264	493642-1425756407	Power Calculator	Static power increases as devices get smaller in SmartFusion2.
50280	493642-1432645767	Project Manager	SmartFusion2 and IGLOO2 Programming file generation on Linux.
50363	493642-1434426673	Power Calculator	Unable to set frequency of an I/O.
50476	493642-1437772870	Power Calculator	SmartFusion2 shows different power only for "Rail Breakdown" when MDDR is used.
50713	493642-1440476962	SmartDesign	Incorrect message - No PLL ext f/b for A3P250/A3P1000 with X-60 marking.

50873	493642-1446945958	SynplifyPro	Crash observed.
	493642-1459050300		
51306	493642-1467150123	Power Calculator	Broken link to document.
52090	493642-1492201391	Designer	Warning message occurs after selecting A3PE3000L device in Designer.
52276	493642-1496804719	TCL	TCL script for importing ENVM content in SmartFusion2.
32535	493642-256481773 493642-844111140 493642-879619923 493642-572325673 493642-723105443 493642-945948352	Project Manager	Version Control support in Libero.
32670	493642-50566891	Compile	Fix the warning displayed in Designer software for EXTFB.
49481		System Builder	System Builder generates non-functional and wrong apb connection to FIC.
3411		Project Manager	Text Editor drag and drop capability is available.
39981		Project Manager	If Profile is set to use all-vendor Synplify Pro, batch invocation fails.
44718		Synplify Pro	RAM Inference for AGLN060V5 only works if no_rw_check attribute is applied.
48258		TCL	Add supported TCL commands to the Help Section.
49001		Project Manager	Core created from HDL loses track of original HDL if the HDL is linked.
51004		Timing	Crash when enabling/ disabling interclocks.
51174		Timing	SmartTime report incorrectly indicates clock inversion through RGB.
51909		Timing	Clock constraint shown is half of what user sets.

Known Limitations, Issues and Workarounds

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines the InstallShield Wizard displays a message stating

The installation of Microsoft Visual C++ 2005 SP1 Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Select **Yes** and the installation will complete successfully.

SmartFusion2 and IGLOO2

SAR 52554 – 325 FCSBGA Package and SERDES lane limitations

In Libero SoC v11.2 SP1 the following protocols are supported:

- PCIe x1
- EPCS x1 and x2 (x2 is a special case where you MUST use the x4 mode to get to lane 0 and 2)

Only lanes 0 and 2 are bonded in this package. See the datasheet for a detailed package description.

There are no restrictions in the configurator today. There are no design rules in Compile to prevent unsupported configurations from passing.

MIL Temp Removed from 400 VF, 676 FBGA & 896 FBGA packages

Military Temperature for all SmartFusion2 and IGLOO2 packages was introduced in V11.2. Subsequently, we decided to offer MIL Temp only for 484 FBGA and 1152 FC packages.

If you started a design using Libero SoC v11.2 and selected MIL Temp for any 400 VF, 676 FBGA or 896 FBGA package, when you open the project in Libero SoC v11.2 SP1 the software will crash. Please contact soc_tech@microsemi.com for instructions on how to modify your project so that it can be opened in the current release.

For IGLOO2 projects use System Builder for the following cores; do not use these cores from the Catalog directly.

- DDR Memory Controller
- CoreConfigP
- CoreResetP
- CoreConfigMaster

SAR 48448 - Zeroization will be available in a future release.

SAR 46571 - M2S050 has only one Oscillator

When you instantiate the Oscillator in your design and also use MSS RTC, the Clock Source of the RTC must match the clock source used in the Oscillator. For example, configuring the RTC with Clock Source set to 32 KHz RTC Crystal Oscillator while the Oscillator block is configured with the External Main Crystal Oscillator set to 5 MHz is invalid. The frequencies must match.

SAR 52174 – M2S090T/TS – The second PCIe core (PCIe_1) of the SERDESIF will not work in simulation.

SAR 51770 – MSS/HPMS VHDL Postsynthesis/Postlayout Simulation fails for existing projects

In SmartFusion2/IGLOO2 VHDL designs that were created with Libero SoC v11.1 SP3 and earlier, post-synthesis and post-layout simulations that use the MSS or HPMS will fail in Libero 11.2. Re-synthesize your design to work around this issue. This issue does NOT affect Verilog designs, nor does it affect new designs created using Libero SoC v11.2.

Libero

52718 - Core generated for VHDL project reports error during synthesis

The code generated by SmartDesign must be modified if you encounter this error. This will be fixed in a future release.

```
Error:

@E: CD393:"E:\Project\sd1.vhd":128:37:128:40|String doesn't match type integer
@E: CD351:"E:\Project\sd1.vhd":128:37:128:40|Can't implement expression type string
yet

In the example below, the error occurs because the generic values for
FIXED_SLAVE0_ADDR_VALUE and FIXED_SLAVE1_ADDR_VALUE are declared as strings:

component COREI2C
    generic(
        ADD_SLAVE1_ADDRESS_EN   : integer := 1 ;
        BAUD_RATE_FIXED         : integer := 0 ;
        BAUD_RATE_VALUE         : integer := 0 ;
        BCLK_ENABLED            : integer := 1 ;
        FIXED_SLAVE0_ADDR_EN    : integer := 1 ;
        FIXED_SLAVE0_ADDR_VALUE : integer := x"0" ;
        FIXED_SLAVE1_ADDR_EN    : integer := 1 ;
        FIXED_SLAVE1_ADDR_VALUE : integer := x"0" ;
        FREQUENCY               : integer := 30 ;
        GLITCHREG_NUM           : integer := 3 ;
        I2C_NUM                 : integer := 1 ;
        IPMI_EN                 : integer := 0 ;
        OPERATING_MODE          : integer := 0 ;
        SMB_EN                  : integer := 0
        );
```

Modify the generic values as shown below and re-run synthesis.

```
component COREI2C
    generic(
        ADD_SLAVE1_ADDRESS_EN   : integer := 1 ;
        BAUD_RATE_FIXED         : integer := 0 ;
        BAUD_RATE_VALUE         : integer := 0 ;
        BCLK_ENABLED            : integer := 1 ;
        FIXED_SLAVE0_ADDR_EN    : integer := 1 ;
        FIXED_SLAVE0_ADDR_VALUE : integer := 0 ;
        FIXED_SLAVE1_ADDR_EN    : integer := 1 ;
        FIXED_SLAVE1_ADDR_VALUE : integer := 0 ;
        FREQUENCY               : integer := 30 ;
        GLITCHREG_NUM           : integer := 3 ;
        I2C_NUM                 : integer := 1 ;
        IPMI_EN                 : integer := 0 ;
        OPERATING_MODE          : integer := 0 ;
        SMB_EN                  : integer := 0
        );
```

SAR 48929 - SmartDesign shows incorrect Memory Map for SmartFusion2 FIC_1

In designs with the default FIC Regions configuration for SmartFusion2, FIC_1 has the following Fabric Slave regions: 0x80000000-0x8fffffff, 0x90000000-0x9fffffff, 0xf0000000-0xffffffff. However, SmartDesign incorrectly shows FIC_1 slaves in the 0x70000000-0x7fffffff region. This is a display issue, and the generated netlist is correct.

SAR 47957 - SmartFusion2/IGLOO2 RAM Initialization Configurator – Importing Simple-Hex and Motorola-Hex files is not working

When you try to import Simple-Hex or Motorola-Hex files for initialization for simulation, Libero may crash or the import may fail (content initialized to all zeroes).

Workaround: There is a workaround available that utilizes a *.shx file generated for Fusion. Contact Microsemi Technical Support at soc_tech@microsemi.com for details. Ask for the workaround for SAR 47957.

SAR 50267 – Selecting SMEV RAM available in Fusion's Advanced Analog System Options dialog degrades the Resolution performance

In the datasheet we state a resolution of 1/0.25 Deg while using ADC in 10/12 bit mode. When using SMEV RAM we have observed a resolution of 3-4 Deg. in some cases.

SAR 51880 – Project Archiving tool states are not retained when a Libero Project is uploaded on SVN

Workaround: Zip the project and upload to SVN in order to retain the tool states.

SAR 41619 - IGLOO+ hot-swappable option is not displayed correctly in the GUI

Hot-swappable is always ON for IGLOO+ and cannot be changed. The GUI allows you to check/uncheck this feature, but it is ignored by the tools. These I/Os are always hot swappable.

SAR 43772 - Linux: The SmartFusion2 configurators for DDR and FICs are missing the diagram describing the details of the block

This issue will be fixed in a future release.

SAR 42170 - MVN Cross probing is not supported for Path List and Expanded Path View of the Min and Max Analysis windows

This issue will be fixed in a future release.

SAR 46161 - The post-synthesis EDN file will not appear in the design hierarchy until the project is closed and reopened.

SAR 49044 –Linux error when using MVN can be ignored

The following messages are displayed on the Linux terminal when the Floorplan Constraints Editor is opened.

```
Start Server 1
Start Server 2
Failed to open Def Table: 9
Failed to open Def Table: 8
Failed to open Def Table: 12
Running in orphan mode!
```

The following message appears on exiting MVN and a core file is created:

```
…/bin/mvn: line 69:  1675 Segmentation fault
(core dumped) "$exedir/../lib/$exename" "$@"
```

System Builder

SAR 49025 – System Builder shows incorrect Memory Map for IGLOO2

In the Memory Map page, the addresses for the HPMS FIC_0/1 slaves are shown as 0x80000000. It should read as (0x00000000-0x0fffffff + 0x20000000-0x2fffffff + 0x400000000-0x4fffffff + 0x60000000-0x6fffffff).

Shared Resources are not available outside System Builder

CCC

- Cannot modify System Builder CCC
  - No advanced options
  - Cannot use unused GL's that are not used in System Builder
- M2S005 – no other Fabric CCC available

Oscillators

- 25/50MHz oscillator is used in System Builder
- Oscillator output not available to user

Only two masters are allowed on current CoreAHBLite

Some applications may require up to 4 masters – CoreConfigP, CoreSysServices, CoreHPDMACtrl, User…

This is a limitation for small devices where FIC_1 is not available

System Services simulation is planned for a future release.

You must configure PDMA/HPDMA dynamically.

SmartTime

SAR 34365 - Asynchronous Register paths are not displayed in Timing Analysis view

This issue will be fixed in a future release.

SAR 43767 – Maximize Window button is missing from the title bar for Constraints Editor, Max Analysis and Min Analysis

Workaround: Double-click the title bar to maximize the window.

SAR 43726 - The exported Tcl file does not include commands to organize SDC files.

Workaround: Requires editing the exported TCL file carefully. This issue will be fixed in a future release.

Synplify Pro

SAR 52503 – Instrumented design fails in synthesis when new implementation option is used

The instrumented design fails in synthesis when the Identify implementation is not created at the same level as the synplify.prj file.

Workaround: Create Identify implementation at the same level as synplify.prj file and then instrument design and run synthesis.

SAR 52013 – The EDIF netlist is incorrect with designs that use TRIBUF, BIBUF and -disable_io_insertion

The generated EDN netlist is incorrect and Compile reports this error:

> ERROR: CMP041: Net <net_name> attached to the IO Pad is connected to input pins <pin_name>
> ERROR: The command 'compile' failed.

In the EDIF netlist there is a net driving a PAD and also 2 other regular pins. This is not legal. Modify your design to correct it.

SAR 51780: Attribute set on SYSRST macro does not get propagated when Compile Point is set

In Synplify Pro, if you set a Compile Point in RTL with a SYSRESET macro and run synthesis then INBUF is inferred on the DEVRST_N port of SYSREST. If INBUF is inferred on this port, which is supposed to be the PAD, Libero Compile reports this error:

ERROR: CMP032: Net DEVRST_N_c attached to the IO pad is not connected to a top level port.

Workaround: Remove this Compile Point.

SAR 51782: Synplify Pro crashes if the Compile Point is set to "soft" for a design using MSS.

Workaround: Remove this Compile Point.

SAR 42808 - Warning: Unrecognized option ignored: "-_include"

When Synplify Pro is invoked through Libero and the design has RTL with “-_include” <file_name>, the following option is added in the *.prj file:

```
add_file -_include <file_name>
```

Synplify Pro issues this message:

```
Warning: Unrecognized option ignored: "-_include"
```

This warning message can be ignored. The synthesis tool will locate the file in the Libero project /hdl folder.

SAR 46982 - Synplify Pro treats the PLL as a black box

SDC constraints applied to the PLL input do not propagate forward. To actively constrain it; you must constrain both the input and the output of the PLL using the create_clock and create_generated_clock constraints. More information can be found in KI70291.

SAR 46983 - False Path, Multicycle Path and Max delay constraints are not propagated to the SDC file used by Synplify Pro

For more information about constraints consult Chapter 4, Specifying Constraints, in the Synplify Pro User Guide.

Synplify Pro Warning: Unrecognized technology/part/package in Synplify Pro

When executing synthesis using the Libero integrated flow a warning appears if the silicon family, die or package is not present in Synplify Pro. In most cases the design will automatically be mapped to an existing device and continue. If no mapping exists the flow will halt.

Missing Die

```
Unrecognized part [die] specified for device [silicon_family] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Package

```
Unrecognized package [package_name] specified for part [die] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Silicon Family

```
Warning: Unrecognized technology: [silicon_family]
Unrecognized technology: [silicon_family] in [design_name]:synthesis
```

Synplify Pro halts.

Programming

SVF for SmartFusion2 and IGLOO2 will be available in a future release.

SAR 52006 - Unable to generate the STAPL file with eNVM client of size 3 bytes or less

Workaround: Increase the size of the client to 4 bytes or more.

SAR 51767 - Error: The command 'load_programming_data' failed.

During programming file generation if the serialization content files cannot be found, then you will see the following error : "Error: The command 'load_programming_data' failed.”

Workaround: Open **Update eNVM Memory Content** and specify a valid path for each serialization content file.

SAR 52264 - There is no error checking for hex values to ensure min is less than max

In the eNVM Memory Block dialog box when hex values are entered for min and max in auto increment data no error is reported if min is greater than max.

Error checking works correctly for decimal values.

SAR 45867 - STAPL player for SmartFusion2 or IGLOO2 will be available in a future release.

SAR 41069 - Add PDB loading from DDF for Libero environment

You may get an exit 6 idcode failure when chain programming within Libero using a PDB file.

Workaround: Use a STAPL file or use the standalone FlashPro tool for chain programming

SAR 47452 - FlashPro verify and erase errors are reported as programming failures.

If you run programming ACTION VERIFY/ERASE and there is a failure, then the error code will indicate it is a programming failure even though you were running action VERIFY/ERASE.

SmartDebug

SmartFusion2 devices will read invalid memory content if the MSS is held in the reset state or M3 is executing invalid microcode programmed into the Flash Memory.

Workaround: Program a valid design. Confirm that the MSS is not in the reset state.

SmartDebug SERDES will not work for M2S050PP and ES parts.

SmartDebug Tcl commands in the Libero flow will be supported in a future release.

System Requirements

Refer to System Requirements on the web for more information regarding operating systems support and minimum system requirements. 64-bit OS is required for designing SmartFusion2 and IGLOO2 150/100 devices.

Setup Instructions for Red Hat Enterprise Linux OS can be found on the Libero SoC Documents webpage.

Synopsys and Mentor Graphics Tools

These tools are included with the Libero SoC v11.2 installation.

Synplify Pro ME 2013.03M SP1-1 Release Notes

ModelSim ME 10.2c

Identify ME 2013.03M SP1 Release Notes (Windows only)

Synphony Model Compiler 2013.09M Release Notes (Windows only)

Prerequisite Software: In order to run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

Download Libero SoC v11.2 SP1

Installation requires Admin privileges

Windows or Linux

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