Power Matters

Programming Software Qualification for Space FPGAs

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Agenda

- RT Programming Qualifications
  - Reliability Test Designs
  - Reliability Experiments
  - S/W Versions Summary

RT Reliability Designs

- Multiple design types are used to address different reliability tests and coverage
  - QBI: Maximizes resource utilization
  - EAQ: Uses highly perceptive and stressful designs for antifuse evaluation
  - HSB: Targets special type of antifuses
  - Larger devices also incorporate TID and SEE blocks
    - RTAX4000S/RTAX4000D devices
  - Different I/O standards are utilized in each design
    - Single ended, differential, and voltage referenced I/O's are configured
  - Design utilizations for each type of design shown in the following slide

Device Utilization

- Microsemi SoC requirement to have a minimum of 95% utilization for each reliability design

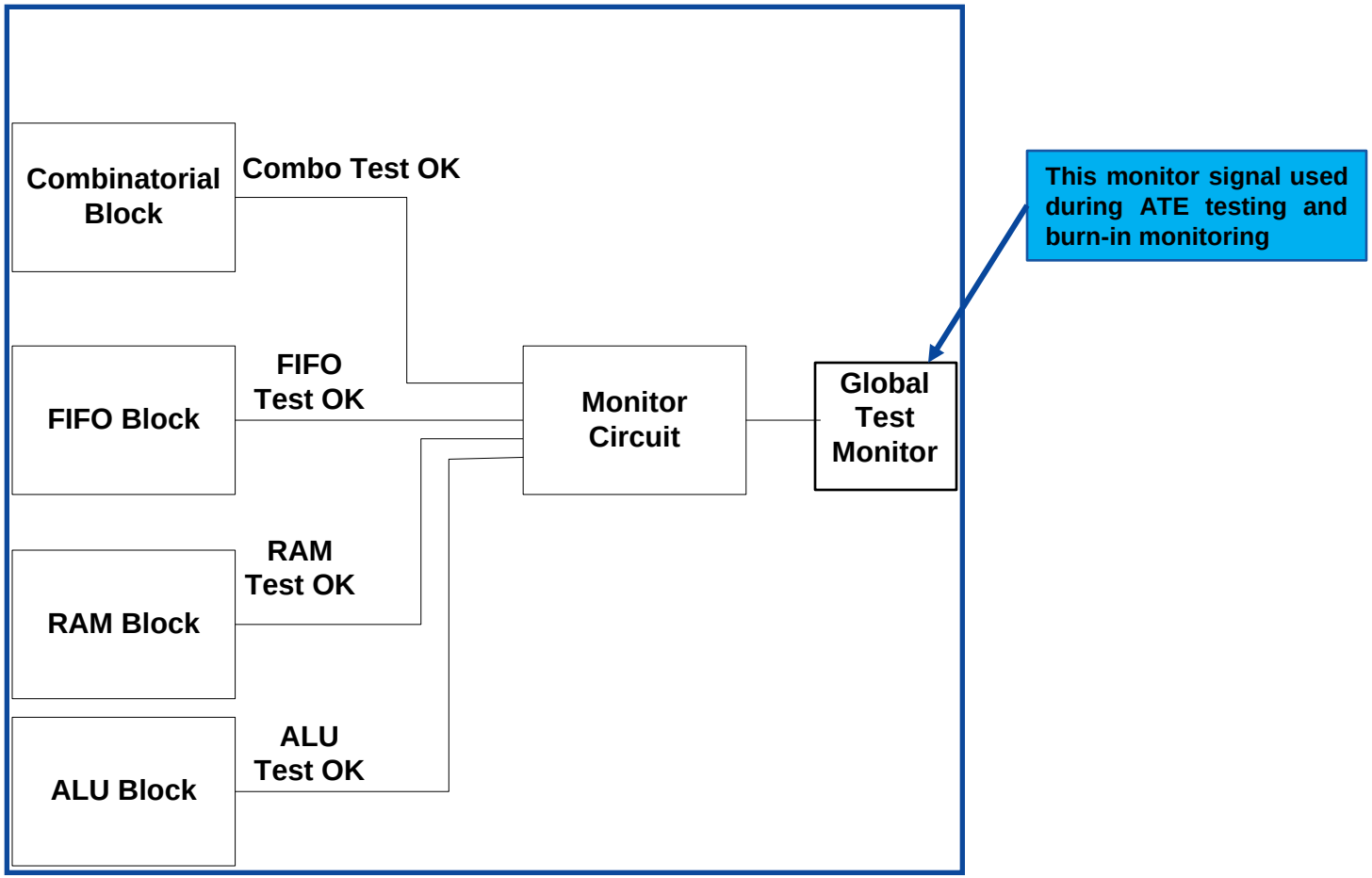
Info			Utilization								
			Pins	Clocks				Cells		Summary	
Design Type	Device	Package	I/O	RCLK	HCLK	RAM/FIFO	Carry Chain	R-Cell	C-Cell	seq + combo	Total Modules
QBI + EAQ + HSB + TID	RTAX4000S	CG1272	840	4	4	120	387	20,155	40,298	99.96%	60453
QBI	RTAX2000S	CQ352	196	4	4	64	32	9,965	21,437	97.35%	31402
EAQ	RTAX2000S	CQ352	198	4	4	64	33	10,666	21,122	98.55%	31788
QBI	RTAX2000S	CG624	196	4	4	64	32	9,965	21,385	97.19%	31350
EAQ	RTAX2000S	CG624	418	4	4	64	33	10,652	21,482	99.62%	32134
EAQ	RTAX2000S	CG1152	684	2	4	64	33	10,632	21,494	99.60%	32126
QBI	RTAX1000S	CQ352	196	4	4	36	17	5,768	12,091	98.43%	17859
EAQ	RTAX1000S	CQ352	198	4	4	36	19	6,027	12,070	99.74%	18097
EAQ	RTAX1000S	CG624	418	4	4	36	19	6,010	12,029	99.42%	18039
EAQ	RTAX250S	CQ352	198	2	3	12	13	1,388	2,798	99.10%	4186
EAQ	RTAX250S	CQ208	115	4	3	12	13	1,397	2,815	99.72%	4212

QBI Design

- Design Overview
  - QBI (Qualification Burn In) design
  - Goal of this design
    - Maximum utilization of logic cells (with different configurations)
    - Test all IO standards
    - Testing of all macros offered (like Carry chain, buffys etc)
    - Test RAM feature (in RTAX-S)
    - Test DSP feature (in RTAX-D)
  - QBI block also used as Quality Control Monitor (QCMON) design in smaller devices

QBI Design Features

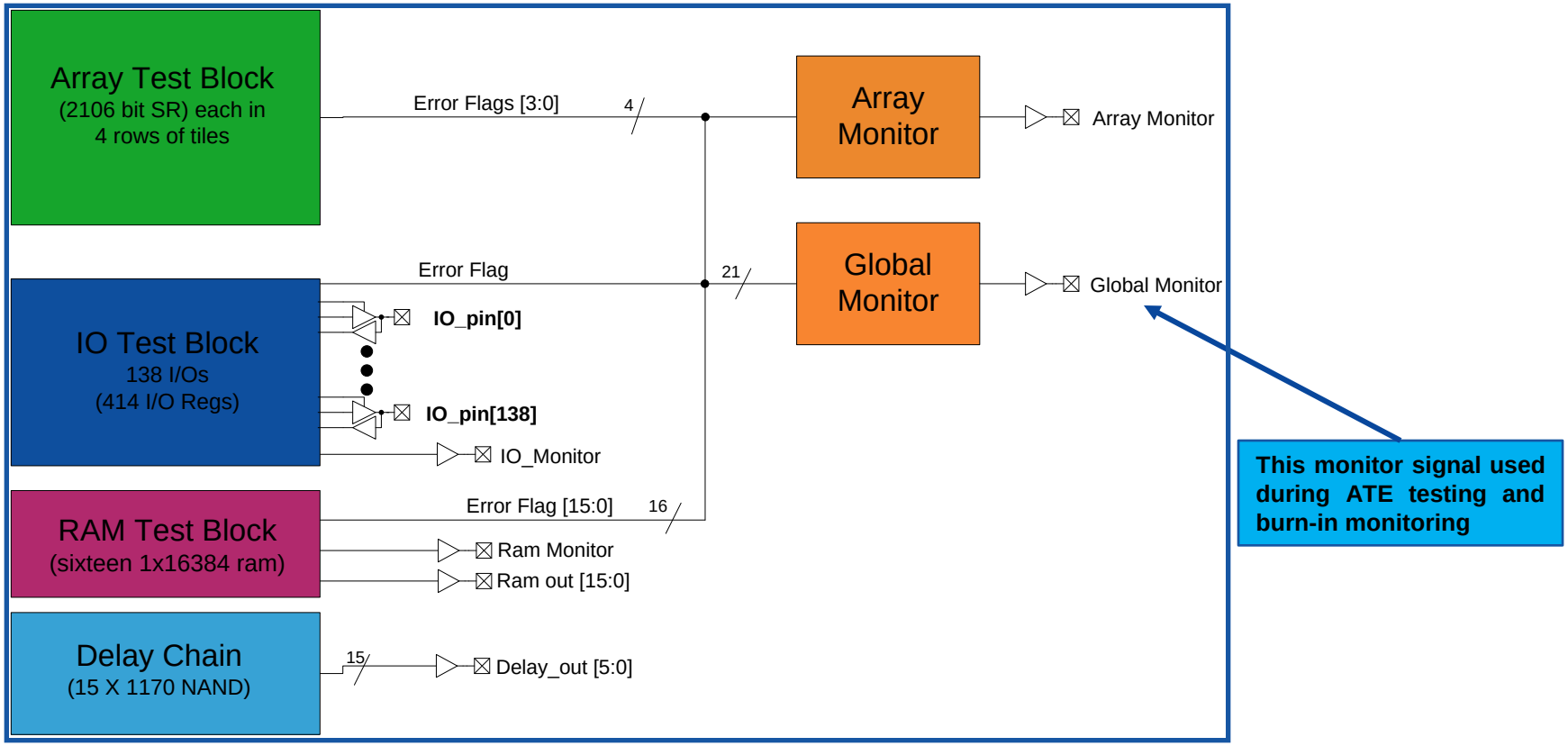
- Top level design includes different blocks to ensure testing of all device features with maximum utilization



EAQ Design Overview

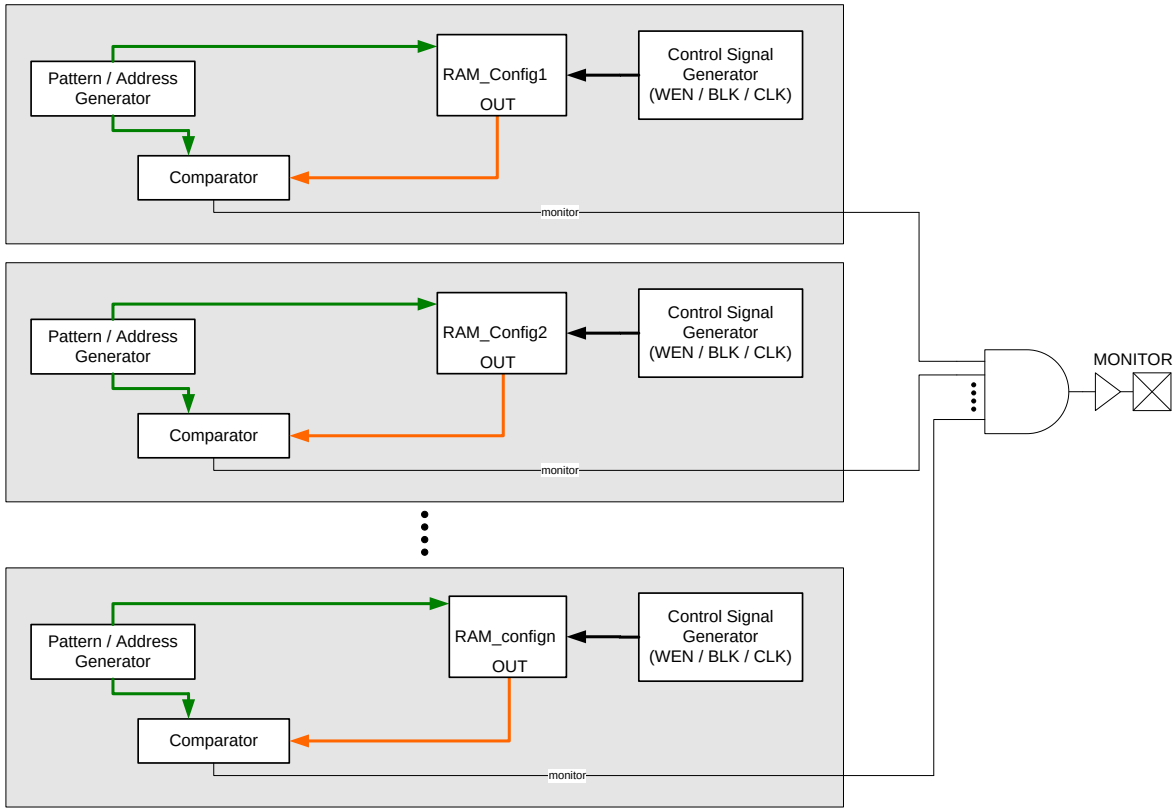
- Goal of Enhanced Antifuse Qualification (EAQ) design
  - Design used for study of antifuse reliability experiment
  - Design fully utilized smaller devices
    - RTAX2000S, RTAX1000S, RTAX250S, RTSX-SU
  - Design has high perceptibility of delay measurement deltas
    - Multiple delay lines of combinatorial modules
    - I/O test block
    - RAM test blocks
  - This design is used for Enhanced Lot Acceptance (ELA) testing
    - Sample of programmed device burn-in from every wafer lot

Top Level EAQ Diagram



SRAM Block Overview

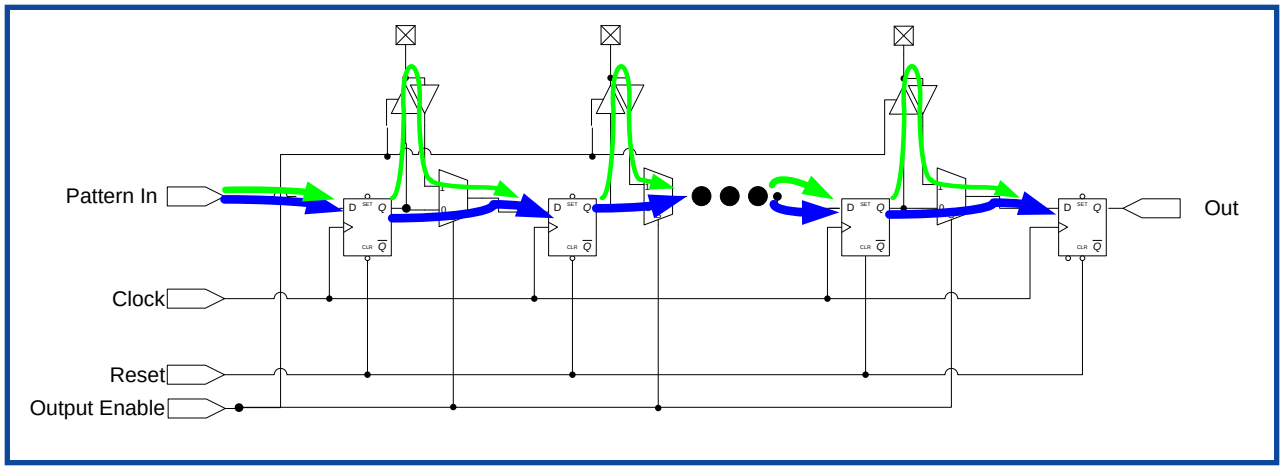
- Embedded SRAM Blocks
  - Full test coverage on all SRAM cells
  - Varying depth and width configurations



I/O Test Block

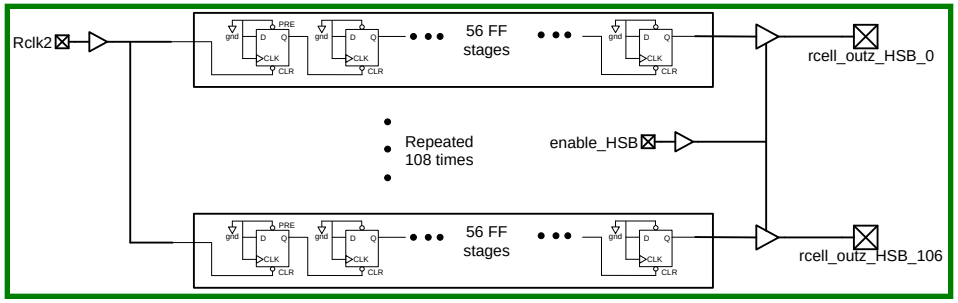
- Scalable block for maximizing I/O utilization
  - Utilizes all possible I/O configurations
  - Controlled simultaneous switching outputs

- Exercises both input and output buffer of each I/O

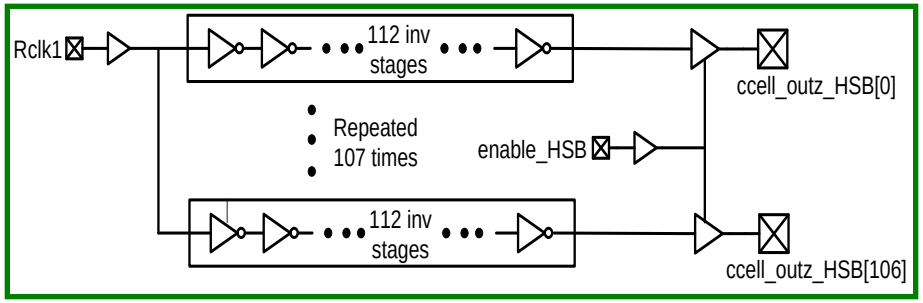


HSB Design Overview

- Goal of High Single-S and Single-B antifuse design
  - Increase the utilization of Single-S and Single-B antifuse
  - Short delay lines of combinatorial and sequential logic
  - Multiple delay lines per device compared against each other at every burn-in pull point
    - Delay lines shown below (All delay lines exercised during burn-in)



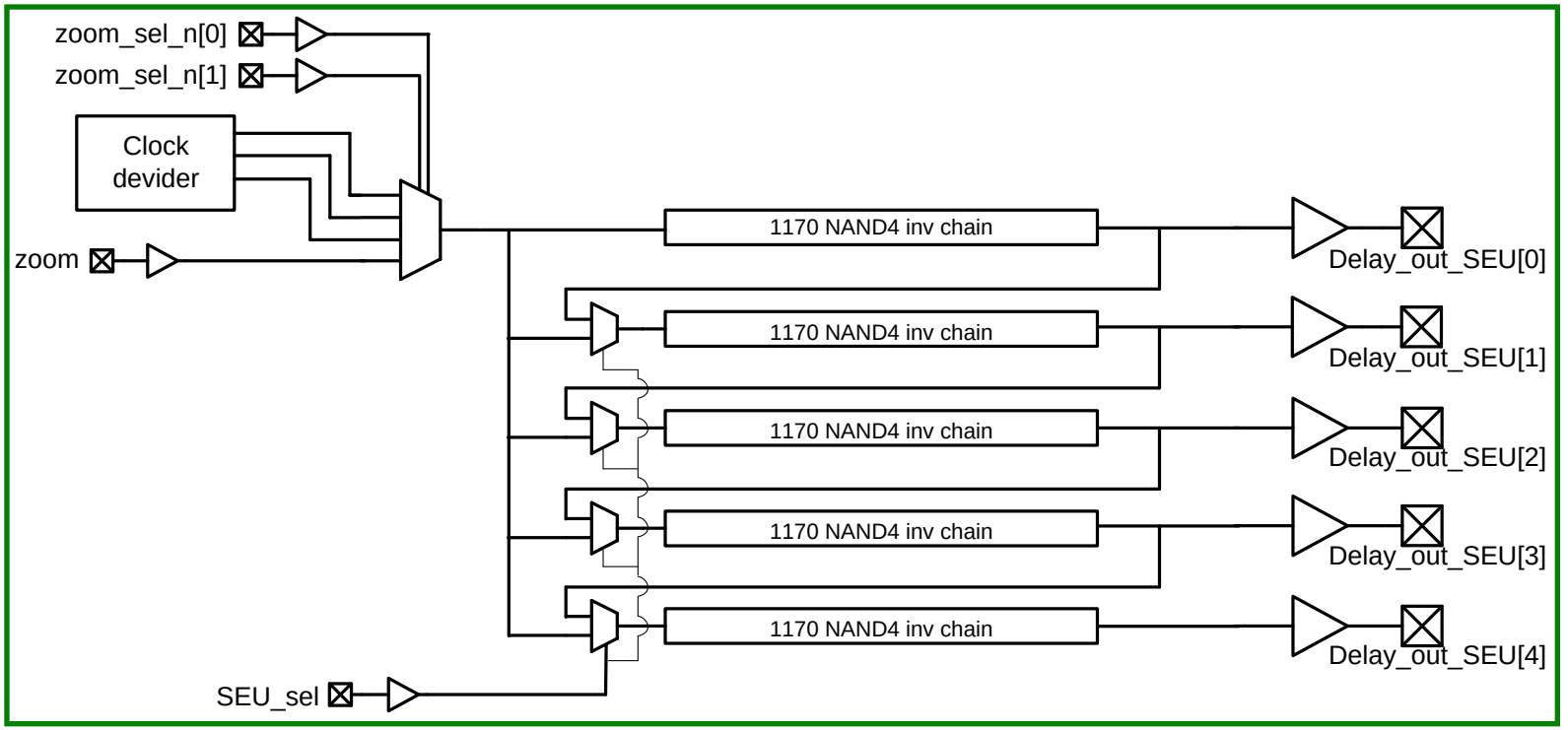
Sequential delay lines



Combinatorial delay lines

SEU Combinatorial Delay Block

- SEU delay lines have longer delays compared to EAQ and HSB delay lines
  - The delay line could be exercised through an input pin or a clock divider block
  - Each delay line can be cascaded to make up one long delay line



Reliability Experiments

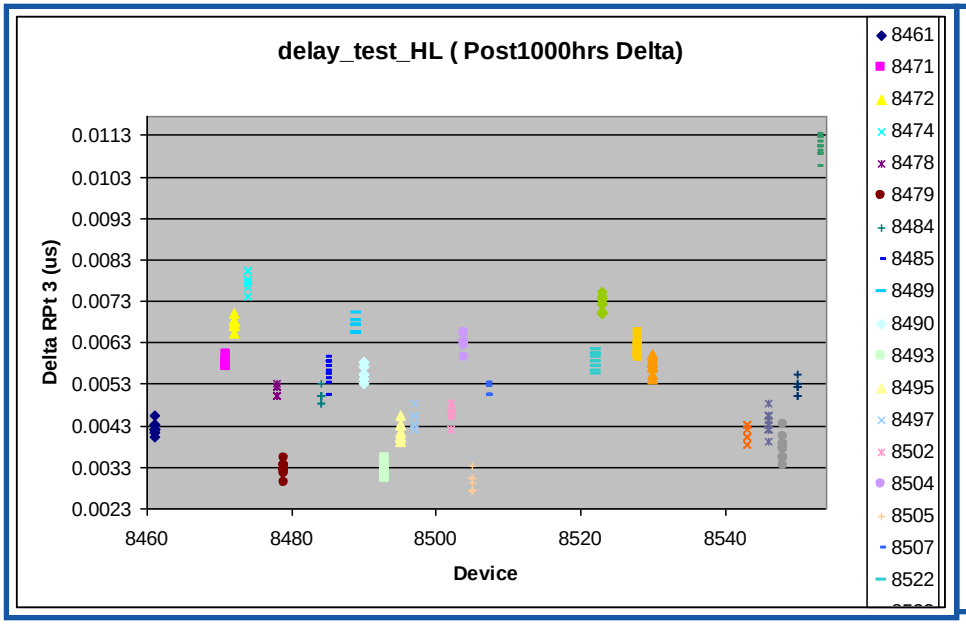
- Different types of experiments performed on Microsemi SoC RT products
  - ELA
    - Performed on every RTAX-S/RTSX-SU wafer lot
    - Burn-in duration of 168hrs HTOL
  - Grp C lifetest
    - Periodic lifetest performed on yearly basis per process technology
    - Burn-in duration of 1000hrs HTOL
  - Class-V Grp C
    - Performed on every Class-V wafer lot
    - Burn-in duration of 2000hrs HTOL

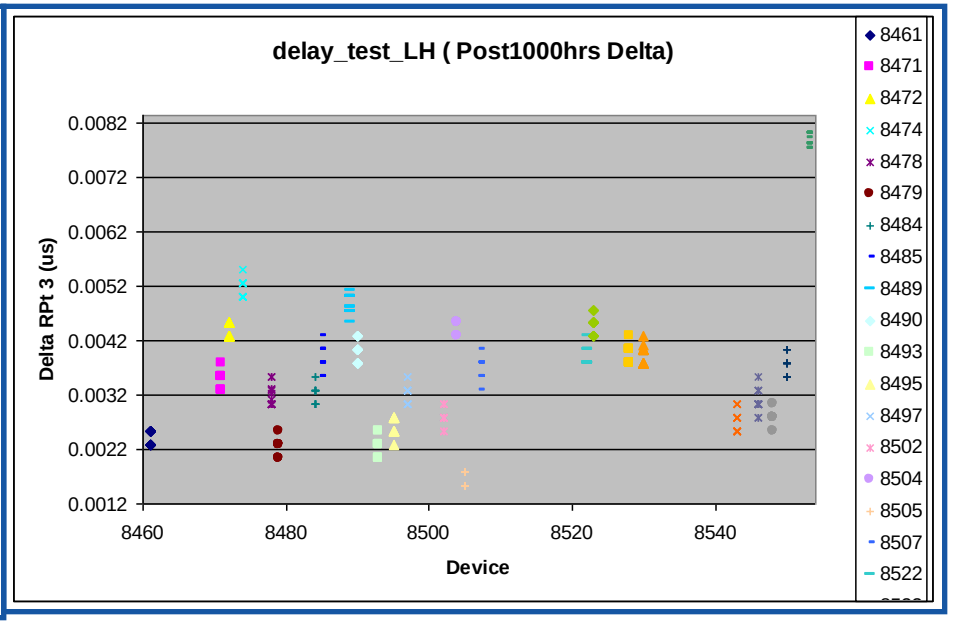
Reliability Experiments

- Customer Lifetest
  - Burn-in duration per request by customer
    - Normally 1000hrs or 2000hrs HTOL
- QBI/EAQ
  - For qualification of new product or process change
  - Burn-in duration of
    - 1000hrs HTOL for QML-Q products
    - 4000hrs HTOL for QML-V products (SoC completed 6000hrs HTOL)
- All above experiments performed on programmed devices
- Latest Sculptor S/W version utilized to program devices at the time of the reliability experiment
  - All burn-ins performed at maximum supply and temperature conditions

Data Analysis Methodology

- All reliability testing is completed on devices that have completed the normal production flow
  - Blank device processing to get to finished goods
- All functional and parametric testing is performed after programming of each device
- Time zero testing and post burn-in testing performed at every pull-point
  - Delta analysis is completed on all parameters





Overall Accumulation of Life Test Data

- Only tracking lifetest data since Sculptor V4.68
  - V4.68 released late 2007
  - Microsemi recommends using the most recent software version

12 Most Recent Releases		Top 12 by Device-Hours	
Silicon Sculptor S/W Version	Device-Hours	Silicon Sculptor S/W Version	Device-Hours
V5.22.4	33,768	V4.68.1	561,704
V5.22.3	115,664	V5.6.0	411,056
V5.22.2	196,624	V5.22.0	351,312
V5.22.1	21,056	V5.2.0	247,336
V5.22.0	351,312	V5.22.2	196,624
V5.18.1	2,856	V5.14.1	180,080
V5.18.0	96,464	V4.80.0	160,368
V5.14.1	180,080	V5.22.3	115,664
V5.12.1	85,536	V5.8.1	109,520
V5.12.0	22,384	V5.18.0	96,464
V5.10.1	14,000	V5.12.1	85,536
V5.8.1	109,520	V4.78.0	80,000

RT Qualification S/W Versions

- Top 12 Silicon Sculptor versions vs. type of reliability experiment

	Type of Reliability Test					
Silicon Sculptor S/W Version	Lifetest	ELA	EV Grp C	Grp C	QML-V Grp C & Qual	Grand Total
V4.68.1	29,000	4,704			528,000	561,704
V5.6.0	14,000	7,056	48,000		342,000	411,056
V5.22.0	96,000	39,312		80,000	136,000	351,312
V5.2.0	29,000	42,336	48,000	80,000	48,000	247,336
V5.22.2	40,000	36,624			120,000	196,624
V5.14.1	24,000	10,080			146,000	180,080
V4.80.0	64,000	46,366			50,000	160,366
V5.22.3	8,000	41,664			66,000	115,664
V5.8.1	7,000	23,520		79,000		109,520
V5.18.0		30,464		66,000		96,464
V5.12.1	16,000	25,536			44,000	85,536
V4.78.0				80,000		80,000

Prog Software Life Test by Product – RTSX-SU

Device	Device-Hours
RTSX32SU	**114,400**
V5.2.0	16,800
V5.22.2	8,000
V5.22.3	8,000
V5.22.4	16,800
V5.6.0	48,000
V5.8.1	16,800
Grand Total	**114,400**

Device	Device-Hours
RTSX72SU	**262,992**
V4.78.1	16,800
V4.80.0	33,600
V5.18.1	2,856
V5.2.0	64,800
V5.22.0	64,800
V5.22.2	16,800
V5.22.3	29,736
V5.22.4	16,800
V5.4.1	16,800
Grand Total	**262,992**

Prog Software Life Test by Product – RTAX-S

Device	Device-Hours
RTAX250S	**213,400**
V3.89	24,800
V3.93	6,000
V4.64.0	16,800
V4.70.1	5,000
V4.80	8,000
V4.80.0	24,000
V5.12.0	8,000
V5.12.1	16,800
V5.2.0	48,000
V5.22.1	8,000
V5.6.0	48,000
Grand Total	**213,400**

Device	Device-Hours
RTAX1000S	**203,736**
V4.70.1	10,000
V4.80.0	74,064
V5.12.0	4,032
V5.12.1	4,032
V5.14.1	12,032
V5.18.0	4,032
V5.2.0	4,032
V5.22.2	66,032
V5.22.3	8,064
V5.4.1	6,048
V5.8.1	11,368
Grand Total	**203,736**

Device	Device-Hours
RTAX2000S	**1,134,920**
V4.68.1	33,704
V4.70.0	2,352
V4.70.1	57,856
V4.74.0	2,352
V4.78.0	80,000
V4.78.1	8,000
V4.80	2,352
V4.80.0	18,352
V5.10.1	14,000
V5.12	8,000
V5.12.0	2,352
V5.12.1	64,704
V5.14.1	114,352
V5.18.0	89,408
V5.2.0	113,704
V5.22.0	282,816
V5.22.1	7,056
V5.22.2	86,112
V5.22.3	48,520
V5.22.4	168
V5.220	2,352
V5.6	10,352
V5.6.0	4,704
V5.8.1	81,352
Grand Total	**1,134,920**

Device	Device-Hours
RTAX4000S	**664,416**
V4.68.1	528,000
V4.70.1	2,520
V4.74	1,344
V4.76.0	2,520
V5.14.1	51,344
V5.18.0	1,344
V5.22.1	6,000
V5.22.2	1,344
V5.22.3	20,000
V5.4.1	44,000
V5.6.0	6,000
Grand Total	**664,416**

Conclusion

- Programming of devices done with highly utilized and perceptive designs
- Reliability testing completed on each wafer lot
- Programming S/W versions tracked by lifetest
- Microsemi recommends using the latest S/W version
- Programming S/W version to be available online
  - Under Microsimi SoC Reliability Report

http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data

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Thank You