Power Matters

Microsemi

FPGA Products Update

Microsemi Space Forum Russia – November 2013

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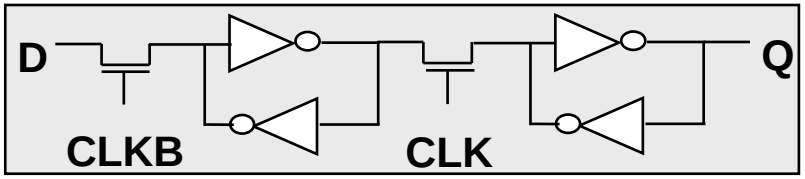
Marketing Manager, Space and Aviation, SoC Products Group

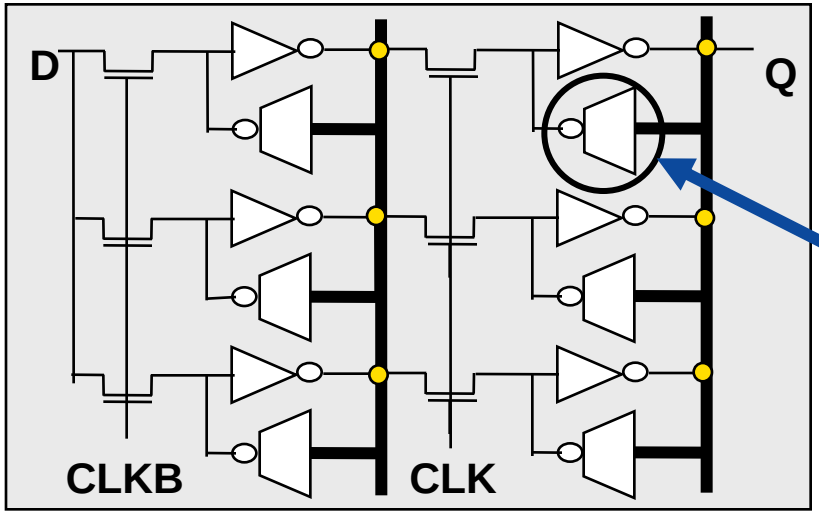
RHBD SEU-Enhanced Flip-Flops

- RTSX-SU, RTAX-S/SL, RTAX-DSP and RTG4 FPGAs

Standard Flip-flop



SEU-Enhanced Flip-flop



Microsemi Advantage

- 100% gate availability - no gate loss to TMR implementation
- Upsets due to single ion strike voted out by the unaffected latches
- Voting the feedback paths prevents the flip flop from changing state
- Transparent to user, no special skill or knowledge needed

Voter Gate

- Two correct inputs outvote single incorrect input
- Self-corrects asynchronously

Screening Flows for Space-Flight FPGAs

Screening Process		
Mil-Std 883 Class B	**Extended Flow**	**QML-V / EV Flow**
Wafer Sort	Wafer Sort	Wafer Sort
Package Assembly (B flow)	Package Assembly (E flow)	Package Assembly (V/EV flow)
Bond Pull (Extended Pull Test)	Bond Pull (Extended Pull Test)	Bond Pull (Extended Pull Test)
Internal Visual (Cond. B)	Internal Visual (Cond. A)	Internal Visual (Cond. A)
	Pre-Cap Source Inpsection (Cond. A)	Pre-Cap Source Inpsection (Cond. A)
Serialization	Serialization	Serialization
Temperature Cycling (10 Cycles)	Temperature Cycling (10 Cycles)	Temperature Cycling (50 Cycles)
Constant Acceleration	Constant Acceleration	Constant Acceleration
PIND	PIND	PIND
Seal (Fine/Gross Leak Test)	Seal (Fine/Gross Leak Test)	Seal (Fine/Gross Leak Test)
	X-Ray	X-Ray
Binning Circuit	Binning Circuit	Binning Circuit
Comm Temp Test	Comm Temp Test	Comp Temp Test
	Pre Read and Record +25C (R&R)	Pre Read and Record +25C (R&R)
Dynamic Burn-in (160 Hrs @125C)	Dynamic Burn-in (240 Hrs @125C)	Dynamic Burn-in (240 Hrs @125C)
Post-BI-Test +25C	Post-BI-Test +25C with R&R	Post-BI-Test +25C with R&R
	Static Burn-in (144 Hrs @125C)	Static Burn-in (144 Hrs @125C)
	Post-BI Test +25C with R&R	Post-BI Test +25C with R&R
Final Test -55C	Final Test -55C	Final Test -55C with R&R
Final Test +125C	Final Test +125C	Final Test +125C with R&R
	Seal (Fine/Gross Leak Test)	Seal (Fine/Gross Leak Test)
	Speed Grade Test (RTAX only)	Speed Grade Test (RTAX only)
100% QA Electrical +25C	100% QA Electrical +25C	100% QA Electrical +25C
Visual Inspection	Visual Inspection	Visual Inspection
Lot Acceptance Tests		
Generic Group B	Lot Specific Group B with RGA	Lot Specific Group B with RGA
Generic Group C	Generic Group C	Wafer Lot Specific Group C (2000 Hrs HTOL)
Generic Group D	Generic Group D	Generic Group D
Generic Radiation Total Dose Report	Generic Radiation Total Dose Report	Generic Radiation Total Dose Report
		Lot Specific DPA (per Date Code)

Agenda

- RTSX-SU
- RTAX-S
  - RTAX-S Reliability and Flight Heritage Update
- RTAX-DSP
- RT ProASIC 3
- IP for Space Applications
- Conclusion

Microsemi

RTSX-SU

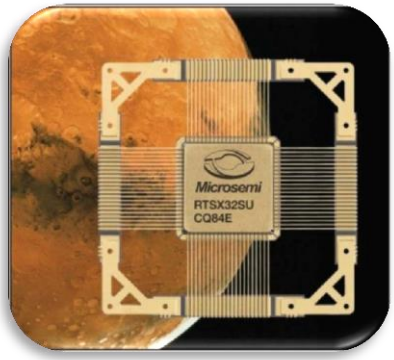
RTSX-SU Family

- RTSX-SU Features
  - Designed specifically for Space Applications
  - Up to 2,012 SEU Hardened Flip-Flops eliminate user-designed TMR
  - Single Event Latch-up Immune
  - Supports Hot-Swapping and Cold Sparing
  - Configurable I/O support multiple 5.0V and 3.3V I/O standards
  - Pin Compatible with commercial SX-A devices for easy prototyping
  - Antifuse secure programmable technology
- QML Certified Devices
  - QML Class Q available today
    - Mil Std 883 Class B
    - Microsemi Extended flow
  - "EV" flow available today
    - All process steps of QML-V
    - 300°C bake with sample destructive pull at wire-bond set-up (bimetalic wire bonding)

	RTSX32SU	RTSX72SU
Dedicated Registers	1,080	2,012
Maximum I/Os	227	360
Packages	CQFP-84 CQFP-208 CQFP-256 CCLG-256	CQFP-208 CQFP-256 CCLG-624
Manufacturing Flows	883B E-Flow EV-Flow	

Latest Packaging for RTSX-SU

- 84-pin Ceramic Quad Flat Pack
  - A54SX32A-CQ84, RTSX32SU-CQ84
  - Smaller footprint than 208-CQFP
    - 273 vs 853 mm^2, 68% saving
  - Lower mass than 208-CQFP
    - 2.2g vs 8.8g, 75% saving



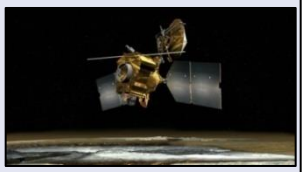
- 256-pin Ceramic Chip-Carrier Land Grid array (CCLG)
  - Integrate programmed and tested FPGAs into Multi-Chip Modules (MCMs)
  - Small package size (17mm x 17mm) fits inside MCM
  - Hermetically sealed, offered with RTSX32SU
  - Uses standard Actel programming hardware

Bond pads on top surface bond FPGA to other components inside MCM

Land grid array underside for testing and programming. Mount on MCM substrate using thermally conductive, electrically non-conductive adhesive

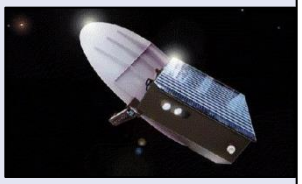
Success in Space – RTSX-SU

Mars Reconnaissance Orbiter Launched August 2005



GPS 2R-M (8 Satellites) Launched Sept 2005 to August 2009

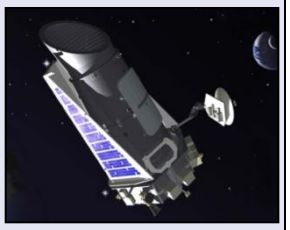
SAR-Lupe 1, 2, 3, 4 and 5 First Launch Dec 2006



TerraSar X Launched June 2007

GLAST Launched June 2008

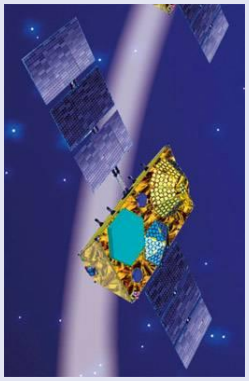
Kepler Launched March 2009



Herschel & Planck Launched May 2009

GPS 2F First Launch May 2010 to May 2013

Globalstar2 First Launch Oct 2010



SBIRS GEO 1/2 May 2011 to March 2013

Mars Science Lab Launched Nov 2011

LandSat 8 Launched Feb 2013

Power Matters

Microsemi

RTAX-S/SL
Designed for Space

RTAX-S/SL

- Radiation-tolerant FPGA alternative to RH ASICs
  - Ten times larger than previous largest space FPGA
    - Up to 4M system gates – approximately 500,000 ASIC gates
  - Designed for space — Single Event Upset (SEU) enhancements
  - 0.15µm, 7-layer metal CMOS with Antifuse, manufactured at UMC
  - Embedded block RAM
  - Multiple Flexible I/O standards
  - Live at Power-up (LAPU)
  - Single chip
  - Low power consumption

RTAX-S/SL FPGA Family

	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL
Dedicated Registers	1,408	6,048	10,752	20,160
I/O Registers	744	1,548	2,052	2,520
Total Modules	4,224	18,144	32,256	60,480
RAM Blocks	12	36	64	120
Total RAM Bits	54K	162K	288K	540K
Max User IO's	248	516	684	840
Packages CQFP CCGA/LGA	 208, 352 624	 352 624	 256, 352 624, 1152	 352 1272
Status	***QML Class Q and QML Class V Qualified Silicon Now Shipping***			

RTAX-SL Low Power Family

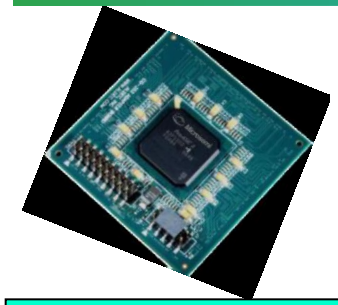
- Reduced stand-by current
- New part numbers
  - SMDs have been updated with new part numbers
  - Power calculator available for all families
- Stand-by current spec
  - Reduced by 70% to 80% relative to standard RTAX-S (worst case conditions)
    - For example RTAX2000SL spec is 150mA at 125°C
  - Dynamic current spec is unchanged
  - Device timing is unchanged

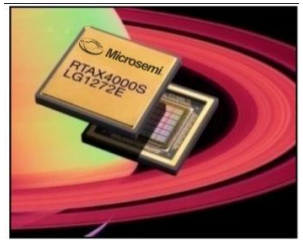
RTAX-S/SL Radiation Data

- Single-event Latch-up (SEL)
  - Testing performed up to LET 117 MeV-cm$^{2/}$mg (125ºC)
  - No SEL observed; No control logic upset observed
- R-Cell Single-event Upset (SEU)
  - LET_{TH} in excess of 37 MeV-cm^2/mg
  - Cross-section < 1E^{-9} cm^2
  - SEU per R-Cell < 4E^{-11} Errors/bit-day (worst case GEO)
- Memory SEU
  - SEU < 1E^{-10} upsets/bit-day (worst case GEO)
    - EDAC operational, background scrubbing at 2MHz
- Single-event Transient (SET)
  - High frequency testing analysis reported at Space Forum www.actel.com/asf
- Total Ionizing Dose (TID)
  - Results indicate suitability for vast majority of space missions
    - Stays within parametric limits beyond 200Krads (si)
    - No functional failure up to 300Krads (si)
  - TID performed on each production wafer lot

All reports posted to http://www.microsemi.com/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data

Complete Development Solutions





Microsemi RTAX-S Prototyping Solutions

Reprogammable Solution Using APA/A3P with ALDEC Adapter	Sockets and Adapter Sockets for using Commercial Devices	Prototype Using Commercial AX Product in Ceramic Package	RTAX-S Proto Units – Mil Temp Tested, No 883B Processing	RTAX-S Production Units – QML Class Q or Class V

Phase 1: Concept Validation	Phase 2: Demonstration Hardware	Phase 3: Test Hardware using flight boards	Phase 4: Final Flight Hardware

Typical Design Phases

RTAX-S/SL Qualification, Reliability and Flight Heritage

RTAX-S/SL Reliability and Qualification Status

- QML Class V qualification granted November 2011
  - RTAX4000S/SL qualified
  - RTAX2000S/SL, RTAX1000S/SL, RTAX250S/SL qualified by extension
  - No plans to discontinue QML-Q (B-flow, E-flow) now that QML-V is available

- Aerospace Corporation (AX2000, I-temp)
  - Identical antifuses, processing, programming to RTAX2000S
  - Longest runners > 38,000 hours HTOL
  - > 26 Million device hours accumulated!
  - One time-zero SRAM failure
    - Would have been detected by 883B screening
  - Testing complete, no antifuse anomalies observed

	Type	Devices	Dev. Hrs
AX2000	HTOL	277	10,894,309
AX2000	LTOL	272	10,011,479
AX2000	Temp Cycle	182	5,586,874
		Total	26,492,662

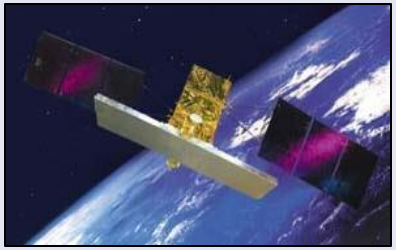
- NASA GSFC (RTAX-S)
  - Testing completed, no anomalies observed

	Type	Devices	Dev. Hrs
RTAX250S	HTOL	82	246,000
RTAX250S	LTOL	82	246,000
RTAX2000S	HTOL	82	246,000
RTAX2000S	LTOL	82	246,000
		Total	984,000

- Microsemi (RTAX-S)
  - Multiple life tests up to 6,000 hours
  - No antifuse failures observed
  - Overall product FIT rate calculated ***< 8 FIT*** (60% confidence level, EA = 0.7eV)

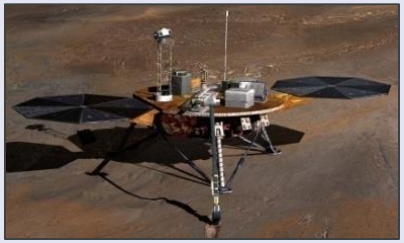
RTAX-S Space Flight Heritage

Cosmo-SkyMed 1, 2, 3 and 4
First Launch
June 2007



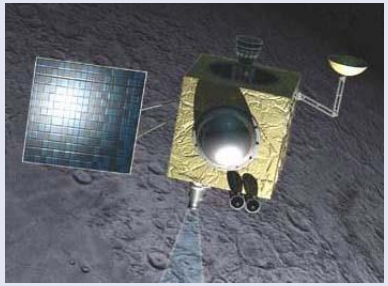
RTAX2000S-CQ352

Mars Phoenix
Launched
August 2007



RTAX1000S-CQ352

Chandrayaan-1
Launched
October 2008



RTAX2000S-CQ352

SDS-1
Launched
January 2009

RTAX2000S-CQ352

GOSAT (IBUKI)
Launched
January 2009

RTAX2000S-CQ352

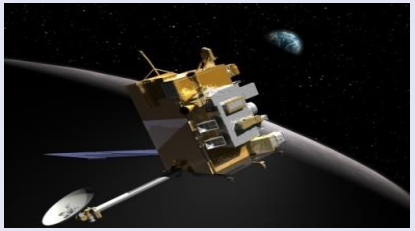
WINDS (KIZUNA)
Launched
February 2009

RTAX2000S-CQ352

Sicral-1B
Launched
April 2009

RTAX2000S-CQ352

LRO & LCROSS
Launched
June 2009



RTAX2000S-CG624 (BAE)
RTAX2000S-CQ352
RTAX250S-CQ208

RTAX-S Space Flight Heritage

IRIS
Launched
November 2009

RTAX1000S-CGS624 (6Σ)
RTAX2000S-CGS624 (6Σ)

Advanced EHF
First Launch
August 2010

RTAX2000S-CQ352

QZSS Michibiki
Launched
September 2010

RTAX2000S-CQ352

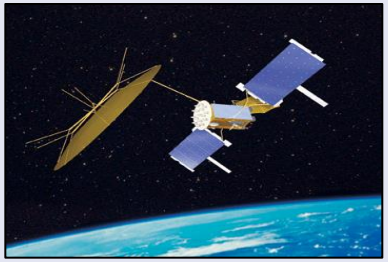
CHIRP
Launched Sept 2011

RTAX4000S-CQ352
RTAX2000S-CG1152
RTAX1000S-CQ352
RTAX250S-CQ208

Mars Science Lab
"Curiosity"
Launched
November 2011

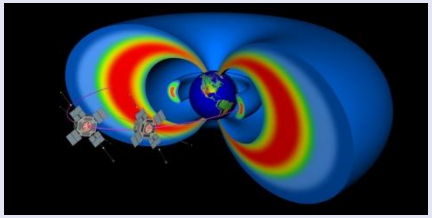
RTAX2000S-CG624 (6Σ)

MUOS
First Launch
February 2012



RTAX2000S-CG624 (BAE)

Radiation Belt
Storm Probes (RBSP)
Launched
August 2012



RTAX1000S-CQ352
RTAX2000S-CQ352

IRNSS-1A
Launched
July 2013

RTAX2000S-CQ256

Planning to Fly RTAX-S

Sentinel 2

CG624

KompSat 3

CG624

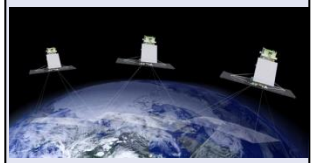
ExoMars

CQ208
CQ256

GOES-R

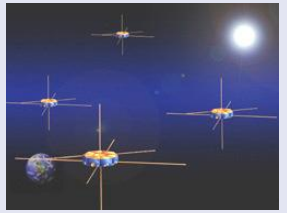
CQ208
CQ352
CG624 - BAE

Radarsat Constellation Mission



CQ352

Magneto-spheric MultiScale

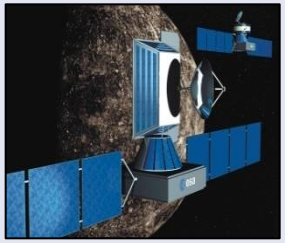


CQ208
CQ352
CG624 - 6Σ

Galileo

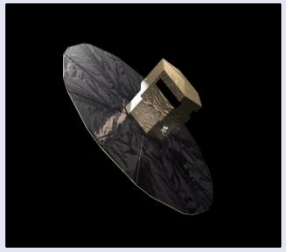
CQ352

Bepi Colombo



CQ208
CQ256
CQ352

Gaia



CG624 - 6Σ
CG1152 - 6Σ

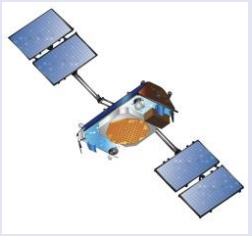
James Webb Space Telescope

CQ352

GPS-III

CQ208
CQ256
CQ352
CG624 - 6Σ

Iridium Next



CQ208
CQ352

Microsemi

Introducing RTAX-DSP

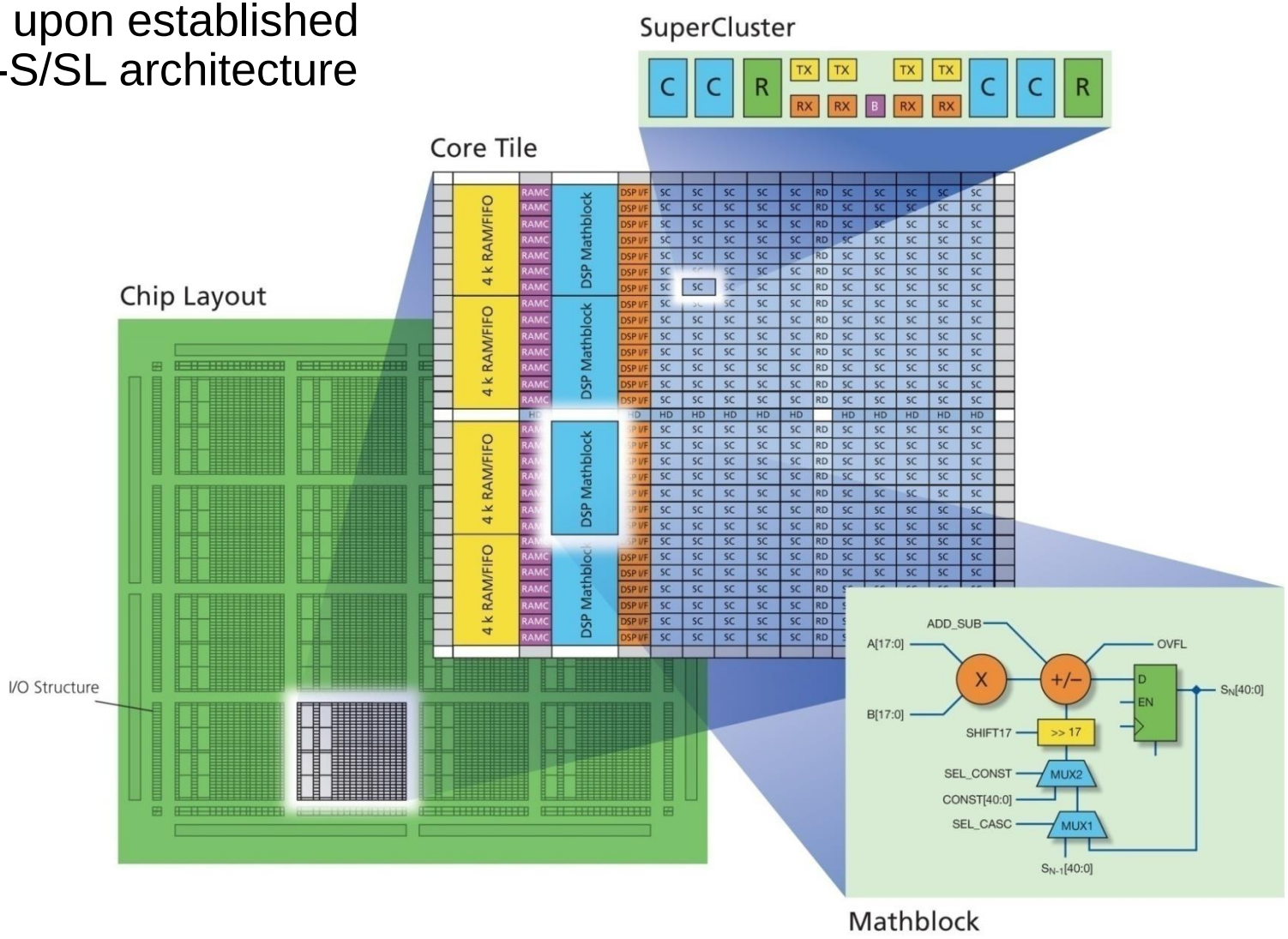
Industry's Most Reliable Space FPGAs Add Sophisticated DSP Capabilities

RTAX-DSP – Fast DSP Without Sacrificing Reliability

- High performance DSP
  - RTAX-DSP Mathblocks run 18bit x 18bit multiply-accumulate at 125MHz over full military temperature range (-55°C to 125°C)
- True radiation tolerance
  - Configuration is not upset or changed by heavy ion radiation
  - DSP blocks protected against heavy ion radiation effects
- Lower power
  - Fewer parts to get the job done means lower power consumption
- Proven reliability
  - RTAX-DSP uses same 0.15µm UMC process, same antifuse programming technology, same basic architecture as RTAX-S/SL
  - Reliability characteristics expected to be identical
- No cost or schedule risk
  - No ASIC tooling charge (or repeat charge, if design changes are made)

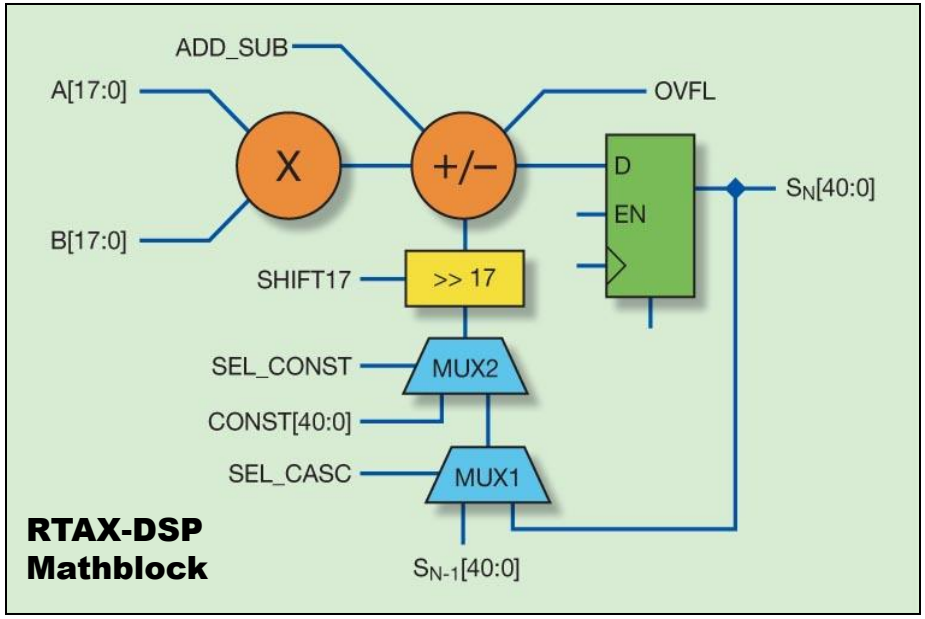
RTAX-DSP Architecture Overview

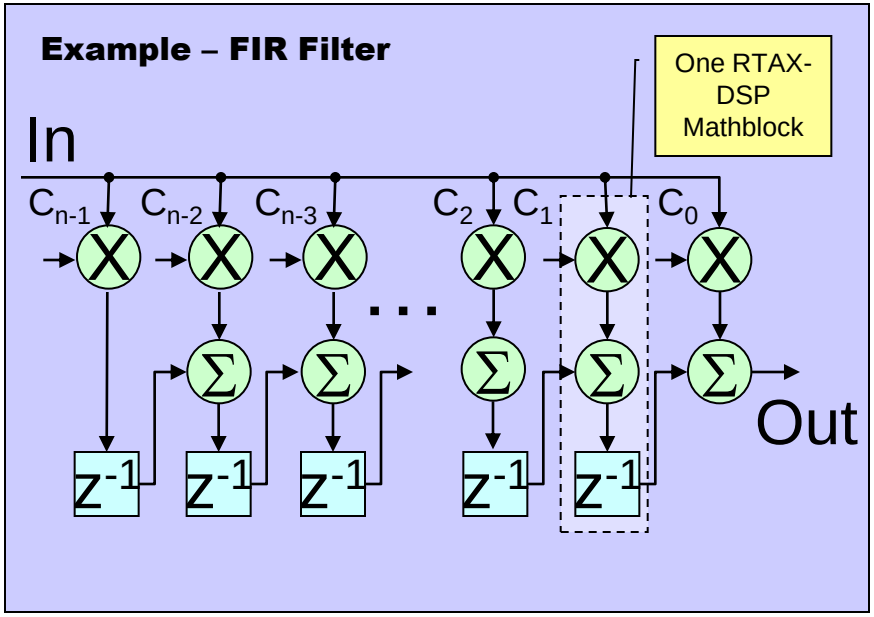
- Builds upon established RTAX-S/SL architecture



RTAX-DSP Mathblocks

- Important in FIR, IIR digital filters and FFT





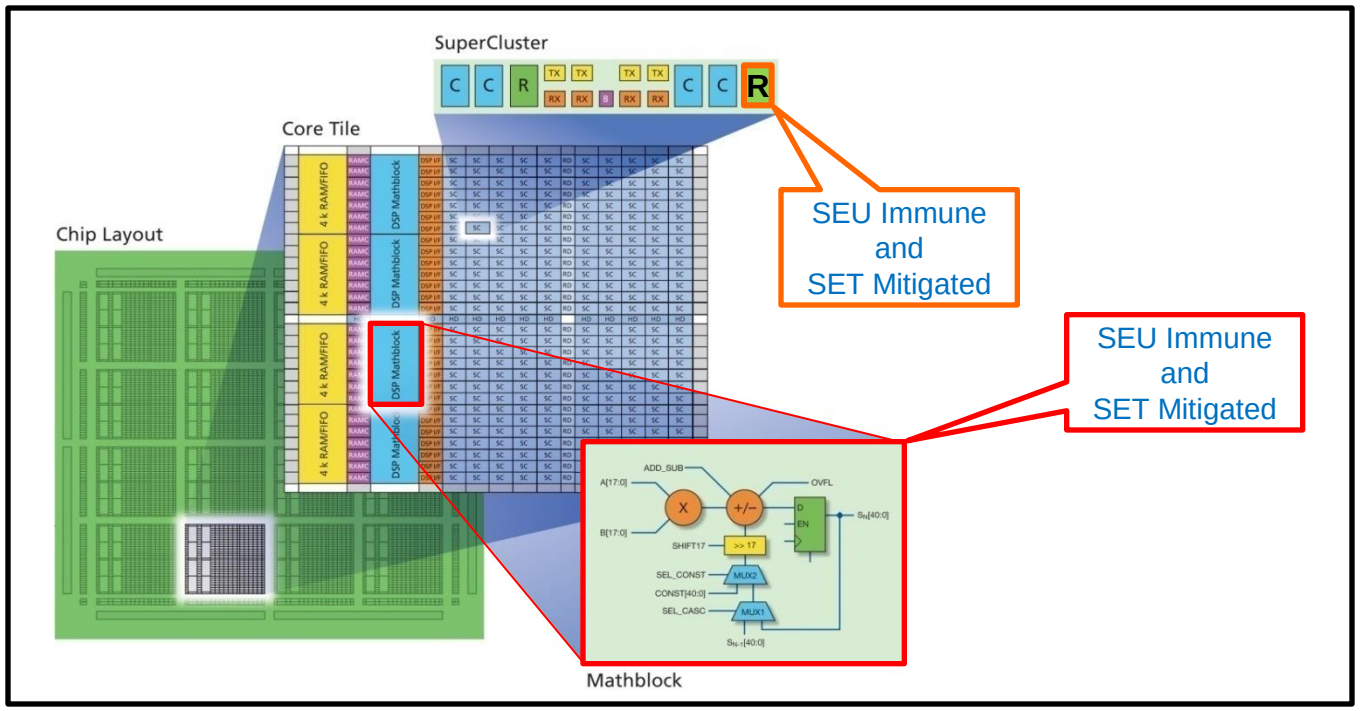
RTAX-S/SL and RTAX-DSP Families

	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX2000D	RTAX4000S/SL	RTAX4000D
System Gates	250K	1M	2M	**2M**	4M	**4M**
Dedicated Registers	1,408	6,048	10,752	**9,856**	20,160	**18,480**
Total RAM Bits	54K	162K	288K	**288K**	540K	**540K**
Max User IO's	248	516	684	**684**	840	**840**
DSP Mathblocks				**64**		**120**
Packages CQFP CCGA/LGA	 208, 352 624	 352 624	 256, 352 624, 1152	 **352** **1272**	 352 1272	 **352** **1272**
Prototype Units	NOW			**NOW (CQ352)**	NOW	**NOW (CQ352)**
Qualification Status	QML Class V Shipping			**QUALIFIED! QML Class V**	QML Class V Shipping	**QUALIFIED! QML Class V**
Flight Units	NOW			**NOW (CQ352)** **Lead Time Applies**	NOW	**NOW (CQ352)** **Lead Time Applies**

- QML class Q and class V qualification completed

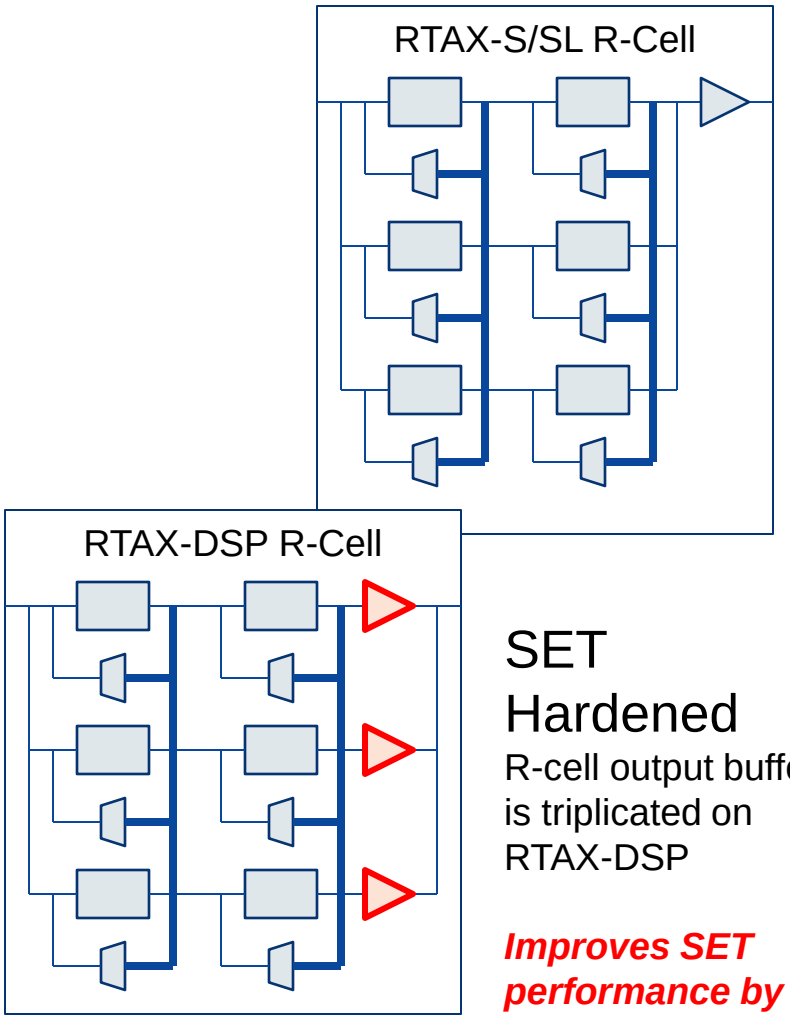
RTAX-DSP Radiation Hardening

- Register Cells
  - Enhanced Single Event Transient (SET) protection in FPGA flip-flops
  - Triple-module redundancy for Single Event Upset (SEU) immunity
- Mathblocks
  - SET protection in Mathblock combinatorial logic
  - SEU protection in Mathblock sequential logic



RTAX-DSP Hardening By Design

R-Cell SET Mitigation

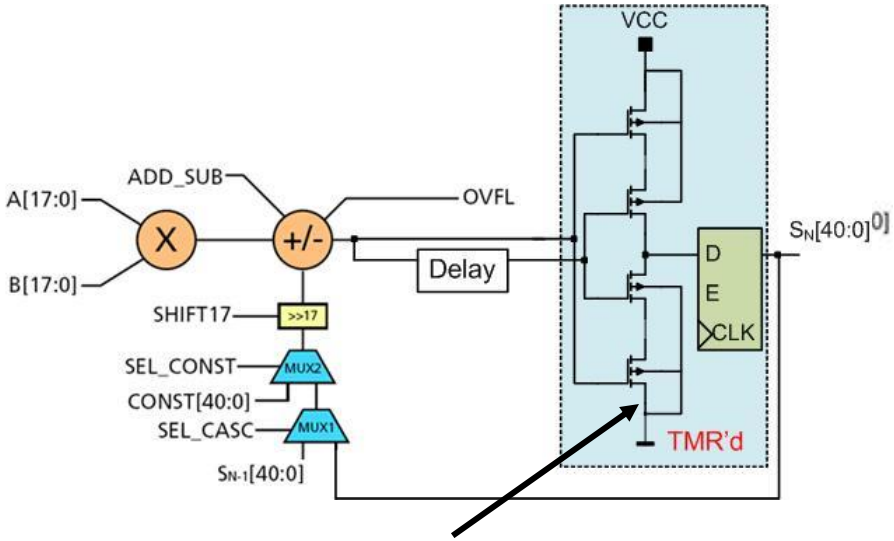


SET Hardened

R-cell output buffer is triplicated on RTAX-DSP

Improves SET performance by up to 16X

Mathblock SET Mitigation



Guard-Gate

- AND gate if signals agree
- Latch if they disagree
- transients less than delay are filtered out

Error rate better than 5E-9 Errors / DSP bit / day

Radiation Summary

- Enhanced R-cell provides approx. 16X more SET protection
  - RTAX-S @120 MHz: 1.9 events / RTAX2000S /100 years
  - **RTAX-D @120 MHz : 0.12 events / RTAX2000D /100 years**

- SET for Mitigated DSP blocks

For a DSP-Bit (SEE/DSP-Bit/Day)
GEO; 100mil; Z=2; no Funneling

SET for DSP blocks	Multiply	ADD/ACC
Frequency	120 MHz	120 MHz
Solar Min	5.03E-09	1.15E-08
Worst Day	4.17E-06	1.27E-05

- All reports for RTAX-DSP can be found in published papers at SEE 2010, NSREC 2010 conferences

  http://www.microsemi.com/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data

IP and Tools

- Smart Gen Mathblock configurator
  - User interface allowing precise configuration of Mathblock
  - Mathblock macro IP cores available now
    - Multiply, Multiply and Add / Subtract, Multiply and Accumulate

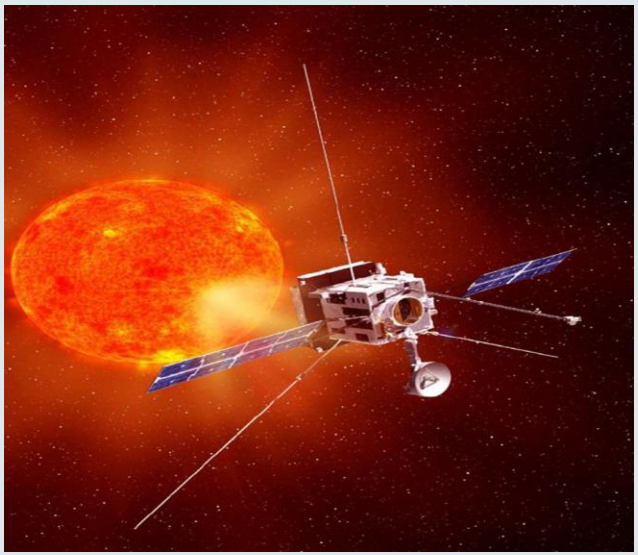
- RTAX-DSP Microsemi IP
  - SmartDesign RTL generator using on-chip math blocks
  - CoreFIR 7.0 for RTAX-DSP available now
  - CoreFFT 5.0 Radix-2 Fast Fourier Transform available now
  - Additional DSP cores to follow

IP Type
Fully enumerated FIR filter
Radix-2 FFT
Folded FIR filter
Interpolation polyphase FIR filter

http://www.microsemi.com/fpga-soc/design-resources/ip-cores

Planning to Fly RTAX-DSP

Solar Orbiter



US Classified Program

Microsemi

Introducing RT ProASIC3 Flash FPGAs for Space

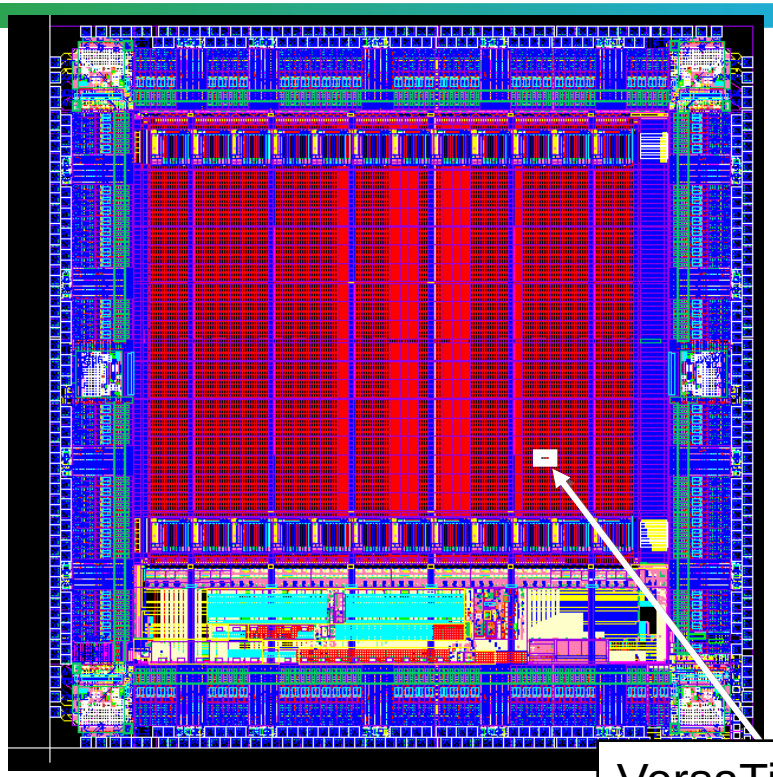
Reprogrammable RT ProASIC®3 Devices Simplify Design of Space Systems

Low Power, Reprogrammable FPGAs for Space

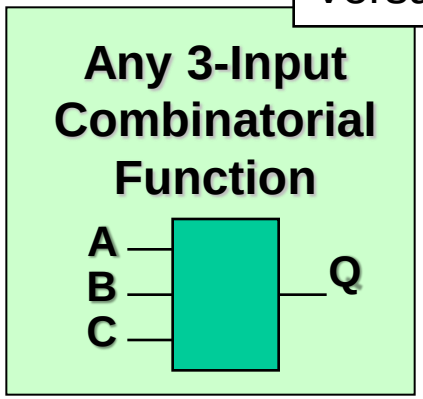
- Reprogrammable FPGAs for Space
  - Easy prototyping and hardware timing validation
    - Prototyping architecture and flight architecture are the same
  - In-system reprogrammable on prototyping board
    - Does not jeopardize integrity of expensive prototyping board
  - Reprogrammable in integrated flight hardware
    - Program with integration test patterns, then reprogram with flight design

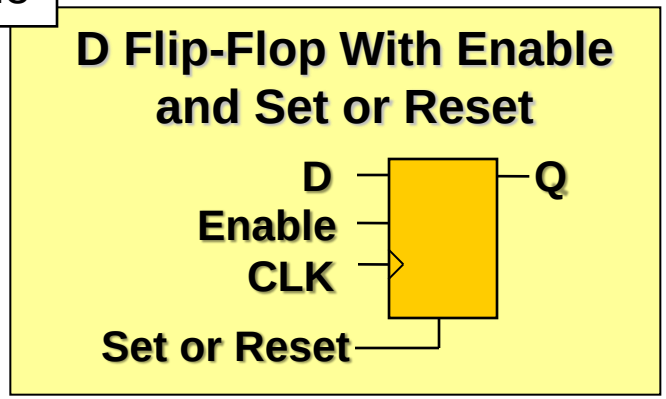
- Advantages of Flash FPGAs over SRAM FPGAs
  - Both Flash- and SRAM-based FPGAs are reprogrammable
  - Flash FPGAs retain their configuration in heavy ion radiation
  - SRAM FPGAs lose their configuration in heavy ion radiation
    - Require mitigation – expensive, excessive power and board space

RT ProASIC3 Device Architecture



- Built using VersaTiles
- Up to 75,264 VersaTiles
  - Each VersaTile Can Be
    - 3-input Combinatorial Gate
    - Latch
    - D-Flip-flop with Enable
  - Register-intensive Applications Handled Easily
- All Input Signals Can Be Inverted
  - Easier Technology Mapping and Netlist Optimizations





RT ProASIC3 Highlights

- Flexible Power Supply Voltage
  - V_{CCA} nominal from 1.2V to 1.5V
  - Lower V_{CCA} for power saving
  - Higher V_{CCA} for higher performance

- Flash*Freeze Ultra Low-Power Mode
  - Flash*Freeze entry / exit in < 1µsec
  - Static power < 0.55mW (RT3PE600L, 25°C)
  - Preserves register states

- Qualification and Screening
  - Mil Std 883 Class B qualification completed
  - B-flow and E-flow available NOW
  - QML class Q qualification is planned for 2014

RT ProASIC3 Summary

	RT3PE600L	RT3PE3000L
System Gates	600K	3M
Tiles	13,824	75,264
Total RAM bits	108K	504K
Flash (ROM) bits	1K	1K
PLLs	6	6
Globals	18	18
Maximum IO	270	620
Packages *(Availability)* CQFP CCGA/LGA	 256 *(NOW)* 484 *(NOW)*	 256 *(NOW)* 484 *(NOW)* , 896 *(NOW)*
STATUS	***Mil Std 883 Class B*** ***Qualification Complete***	

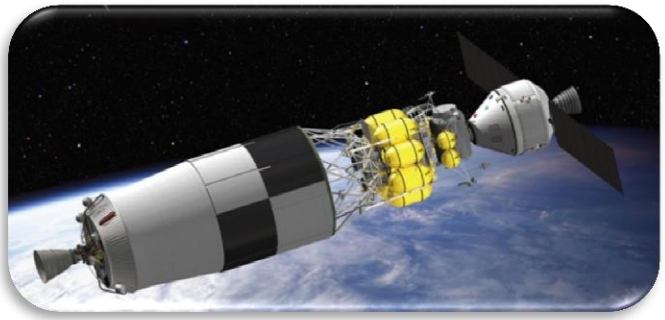
- Prototype with low-cost commercial ProASIC3 devices today
  - Identical silicon, identical timing
    - Plastic FG484 and FG896 match Ceramic CG484 and CG896 footprint
    - RT-PROTO versions are available NOW

Reliability Summary

- Qualification was completed per MIL-STD-883 Class B
- RT3PE3000L-CG896 used as qualifying vehicle
  - 79 units finished 3000+ hours of HTOL
- ESD Results – HBM
  - 2000V on all pins except PLL (500V)
  - Class 1B achieved
- Extensive reliability data set collected for 0.13um Flash process from UMC
  - Overall product FIT rate calculated ***< 8 FIT*** (60% confidence level, EA = 0.7eV)
  - For more details refer to http://www.microsemi.com/soc/documents/ORT_Report.pdf

RT ProASIC3 Radiation Effects and Mitigation

- Projected SEL onset LET at 68 MeV-cm^2/mg
  - Non-destructive SEL events have been observed at LET 80 MeV-cm^2/mg
- No Flash cell configuration upset > 96 MeV-cm^2/mg LET
- Single Event Upsets and Single Event Transients
  - Flip Flops do not upset with TMR mitigation
    - Synopsys Synplify and Mentor Precision RT synthesis have TMR options
  - Memory upsets – use EDAC or redundancy for memory protection
    - Onset LET_{TH} ~ 0.5 MeV-cm^2/mg
  - Other SEEs, requiring manual instantiation of mitigation
    - Clock upsets, Logic transients, I/O bank transients
- Well suited to Low Earth Orbit (LEO)



RT ProASIC3 SEE Summary

	SEL (Events / FPGA-day)	FF SEU (No TMR, Errors / bit-day)	FF SEU (TMR, Errors / bit-day)	Logic Cell SET (Errors / bit-day)	I/O SET (Errors / bit-day)	I/O Bank SET (Errors / bit-day)
Op Frequency	Any	50 MHz	50 MHz	Max	50 MHz	50 MHz
LEO	1.9E-12 (RT3PE600L) 2.7E-10 (RT3PE3000L)	9.6 E-9	SEU Immune	2.9 E-10	7.4 E-10	3.5 E-8
GEO Solar Max		4.82 E-8	SEU Immune	1.79 E-9	4.55 E-9	1.77 E-7
GEO Solar Min		2.65 E-7	SEU Immune	1.45 E-8	3.29 E-8	1.02 E-6
GEO Worst Week		5.73 E-5	SEU Immune	4.22 E-6	8.09 E-6	2.31 E-4
GEO Worst Day		2.08 E-4	SEU Immune	1.44 E-5	2.76 E-5	8.27 E-4

LEO: 1000Km, 41° Inclination
GEO: 100mil; Z=2; No Funneling
http://www.microsemi.com/soc/documents/RT3P_Rad_Rpt.pdf
http://www.microsemi.com/soc/documents/RT3P_SEL_Rpt.pdf

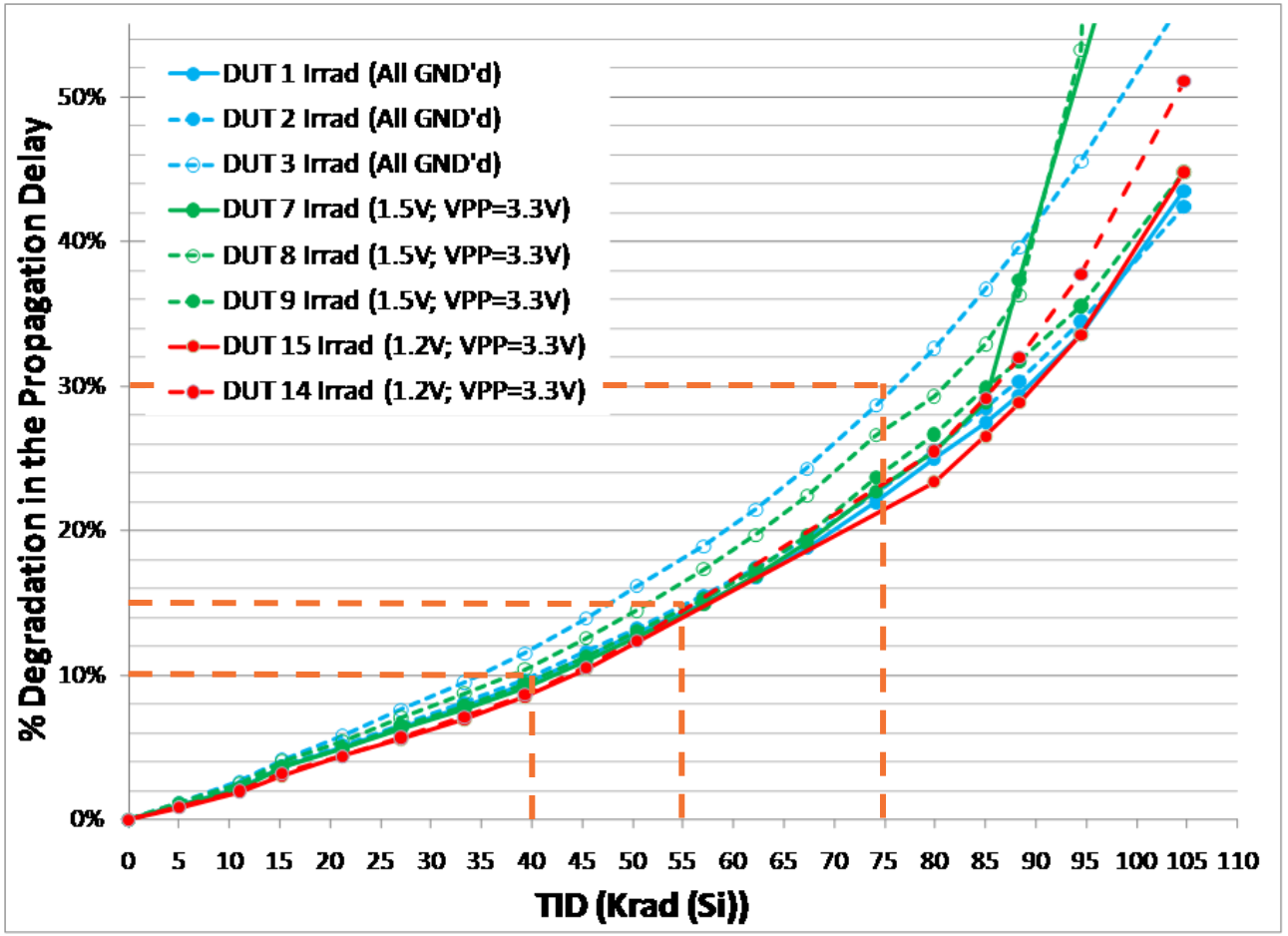
RT ProASIC3 Total Ionizing Dose (TID)

- Production TID test on RT3PE3000L-CG484 flight units
  - Testing at lower dose rates (500 and 5k rad / minute), per TM 1019
    - More representative of space than prior testing (~ 40 Krad / min and higher)
    - For comparison, dose rate in GEO space is around 10 mrad / min
  - Testing with V_{PUMP} pin grounded (recommended)
  - Devices functional after 30 Krad
  - Propagation delay degradation 10% at 25 Krad to 30 Krad
  - DC parameters remain within datasheet specification at 50 Krad
    - Power Supply Current, Input threshold, Output drive and Transition Time
  - http://www.microsemi.com/soc/documents/11T-RT3PE3000L-CG484-QJA2G.PDF

- Experimental low dose-rate TID test
  - Propagation delay degradation 10% at ~40 Krad, 15% at ~55 Krad

Low Dose Rate TID Tests

- Testing at ~ 1 rad / minute
- Propagation delay degradation (two wafer lots tested)
  - 10% at ~ 40 Krad, 15% at ~ 50 Krad, 30% at > 75 Krad



RT ProASIC3 Now in Space

International Space Station

RT3PE3000L-CG484

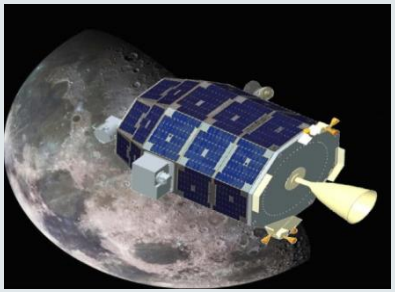
Interface Region Infrared Spectrograph

RT3PE600L-CG484
RT3PE3000L-CG484

Resurs P

RT3PE600L-CG484
RT3PE3000L-LG484

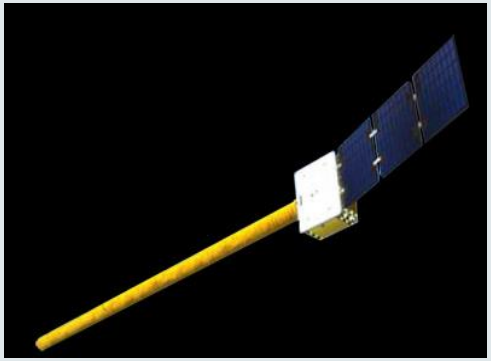
Lunar Atmosphere Dust Environment Explorer



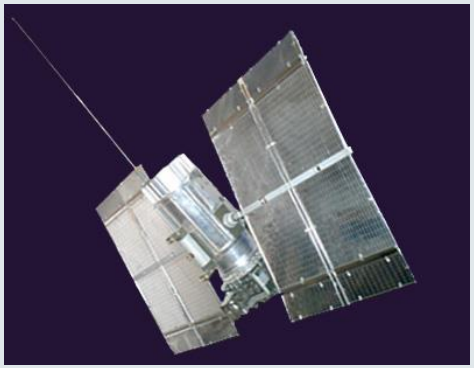
RT3PE3000L-CG484

Planning to Fly RT ProASIC3

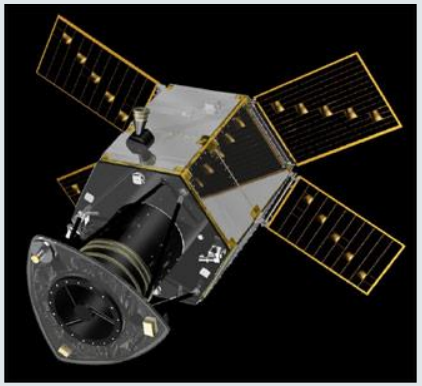
Orbcomm Generation 2



Glonass

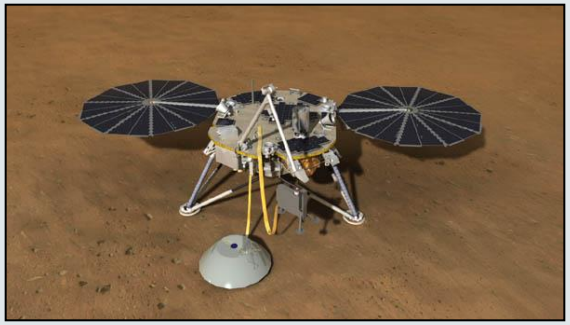


Deimos 2



Iridium Next (Hosted Payload)

Mars InSight



DubaiSat 2

IP for Space Applications

IP for Space Applications

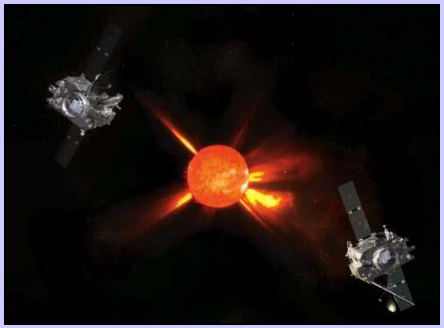
- Microsemi Mil-Std 1553B
  - Bus Controller (BC), Remote Terminal (RT), Monitor Terminal (MT)
  - Can be supplied as netlist or as RTL, includes full test bench
  - Certified per RT validation test plan Mil-Hdbk-1553 Appendix A
- Microsemi CorePCIF
  - 33MHz and 66MHz; Target, Master, Target + Master configurations
- Microsemi CoreFIR
  - Fully enumerated, Folded, and Interpolation Polyphase versions
  - Utilize Mathblocks when targeted to RTAX-DSP
- Microsemi Core FFT
  - Radix-2, forward and inverse up to 8,192-point complex FFT
  - Utilizes Mathblocks when targeted to RTAX-DSP
- Gaisler Leon3-FT
  - 32-bit, SEE immune, 25 DMIPs at 25 MHz in RTAX-S/SL
  - Building flight and design-in heritage

    In Flight: SIR-2 (Norway) on Chandrayaan-1(India), Prisma (Sweden), Tacsat-4 (USA) , RBSP (USA)
    Planning to fly: Bepi Colombo (ESA), MMS (USA), Orbcomm (USA), Glonass-K (Russia)
- Gaisler Spacewire
  - 100Mb/sec or higher in RTAX-S across T and V range

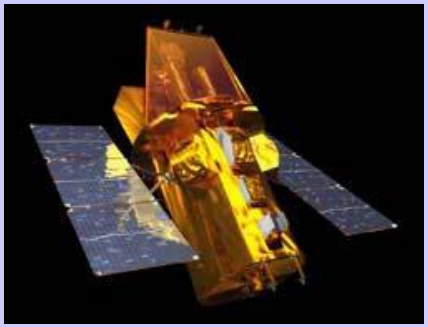
Flight Heritage – IP Cores

EFA Typhoon
First Production Aircraft 2002
PCI

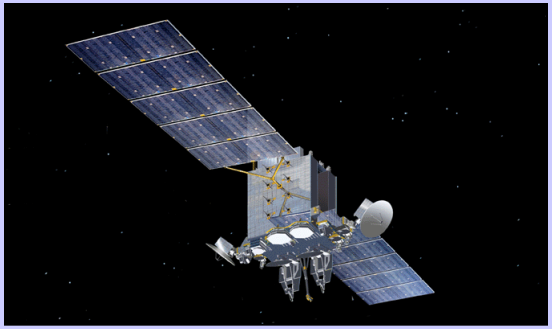
STEREO
Launched 2006
PCI



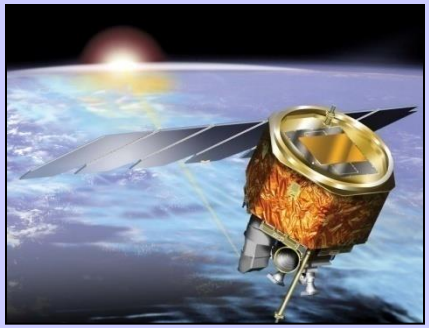
SWIFT / MIDEX
Launched 2004
PCI



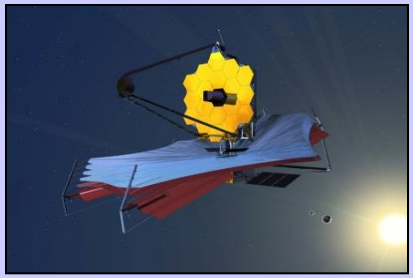
Advanced EHF
Launched August 2010
PCI



SOFIE (Instrument) / AIM
Launched 2007
Mil Std 1553



James Webb
Space Telescope
Launch Expected 2018
Mil Std 1553



Conclusion

- Microsemi is dedicated, focused, and investing in space products and capabilities
- Microsemi has been in the space business as a partner with our customers for more than 55 years
- Microsemi has the system, circuit, and production experience in space to be a long term supplier of state-of-the-art products for long life cycles
- Microsemi uses a system view of applications, and a broad range of technology and design experience to build the best-in-class products for space

Microsemi

Thank You