DG0517
Demo Guide
SmartFusion2 and IGLOO2 PCIe Data Plane Demo Using 2 Channel Fabric DMA

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 9.0

The following is a summary of the changes made in this revision.

- Updated the document for Libero SoC v12.6.
- Removed the references to Libero version numbers.

1.2 Revision 8.0

Updated the document for Libero SoC v11.8 software release.

1.3 Revision 7.0

Updated the document for Libero SoC v11.7 software updates (SAR 77470).

1.4 Revision 6.0

Updated the document for Libero SoC v11.6 software updates (SAR 72063).

1.5 Revision 5.0

Updated the designs files links.

1.6 Revision 4.0

Updated the document for Libero SoC v11.4 software updates (SAR 59587).

1.7 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Updated document for Libero SoC v11.3 and for other enhancements (SAR 56080).
- Updated throughput values in Summary, page 27 (SAR 53490).
- Throughput for Read and Write Transfer type is reversed in Throughput Summary, page 27 (SAR 53822).
- MDDR throughput displayed in Mbps (SAR 53589).

1.8 Revision 2.0

Updated Table 4, page 27 (SAR 53490).

1.9 Revision 1.0

Revision 1.0 is the first publication of this document.

2 SmartFusion2 and IGLOO2 PCIe Data Plane Demo Using 2 Channel Fabric DMA

This demo highlights the high-speed data transfer, the capability of SmartFusion®2 and IGLOO®2 devices through the PCIe interface. To achieve the high-speed data transfers, an Advanced eXtensible Interface (AXI) based Direct Memory Access (DMA) controller is implemented in the FPGA fabric. An application, **PCIe_Demo** that runs in the host PC is provided for setting up and initiating DMA transactions from the SmartFusion2 and IGLOO2 PCIe endpoint to the host PC device. Drivers for connecting the host PC to the SmartFusion2 and IGLOO2 PCIe endpoint are provided as part of the demo deliverables.

Microsemi provides three different PCIe data plane demos for SmartFusion2 devices:

- *DG0501: SmartFusion2 PCIe MSS HPDMA Demo Guide*: This demo shows the low throughput data transfers between PCIe and Double Data Rate (DDR).
- *DG0535: SmartFusion2 PCIe Data Plane Demo using MSS HPDMA and SMC_FIC Demo Guide*: This demo shows the medium throughput data transfers between PCIe and embedded Static Random Access Memory (eSRAM).
- DG0517: SmartFusion2 and IGLOO2 PCIe Data Plane Demo using 2 Channel Fabric DMA Demo Guide (current demo): This demo shows the high throughput data transfers between PCIe and Large Static Random Access Memory (LSRAM).

The high-speed serial interface (SERDESIF) available in the SmartFusion2 and IGLOO2 devices provide a fully hardened PCIe endpoint implementation and is compliant to the PCIe Base Specification Revision 2.0, 1.1, and 1.0. For more information, refer to the *UG0447: SmartFusion2 and IGLOO2 FPGA High Speed Serial Interfaces User Guide*.

This demo demonstrates the performance of the PCIe and DDR controller of the SmartFusion2 and IGLOO2 device families. For a tutorial design on how to develop and use the PCIe endpoint including the tools flow and simulation, refer to the *TU0456: SmartFusion2 SoC FPGA PCIe Control Plane Demo Tutorial.*

2.1 Design Requirements

The following table lists the hardware and software requirements for running this demo design.

Table 1 • **Design Requirements**

Requirement	Version
Hardware	
SmartFusion2 Advanced Development Kit: • 12 V adapter • USB A to Mini-B cable	Rev B or later
IGLOO2 Evaluation Kit: • FlashPro4 programmer • 12 V adapter • USB A to Mini-B cable	Rev C or later
Host PC (or Laptop) with 8 GB RAM and PCIe 2.0 Gen1 or Gen2 compliant slot.	Any 64-bit Windows Operating System
PCI Edge Card Ribbon Cable	
Software	
FlashPro Express	**Note:** Refer to the `readme.txt` file provided in the design files for the software versions used with this reference design.
Libero® System-on-Chip (SoC)	

Note: Libero SmartDesign and configuration screen shots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

Note: For IGLOO2 Kit, PCIe with ×1 or higher is required. For SmartFusion2 Kit, PCIe with ×4 or higher is required.

PCI Express card slot and PCIe Express card adapter (for Laptop only).

PCIe Express card adapter is not supplied with the IGLOO2 Evaluation Kit.

2.2 Prerequisites

Before you begin:

Download and install Libero SoC (as indicated in the website for this design) on the host PC from the following location.

https://www.microsemi.com/product-directory/design-resources/1750-libero-soc

2.3 Demo Design

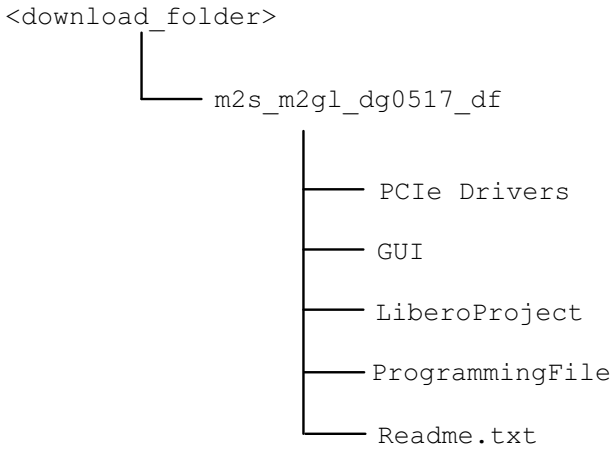
The demo design files are available for download from the following path in the Microsemi website: *http://soc.microsemi.com/download/rsc/?f=m2s_m2gl_dg0517_df*

The demo design files include:

- PCIe Drivers
- GUI
- Libero Project
- Programming files
- Readme file

The following figure illustrates the top-level structure of the design files. For more information, refer to the `readme.txt` file.

Figure 1 • **Demo Design Files Top Level Structure**



The PCIe core in the SmartFusion2 and IGLOO2 devices support both the AXI and AMBA high-performance bus (AHB) master and slave interfaces. This demo design uses the AXI master and slave interfaces to achieve maximum bandwidth. The PCIe_Demo application on the host PC initiates the DMA transfers, and the embedded PCIe core in the SmartFusion2 and IGLOO2 device initiates the AXI transactions through the AXI master interface to the DMA controller in the FPGA fabric. The DMA controller has two independent channels that share the AXI read/write channels of the PCIe AXI slave interface and the MDDR AXI slave interface. The DMA controller in the FPGA fabric initiates the DMA channels depending on the type of the DMA transfer. Each channel has a timer for calculating the throughput and has 4 KB of LSRAM buffer.

DMA channel 0 handles the following DMA transfers:

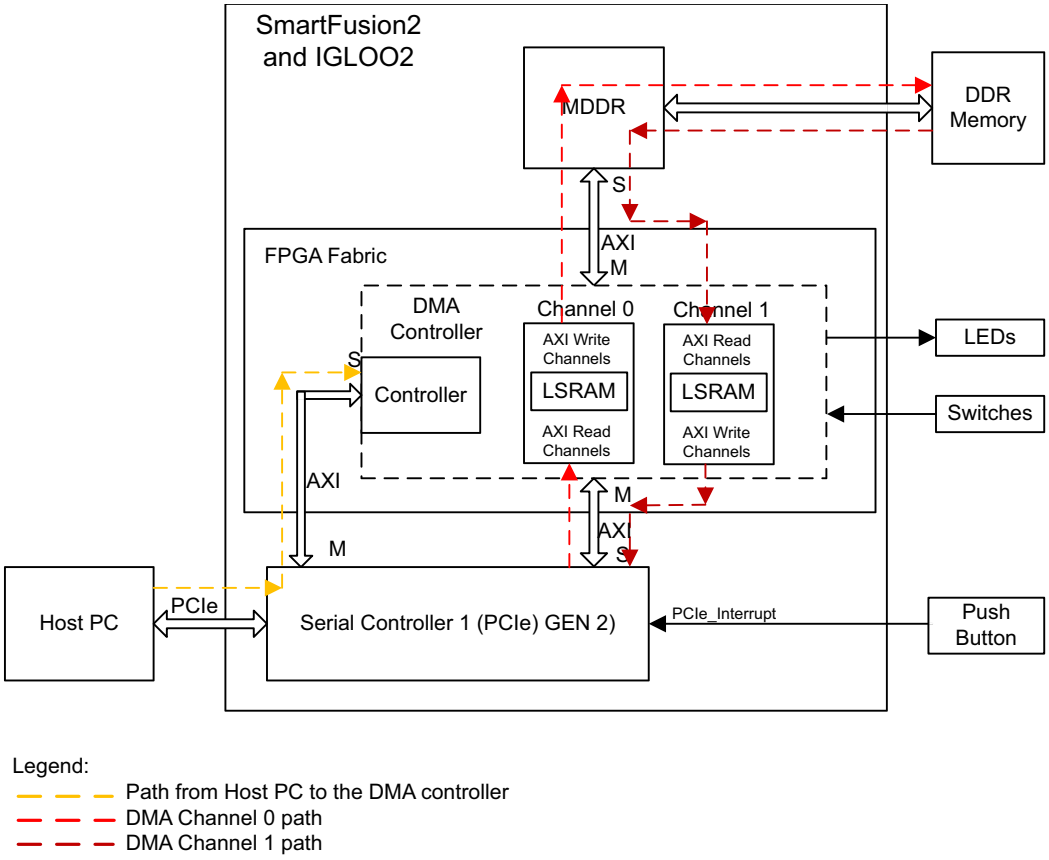
- Host PC memory to LSRAM
- Host PC memory to DDR memory
- LSRAM to DDR memory

DMA channel 1 handles the following DMA transfers:

- LSRAM to host PC memory
- DDR memory to host PC memory
- DDR memory to LSRAM

The following figure illustrates the demo design:

Figure 2 • **PCIe Data Plane Demo Block Diagram**



Legend:

- Path from Host PC to the DMA controller
- DMA Channel 0 path
- DMA Channel 1 path

For the IGLOO2 Evaluation Kit, MDDR is configured for accessing LPDDR memory in x16 mode. The MDDR clock is configured to 155 MHz (310 Mbps DDR) with a 155 MHz DDR_FIC clock for an aggregate memory bandwidth of nearly 620 Mbps. The PCIe AXI interface clock and fabric DMA controller clocks are configured to 155 MHz.

For SmartFusion2 Advanced Development Kit, MDDR is configured for accessing DDR3 memory in x32 mode. The MDDR clock is configured to 310 MHz (620 Mbps DDR) with a 155 MHz DDR_FIC clock for an aggregate memory bandwidth of nearly 2480 Mbps. The PCIe AXI interface clock, ARM Cortex-M3 clock, PCIe AXI interface clock, and fabric DMA controller clocks are configured to 155 MHz.

2.3.1 Demo Design Features

The following are the demo design features:

- DMA data transfers between the host PC memory and the LSRAM
- DMA data transfers between the host PC memory and the DDR memory
- DMA data transfers between the DDR memory and the LSRAM
- Throughput for every DMA data transfer
- Enables continuous DMA transfers for observing throughput variations
- Displays the PCIe link enable/disable, negotiated link width, and the link speed on the PCIe_Demo application
- Displays the position of DIP switches on the SmartFusion2 Advanced Development Kit and IGLOO2 Evaluation Kit on the PCIe_Demo application
- Displays the PCIe Configuration Space on the PCIe_Demo application
- Controls LEDs on the board according to the command from the PCIe_Demo application
- Enables read and write operations to scratchpad register in the FPGA fabric
- Interrupts the host PC, when the Push button is pressed. The PCIe_Demo application displays the count value of the number of interrupts sent from the board.

2.3.2 Demo Design Description

This demo design supports the six different types of data transfers. The following sections describe the process of each data transfer:

- Host PC Memory to LSRAM (Read), page 6
- LSRAM to Host PC Memory (Write), page 6
- Host PC Memory to DDR Memory (Read), page 7
- DDR Memory to Host PC Memory (Write), page 7
- LSRAM to DDR Memory (Write), page 7
- DDR Memory to LSRAM (Read), page 7

2.3.2.1 Host PC Memory to LSRAM (Read)

Data transfer from PC memory to the LSRAM occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address, and size (4 KB).
2. Fabric DMA controller initiates a 16 beat AXI burst (that is, 128 bytes) read transaction to the PCIe AXI slave interface.
3. The PCIe core sends the Memory Read (MRd) Transaction Layer Packets (TLP) to the host PC.
4. The host PC returns a completion (CplD) TLP to the PCIe link.
5. This returned data completes the AXI read initiated by the fabric DMA controller.
6. This data is stored in the LSRAM.
7. The fabric DMA controller repeats this process until the 4 KB of data transfer is completed.
8. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

2.3.2.2 LSRAM to Host PC Memory (Write)

Data transfer from the LSRAM to PC memory occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address, and size (4 KB).
2. Fabric DMA controller reads the LSRAM data and initiates an AXI 16 beat burst write transaction to the PCIe AXI slave interface.
3. The PCIe core sends a Memory Write (MWr) TLP to the host PC.
4. The fabric DMA controller repeats this process until the 4 KB size of the data transfer is completed.
5. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

2.3.2.3 Host PC Memory to DDR Memory (Read)

Data transfer from the PC memory to the DDR memory occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address, and size (4 KB).
2. Fabric DMA controller initiates 16 beat AXI burst (that is, 128 bytes) read transaction to the PCIe AXI interface.
3. The PCIe core sends a memory read (MRd) transaction layer packets (TLP) to the host PC.
4. The host PC returns a Completion Data (CplD) TLP to the PCIe link.
5. This returned data completes the AXI read initiated by the fabric DMA controller.
6. This data is stored in the dual port LSRAM.
7. The LSRAM data is written to the DDR controller through the AXI interface as an AXI 16 beat burst write transaction. The reads from the host PC memory and the writes to the DDR memory occur independent of each other for achieving high throughput. Empty flags are generated in the fabric DMA controller to avoid reading unknown data from the LSRAM.
8. The fabric DMA controller repeats this process until 4 KB of data transfer is completed.
9. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

2.3.2.4 DDR Memory to Host PC Memory (Write)

Data transfer from the DDR memory to the PC memory occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address, and size (4 KB).
2. The fabric DMA controller initiates a 16 beat burst (that is, 128 bytes) AXI read transaction from the DDR through the MDDR controller.
3. The data is stored in the dual port LSRAM.
4. The LSRAM data is written to the PCIe core as an AXI 16 beat burst write transaction. The reads from the DDR memory and writes to the host PC memory occur independent of each other for achieving high throughput. Empty flags are generated in the fabric DMA controller to avoid reading unknown data from the LSRAM.
5. The PCIe core sends a Memory Write (MWr) TLP to the host PC.
6. The fabric DMA controller repeats this process until 4 KB of data transfer is completed.
7. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

2.3.2.5 LSRAM to DDR Memory (Write)

Data transfer from the LSRAM to the DDR memory occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address, and size (4 KB).
2. The LSRAM data is written to the DDR controller through the AXI interface as an AXI 16 beat burst write transaction.
3. The fabric DMA controller repeats this process until 4 KB of data transfer is completed.
4. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application for display.

2.3.2.6 DDR Memory to LSRAM (Read)

Data transfer from the DDR memory to the LSRAM occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address, and size (4 KB).
2. The fabric DMA controller initiates a 16 beat burst AXI read transaction of the DDR through the MDDR controller.
3. The data is stored in the dual port LSRAM.
4. The fabric DMA controller repeats this process until 4 KB of data transfer is completed.
5. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application for display.

2.4 Throughput Calculation

This demo implements a timer to measure the throughput of DMA transfers. The throughput measured includes all of the overhead of the AXI, PCIe, and DMA controller transactions. The procedure for measuring throughput is:

1. Setup the DMA controller for the complete transfer.
2. Start a timer and the DMA controller.
3. Initiate data transfer for the requested number of bytes.
4. Wait till the DMA transfer is completed.
5. Record the number of clock cycles consumed for steps 2-4.

To arrive at realistic system performance, the throughput calculation takes into account all the overheads during a transfer. The throughput formula is as follows:

Throughput = Transfer Size (Bytes) / (Number of clock cycles taken for a transfer * Clock Period)

2.5 Setting Up the Demo Design

2.5.1 Jumper Settings for IGLOO2 Evaluation Kit

1. Connect the jumpers on the IGLOO2 Evaluation Kit, as shown in the following table.

Note: While making the jumper connections, the power supply switch SW7 must be switched OFF.

Table 2 • **IGLOO2 FPGA Evaluation Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J22	1	2	Default
J23	1	2	Default
J24	1	2	Default
J8	1	2	Default
J3	1	2	Default

2. Connect the FlashPro4 programmer to the **J5** connector of the IGLOO2 Evaluation Kit.
3. Connect the power supply to the J6 connector. Switch ON the power supply switch **SW7**.

2.5.2 Jumper Settings for SmartFusion2 Advanced Development Kit

1. Connect the jumpers on the SmartFusion2 Advanced Development Kit, as shown in the following table.

CAUTION: While making the jumper connections, the power supply switch **SW7** must be switched OFF.

Table 3 • **SmartFusion2 FPGA Advanced Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J116, J353, J354, J54	1	2	These are the default jumper settings of the Advanced Development Kit board. Make sure these jumpers are set accordingly.
J123	2	3	
J124, J121, J32	1	2	JTAG programming via FTDI

2. Connect the host PC to the J33 Connector using the USB A to mini-B cable. The USB to UART bridge drivers are automatically detected. Connect the power supply to the J18 connector. Switch ON the power supply switch **SW7**.

2.5.3 Programming the Device

Program the SmartFusion2 Advanced Development kit board or IGLOO2 Evaluation kit board with the job file provided as part of the design files using FlashPro Express software, refer to Appendix 1: Programming the Device Using FlashPro Express, page 27.

2.5.4 Connecting the Kit to Host PC PCIe Slot

1. After successful programming, switch OFF the SmartFusion2 Advanced Development Kit and IGLOO2 Evaluation Kit and **shut down** the host PC.
2. This demo is designed to run in any PCIe Gen 2 compliant slot. If the host PC does not support Gen 2 compliant slot the demo switches to Gen 1 mode.

   Connect the CON1 - PCIe Edge connector of the IGLOO2 Evaluation Kit to the PCIe slot of the host PC or connect the CON1-PCIe Edge connector to the laptop PCIe slot using the Express card adapter. If using a laptop, the Express card adapters support only Gen 1 and the demo works in Gen 1 mode.

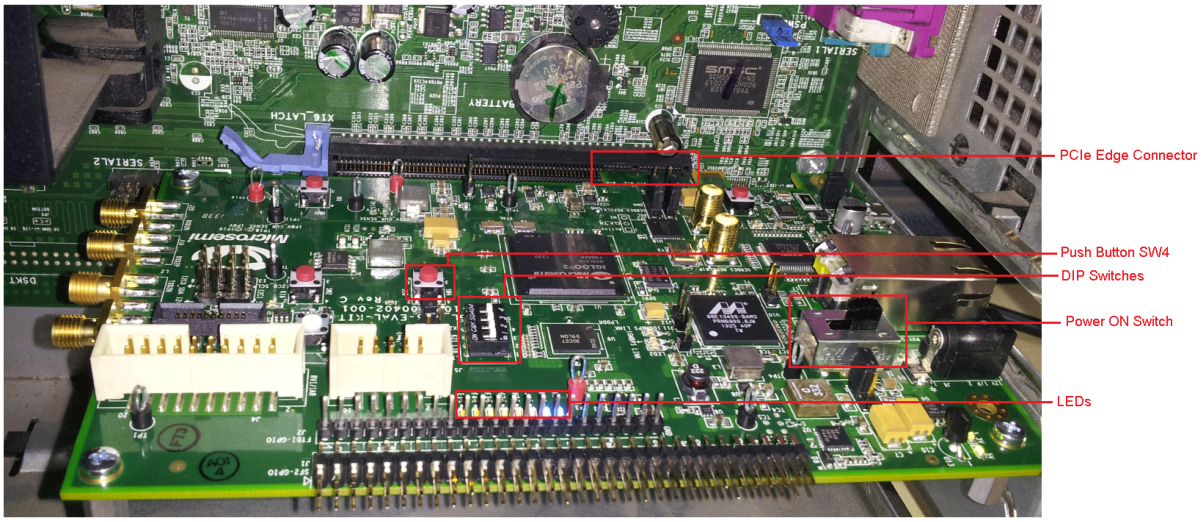
   Or

   Connect the CON1 - PCIe Edge connector of the SmartFusion2 Advanced Development Kit to the host PC's PCIe slot through the PCI Edge card ribbon cable.

Note: Power OFF the host PC (or laptop) while inserting the PCIe Edge connector. If it is not powered OFF, the PCIe device detection and the selection of Gen1 or Gen2 mode may not occur properly. The device detection and selection are dependent on the host PC (or laptop) PCIe configuration.

3. The following figure shows the board setup for the host PC in which IGLOO2 Evaluation Kit is connected to the host PC PCIe slot. To connect the IGLOO2 Evaluation Kit to the laptop using the Express card adapter, refer to Appendix 2: IGLOO2 Evaluation Kit Board Setup for Laptop, page 30.

Figure 3 • **IGLOO2 Evaluation Kit Setup for Host PC**

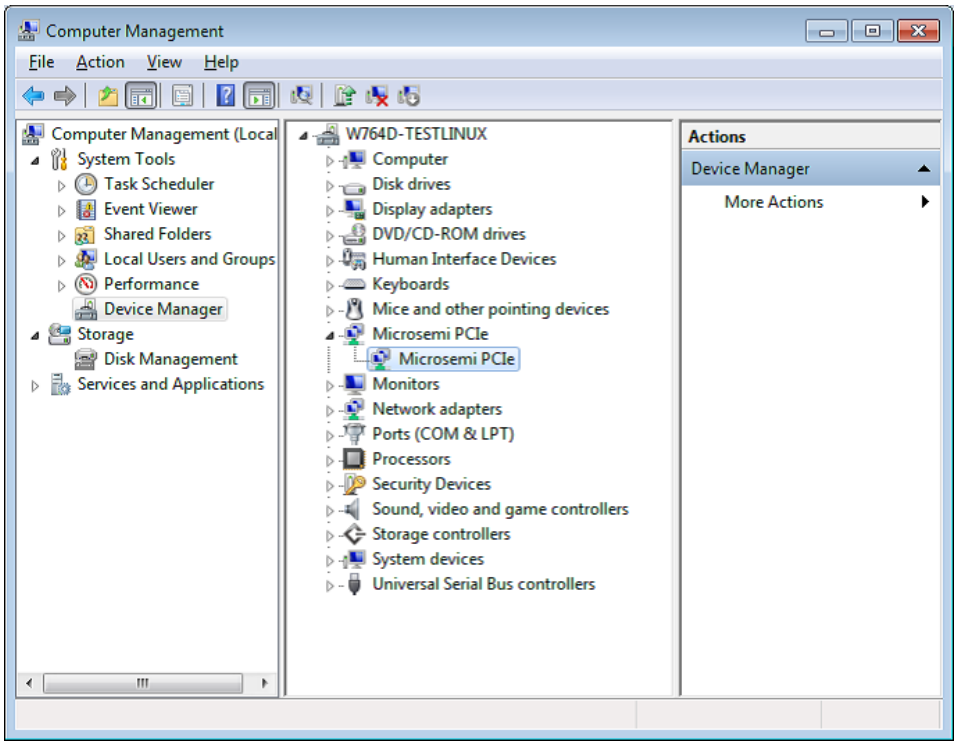


The following figure shows the board setup for the host PC in which the SmartFusion2 Advanced Development Kit is connected to the host PC PCIe slot.

Figure 4 • **SmartFusion2 Advanced Development Kit Setup for Host PC**

4. Switch ON the power supply switch **SW7**.
5. Switch ON the host PC and check the **Device Manager of the Host PC** for **PCIe Device**. The following figure shows the example **Device Manager** window. If the device is not detected, power cycle the SmartFusion2 Advanced Development Kit and IGLOO2 Evaluation Kit and click **scan for hardware changes** option in the **Device Manager**.

Figure 5 • **Device Manager - PCIe Device Detection**



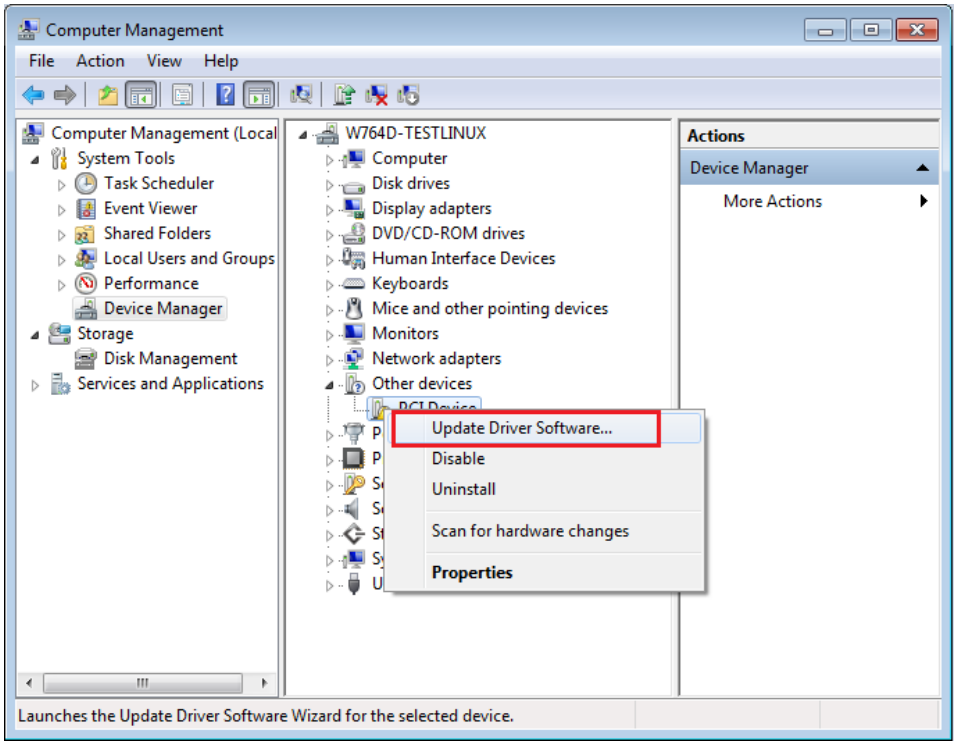
Note: If the device is still not detected, check whether or not the BIOS version in the host PC is latest, and if PCI is enabled in the host PC BIOS.

2.5.5 Driver Installation

Perform the following steps to install the PCIe drivers on the host PC:

1. Right-click **PCI Device** in Device Manager and select **Update Driver Software**... as shown in the following figure.

Figure 6 • **Update Driver Software**



2. In the Update **Driver Software - PCIe Device** window, select the **Browse my computer for driver software** option as shown in the following figure.

Figure 7 • **Browse for Driver Software**

3. Browse the drivers folder: **m2s_m2gl_dg0517_df\PCIe_Drivers\Win_64bit_PCIe_Drivers** and click **Next**, as shown in the following figure.

Figure 8 • **Browse for Driver Software Continued**

4. The **Windows Security** dialog box is displayed and click **Install** as shown in the following figure. After successful driver installation, a message window appears as shown in Figure 10, page 14.

Figure 9 • **Windows Security**

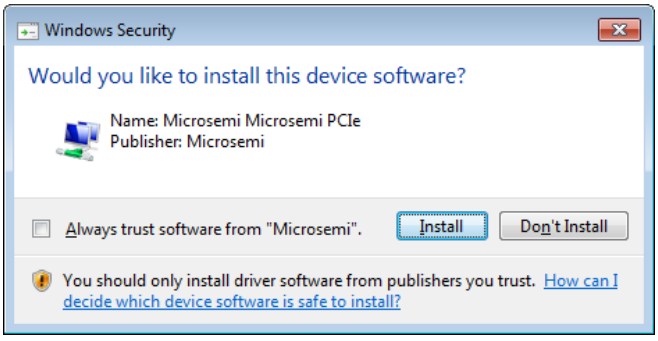
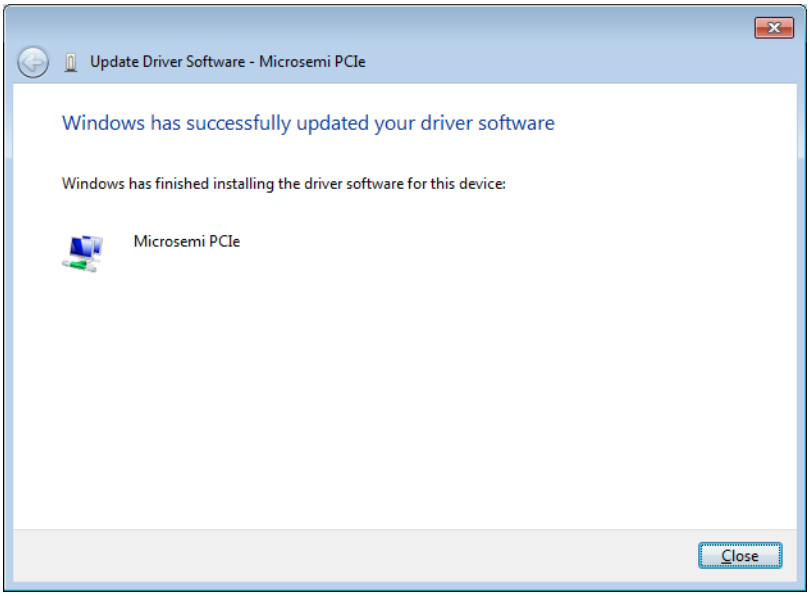


Figure 10 • **Successful Driver Installation**

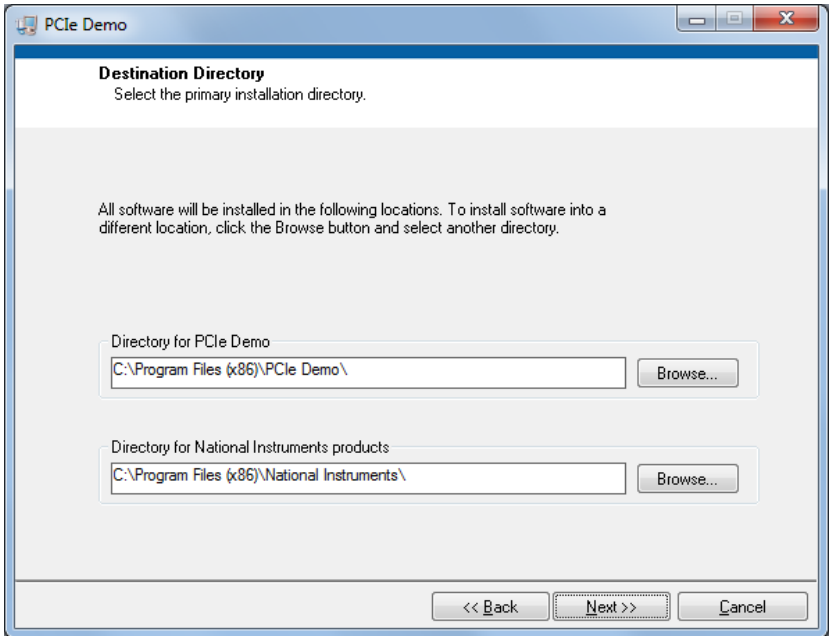


2.5.6 PCIe_Demo Application

The PCIe_Demo application is a simple graphic user interface that runs on the host PC to communicate with the SmartFusion2 and IGLOO2 PCIe endpoint devices. It provides PCIe link status, driver information, and demo controls. The PCIe_Demo application invokes the PCIe driver installed on the host PC and provides commands to the driver according to the selection made. To install the PCIe_Demo application:

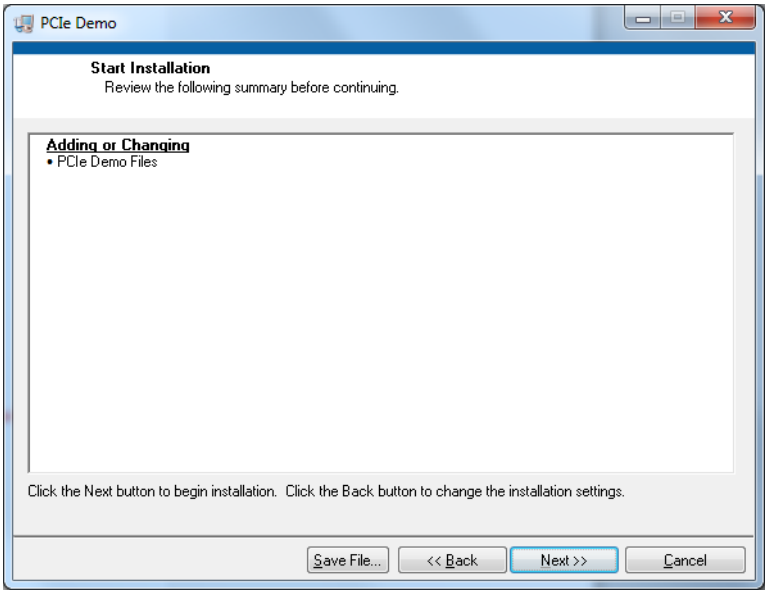
1. Extract the **PCIe_Demo_GUI_Installer.rar** and locate the files at **m2s_m2gl_dg0517_df\GUI**.
2. Double-click the **setup.exe** in the provided GUI installation (`PCIe_Demo_GUI_Installer\setup.exe`).
3. Apply default options, as shown in the following figure.

Figure 11 • **Installing PCIe_Demo Application**



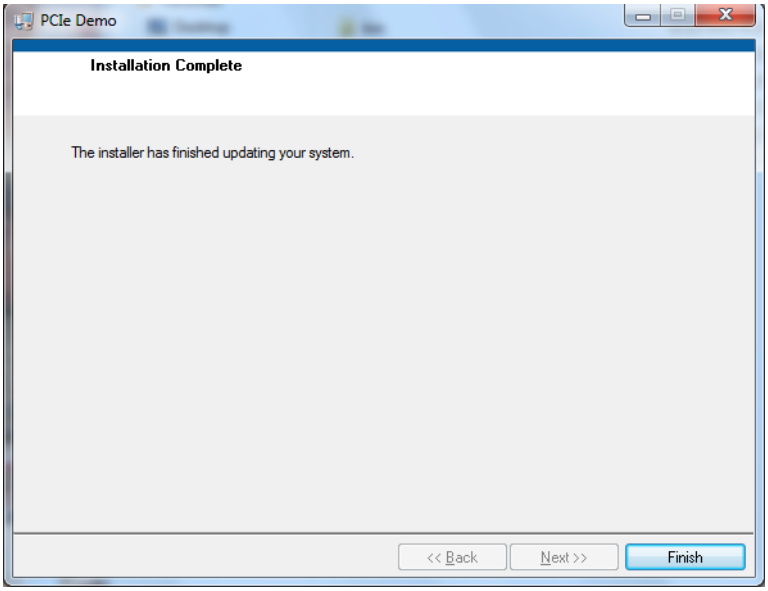
4. To start the installation, click **Next**.

Figure 12 • **PCIe_Demo Application Installation Steps**



5. Click **Finish** to complete the installation.

Figure 13 • **Successful Installation of PCIe_Demo Application**



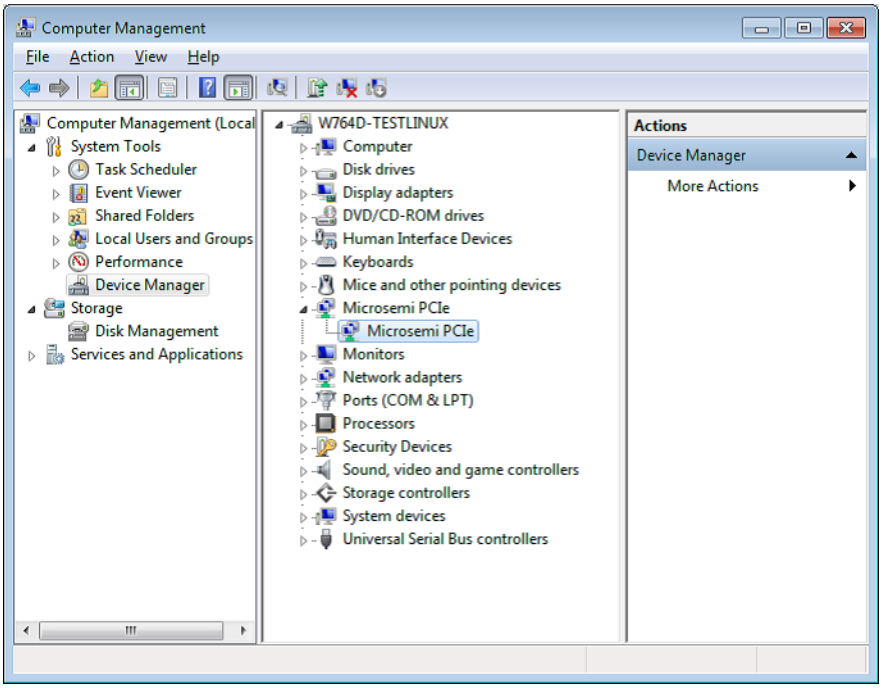
6. Shut down the host PC.
7. Power cycle the SmartFusion2 Advanced Development Kit.
8. Restart the host PC.

2.6 Running the Design

The following steps describe how to run the demo design:

1. Expand the **Microsemi PCIe** device in the host PC **Device Manager**, as shown in the following figure.

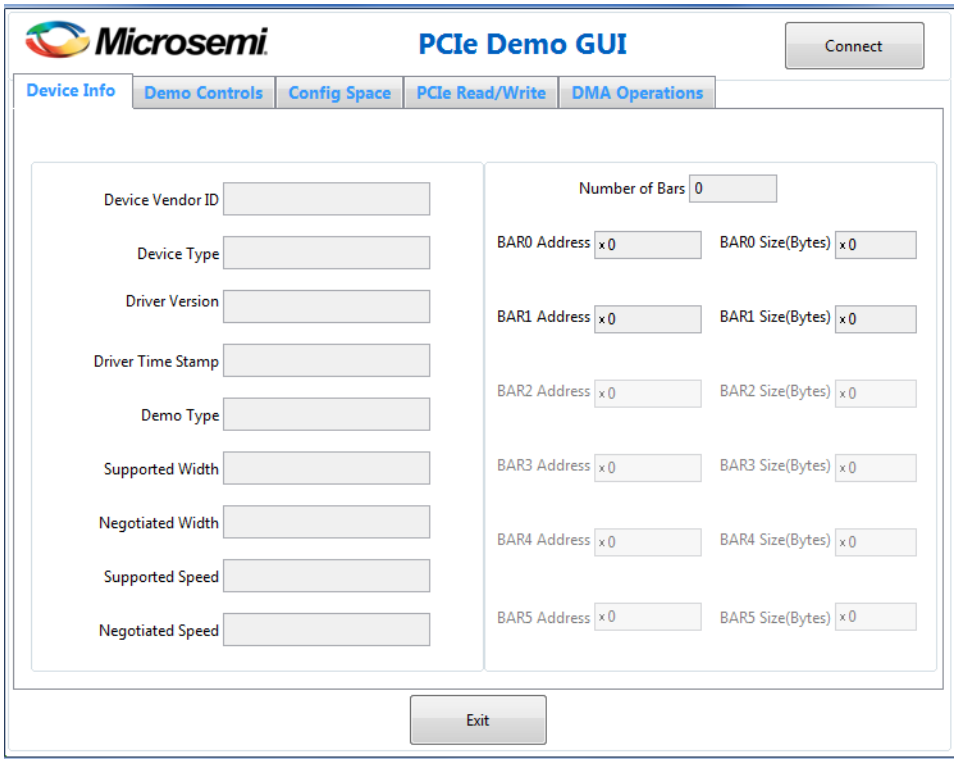
Figure 14 • **Device Manager - PCIe Device Detection**



Note: If a warning message is displayed for Microsemi PCIe driver while accessing, uninstall and re-install the driver.

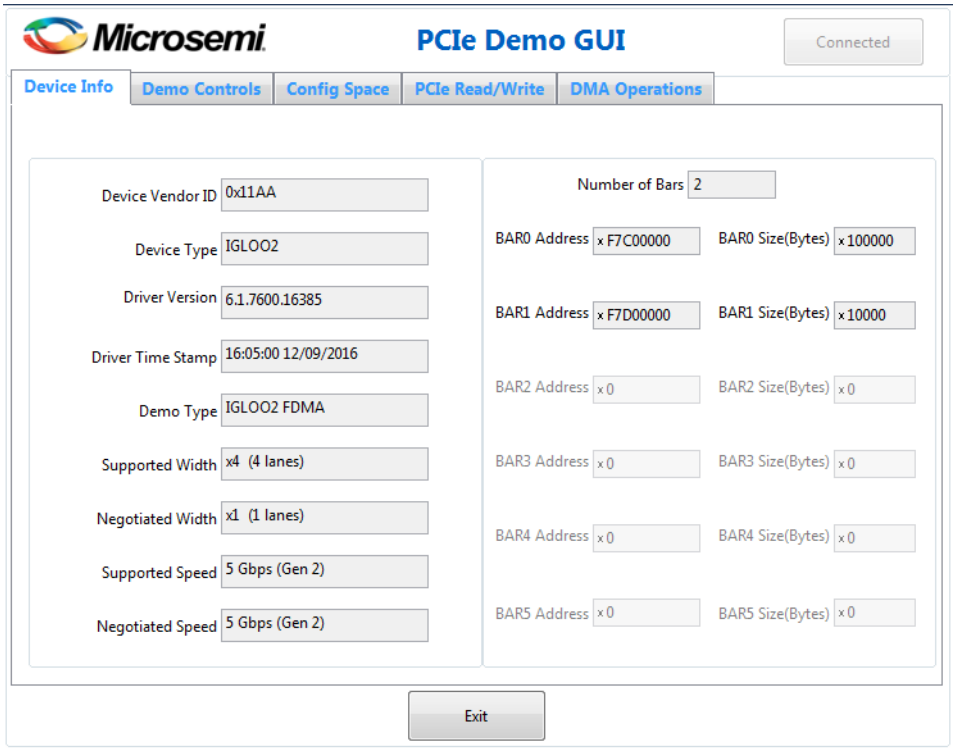
2. Go to **All Programs** > **Microsemi_PCIe_Demo** > **Microsemi_PCIe_GUI**. The **PCIe Demo GUI** window is displayed as shown in the following figure.

Figure 15 • **PCIe Demo Application**



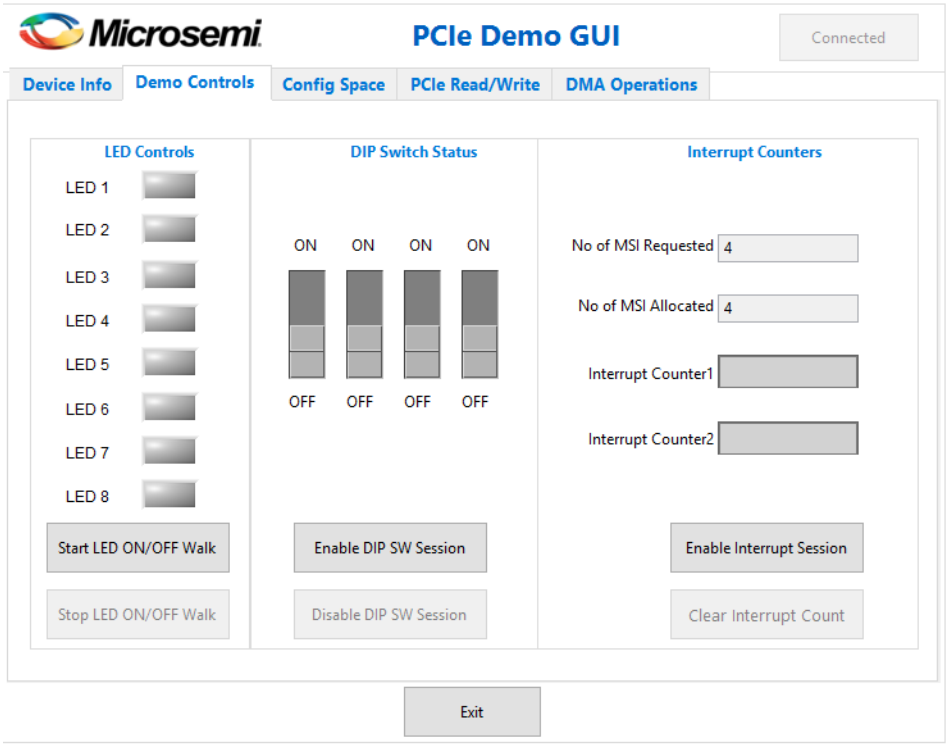
3. Click **Connect**. The application detects and displays the information related to the connected kit such as Device Vendor ID, Device Type, Driver Version, Driver Time Stamp, Demo Type, Supported Width, Negotiated Width, Supported Speed, Negotiated Speed, Number of Bars, and BAR Address as shown in the following figure.

Figure 16 • **Device Info**



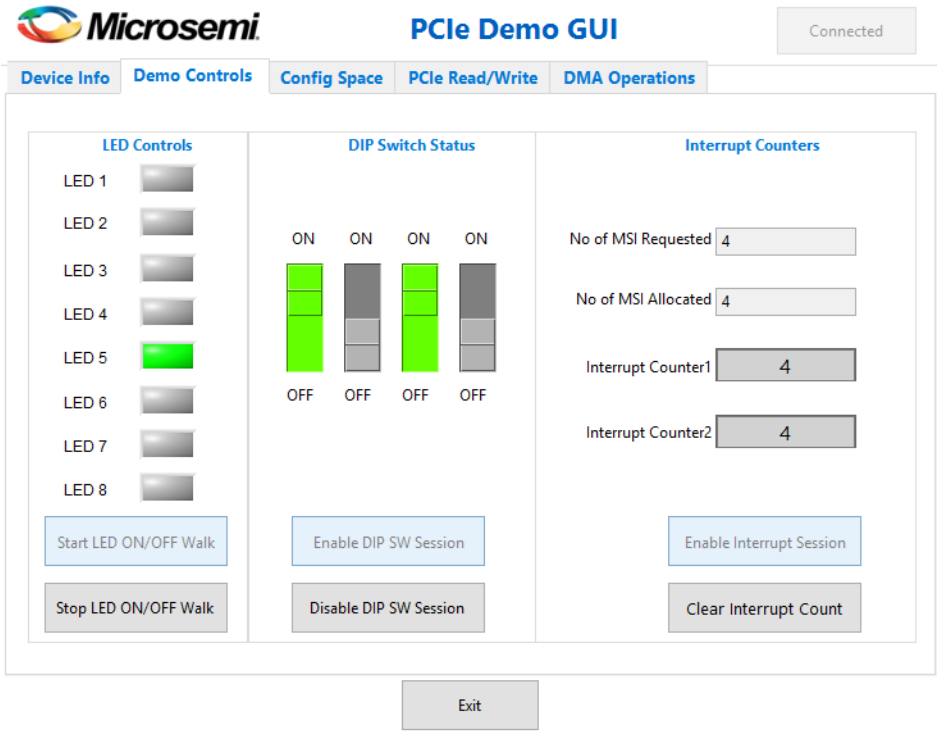
4. Click **Demo Controls** tab to display the **LED Controls**, **DIP Switch Status**, and **Interrupt Counters**, as shown in the following figure.

Figure 17 • **Demo Controls**



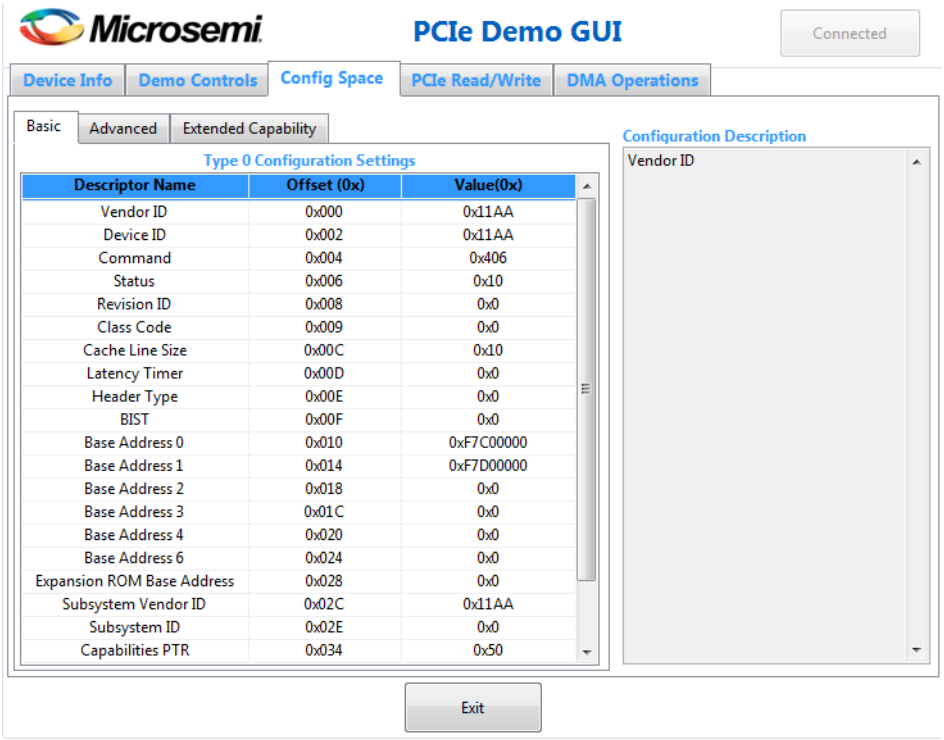
5. Click **Start LED ON/OFF Walk**, **Enable DIP SW Session**, and **Enable Interrupt Session** to view controlling LEDs, getting the DIP switch status, and monitoring the interrupts simultaneously, as shown in the following figure.

Figure 18 • **Demo Controls – Continued**



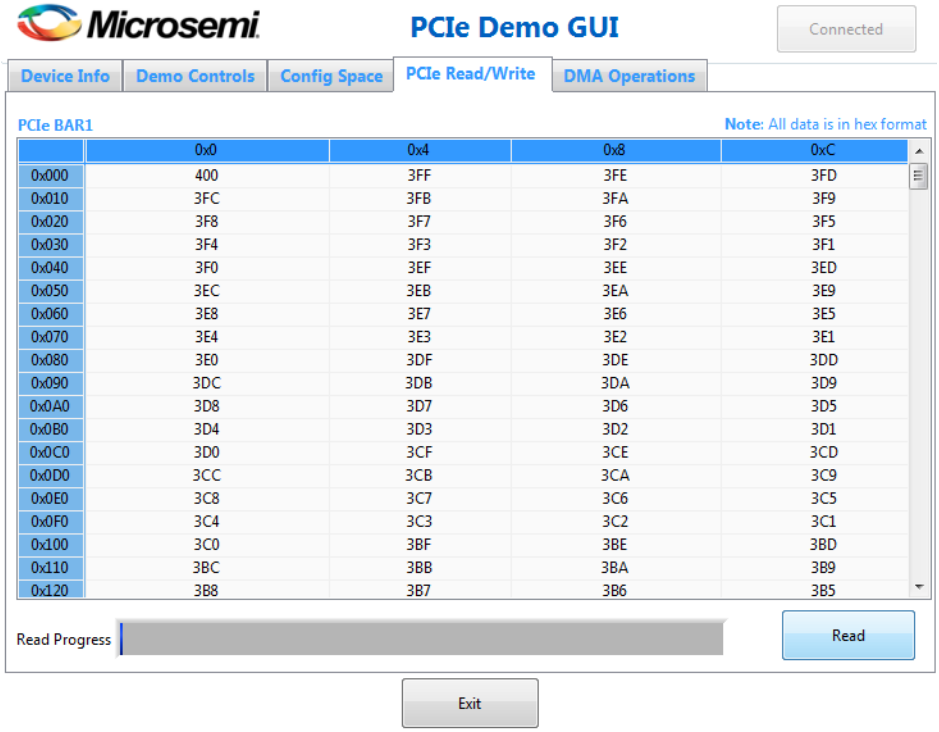
6. Click **Config Space** tab to view the details about the PCIe configuration space, as shown in the following figure.

Figure 19 • **Configuration Space**



7. Click **PCIe Read/Write** tab to perform read and write to LSRAM using BAR1 space.
8. Click **Read** to read the 4 KB memory mapped to BAR1 space as shown in the following figure.

Figure 20 • **PCIe BAR1 Memory Access**



	0x0	0x4	0x8	0xC
0x000	400	3FF	3FE	3FD
0x010	3FC	3FB	3FA	3F9
0x020	3F8	3F7	3F6	3F5
0x030	3F4	3F3	3F2	3F1
0x040	3F0	3EF	3EE	3ED
0x050	3EC	3EB	3EA	3E9
0x060	3E8	3E7	3E6	3E5
0x070	3E4	3E3	3E2	3E1
0x080	3E0	3DF	3DE	3DD
0x090	3DC	3DB	3DA	3D9
0x0A0	3D8	3D7	3D6	3D5
0x0B0	3D4	3D3	3D2	3D1
0x0C0	3D0	3CF	3CE	3CD
0x0D0	3CC	3CB	3CA	3C9
0x0E0	3C8	3C7	3C6	3C5
0x0F0	3C4	3C3	3C2	3C1
0x100	3C0	3BF	3BE	3BD
0x110	3BC	3BB	3BA	3B9
0x120	3B8	3B7	3B6	3B5

9. Click **DMA Operations** tab for different DMA operations such as DDR and LSRAM.

2.6.1 DDR DMA Operations

The following instructions describe the different ways to read data through DDR:

1. Select one of the following options from the **FDMA Transfer Type Selection** drop-down list:
   - **PC -> DDR**—to transfer the data from host PC to SmartFusion2/IGLOO2 DDR memory
   - **DDR-> PC**—to transfer the data from SmartFusion2/IGLOO2 DDR memory to host PC
   - **Both PC <-->DDR**—to transfer the data from host PC to and from SmartFusion2/IGLOO2 DDR memory
2. Enter the **Loop Count** in the box.
3. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput in Mbps and average throughput in Mbps, as shown in the following figures.

Figure 21 • **FDMA Transfer Type Selection – PC to DDR**

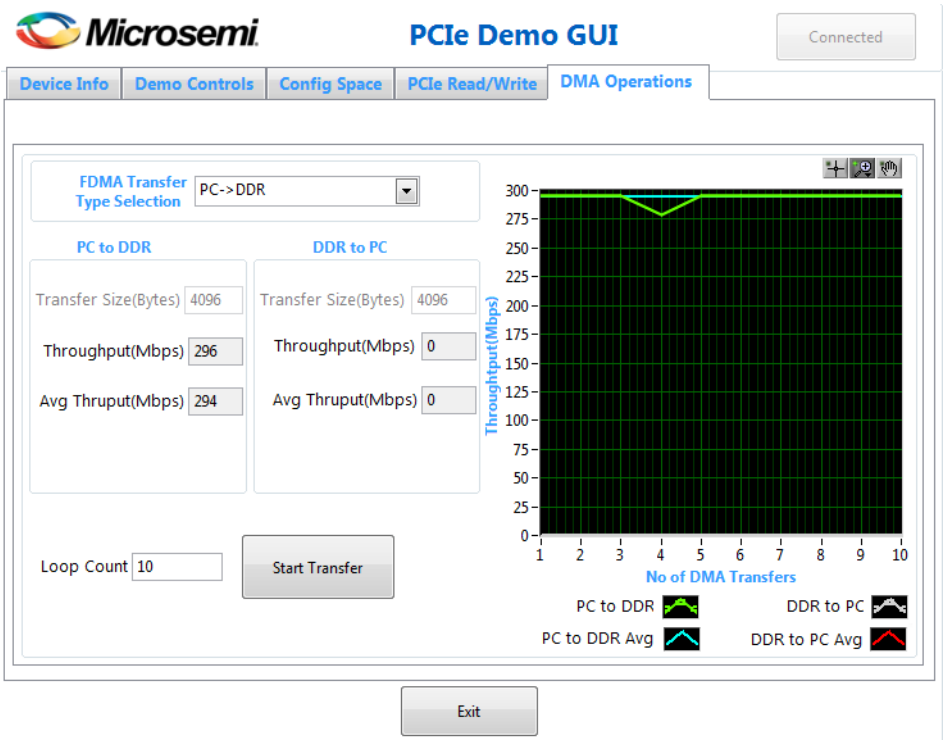


Figure 22 • **FDMA Transfer Type Selection – DDR to PC**

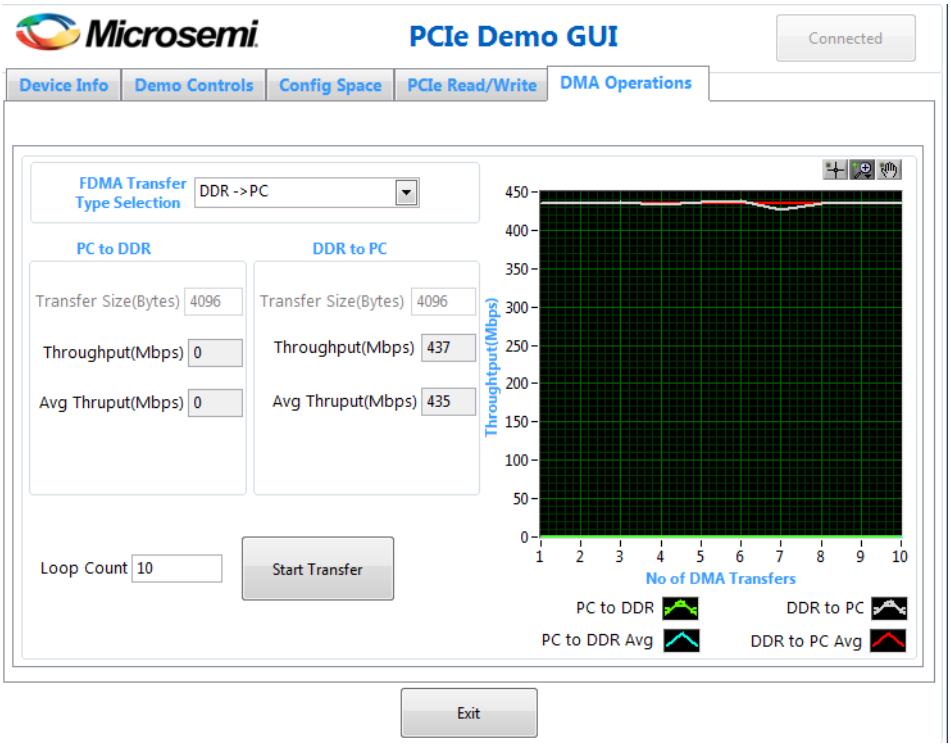
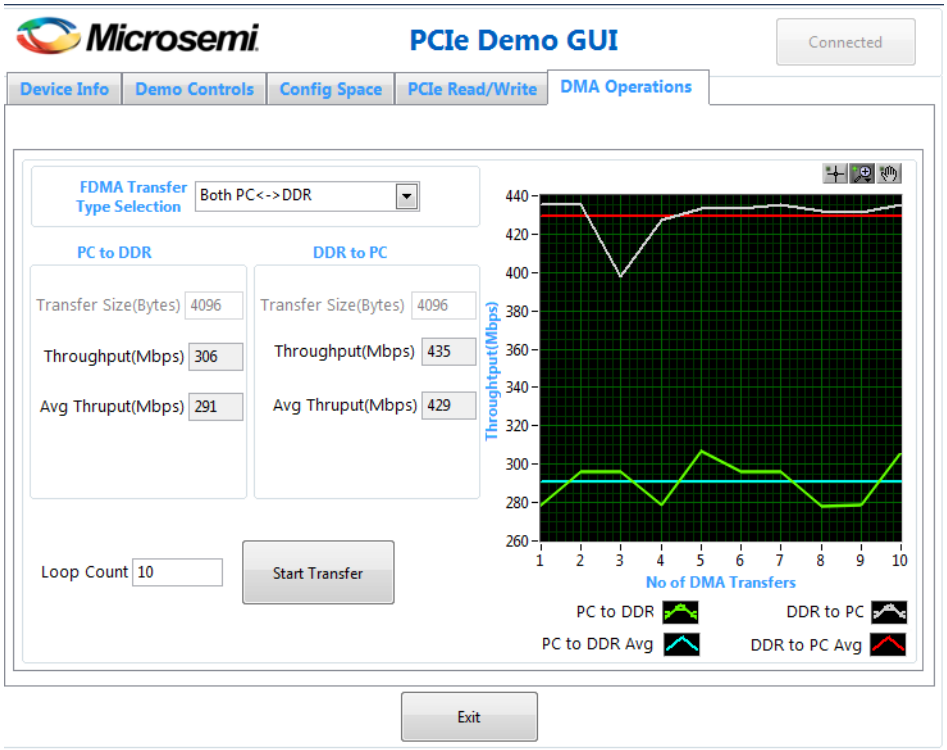


Figure 23 • **FDMA Transfer Type Selection – Both PC to and from DDR**



2.6.2 LSRAM DMA Operations

The following instructions describe the different ways to read data through LSRAM:

1. Select one of the following options from the **FDMA Transfer Type Selection** drop-down list:
   - **PC -> LSRAM**—to transfer the data from host PC to SmartFusion2/IGLOO2 LSRAM memory
   - **LSRAM-> PC**—to transfer the data from SmartFusion2/IGLOO2 LSRAM memory to host PC
   - **Both PC <-->LSRAM**—to transfer the data from host PC to and from SmartFusion2/IGLOO2 LSRAM memory
2. Enter the **Loop Count** in the box.
3. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput in Mbps and average throughput in Mbps, as shown in the following figures.

Figure 24 • **PC to LSARM – FDMA Transfer Type Selection**

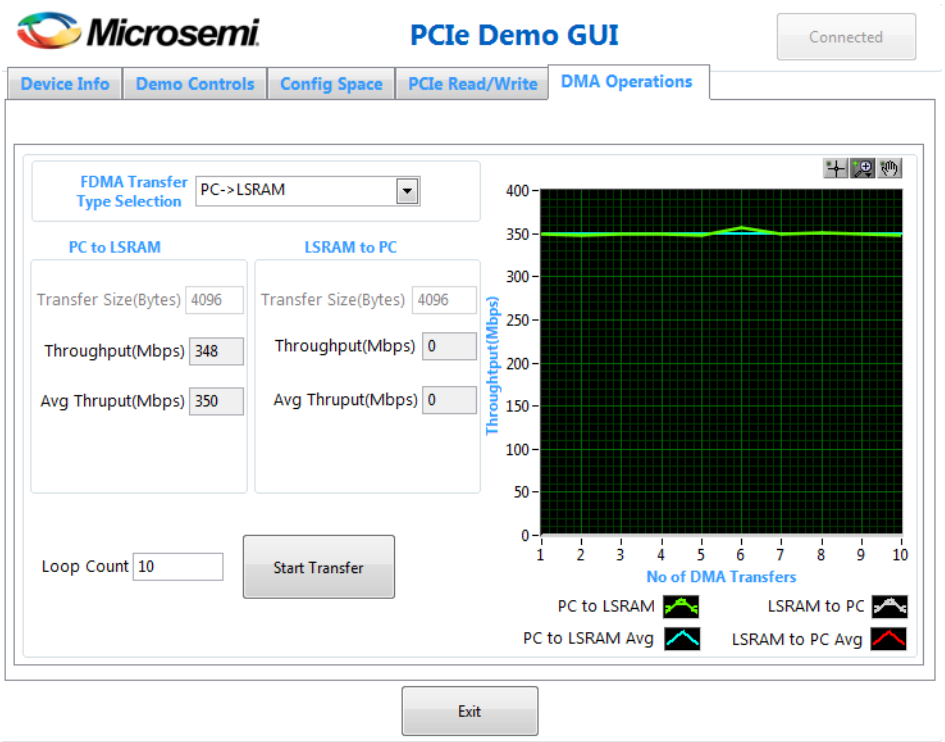


Figure 25 • **LSARM to PC – FDMA Transfer Type Selection**

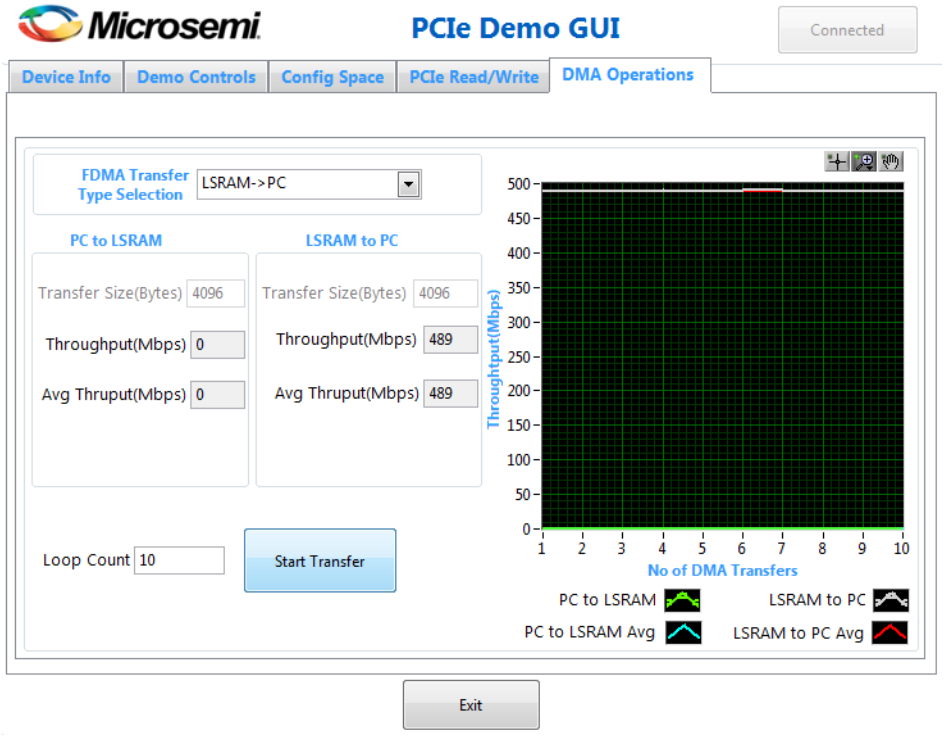
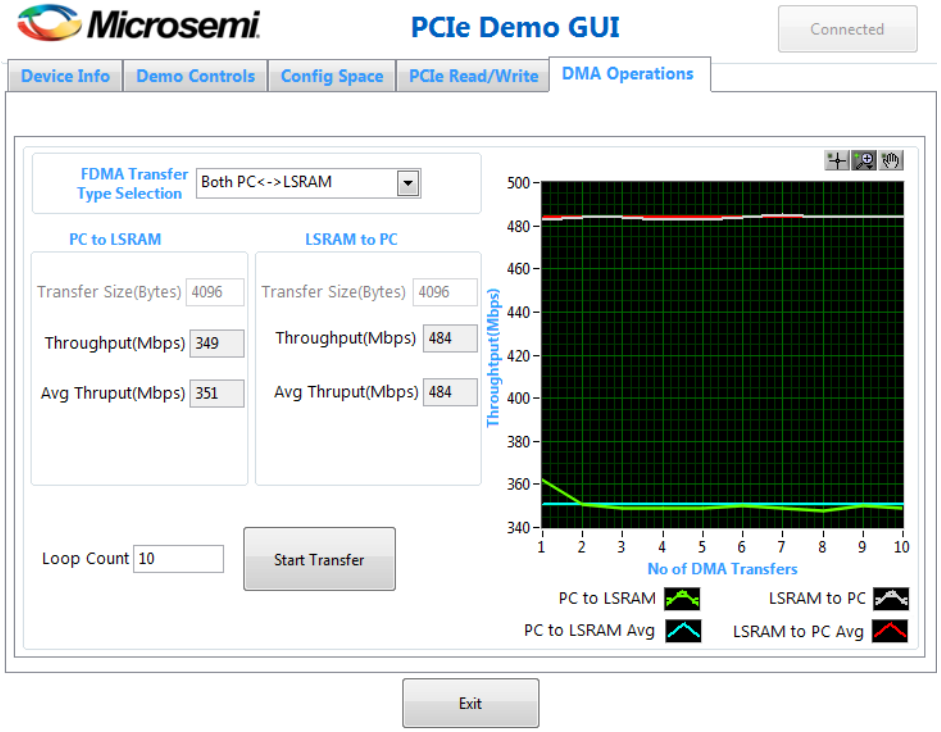


Figure 26 • **Both PC to and from LSRAM – FDMA Transfer Type Selection**



2.6.3 LSRAM and DDR DMA Operations

The following instructions describe the different ways to read data through LSRAM and DDR:

1. Select one of the following options from the **FDMA Transfer Type Selection** drop-down list:
   - **DDR -> LSRAM**—to transfer the data from DDR to SmartFusion2/IGLOO2 LSRAM memory.
   - **LSRAM-> DDR**—to transfer the data from SmartFusion2/IGLOO2 LSRAM memory to DDR.
   - **Both DDR <-->LSRAM**—to transfer the data from DDR to and from SmartFusion2/IGLOO2 LSRAM memory
2. Enter the **Loop Count** in the box.
3. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput in Mbps and average throughput in Mbps, as shown in the following figures.

Figure 27 • **FDMA Transfer Type Selection – DDR to LSRAM**

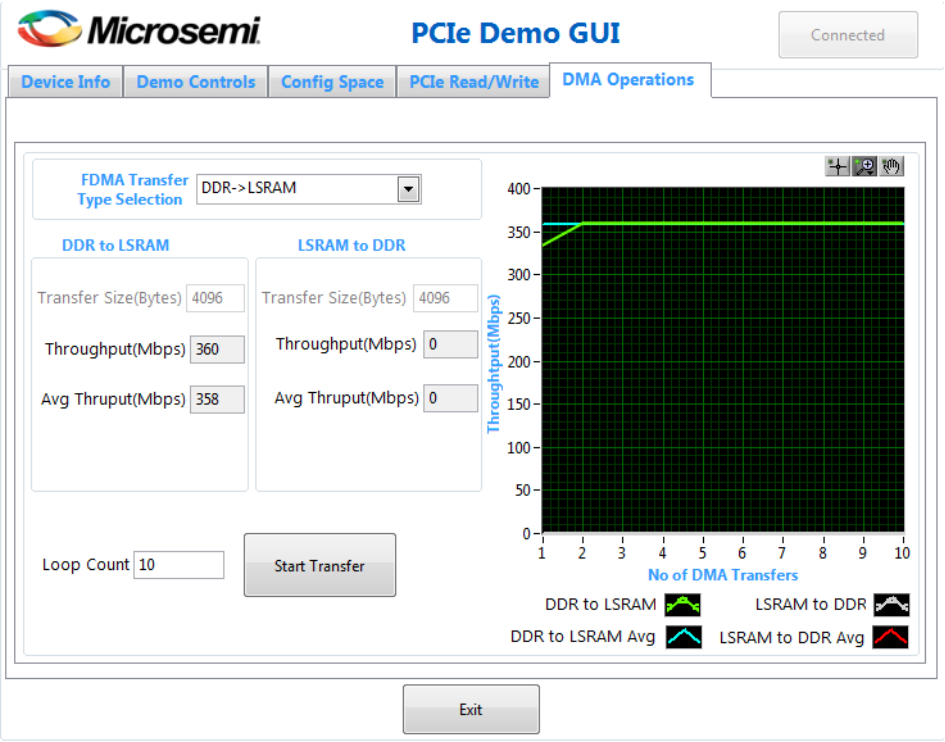


Figure 28 • **FDMA Transfer Type Selection – LSRAM to DDR**

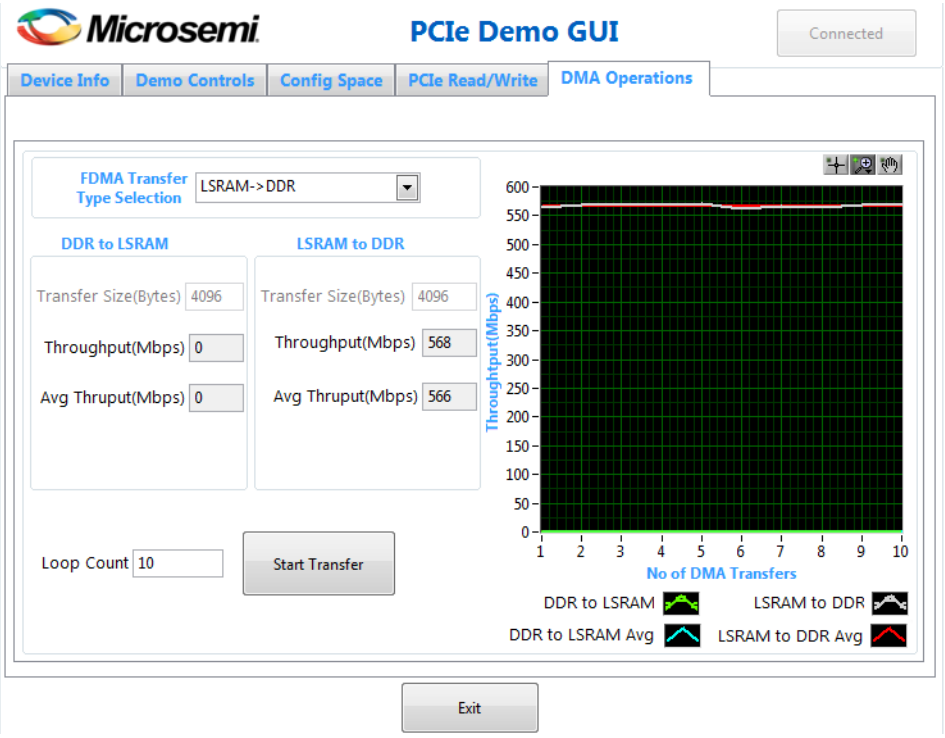
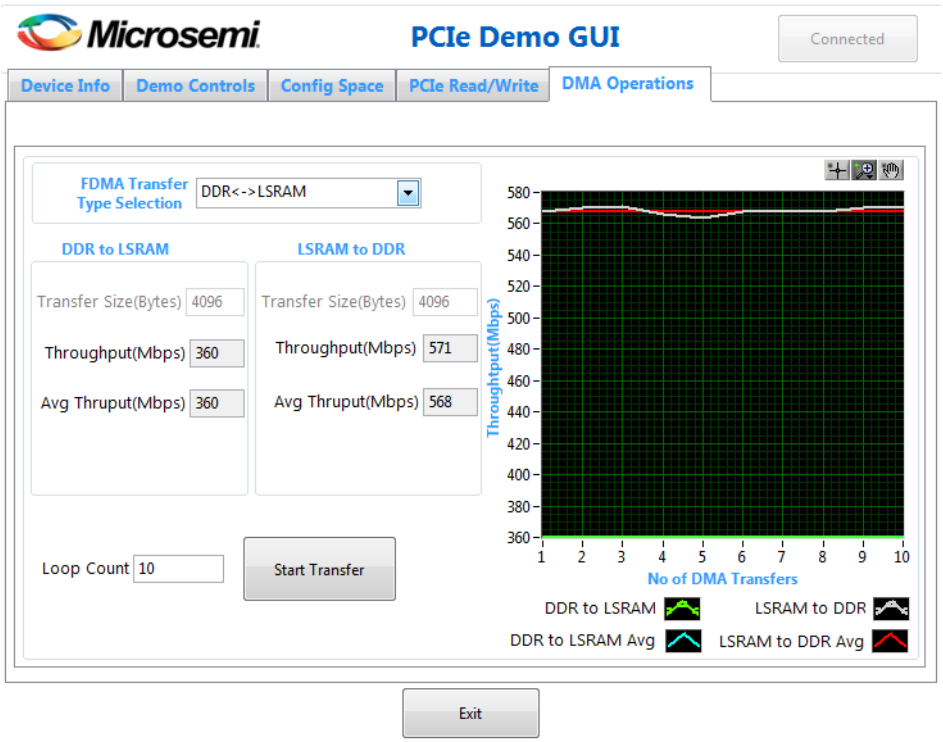


Figure 29 • **FDMA Transfer Type Selection – Both DDR to LSRAM**



4. Click **Exit** to quit the demo.

2.7 Summary

This demo shows how to implement a PCIe data plane design using the AXI-based fabric DMA controller. Throughput for data transfers is dependent on the host PC system configuration and the type of PCIe slots used.

The following table lists the throughput values observed on the HP workstation Z220 PCIe slot 4.

Table 4 • **Throughput Summary**

		Throughput in Mbytes/Sec							
		IGLOO2 (X1 Lane)				SmartFusion2 (X4 Lane)			
		Gen1		Gen2		Gen3		Gen4	
DMA Transfer Type		**Single xfer**	**Loop xfer (50)**	**Single xfer**	**Loop xfer (50)**	**Single xfer**	**Loop xfer (50)**	**Single xfer**	**Loop xfer (50)**
Host PC to LSRAM	Read	168	184	351	352	574	509	710	689
	Write	242	242	478	479	819	820	1096	1096
	R/W	169/241	184/282	353/480	353/478	529/817	508/820	690/1096	691/1096
Host PC to DDR	Read	175	175	284	281	465	456	422	488
	Write	228	226	423	420	577	566	577	574
	R/W	147/199	167/197	188/288	197/308	334/570	323/488	351/510	377/494
DDR to LSRAM	Read	336	332	336	329	606	599	606	592
	Write	530	520	519	521	606	590	606	584
	R/W	336/502	331/519	336/526	332/522	606/606	606/592	606/606	594/587

3 Appendix 1: Programming the Device Using FlashPro Express

This section describes how to program the SmartFusion2 and IGLOO2 devices with the programming job file using FlashPro Express.

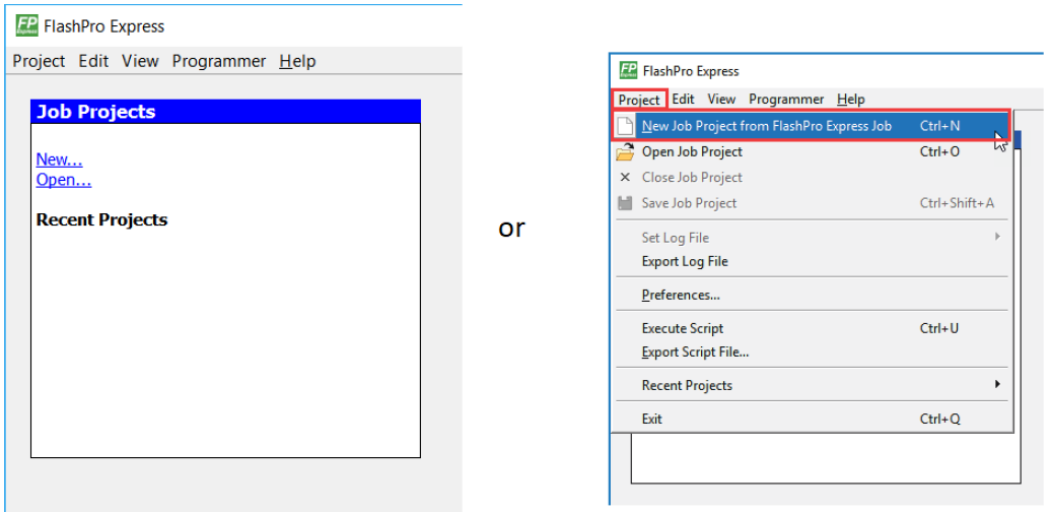
To program the device, perform the following steps:

1. Ensure that the jumper settings on the board are the same as those listed in Table 2, page 8 for IGLOO2 device and Table 3, page 8 for SmartFusion2 device.

Note: The power supply switch must be switched off while making the jumper connections.

2. Connect the power supply cable to the **J6** connector on the board for the IGLOO2 Evaluation Kit board and the J18 connector for the SmartFusion2 Advanced Development Kit board..
3. Power **ON** the power supply switch **SW7**.
4. On the host PC, launch the **FlashPro Express** software.
5. Click **New** or select **New Job Project from FlashPro Express Job** from **Project** menu to create a new job project, as shown in the following figure.

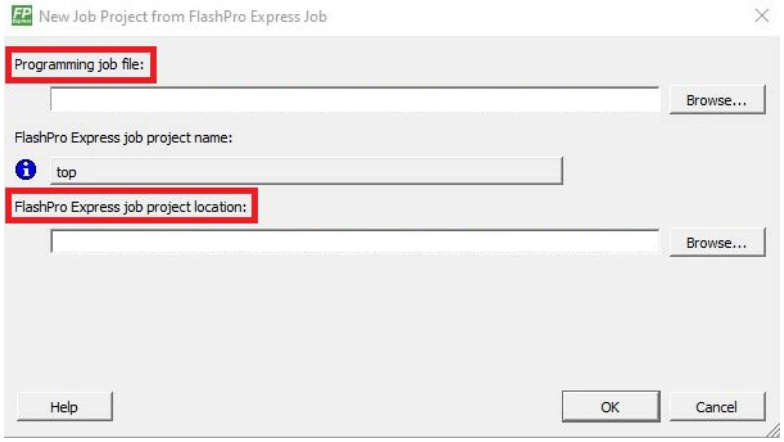
Figure 30 • **FlashPro Express Job Project**



6. Enter the following in the **New Job Project from FlashPro Express Job** dialog box:

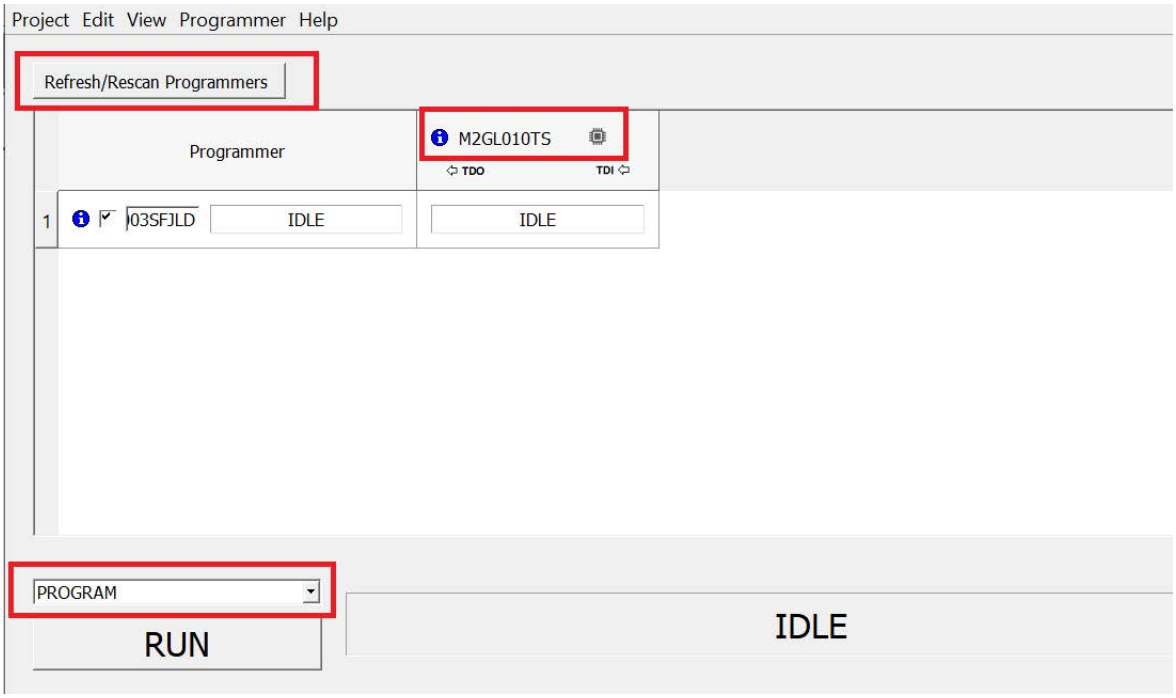
- **Programming job file:** Click **Browse**, and navigate to the location where the .job file is located and select the file. The default location is:
  <download_folder>\m2s_m2gl_dg0517_df\Programming_Job
- **FlashPro Express job project name:** Click **Browse** and navigate to the location where you want to save the project.

Figure 31 • **New Job Project from FlashPro Express Job**



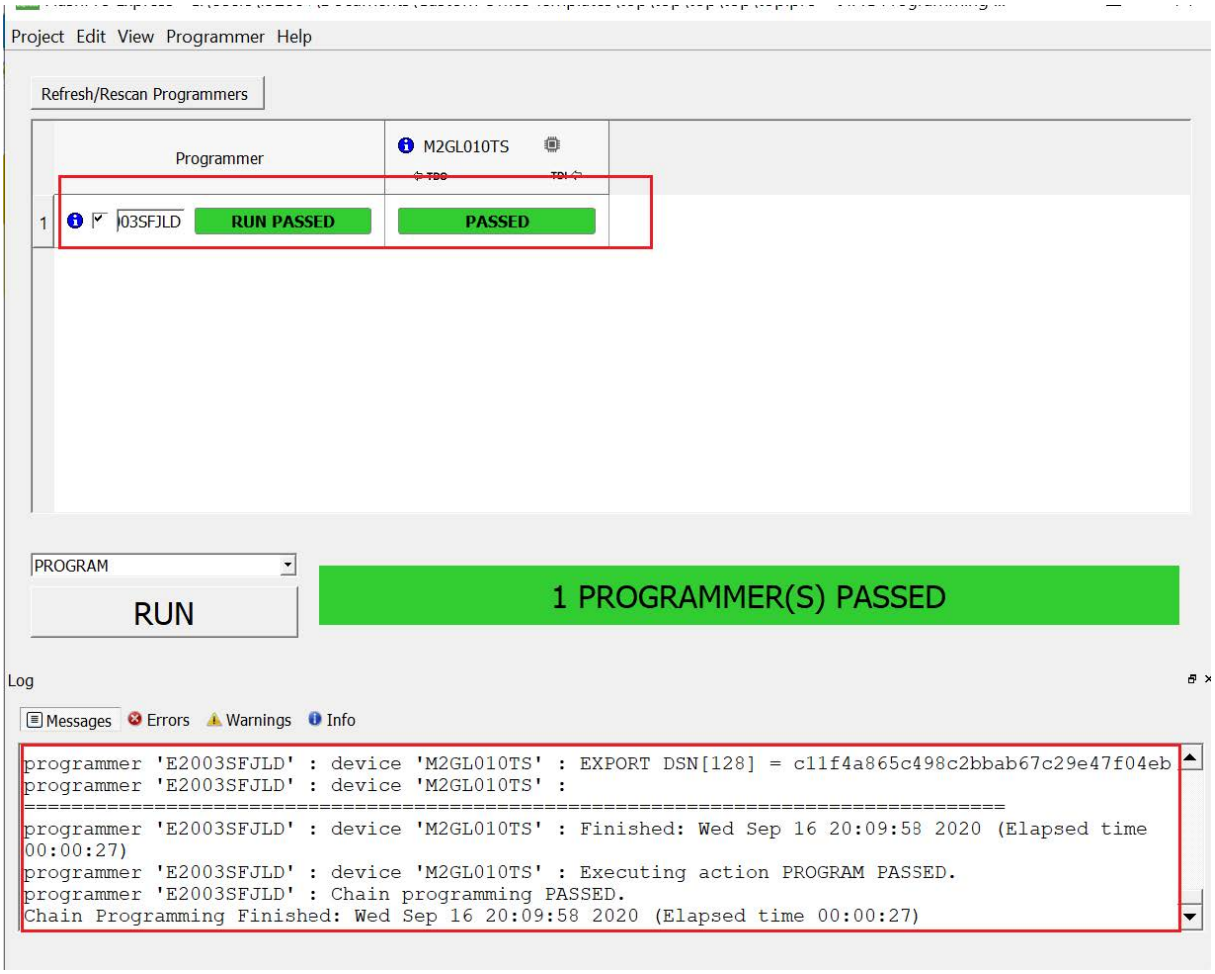
7. Click **OK**. The required programming file is selected and ready to be programmed in the device.
8. The FlashPro Express window appears as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan** Programmers.

Figure 32 • **Programming the Device**



9. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in the following figure.

Figure 33 • **FlashPro Express—RUN PASSED**

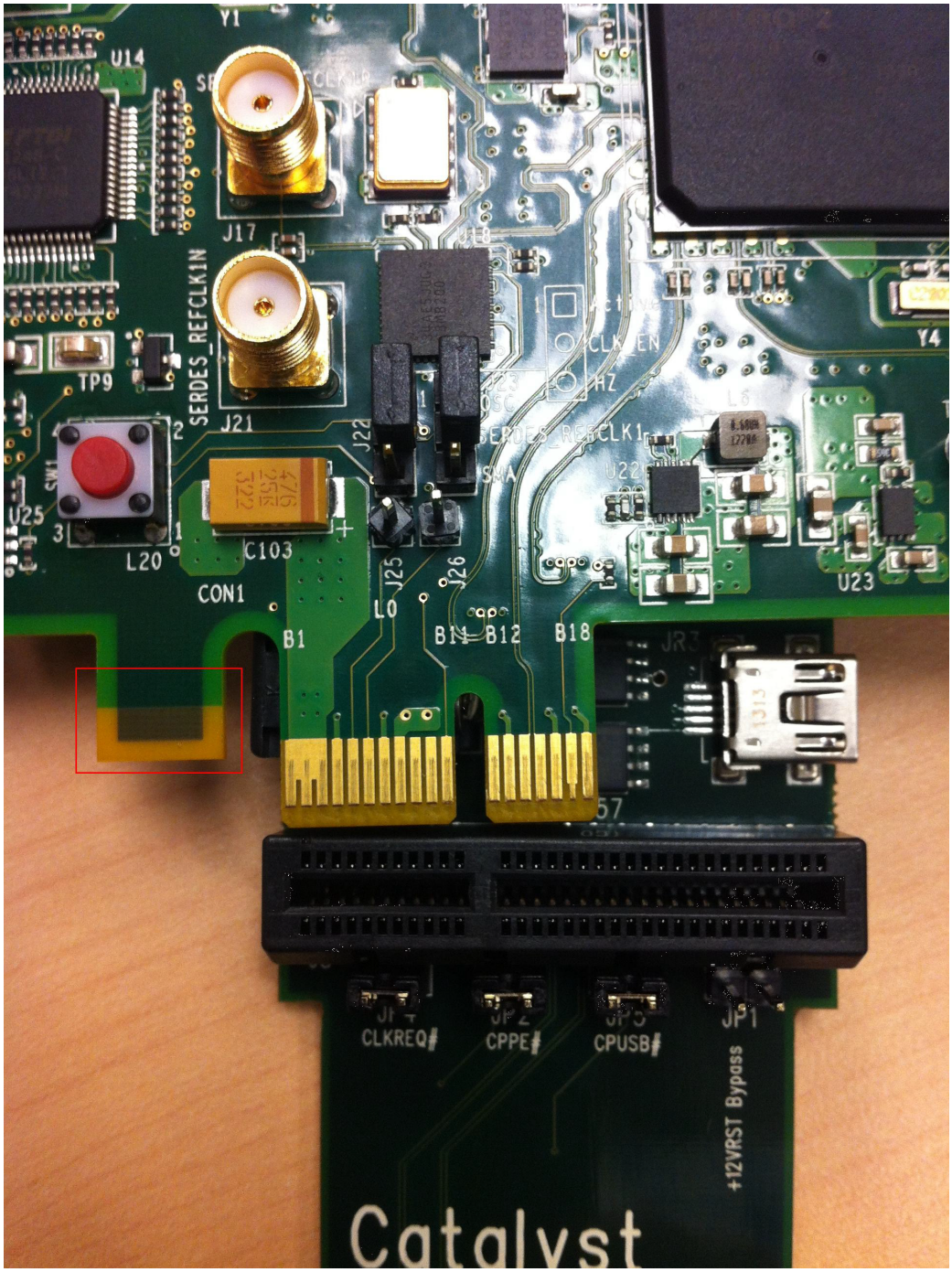


10. Close **FlashPro Express** or in the Project tab, click **Exit**.

4 Appendix 2: IGLOO2 Evaluation Kit Board Setup for Laptop

The following figure shows how to line up the IGLOO2 Evaluation Kit PCIe connector with the adapter card slot.

Figure 34 • **Lining up the IGLOO2 Evaluation Kit Board**



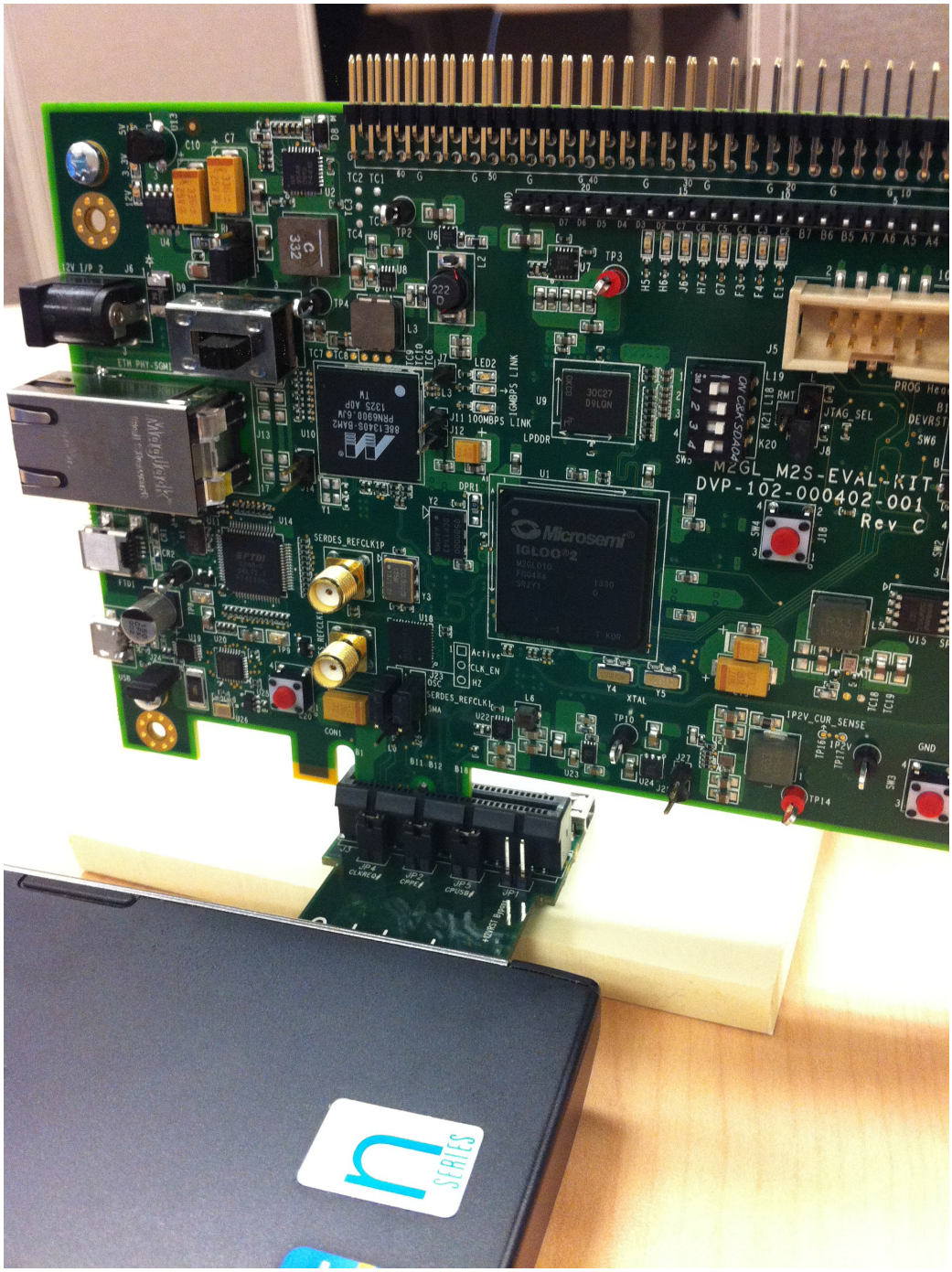
Note: The notch (highlighted in red) does not go into the adapter card.

The following figure shows the IGLOO2 Evaluation Kit PCIe connector inserted into the PCIe adapter card slot.

Figure 35 • **Inserting the IGLOO2 Evaluation Kit PCIe Connector**

The following figure shows the PCIe adapter card and the IGLOO2 Evaluation Kit connected to the laptop.

Figure 36 • **IGLOO2 Evaluation Kit Connected to the Laptop**



5 Appendix 3: Register Details

The following table lists the registers used to interface with the fabric DMA Controller. These registers are in BAR1 address space.

Table 5 • **Register Details**

Register Name	Register Address	Description
PC_BASE_ADDR	0X8028	Host PC memory base address provided by the driver.
DMA_DIR	0X8008	DMA direction: **Direction**.....**Register Value** 1. PCIe → DDR memory.....0 × 11AA0001 2. DDR → PCIe memory.....0 × 11AA0002 3. LSRAM → DDR memory.....0 × 11AA0003 4. DDR → LSRAM memory.....0 × 11AA0004 5. PCIe → LSRAM memory.....0 × 11AA0005 6. LSRAM → PCIe memory.....0 × 11AA0006 To reset the DMA, the register value is 0 × 11AA0007. Before initiating DMA transactions, reset the DMA with the register value, 0X11AA0007. The DMA transactions 1 and 2, 3 and 4, or 5 and 6 can be performed simultaneously by writing the corresponding values one after other.
DMA_CH0_STATUS	0X8100	DMA Channel-0 status DMA_CH0_STATUS[31] 1 = DMA operation completed 0 = DMA operation not completed DMA_CH0_STATUS[15:0] = CLK count
DMA_CH1_STATUS	0X8108	DMA Channel-1 status DMA_CH1_STATUS[31] 1 = DMA operation completed 0 = DMA operation not completed DMA_CH1_STATUS[15:0] = CLK count
RW/REG	0X0	Scratchpad register for PCIe R/W.
LED/CTRL	0XA0	LEDs control register.
SWITCH/STATUS	0X90	DIP switch status.
MEMORY	0X9000	4 k memory to access from BAR1

Note: For the DDR memory, the source memory address is fixed as 0x0100_0000 and the destination memory address is fixed as 0 × 0000_0000.