IGLOO2 High Speed SERDES 3x Oversampling Design

User Guide

Microsemi

Table of Contents

IGLOO2 High Speed SERDES 3x Oversampling Design

Introduction

IGLOO®2 field programmable gate array (FPGA) devices have embedded high speed serial/deserializer (SERDES) blocks that can handle data rates from 1 Gbps to 5 Gbps. Because of internal phase locked loop (PLL) operating range limitations, the lower cutoff data rate of the high speed SERDES block is 1000 Mbps. There are several serial protocols that operate below the 1000 Mbps operating data range. For example, the commonly used IEEE1394 firewire protocol that extends its operating data rate from 400 Mbps to 3.2 Gbps. To support the lower data rates of such protocols, an oversampling technique can be used. In this technique, each data bit is sampled in multiple clock cycles before being transmitted.

Hardware Requirements

The following hardware is required to run this demo:

- M2GL-EVAL-KIT IGLOO2 FPGA Evaluation Kit (1)
- FlashPro4 JTAG Programmer (1)
- USB 2.0 A-male to mini-B for UART (1)
- 12 V 2A wall-mounted power supply (1)
- STAPL/PDB file
  - GUI software

Design Description

This user guide demonstrates transmitting a low speed data rate over the IGLOO2 high speed SERDES interface. The SERDES is configured for 1.179 Gbps operational speed. However, the actual data rate on the wire is 1/3rd of the configured rate, running at 393 Mbps. This is achieved by oversampling each bit 3 times before transmission and correspondingly down-sampling the data by 3x on the receiver side. To the outside world, it appears as if the SERDES is transmitting and receiving speeds at 393 Mbps.

The system block diagram for the design implemented in an IGLOO2 device as shown in Figure 1.

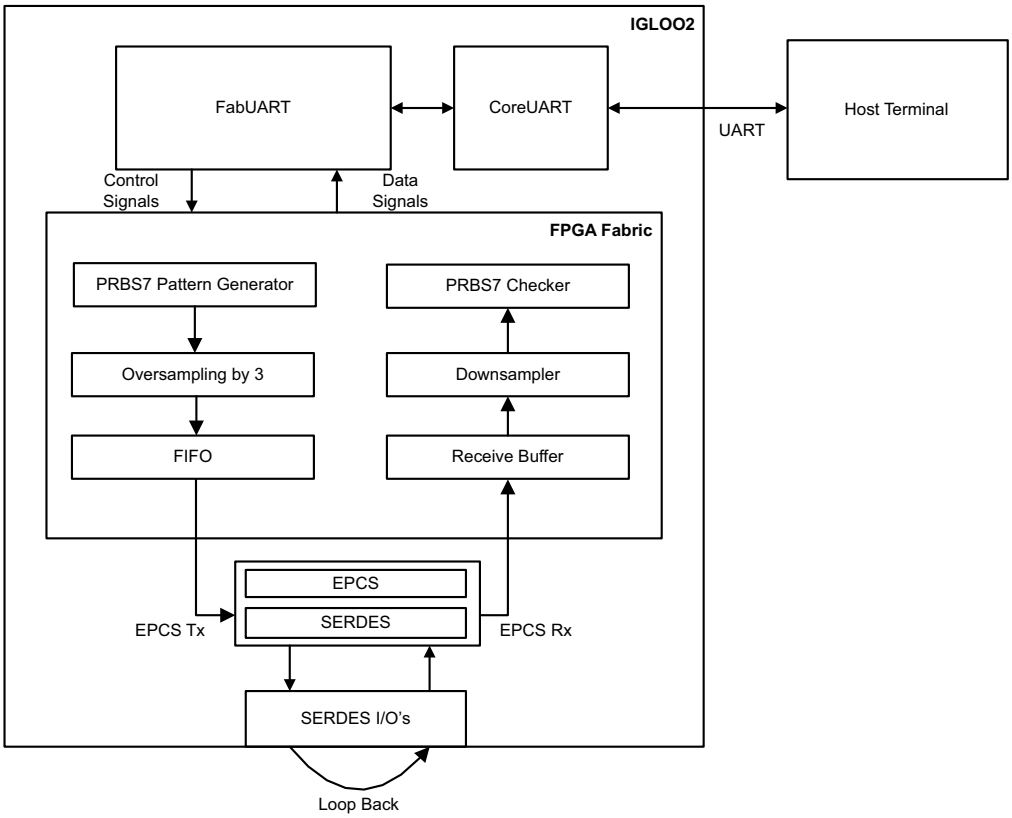

Figure 1 • **Reference Design Block Diagram**

Hardware Design

The hardware design for the implementation includes a pseudo-random bit sequences (PRBS) pattern generator, oversampler, downsampler, PRBS sequence checker, error counter and high speed serial interface block connected to IGLOO2 SERDES. The block diagram for the design is shown in Figure 2.

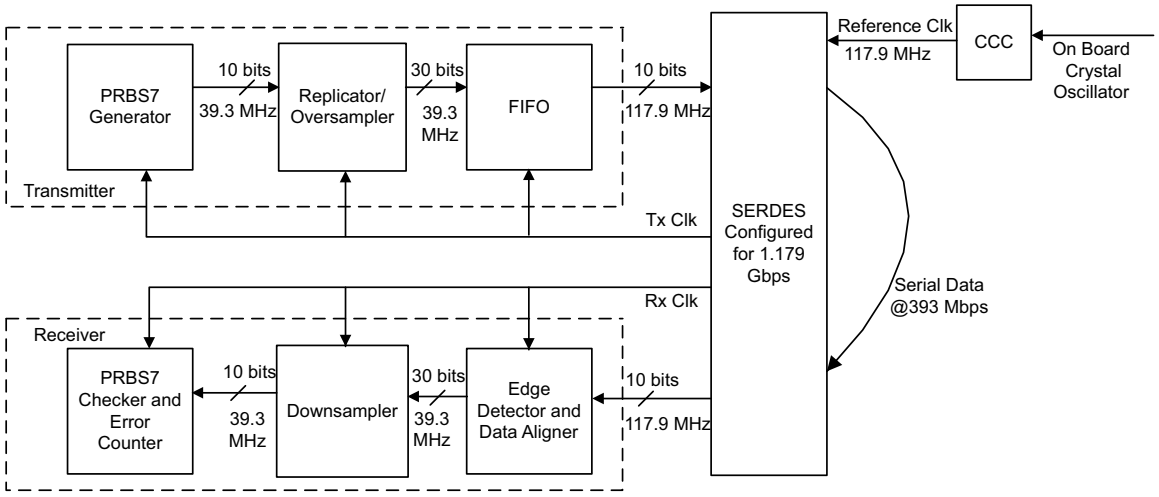

Figure 2 • **Hardware Design Block Diagram**

Block Descriptions

PRBS7 Generator

The generator implements the PRBS7 polynomial (x^7+x^6+1) and generates a continuous sequence of PRBS7 patterns of ten bits each. Each ten-bit transmission from the generator occurs at a frequency of 39.3 MHz.

Replicator/Oversampler

The replicator or oversampler takes the 10-bit input from the PRBS7 generator and replicates each bit into three bits. After bit-replication, the 10-bit input becomes a 30-bit output.

FIFO

The FIFO is used to rate match between 30-bit parallel output of the Replicator/Oversampler running at 39.3 MHz and the 10-bit SERDES input running at 117.9 MHz.

Note: Both 39.3 MHz and 117.9 MHz clocks are derived from the same clock source.

SERDES

IGLOO2 FPGA high speed SERDES is a hard IP block on chip that supports rates up to 5 Gbps. The SERDES block offers embedded protocol support for PCIe, SRIO, XAUI, SGMII etc. The SERDES block also supports external physical coding sub layer (EPCS) interface which can be used for custom protocols. Refer to the *IGLOO2 FPGA Fabric User Guide* for more information on SERDES block.

In this user guide, the SERDESIF_0 block is configured for EPCS mode on Lane1, with 10 bit parallel interface on both transmit and receive side, with reference clock from fabric. The configurator window for SERDES in SmartDesign is shown in Figure 3.

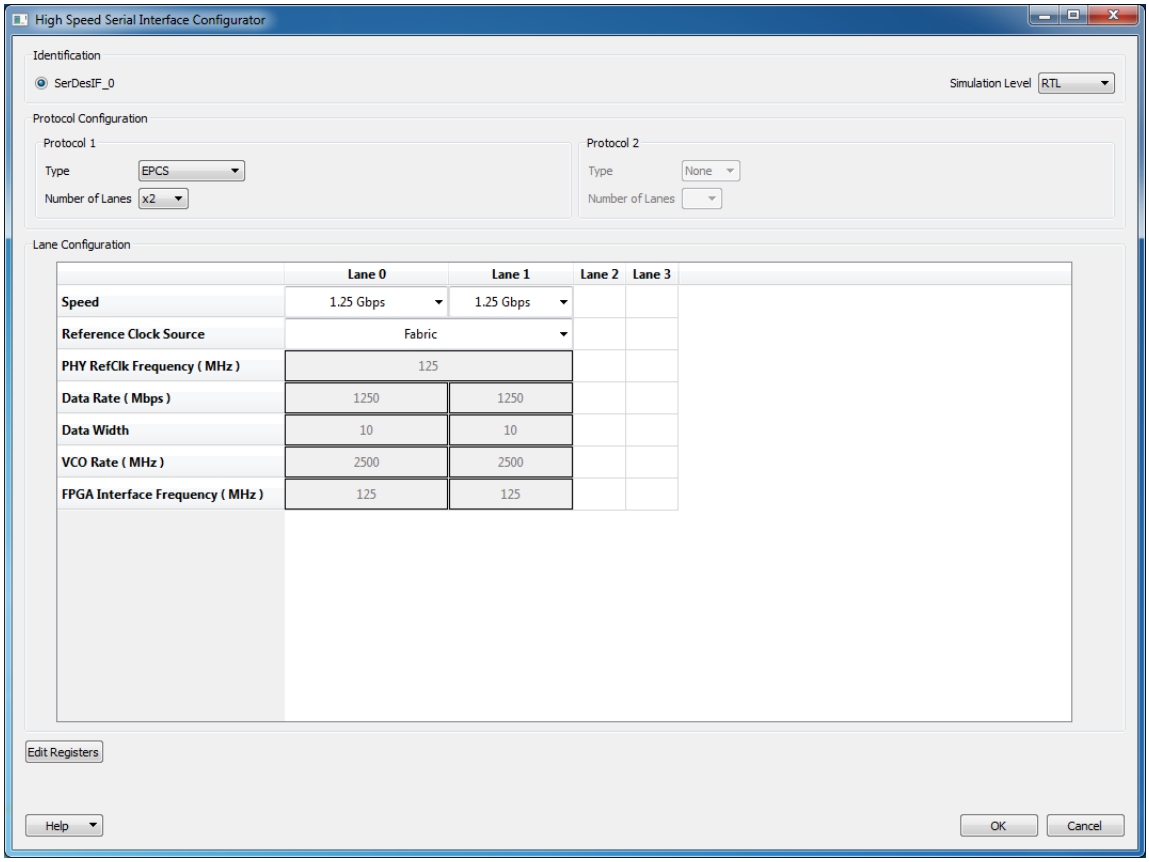

Figure 3 • **SERDES Configurator Window**

Table 1 shows the default values for SERDESIF macro registers.

Table 1• **SERDES Macro Register Values**

Offset (Hex)	Register Name	Register Value in Reference Design
0x010	PLL_F_PCLK_RATIO	0x00
0x014	PLL_M_N	0x49

SERDES Reference CLK = 117.90 MHz

VCO Frequency = 4716 MHz

Edge Detector and Data Aligner

This module is implemented using a barrel shifter that takes sequential 10-bit output of the receive side of SERDES and bit aligns to a known sequence and/or pattern. The design looks for bit transitions and checks for contiguous patterns of three 1's or three 0's.

Note: 3x oversample design, bit patterns of three 1's and three 0's are known to occur as each sample of 1 and 0 is oversampled thrice on the transmit-side before transmission. Once the alignment lock is achieved, the data is grouped into 30-bit of sequential received data and the 30-bit output is presented to the next module.

Downsampler

The downsampler takes the 30-bit data from the aligner and reverses the function of the replicator (in the transmit section) to produce the original 10-bit PRBS7 sequence. There is a first level of error check in this module where if the bits coming in are not replicated 3 times, the received packet is considered as corrupted and discarded, and the error count is incremented.

PRBS7 Checker

PRBS7 checker checks for valid PRBS sequences. If the received sequence does not match the one transmitted by the generator, the checker indicates an error. The checker also implements an error counter that is incremented for each error in the received PRBS sequence.

Clock Conditioning Circuitry (CCC)

CCC provides reference clock needed for SERDES operation. Refer to the *IGLOO2 FPGA Fabric User Guide* for more information on CCC blocks. In this user guide, the CCC is configured as shown in Figure 4 on page 7.

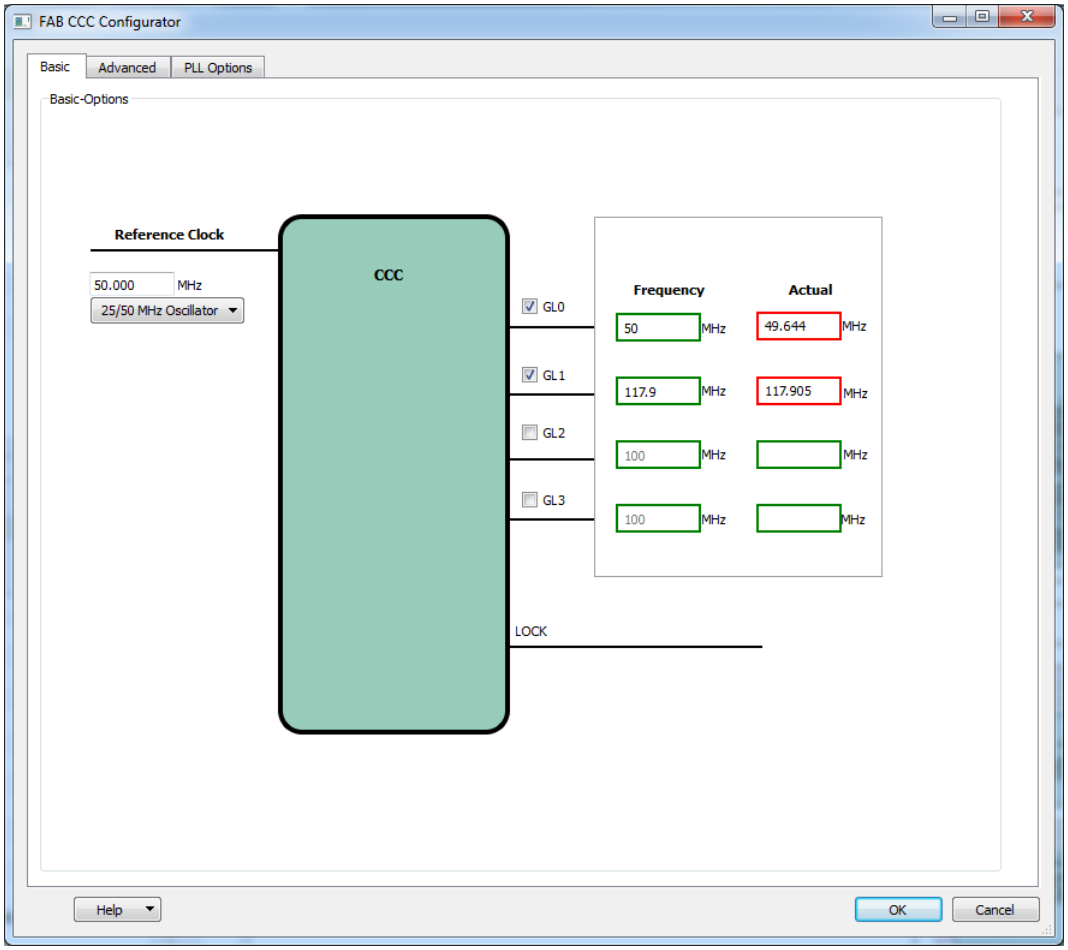

Figure 4 • **CCC Configuration Window**

Design Files Directory Structure

Download the design files from *http://soc.microsemi.com/download/rsc/?f=IGLOO2_3xOversampling*.

Figure 5 shows the design files directory structure.

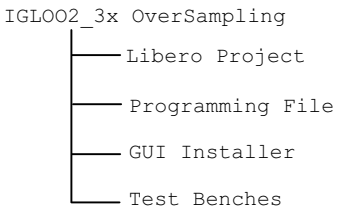

Figure 5 • **Design Files Directory Structure**

Setting Up the Design

Use the following steps to set up the design:

1. Connect the **FlashPro4** programmer to the programming header J5.
2. Connect one end of the USB 2.0 Mini-B to the USB Mini connector marked J18 on the board.
3. Connect the other end of the USB 2.0 A-male connector to the host PC or laptop.
4. Connect 12 V 2 A-power jack to the board J6 power connector.
5. Install USB to UART drivers on the host PC. Make sure that the **USB to UART bridge drivers** are automatically detected. Download and install the drivers from www.*microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip.*
6. Connect the jumpers on the board, as listed in Table 2. For more information on jumper locations, refer to "Appendix 1: Jumper Locations" on page 19.
   – **Caution:** Before making the jumper connections, turn off the power supply switch.

Table 2 • **Jumper Settings**

Jumper Number	Settings	Notes
J22	1-2 Closed	Line side output enabled
J23	1-2 Closed	On board 125 MHz differential. Clock oscillator output will be routed to line side.
J3	1-2 Closed	Manual power switching using SW7 switch.
J8	1-2 Closed	FlashPro4 for Soft Console/FlashPro

7. Connect the power supply to the J18 DC jack.

8. Figure 6 shows the IGLOO2 Evaluation board.

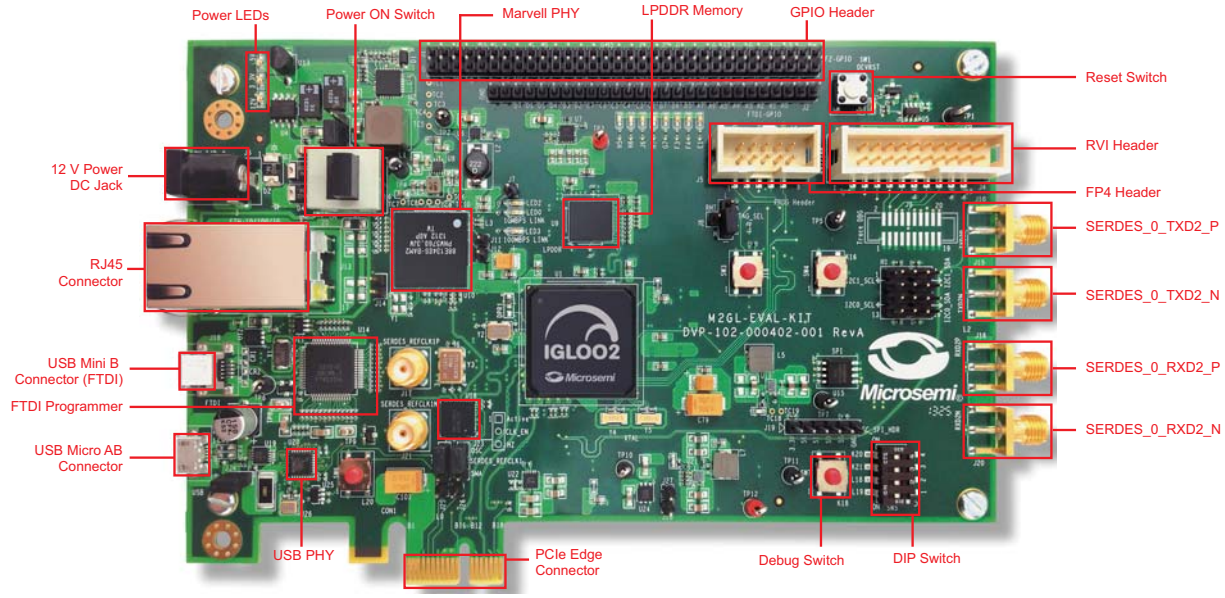

Figure 6 • **IGLOO2 Evaluation Kit**

Note: The design uses SERDES LANE 1 which is looped back from Transmit to receive on the board. Hence, it is not required to connect external SMA Loopback cables for this design to work.

Running the Device

Use the following steps to start programming the device:

1. Download the design files to *<download_folder>\IGLOO2_3xOversampling*. Programming file (STAPL/PDB) is located in the **Programming File** folder.
2. Turn on the power supply switch.
3. Run the Flashpro4 v11.3 (installed as part of Libero IDE).
4. Click **New Project**.

5. In the **New Project** window, type the project name as **OverSampling_Demo**.

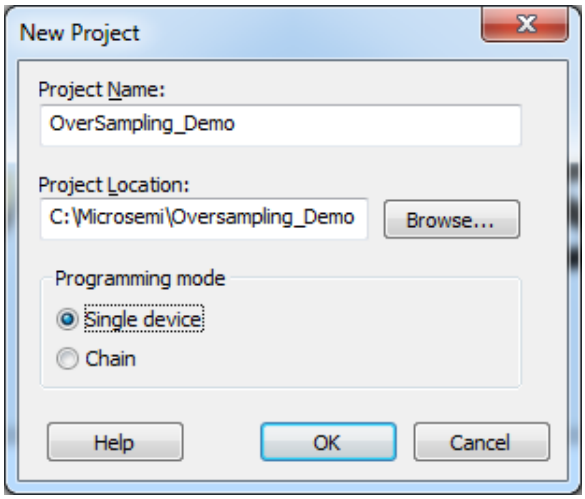

Figure 7 • **New Project Window**

6. If necessary, change the default location of project in the **Project Location** field.
7. Select the **Programming mode** as **Single Device**.
8. Click **OK** to save the project.
9. The FlashPro GUI is displayed as shown in Figure 8. The Programmer List Window updates the programmer information.

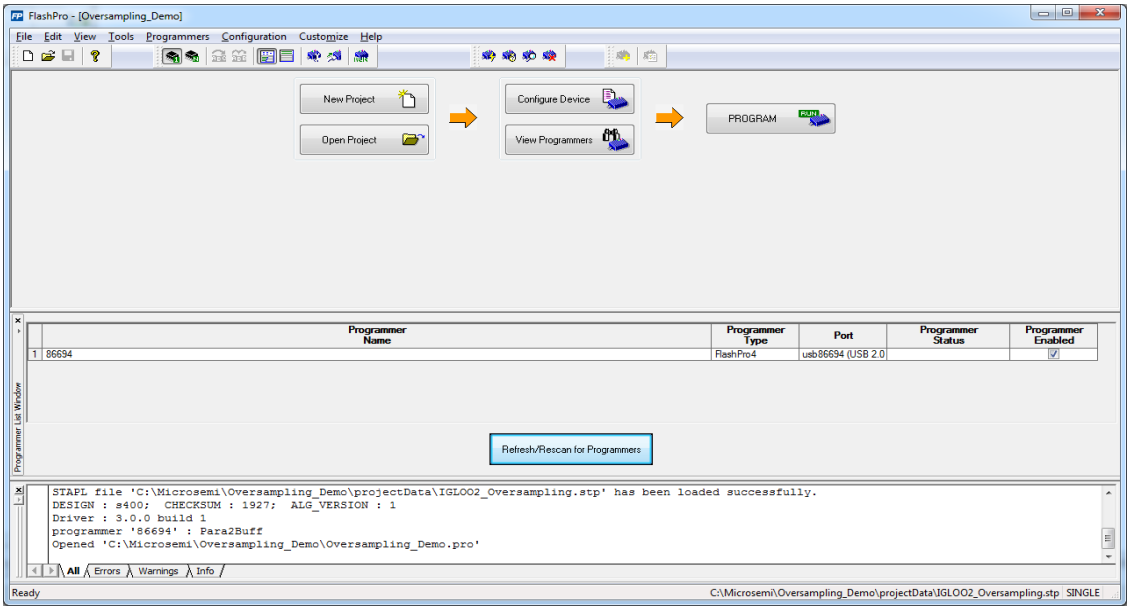

Figure 8 • **Flash pro GUI Window**

10. Once the project is created and connected the programmer, you can load the STAPL/PDB file downloaded in Step 1.

Configuring the Device

Use the following steps to configure the device:

1. Click **Configure Device**. The **Single Device Configuration** window is displayed as shown in Figure 9.
2. Click **Browse** and navigate to the location where the IGLOO2_Oversampling.stp file is located and select the file. The default location is: *<download_folder>\IGLOO2_3xOversampling\Programming File*
3. Click **Open**. The required programming file is selected and is ready to be programmed in the device.
4. The **Single Device Configuration** Window updates to list your **Programming file** information and the actions available with your Programming file in the **Action list box** as shown in Figure 9. **Program** is the default action displayed in the Action list box.

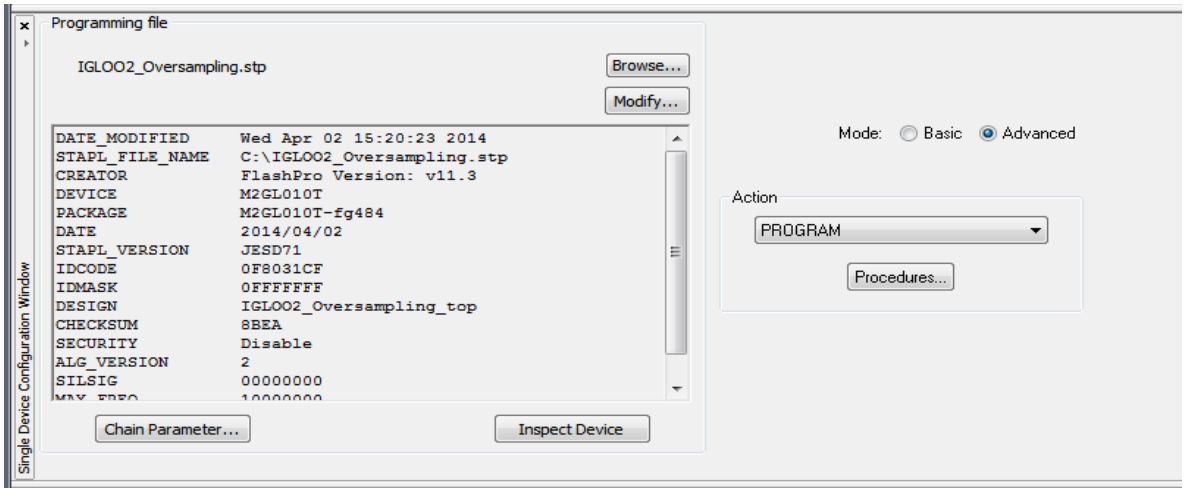

Figure 9 • **Single Device Configuration**

Note: Microsemi recommends the use of default settings.

Programming the Device

Use the following steps to start programming the device:

1. Click **Program** to start programming the device.
2. Click **Procedures** as shown in Figure 10.

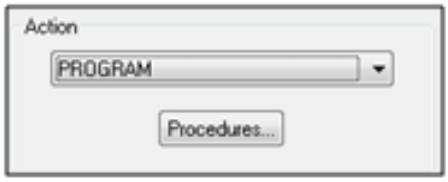

Figure 10 • **Action List Window**

3. The **Select Action and Procedures** window appears, showing the procedures for the Programming action as shown in Figure 11. Microsemi recommends using the default settings. Click the **Restore Default Procedures**.

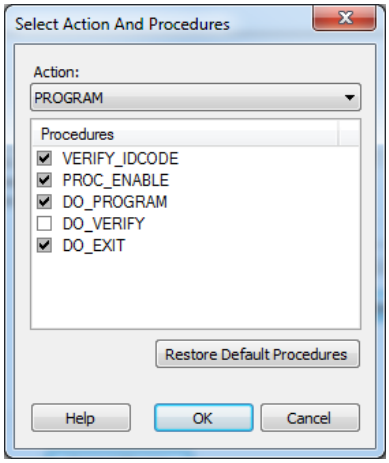

Figure 11 • **Select Action and Procedures**

4. In FlashPro, click **Program** to program your device.
   The Programmer List Window updates the Programmer Status column with **Run Passed** indicating that you have successfully programmed the device.

Note: The status indicator updates during programming to show the programming progress, then it changes to a pass or fail result when the operation is complete.

5. View the **Log window** and take note of the details about your programmed device.
6. Power Cycle the board.

Installing the GUI

To install the GUI, run the following steps:

1. Browse for GUI Installer folder in <download_folder>/IGLOO2_3xOversampling.
2. Open GUI **Installer->Volume->setup**.exe
3. Click **Yes** for any message from **User Account Control**.

4. Setup window appears as shown in Figure 12. Default locations are displayed. Click **Next**.

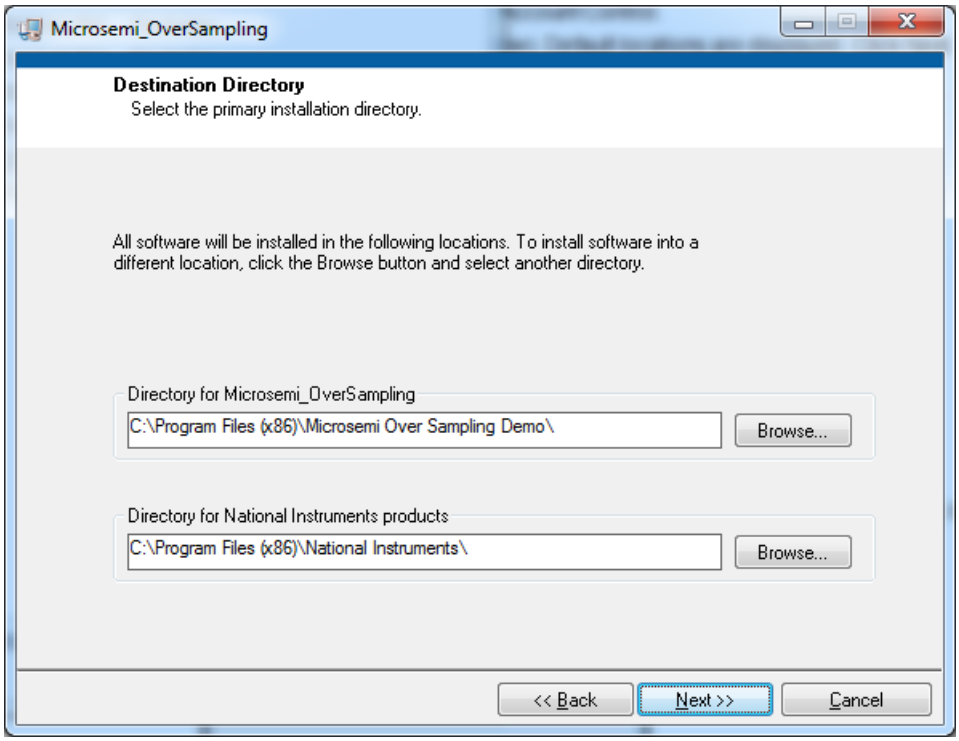

Figure 12 • **GUI Setup Window**

5. A progress bar appears is displayed that shows the progress of installation as shown in Figure 13. Wait until you get a message **Installation Complete**. It may take few minutes.

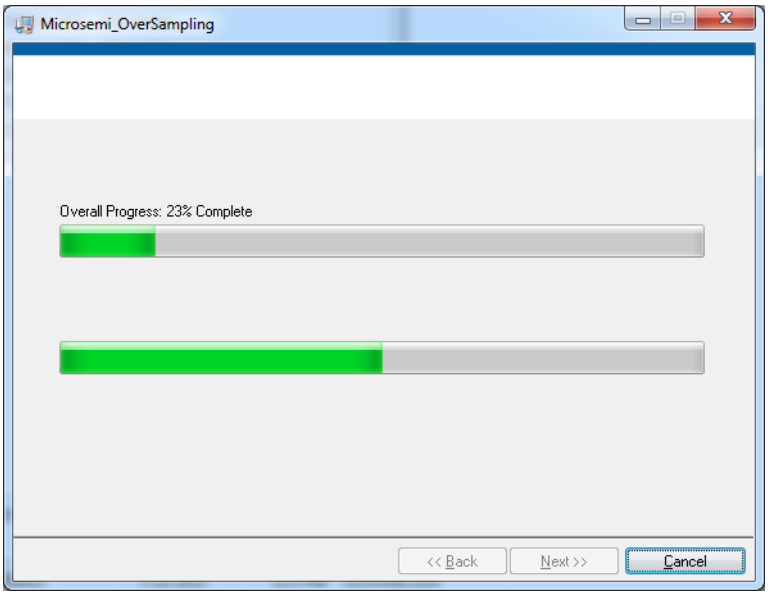

Figure 13 • **GUI Setup Progress Bar**

6. Click **Finish**.

7. Restart your computer before you start using the installed GUI.

Running the Design

1. Open **Programs>Microsemi_OverSamplingDemo.**
2. The GUI window is displayed as shown in Figure 14.

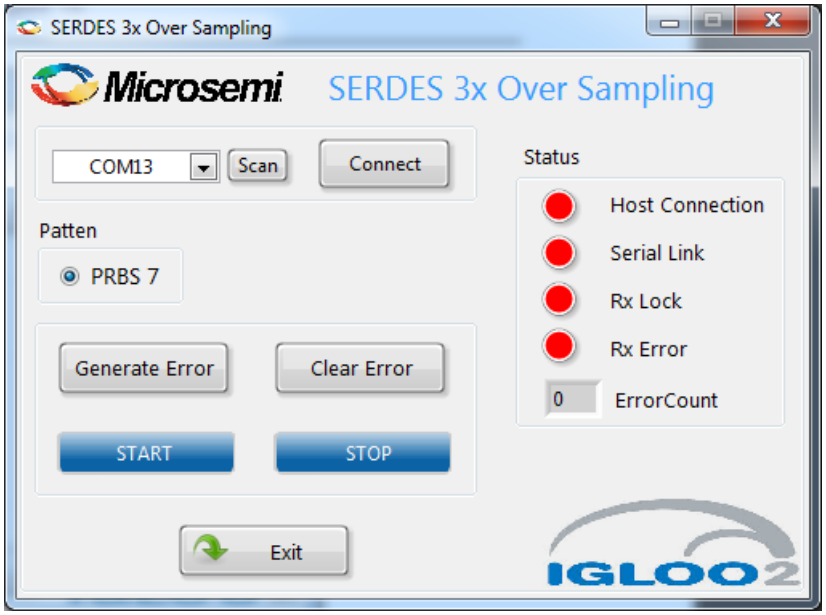

Figure 14 • **Oversampling GUI Window**

All the available serial ports on the host PC are listed in the drop-down menu. Only the working ports are enabled. The ports that are not available are grayed out.

Note: Default settings for the design are 9600 Baud, no flow control, one stop and no parity.

3. Click **Scan** to refresh the list of ports available. If ports are not available, a message is displayed to reset the connection, as shown in Figure 15.

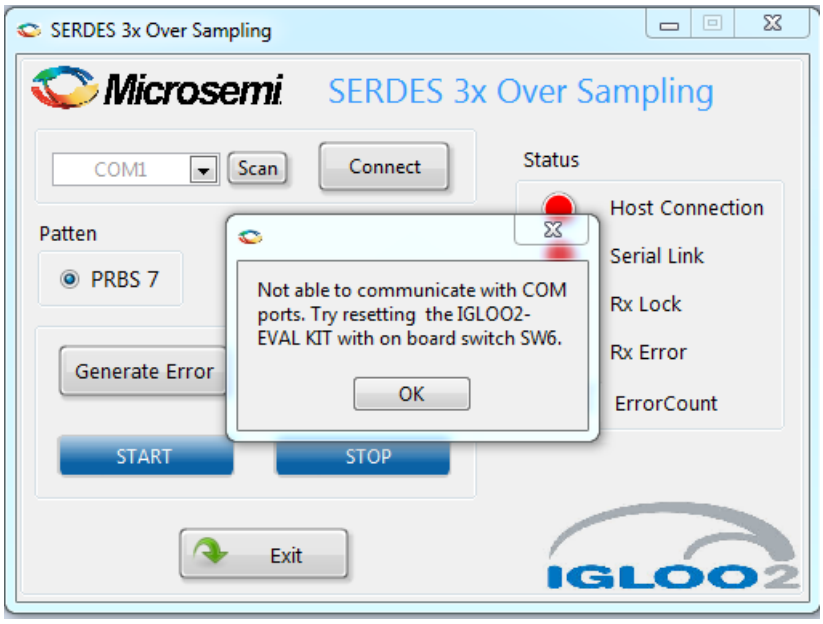

Figure 15 • **Oversampling Window - No Ports Available**

4. Click **Connect** to connect the host PC to the hardware through the selected port. After the host PC is connected, the Oversampling window is displayed as shown in Figure 16.

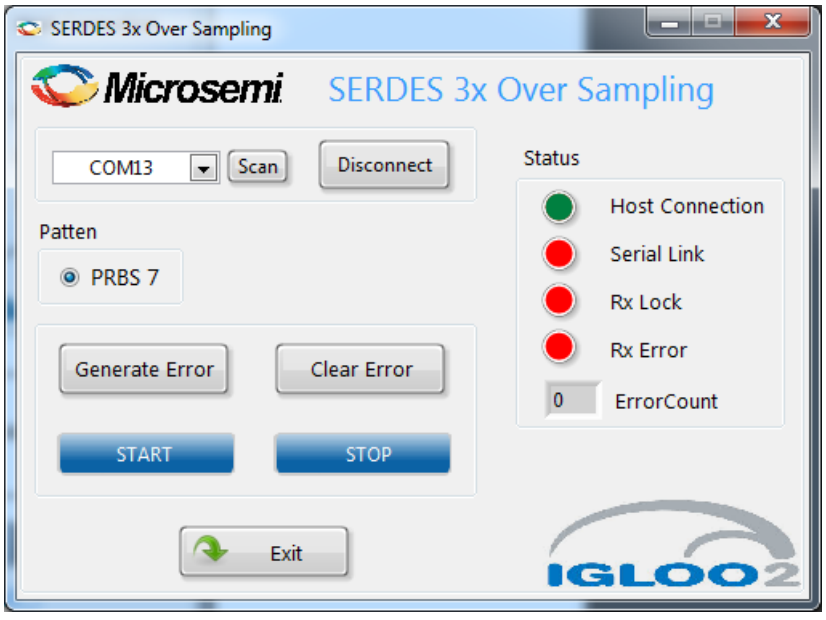

Figure 16 • **Connected Oversampling Window**

5. Click **Start** to start the SERDES 3x Oversampling demo. The PRBS7 data is generated and transmitted over the serial transmit link. The receiver receives the data through the serial receive link and checks for any errors. The status at any time can be monitored using the status signals in the window. For more information on the status signals, refer to the "Appendix 2: Status Signals" on page 20.
6. Click **Stop** to stop the SERDES 3x Oversampling demo.
7. Click **Exit** to exit the window.
8. Figure 17 shows a sample window during an error free operation of the SERDES 3x Oversampling demo.

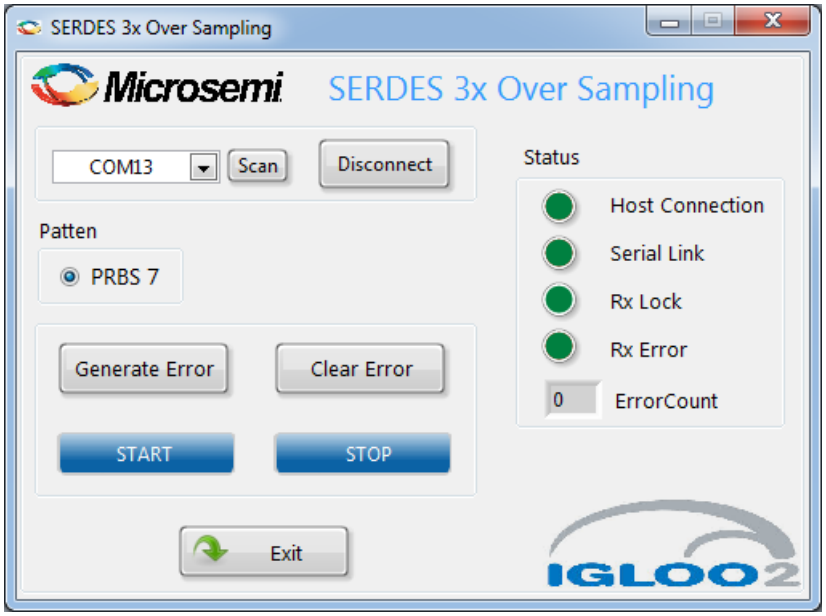

Figure 17 • **Sample Window**

Simulating Design Using Test bench

The simulation for this design is done through testbench. It simulates the SERDES block in the Over sampling mode. To run the simulation, double-click **Simulate** under Verify
Pre-Synthesized Design in the Design Flow window of the Libero project, as shown in Figure 18.

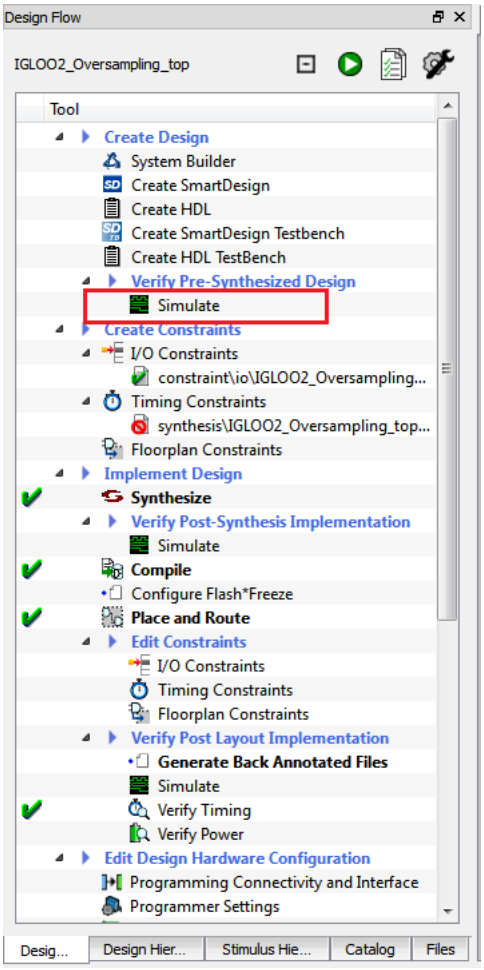

Figure 18 • **Simulating the Design**

After the simulation, the Simulation Waveform window is displayed as shown in Figure 19.

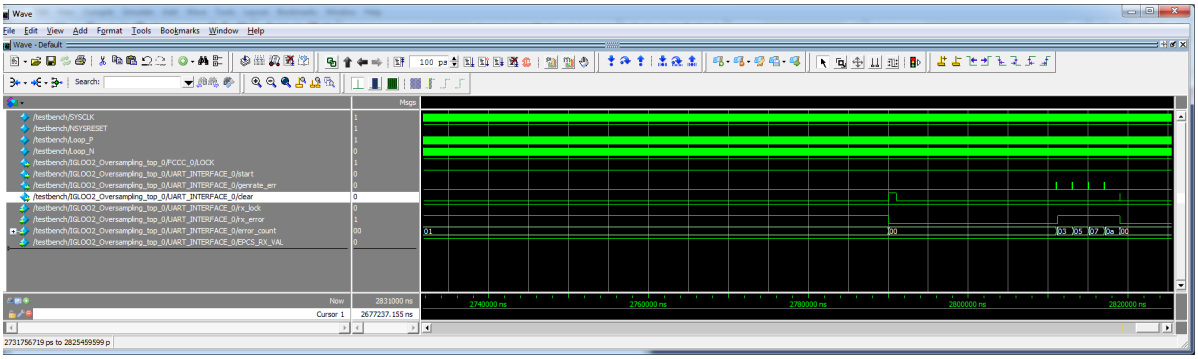

Figure 19 • **Simulation Waveform Window**

Reference Design Features

Replacing PRBS7 Modules with Customer Design

Transmitter Section

The PRBS7 generator in the transmitter section can be replaced with your data generator. The data generator is interfaced with the replicator for oversampling as shown in Figure 20.

Receiver Section

The PRBS7 checker in the receiver section can be replaced with the data receiver in your design. The data receiver takes input from the downsampler as shown in Figure 20.

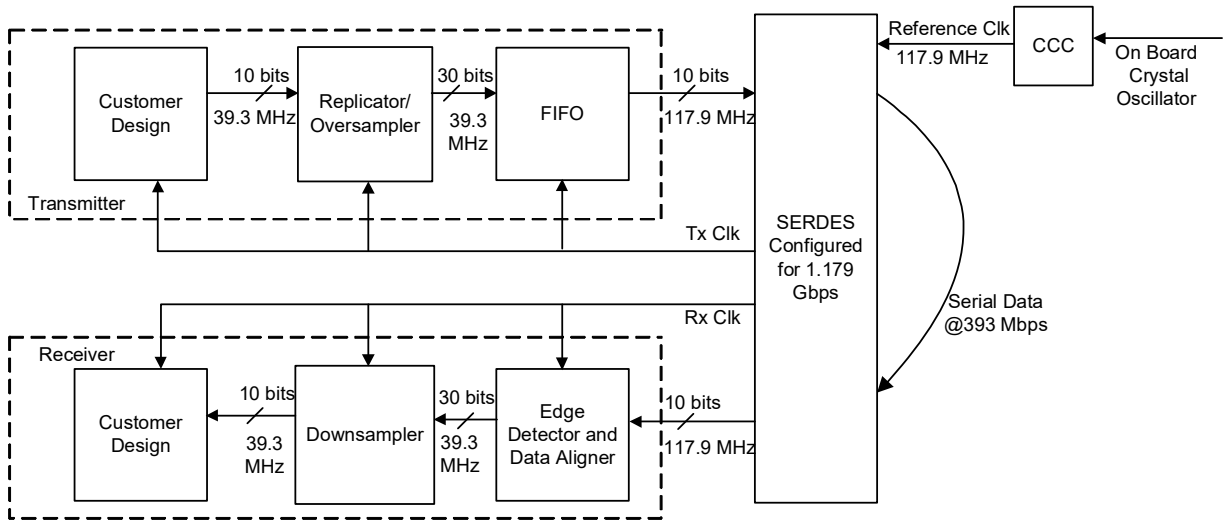

Figure 20 • **Reference Design for Custom Oversampling Application on IGLOO2**

Guidelines for Libero Design Flow

1. Create the design using Smart Design in Libero v11.3.
2. Go through the synthesis and check for any warnings.
3. Program the Device.
4. Run the design.

Appendix 1: Jumper Locations

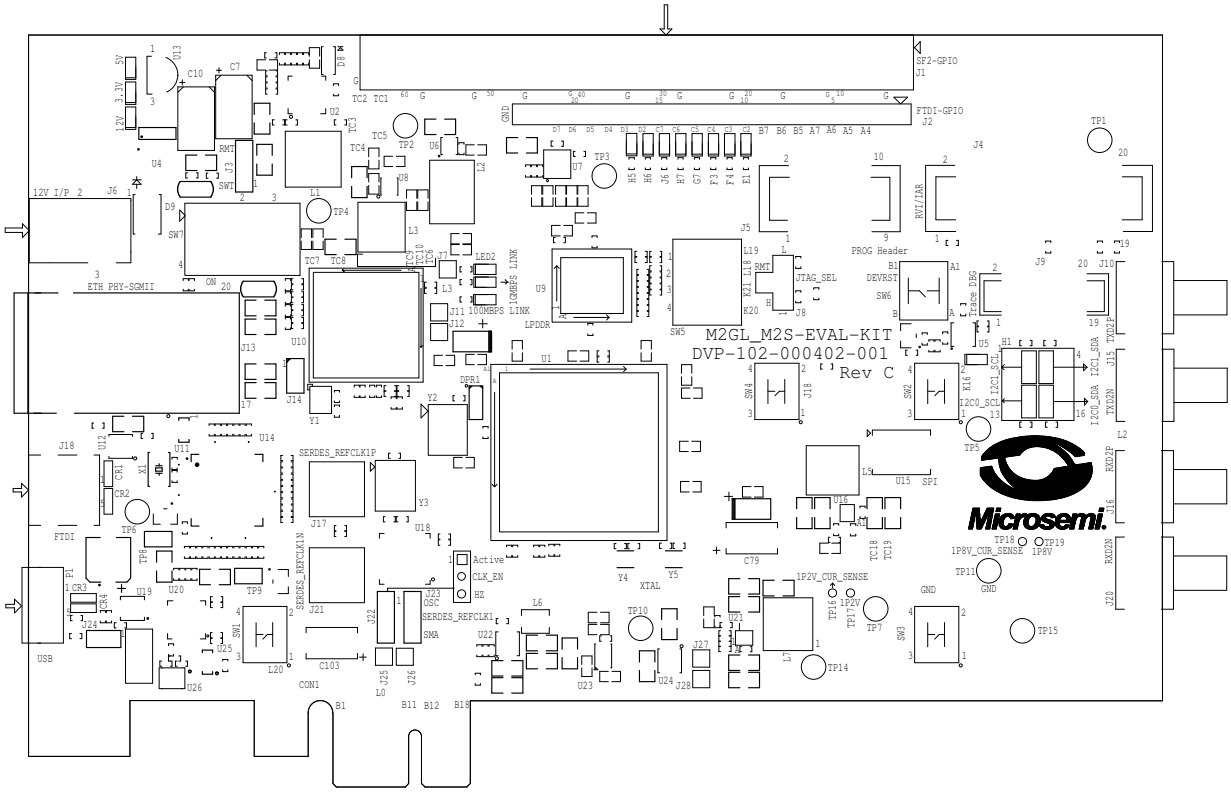

Figure 21 • **IGLOO2 Evaluation Kit Silkscreen Top View**

Figure 21 shows the jumper locations in the IGLOO2 Evaluation Kit.

Appendix 2: Status Signals

Table 3 describes the various status signals.

Table 3 • **Status Signals**

Status Signals	Description
Host Connection	Indicates COM port connection on the host PC. GREEN: COM port is connected. RED: COM port is disconnected.
Serial Link	Indicator of transmission link for serial data. GREEN: Link is up and running. RED: Link is down.
Rx Lock	Receiver lock. GREEN: The receiver is receiving valid and error-free data. It means that the receiver is locked to the PRBS7 sequences and the subsequent transmitted sequences can successfully be received. RED: The receiver is receiving invalid data.
Rx Error	Indicates the status of the packets received. GREEN: Received packets are error-free. RED: A corrupted packet or any error is detected in the received PRBS7 sequences.
Error Count	Count of errors detected in the received PRBS sequences.
Generate Error	Used to introduce errors in the transmission for debug purposes. Injects the error in the transmitted PRBS sequence, which as a result, increments the Error Count display.
Clear Error	Sets error count to zero.

A – List of Changes

The following table lists critical changes that were made in each revision of the chapter in the demo guide.

Date	Changes	Page
Revision 3 (June 2020)	Updated "Design Files Directory Structure" section (SAR 113238).	8
Revision 2 (April 2014)	Updated the document for Libero v11.3 software release (SAR 56875).	NA
	Updated "Running the Design" section (SAR 56875).	14
Revision 1 (December 2013)	Initial Release	NA

B – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.

50200518-3/06-20