DG0438
Demo Guide
SmartFusion2 SoC FPGA DSP FIR Filter

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 7.0

The following is a summary of the changes made in this revision.

- Updated the document for Libero SoC v2021.1.
- Removed the references to Libero version numbers.

1.2 Revision 6.0

Updated the document for Libero v11.7 software release (SAR 78581).

1.3 Revision 5.0

Updated the document for Libero v11.6 software release (SAR 71411).

1.4 Revision 4.0

Updated the document for Libero v11.5 software release (SAR 63931).

1.5 Revision 3.0

Updated the document for Libero v11.4 software release (SAR 60160).

1.6 Revision 2.0

The following are the changes made in revision 2.0 of this document.

- Updated the document for Libero v11.3 software release (SAR 58923).
- Updated the Demo Design, page 4 (SAR 58923).
- Updated the Setting Up the Demo Design, page 8 (SAR 58923).

1.7 Revision 1.0

Updated the document for Libero v11.2 software release (SAR 52985).

1.8 Revision 0.0

Initial release.

2 Preface

2.1 Purpose

This demo is for SmartFusion$^®$2 System-on-Chip (SoC) Field Programmable Gate Array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

2.2 Intended Audience

This demo guide is intended for:

- FPGA designers
- Embedded designers
- System-level designers

2.3 References

The following documents are referred in this demo guide:

- *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*
- *SmartFusion2 System Builder User Guide*
- *SmartFusion2/IGLOO2 Digital Signal Processing Reference Guide*

Refer to the following web page for a complete and up-to-date listing of SmartFusion2 device documentation: http://www.microsemi.com/products/fpga-soc/soc-fpga/sf2docs.

3   SmartFusion2 SoC FPGA - DSP FIR Filter Demo

3.1   Introduction

The SmartFusion2 FPGA devices integrate a fourth generation flash-based FPGA fabric and an ARM®
Cortex®-M3 processor, which includes embedded math blocks are optimized specifically for Digital
Signal Processing (DSP) applications such as, Finite Impulse Response (FIR) filters, Infinite Impulse
Response (IIR) filters, and Fast Fourier Transform (FFT) functions.

This demo shows a DSP FIR filter application using the SmartFusion2 device. In this DSP FIR filter
application, the FIR filter is implemented in fabric for Low pass, High pass, Band pass, and Band reject
filtering operations. The host interface is implemented in the microcontroller subsystem (MSS) to
communicate with the host PC. A user friendly Graphical User Interface (GUI) generates the filter
coefficients, input signals (Pass-band frequency + Stop-band frequency) and also plots the input/output
waveforms and the required spectrum. Microsemi CoreFIR filter IP is used to suppress the unwanted
frequency components, and CoreFFT IP is used to generate the output spectrum to verify the filtering
operation.

Figure 1 shows the top-level diagram for DSP FIR filter demo.

Figure 1 •   **Top-Level Diagram of DSP FIR Filter Demo**
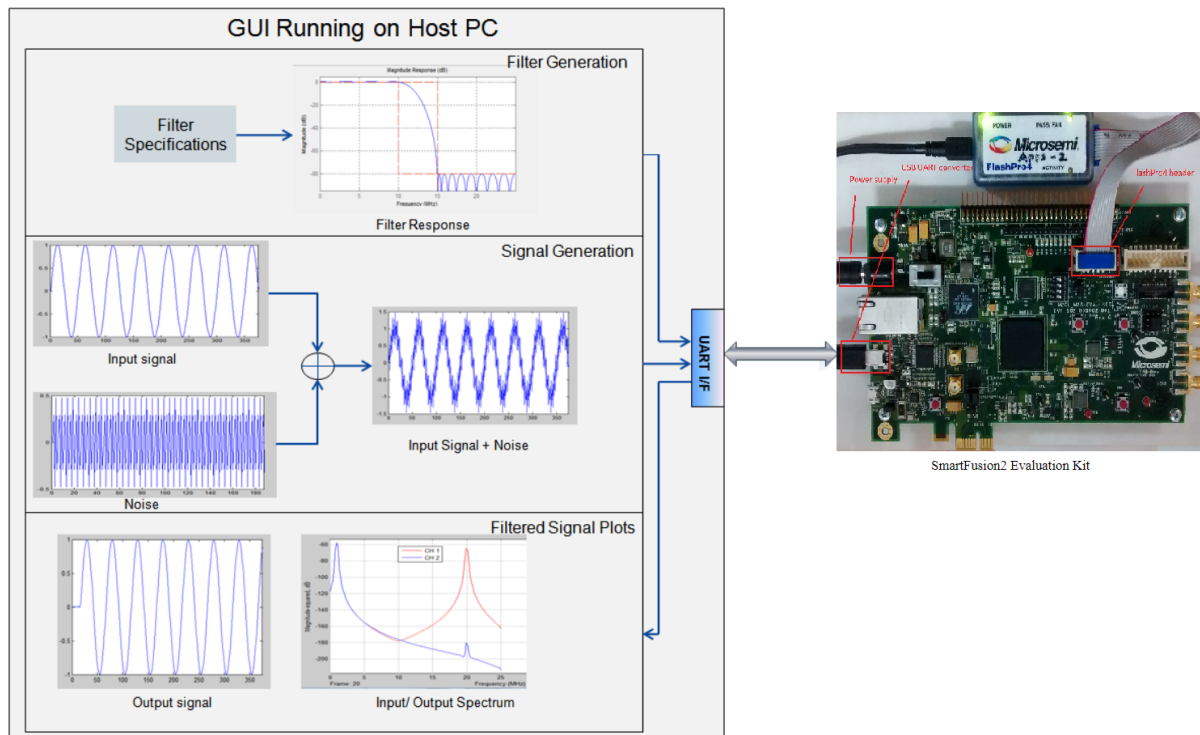
3.2   Design Requirements

Table 1 lists the hardware and software requirements for this demo design.

Table 1 •   **Design Requirements**

Requirement	Version
Operating System	64 bit Windows 7 and 10
Hardware	
SmartFusion2 Security Evaluation Kit: • FlashPro4 programmer • USB A to Mini-B cable	Rev D or later (M2S090TS-FGG484)
Host PC or Laptop	
Software	
FlashPro Express	Refer to the readme.txt file provided in the design files for the software versions used with this reference design.
Libero® System-on-Chip (SoC)	
Host PC Drivers	USB to UART drivers
Framework	Microsoft .NET Framework 4 client for launching demo GUI

Note: Libero SmartDesign and configuration screen shots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

3.3   Prerequisites

Before you begin:

Download and install Libero SoC (as indicated in the website for this design) on the host PC from the following location.

https://www.microsemi.com/product-directory/design-resources/1750-libero-soc

3.4   Demo Design

3.4.1   Introduction

The design files are available for download from the following paths in the Microsemi website:

http://soc.microsemi.com/download/rsc/?f=m2s_dg0438_df

The design files include:

• Libero_Project
• Programming_Job
• GUI executable
• Readme.txt file

Figure 2 shows the top-level structure of the SmartFusion2 Security Evaluation Kit design files. Refer to the Readme.txt file provided in the demo file folder for the complete directory structure.

Figure 2 •   **SmartFusion2 Security Evaluation Kit Demo Design Files Top-Level Structure**

```
<download_folder>
    │
    └──── m2s_dg0438_df
                    │
                    ├──── Libero_Project
                    │
                    ├──── GUI
                    │
                    ├──── Programming_Job
                    │
                    └──── Readme.txt
```
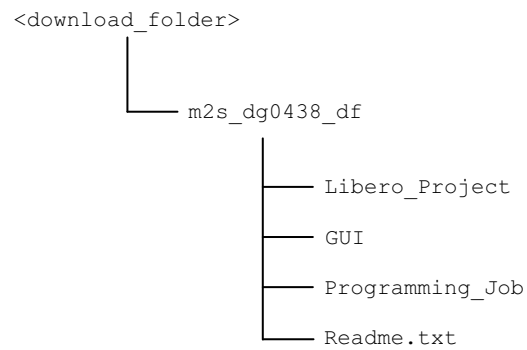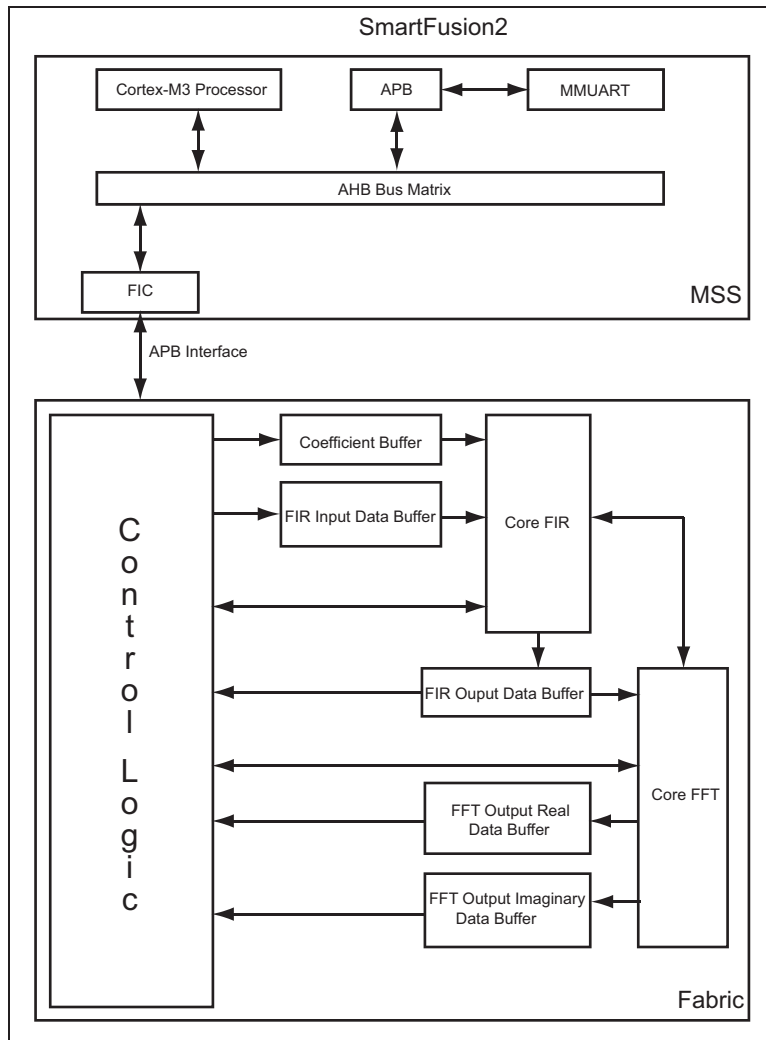
3.4.2   Demo Design Description

This demo design uses the following blocks:

- MSS Block, page 6
- Control Logic, page 6
- TPSRAM IP, page 7
- CoreFIR, page 7
- CoreFFT, page 7

Figure 3 shows the detailed block diagram of the demo design.

Figure 3 •   **DSP FIR Filter Demo Design Block Diagram**

3.4.2.1   MSS Block

MSS block sends and receives the data between the host PC (GUI interface) and fabric logic. MMUART interface is used to communicate with the host PC. FIC_0 interface (APB master) is used to communicate with the fabric user logic.

3.4.2.2   Control Logic

The user logic implemented in the fabric consists of the following Finite-State Machines (FSM):

- **Data Handling:** Implements and controls operations like loading the filter input data to the corresponding input data buffer and loading filter coefficients to the corresponding coefficient memory buffers. An APB bus slave is implemented to communicate with the MSS APB master.
- **Filter Control:** Controls the FIR filter and FFT operations. Loads the filtered data to the corresponding output buffer and moves the FFT output data to the corresponding output data buffer.

3.4.2.3 TPSRAM IP

TPSRAM IP is used to implement the following:

- Filter coefficient buffer (depth: 63, width: 16)
- Input signal data buffer (depth: 1024, width: 16)
- Output signal buffer (depth: 1024, width: 16)
- Output signal FFT real data buffer (depth: 1024, width: 16)
- Output signal FFT imaginary data buffer (depth: 1024, width: 16)

3.4.2.4 CoreFIR

The Core FIR IP is used in Reloadable coefficient mode to support Low pass, High pass, Band pass, and Band reject filters. Core FIR IP configuration is as follows:

- Filter Type: Single rate fully enumerated
- No of taps: 31
- Coefficients type: Reloadable
- Coefficients bit width: 16 (signed)
- Data bit width: 16 (signed)
- Filter structure: Transposed with symmetry

3.4.2.5 CoreFFT

The Core FFT IP is used for generating the frequency spectrum of the filtered data. Core FFT IP configuration is as follows:

- FFT Architecture: In place
- FFT type: Forward
- FFT Scaling: Conditional
- FFT Transform Size: 256
- Width: 16

3.5 Setting Up the Demo Design

3.5.1 Setting Up the Demo Design for SmartFusion2 Security Evaluation Kit

The following steps describe how to setup the hardware demo for SmartFusion2 Security Evaluation Kit:

1. Connect the jumpers on the SmartFusion2 Security Evaluation Kit board, as shown in Table 2.

*Table 2 •* **SmartFusion2 Security Evaluation Kit Jumper Settings**

Jumper	Configuration	Comments
J23	–	Jumper to select switch-side MUX inputs of A or B to the lineside.
	Close	Pin 1-2 (Input A to the lineside) that is on board 125 MHz differential clock oscillator output will be routed to lineside.
	Open	Pin 2-3 (Input B to the lineside) that is external clock required to source through SMA connectors to the lineside.
J22	–	Jumper to select the output enables control for the lineside outputs.
	Close	Pin 1-2 (Lineside output enabled)
	Open	Pin 2-3 (Lineside output disabled)
J24	Open	Jumper to provide the VBUS supply to USB when using in Host mode.
J8	–	JTAG selection jumper to select between RVI header or FP4 header for application debug.
	Close	Pin 1-2 FP4 for SoftConsole/FlashPro
	Open	Pin 2-3 RVI for Keil™ ULINK™/IAR J-Link®
	Open	Pin 2-4 for Toggling JTAG_SEL signal remotely using GPIO capability of FT4232 chip.
J3	–	Jumpers to select either SW2 input or signal ENABLE_FT4232 from FT4232H chip.

Note:

- Ensure that the power supply switch, SW7 is OFF while making the jumper connections.
- Connect the Power supply to the J6 connector, switch on the power supply switch, SW7.
2. Connect the FlashPro4 programmer to the J5 connector of the SmartFusion2 Security Evaluation Kit board.
3. Connect the host PC USB port to the P1 Mini USB connector on the SmartFusion2 Security Evaluation Kit board using the USB Mini-B cable.

Figure 4 shows the board setup for running the DSP FIR filter demo on the SmartFusion2 Security Evaluation Kit.
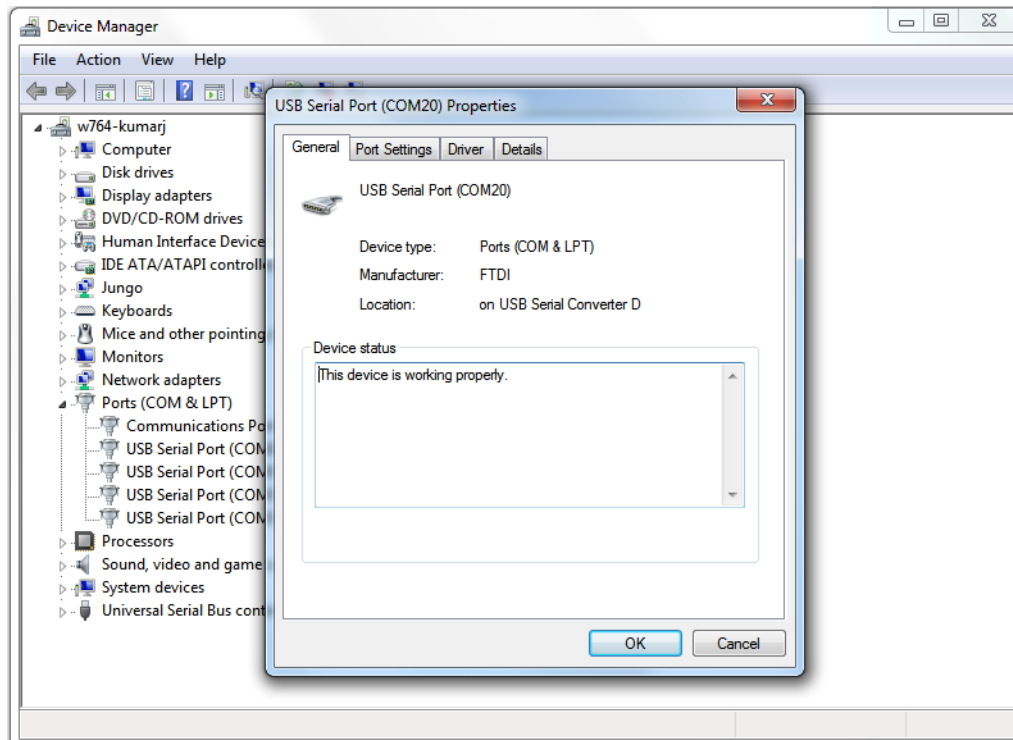
Figure 4 • **SmartFusion2 Security Evaluation Kit Setup**
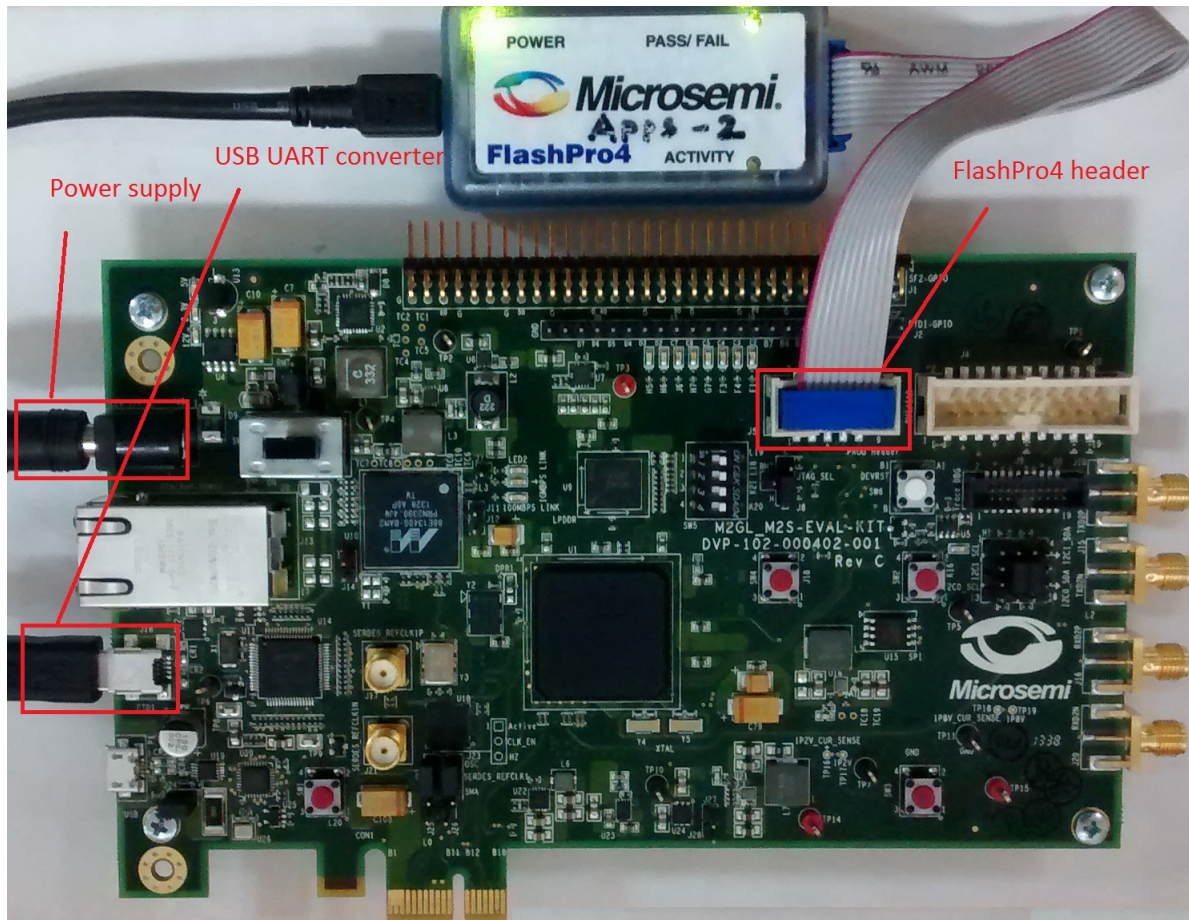
4.   Switch **ON** the power supply switch, SW7.
5.   Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the **Device Manager** of the host PC.

Figure 5 shows the USB Serial port.

Figure 5 • **USB to UART Bridge Drivers for SmartFusion2 Security Evaluation Kit**

6.   If USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip.

3.6   Programming the Demo Design

To program the SmartFusion2 Security Evaluation Kit board with the job file provided as part of the design files using FlashPro Express software, refer to Appendix 1: Programming the Device Using FlashPro Express, page 25.

3.6.1 DSP FIR Demo GUI

The DSP FIR demo is provided with a user-friendly GUI that runs on the host PC which communicates with the SmartFusion2 Security Evaluation Kit. The UART is used as the underlying communication protocol between the host PC and SmartFusion2 Security Evaluation Kit. Figure 6 shows the DSP FIR demo GUI.

Figure 6 • **DSP FIR Demo Window**
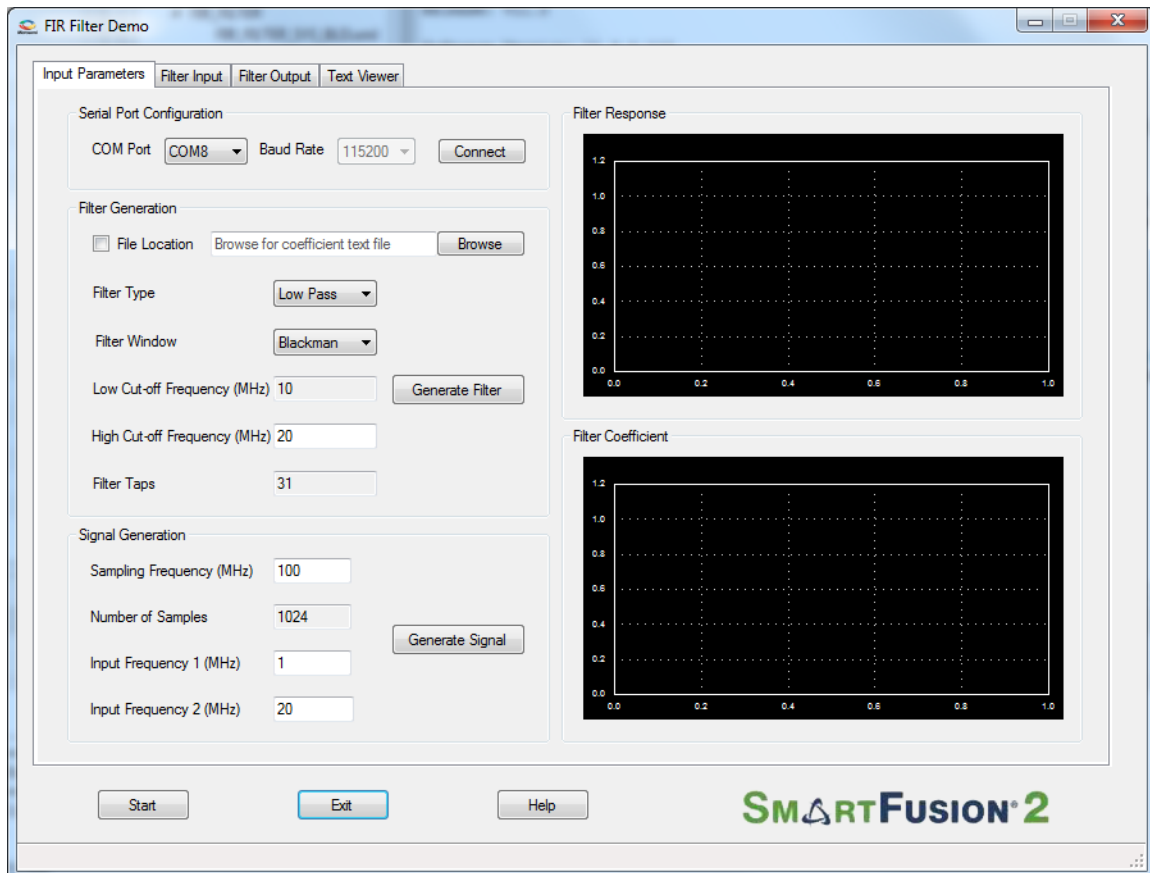
The DSP FIR demo window consists of the following tabs:

- **Input Parameters:** Configures the serial COM port, filter generation, and signal generation.
- **Filter Input:** Plots the input signal and its frequency spectrum
- **Filter Output:** Plots the output signal and its frequency spectrum
- **Text Viewer:** Shows the coefficients, input signal, output signal, and FFT data values

Click **Help** for more information on the GUI.
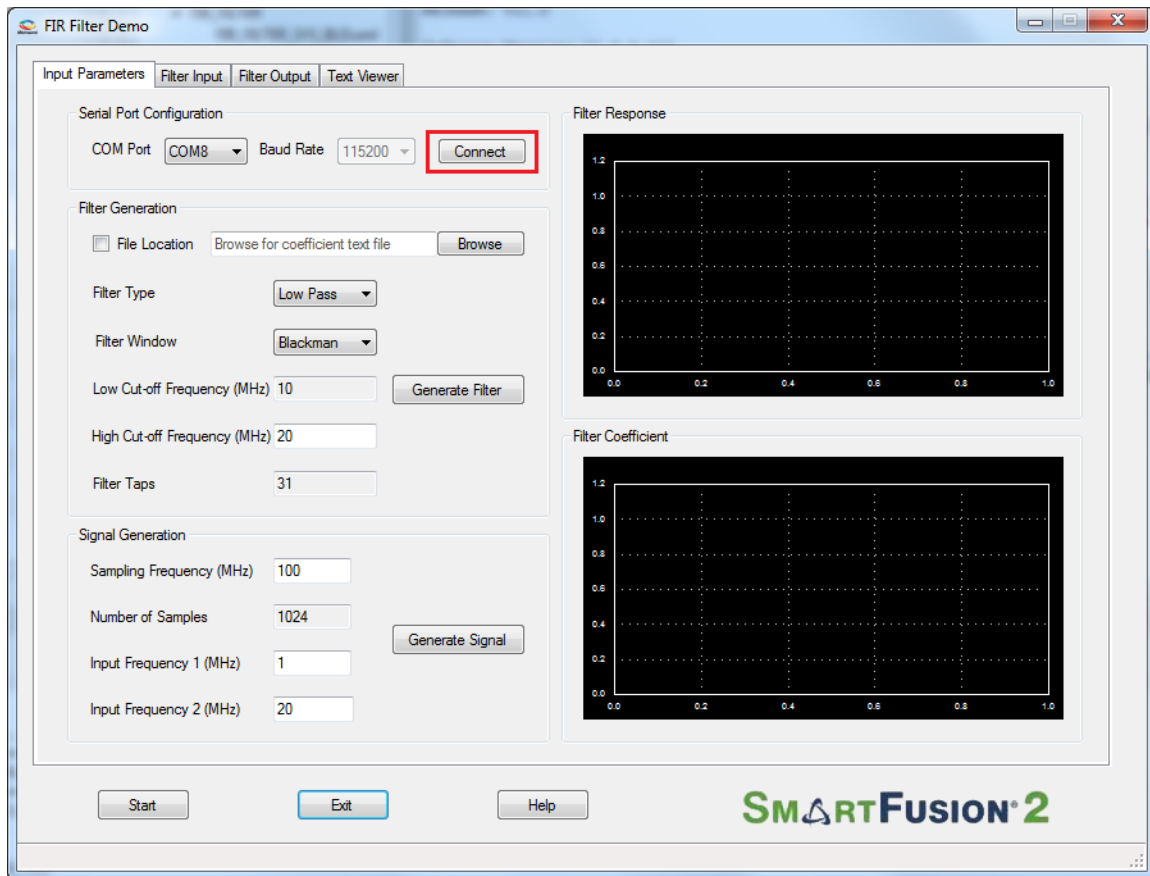
3.7 Running the Demo Design

The following steps describe how to run the demo design:

1. Launch the DSP FIR demo GUI, install and invoke the executable file provided with the design files. The default location of the executable file is:

   <download_folder>\m2s_dg0438_df\GUI\SF2_FIR_Filter.exe

   The FIR Filter Demo window is displayed, refer to Figure 7.

*Figure 7 •* **Serial Port Configuration**

2. **Serial Port Configuration:** The COM port number is automatically detected and baud rate is fixed at 115200. Click **Connect**, as shown in Figure 7.
3. **Filter Generation:** Two options are provided for generating the filter coefficients:
   • Generate the coefficients using MATLAB or any similar tool and save it as a text file (Refer Appendix 4: Coefficient Text File Format, page 30 for the format of the text file). The GUI can be used to browse and load this file, as shown in Figure 8.

Figure 8 • **Filter Generation - 1**
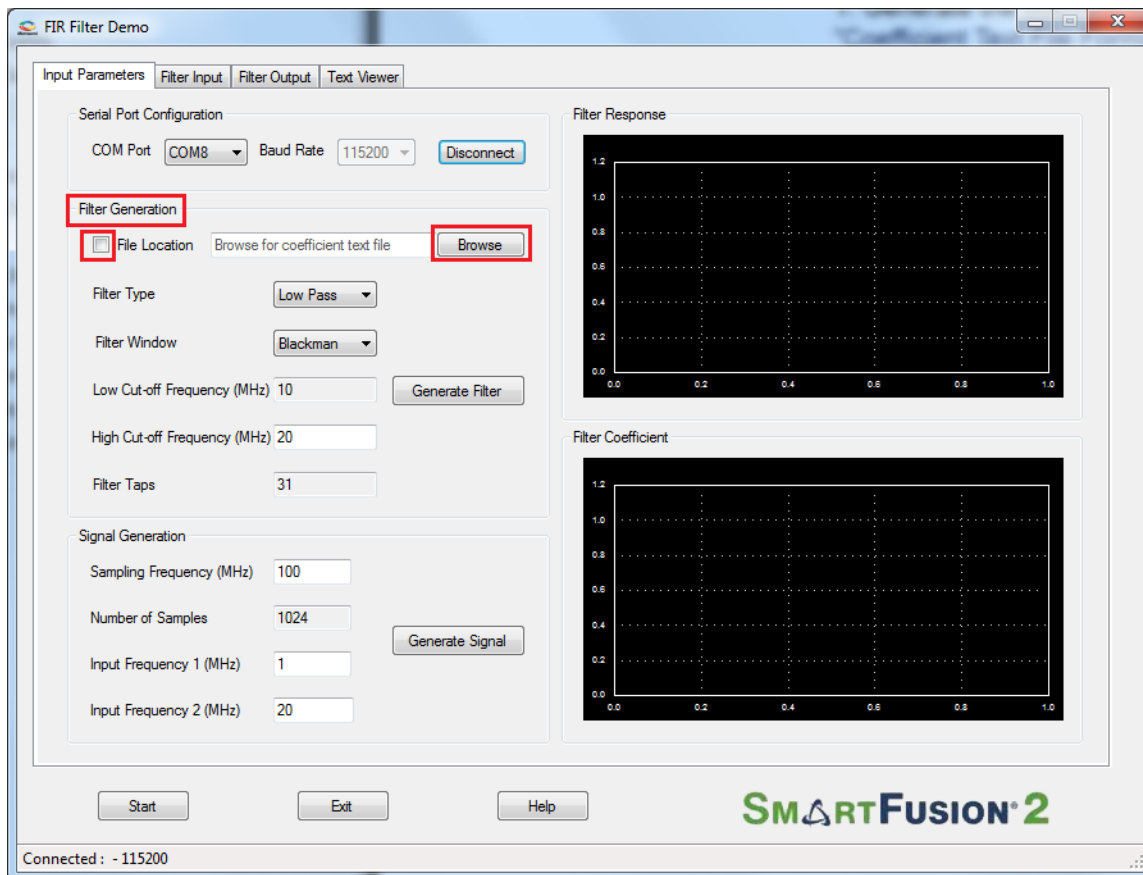
4. Generate the Filter coefficients using GUI as follows:

The following parameters are required to generate filter coefficients. Refer to Figure 9.

- **Filter Type:** Low Pass (Low-pass/High-pass /Band-pass/Band-reject filter)
- **Filter Window:** Blackman (Blackman/Hamming window)
- **Low Cut-off Frequency:** Disabled for Low-pass filter required (High cut-off frequency is disabled for High-pass filter)
- **High Cut-off Frequency:** 20 MHz
- **Filter Taps:** 31 (Fixed)

5. Press **Generate Filter** to generate the filter coefficients.

Figure 9 • **Filter Generation - 2**
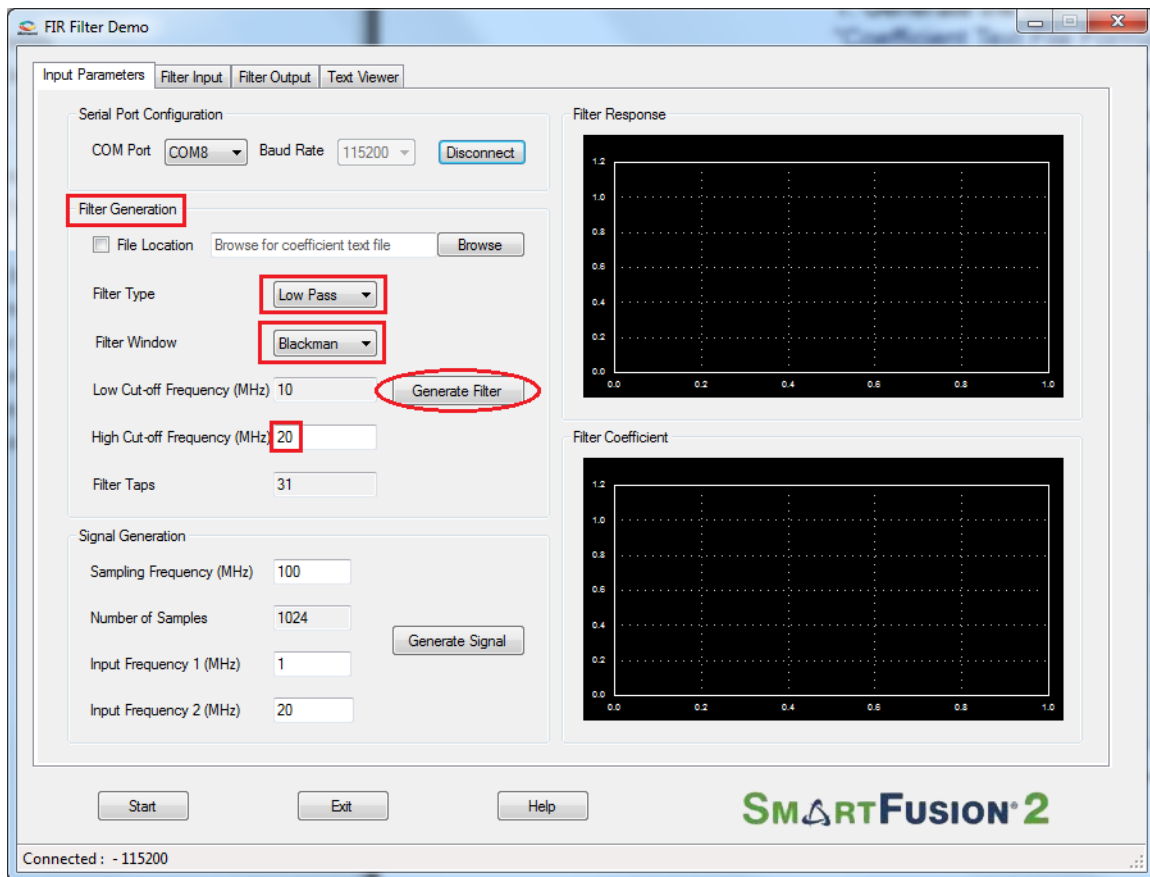
The successful after-generation graphs of the filter coefficients, filter response, and the filter coefficient plots, are displayed. Refer to Figure 10.

Figure 10 • **Filter Response and Filter Coefficient Plot**
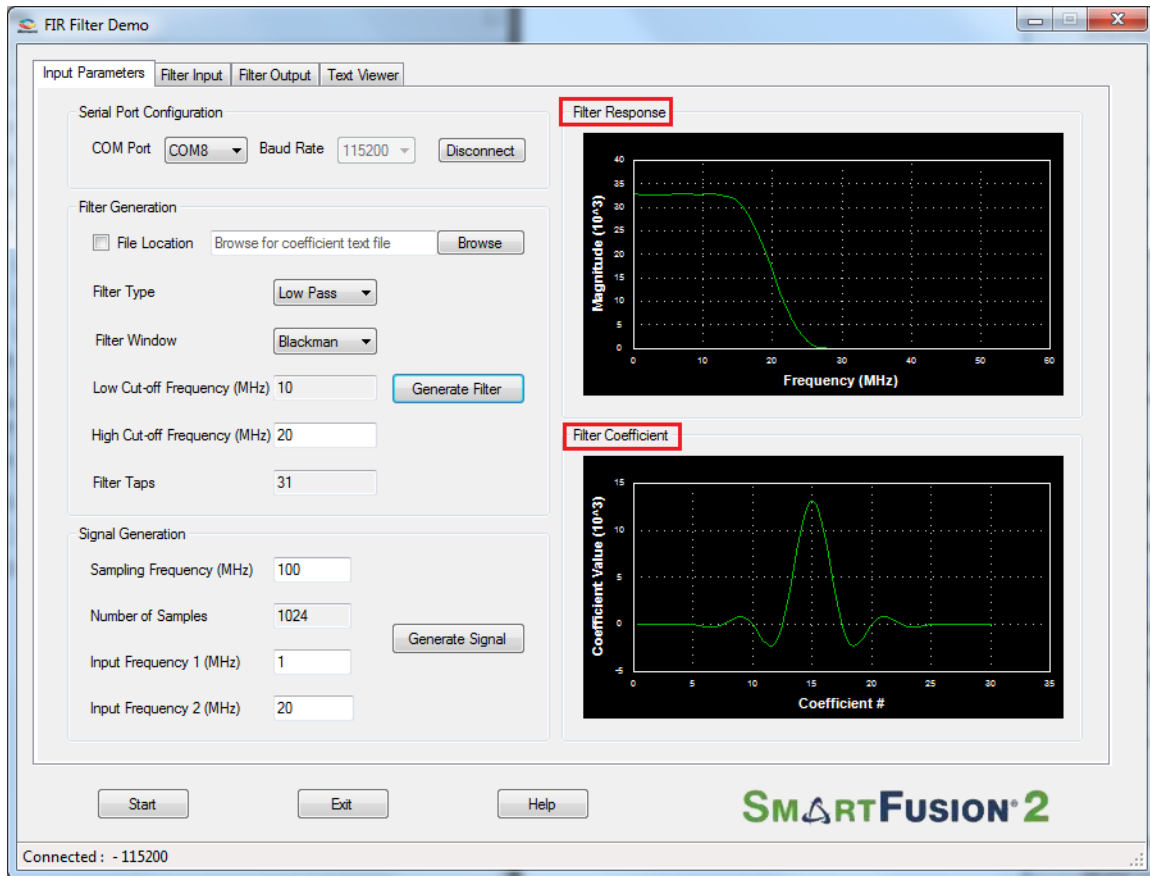
6. Select the following parameters in **Signal Generation**:
    - **Sampling Frequency:** 100 MHz (Fixed)
    - **Number of Samples:** 1024 (Fixed)
    - **Input Frequency 1:** Enter the signal frequency in the Pass-band region.
      For example, 1 MHz to High cut-off frequency.

    - **Input Frequency 2:** Enter the signal frequency in the Stop-band region.
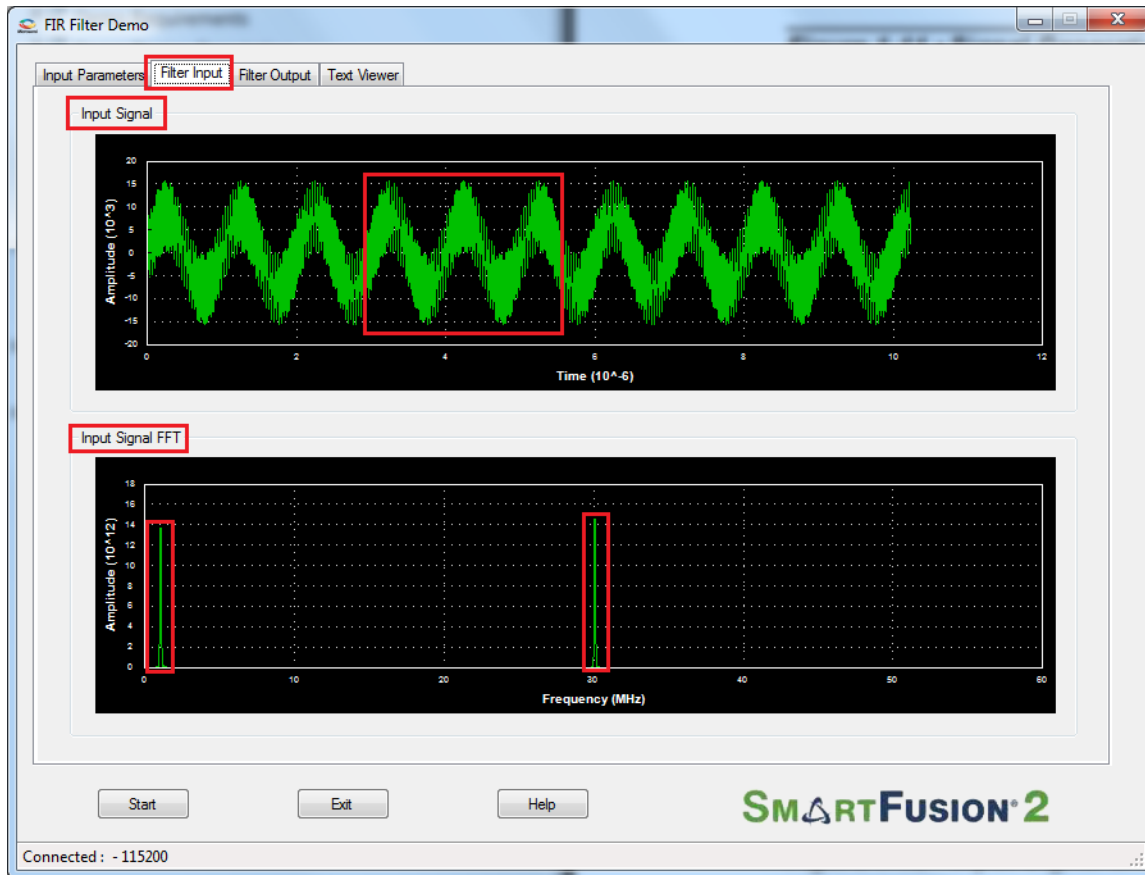   For example, High cut-off frequency to Sampling frequency/2.

7.   Click **Generate Signal**, as shown in Figure 11.

*Figure 11 •*   **Signal Generation**
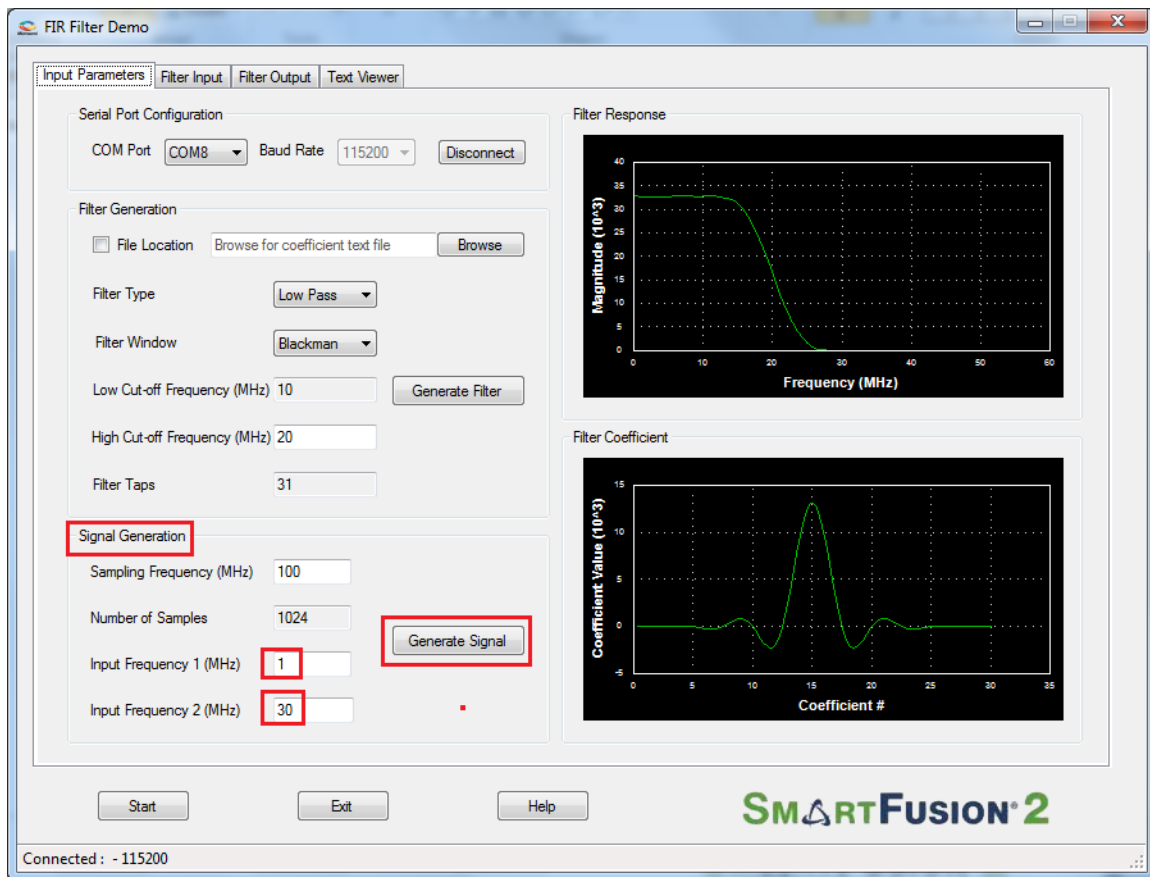
Input signal and the frequency spectrum of the specified signal are displayed, as shown in Figure 12.

*Figure 12 •* **Input Signal and Input Signal FFT Plot**

8. To configure the input frequencies and coefficients click **Start**, as shown in Figure 13. It sends the input data (1K samples) and filter coefficients to the SmartFusion2 device for processing the filtering operation.

*Figure 13* •   **DSP FIR Filter Demo - Start**
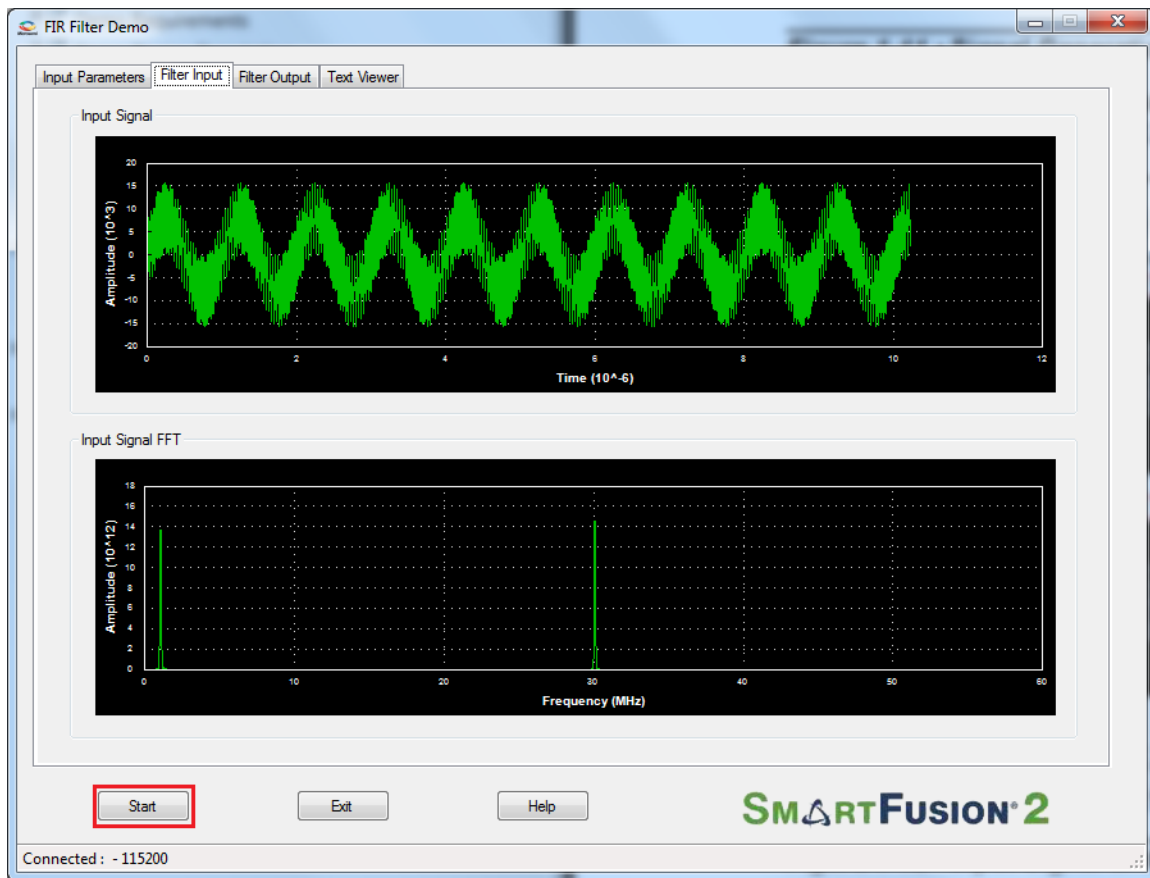
After completing the filter operation by SmartFusion2, the GUI plots the filtered data and FFT data on filter output window, refer to Figure 14. Since Low-pass filter option was selected, the High frequency component is suppressed while the Low frequency signal is preserved. This can be observed in the frequency spectrum of the output signal.

*Figure 14 •* **Filtered Signal: Time and Frequency Plot**
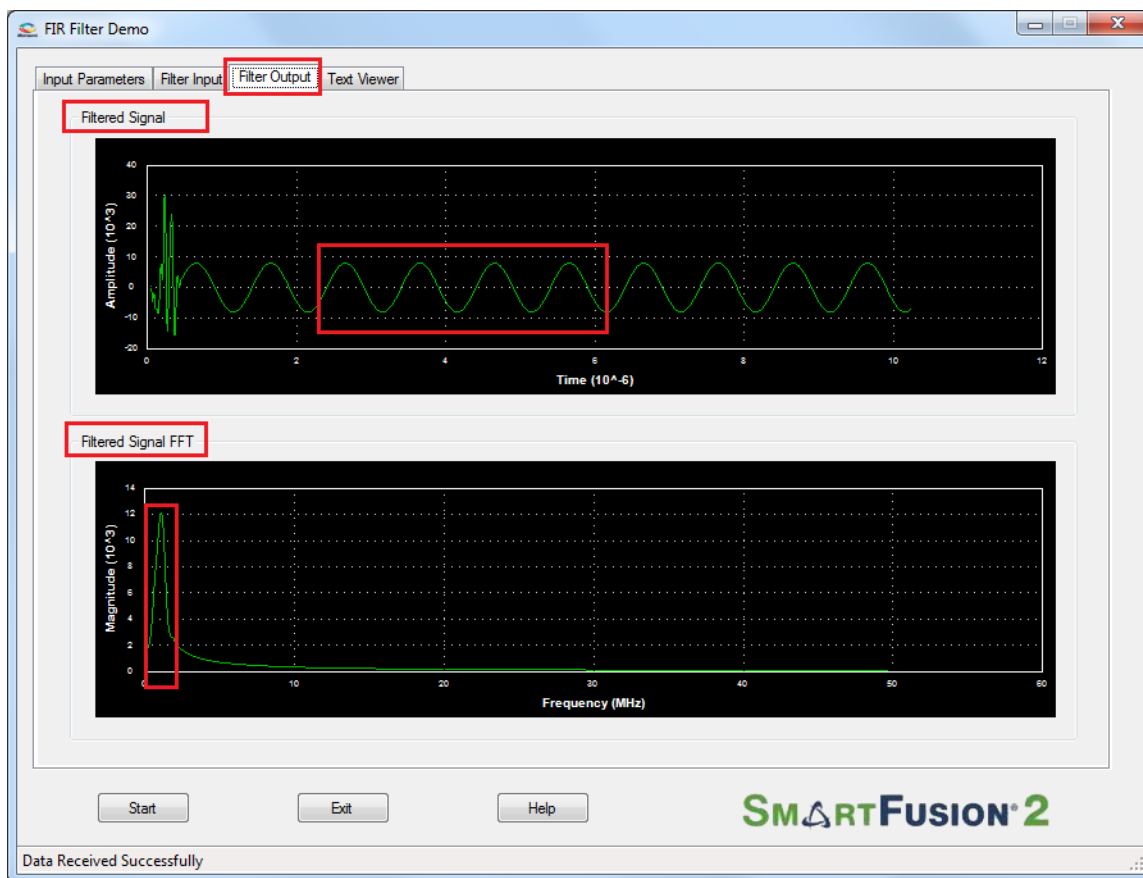
9. Right-click on the window, it shows different options, as shown in Figure 15. The data can be copied, saved, and exported to the CSV plot for analysis purpose. Page setup, print, show point values, zoom, and set scale are set to default.

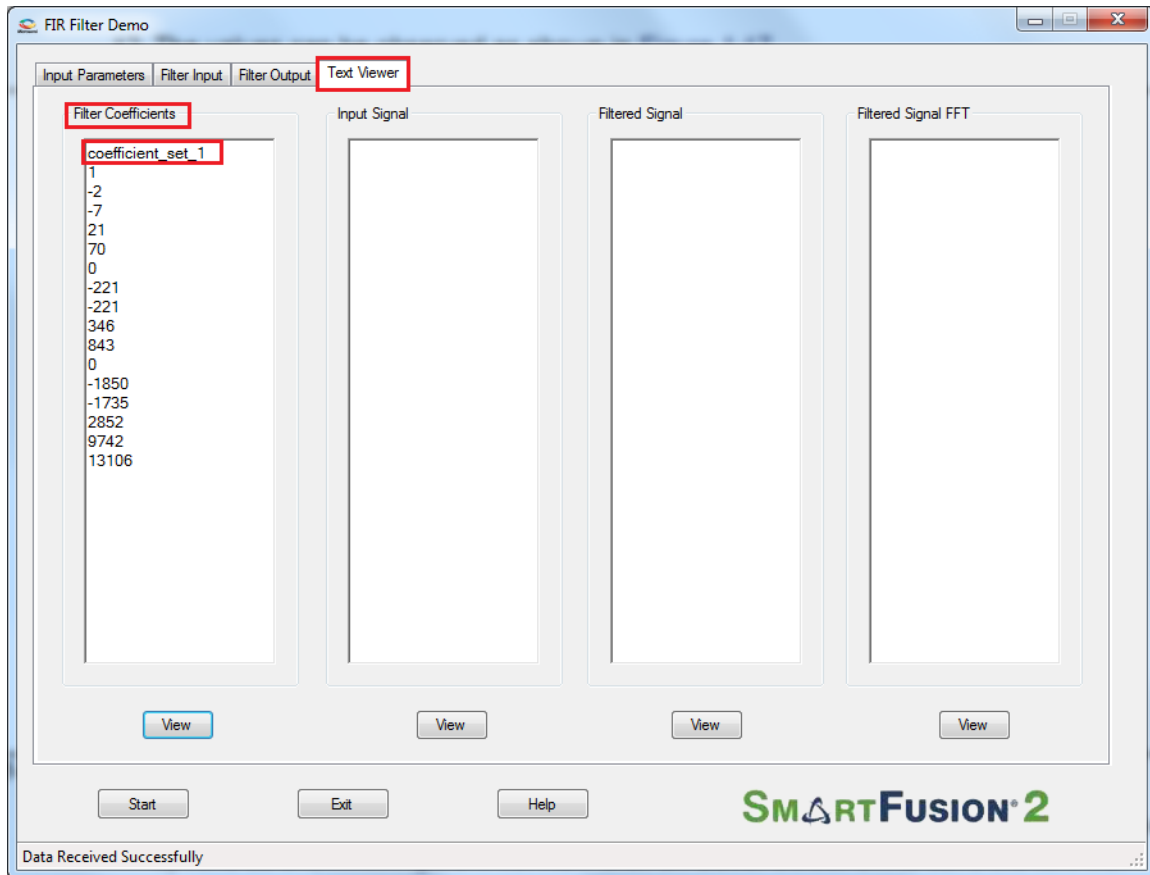*Figure 15 •* **Filtered Signal: GUI options**
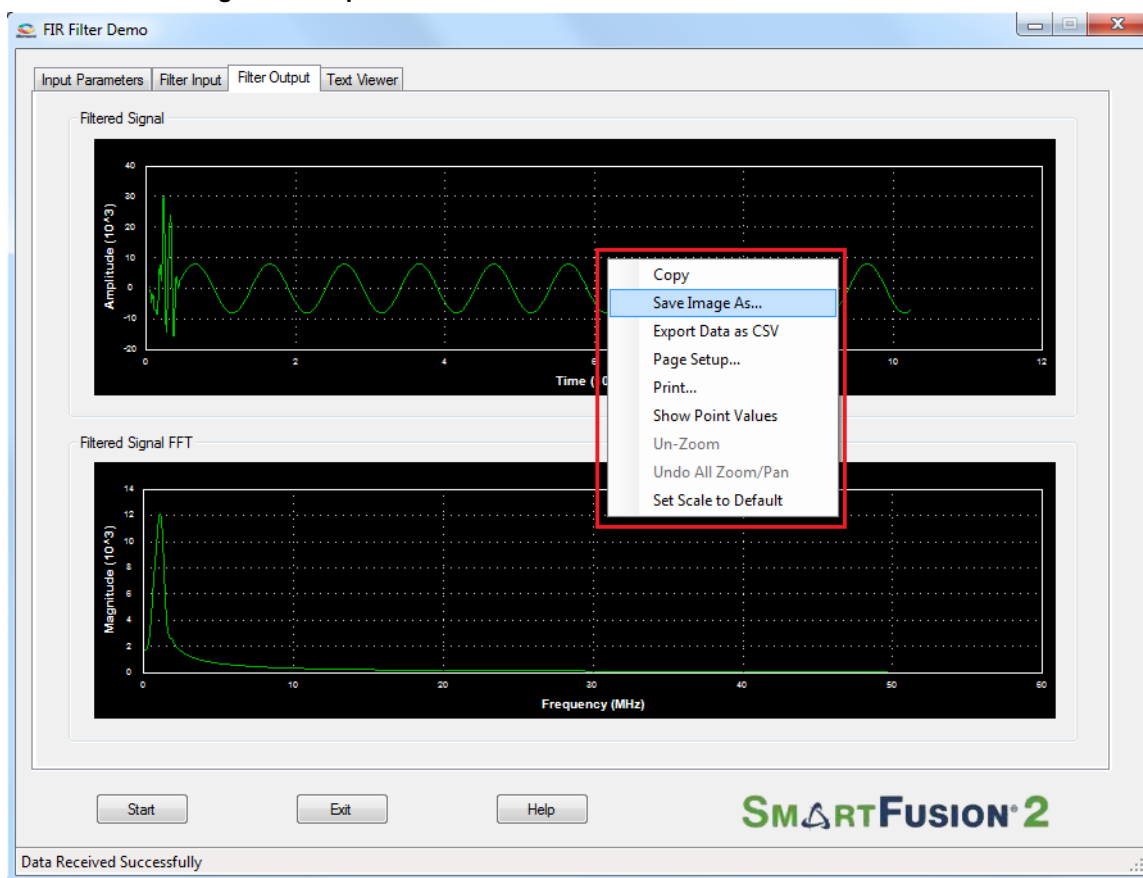
10. The filter coefficients, input signal, output signal, and FFT output data values can be viewed in **Text viewer**. Click **Text Viewer** tab and then click the corresponding **View**, as shown in Figure 16.

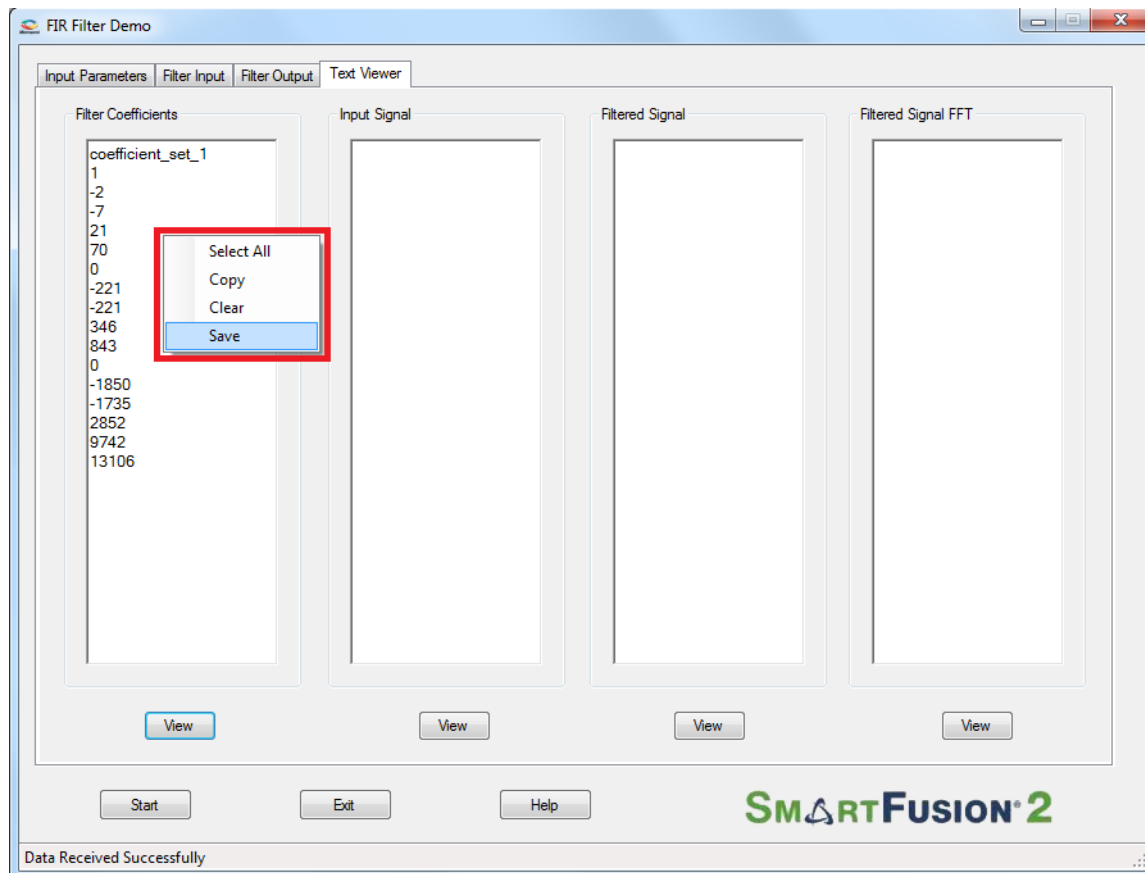*Figure 16 •* **Text Viewer**
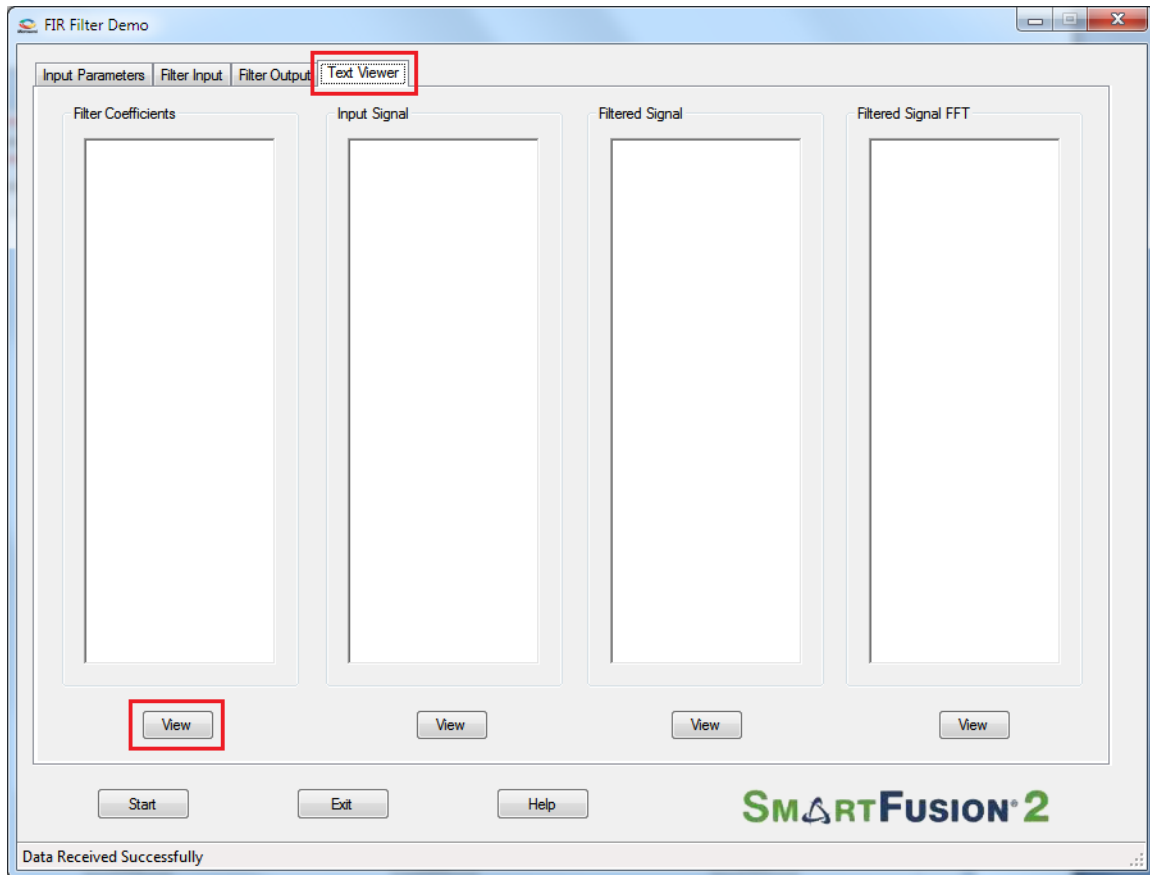
The values can be observed, as shown in Figure 17.

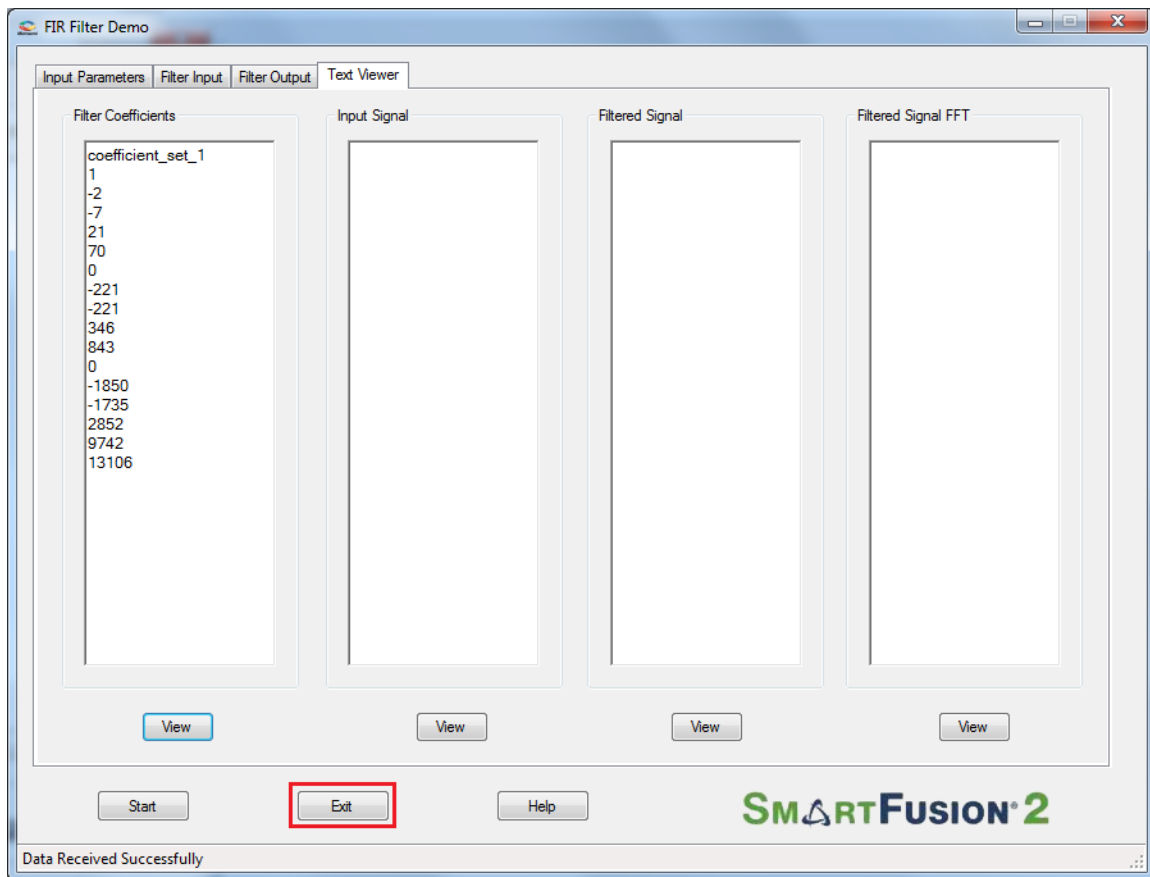*Figure 17 •*   **Text Viewer: Filter Coefficient Values**

11. To save the coefficients as a text file, right-click the **Filter Coefficients** window, it shows different options, as shown in Figure 18. Now click **Save**. Select **OK** to save the text file.

Figure 18 • **Text Viewer: Coefficients Save Options**

12. Click **Exit** to stop the demo. Refer to **Figure 25**.

Figure 19 • **Exit Demo**

3.8   Conclusion

This demo shows the features of the SmartFusion2 device including MSS, mathblocks, and LSRAMS for DSP specific applications. Also provides information about how to use the Microsemi DSP IP cores (CoreFIR, CoreFFT). This GUI-based demo is easy to use and provides several options to understand and implement DSP filters on the SmartFusion2 device.

4 Appendix 1: Programming the Device Using FlashPro Express

This section describes how to program the SmartFusion2 device with the programming job file using FlashPro Express.

To program the device, perform the following steps:

1. Ensure that the jumper settings on the board are the same as those listed in Table 2, page 8.

Note: The power supply switch must be switched off while making the jumper connections.

2. Connect the power supply cable to the **J6** connector on the board.
3. Power **ON** the power supply switch **SW7**.
4. On the host PC, launch the **FlashPro Express** software.
5. Click **New** or select **New Job Project from FlashPro Express Job** from **Project** menu to create a new job project, as shown in Figure 20.

Figure 20 • **FlashPro Express Job Project**
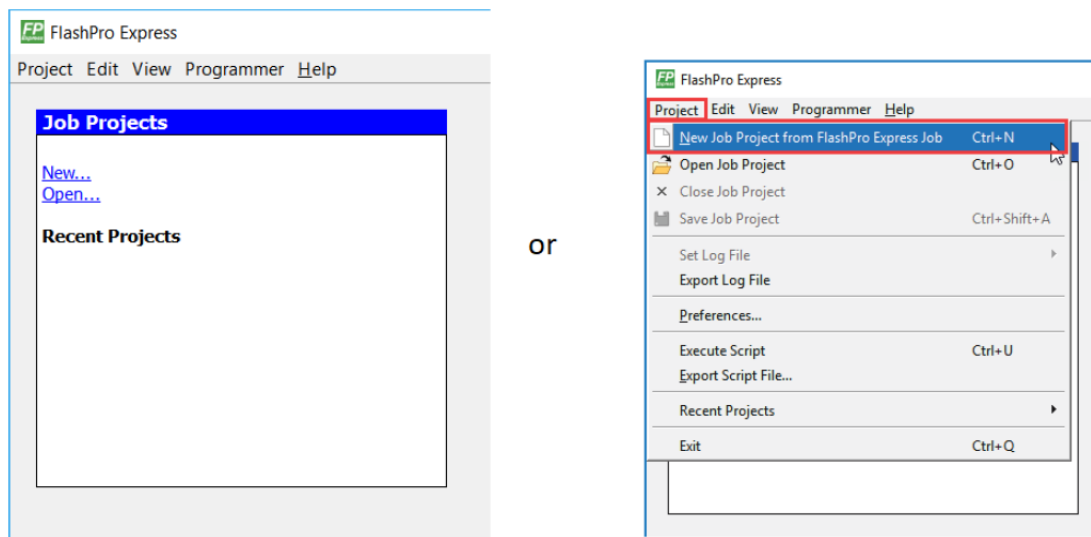
6. Enter the following in the **New Job Project from FlashPro Express Job** dialog box:
• **Programming job file:** Click **Browse**, and navigate to the location where the .job file is located and select the file. The default location is:
   `<download_folder>\m2s_dg0438_df\Programming_Job`
• **FlashPro Express job project name:** Click **Browse** and navigate to the location where you want to save the project.

Figure 21 • **New Job Project from FlashPro Express Job**
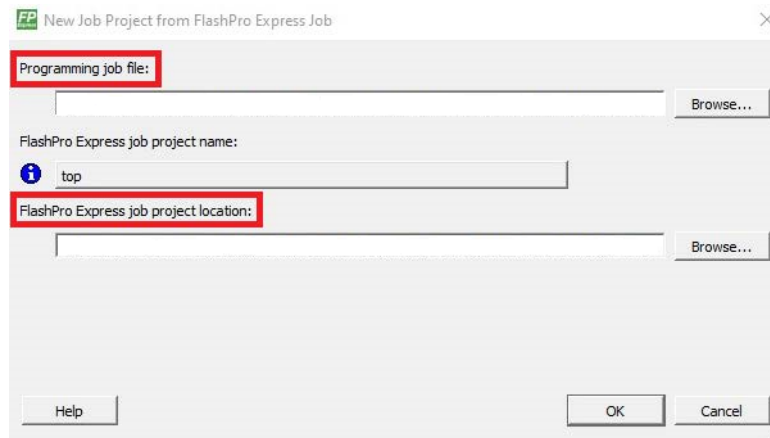
7. Click **OK**. The required programming file is selected and ready to be programmed in the device.
8. The FlashPro Express window appears as shown in Figure 22. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan** Programmers.

Figure 22 • **Programming the Device**
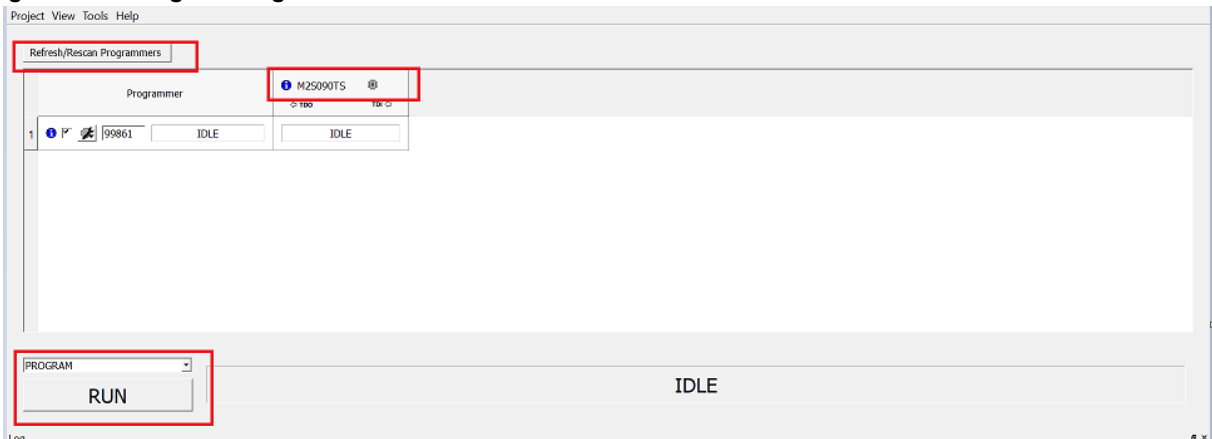
9. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in Figure 23.

Figure 23 • **FlashPro Express—RUN PASSED**
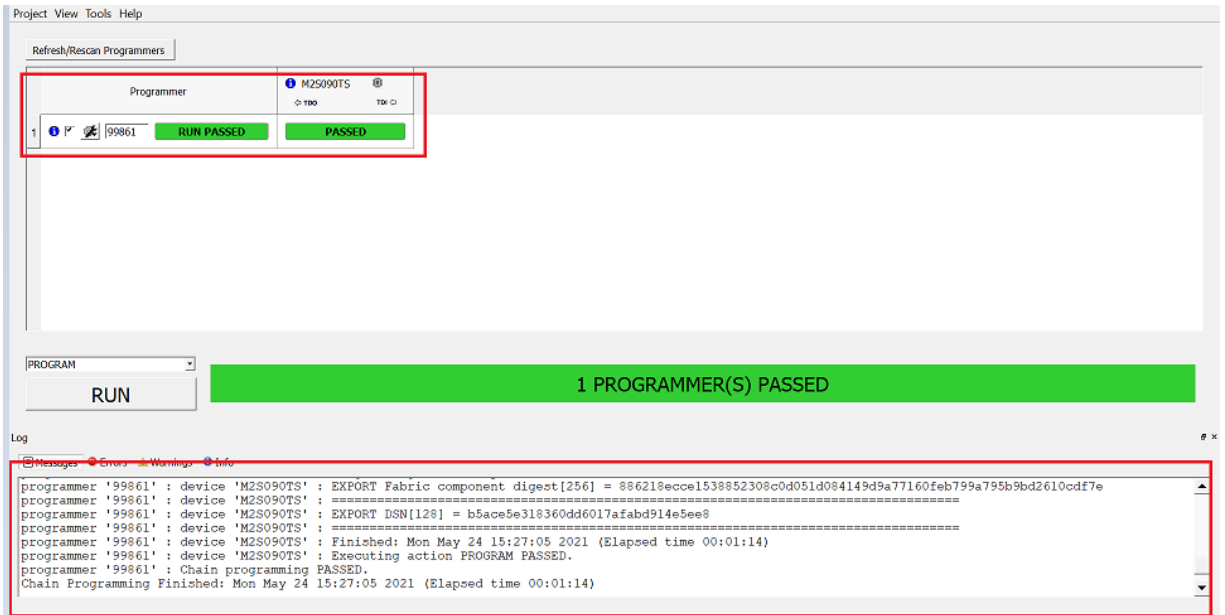
10. Close **FlashPro Express** or in the Project tab, click **Exit**.

5 Appendix 2: SmartDesign Implementation

DSP FIR filter SmartDesign is shown in Figure 24.
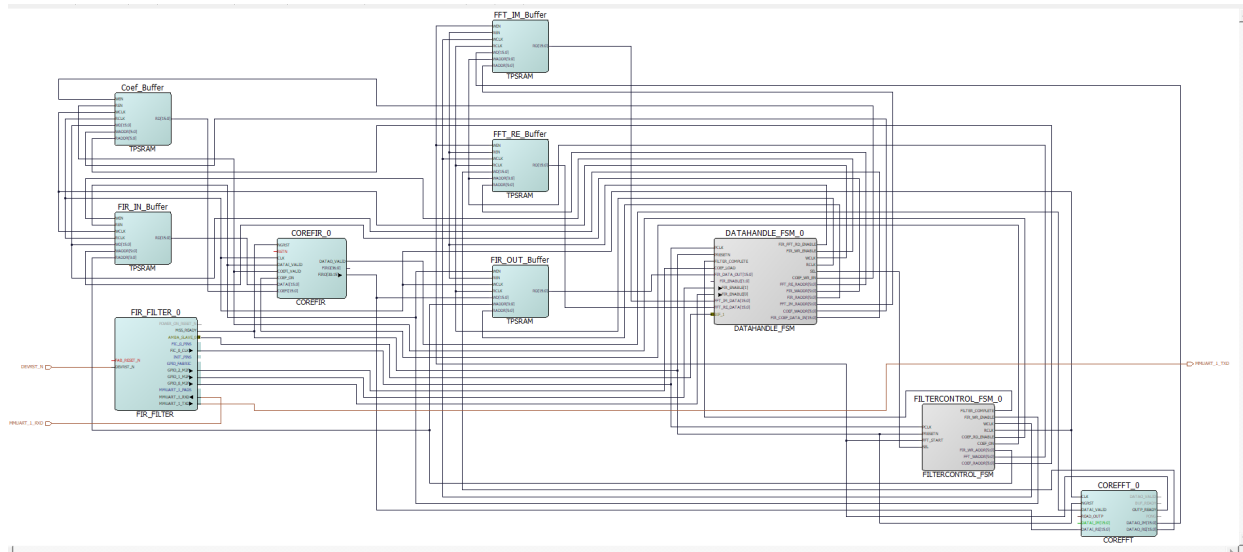
Figure 24 • **DSP FIR Filter SmartDesign**

Table 3 shows SmartDesign blocks in DSP FIR Filter.

Table 3 • **DSP FIR Filter Demo SmartDesign Blocks and Description**

S.No	Block Name	Description
1	FIR_FILTER_0	FIR_FILTER_0 is a System Builder generated component, in which MMUART is configured to handle the communication between the host PC and fabric logic. To generate a System Builder component, refer to the *SmartFusion2 System Builder User Guide*.
2	DATAHANDLE_FSM	Control logic to send/receive the data between MSS and data buffers.
3	FILTERCONTROL_FSM	Control logic to generate the control signals for FIR and FFT operations.
4	Coef_Buffer	TPSRAM IP for filter coefficient buffer
	FIR_IN_Buffer	TPSRAM IP for FIR input signal data buffer
	FIR_Out_Buffer	TPSRAM IP for FIR output signal buffer
	FFT_Im_Buffer	TPSRAM IP for FFT output imaginary data buffer
	FFT_Re_Buffer	TPSRAM IP for FFT output real data buffer
5	COREFIR	COREFIR IP
6	COREFFT	COREFFT IP

6   Appendix 3: Resource Usage Summary

Table 4 shows DSP FIR filter resource usage summary.

Device: SmartFusion2 device

Die: M2S090TS

Package: 484 FBGA

Table 4 •   **DSP FIR Filter Demo Resource Usage Summary**

Type	Used	Total	Percentage
4LUT	2645	86184	3.07
DFF	3382	86184	3.92
RAM64x18	0	112	0.00
RAM1K18	12	109	11.01
MACC	20	84	23.81

Table 5 shows MACC blocks usage summary.

Table 5 •   **MACC Blocks Usage Summary**

CoreFIR	CoreFFT	Total
16	04	20

Table 6 shows RAM1K x 18 blocks usage summary.

Table 6 •   **RAM1Kx18 Blocks Usage Summary**

CoreFIR	CoreFFT	Fabric Buffers	Total
0	7	5	12

7   Appendix 4: Coefficient Text File Format

The FIR filter coefficients can be loaded from an ASCII text file (`*.txt`). Create the coefficient file using a text editor. The format of text file should be, as shown in Figure 25. Coefficient values must be entered as integer numbers. For a symmetric or anti-symmetric filter, only half of the coefficients must be listed in the file (applies to the Fully Enumerated type only). Only one coefficient value per line is permitted. An extra empty line must be placed after the last coefficient of the last set.

Figure 25 •   **Coefficient File Example - 9 Taps, Decimal Values**

```
coefficient_set_1
5
6
10
25
63
- 1
- 11
- 32
- 63
```