Total Ionizing Dose Test Report

No. 11T-RTAX2000S-CG624-D4Y4F1

February 2011

Table of Contents

TOTAL IONIZING DOSE TEST REPORT

No. 11T-RTAX2000S-CG624-D4Y4F1

February 16, 2011

C.K. Huang and J.J. Wang

(650) 318-4209, 318-4576

chang-kai.huang@microsemi.com, jih-jong.wang@microsemi.com

I. Summary Table

Parameter	Tolerance
1. Functionality	Passed 300 krad(SiO_2)
2. Standby Power Supply Current (I_{CCA}/I_{CCI})	Passed 200 krad(SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 300 krad(SiO_2)
4. Output Threshold (VOL/VOH)	Passed 300 krad(SiO_2)
5. Propagation Delay	Passed 300 krad(SiO_2) for ±10% degradation criterion
6. Transition Characteristic	Passed 300 krad(SiO_2)

II. Total Ionizing Dose (TID) Testing

The design of the following testing is based on an extensive, published database accumulated from the TID testing of many generations of antifuse-based FPGAs. The link to the database:

http://www.actel.com/products/milaero/hireldata.aspx#tid

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. Each input is grounded during irradiation and annealing.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000S
Package	CG624
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	rtax2000_CG624_Top
Die Lot Number	D4Y4F1
Quantity Tested	6
Serial Number	200 krad(SiO_2): 11453, 11454, 11455 300 krad(SiO_2): 11457, 11460, 11461
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	5 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Annealing Bias VCCI/VCCA	Static at 3.3 V/1.5 V
I/O Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

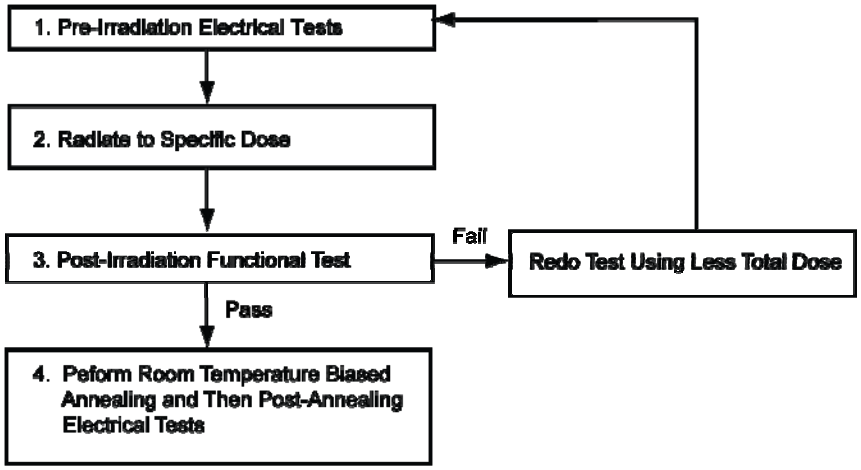

Figure 1 Parametric Test Flow Chart

The test method basically is in compliance with the military standard TM1019.8. Figure 1 is the flow chart of the testing sequence. The accelerated annealing test in section 3.12 is not performed lot-to-lot. This is because for a deep-submicron CMOS technology used by the RTAXS product, the adverse effects due to interface state at the gate SiO_2/Si interface are negligible. The function of commercial non-irradiated transistors would be unreliable if the degradation of interface plays an important role. In other words, the SiO_2/Si interface in deep submicron CMOS transistors has to be radiation hard for even commercial applications. Thus the dominant annealing effect in RTAXS devices is the reduction of trapped holes in the SiO_2; this basically alleviates the radiation effects on the DUT. A separate report on the accelerated annealing test will be provided to justify the omission of it in the lot testing; the justification testing will follow section 3.12.1.b.5.

Section 3.11 extended room temperature anneal test is also applied; room temperature annealing for 7 days was done on each device before the final parameter measurements.

C. Logic Design and Electrical Parameter Measurements

The DUT uses a high utilization generic design, rtax2000_CG624_Top, for testing total dose effects. These logic designs are described in the following subsections. Figure 2 shows the block diagram and the Verilog file (rtax2000_CG624_Top.v) is located at this URL:

http://www.actel.com/products/milaero/hireldata.aspx#tid

Generally, the functional test is performed on every design; most inputs are tested for threshold voltage and leakage current, including global clocks; the standby I_{CC} includes I_{CCI} and I_{CCA}. Except propagation delay and the transition characteristic, which is measured on the output O_BS, all other parameter measurements are done on a tester. Also note that, due to logistics limitation, the post-irradiation but pre-room-temperature-annealing functional test is performed on bench; the tested designs are shift registers and long buffer string, which are design 5 and 6 described in the following.

1. Embedded SRAM

   This design is to test the function of the embedded SRAM. It uses all the RAM blocks available in the DUT. This design enables an automatic testing sequence that every bit is written and then read. Any error will be reported as a signal in the output.

2. Unidirectional LVTTL Input and Output

   This is for testing radiation effects on unidirectional input and output threshold, leakage, and buffer fan-out. There are 3 sub-designs: a) a logic-core buffer with 8 fan-outs; b) a logic-core buffer with 3 fan-outs; c) 6 channels of input buffer directly connected to output buffer without core logic. LVTTL is used because it is the worst case among all the single-ended standards.

3. Bidirectional LVTTL I/O

   This design is for testing the radiation effects on the input/output characteristic of the bidirectional /IO. There are 7 channels of bidirectional IO for radiation effects testing.

4. LVPECL Input

   This design is for testing the radiation effects on the LVPECL differential inputs. 3.3 V LVPECL is considered the worst case differential input standard in the DUT. There are 7 channels.

5. Shift Registers

   This design is to test the radiation effects on the function of flip-flops, which are configured R-Cells. There are 4 shift registers and each using a different global clock; one has 3,584 bits and the other three each has 2,048 bits.

6. Long Buffer String

   This design is to measure the radiation effects on the propagation delay. The input of the design uses a clock feeding a toggle flip-flop to generate a checkerboard signal; this signal is then fed into a buffer string with 10,000 stages. The time delay between the input clock edge at CLOCK_IN and the output switching due to this clock edge at O_BS is defined as propagation delay high to low (T_{pdhl}) or low to high (T_{pdlh}); the percentage change of the average of T_{pdhl} and T_{pdlh} is used to determine the radiation effects. More than 10% of propagation change is considered a failure.

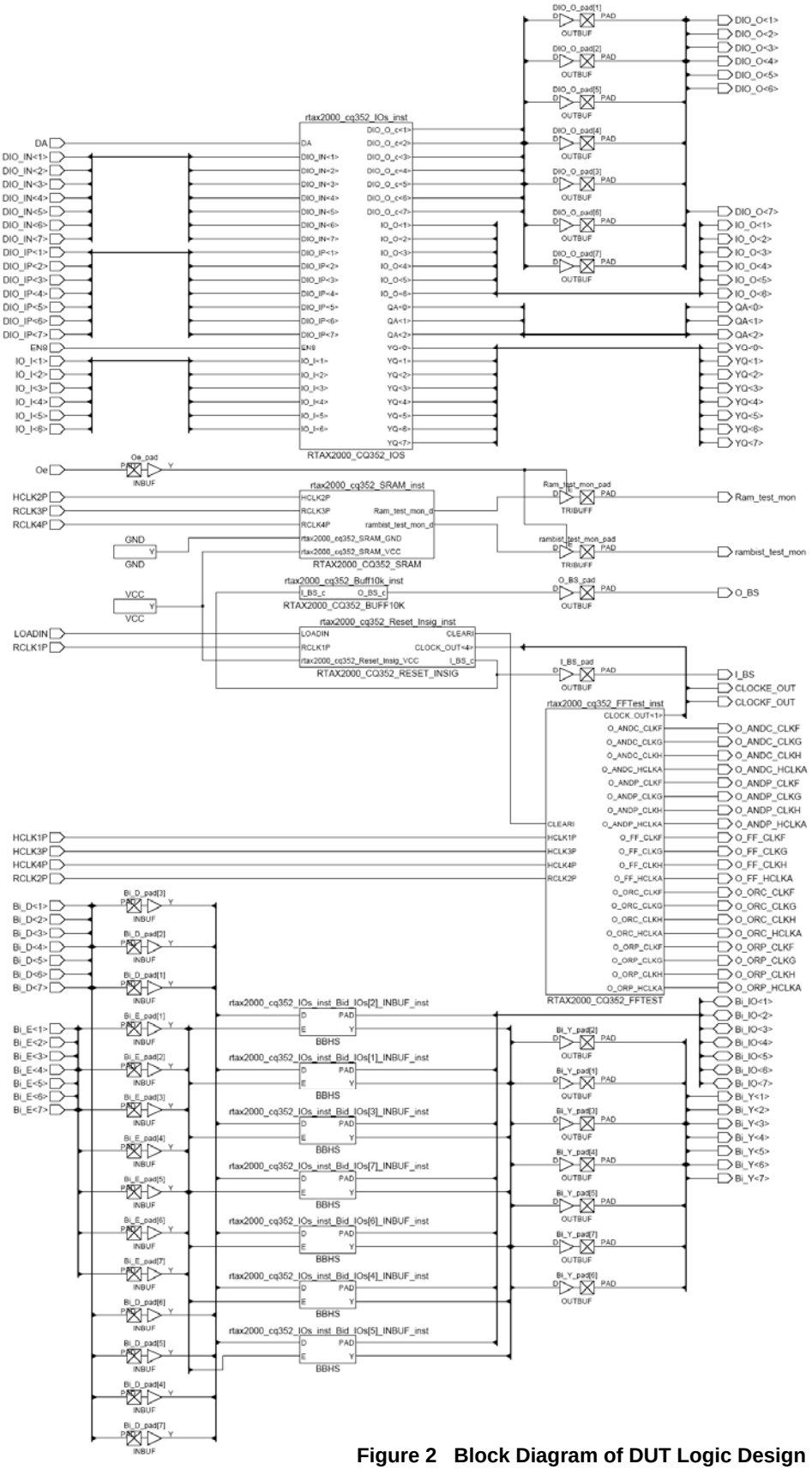

Figure 2 Block Diagram of DUT Logic Design

III. Test Results

A. Functional Test

Every DUT passed the pre-irradiation and post-annealing functional tests on the tester; it also passed post-irradiation test on-bench.

B. Standby Power Supply Current (I_{CCA} and I_{CCI})

Figure 3 through Figure 8 show the influx standby I_{CCA} and I_{CCI} versus total dose of every DUT.

In compliance with TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing I_{CC} in this test is defined as the addition of highest I_{CCI}, $I_{CCDA.}$ and $I_{CCDIFFA}$ values in Table 2-4 of the RTAXS specification sheet:

http://www.actel.com/documents/RTAXS_DS.pdf

Thus for I_{CCA}, the PIPL is 500 mA; the PIPL of I_{CCI} equals 35+10+3.13 × 7 = 66.91 (mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT.

Table 2 summarizes the pre-irradiation, post-irradiation and post-annealing I_{CC} data: the post-annealing I_{CCA} of every DUT pass the PIPL easily; the post-annealing I_{CCI} of DUTs irradiated to 200 krad(SiO_2) all pass the PIPL, while the I_{CCI} of DUTs irradiated to 300 krad(SiO_2) all exceed the PIPL.

Table 2 Pre-Irradiation, Post-Irradiation and Post-Annealing I_{CCA} and I_{CCI}

DUT	Total Dose krad (SiO_2)	I_{CCA} (mA)			I_{CCI} (mA)		
		Pre-Irrad.	Post-Irrad.	Post-Ann.	Pre-Irrad.	Post-Irrad.	Post-Ann.
11453	200 krad	6.31	6.19	6.01	26.02	95.30	63.70
11454	200 krad	4.23	4.35	3.87	24.49	102.25	48.86
11455	200 krad	7.17	5.74	5.23	24.30	115.11	55.59
11457	300 krad	7.63	64.75	10.11	25.24	280.20	142.92
11460	300 krad	4.27	65.80	5.97	24.15	237.20	155.95
11461	300 krad	7.75	41.68	8.42	25.10	238.20	140.92

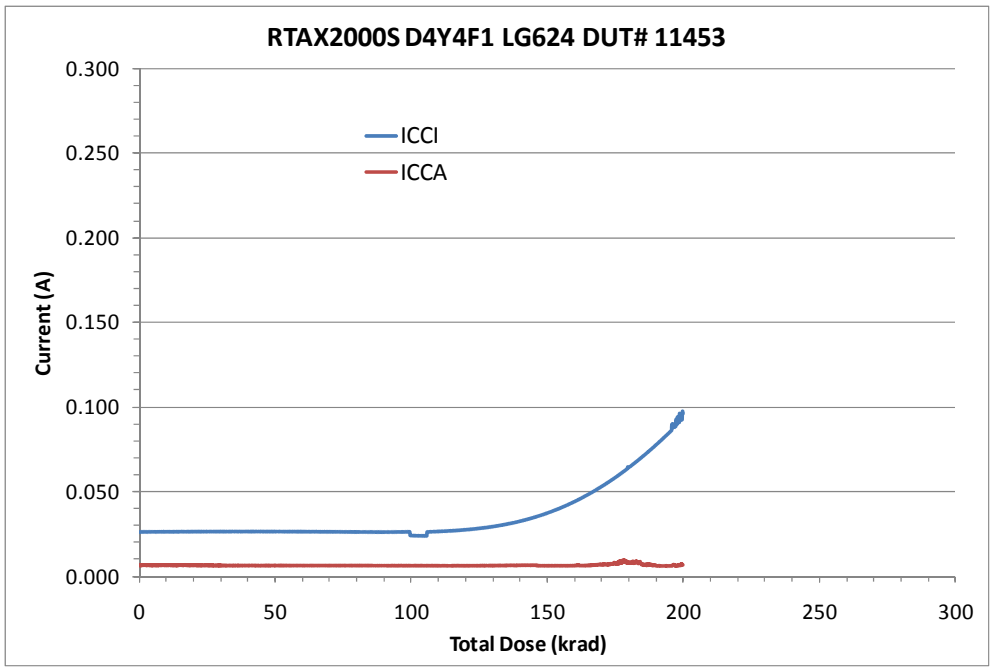

Figure 3 DUT 11453 Influx I_{CCA} and I_{CCI}.

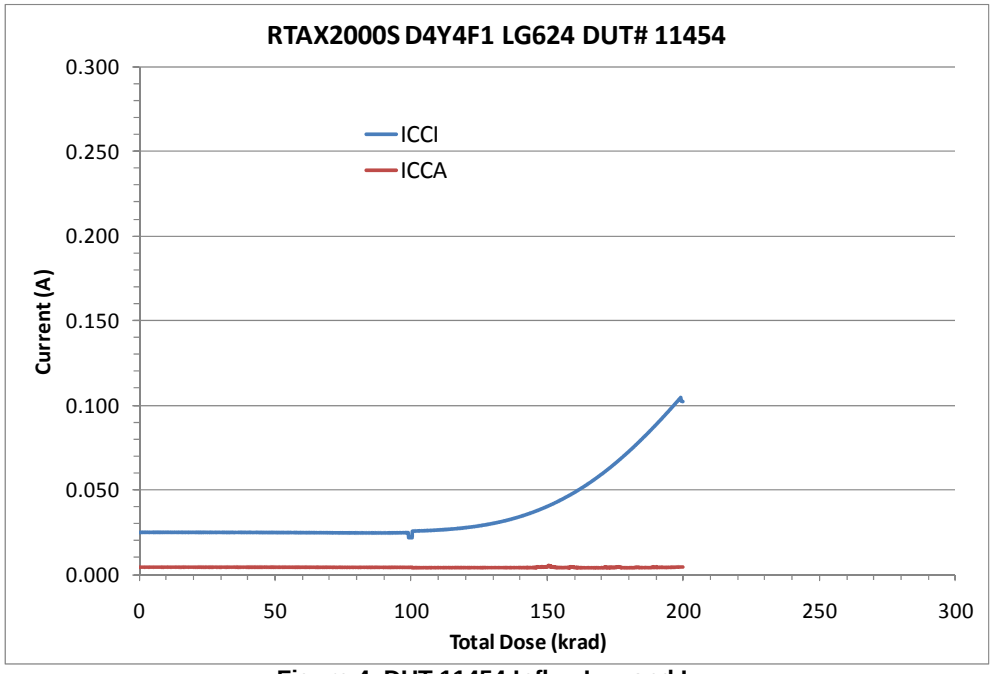

Figure 4 DUT 11454 Influx I_{CCA} and I_{CCI}

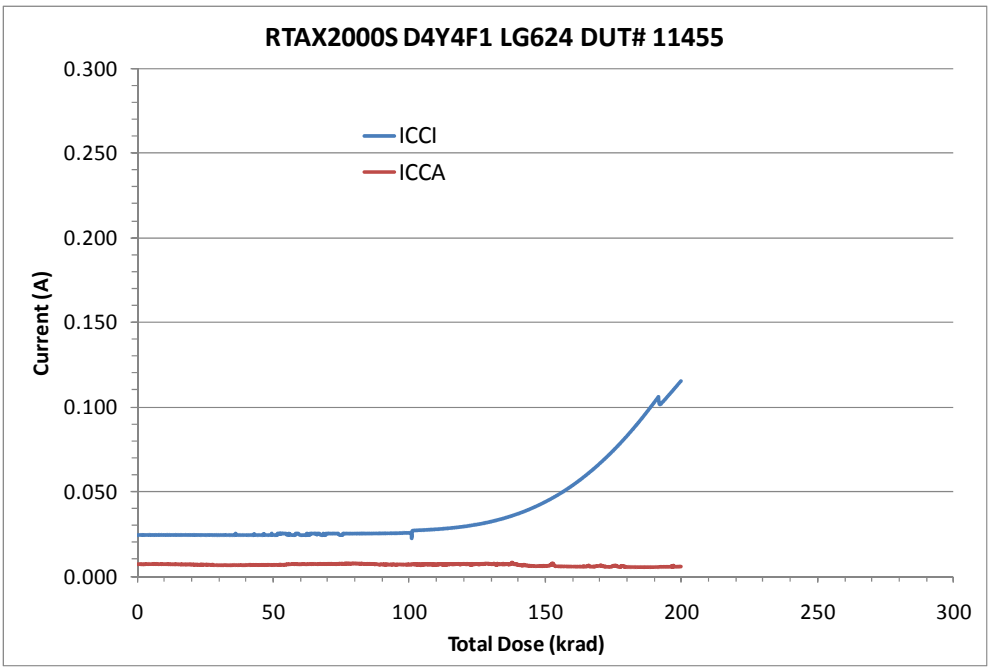

Figure 5 DUT 11455 Influx I_{CCA} and I_{CCI}

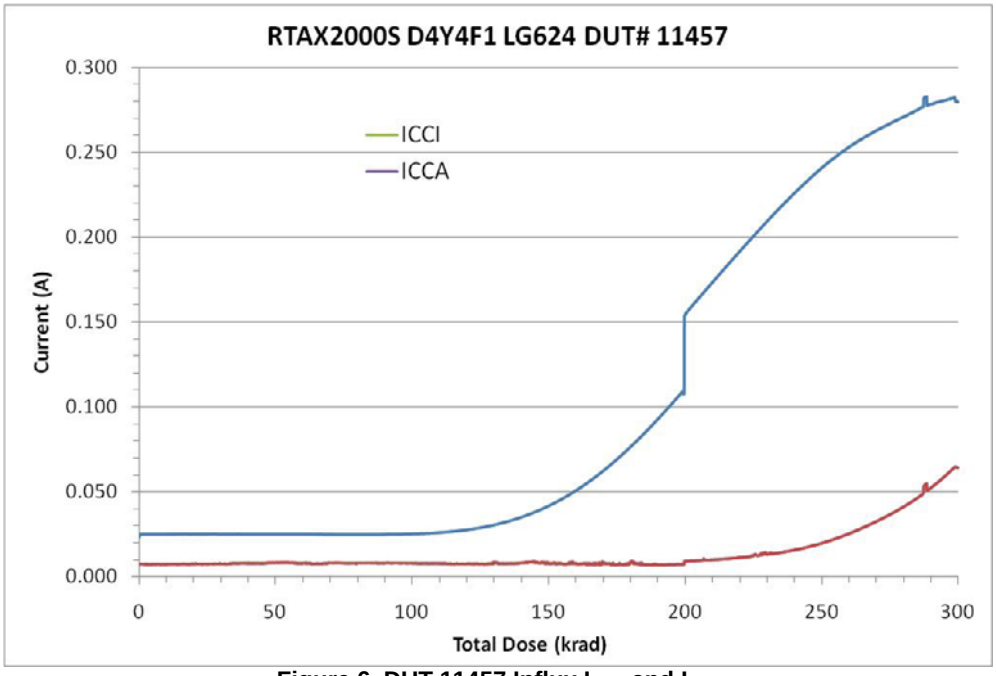

Figure 6 DUT 11457 Influx I_{CCA} and I_{CCI}

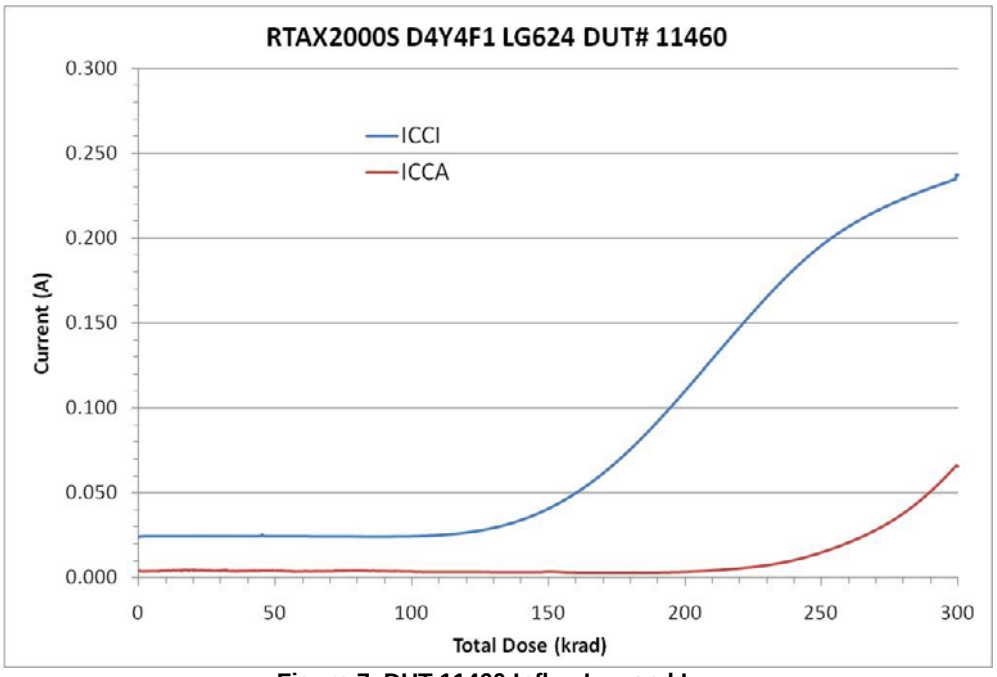

Figure 7 DUT 11460 Influx I_{CCA} and I_{CCI}

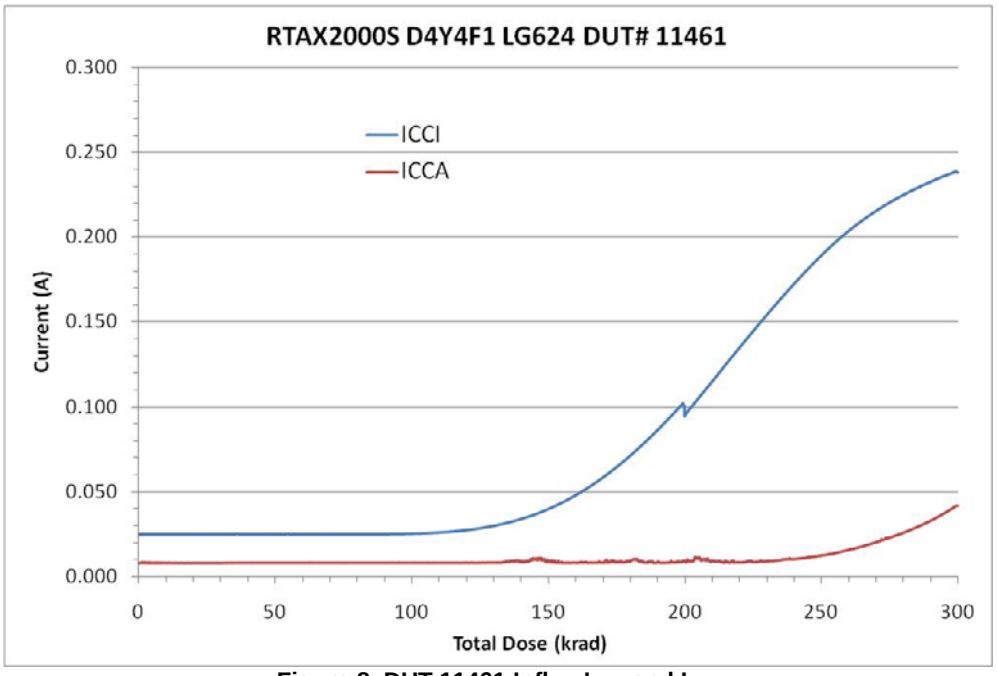

Figure 8 DUT 11461 Influx I_{CCA} and I_{CCI}

C. Single-Ended VIL / VIH and I_{IL} / I_{IH}

Table 3a and Table 3b display the pre-irradiation and post-annealing single-ended VIL; all data in these tables passes the specification. Table 4a and Table 4b display the pre-irradiation and post-annealing single-ended VIH; all data in these tables passes the specification.

Table 5a through Table 5d display the pre-irradiation and post-annealing single-ended I_{IL}; all data in these tables passes the specification. Table 6a through Table 6d display the pre-irradiation and post-annealing single-ended I_{IH}; all data in these tables passes the specification. The PIPL for both I_{IL} and I_{IH} is 5 µA.

Table 3a

DUT		11453		11454		11455	
Parameter (V)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_vil	Bi_D_7	1.380	1.365	1.380	1.370	1.385	1.370
bi_levels_vil	Bi_D_6	1.365	1.350	1.365	1.350	1.365	1.350
bi_levels_vil	Bi_D_5	1.375	1.360	1.375	1.360	1.375	1.360
bi_levels_vil	Bi_D_4	1.375	1.360	1.375	1.365	1.375	1.365
bi_levels_vil	Bi_D_3	1.370	1.360	1.370	1.365	1.375	1.370
bi_levels_vil	Bi_D_2	1.370	1.360	1.370	1.355	1.365	1.360
bi_levels_vil	Bi_D_1	1.370	1.355	1.370	1.350	1.365	1.360
bi_levels_vil	DA	1.385	1.360	1.385	1.365	1.385	1.365
bi_levels_vil	EN8	1.345	1.325	1.345	1.330	1.345	1.330
bi_levels_vil	IO_I_6	1.360	1.350	1.365	1.345	1.360	1.355
bi_levels_vil	IO_I_5	1.365	1.340	1.365	1.345	1.370	1.340
bi_levels_vil	IO_I_4	1.405	1.390	1.405	1.390	1.400	1.390
bi_levels_vil	IO_I_3	1.385	1.370	1.380	1.365	1.385	1.385
bi_levels_vil	IO_I_2	1.410	1.395	1.410	1.390	1.400	1.395
bi_levels_vil	IO_I_1	1.400	1.395	1.400	1.385	1.400	1.390
bi_levels_vil	RCLK1P	1.435	1.435	1.435	1.440	1.440	1.435
bi_levels_vil	RCLK2P	1.435	1.430	1.435	1.435	1.440	1.435

Table 3b

DUT		11457		11460		11461	
Parameter (V)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_vil	Bi_D_7	1.385	1.365	1.380	1.360	1.385	1.365
bi_levels_vil	Bi_D_6	1.365	1.350	1.360	1.340	1.365	1.345
bi_levels_vil	Bi_D_5	1.375	1.360	1.375	1.355	1.375	1.355
bi_levels_vil	Bi_D_4	1.380	1.360	1.375	1.360	1.380	1.360
bi_levels_vil	Bi_D_3	1.375	1.365	1.370	1.355	1.380	1.365
bi_levels_vil	Bi_D_2	1.370	1.355	1.370	1.355	1.370	1.355
bi_levels_vil	Bi_D_1	1.370	1.355	1.370	1.350	1.370	1.355
bi_levels_vil	DA	1.385	1.355	1.385	1.355	1.380	1.360
bi_levels_vil	EN8	1.345	1.325	1.340	1.320	1.355	1.330
bi_levels_vil	IO_I_6	1.360	1.345	1.355	1.340	1.365	1.350
bi_levels_vil	IO_I_5	1.355	1.335	1.370	1.355	1.355	1.335
bi_levels_vil	IO_I_4	1.400	1.390	1.410	1.390	1.410	1.390
bi_levels_vil	IO_I_3	1.400	1.365	1.385	1.375	1.390	1.385
bi_levels_vil	IO_I_2	1.405	1.390	1.405	1.390	1.415	1.390
bi_levels_vil	IO_I_1	1.400	1.385	1.410	1.385	1.410	1.395
bi_levels_vil	RCLK1P	1.445	1.440	1.435	1.430	1.440	1.440
bi_levels_vil	RCLK2P	1.445	1.440	1.435	1.430	1.440	1.435

Table 4a

DUT		11453		11454		11455	
Parameter (V)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_vih	Bi_D_7	1.380	1.365	1.380	1.370	1.380	1.370
bi_levels_vih	Bi_D_6	1.385	1.370	1.385	1.375	1.390	1.380
bi_levels_vih	Bi_D_5	1.385	1.370	1.385	1.370	1.385	1.370
bi_levels_vih	Bi_D_4	1.375	1.360	1.375	1.365	1.380	1.365
bi_levels_vih	Bi_D_3	1.390	1.375	1.390	1.375	1.390	1.380
bi_levels_vih	Bi_D_2	1.390	1.375	1.390	1.370	1.385	1.380
bi_levels_vih	Bi_D_1	1.385	1.370	1.385	1.370	1.380	1.380
bi_levels_vih	DA	1.410	1.395	1.410	1.400	1.415	1.405
bi_levels_vih	EN8	1.455	1.440	1.455	1.385	1.445	1.450
bi_levels_vih	IO_I_6	1.435	1.415	1.435	1.415	1.430	1.420
bi_levels_vih	IO_I_5	1.435	1.395	1.435	1.395	1.430	1.390
bi_levels_vih	IO_I_4	1.400	1.385	1.400	1.380	1.395	1.385
bi_levels_vih	IO_I_3	1.405	1.390	1.405	1.390	1.405	1.390
bi_levels_vih	IO_I_2	1.400	1.385	1.400	1.385	1.400	1.385
bi_levels_vih	IO_I_1	1.405	1.395	1.405	1.385	1.400	1.395
bi_levels_vih	RCLK1P	1.425	1.425	1.425	1.430	1.430	1.425
bi_levels_vih	RCLK2P	1.430	1.430	1.430	1.430	1.435	1.430

Table 4b

DUT		11457		11460		11461	
Parameter (V)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_vih	Bi_D_7	1.385	1.365	1.380	1.355	1.385	1.365
bi_levels_vih	Bi_D_6	1.395	1.375	1.385	1.365	1.395	1.375
bi_levels_vih	Bi_D_5	1.390	1.365	1.385	1.365	1.385	1.365
bi_levels_vih	Bi_D_4	1.380	1.365	1.380	1.360	1.380	1.360
bi_levels_vih	Bi_D_3	1.395	1.375	1.385	1.365	1.390	1.375
bi_levels_vih	Bi_D_2	1.390	1.370	1.390	1.375	1.395	1.370
bi_levels_vih	Bi_D_1	1.390	1.370	1.385	1.365	1.390	1.370
bi_levels_vih	DA	1.410	1.395	1.415	1.390	1.420	1.400
bi_levels_vih	EN8	1.460	1.440	1.400	1.430	1.475	1.450
bi_levels_vih	IO_I_6	1.430	1.400	1.435	1.410	1.435	1.415
bi_levels_vih	IO_I_5	1.430	1.415	1.445	1.395	1.440	1.415
bi_levels_vih	IO_I_4	1.400	1.380	1.400	1.385	1.400	1.385
bi_levels_vih	IO_I_3	1.405	1.390	1.415	1.400	1.415	1.395
bi_levels_vih	IO_I_2	1.400	1.380	1.405	1.385	1.405	1.390
bi_levels_vih	IO_I_1	1.400	1.385	1.410	1.395	1.415	1.390
bi_levels_vih	RCLK1P	1.435	1.430	1.425	1.420	1.430	1.430
bi_levels_vih	RCLK2P	1.435	1.435	1.430	1.430	1.435	1.430

Table 5a

DUT		11453		11454		11455	
Parameter (nA)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
IIL_Inputs_Max_	Bi_D_1	-4.933	< 1 uA	-3.886	< 1 uA	-3.676	-5.142
IIL_Inputs_Max_	Bi_D_2	-5.980	< 1 uA	-4.933	< 1 uA	-2.629	-4.723
IIL_Inputs_Max_	Bi_D_3	-4.304	< 1 uA	-1.372	< 1 uA	-3.886	-2.210
IIL_Inputs_Max_	Bi_D_4	-5.129	400.336	-5.339	517.620	-4.291	-4.920
IIL_Inputs_Max_	Bi_D_5	-1.778	411.436	-2.825	501.074	-2.616	-1.359
IIL_Inputs_Max_	Bi_D_6	-15.500	< 1 uA	-15.500	< 1 uA	-16.547	-14.244
IIL_Inputs_Max_	Bi_D_7	-6.119	-446.551	-6.119	-800.070	-4.863	-5.072
IIL_Inputs_Max_	Bi_E_1	-2.140	418.606	-2.978	542.588	-1.302	-1.093
IIL_Inputs_Max_	Bi_E_2	-0.883	438.292	-1.093	445.203	-1.931	-0.465
IIL_Inputs_Max_	Bi_E_3	-0.883	408.762	1.211	494.210	-0.674	-1.721
IIL_Inputs_Max_	Bi_E_4	-1.302	366.876	-1.512	454.628	-0.046	-1.302
IIL_Inputs_Max_	Bi_E_5	-2.350	472.848	-0.674	410.857	-0.674	-0.883
IIL_Inputs_Max_	Bi_E_6	-0.674	352.635	0.583	485.414	-1.512	-1.931
IIL_Inputs_Max_	Bi_E_7	-1.512	469.078	-1.302	465.309	-0.255	-1.931
IIL_Inputs_Max_	DA	-1.801	-2.638	-2.010	-0.963	-2.429	-2.848
IIL_Inputs_Max_	DIO_IN_1	-9.847	-9.428	-9.847	-11.313	-10.057	-7.963
IIL_Inputs_Max_	DIO_IN_2	-0.963	0.293	-0.126	1.969	-0.963	1.340
IIL_Inputs_Max_	DIO_IN_3	-0.335	0.293	0.084	-0.544	0.712	1.759
IIL_Inputs_Max_	DIO_IN_4	-7.963	-7.963	-7.963	-7.753	-9.010	-7.963
IIL_Inputs_Max_	DIO_IN_5	-0.335	0.503	-0.335	0.084	-0.126	-0.335
IIL_Inputs_Max_	DIO_IN_6	0.503	-0.544	-2.010	1.131	-0.544	-0.126
IIL_Inputs_Max_	DIO_IN_7	1.759	0.084	-0.335	-2.010	-0.544	-0.335
IIL_Inputs_Max_	DIO_IP_1	-9.010	-9.428	-8.172	-9.010	-8.172	-8.800
IIL_Inputs_Max_	DIO_IP_2	0.712	-1.173	-1.382	0.922	-0.544	-1.382
IIL_Inputs_Max_	DIO_IP_3	-6.288	-10.266	-7.335	-7.125	-7.125	-9.219
IIL_Inputs_Max_	DIO_IP_4	0.293	-0.963	-2.848	0.922	0.293	0.503
IIL_Inputs_Max_	DIO_IP_5	-1.382	-1.173	-1.173	-0.963	-0.126	0.084
IIL_Inputs_Max_	DIO_IP_6	0.293	-0.754	0.084	-0.544	-0.126	0.712
IIL_Inputs_Max_	DIO_IP_7	0.922	-0.335	-0.126	-0.544	-1.591	0.084
IIL_Inputs_Max_	EN8	0.084	-0.335	-1.591	-0.335	1.340	-0.544
IIL_Inputs_Max_	HCLK1P	-0.255	-1.721	-1.302	-1.512	-0.674	-1.721
IIL_Inputs_Max_	HCLK2P	-9.847	-10.057	-9.010	-7.963	-6.497	-8.382
IIL_Inputs_Max_	HCLK3P	-3.048	-4.304	-2.001	-1.791	-2.419	-4.095
IIL_Inputs_Max_	HCLK4P	-1.569	-1.569	-1.359	-2.825	-1.150	-0.521
IIL_Inputs_Max_	IO_I_1	-8.800	-7.544	-9.638	-8.172	-6.497	-9.010
IIL_Inputs_Max_	IO_I_2	-2.838	-2.629	-4.304	-6.189	-3.886	-5.980
IIL_Inputs_Max_	IO_I_3	-7.335	-9.428	-8.172	-8.172	-7.753	-6.916
IIL_Inputs_Max_	IO_I_4	-4.514	-7.446	-2.419	-8.703	-3.886	-5.142
IIL_Inputs_Max_	IO_I_5	-6.916	-7.753	-7.125	-7.125	-8.172	-6.707
IIL_Inputs_Max_	IO_I_6	0.712	0.084	0.503	0.503	1.340	1.131

Table 5a

IIL_Inputs_Max_	LOADIN	-3.024	-4.491	-3.862	-2.186	-1.349	0.327
IIL_Inputs_Max_	RCLK1P	-7.544	520.702	-7.335	526.774	-7.963	-9.010
IIL_Inputs_Max_	RCLK2P	-1.150	476.152	-0.940	448.716	-3.663	-0.940
IIL_Inputs_Max_	RCLK3P	-1.791	-3.257	-1.582	-1.372	-4.095	-3.676
IIL_Inputs_Max_	RCLK4P	-2.978	-0.674	-0.674	-0.674	-0.883	-1.512

Table 5b

DUT		11457		11460		11461	
Parameter (nA)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
IIL_Inputs_Max_	Bi_D_1	-4.514	< 1 uA	-3.676	< 1 uA	-3.048	< 1 uA
IIL_Inputs_Max_	Bi_D_2	-1.582	< 1 uA	-2.210	< 1 uA	-3.676	< 1 uA
IIL_Inputs_Max_	Bi_D_3	-2.629	< 1 uA	-2.629	< 1 uA	-3.676	< 1 uA
IIL_Inputs_Max_	Bi_D_4	-2.406	321.798	-4.082	402.012	-5.548	288.498
IIL_Inputs_Max_	Bi_D_5	-2.616	439.710	-0.312	451.857	-1.569	434.055
IIL_Inputs_Max_	Bi_D_6	-16.338	< 1 uA	-15.081	< 1 uA	-14.663	-910.147
IIL_Inputs_Max_	Bi_D_7	-2.140	177.342	-4.025	-88.844	-3.816	132.314
IIL_Inputs_Max_	Bi_E_1	-0.674	560.809	-0.255	464.471	-2.140	469.916
IIL_Inputs_Max_	Bi_E_2	-0.674	340.488	-2.350	472.010	-0.674	388.448
IIL_Inputs_Max_	Bi_E_3	-1.302	512.849	-2.350	584.056	-2.978	373.369
IIL_Inputs_Max_	Bi_E_4	-1.721	494.210	0.583	525.415	-2.350	356.195
IIL_Inputs_Max_	Bi_E_5	1.420	357.661	1.420	518.923	-2.140	345.096
IIL_Inputs_Max_	Bi_E_6	-1.931	412.323	-0.883	594.946	-1.512	363.316
IIL_Inputs_Max_	Bi_E_7	-1.093	371.903	-3.397	529.813	-0.883	411.066
IIL_Inputs_Max_	DA	-3.057	-0.963	-1.382	-2.638	-2.010	-2.848
IIL_Inputs_Max_	DIO_IN_1	-9.010	-10.057	-9.428	-10.266	-11.313	-11.103
IIL_Inputs_Max_	DIO_IN_2	1.550	0.293	0.084	-1.591	0.084	0.084
IIL_Inputs_Max_	DIO_IN_3	-1.173	0.293	-0.335	-1.591	1.131	-2.010
IIL_Inputs_Max_	DIO_IN_4	-6.916	-9.010	-7.335	-9.638	-7.753	-9.219
IIL_Inputs_Max_	DIO_IN_5	-1.382	0.922	1.550	-0.335	0.503	1.131
IIL_Inputs_Max_	DIO_IN_6	-1.173	0.084	1.131	0.712	0.293	0.293
IIL_Inputs_Max_	DIO_IN_7	0.503	0.922	0.503	-0.126	0.293	3.016
IIL_Inputs_Max_	DIO_IP_1	-10.475	-7.753	-6.497	-6.288	-9.219	-7.544
IIL_Inputs_Max_	DIO_IP_2	-0.126	0.922	1.131	-0.335	-0.335	0.922
IIL_Inputs_Max_	DIO_IP_3	-7.335	-8.172	-7.125	-7.544	-6.916	-8.172
IIL_Inputs_Max_	DIO_IP_4	-0.126	0.712	0.503	-0.126	1.550	0.084
IIL_Inputs_Max_	DIO_IP_5	1.340	2.178	1.550	-1.382	0.293	1.131
IIL_Inputs_Max_	DIO_IP_6	-0.335	-0.126	0.084	-1.173	1.969	-0.963
IIL_Inputs_Max_	DIO_IP_7	-0.754	0.293	0.293	0.084	1.340	0.712
IIL_Inputs_Max_	EN8	0.503	-1.801	-0.335	-1.382	0.922	2.597
IIL_Inputs_Max_	HCLK1P	-0.883	-0.674	-1.302	-0.046	-0.046	-2.559
IIL_Inputs_Max_	HCLK2P	-7.963	-6.707	-5.032	-8.382	-7.753	-9.010
IIL_Inputs_Max_	HCLK3P	-3.048	-3.257	-2.001	-4.933	-2.419	-2.838

Table 5b

IIL_Inputs_Max_	HCLK4P	-2.825	-1.359	-0.312	-3.244	-0.103	-1.778
IIL_Inputs_Max_	IO_I_1	-6.288	-7.335	-9.219	-8.800	-8.382	-6.916
IIL_Inputs_Max_	IO_I_2	-3.467	-5.771	-2.838	-5.352	-4.095	-3.257
IIL_Inputs_Max_	IO_I_3	-9.847	-9.219	-7.335	-9.638	-6.288	-7.544
IIL_Inputs_Max_	IO_I_4	-1.791	-9.960	-2.001	-7.656	-2.419	-13.730
IIL_Inputs_Max_	IO_I_5	-7.125	-8.382	-7.125	-6.707	-7.963	-7.753
IIL_Inputs_Max_	IO_I_6	0.503	-1.591	1.131	-1.173	-0.126	0.084
IIL_Inputs_Max_	LOADIN	-2.186	-1.977	-4.909	-2.186	-3.862	-1.139
IIL_Inputs_Max_	RCLK1P	-9.428	503.115	-7.335	549.176	-5.869	287.671
IIL_Inputs_Max_	RCLK2P	-2.197	433.008	-0.312	563.486	-1.150	362.010
IIL_Inputs_Max_	RCLK3P	-1.372	-4.514	-2.629	-3.257	-2.838	-3.886
IIL_Inputs_Max_	RCLK4P	-1.931	-0.883	-0.465	-0.255	-1.721	-1.512

Table 5c

DUT		11453		11454		11455	
Parameter (nA)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
IIL_BiOuts_Max_	Bi_IO_1	-12.360	381.679	-10.057	340.223	-12.150	324.311
IIL_BiOuts_Max_	Bi_IO_2	-4.082	-573.535	-4.710	-176.237	-3.663	< 1 uA
IIL_BiOuts_Max_	Bi_IO_3	-4.291	281.587	-3.663	307.766	-1.150	266.508
IIL_BiOuts_Max_	Bi_IO_4	-8.172	< 1 uA	-8.800	< 1 uA	-10.057	< 1 uA
IIL_BiOuts_Max_	Bi_IO_5	-2.197	< 1 uA	-2.406	< 1 uA	-1.988	< 1 uA
IIL_BiOuts_Max_	Bi_IO_6	-2.186	-15.383	-0.511	-93.933	-1.139	22.531
IIL_BiOuts_Max_	Bi_IO_7	-1.767	-0.720	-0.092	-1.558	-5.747	-0.092

Table 5d

DUT		11457		11460		11461	
Parameter (nA)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
IIL_BiOuts_Max_	Bi_IO_1	-11.103	375.816	-12.988	413.503	-11.522	354.879
IIL_BiOuts_Max_	Bi_IO_2	-6.386	< 1 uA	-6.386	-180.426	-5.548	< 1 uA
IIL_BiOuts_Max_	Bi_IO_3	-2.197	290.802	-2.406	311.327	-1.359	262.528
IIL_BiOuts_Max_	Bi_IO_4	-8.591	< 1 uA	-9.428	< 1 uA	-9.010	< 1 uA
IIL_BiOuts_Max_	Bi_IO_5	-1.359	< 1 uA	0.316	< 1 uA	-1.778	< 1 uA
IIL_BiOuts_Max_	Bi_IO_6	-1.139	-4.909	0.118	-560.837	-0.720	21.693
IIL_BiOuts_Max_	Bi_IO_7	-1.977	195.970	-2.396	272.007	1.794	-3.024

Table 6a

DUT		11453		11454		11455	
Parameter (nA)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
IIH_Inputs_Max_	Bi_D_1	1.560	< 1 uA	1.979	< 1 uA	1.560	0.303
IIH_Inputs_Max_	Bi_D_2	-0.116	< 1 uA	0.094	< 1 uA	2.817	-2.001
IIH_Inputs_Max_	Bi_D_3	-0.744	< 1 uA	-1.582	< 1 uA	1.351	-1.791
IIH_Inputs_Max_	Bi_D_4	4.714	562.020	6.809	676.790	3.877	3.667
IIH_Inputs_Max_	Bi_D_5	1.154	595.111	1.154	689.984	1.363	1.992
IIH_Inputs_Max_	Bi_D_6	-3.566	< 1 uA	-1.682	< 1 uA	-4.194	-2.938
IIH_Inputs_Max_	Bi_D_7	1.630	740.500	4.143	932.757	2.467	2.886
IIH_Inputs_Max_	Bi_E_1	0.373	642.068	1.001	794.743	1.420	-0.255
IIH_Inputs_Max_	Bi_E_2	1.211	487.089	-1.302	434.104	-1.302	-0.046
IIH_Inputs_Max_	Bi_E_3	-0.465	392.636	-0.046	428.239	-0.465	-1.931
IIH_Inputs_Max_	Bi_E_4	-2.140	771.915	-0.465	929.825	-1.721	-0.674
IIH_Inputs_Max_	Bi_E_5	-1.931	409.810	0.373	352.216	-1.721	-1.093
IIH_Inputs_Max_	Bi_E_6	1.420	321.221	-0.465	340.698	0.583	-1.931
IIH_Inputs_Max_	Bi_E_7	-0.255	349.913	-0.255	1.001	-1.512	-0.465
IIH_Inputs_Max_	DA	4.481	4.481	6.575	4.272	3.644	3.644
IIH_Inputs_Max_	DIO_IN_1	-5.450	-7.335	-4.194	-3.985	-2.729	-6.078
IIH_Inputs_Max_	DIO_IN_2	2.178	2.597	-0.754	2.178	4.063	2.806
IIH_Inputs_Max_	DIO_IN_3	2.597	4.481	2.178	3.853	2.178	2.806
IIH_Inputs_Max_	DIO_IN_4	-3.775	-6.497	-7.335	-4.822	-5.869	-7.544
IIH_Inputs_Max_	DIO_IN_5	3.225	3.644	1.969	6.575	2.178	2.806
IIH_Inputs_Max_	DIO_IN_6	0.712	1.550	1.550	2.178	1.550	3.016
IIH_Inputs_Max_	DIO_IN_7	3.644	4.063	0.922	0.712	0.503	2.597
IIH_Inputs_Max_	DIO_IP_1	-7.125	-6.707	-5.660	-8.382	-5.450	-7.963
IIH_Inputs_Max_	DIO_IP_2	1.131	3.853	1.759	2.806	0.503	1.550
IIH_Inputs_Max_	DIO_IP_3	-7.544	-7.963	-6.078	-6.916	-7.125	-5.032
IIH_Inputs_Max_	DIO_IP_4	1.340	4.063	2.597	0.922	0.712	1.131
IIH_Inputs_Max_	DIO_IP_5	-0.335	1.759	3.853	2.597	2.387	2.387
IIH_Inputs_Max_	DIO_IP_6	3.644	2.387	2.597	3.016	1.550	1.969
IIH_Inputs_Max_	DIO_IP_7	2.387	1.759	1.969	3.225	2.806	2.597
IIH_Inputs_Max_	EN8	2.806	2.387	1.969	0.293	2.178	1.550
IIH_Inputs_Max_	HCLK1P	-1.093	-1.721	-1.093	-1.093	-0.883	-1.512
IIH_Inputs_Max_	HCLK2P	-6.497	-5.869	-4.822	-5.660	-6.497	-6.497
IIH_Inputs_Max_	HCLK3P	-0.744	1.351	-1.372	-3.048	-0.325	-2.629
IIH_Inputs_Max_	HCLK4P	-0.731	0.735	0.107	1.154	1.154	0.526
IIH_Inputs_Max_	IO_I_1	-4.403	-3.566	-6.916	-7.125	-4.613	-6.078
IIH_Inputs_Max_	IO_I_2	-0.325	0.094	0.303	2.398	-2.629	-3.886
IIH_Inputs_Max_	IO_I_3	-6.078	-6.916	-6.497	-7.125	-6.497	-6.078
IIH_Inputs_Max_	IO_I_4	-1.582	9.938	-0.953	1.141	-2.419	-3.676
IIH_Inputs_Max_	IO_I_5	-6.078	-6.288	-5.660	-7.544	-6.078	-6.078
IIH_Inputs_Max_	IO_I_6	2.387	0.922	1.969	1.969	4.691	0.922

Table 6a

IIH_Inputs_Max_	LOADIN	3.679	3.260	4.726	4.098	1.375	4.307
IIH_Inputs_Max_	RCLK1P	-6.916	917.462	-7.125	881.240	-8.800	-6.288
IIH_Inputs_Max_	RCLK2P	-0.940	462.120	1.154	371.644	2.620	2.411
IIH_Inputs_Max_	RCLK3P	-0.116	-0.744	-2.419	-0.953	-1.372	-3.257
IIH_Inputs_Max_	RCLK4P	-1.093	0.164	1.420	-0.046	-0.883	-0.674

Table 6b

DUT		11457		11460		11461	
Parameter (nA)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
IIH_Inputs_Max_	Bi_D_1	-0.116	< 1 uA	-0.116	< 1 uA	0.303	< 1 uA
IIH_Inputs_Max_	Bi_D_2	-1.163	< 1 uA	1.351	< 1 uA	-1.163	< 1 uA
IIH_Inputs_Max_	Bi_D_3	1.141	< 1 uA	0.932	< 1 uA	-0.744	< 1 uA
IIH_Inputs_Max_	Bi_D_4	3.877	655.428	3.877	773.549	4.505	500.865
IIH_Inputs_Max_	Bi_D_5	1.363	581.707	3.667	787.790	3.667	720.352
IIH_Inputs_Max_	Bi_D_6	-3.357	< 1 uA	-4.194	< 1 uA	-3.357	954.102
IIH_Inputs_Max_	Bi_D_7	5.190	930.454	2.049	< 1 uA	2.677	704.688
IIH_Inputs_Max_	Bi_E_1	3.724	741.757	2.049	834.535	-0.674	814.220
IIH_Inputs_Max_	Bi_E_2	-0.465	450.649	-1.302	428.030	-1.512	385.306
IIH_Inputs_Max_	Bi_E_3	1.211	359.127	1.839	444.575	0.164	346.352
IIH_Inputs_Max_	Bi_E_4	-1.093	882.913	-0.883	927.522	-1.512	613.795
IIH_Inputs_Max_	Bi_E_5	0.583	373.369	1.001	372.740	-0.465	325.200
IIH_Inputs_Max_	Bi_E_6	2.677	228.024	-1.512	345.514	-0.255	221.113
IIH_Inputs_Max_	Bi_E_7	-3.397	351.588	-0.883	406.249	-0.255	-0.046
IIH_Inputs_Max_	DA	3.434	4.900	3.644	5.319	4.272	4.063
IIH_Inputs_Max_	DIO_IN_1	-1.682	-4.403	-5.032	-5.660	-6.916	-5.660
IIH_Inputs_Max_	DIO_IN_2	2.178	0.712	0.084	4.272	0.084	4.272
IIH_Inputs_Max_	DIO_IN_3	2.597	2.597	0.922	1.969	3.225	1.550
IIH_Inputs_Max_	DIO_IN_4	-6.288	-3.775	-7.753	-3.775	-8.172	-6.078
IIH_Inputs_Max_	DIO_IN_5	5.528	2.806	3.225	1.759	3.434	1.340
IIH_Inputs_Max_	DIO_IN_6	2.387	1.759	1.969	2.178	2.597	3.016
IIH_Inputs_Max_	DIO_IN_7	0.293	4.900	1.969	3.225	2.806	3.016
IIH_Inputs_Max_	DIO_IP_1	-5.241	-8.800	-7.125	-6.707	-6.078	-7.963
IIH_Inputs_Max_	DIO_IP_2	4.900	0.293	1.340	-0.544	3.434	0.922
IIH_Inputs_Max_	DIO_IP_3	-5.660	-5.660	-5.241	-5.869	-6.497	-6.497
IIH_Inputs_Max_	DIO_IP_4	2.387	3.225	0.712	1.759	2.387	1.550
IIH_Inputs_Max_	DIO_IP_5	0.293	1.969	1.131	1.759	3.434	0.293
IIH_Inputs_Max_	DIO_IP_6	0.922	2.178	2.597	1.759	1.550	-0.126
IIH_Inputs_Max_	DIO_IP_7	2.387	3.016	1.969	5.319	3.644	3.853
IIH_Inputs_Max_	EN8	2.178	1.969	0.712	3.225	1.969	2.387
IIH_Inputs_Max_	HCLK1P	-3.187	1.630	-0.674	-1.721	-0.465	-1.302
IIH_Inputs_Max_	HCLK2P	-7.125	-4.822	-5.869	-7.335	-6.288	-7.335
IIH_Inputs_Max_	HCLK3P	-0.534	-0.534	-2.001	0.303	-0.116	-3.257

Table 6b

IIH_Inputs_Max_	HCLK4P	-0.731	1.154	0.526	0.945	0.735	3.667
IIH_Inputs_Max_	IO_I_1	-6.707	-6.916	-6.288	-7.544	-7.335	-7.963
IIH_Inputs_Max_	IO_I_2	0.932	1.560	-1.582	0.722	-1.163	-0.116
IIH_Inputs_Max_	IO_I_3	-5.241	-7.544	-7.125	-7.963	-5.660	-8.172
IIH_Inputs_Max_	IO_I_4	-1.791	2.188	0.303	14.755	-0.534	17.268
IIH_Inputs_Max_	IO_I_5	-5.869	-5.241	-5.032	-6.078	-4.613	-5.660
IIH_Inputs_Max_	IO_I_6	-0.963	-0.335	1.340	-0.544	3.016	1.340
IIH_Inputs_Max_	LOADIN	3.888	3.679	1.794	3.469	2.631	4.936
IIH_Inputs_Max_	RCLK1P	-6.707	851.719	-5.660	< 1 uA	-6.078	488.877
IIH_Inputs_Max_	RCLK2P	0.735	301.902	3.039	474.057	1.573	339.391
IIH_Inputs_Max_	RCLK3P	-1.163	-1.582	-2.210	-1.791	-1.163	-3.257
IIH_Inputs_Max_	RCLK4P	-2.350	0.583	0.583	-3.816	-1.093	2.049

Table 6c

DUT		**11453**		**11454**		**11455**	
Parameter (nA)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
IIH_BiOuts_Max_	**Bi_IO_1**	**-4.613**	**233.234**	**-6.707**	**167.491**	**-7.963**	**248.309**
IIH_BiOuts_Max_	**Bi_IO_2**	**-0.312**	**< 1 uA**	**-0.521**	**< 1 uA**	**1.782**	**< 1 uA**
IIH_BiOuts_Max_	**Bi_IO_3**	**-0.103**	**194.462**	**-0.940**	**187.970**	**0.316**	**273.419**
IIH_BiOuts_Max_	**Bi_IO_4**	**-8.382**	**< 1 uA**	**-7.544**	**< 1 uA**	**-6.916**	**< 1 uA**
IIH_BiOuts_Max_	**Bi_IO_5**	**0.735**	**< 1 uA**	**< 1 uA**	**< 1 uA**	**-0.103**	**< 1 uA**
IIH_BiOuts_Max_	**Bi_IO_6**	**-3.234**	**< 1 uA**	**< 1 uA**	**< 1 uA**	**-0.511**	**583.905**
IIH_BiOuts_Max_	**Bi_IO_7**	**-0.301**	**< 1 uA**	**2.970**	**< 1 uA**	**-1.558**	**< 1 uA**

Table 6d

DUT		**11457**		**11460**		**11461**	
Parameter (nA)	**Design**	**Pre-Irrad**	**Post-Ann**	**Pre-Irrad**	**Post-Ann**	**Pre-Irrad**	**Post-Ann**
IIH_BiOuts_Max_	Bi_IO_1	-7.753	258.568	-8.172	211.040	-5.450	275.946
IIH_BiOuts_Max_	Bi_IO_2	-0.312	< 1 uA	-1.150	< 1 uA	0.526	< 1 uA
IIH_BiOuts_Max_	Bi_IO_3	-0.940	268.602	0.107	197.394	0.107	356.774
IIH_BiOuts_Max_	Bi_IO_4	-6.078	< 1 uA	-6.707	< 1 uA	-8.172	< 1 uA
IIH_BiOuts_Max_	Bi_IO_5	0.107	< 1 uA	0.735	< 1 uA	1.154	< 1 uA
IIH_BiOuts_Max_	Bi_IO_6	-0.092	< 1 uA	-0.720	< 1 uA	-0.720	925.547
IIH_BiOuts_Max_	Bi_IO_7	-0.930	< 1 uA	-1.558	< 1 uA	-1.349	< 1 uA

D. Differential Input (LVPECL) Threshold Voltage (VIL/VIH)

Table 7a through and 8b show the pre-irradiation and post-annealing threshold-voltages of the LVPECL input. All data passes the specification.

Table 7a

DUT		11453		11454		11455	
Parameter (mV)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_vil	DIO_IP_7	100	95	100	95	95	115
bi_levels_vil	DIO_IP_6	100	100	100	110	110	110
bi_levels_vil	DIO_IP_5	120	120	120	110	110	110
bi_levels_vil	DIO_IP_4	100	100	100	95	95	85
bi_levels_vil	DIO_IP_3	90	90	90	85	85	80
bi_levels_vil	DIO_IP_2	85	85	85	90	90	100
bi_levels_vil	DIO_IP_1	75	75	75	85	80	75

Table7b

DUT		11457		11460		11461	
Parameter (mV)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_vil	DIO_IP_7	105	110	95	100	105	105
bi_levels_vil	DIO_IP_6	100	100	105	105	105	110
bi_levels_vil	DIO_IP_5	105	110	110	110	105	105
bi_levels_vil	DIO_IP_4	100	100	95	95	100	100
bi_levels_vil	DIO_IP_3	95	95	95	95	90	90
bi_levels_vil	DIO_IP_2	85	85	90	90	85	85
bi_levels_vil	DIO_IP_1	80	80	80	80	90	95

Table 8a

DUT		11453		11454		11455	
Parameter (mV)	**Design**	**Pre-Irrad**	**Post-Ann**	**Pre-Irrad**	**Post-Ann**	**Pre-Irrad**	**Post-Ann**
bi_levels_vih	DIO_IP_7	95	95	95	95	95	115
bi_levels_vih	DIO_IP_6	95	100	95	110	105	110
bi_levels_vih	DIO_IP_5	115	120	115	110	105	110
bi_levels_vih	DIO_IP_4	100	100	100	95	90	85
bi_levels_vih	DIO_IP_3	85	90	85	85	80	80
bi_levels_vih	DIO_IP_2	85	85	85	90	90	100
bi_levels_vih	DIO_IP_1	75	75	75	85	85	75

Table 8b

DUT		11457		11460		11461	
Parameter (mV)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_vih	DIO_IP_7	100	110	90	100	100	105
bi_levels_vih	DIO_IP_6	95	100	105	105	105	110
bi_levels_vih	DIO_IP_5	105	110	110	110	100	105
bi_levels_vih	DIO_IP_4	95	100	90	95	95	100
bi_levels_vih	DIO_IP_3	95	95	90	95	85	90
bi_levels_vih	DIO_IP_2	80	85	85	90	85	85
bi_levels_vih	DIO_IP_1	85	80	85	80	100	95

E. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Table 9a through 10b. All post-annealing data passes the specification.

Table 9a

DUT		11453		11454		11455	
Parameter (mV)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_vol	Bi_IO_7	35	35	35	35	35	35
bi_levels_vol	Bi_IO_6	30	30	30	35	30	30
bi_levels_vol	Bi_IO_5	35	35	35	35	35	35
bi_levels_vol	Bi_IO_4	35	30	35	35	35	35
bi_levels_vol	Bi_IO_3	35	30	30	35	35	35
bi_levels_vol	Bi_IO_2	35	35	35	35	35	35
bi_levels_vol	Bi_IO_1	35	30	35	35	35	35
bi_levels_vol	Bi_Y_7	25	25	25	25	25	25
bi_levels_vol	Bi_Y_6	25	25	25	25	25	25
bi_levels_vol	Bi_Y_5	25	25	25	25	25	25
bi_levels_vol	Bi_Y_4	25	25	25	25	25	25
bi_levels_vol	Bi_Y_3	25	25	25	25	25	25
bi_levels_vol	Bi_Y_2	25	25	25	25	25	25
bi_levels_vol	Bi_Y_1	25	25	25	25	25	25
bi_levels_vol	CLOCKE_OUT	20	20	20	20	20	20
bi_levels_vol	CLOCKF_OUT	20	20	20	20	20	20
bi_levels_vol	QA_2	20	20	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20	20	20
bi_levels_vol	QA_0	0	0	0	0	0	0

Table 9b

DUT		11457		11460		11461	
Parameter (mV)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_vol	Bi_IO_7	35	35	35	35	35	35
bi_levels_vol	Bi_IO_6	30	30	30	30	30	30
bi_levels_vol	Bi_IO_5	35	35	35	35	35	35
bi_levels_vol	Bi_IO_4	35	35	30	35	35	35
bi_levels_vol	Bi_IO_3	35	35	35	35	35	35
bi_levels_vol	Bi_IO_2	30	35	35	35	35	35
bi_levels_vol	Bi_IO_1	35	35	35	35	35	35
bi_levels_vol	Bi_Y_7	25	25	25	25	25	25
bi_levels_vol	Bi_Y_6	25	25	25	25	25	25
bi_levels_vol	Bi_Y_5	25	25	25	25	25	25
bi_levels_vol	Bi_Y_4	25	25	25	25	25	25
bi_levels_vol	Bi_Y_3	25	25	25	25	25	25
bi_levels_vol	Bi_Y_2	25	25	25	25	25	25
bi_levels_vol	Bi_Y_1	25	25	25	25	25	25
bi_levels_vol	CLOCKE_OUT	20	20	20	20	20	20
bi_levels_vol	CLOCKF_OUT	25	20	25	25	20	20
bi_levels_vol	QA_2	0	20	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20	20	20
bi_levels_vol	QA_0	0	0	0	0	0	0

Table 10a

DUT		11453		11454		11455	
Parameter (V)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_voh	Bi_IO_7	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_IO_6	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_5	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_IO_4	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_IO_3	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_IO_2	2.970	2.965	2.970	2.965	2.970	2.970
bi_levels_voh	Bi_IO_1	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_Y_7	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_6	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_5	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_4	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_3	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_2	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_1	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	CLOCKE_OUT	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	CLOCKF_OUT	2.970	2.970	2.975	2.970	2.975	2.970
bi_levels_voh	QA_2	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	QA_1	2.975	2.970	2.975	2.970	2.975	2.970
bi_levels_voh	QA_0	2.970	2.975	2.970	2.970	2.970	2.975

Table 10b

DUT		11457		11460		11461	
Parameter (V)	**Design**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**	**Pre-Irrad.**	**Post-Ann.**
bi_levels_voh	Bi_IO_7	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_IO_6	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_5	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_IO_4	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_IO_3	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_IO_2	2.970	2.970	2.970	2.965	2.970	2.970
bi_levels_voh	Bi_IO_1	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	Bi_Y_7	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_6	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_5	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_4	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_3	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_2	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	Bi_Y_1	2.985	2.985	2.985	2.985	2.985	2.985
bi_levels_voh	CLOCKE_OUT	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	CLOCKF_OUT	2.975	2.970	2.975	2.970	2.970	2.970
bi_levels_voh	QA_2	2.970	2.970	2.970	2.970	2.970	2.970
bi_levels_voh	QA_1	2.975	2.970	2.975	2.970	2.970	2.970
bi_levels_voh	QA_0	2.970	2.970	2.970	2.970	2.970	2.970

F. Propagation Delay

Table 11 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case the percentage change is well below ±10%.

Table 11 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation (µs)	Post-Irradiation (µs)	Post-Annealing (µs)	Post-Irradiation Degradation (%)	Post-Annealing Degradation (%)
11453	200 krad	7.031	7.000	7.134	-0.4%	1.5%
11454	200 krad	7.008	6.975	6.993	-0.5%	-0.2%
11455	200 krad	6.837	6.821	6.833	-0.2%	-0.1%
11457	300 krad	6.923	7.163	7.020	3.5%	1.4%
11460	300 krad	7.140	7.440	7.255	4.2%	1.6%
11461	300 krad	6.766	6.915	6.846	2.2%	1.2%

G. Transition Characteristic

Figure 9a through Figure 20b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

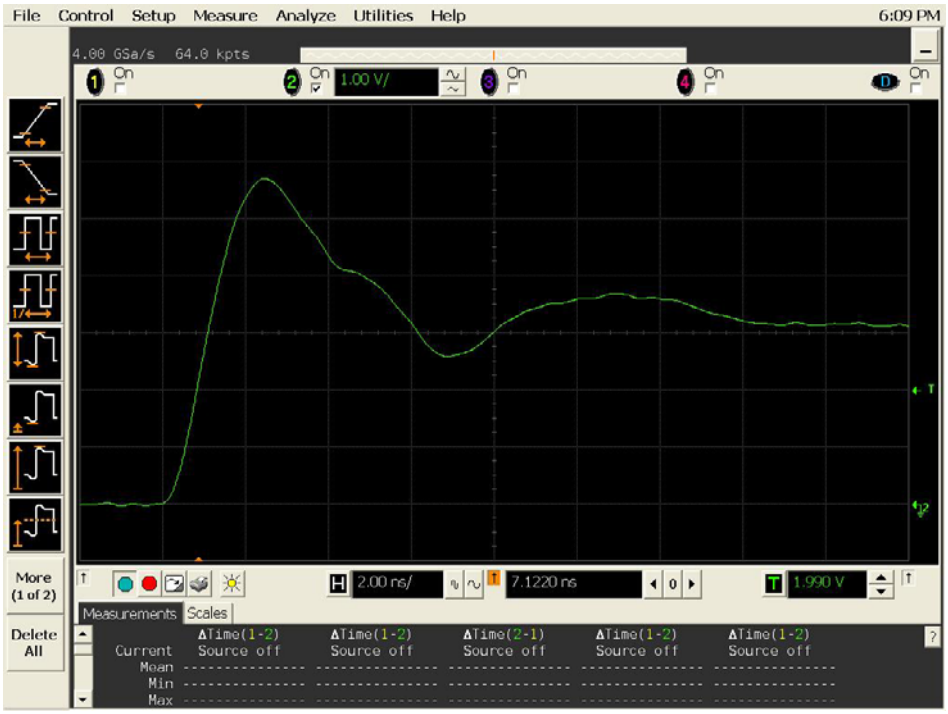

Figure 9a DUT 11453 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

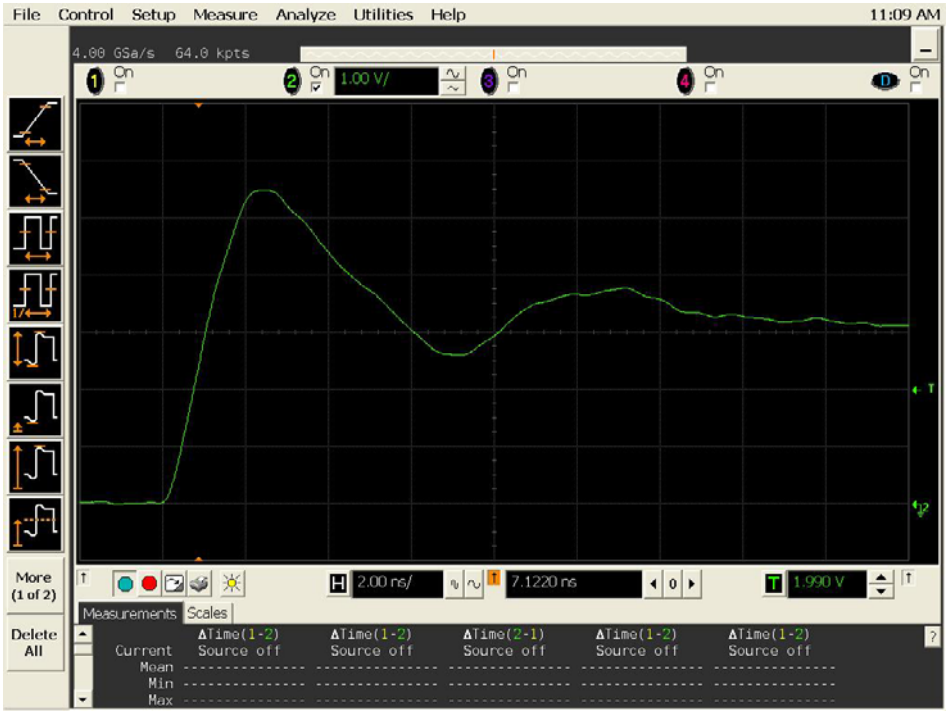

Figure 9b DUT 11453 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

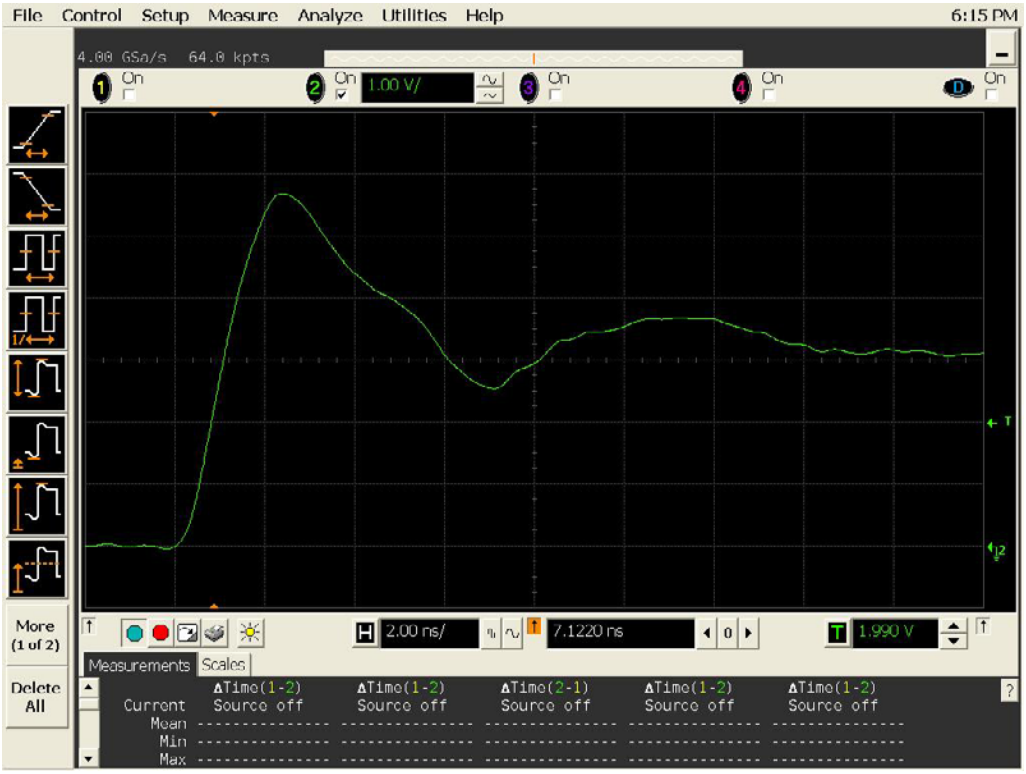

Figure 10a DUT 11454 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

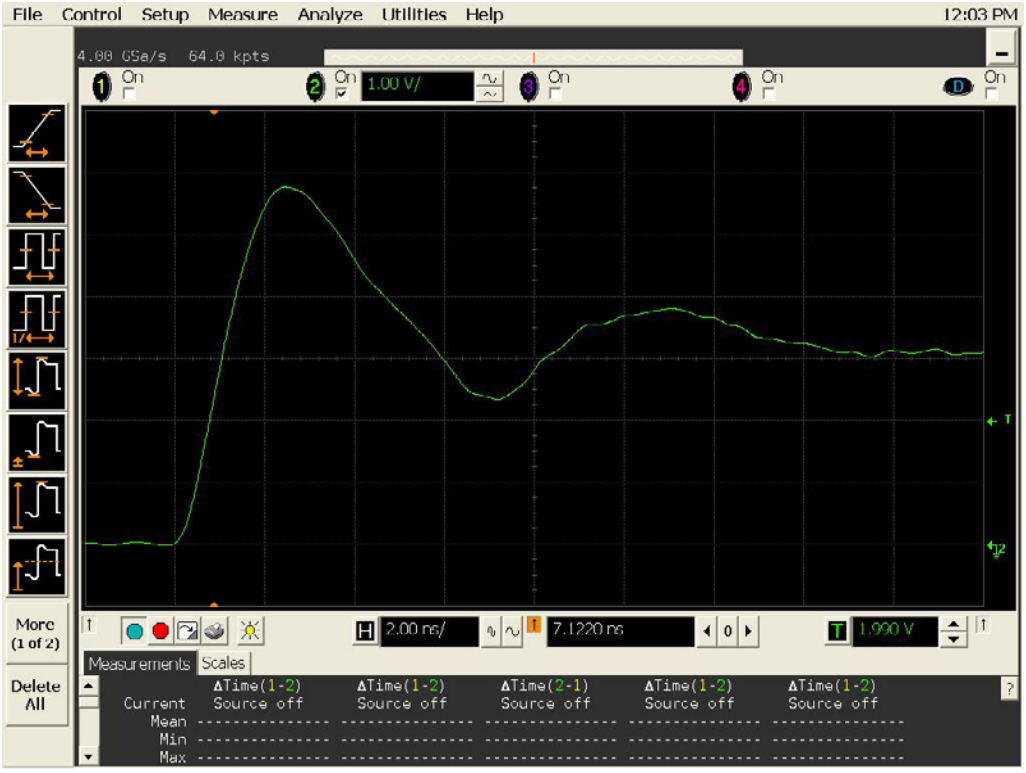

Figure 10b DUT 11454 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

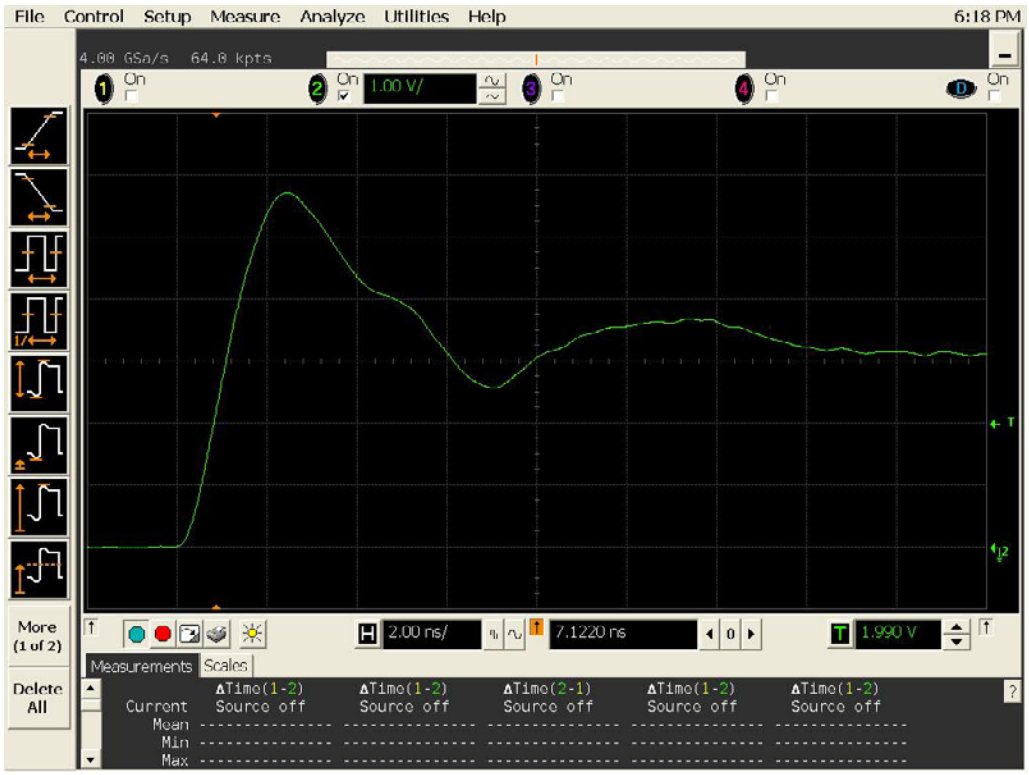

Figure 11a DUT 11455 pre-radiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

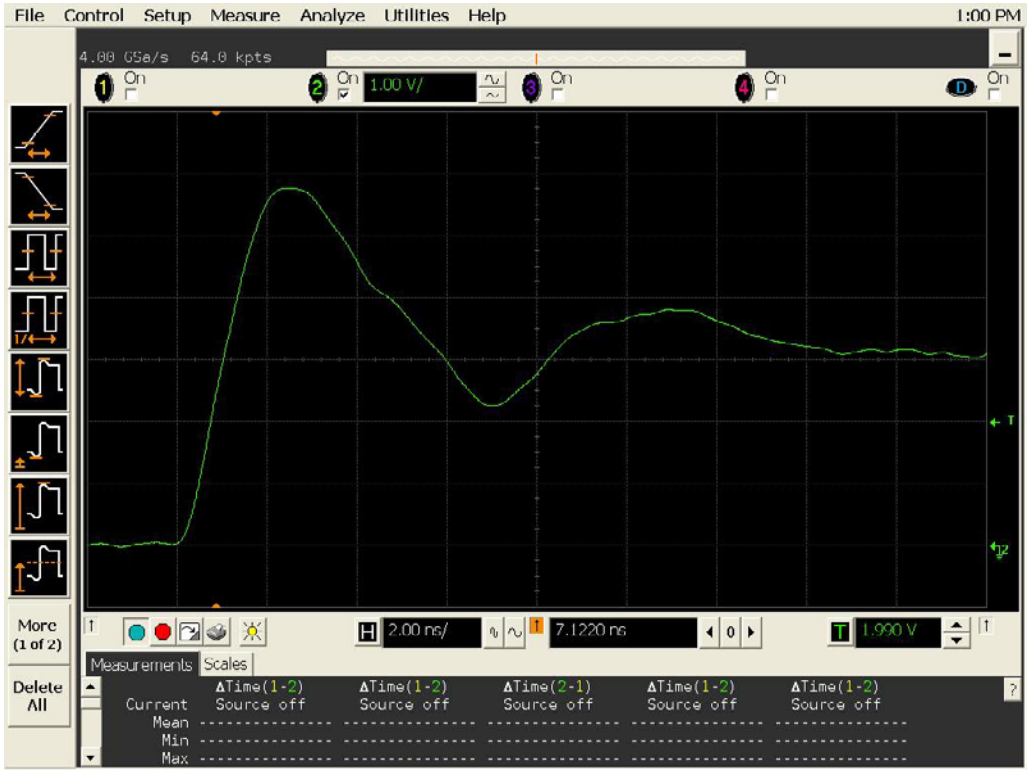

Figure 11b DUT 11455 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

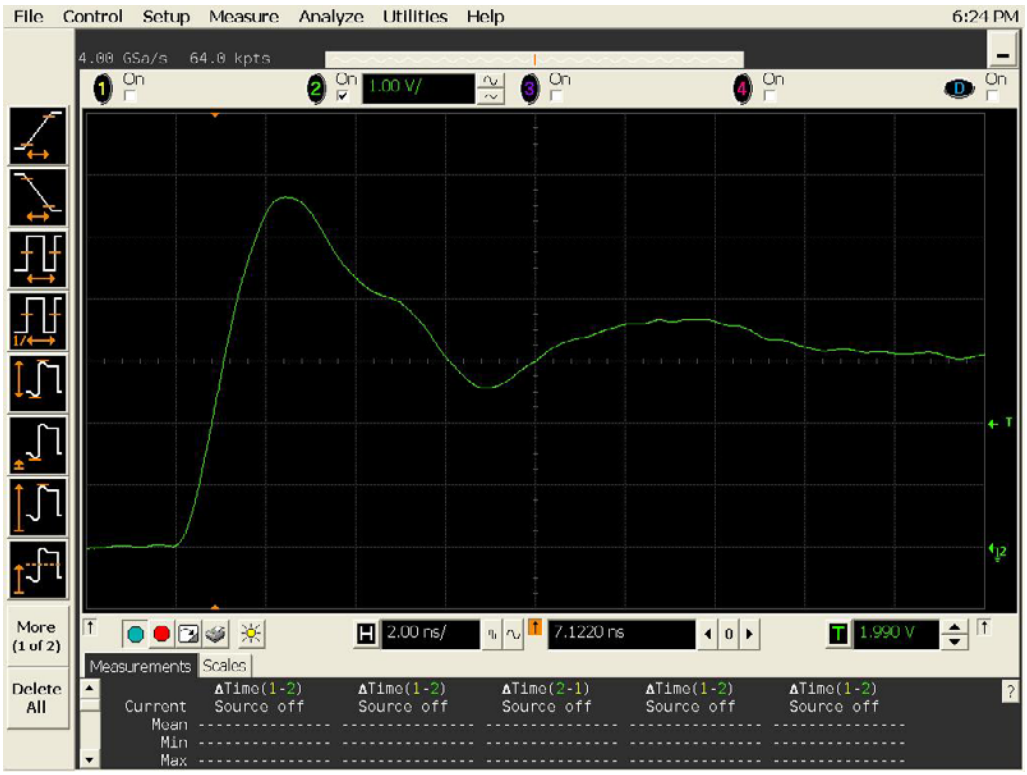

Figure 12a DUT 11457 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

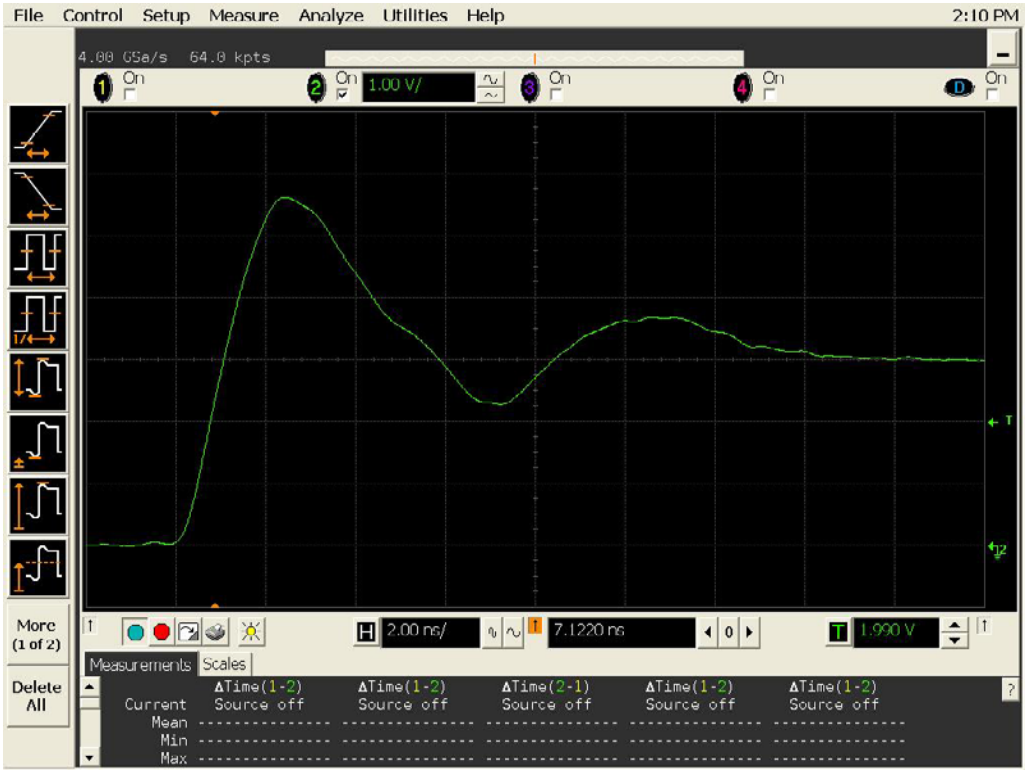

Figure 12b DUT 11457 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

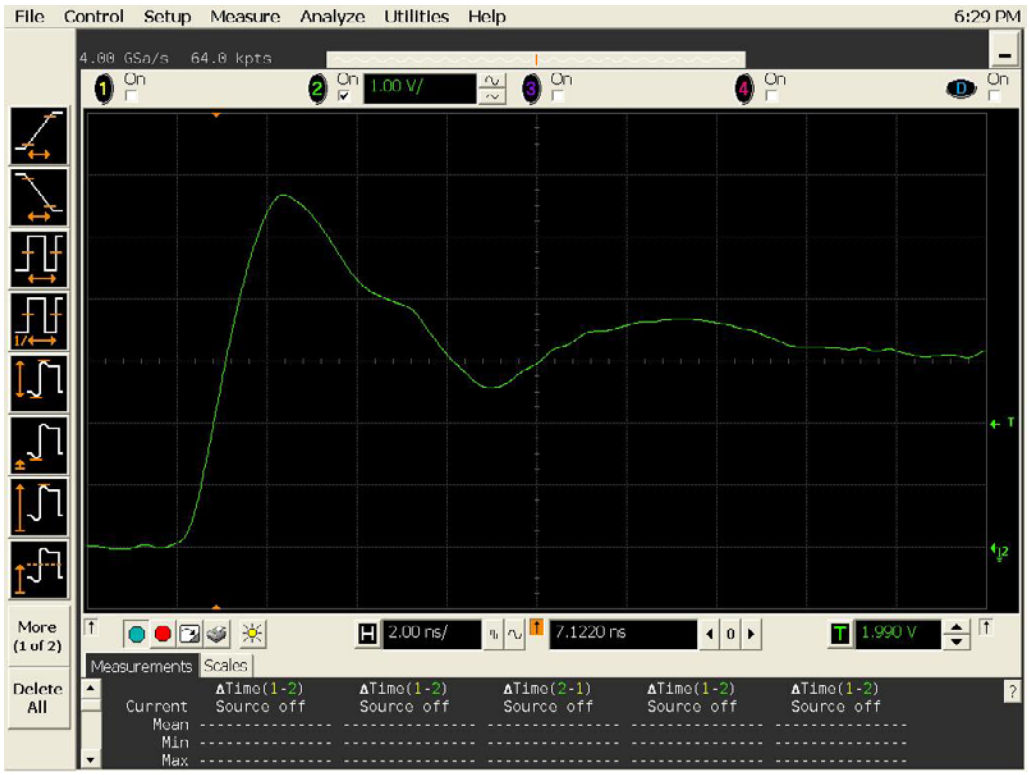

Figure 13a DUT 11460 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

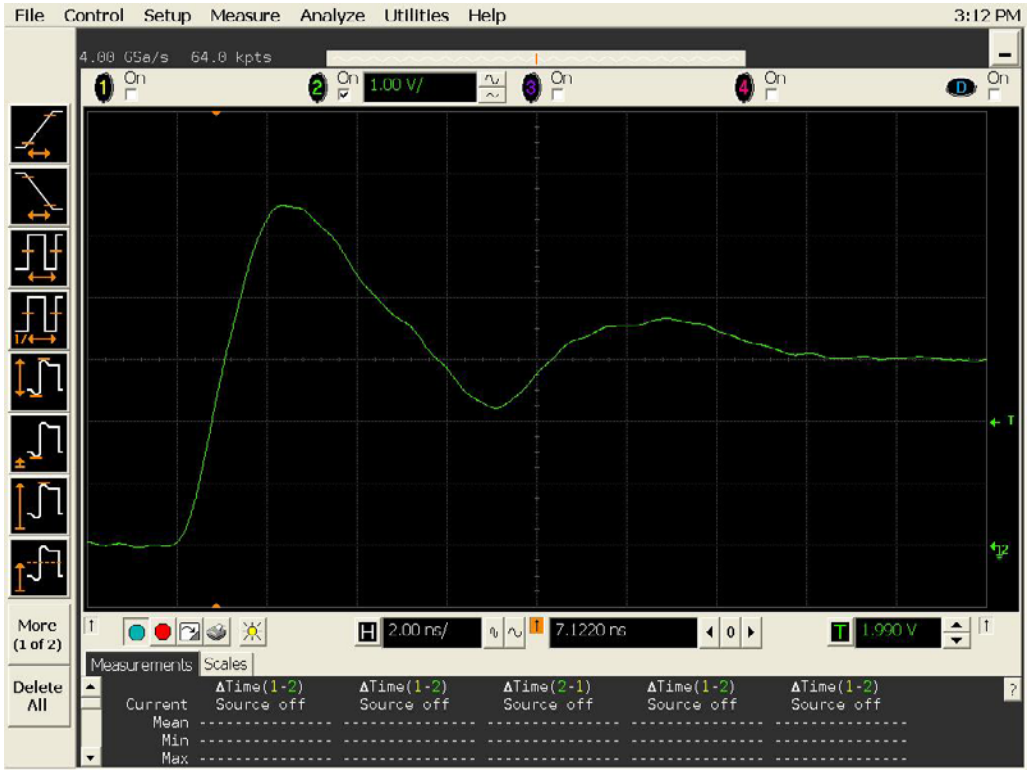

Figure 13b DUT 11460 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

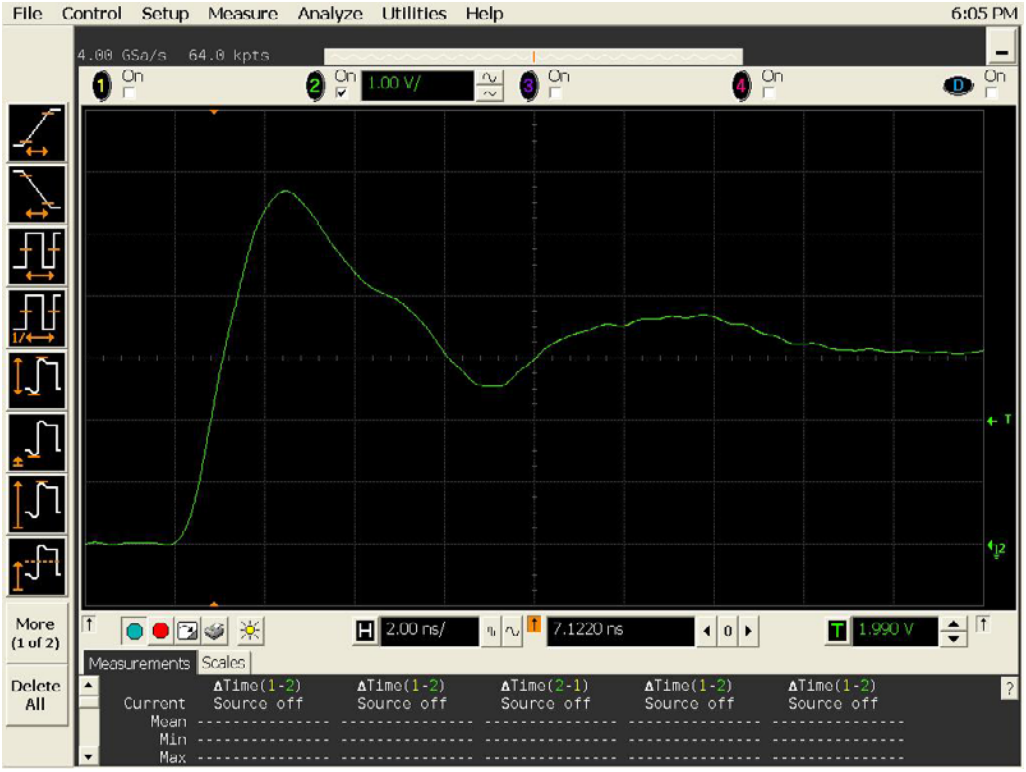

Figure 14a DUT 11461 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

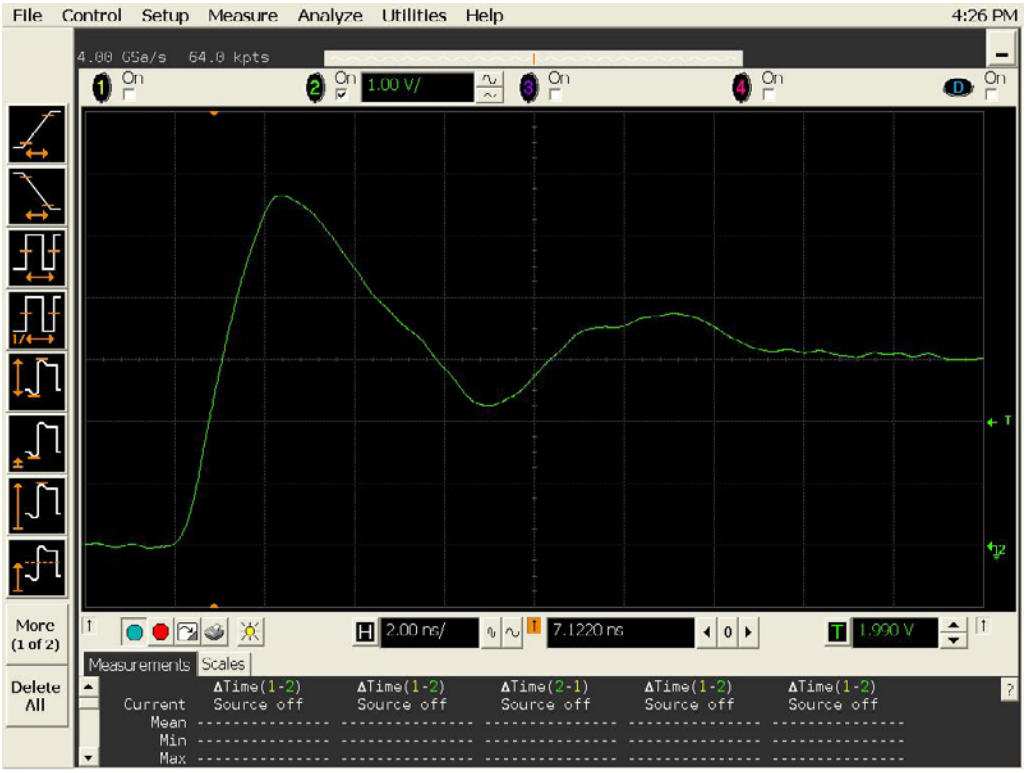

Figure 14b DUT 11461 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

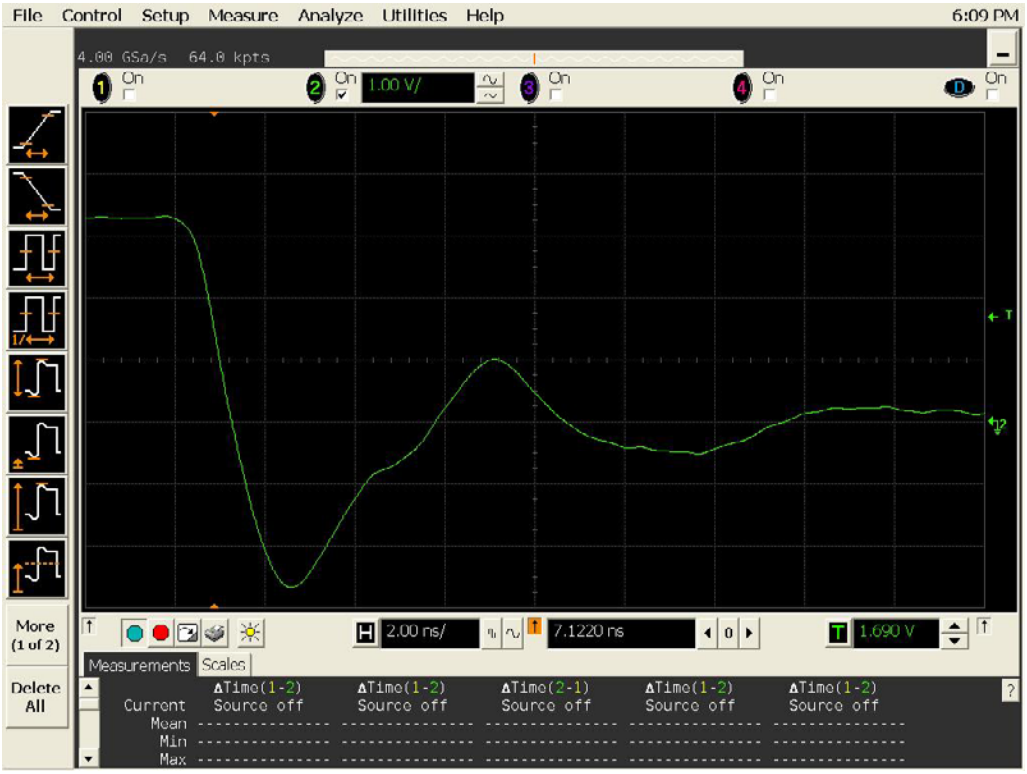

Figure 15a DUT 11453 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

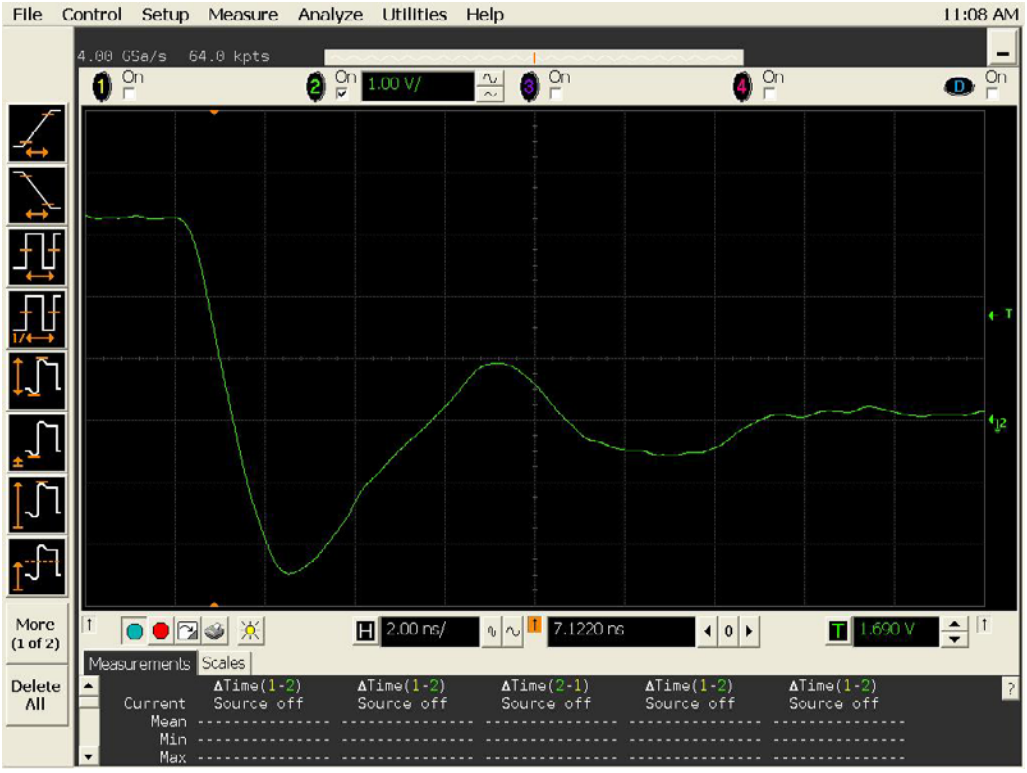

Figure 15b DUT 11453 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

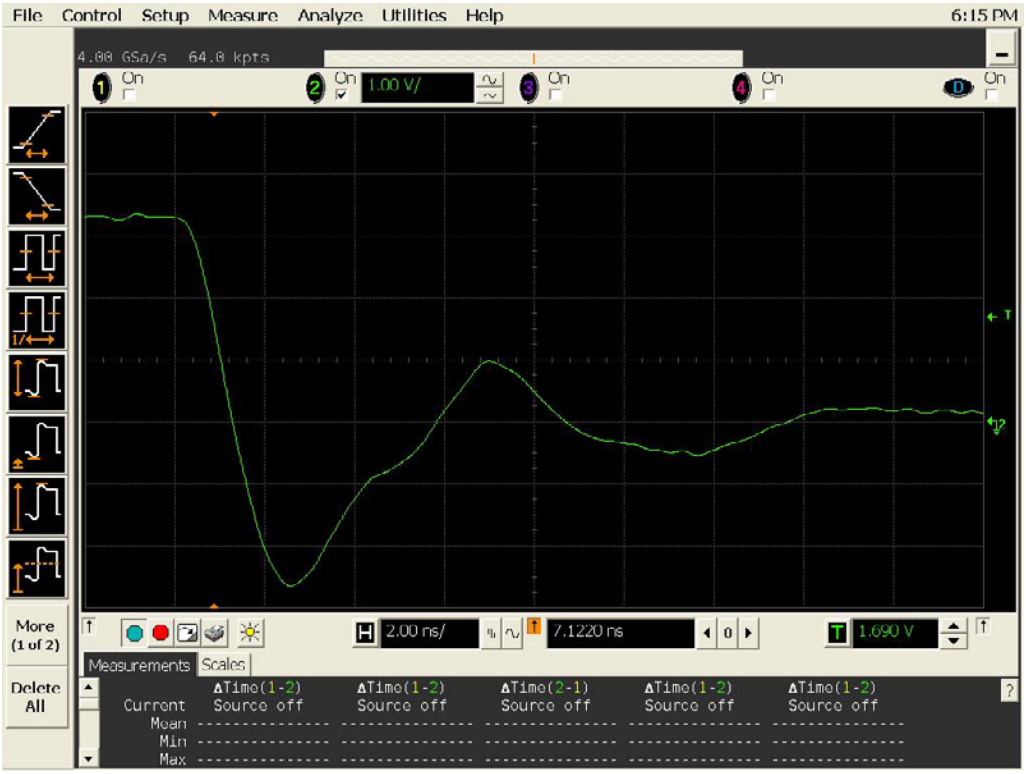

Figure 16a DUT 11454 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

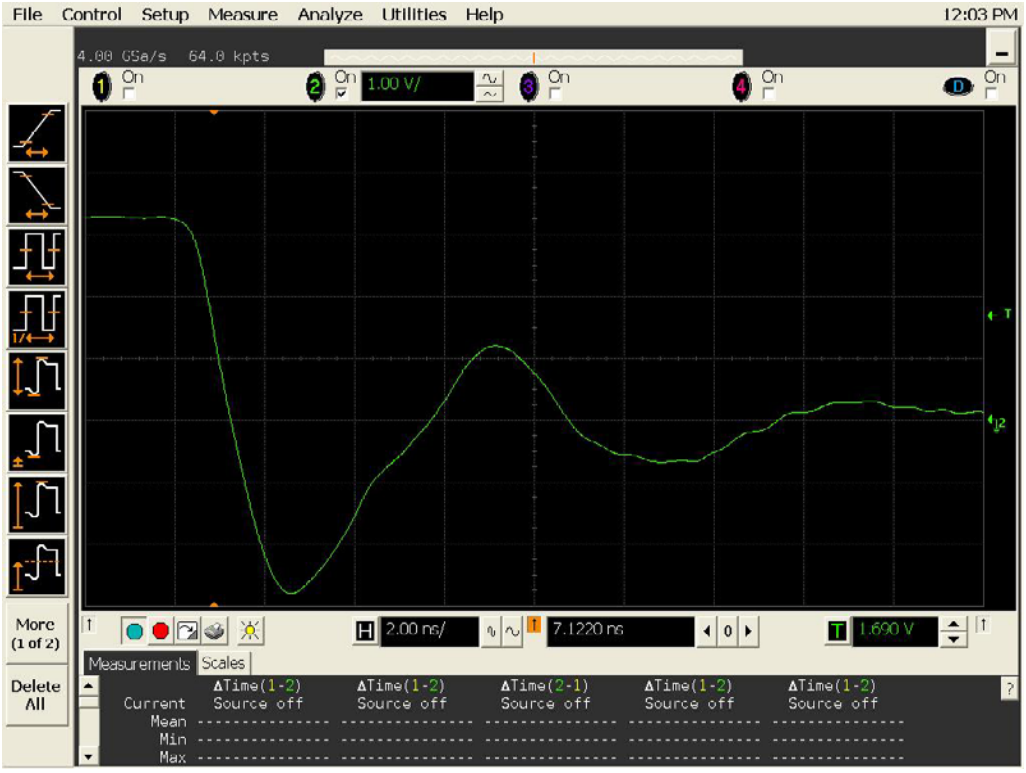

Figure 16b DUT 11454 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

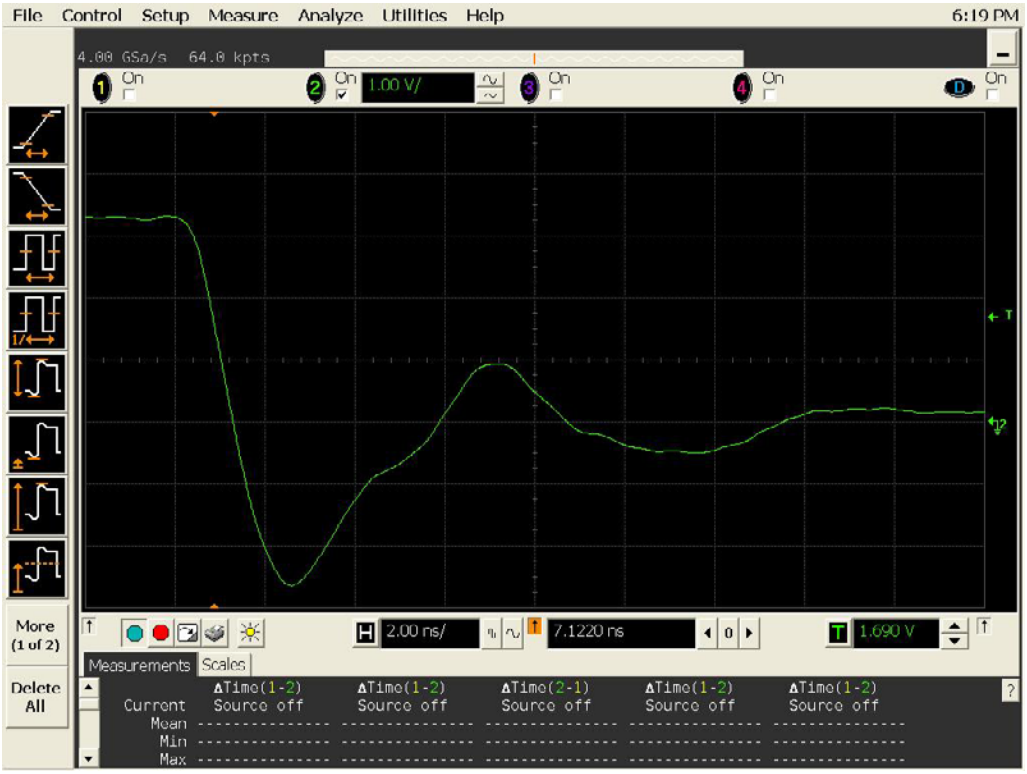

Figure 17a DUT 11455 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

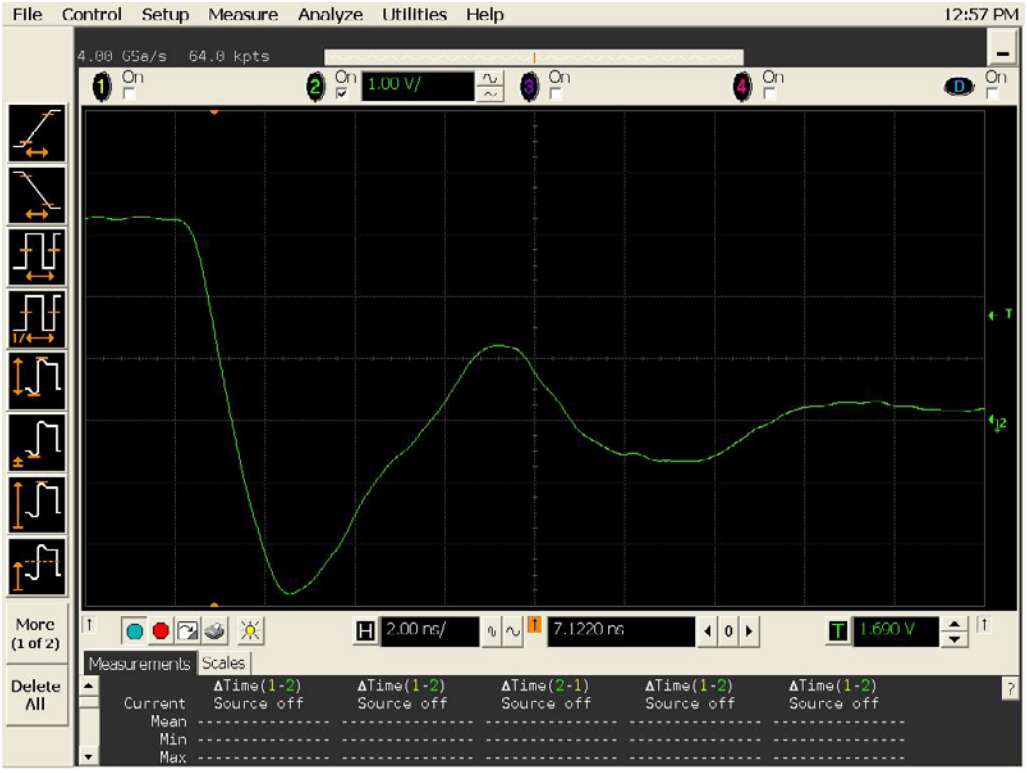

Figure 17b DUT 11455 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

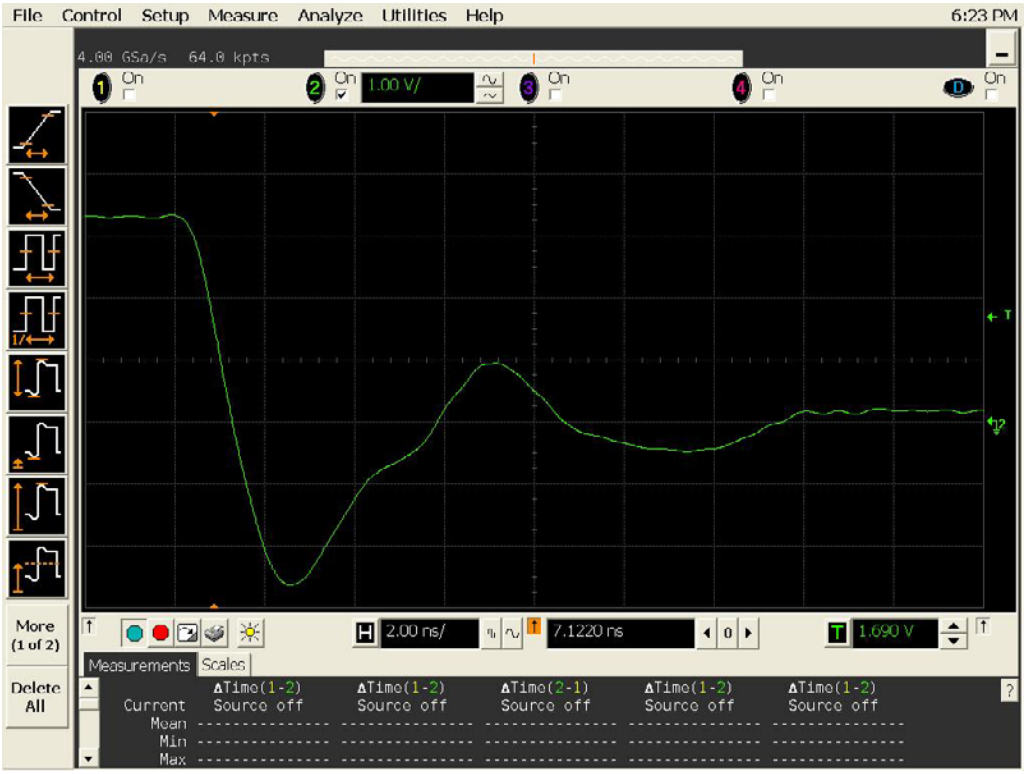

Figure 18a DUT 11457 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

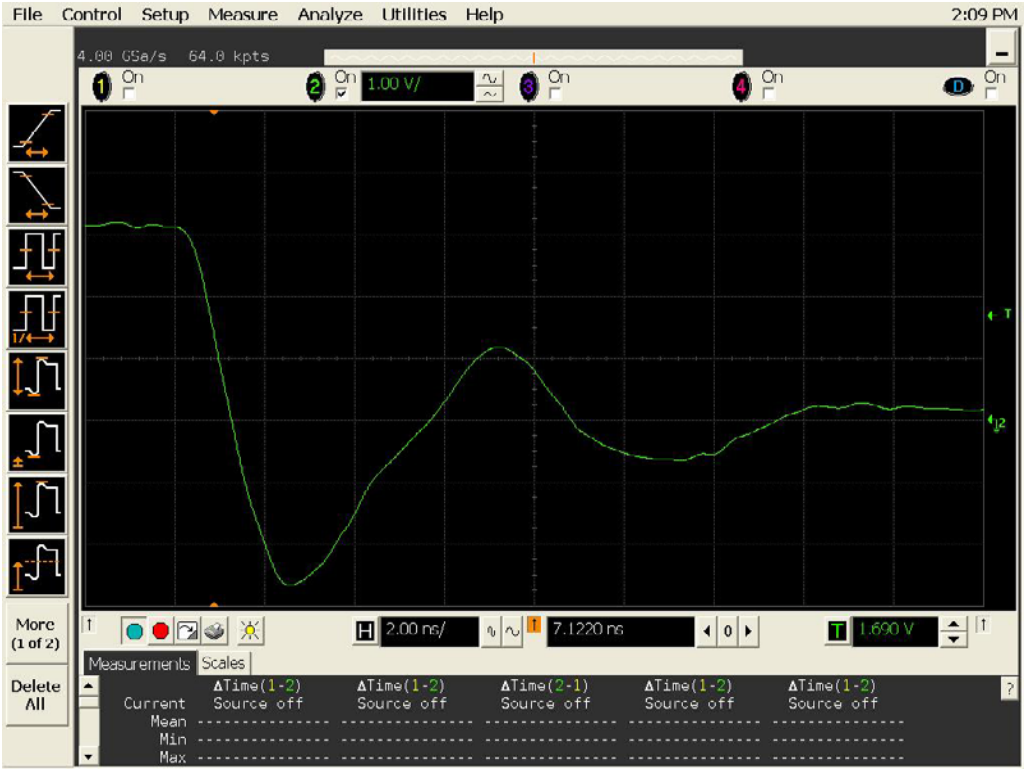

Figure 18b DUT 11457 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

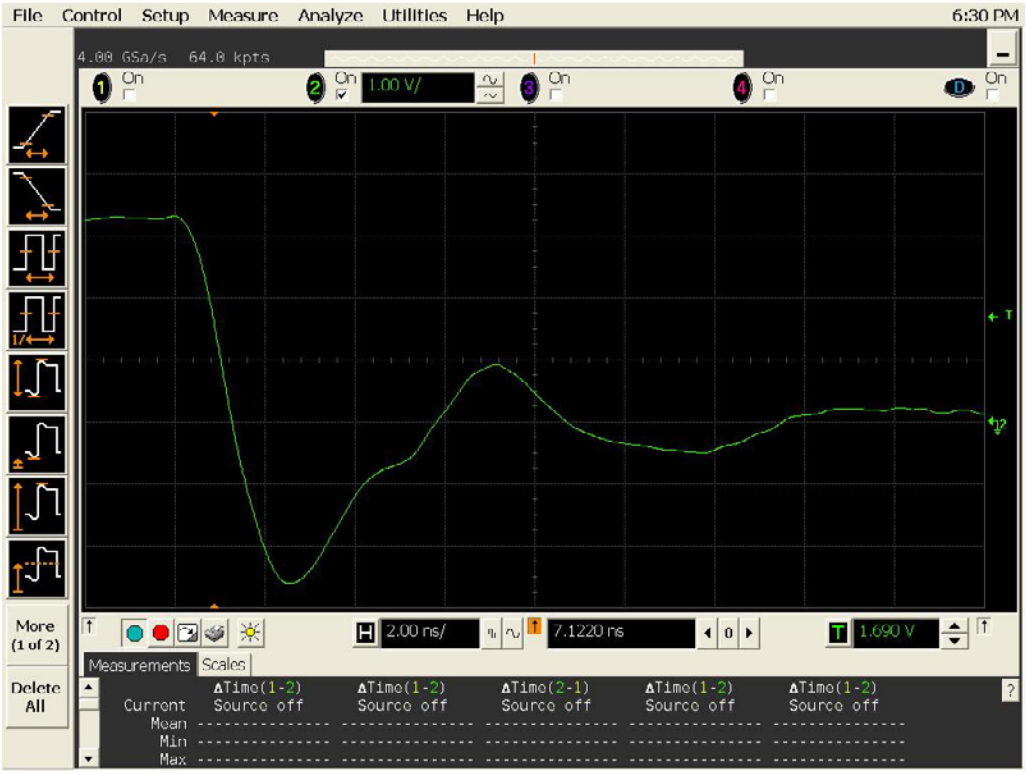

Figure 19a DUT 11460 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

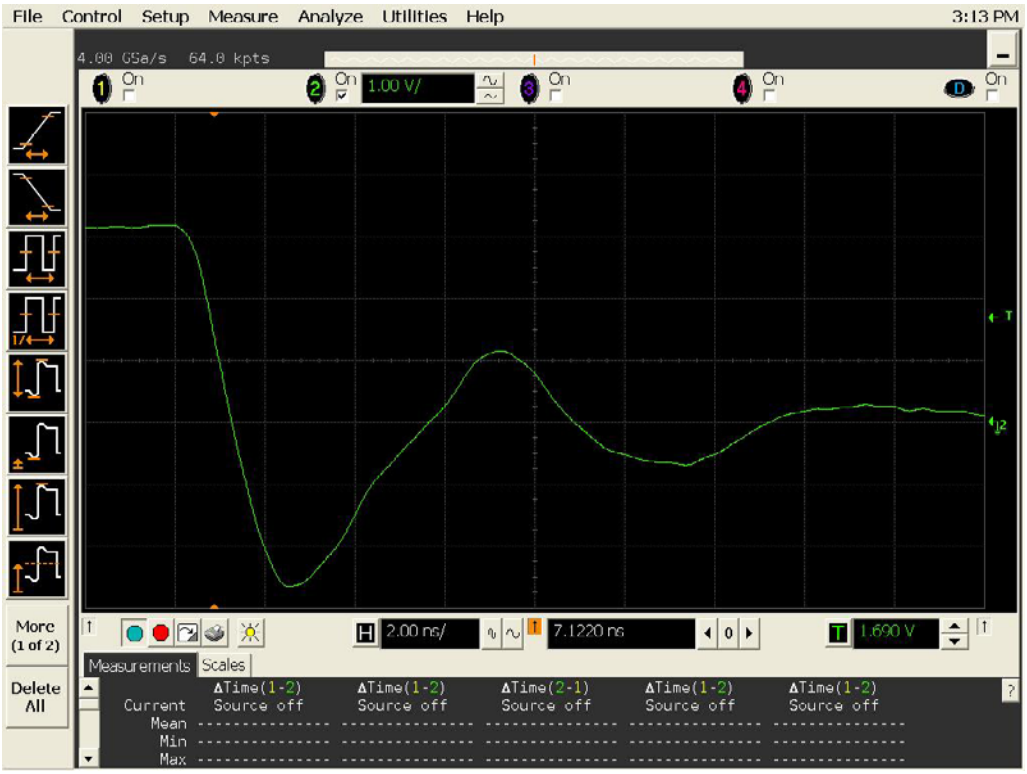

Figure 19b DUT 11460 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

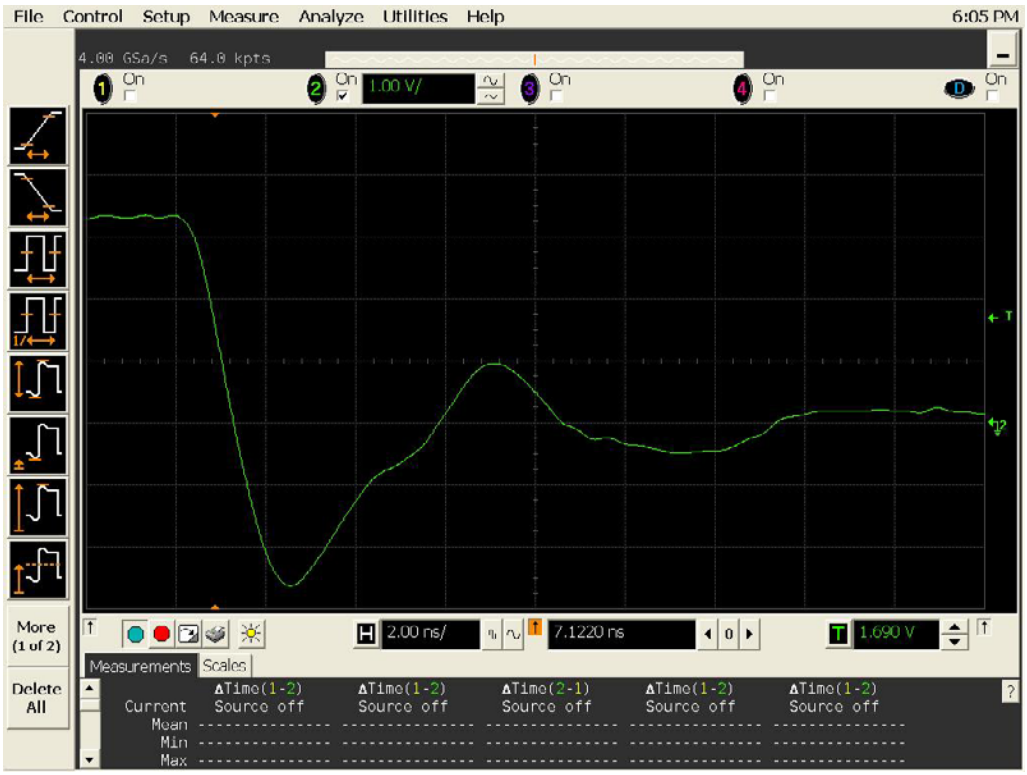

Figure 20a DUT 11461 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

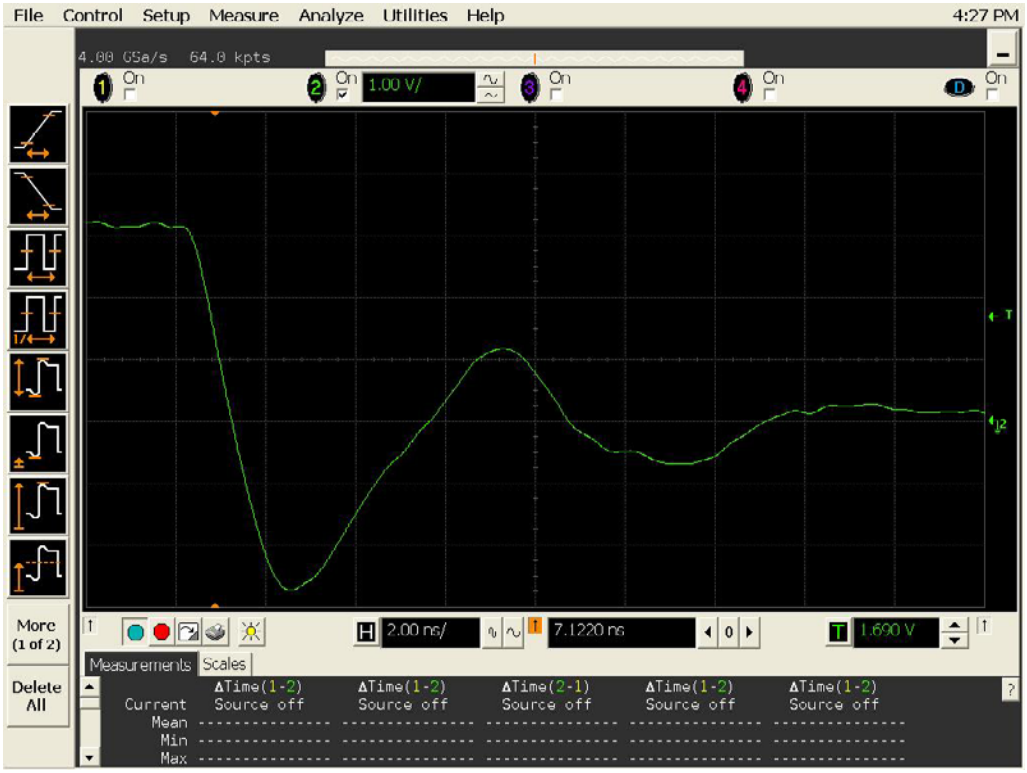

Figure 20b DUT 11461 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

Microsemi Corporate Headquarters
2381 Morse Avenue, Irvine, CA 92614
Phone; 949.221.7100 · Fax: 949.756.0308
www.microsemi.com

Microsemi Corporation (NASDAQ: MSCC) offers the industry's most comprehensive portfolio of semiconductor technology. Committed to solving the most critical system challenges, Microsemi's products include high-performance, high-reliability analog and RF devices, mixed signal integrated circuits, FPGAs and customizable SoCs, and complete subsystems. Microsemi serves leading system manufacturers around the world in the defense, security, aerospace, enterprise, commercial, and industrial markets. Learn more at **www.microsemi.com** .