Ball Grid Array (BGA) Solder Joint Intermittency Detection: SJ BIST™

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Abstract—This paper presents test results and specifications for SJ BIST™, an innovative sensing method for detecting faults in solder-joint networks that belong to the I/O ports of Field Programmable Gate Arrays (FPGAs), especially in Ball Grid Array packages. It is well-known that fractured solder joints typically maintain sufficient electrical contact to operate correctly for long periods of time. Subsequently the damaged joint begins to exhibit intermittent failures: the faces of a fracture separate during periods of stress, causing incorrect FPGA signals. SJ BIST detects faults of 100 Ω or lower with zero false alarms: minimum detectable fault period is one-half the period of the FPGA clock; guaranteed detection is two clock periods. Being able to detect solder joint faults in FPGAs increases fault coverage and health management capabilities, and provides support for condition-based and reliability-centered maintenance[12].

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1. INTRODUCTION

This paper presents test results and specifications for SJ BIST™ (Solder Joint Built-in-Self-Test™), which is an innovative sensing method for detecting faults in solder-joint networks that belong to the I/O ports of Field Programmable Gate Arrays (FPGAs), especially FPGAs in Ball Grid Array (BGA) packages such as a XILINX® FG1156 [1-6]. FPGAs are widely used as controllers in aerospace applications, and being able to detect solder joint faults increases both fault coverage and health management capabilities and support for condition-based and reliability-centered maintenance. As both the pitch between the solder balls of the solder joints of BGA packages and the diameter of the solder balls decrease, the importance a real-time solder-joint fault sensor for FPGAs increases. SJ BIST is the first known for detecting high-resistance faults in solder joint networks of operational FPGAs.

The current version of SJ BIST is a Verilog-based, two-pin test group core intended to be incorporated within an end-use application in the FPGA. Test assemblies of printed wire (circuit) boards (PWBs) with programmed FPGAs have been assembled and are being tested to failure at the Center for Advanced Vehicle Electronics (CAVE) at Auburn University; in Germany under the sponsorship of an automobile manufacturer, and at Ridgetop Group facility in Tucson, Arizona. Raytheon Missile Systems, Tucson, has acquired demonstration boxes for both evaluation and for testing.

SJ BIST correctly detects and reports instances of high-resistance with no false alarms: test results are shown in this paper. The program for the test boards contains temporary

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[1] 1-4244-1488-1/08/$25.00 ©2008 IEEE.
[2] IEEEAC paper #1148, Version 1, Updated Aug. 14, 2007.

data collection routines for statistical analysis and uses less than 250 cells out of over 78,000 cells for a 5-million gate, 1156-pin FPGA to test 8 pins.

Initial testing indicates SJ BIST is capable of detecting high-resistance faults of 100 Ω or lower and which last one-half of a clock period or longer. In addition to producing no false alarms in the current period of testing, no additional failure mechanisms are introduced to an assembly because, with the exception of fault reporting and handling, SJ BIST is (1) not invasive to an application program; (2) is not compute intensive and so timing problems are not anticipated; and (3) any failures in SJ BIST itself is a failure in the FPGA or the board. Therefore either a real failure is reported or no failure is reported and neither is a false alarm.

Mechanics of Failure

Solder-joint fatigue damage caused by thermo-mechanical and shock stresses is cumulative and manifests as voids and cracks, which propagate in number and size. Eventually, the solder ball (or bump) of the joint fractures [7-10] and FPGA operational failures occur. An illustration of a damaged solder bump on the verge of fracturing is shown in Figure 1.

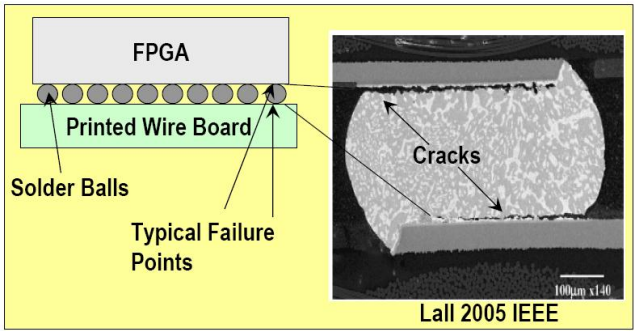


Figure 1: Crack Propagation at the Top and Bottom of a Solder Ball (Bump), 15mm BGA [8].

Figure 2 and Figure 3 depict a cracked solder ball of a BGA package attached to an electronic printed circuit board (PCB); Figure 4 depicts a fractured solder ball, which is what happens to a crack as an end result of accumulated fatigue damage. A fracture is the complete separation of a solder ball that can result in a break in the electrical connection between the BGA and the electronic board.

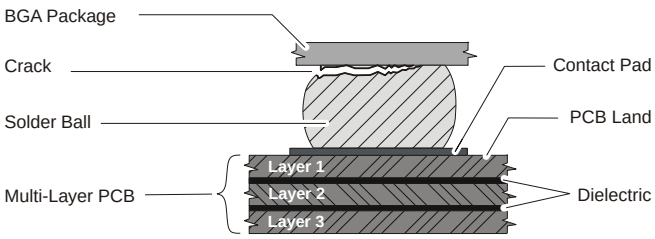


Figure 2: Crack at BLM and Solder Ball.

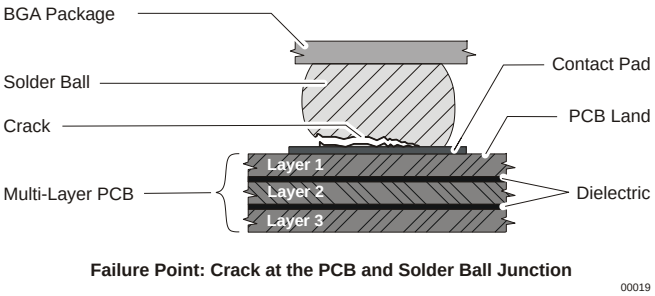


Figure 3: Crack at Solder Ball-PCB Junction.

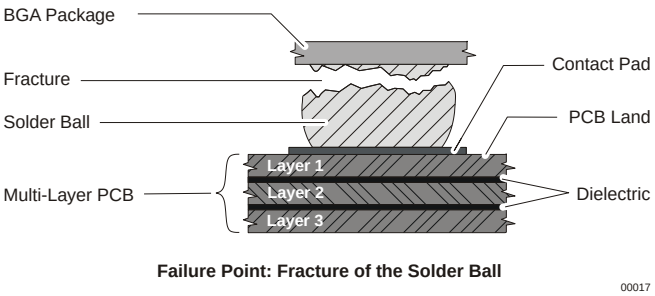


Figure 4: Fractured Solder Ball.

Intermittent Behavior of Fractured Solder Bumps

Over time, contamination and/or oxidation coats the fractured surfaces and a failure progression occurs: from degraded joints to intermittent opens of short duration (nanoseconds or less) to longer durations (microseconds) to very long durations (milliseconds or longer). The latter, faults of milliseconds or longer, are very likely to cause faults in the correct FPGA operation. Test results confirm this physics of failure behavior. As seen in Figure 5, during periods of high stress, fractured bumps tend to momentarily open and cause hard-to-diagnose, intermittent faults of high resistance of 100s of Ohms [10-12]. Such faults typically last for periods of hundreds of nanoseconds, or less, to more than 1 µs [7, 11, 13-16]. The intermittent faults are caused by the opening and closing of the fractured faces of the solder balls, as depicted in Figure 6.

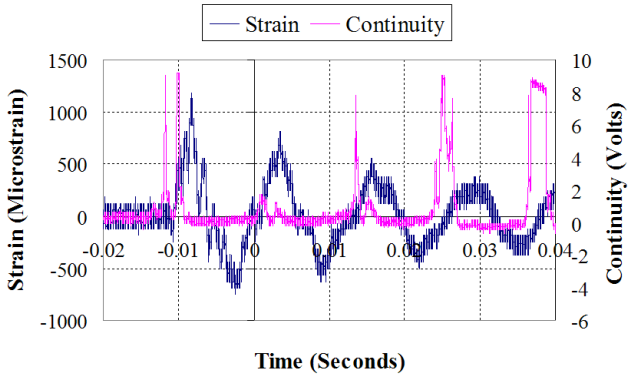


Figure 5: Shock-actuated Failure: Transient Strain (Blue) and Intermittent Opens (Mauve) (From Lall).

These intermittent faults increase in frequency as evidenced by a practice of logging BGA package failures only after multiple events of high-resistance: an initial event followed by some number (for example, 2 to 10) of additional events within a specified period of time, such as ten percent of the number of cycles of the initial event [14-16]. Even then, an intermittent fault in a solder-joint network might not result in an operational fault. For example, the fault might be in a ground or power connection; or it might occur during a period when the network is not being written; or it might be too short in duration to cause a signal error. In Figure 5, the duration of the fault in the 5th cycle of stress is over 3 milliseconds.

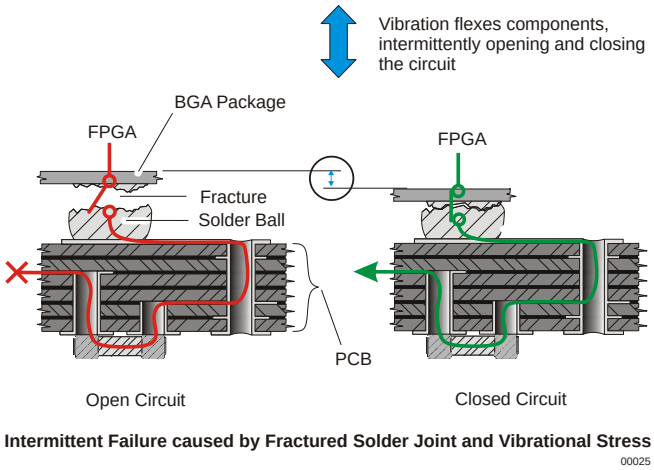


Figure 6: Intermittent Open and Closed Connection.

Damage accumulates and eventually there is a catastrophic failure, such as might happen when a solder ball becomes displaced as depicted in Figure 7.

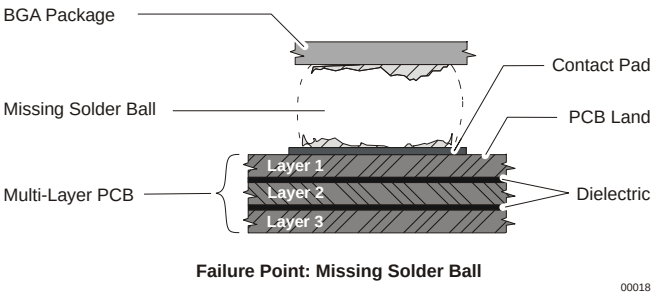


Figure 7: Displaced (Missing) Solder Ball.

Figure 8 represents HALT test results performed on XILINX FG1156 Daisy Chain packages in which 30 out of 32 tested packages failed in a test period consisting of 3108 HALT cycles. Each temperature cycle of the HALT was a transition from -55°C to 125 °C in 30 minutes: 3-minute ramps and 12-minute dwells. What is not immediately apparent is that each of the logged FPGA failures (diamond symbols) represents at least 30 events of high resistance: a FAIL was defined as being at least 2 OPENS within the same temperature cycle. A single OPEN in any temperature cycle was not counted as a FAIL event; and the package was deemed as failed only after 15 FAILS [15] had been logged.

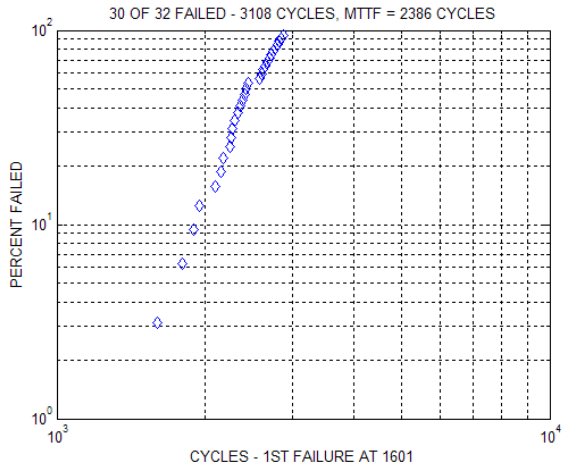


Figure 8: XILINX FPGA HALT Test Results [15].

State of the Art

The use of leading indicators of failure for prognostication of electronics has been previously demonstrated [17-20]. One important reason for using an in-situ solder-joint fault sensor is that stress magnitudes are hard to derive, much less keep track of [21]; another reason is that even though a particular damaged solder-joint might not result in immediate FPGA operational faults, the fault indicates the FPGA is likely to have, or will soon have, other damaged I/O ports – the FPGA is no longer reliable. In a manufacturing environment, SJ BIST addresses a concern that failure modes caused by the PWB-FPGA assembly are not being detected during component qualification [12].

FPGAs are not amenable to the measurement techniques typically used in manufacturing reliability tests such as Highly Accelerated Life Tests (HALTs) [10]. This is because, for example, a 4-point probe measurement requires devices to be powered-off; and because FPGA I/O ports are digital, rather than analog, circuits (see Figure 9).

Modern BGA FPGAs have more than a thousand pins and very small pitch and ball sizes, for example, the left side of Figure 10 shows the position of the XILINX FG1156 FPGA die with respect to a ceramic base and the right side shows the bottom of the package – a footprint of 35x35 mm^2, and an array of 34x34 solder balls. The dense array of fine-pitch and ultra fine-pitch BGA packages with very small pitch and solder ball tends to make physical-, optical-, X-ray- and sonic-based inspection techniques impractical for detecting the onset of damage.

A test board was ground to create the cut view shown in Figure 11. The cut view shows the FPGA die is connected by either flip-chip collapsed connections or by bonding to a ceramic base. Wire interconnects connect the die to ball limiting metallurgy (BLM), to which solder balls are attached. The FPGA package is then placed over connection lands on the printed circuit board (PCB) and soldered. Note

the presence of voids in the two solder balls on the right-hand side of the figure.

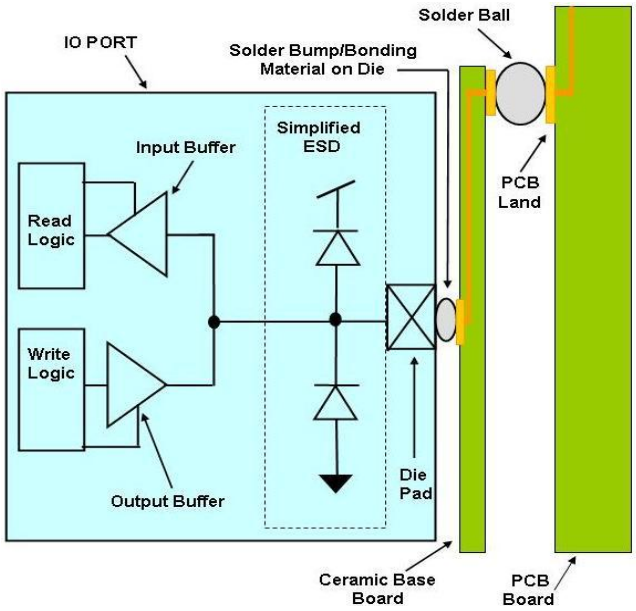


Figure 9: FPGA Diagram, I/O Buffer [22].

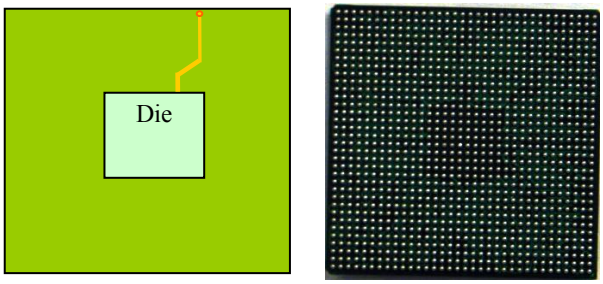


Figure 10: FG1156: Size is 35x35 mm^2; Pitch: 1.0 mm. Ball: 0.6 mm [23].

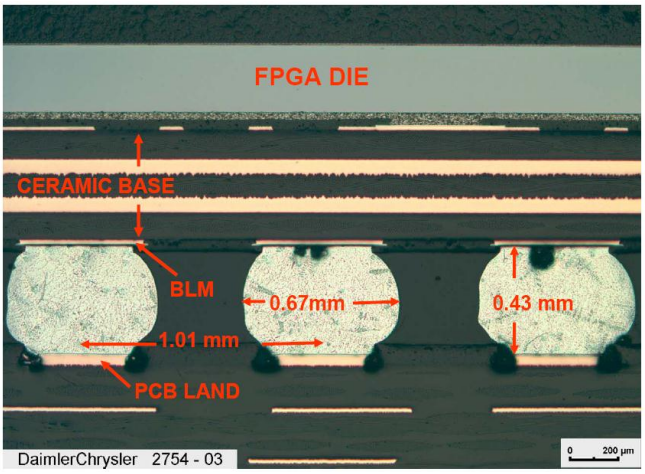


Figure 11: View Showing FPGA Die to PCB Connection.

2. SJ BIST

SJ BIST requires the attachment of a small capacitor to two unused I/O ports as near as possible to a corner of the package. Figure 12 is a block diagram of an FPGA containing SJ BIST with a capacitor connected to two I/O pins: Figure 13 shows the signal for a no-fault condition (A) and a fault condition (B). SJ BIST writes a logical '1' to charge the capacitor and then reads the voltage across the charged capacitor. If the solder-joint network of the I/O port of the FPGA is undamaged, the write causes the capacitor to be fully charged and a logical '1' is read by SJ BIST. When the solder-joint network is damaged, the effective resistance of the SJ network increases, the charging time constant increases, the write fails to sufficiently charge the capacitor, and a logical '0' instead of a logical '1' is read: a fault occurs, is detected by SJ BIST and is reported.

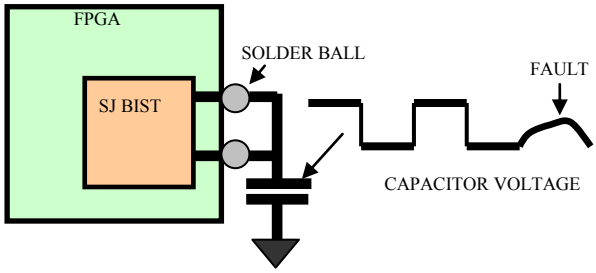
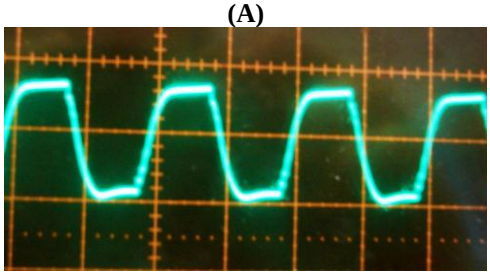


Figure 12: SJ BIST Block Diagram

(A)



(B)

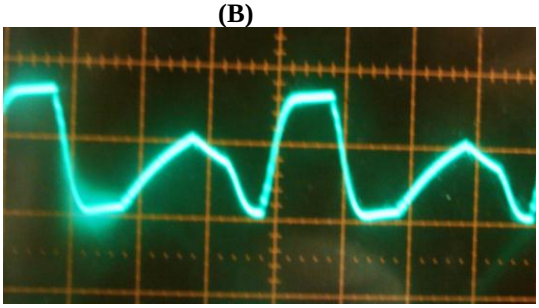


Figure 13: SJ BIST: 1 MHz Capacitor Signal. (A) No Fault; (B) 100 Ω Fault – 0.5 µs x 2.0V Grid.

Test Results

Tests have been run at various clock frequencies ranging from 10 KHz to 100 MHz and for varying solder-joint network conditions ranging from no fault to over 100 Ω of

fault resistance: All faults of 100 Ω or larger were detected, and there were no false alarms.

Referring to Figure 13, voltages on a 1.0 µF capacitor connected to a group of two I/O ports are shown. Figure 13A shows the capacitor voltage when one of the two ports connected to the capacitor has a 1 Ω resistor connected in series with the solder joint: the resistance is not high enough cause a write fault to occur, and SJ BIST correctly did not report a detected fault. Figure 13B shows the capacitor voltage when the resistance is increased to 100 Ω, a write fault occurs. SJ BIST correctly reported the fault and incremented the fault count for that I/O pin.

Clock Frequency, Capacitor Value and Fault Resistance

The relationship between the frequency of the FPGA clock, the value of the connected capacitor to each group of two I/O pins, and the detectable fault resistance is shown in Figure 14.

SJ BIST Sensitivity and Resolution

For a given clock frequency, there is a capacitor value that will cause SJ BIST to always detect a fault resistance at least as low as 100 Ω with a duration of at least two clock periods. Faults of shorter duration are detectable when they occur at the beginning of the write and last for about one-half of a clock period.

For clock frequencies of one-half or higher of the maximum clock frequency of the FPGA, the capacitance of the I/O port is sufficient – no external capacitance needs to be connected for SJ BIST to correctly detect faults with no alarms.

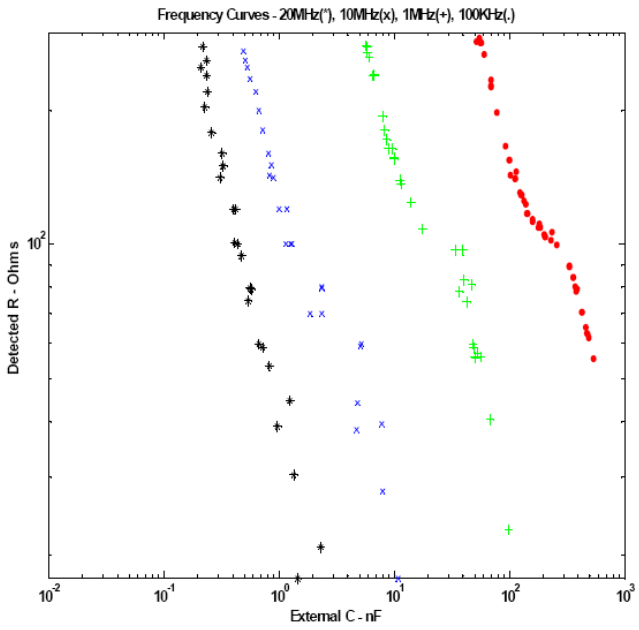


Figure 14: Frequency, Capacitor and Resistance.

SJ BIST Signals and Controls

SJ BIST needs to present at least one error signal (a fault indicator) either to an external FPGA I/O port or to an internal fault management program. At least one control signal is required: an enable (disable) BIST.

Error Signals and Fault Counts—Each SJ BIST core has two error signals: (1) at least one previous fault has been detected and (2) a fault is currently active. A fault counter (1:255) is also provided. For a deployed SJ BIST, we anticipate most applications would only the first error signal without any count: we use the count for statistical purposes

Control Signals— In addition to CLK, SJ BIST has two input signals: ENABLE and RESET. ENABLE is used to turn SJ BIST detection on and off; RESET is used to reset both the fault signal latches and the fault counters. For a deployed SJ BIST, RESET might not be used.

3. INTERMITTENCY MITIGATION

SJ BIST is a very useful sensor for mitigating intermittencies. Early detection of failure of an unused I/O pin allows the electronic board to be replaced before subsequent fatigue damage causes an application I/O pin to fail, and therefore intermittent operational anomalies are avoided.

Intermittent Behavior of Fractured Solder Joints

As previously seen in Figure 5, fractured solder joints tend to maintain electrical contact until periods of increasing stress occur: a hard open longer than a millisecond did not occur until the fifth shock wave. SJ BIST would have recorded at least eight instances of faults: two in each of the first three waves and one each in the fourth and fifth waves

Intermittent Confirmation and Prognostic Warning

Detection of intermittent faults can be used to confirm that the electronic board with that FPGA is a likely candidate for replacement to address reported operational anomalies. In the absence of any reported operational anomalies, detected faults can be used as a prognostic warning that the board is likely to experience future operational anomalies.

4. PIN SELECTION

We recommend a deployed SJ BIST application use at least four groups of cores: one group of two I/O pins near each corner of an FPGA (the pink-shaded pins) because research indicates the solder balls nearest the corner are most likely to fail first. The next-most likely solder balls to fail are those under the die of the FPGA. Evidence of this failure distribution is the reserving of the four I/O pins at each corner for ground and all of the pins under the dies for power and ground (the orange-shaded pins).

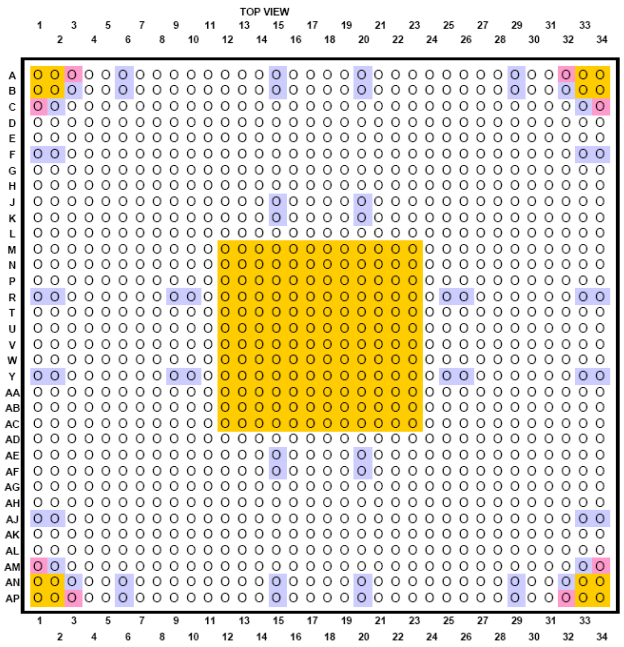


Figure 15: FG1156 I/O Pin Footprint [22].

5. TEST ACTIVITIES

Extensive experiments, including HALTs, have been planned and are presently being conducted. The primary objectives are the following: (1) perform final sensitivity, resolution and clock frequency measurements to update Figure 14; (2) collect, evaluate and publish statistical data related to test I/O port location, first failure and probability of failure distribution. The pink- and light-blue-shaded pins in Figure 15 are the sixty-four pins we selected for HALT testing: 32 groups of two-pin SJ BIST cores.

HALT Test Board

Figure 16 is a block diagram of the HALT test board we designed. The SJ BIST test program is loaded into a PROM, which then loads the program into each FPGA when the board is powered on. Each FPGA generates 640 bits of data (64 x (2 faults signals + 8 bits of count)); each board generates 2560 bits of data. We wrote a LabVIEW® program to control the collection of data, and we wrote a MATLAB® program to process the data.

Figure 17 shows a manufactured, populated and soldered HALT test board. There are three connectors: (1) XILINX programmer connection, (2) power input and (3) experiment control connections.

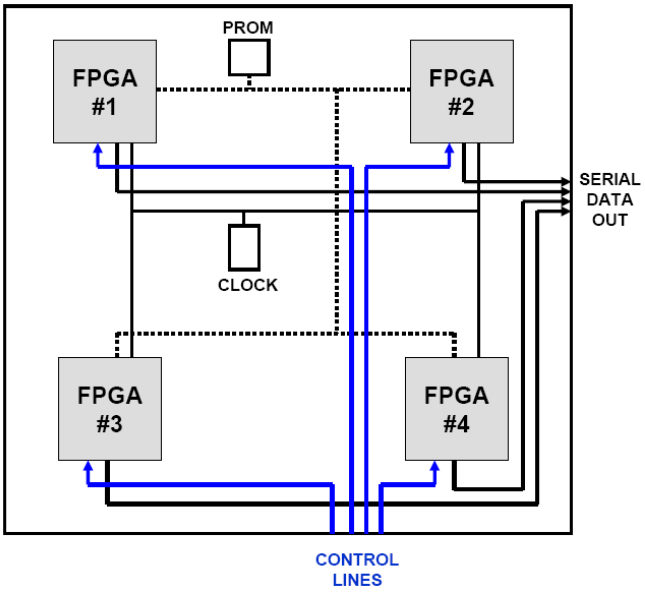


Figure 16: HALT Test Board Block Diagram.

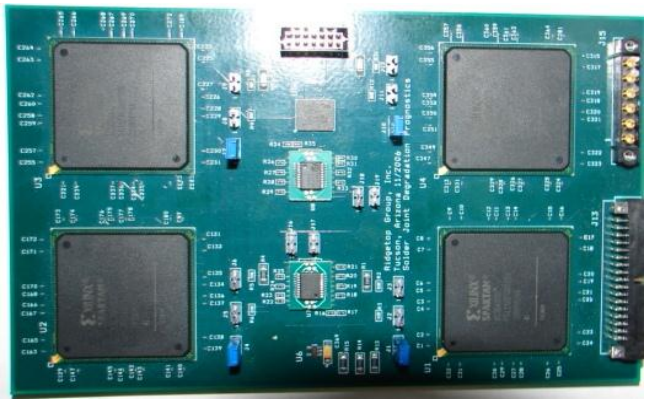


Figure 17: HALT Experiment Board with Four XILINX FG1156 FPGAs.

At the Center for Advanced Vehicle Electronics at Auburn University, Alabama, test boards are placed in a thermal oven (Figure 18) and cycled from -55 ^{o}C to 125 ^{o}C in 30 minute ramps and 15 minute dwells. The boards are subjected random cyclic shock with variable frequency superimposed with random vibrations. A drop test is performed and the test board is placed in the oven for 5 days. Data is collected at the beginning of the test and then twice a day. At the end of 5 days, another drop test is performed with data collected before and after the drop test. This procedure is repeated for each test board until the boards are damaged.

Figure 18: Thermal Oven for Solder Joint HALT Testing – CAVE, Auburn University, Alabama.

Figure 19 shows the HALT test block diagram: a National Instrument (NI) 6541 digital generator is connected to test board and a CB 2162 connector board to collect the digital data. The power board provides 1.2 V, 1.8 V, 2.5 V and 3.0 V power to the FPGA test board. Data from the test board is extracted using a platform cable USB.

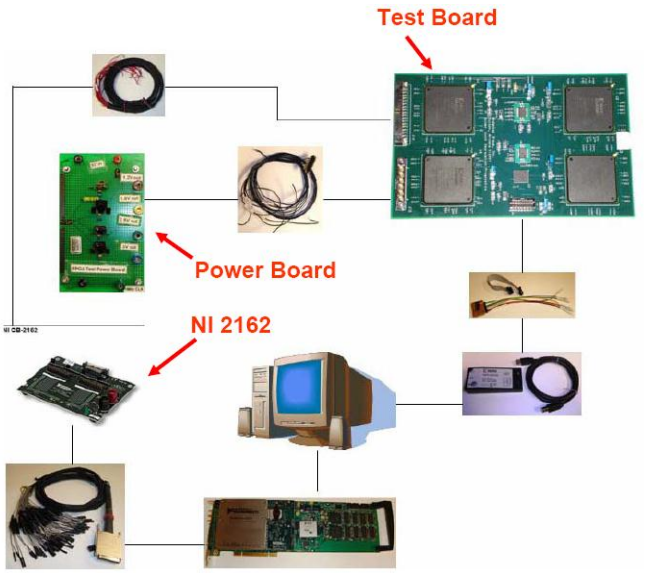


Figure 19: HALT Test Block Diagram.

Independent Test Result

Figure 20 shows a test result from Sindelfingen, Germany, using a known fault of 300 Ω, a 50 MHz clock and a 47 pF capacitor. The result is actually better than that predicted by Figure 14, which shows for a 10 MHz clock, a 500 pF capacitor, the fault sensitivity is 300 Ω, and by extrapolation a 100 MHz clock and a 50 pF capacitor should result in a fault sensitivity of 300 Ω. The total capacitance is the sum of the external, the parasitic capacitance of the port plus the capacitance of everything connected to the port, including the oscilloscope. Note the display of the digital oscilloscope indicates a detected frequency of 24.9 MHz, indicating the oscilloscope the lower voltage signals were not included.

6. SJ BIST Demonstration Box

Figure 21 is a picture of one of the SJ BIST demonstration boxes being tested for delivery to Raytheon Missile Systems. The front panel shows a fault count of 7, a previously detected fault in an upper-right pin, and both an active (the fault inject button is depressed) and a previously detected fault in a lower-right pin. The purpose of the box is to allow for portable demonstrations, and to allow non-Ridgetop personnel to independently demonstrate and evaluate SJ BIST.

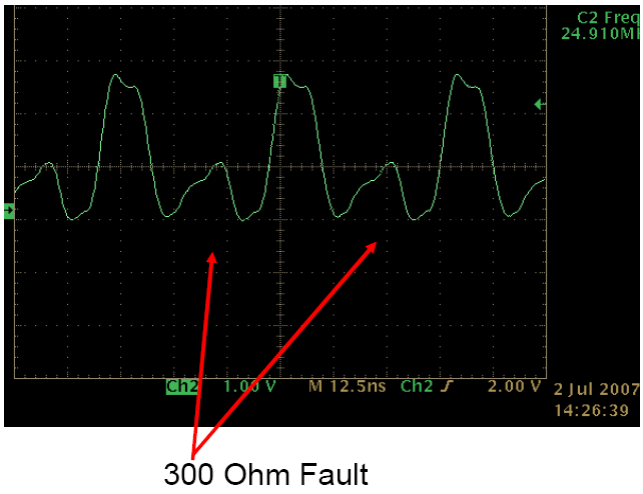


Figure 20: 50 MHz CLK, 47 pF, 300 Ω Fault Test.

An inside view of the demonstration box is shown in Figure 22. The FPGA is programmed to test 8 pins; two of the pins are configured to enable injection of a 100 Ω fault. As faults occur, they are summed and displayed. The control board supports an ENABLE switch and a RESET switch.

Figure 23 is a picture of the display control board for the SJ BIST demonstration board. The board provides the interface and control between the box front panel and the FPGA. Not shown is a small board upon which the 7-segment LED is mounted. We have since designed, fabricated and assembled a printed wire board to replace the wire-wrapped bread board.

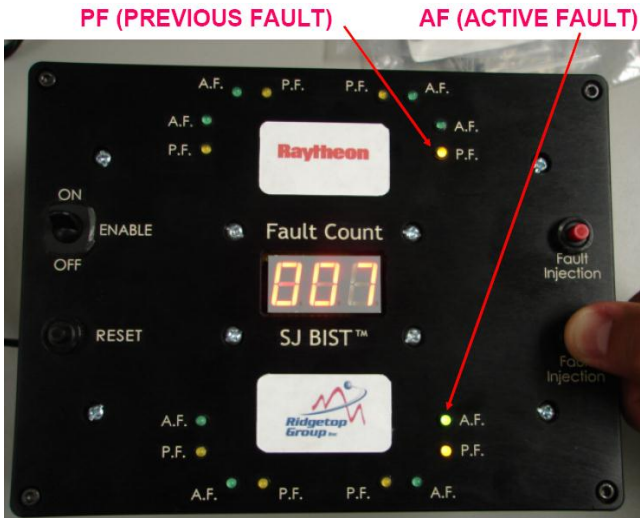


Figure 21: SJ BIST Demonstration Box.

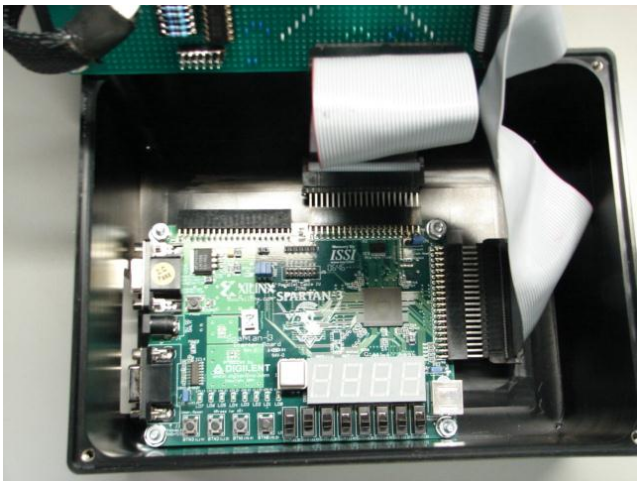


Figure 22: SJ BIST Demonstration Box, XILINX Spartan-3 XC3S200FT256 Board.

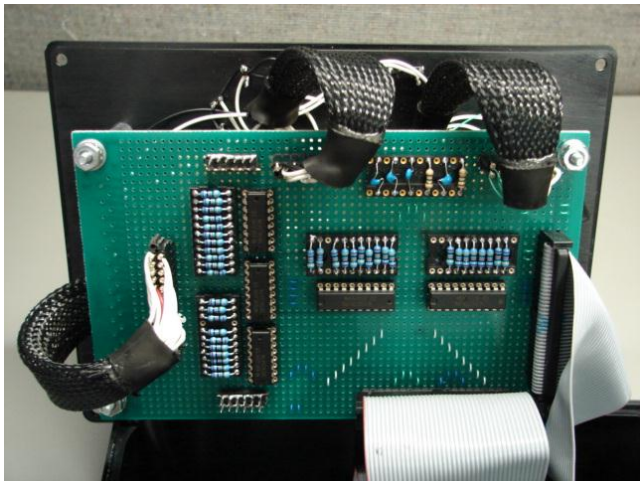


Figure 23: SJ BIST Demonstration Box, Display Board.

7. Summary and Conclusion

In this paper we provided updated information on SJ BIST. A brief overview of the mechanics-of-failure was included: the primary contributor to fatigue damage is thermo-mechanical stresses related to CTE mismatches, shock and vibration, and power on-off sequencing. Solder-joint fatigue damage can result in fractures that cause intermittent instances of high-resistance spikes that are hard-to-diagnose. In reliability testing, OPENS (faults) are often characterized by spikes of a 100Ω or more lasting for less than 100 ns to 1 μs or longer.

Prior to SJ BIST, there were no known methods for detecting high-resistance faults in solder-joint networks belonging to the I/O ports of operational, fully-programmed FPGAs.

An in-situ SJ BIST to test or monitor selected I/O pins is useful because stress magnitudes are hard to derive, which leads to inaccurate life expectancy predictions; and even though a particular damaged solder-joint port might not result in immediate FPGA operational failure, the damage indicates the FPGA is no longer reliable. SJ BIST can also be used in newly designed manufacturing reliability tests to investigate failure modes related to the PWB-FPGA assembly.

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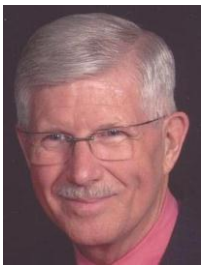

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