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0.04	Marcos Olmos	8-Mar-04	- Completed cosmic ray results of the LANSCE campaign in Feb 04. - Added FIT at 5,000 ft
0.05	Marcos Olmos	18-Mar-04	- Linked excel files copied in appendix A
0.06	Marcos Olmos	25-Mar-04	- Added executive summary
0.06A	Marcos Olmos	31 Mar-04	- Minor typographical errors corrected
0.07	Marcos Olmos	16-Apr-04	- Added alpha results for AX1000 and XC3S1000
0.08	Marcos Olmos	25-Oct-04	- Added alpha results for APA1000 - Added alpha results for XC2V3000 - Added alpha results for EP1C20

Applicable Documents

[1] Title: ASER test for FPGAs Commercial Proposal
Doc. Number: ACTEL 081903 v2
Version:
Date: Sep 03
Source: iRoC

[2] Title: JEDEC Standard - Measurement and Reporting of Alpha Particles and Terrestrial Cosmic-ray-Induced Soft Errors in Semiconductor Devices
Doc. Number: JESD89
Version:
Date: August 2001
Source: JEDEC

[3] Title: Test Plan for the SER Test of Actel, Xilinx and Altera FPGA instances
Doc. Number: GRE_2_ACTEL_SERTEST_DEC_03_ENG_TP_005
Version: 0.05
Date: 24-Nov-03
Source: iRoC

[4] Title: A. Taber and E. Normand, "Single Event Upset in Avionics", IEEE Trans. Nucl. Sci., NS-40, 120, 1993
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1 Executive summary

- Cosmic-ray and alpha-particle soft error rates were measured for five different architectures of FPGAs, from three different vendors, using three different programming technologies.
- Test methodology was compliant with JESD-89.
- SRAM-based FPGAs are liable to configuration SEU and SEFI when exposed to high-energy neutrons and alpha particles.
- Antifuse-based and Flash-based FPGAs did not exhibit any configuration SEU or SEFI when exposed to high-energy neutrons and alpha particles.
- Test results allowed the calculation of the ratio of SEFIs to SEUs.

2 Object

This test report provides the cosmic-ray SER of AX1000, APA1000, XC2V3000, XC3S1000 and EP1C20 devices. The cosmic-ray SER was measured at the LANSCE WNR facility at Los Alamos in February 2004.

The LANSCE results are compared with the preliminary SER of AX1000, APA1000 and XC2V3000 devices. The preliminary SER was measured using 14 MeV neutrons at the Interfaculty Reactor Institute (IRI) at Delft in The Netherlands in December 2003.

This test report also provides the alpha particle SER of AX1000, APA1000, XC2V3000, XC3S1000 and EP1C20 devices. The alpha particle SER was measured at iRoC premises using calibrated Am241 foil sources in April and October 2004.

The tests were conducted following the Test Plan [3]. Table 1 summarizes the tests performed for each device.

Mfg	Family	Device	14 MeV neutrons	Full spectrum neutrons	Alpha particles
Actel	Axcelerator	AX1000	√	√	√
Actel	ProASIC^{PLUS} Flash	APA1000	√	√	√
Xilinx	Virtex-II	XC2V3000	√	√	√
Xilinx	Spartan-3	XC3S1000		√	√
Altera	Cyclone	EP1C20		√	√

Table 1. Summary of test campaigns

This test report includes the description of the different tests performed during the experiments, and provides the detailed analysis and explanation of the FIT results.

2.1 Test strategy

This section recalls the test strategy. The test strategy is described in the Test Plan [3].

The test approach has special emphasis for the faults affecting the configuration memory.

The test strategy is based in the continuous monitoring of the outputs of a combinatorial circuit implemented in the FPGA under test. As soon as a permanent mismatch of the output values is observed, the test is stopped and the configuration memory read back and stored in a file. Additionally, the FPGA configuration memory is periodically read back, even if the output values are correct. The test strategy enables to identify the non critical and the critical SEU in the configuration memory, that is, those SEU in the configuration memory that do not create an error in the output, and those that create an error in the output.

The target circuit implemented in the DUT is composed of an array of 16x16-bit binary multipliers. Inputs of the multipliers are connected in parallel, and the outputs are connected to a multiplexer. The tester checks the output of each multiplier sequentially by means of the multiplexer. The main feature of this circuit is that

it is purely combinatorial and uses a large part of the Look-Up Table (LUT) resources. The absence of Flip-Flops ensures that fails occur only when the configuration memory is modified.

The test of the IO blocks (IOB) is accomplished by connecting a chain of IOB between the outputs of the multiplexer and the tester. In this way all the available IOB of the FPGA can be tested.

Figure 1 presents the block diagram of the target circuit.

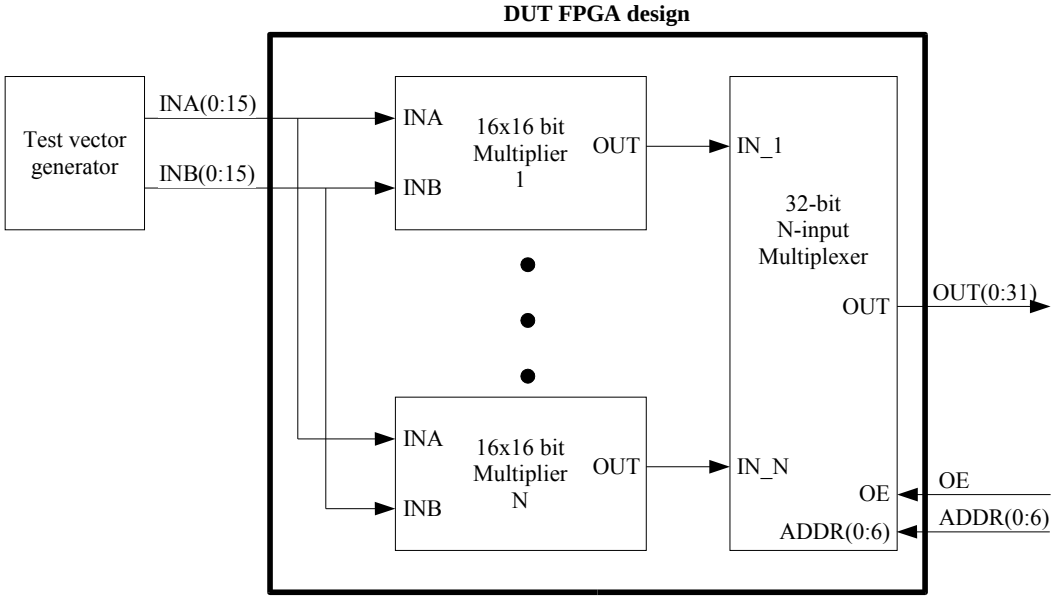


Figure 1. Test circuit block diagram

2.2 Error definition

This section recalls the error definitions. Error definitions are included in the Test Plan [3].

Type of error	Description
SEU in the configuration memory	A bit flip in the configuration memory caused by a single particle strike, neutron or alpha.
SEFI in the target circuit	A permanent mismatch of the output of the target circuit. It is created by a SEU in the configuration memory that alters the Look-Up Tables (LUT) or the routing of signals in the target circuit.
Configuration circuitry failure	A failure in the controlling circuitry of the FPGA. Configuration and read back operations fail.
Latchup	The activation of a parasitic structure in the silicon by a single neutron strike. The latchup effects are an increase of the current consumption and failures in the target circuit, the configuration memory or the controlling circuitry of the FPGA.
Hard error	A permanent failure in the FPGA that cannot be recovered after switching the beam off, switching the power off/on, and reconfiguration.

Table 2. Error definitions

3 14 MeV tests

3.1 Tested conditions and schedule

The following tables provide the sequence of conditions that were tested. Additionally to the test conditions, stability and consistency checks have been performed at the beginning and the end of each test sequence. A stability test (beam off) has been carried out before irradiation (cf. section 3.3). A consistency test (repetition of the first condition) has been carried out at the end of the test sequence The order of the test conditions follows the Test Plan [3].

The tables are extracted from the campaign logbook files in appendix A.1.

Run #	Device	Energy (MeV)	Start		Stop	Condition		
			Date	Time	Time	Cycle	VDD	Temp
1	AX1000	14	Dec-16	14:29:13	14:44:16	200ns	1.4	25°C
2	AX1000	14	Dec-16	14:47:15	16:59:27	200ns	1.4	25°C
3	AX1000	14	Dec-17	8:00:00	9:08:22	200ns	1.5	25°C
4	AX1000	14	Dec-17	9:10:42	10:21:37	200ns	1.6	25°C
5	AX1000	14	Note 1	Note 1	Note 1	200ns	1.4	25°C

Table 3. Conditions tested for AX1000

Run #	Device	Energy (MeV)	Start		Stop	Condition		
			Date	Time	Time	Cycle	VDD	Temp
1	APA1000	14	Dec-16	14:30:26	14:44:14	200ns	2.3	25°C
2	APA1000	14	Dec-16	14:47:31	16:59:35	200ns	2.3	25°C
3	APA1000	14	Dec-17	8:00:00	9:08:20	200ns	2.5	25°C
4	APA1000	14	Dec-17	9:10:45	10:21:34	200ns	2.7	25°C
5	APA1000	14	Note 1	Note 1	Note 1	200ns	2.3	25°C

Table 4. Conditions tested for APA1000

Run #	Device	Energy (MeV)	Start		Stop	Condition		
			Date	Time	Time	Cycle	VDD	Temp
1	XC2V3000	14	Dec-17	13:31:49	13:36:11	200ns	1.425	25°C
2	XC2V3000	14	Dec-17	13:36:31	14:29:04	200ns	1.425	25°C
3	XC2V3000	14	Dec-17	14:31:12	15:08:02	200ns	1.500	25°C
4	XC2V3000	14	Dec-17	15:08:40	15:46:06	200ns	1.575	25°C
5	XC2V3000	14	Dec-17	15:52:07	16:34:41	200ns	1.425	25°C

Table 5. Conditions tested for XC2V3000

Note 1: The consistency check, run #5, was not done for the AX1000 and APA1000 because no errors were observed for any of the conditions tested.

3.2 Devices tested

The following tables show the lot codes of the chips that were actually tested:

Chip 1	Chip 2	Chip 3
DOAAJ1 0320	DOJC21 0345	DOJC21 0345
Chip 4	Chip 5	
DOH5S21 0331	DOJC21 0345	

Table 6. Lot codes of the AX1000 chips tested

Chip 1	Chip 2	Chip 3
MF7G7 0247	MF7G7 0247	MF7G7 0247
Chip 4	Chip 5	Chip 6
MF7G7 0247	MF7G7 0247	MF7G7 0247

Table 7. Lot codes of the APA1000 chips tested

Chip 1	Chip 2	Chip 3
AGT0337 F2149925A	AGT0337 F2149925A	AGT0337 F2149925A
Chip 4	Chip 5	Chip 6
AGT0337 F2149925A	AGT0337 F2149925A	AGT0337 F2149925A

Table 8. Lot codes of the XC2V3000 chips tested

3.3 Stability without neutron beam

An error rate measurement is performed with the beam off and with the components placed in the target. The components are in the real environment with the real electromagnetic parasitic. This aims at verifying the robustness of both the tester and the DUT boards against the real noisy environment.

This experiment was done during 10 minutes for each DUT board and no error occurred (cf run #1 in Table 3 to Table 5).

4 14 MeV results

4.1 Cross-section and FIT calculation

The cross-section defines the sensitivity of a device. The cross-section per chip, as a function of neutron energy E, is defined as $\sigma(E)=N/(F*C)$ where N is the total number of errors, F is the fluence and C is the number of chips tested. In this document, the cross-section is given in cm²/chip.

The cross-section measured with 14 MeV neutrons is directly used to estimate the terrestrial failure rate. We approximate the full energy spectrum cross-section by the cross-section at 14 MeV. The approximation results in a lower estimate of the full spectrum cross-section because of the regular increase of cross-section at high energy. The full spectrum cross-section could be up to 50% higher than the 14 MeV cross-section.

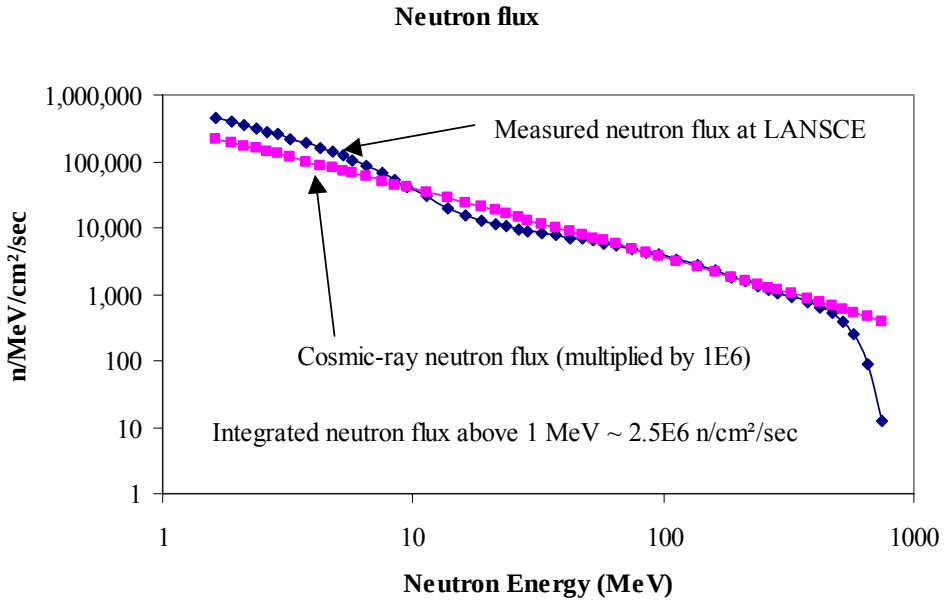


Figure 2. Cosmic-ray neutron flux at ground level

According to the JESD89 specification [2], the FIT rate is calculated using the value of neutron flux for the New-York City, f_{NYC} =14 n/cm^2/hour for neutrons with energy above 10 MeV. Thus, the FIT is given by the following formula:

$$FIT=\sigma*f_{NYC}*10^9 \text{ (errors/}10^9\text{ hour)}$$

Where σ is the cross-section given in cm²/chip, and f_{NYC} is the flux given in n/cm^2/hour.

The FIT is calculated using the neutron flux for the New-York City at sea level. The neutron flux depends on the altitude and location. Appendix E of the JESD89 specification [2] shows how to adjust the error rates calculated for the NYC for other locations.

4.2 Overall FIT results

Table 9 presents the overall cosmic-ray FIT for each device at sea level in NYC. The overall FIT is calculated as the average of all chips and test conditions for the XC2V3000. Appendix A details the cross-section and FIT for each chip and test condition.

Device	Overall FIT (SEFI) per Device	Overall FIT (SEU) per Device
AX1000	<0.017	<0.017
APA1000	<0.026	<0.026
XC2V3000	680	4700

Table 9. Overall cosmic-ray FIT at sea level in NYC

In Table 9, it is important to understand that no errors were observed for the AX1000 and APA1000, for anyof the test conditions. The given figure of FIT is an upper bound calculated considering one error for all chips and test conditions. The AX1000 and APA1000, based in Antifuse and Flash processes respectively, are considered insensitive to 14 MeV neutrons, therefore extending the test for longer periods would still produce no errors, and result in lower bounds of FIT.

The neutron flux increases with altitude, and has a maximum at approximately 60,000 ft. The FIT at sea level, 5,000 ft, 30,000 ft and 60,000 ft is provided in Table 10:

Device	FIT (SEFI) at sea level	FIT (SEFI) at 5,000 ft	FIT (SEFI) at 30,000 ft	FIT (SEFI) at 60,000 ft
AX1000	<0.017	<0.058	<2.5	<8.1
APA1000	<0.026	<0.089	<3.8	<12
XC2V3000	680	2,300	99,000	320,000

Table 10. Overall cosmic-ray FIT at different altitudes

The altitude effect at 5,000 ft and 30,000 ft is evaluated using the formula provided in appendix E of JESD89 [2]:

$$\text{Neutron flux (n/cm}^2\text{/hour)} = 15E3 * e^{-(A/148)}$$

Where the altitude, a, in feet above sea level, is expressed as the areal density of the air column, A, in units of g/cm². The altitude, a, can be converted to the areal density, A using the following equation:

$$A = 1033 \times \exp[-.03813 \times (a/1000) - .00014 \times (a/1000)^2 + 6.4E\text{-}7 \times (a/1000)^3]$$

The altitude effect at 60,000 ft is evaluated using Figure 3 from reference [4].

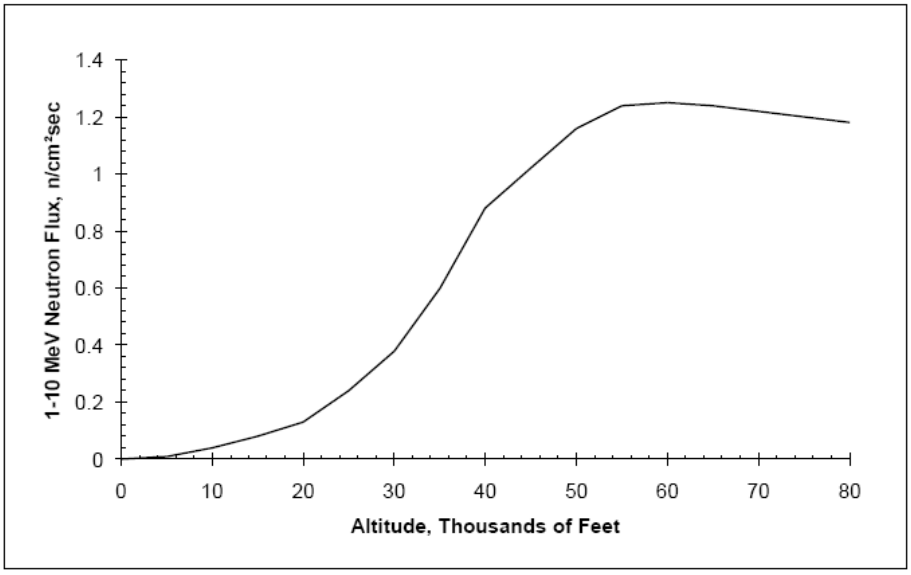


Figure 3. Neutron flux vs altitude

4.3 Accuracy of results

The accuracy of the cross-section results is assessed in this section. The accuracy of the cross-section is the sum of the error count and fluence measurement accuracies.

4.3.1 Error count statistics

The error count is generally described by a Poisson distribution, cf appendix C.1 in [2]. If N errors occur, the mean error count is approximated by N. The standard deviation is given by √N.

The error count can be bounded using the upper and lower limits in Table 11, extracted from appendix C.2 of [2]. In using this table, the first column is the actual number of events observed in the experiment. The upper and lower limits define the 95% confidence interval for the true mean of the distribution. The upper and lower limits for any number of events can be calculated using the formulas given in appendix B.

	95% confidence limit	
Events	Lower limit	Upper limit
0	0.0	3.7
1	0.0	5.6
2	0.2	7.2
3	0.6	8.8
4	1.1	10.2
5	1.6	11.7
6	2.2	13.1
7	2.8	14.4
8	3.5	15.8
9	4.1	17.1
10	4.8	18.4
20	12.2	30.9
50	37.1	65.9
100	81.4	121.6

Table 11. 95% confidence limits for small number of events

The accuracy of the error count is defined in this report using 95% confidence intervals. The 95% confidence limits depend on the number of errors observed. The number of errors is detailed in appendix A for each chip and test condition.

The following table summarizes the 95% confidence intervals for each device. For example, the overall number of SEFI per chip and test condition is 18 for the XC2V3000. By using the formulas given in appendix B, we find that the lower and upper limits are 10.7 and 28.4 respectively. The limits in Table 12 are calculated as (Lower limit/Mean error count – 1)*100 = -41%, and (Upper limit/Mean error count – 1)*100 = +58%.

Device	Error type	Mean error count	Lower limit	Upper limit	Comment
AX1000	SEFI	0	n/a	n/a	No errors observed
APA1000	SEFI	0	n/a	n/a	No errors observed
XC2V3000	SEFI	18	-41%	+58%	Errors per chip and test condition
		105	-18%	+21%	Errors for all chips per test condition
		420	-9%	+10%	Errors for all chips and test conditions
	SEU	122	-17%	+19%	Errors per chip and test condition
		730	-7%	+8%	Errors for all chips per test condition

Table 12. 95% confidence intervals for all devices

4.3.2 Fluence measurement accuracy

The accuracy of the fluence measurement is better than 10% for the IRI facility.

4.4 Detailed analysis

Detailed analysis of the results is presented hereafter. The following table summarizes the analyses presented for each device:

Analysis	AX1000	APA1000	XC2V3000
Voltage influence on FIT			√
Analysis of critical vs non critical SEU			√
Analysis of single event latchup	√	√	√
Bitmaps of errors			√
Chip to chip variations			√
Special observations	√	√	√

Table 13. Detailed analysis for 14 MeV tests

Many of the detailed analysis cannot be performed for the AX1000 and APA1000 because no errors were observed for these devices.

4.4.1 Voltage influence on FIT

The SEFI and SEU FIT dependence vs VDD is presented in this section. The FIT is plotted separately for each chip. The FIT average of all chips is also plotted, and the average FIT is used to fit an exponential curve.

Figure 4 and Figure 5 show a regular decrease of FIT at the higher VDD, as expected.

The FIT dispersion between chips is consistent with the accuracy assessments given in section 4.3.

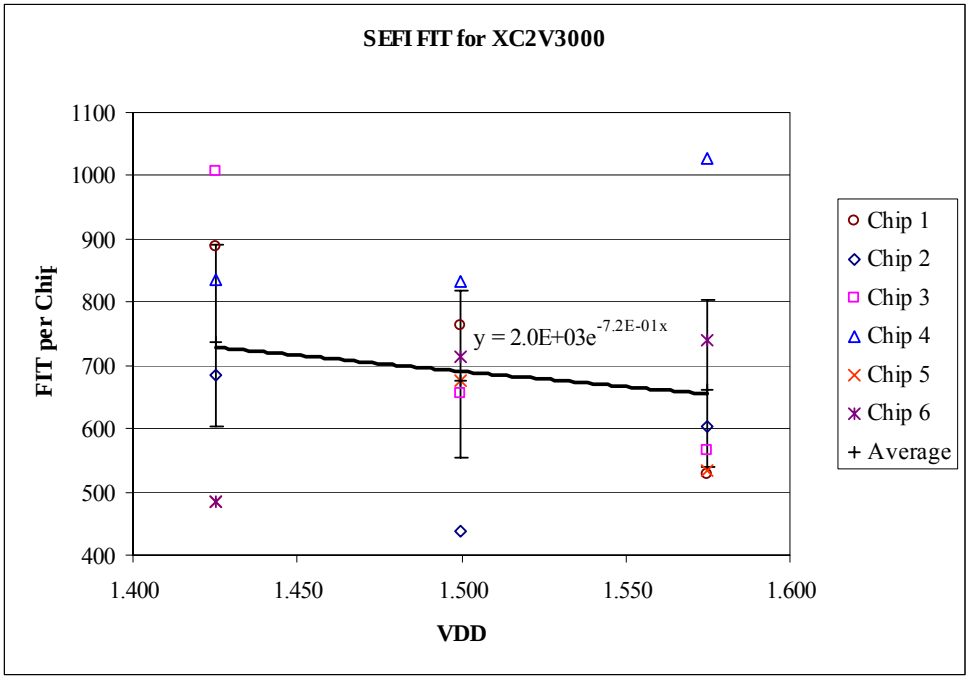


Figure 4. SEFI FIT of XC2V3000 vs VDD

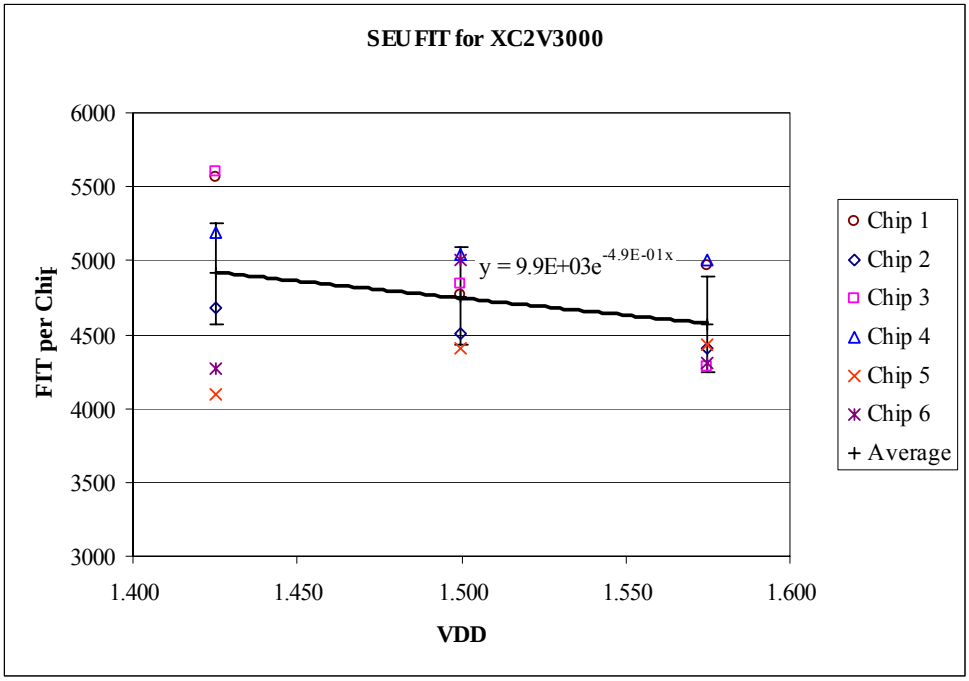


Figure 5. SEU FIT of XC2V3000 vs VDD

4.4.2 Analysis of critical vs non critical SEU

The test strategy enables to identify the critical and the non critical SEU in the configuration memory, that is, those SEU in the configuration memory that create an SEFI, and those that do not create an SEFI.

Figure 6 presents the ratio SEFI / Total SEU for each chip and test condition. The overall ratio is 15% independent of the test condition.

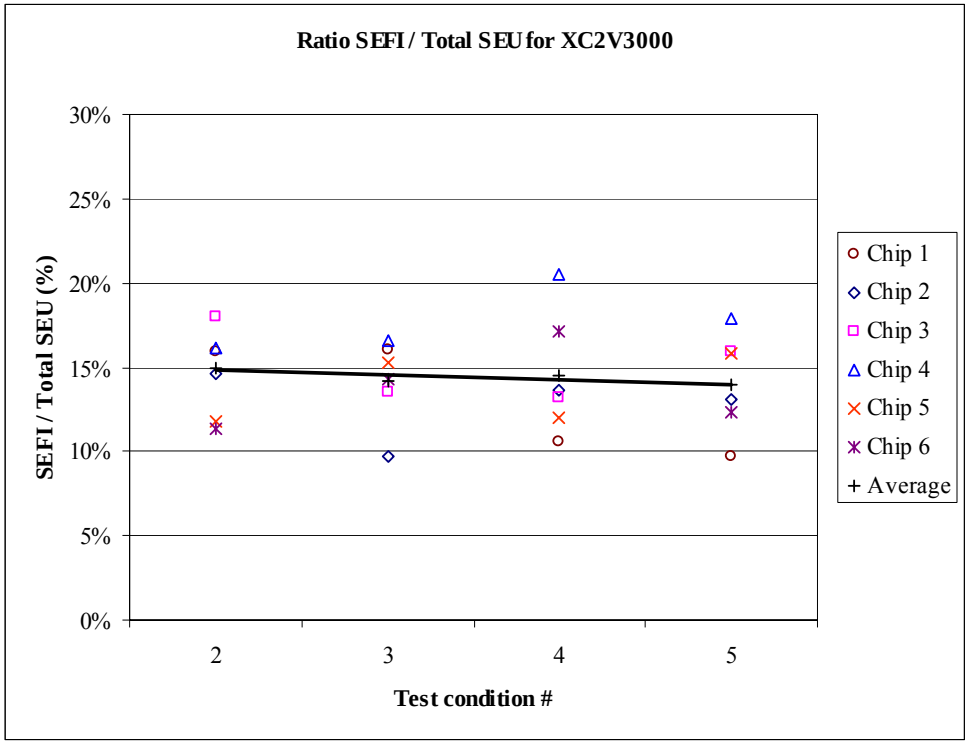


Figure 6. SEFI vs Total SEU XC2V3000

4.4.3 Analysis of single event latchup

Single event latchup (SEL) consists in the neutron induced activation of parasitic thyristor structures in the CMOS process. In case a process is sensitive to latchup, the latchup rate is higher at the higher voltage, temperature and particle energy.

Latchups result in increased current consumption, partial or total configuration memory wipe out, or complete loss of operation. Because the current is limited for protection, latchups lead to voltage shutdown to the DUT. The way the tester detects latchups is by monitoring the DUT supply voltages. In case a latchup is detected, the tester logs the event and switches the power off/on for recovering.

A particular case of latchup is the microlatchup. The microlatchup consists in the activation of a parasitic thyristor structure with weak on-resistance and a low increase of current consumption. In case of microlatchup, the voltage and current can find a stability point that cannot be detected by the tester. In this case, one or more chips are partially or totally wiped out, or experience complete loss of operation during the duration of a test condition.

No latchups were detected for any of the devices and conditions tested. In the following subsections, the voltage and current waveforms, acquired during the experiments, will be presented for each device and test condition. The sensitivity to microlatchup will be analyzed by inspection of the voltage and current waveforms and correlation with the observed number of errors in each chip.

4.4.3.1 AX1000

We observe regular voltage and current waveforms in Figure 7 and Figure 8. No errors were observed for any of the chips and conditions tested. Therefore, there is no indication of latchup.

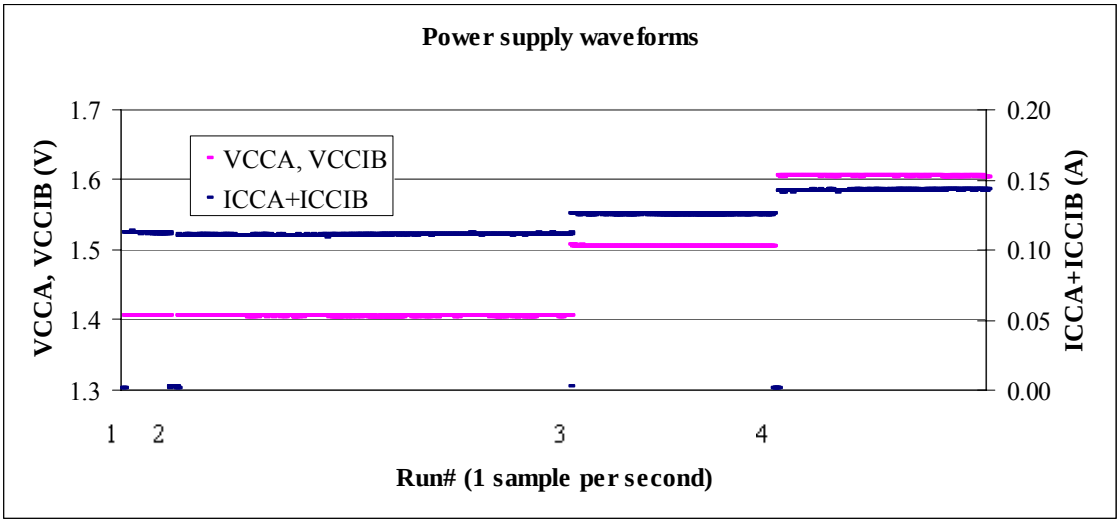


Figure 7. AX1000 VCCA and VCCIB waveforms

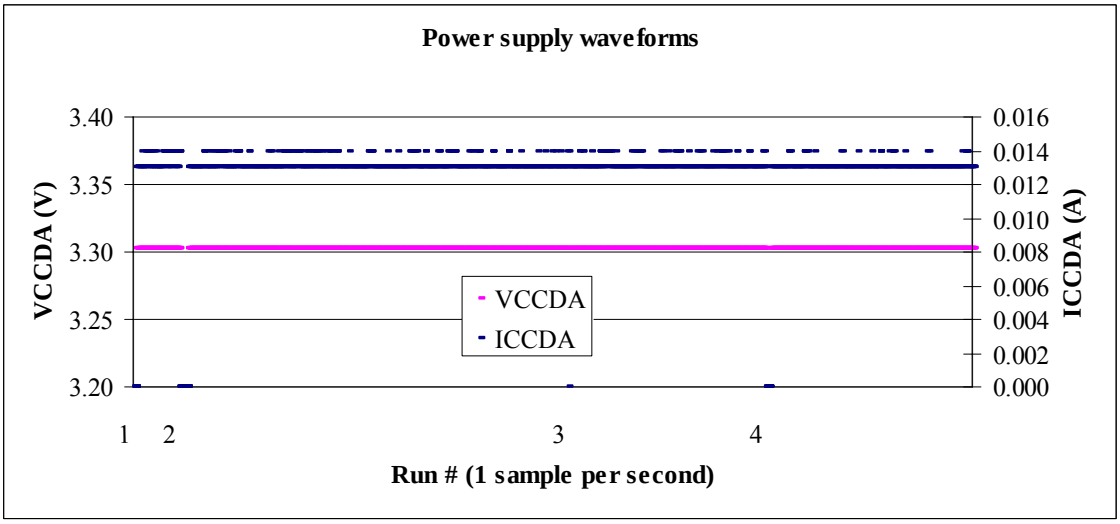


Figure 8. AX1000 VCCDA waveform

4.4.3.2 APA1000

We observe regular voltage and current waveforms in Figure 9 and Figure 10. No errors were observed for any of the chips and conditions tested. Therefore, there is no indication of latchup.

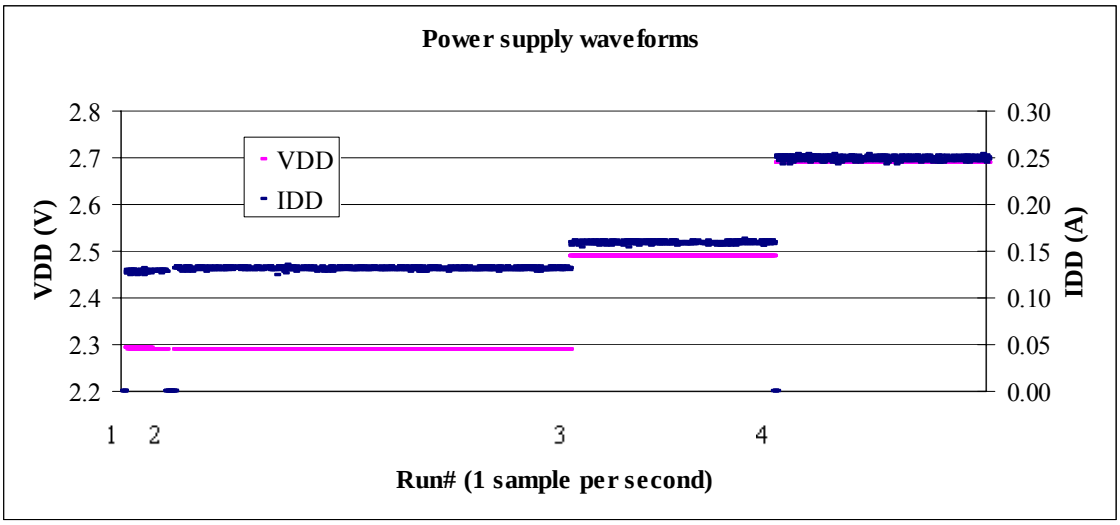


Figure 9. APA1000 VDD waveform

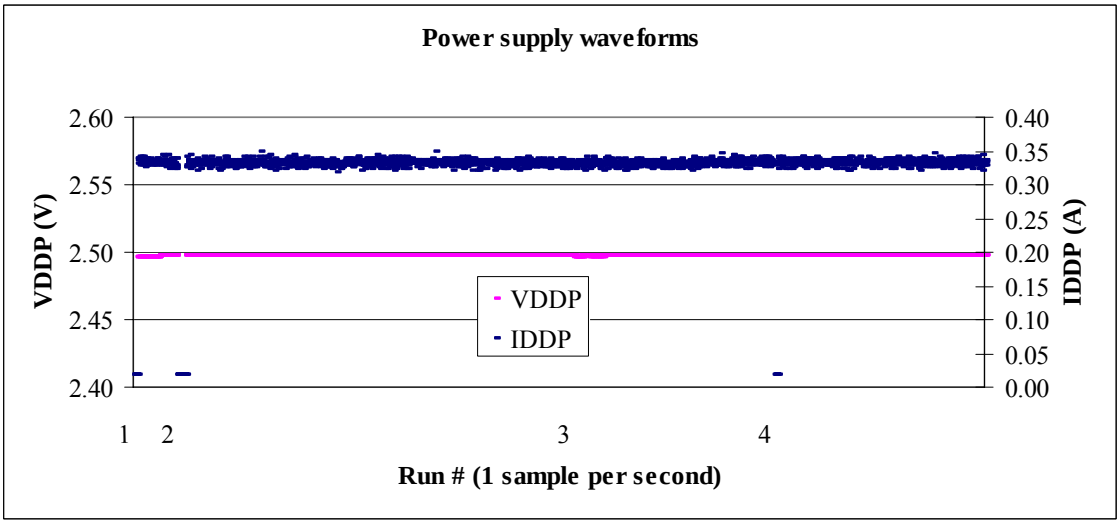


Figure 10. APA1000 VDDP waveform

4.4.3.3 XC2V3000

We observe regular voltage and current waveforms in Figure 11 and Figure 12. The number of errors, presented in the following table is regular across the six chips tested. Therefore, there is no indication of latchup.

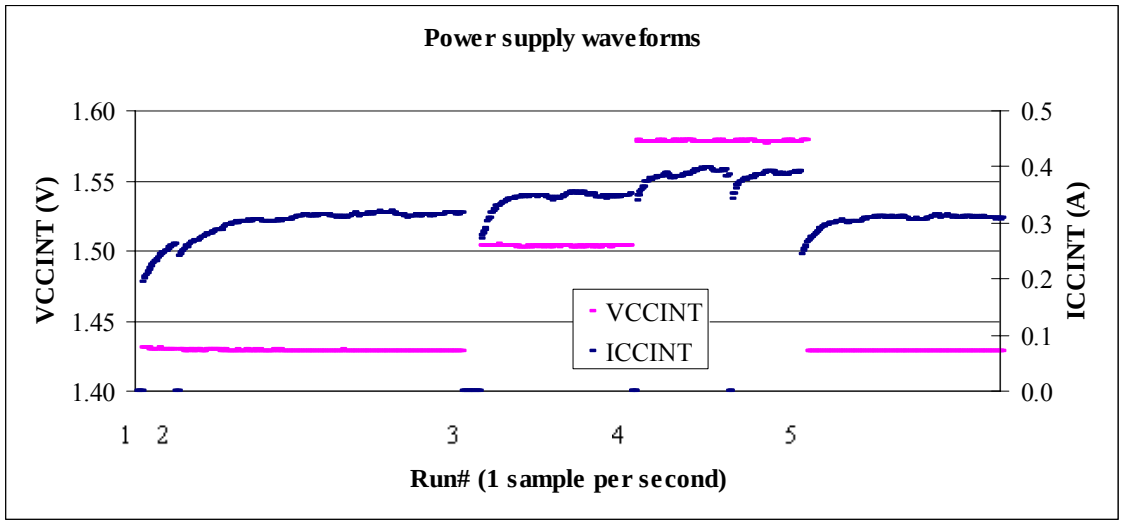


Figure 11. XC2V3000 VCCINT waveform

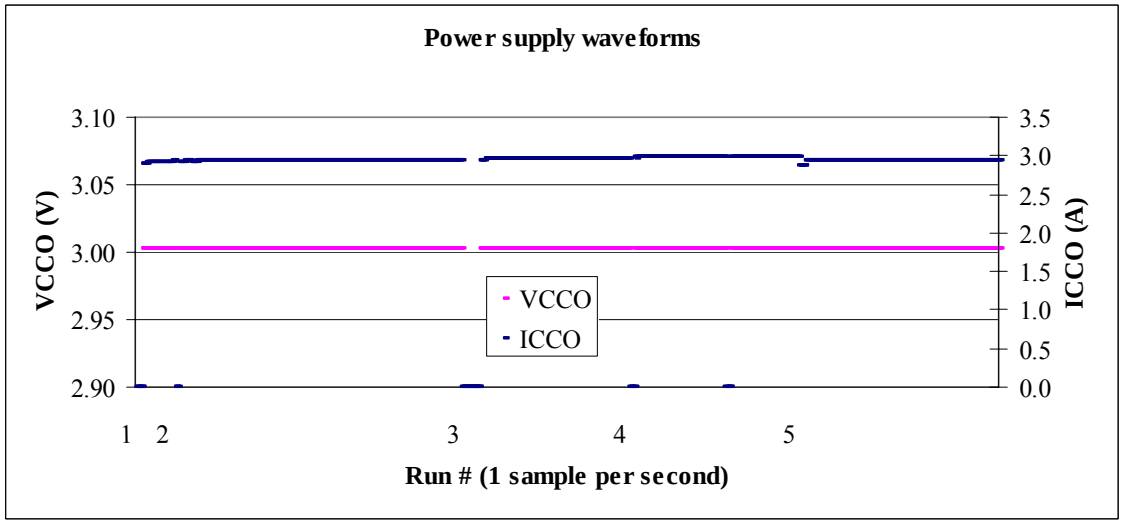


Figure 12. XC2V3000 VCCO waveform

Run #	Condition	Number of SEFI					
	VDD	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6
1	1.425	0	0	0	0	0	0
2	1.425	22	17	25	19	11	11
3	1.500	21	12	18	21	17	18
4	1.575	14	16	15	25	13	18
5	1.425	14	18	23	20	16	16

Table 14. XC2V3000 number of SEFI for each chip

Note: run #1 was a test run with the beam switched off, to test that the tester electronics was working correctly (cf section 3.3).

4.4.4 Bitmaps of errors

Bitmaps allow to check the expected random distribution of errors in the configuration memory arrays.

Each point in the bitmap represents a failing address. The bitmaps are logical bitmaps, not physical bitmaps, because the layout of the configuration memory is not available. In the logical bitmaps, the address LSB are mapped in the x-axis and the address MSB are mapped in the y-axis.

The address refers to the location where the verification bitstream is stored in the tester memory. Valid addresses for the XC2V3000 are in the range 0x400069 to 0x5D4329. Each address holds 5 bits. Therefore, the verification bitstream length is 9,588,165 bits.

The bitmaps show the expected random distribution of errors.

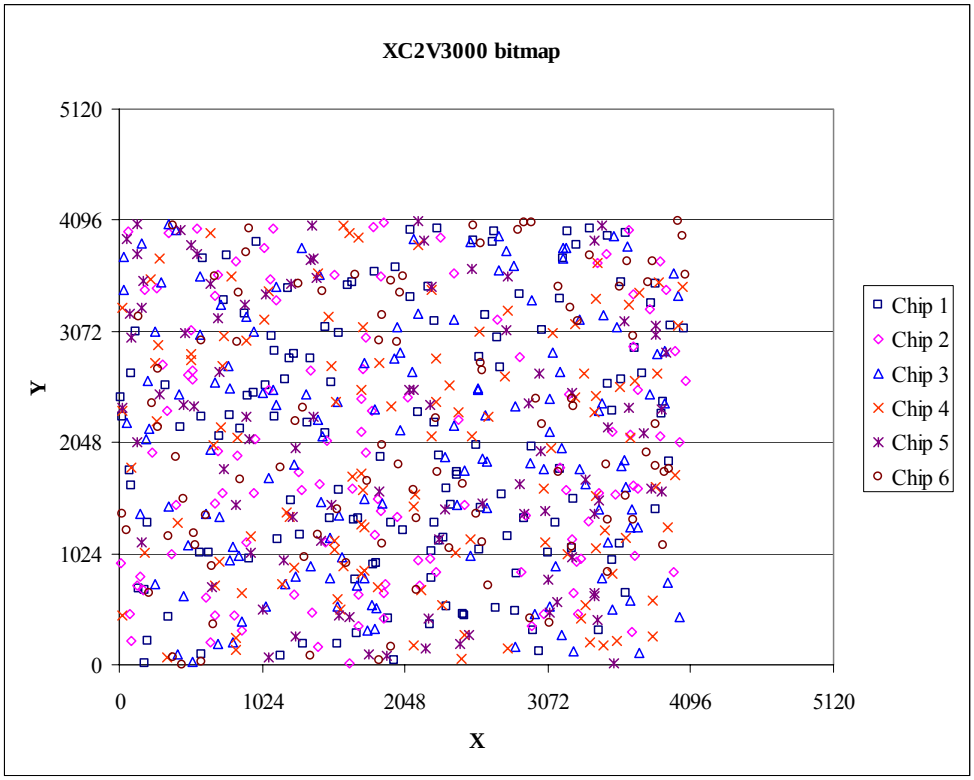


Figure 13. Bitmap for run#2 of XC2V3000

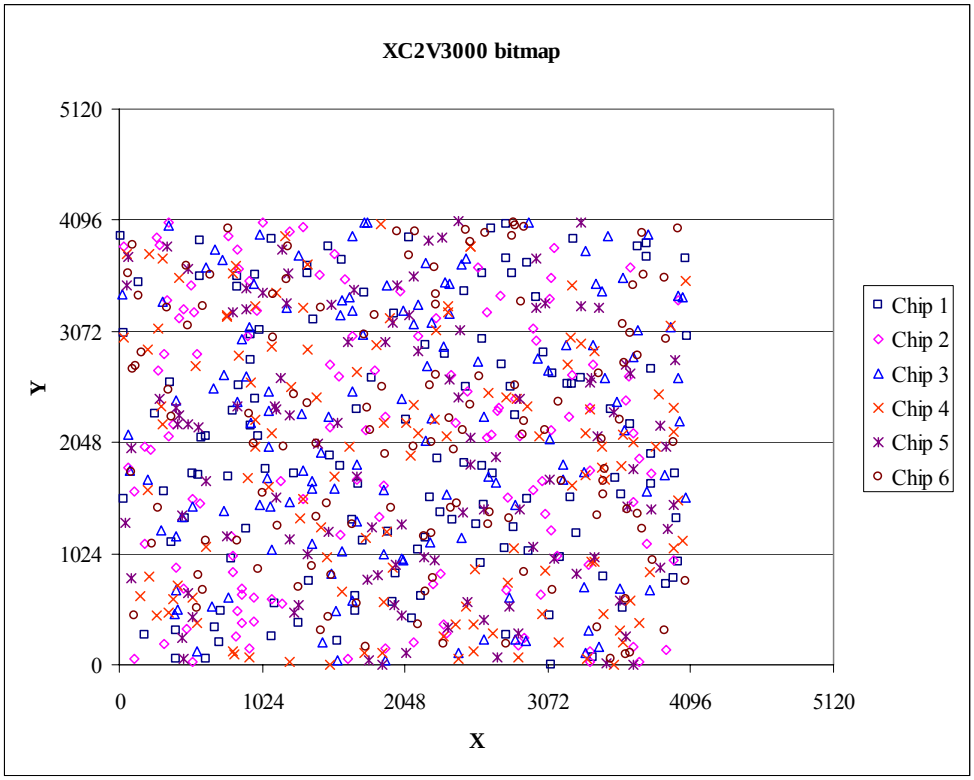


Figure 14. Bitmap for run#3 of XC2V3000

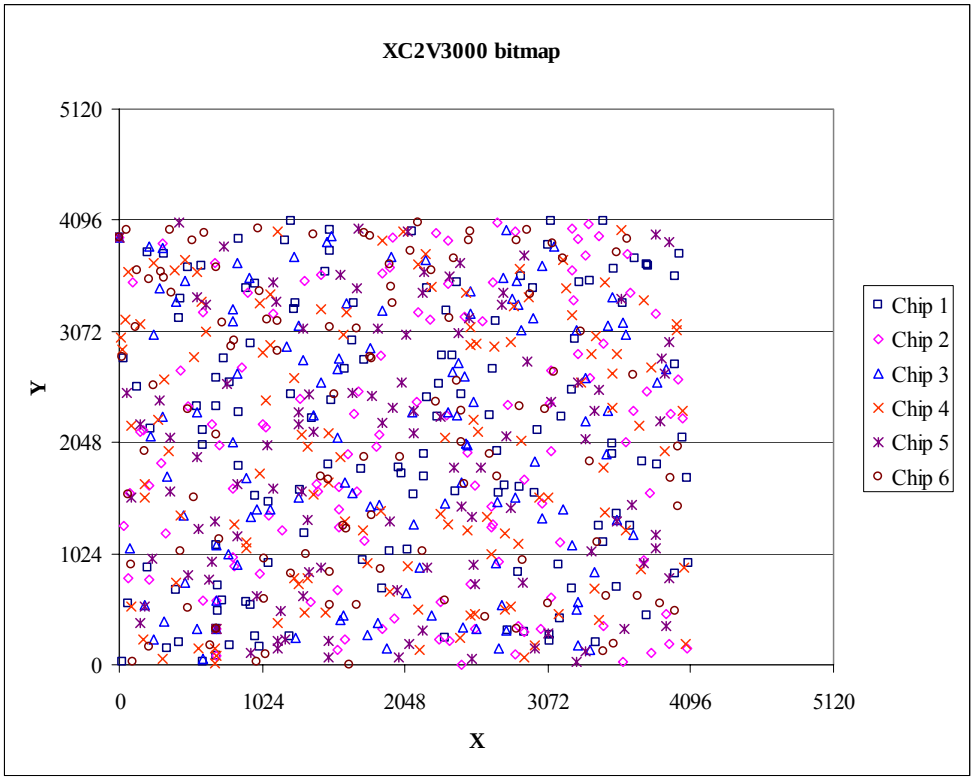


Figure 15. Bitmap for run#4 of XC2V3000

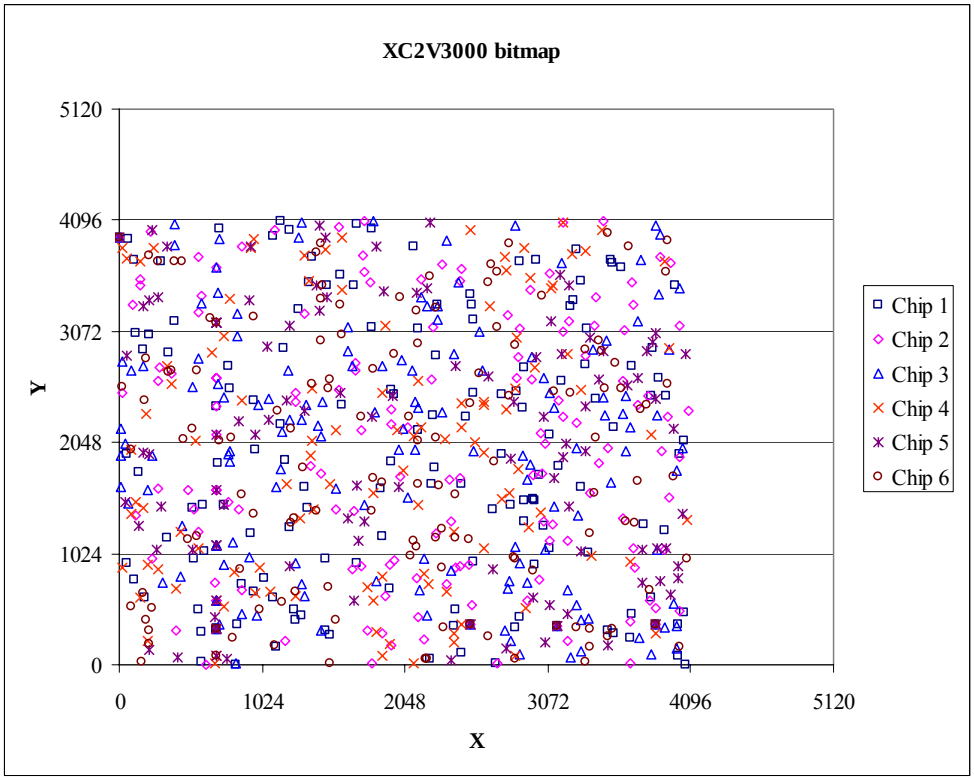


Figure 16. Bitmap for run#5 of XC2V3000

4.4.5 Chip to chip variation

This section presents the chip to chip FIT variations observed. The objective of this section is to check the neutron flux uniformity.

The FIT variations shown in Figure 17 are defined as the variation relative to the average of the 6 chips tested.

$$\text{FIT variation for chip(i) (\%)} = \left(\frac{\text{FIT Chip(i)}}{\text{Average FIT Chips(1 to 6)}} - 1 \right) \times 100$$

The FIT variations observed are within the expected statistical uncertainty: –17% to +19%, see Table 12. Therefore, we verify that the neutron flux is uniform.

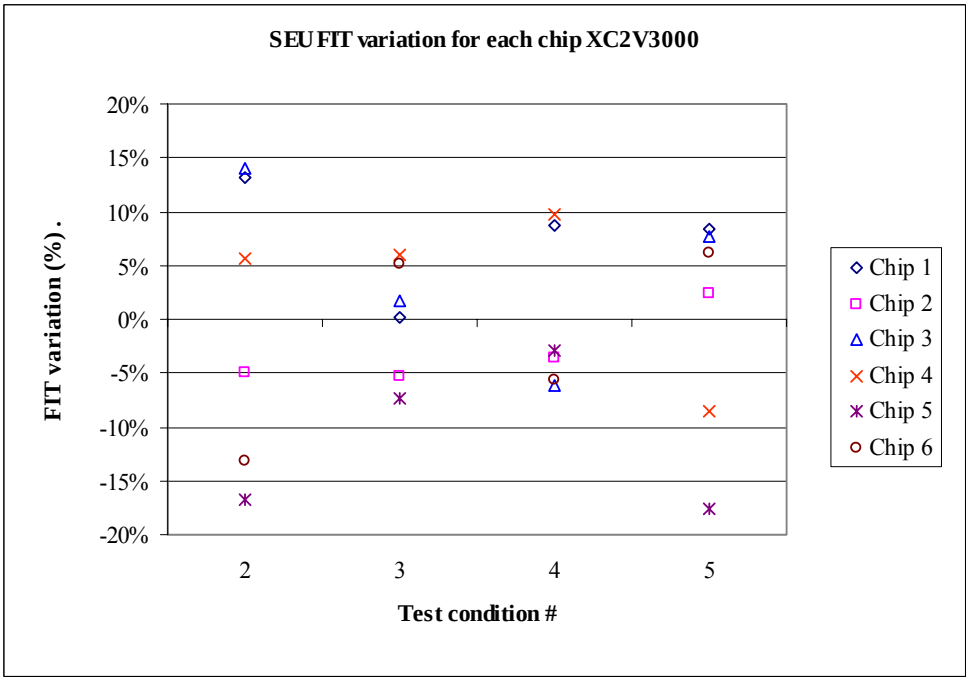


Figure 17. Chip to chip FIT variation

4.4.6 Consistency check

A consistency test (repetition of the first condition) has been carried out at the end of the test sequence. The consistency test verifies the stability of the beam, DUT and tester.

Figure 18 verifies that the results of runs #2 and #5 are consistent, taking into account the statistical uncertainty shown by the error bars.

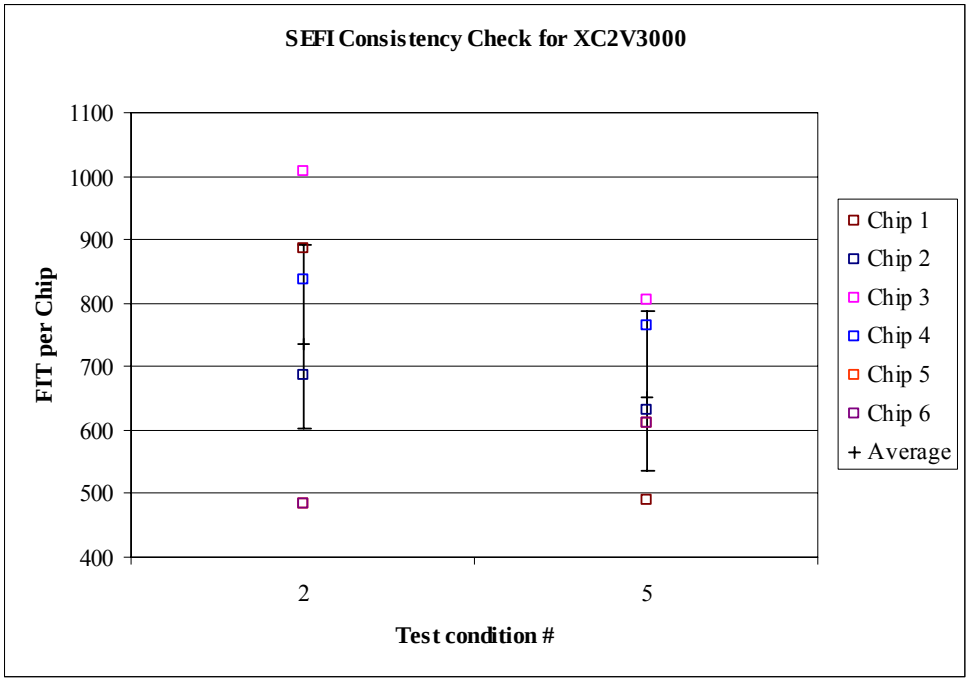


Figure 18. SEFI consistency check for XC2V3000

4.4.7 Special observations

A verify operation using the Flash Pro programmer was performed for the APA1000 chips, at the end of the radiation tests performed. The verify operation was successful for all the APA1000 chips.

5 14 MeV conclusions

The preliminary cosmic-ray SER of AX1000, APA1000 and XC2V3000 devices was measured using 14 MeV neutrons at the Interfaculty Reactor Institute (IRI) at Delft in The Netherlands in December 2003.

Table 15 presents the overall cosmic-ray FIT for each device at sea level in NYC. The overall FIT is calculated as the average of all chips and test conditions for the XC2V3000.

Device	Overall FIT (SEFI) per Device	Overall FIT (SEU) per Device
AX1000	<0.017	<0.017
APA1000	<0.026	<0.026
XC2V3000	680	4700

Table 15. Overall cosmic-ray FIT at sea level in NYC

In Table 15, it is important to understand that no errors were observed for the AX1000 and APA1000, for any of the test conditions. The given figure of FIT is an upper bound calculated considering one error for all chips and test conditions. The AX1000 and APA1000, based in Antifuse and Flash processes respectively, are considered insensitive to 14 MeV neutrons, therefore extending the test for longer periods would still produce no errors, and result in lower bounds of FIT.

The neutron flux increases with altitude, and has a maximum at approximately 60,000 ft. The FIT at sea level, 5,000 ft, 30,000 ft and 60,000 ft is provided in Table 16.

Device	FIT (SEFI) at sea level	FIT (SEFI) at 5,000 ft	FIT (SEFI) at 30,000 ft	FIT (SEFI) at 60,000 ft
AX1000	<0.017	<0.058	<2.5	<8.1
APA1000	<0.026	<0.089	<3.8	<12
XC2V3000	680	2,300	99,000	320,000

Table 16. Overall cosmic-ray FIT at different altitudes

No occurrences of latchup have been observed for any of the devices.
No errors in the configuration circuitry of the XC2V3000 were observed.
No hard errors were observed for any of the devices.

It is important to understand that we approximate the full energy spectrum cross-section by the cross-section at 14 MeV. The approximation results in a lower estimate of the full spectrum cross-section, that could be up to 50% higher than the 14 MeV cross-section. Additionally, devices that are not sensitive to latchup for 14 MeV neutrons, can be sensitive for neutrons of higher energy. Therefore, full spectrum tests at LANSCE will be performed to consolidate these preliminary results.

6 LANSCE tests

6.1 Tested conditions and schedule

The following tables provide the sequence of conditions that were tested. Additionally to the test conditions, stability and consistency checks have been performed at the beginning and the end of each test sequence. A stability test (beam off) has been carried out before irradiation (cf. section 6.3). A consistency test (repetition of the first condition) has been carried out at the end of the test sequence The order of the test conditions follows the Test Plan [3].

The tables are extracted from the campaign logbook files in appendix A.2.

Run #	Device	Energy (MeV)	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	AX1000	LANSCE	17-Feb	14:27:15	17-Feb	14:38:02	200ns	1.4	25°C
2	AX1000	LANSCE	17-Feb	15:46:19	17-Feb	22:40:35	200ns	1.4	25°C
3	AX1000	LANSCE	17-Feb	22:41:50	18-Feb	4:27:11	200ns	1.5	25°C
4	AX1000	LANSCE	18-Feb	4:28:29	18-Feb	9:46:52	200ns	1.6	25°C
5	AX1000	LANSCE	Note 1	Note 1	Note 1	Note 1	200ns	1.4	25°C

Table 17. Conditions tested for AX1000

Note 1: The consistency check, run #5, was not done for the AX1000 because no errors were observed for any of the conditions tested.

Run #	Device	Energy (MeV)	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	APA1000	LANSCE	18-Feb	10:36:44	18-Feb	10:46:44	200ns	2.3	25°C
2	APA1000	LANSCE	18-Feb	10:47:46	18-Feb	15:21:14	200ns	2.3	25°C
3	APA1000	LANSCE	18-Feb	15:22:12	18-Feb	21:07:56	200ns	2.5	25°C
4	APA1000	LANSCE	18-Feb	21:09:08	19-Feb	5:55:00	200ns	2.7	25°C
5	APA1000	LANSCE	19-Feb	5:56:33	19-Feb	21:26:26	200ns	2.3	25°C

Table 18. Conditions tested for APA1000

No errors were observed for any of the conditions tested for the APA1000. The consistency check, run #5, was done because beam time was available, to increase the fluence and thus the accuracy of the FIT bound.

Run #	Device	Energy (MeV)	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	XC2V3000	LANSCE	17-Feb	14:28:11	17-Feb	14:38:56	200ns	1.425	25°C
2	XC2V3000	LANSCE	17-Feb	15:46:53	17-Feb	15:57:28	200ns	1.425	25°C
3	XC2V3000	LANSCE	17-Feb	15:59:04	17-Feb	16:09:44	200ns	1.500	25°C
4	XC2V3000	LANSCE	17-Feb	16:10:38	17-Feb	16:22:29	200ns	1.575	25°C
5	XC2V3000	LANSCE	17-Feb	16:23:38	17-Feb	16:35:45	200ns	1.425	25°C

Table 19. Conditions tested for XC2V3000

Run #	Device	Energy (MeV)	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	XC3S1000	LANSCE	17-Feb	17:16:20	17-Feb	17:25:22	200ns	1.140	25°C
2	XC3S1000	LANSCE	17-Feb	17:25:56	17-Feb	17:51:15	200ns	1.140	25°C
3	XC3S1000	LANSCE	17-Feb	17:52:36	17-Feb	19:40:45	200ns	1.200	25°C
4	XC3S1000	LANSCE	17-Feb	19:41:23	17-Feb	20:07:31	200ns	1.260	25°C
5	XC3S1000	LANSCE	17-Feb	20:08:11	17-Feb	20:23:55	200ns	1.140	25°C

Table 20. Conditions tested for XC3S1000

Run #	Device	Energy (MeV)	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	EP1C20	LANSCE	17-Feb	20:58:26	17-Feb	21:08:40	200ns	1.425	25°C
2	EP1C20	LANSCE	17-Feb	21:09:30	17-Feb	21:27:50	200ns	1.425	25°C
3	EP1C20	LANSCE	17-Feb	21:49:43	17-Feb	22:03:20	200ns	1.500	25°C
4	EP1C20	LANSCE	17-Feb	22:04:36	17-Feb	22:21:21	200ns	1.575	25°C
5	EP1C20	LANSCE	17-Feb	22:22:38	17-Feb	22:39:26	200ns	1.425	25°C

Table 21. Conditions tested for EP1C20

6.2 Devices tested

The following tables show the lot codes of the chips that were actually tested:

Chip 1	Chip 2	Chip 3
DOAAJ1 0320	DOJC21 0345	DOJC21 0345
Chip 4	Chip 5	
DOH5S21 0331	DOJC21 0345	

Table 22. Lot codes of the AX1000 chips tested

Chip 1	Chip 2	Chip 3
MF7G7 0247	MF7G7 0247	MF7G7 0247
Chip 4	Chip 5	
MF7G7 0247	MF7G7 0247	

Table 23. Lot codes of the APA1000 chips tested

Chip 1	Chip 2	Chip 3
AGT0337 F2149925A	AGT0337 F2149925A	AGT0337 F2149925A
Chip 4	Chip 5	Chip 6
AGT0337 F2149925A	AGT0337 F2149925A	AGT0337 F2149925A

Table 24. Lot codes of the XC2V3000 chips tested

Chip 1	Chip 2	Chip 3
FT256AFQ0341 D13989A	FT256AFQ0341 D13989A	FT256AFQ0341 D13990A
Chip 4	Chip 5	Chip 6
FT256AFQ0341 D13989A	FT256AFQ0341 D13989A	FT256AFQ0341 D13989A

Table 25. Lot codes of the XC3S1000 chips tested

Chip 1	Chip 2	Chip 3
EP1C20F324C8 AAD900313A	EP1C20F324C8 AAD900313A	EP1C20F324C8 AAD900313A
Chip 4	Chip 5	Chip 6
EP1C20F324C8 AAD900313A	EP1C20F324C8 AAD900313A	EP1C20F324C8 AAD900313A

Table 26. Lot codes of the EP1C20 chips tested

6.3 Stability without neutron beam

An error rate measurement is performed with the beam off and with the components placed in the target. The components are in the real environment with the real electromagnetic parasitic. This aims at verifying the robustness of both the tester and the DUT boards against the real noisy environment.

This experiment was done during 10 minutes for each DUT board and no error occurred (cf run #1 in Table 17 to Table 21).

7 LANSCE results

7.1 Cross-section and FIT calculation

The cross-section defines the sensitivity of a device. The cross-section per chip, as a function of neutron energy E, is defined as $\sigma(E)=N/(F*C)$ where N is the total number of errors, F is the fluence and C is the number of chips tested. In this document, the cross-section is given in cm²/chip.

Since the WNR neutron beam has a neutron energy spectrum very similar to the terrestrial neutron energy spectrum, the cross-section per bit obtained at WNR can be used directly to estimate the terrestrial failure rate.

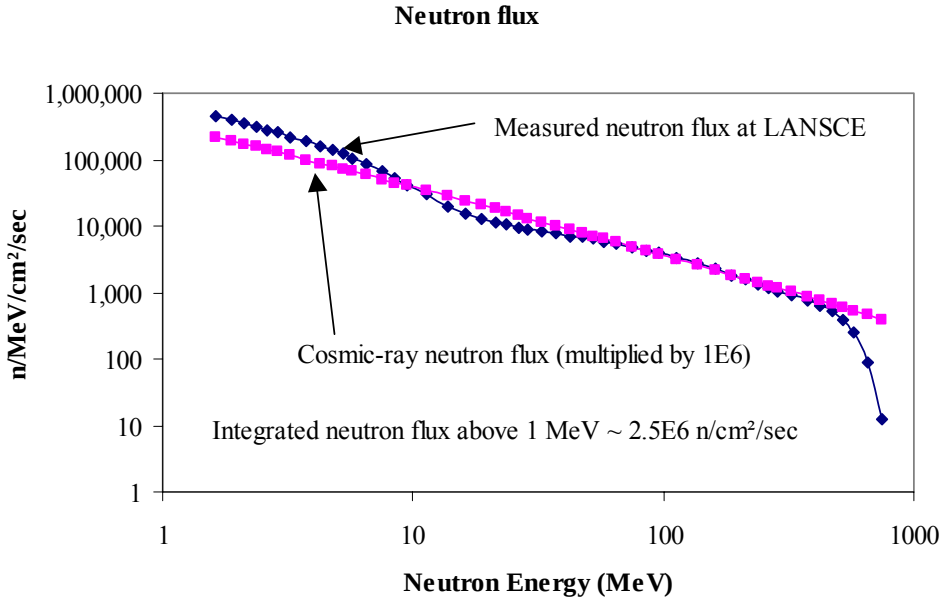


Figure 19. Cosmic-ray neutron flux at ground level

According to the JESD89 specification [2], the FIT rate is calculated using the value of neutron flux for New-York City, f_{NYC} =14 n/cm²/hour for neutrons with energy above 10 MeV. The FIT is calculated in this report for one device. Thus, the FIT is given by the following formula:

$$FIT=\sigma*f_{NYC}*10^9 \text{ (errors/}10^9\text{ hour)}$$

Where σ is the cross-section given in cm²/chip, and f_{NYC} is the flux given in n/cm^2/hour.

The FIT is calculated using the neutron flux for the New-York City at sea level. The neutron flux depends on the altitude and location. Appendix E of the JESD89 specification [2] shows how to adjust the error rates calculated for the NYC for other locations.

7.2 Overall FIT results

Table 27 presents the overall cosmic-ray FIT for each device at sea level in NYC. The overall FIT is calculated as the average of all chips and test conditions for the XC2V3000, XC3S1000 and EP1C20 devices. Appendix A details the cross-section and FIT for each chip and test condition.

Device	Overall FIT (SEFI) per Device	Overall FIT (SEU) per Device
AX1000	<0.082	<0.082
APA1000	<0.038	<0.038
XC2V3000	1,150	8,680
XC3S1000	320	1,240
EP1C20	460	n/a

Table 27. Overall cosmic-ray FIT at sea level in NYC

In Table 27, it is important to understand that no errors were observed for the AX1000 and APA1000, for any of the test conditions. The given figure of FIT is an upper bound calculated considering one error for all chips and test conditions. The AX1000 and APA1000, based in Antifuse and Flash processes respectively, are considered insensitive to terrestrial spectrum of neutrons, therefore extending the test for longer periods would still produce no errors, and result in lower bounds of FIT.

The readback of the configuration memory is not available for the EP1C20. Therefore, the SEU FIT could not be measured for the EP1C20.

The neutron flux increases with altitude, and has a maximum at approximately 60,000 ft. The FIT at sea level, 5,000 ft, 30,000 ft and 60,000 ft is provided in Table 28.

Device	FIT (SEFI) at sea level	FIT (SEFI) at 5,000 ft	FIT (SEFI) at 30,000 ft	FIT (SEFI) at 60,000 ft
AX1000	<0.082	<0.28	<12	<39
APA1000	<0.038	<0.13	<5.6	<18
XC2V3000	1,150	3,900	170,000	540,000
XC3S1000	320	1,100	47,000	150,000
EP1C20	460	1,600	67,000	220,000

Table 28. Overall cosmic-ray FIT at different altitudes

The altitude effect at 5,000 ft and 30,000 ft is evaluated using the formula provided in appendix E of JESD89 [2]:

$$\text{Neutron flux (n/cm}^2\text{/hour)} = 15E3 * e^{-(A/148)}$$

Where the altitude, a, in feet above sea level, is expressed as the areal density of the air column, A, in units of g/cm². The altitude, a, can be converted to the areal density, A using the following equation:

$$A = 1033 \times \exp[-.03813 \times (a/1000) - .00014 \times (a/1000)^2 + 6.4E\text{-}7 \times (a/1000)^3]$$

The altitude effect at 60,000 ft is evaluated using Figure 3 from reference [4].

7.3 Accuracy of results

The accuracy of the cross-section results is assessed in this section. The accuracy of the cross-section is the sum of the error count and fluence measurement accuracies.

7.3.1 Error count statistics

The error count is generally described by a Poisson distribution, cf appendix C.1 in [2]. If N errors occur, the mean error count is approximated by N. The standard deviation is given by √N.

The error count can be bounded using the upper and lower limits in Table 11, extracted from appendix C.2 of [2]. In using this table, the first column is the actual number of events observed in the experiment. The upper and lower limits define the 95% confidence interval for the true mean of the distribution. The upper and lower limits for any number of events can be calculated using the formulas given in appendix B.

The accuracy of the error count is defined in this report using 95% confidence intervals. The 95% confidence limits depend on the number of errors observed. The number of errors is detailed in appendix A for each chip and test condition.

The following table summarizes the 95% confidence intervals for each device. For example, the overall number of SEFI per chip and test condition is 15 for the XC2V3000. By using the formulas given in appendix B, we find that the lower and upper limits are 8.4 and 24.7 respectively. The limits in Table 29 are calculated as (Lower limit/Mean error count – 1)*100 = -44%, and (Upper limit/Mean error count – 1)*100 = +65%.

Device	Error type	Errors	Lower limit	Upper limit	Comment
AX1000	SEFI	0	n/a	n/a	No errors observed
APA1000	SEFI	0	n/a	n/a	No errors observed
XC2V3000	SEFI	15	-44%	65%	Errors per chip and test condition
		87	-20%	23%	Errors for all chips per test condition
		349	-10%	11%	Errors for all chips and test conditions
	SEU	144	-16%	18%	Errors per chip and test condition
		865	-7%	7%	Errors for all chips per test condition
XC3S1000	SEFI	17	-42%	60%	Errors per chip and test condition
		101	-19%	22%	Errors for all chips per test condition
		405	-10%	10%	Errors for all chips and test conditions
	SEU	81	-21%	24%	Errors per chip and test condition
		484	-9%	9%	Errors for all chips per test condition
EP1C20	SEFI	19	-40%	56%	Errors per chip and test condition
		113	-18%	20%	Errors for all chips per test condition
		453	-9%	10%	Errors for all chips and test conditions

Table 29. 95% confidence intervals for all devices

7.3.2 Fluence measurement accuracy

The accuracy of the fluence measurement is better than 5% for the LANSCE facility.

7.4 Detailed analysis

Detailed analysis of the results is presented hereafter. The following table summarizes the analyses presented for each device:

Analysis	AX1000	APA1000	XC2V3000	XC3S1000	EP1C20
Voltage influence on FIT			√	√	√
Analysis of critical vs non critical SEU			√	√	
Analysis of single event latchup	√	√	√	√	√
Bitmaps of errors			√	√	
Chip to chip variations			√	√	√
Special observations	√	√	√	√	√

Table 30. Detailed analysis for LANSCE tests

Many of the detailed analysis cannot be performed for the AX1000 and APA1000 because no errors were observed for these devices.

7.4.1 Voltage influence on FIT

The SEFI and SEU FIT dependence vs VDD is presented in this section. The FIT is plotted separately for each chip. The FIT average of all chips is also plotted, and the average FIT is used to fit an exponential curve.

7.4.1.1 XC2V3000

Figure 20 does not show a regular decrease of SEFI FIT at the higher VDD, as measured with 14 MeV neutrons. This is partially explained because of the statistical uncertainty of SEFI events, ±20% as shown in Table 29. Figure 21 shows a regular decrease of SEU FIT at the higher VDD, as expected.

The FIT dispersion between chips is consistent with the accuracy assessments given in section 7.3.

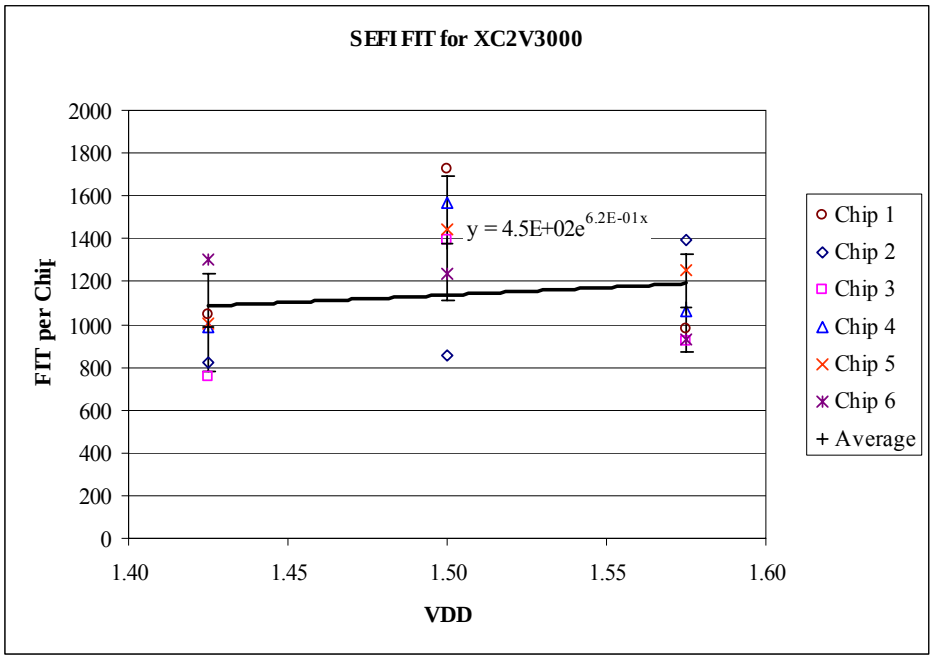


Figure 20. SEFI FIT of XC2V3000 vs VDD

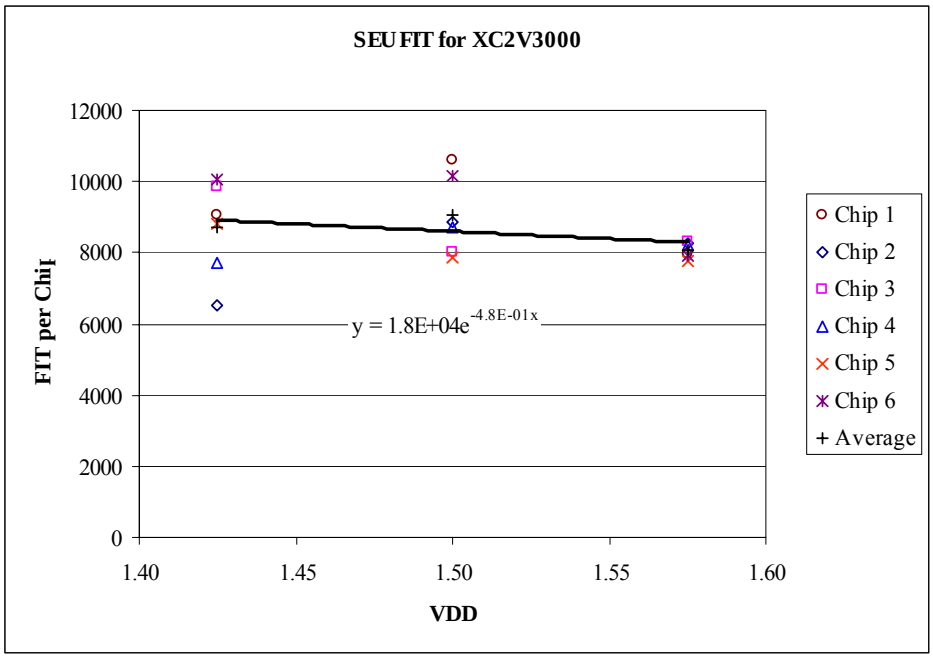


Figure 21. SEU FIT of XC2V3000 vs VDD

7.4.1.2 XC3S1000

Figure 22 does not show a regular decrease of SEFI FIT at the higher VDD, as expected. This is partially explained because of the statistical uncertainty of SEFI events, ±20% as shown in Table 29. Figure 23 shows a regular decrease of SEU FIT at the higher VDD, as expected.

The FIT dispersion between chips is consistent with the accuracy assessments given in section 7.3.

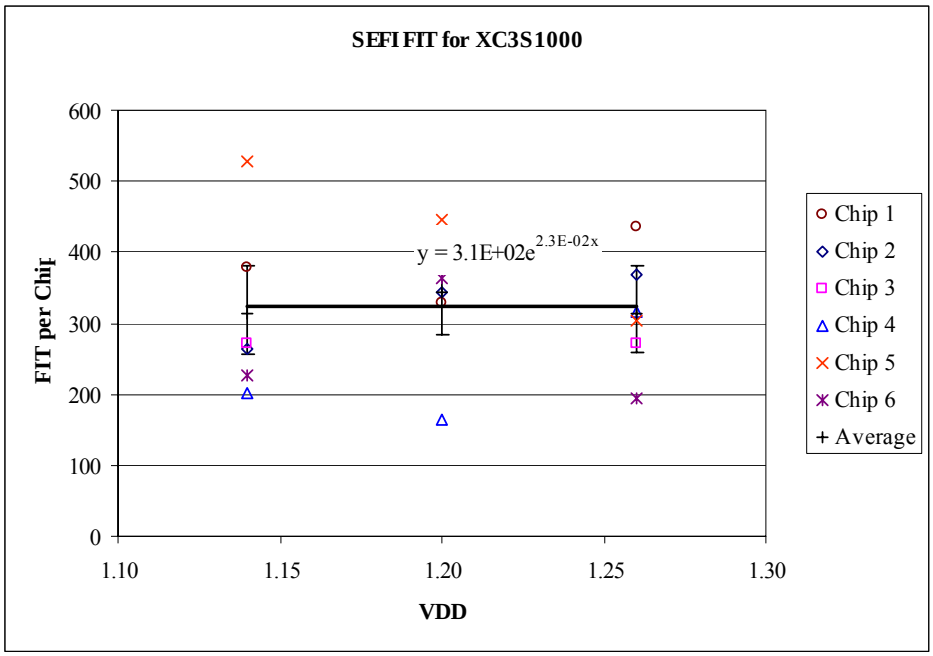


Figure 22. SEFI FIT of XC3S1000 vs VDD

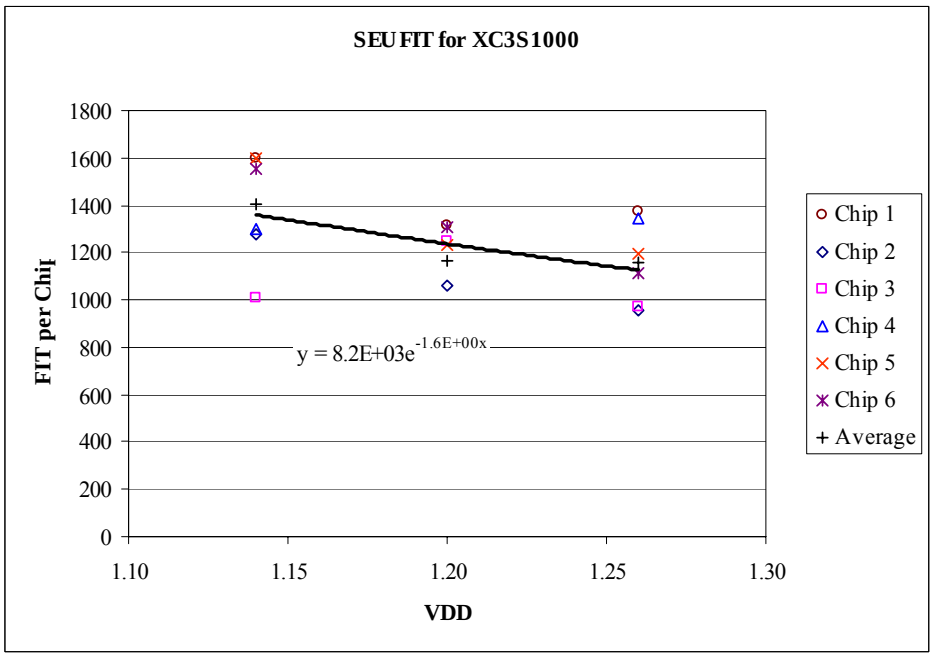


Figure 23. SEU FIT of XC3S1000 vs VDD

7.4.1.3 EP1C20

Figure 24 does not show a regular decrease of SEFI FIT at the higher VDD, as expected. This is partially explained because of the statistical uncertainty of SEFI events, ±20% as shown in Table 29.

The FIT dispersion between chips is consistent with the accuracy assessments given in section 7.3.

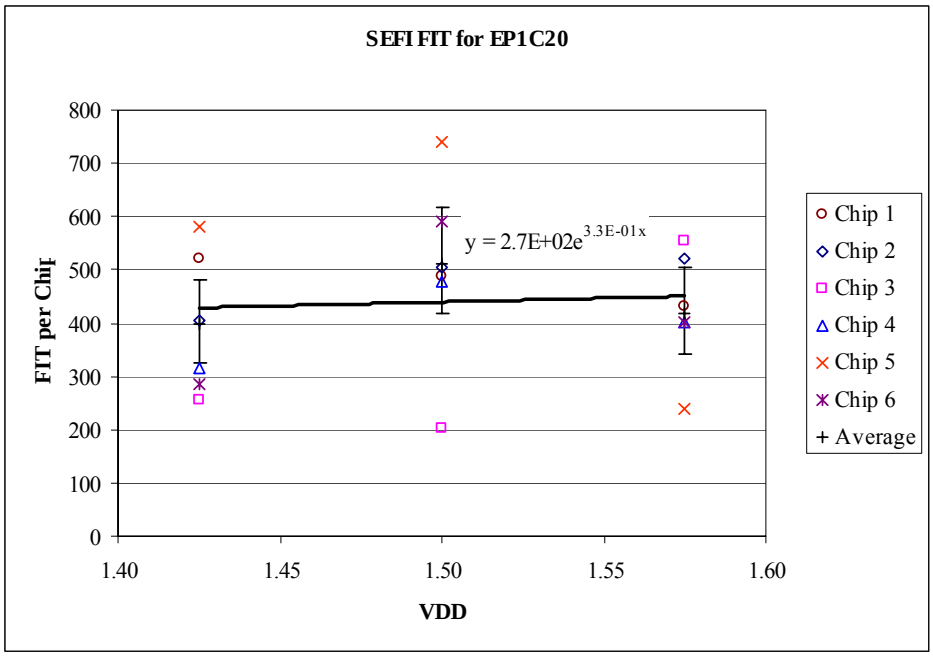


Figure 24. SEFI FIT of EP1C20 vs VDD

7.4.2 Analysis of critical vs non critical SEU

The test strategy enables to identify the critical and the non critical SEU in the configuration memory, that is, those SEU in the configuration memory that create an SEFI, and those that do not create an SEFI.

7.4.2.1 XC2V3000

Figure 25 presents the ratio SEFI / Total SEU for each chip and test condition. The overall ratio is 10% independent of the test condition.

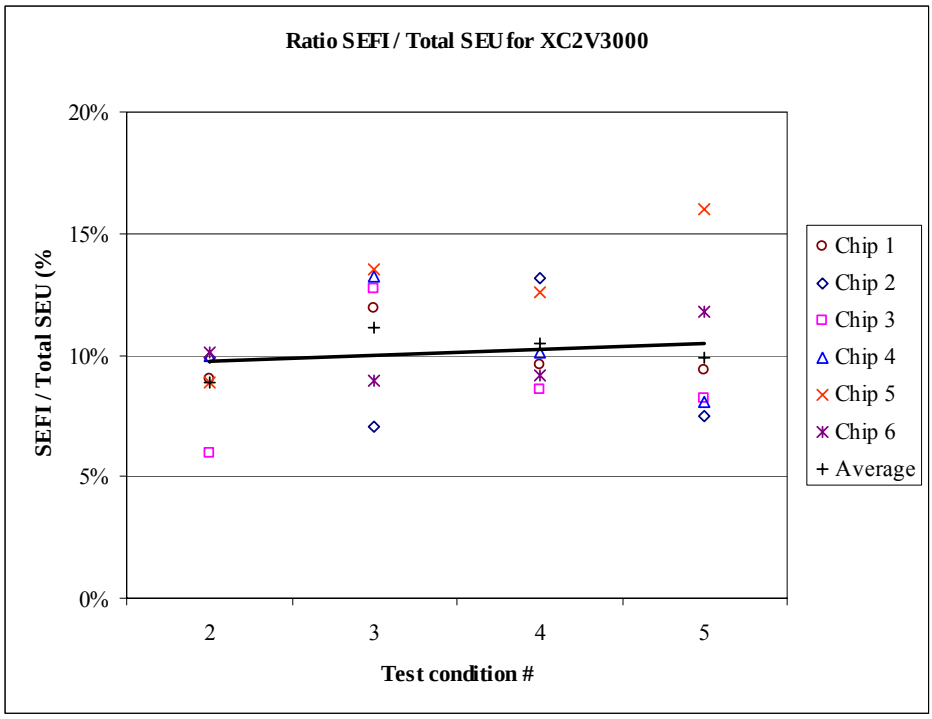


Figure 25. SEFI vs Total SEU XC2V3000

7.4.2.2 XC3S1000

Figure 26 presents the ratio SEFI / Total SEU for each chip and test condition. The overall ratio is 22% independent of the test condition.

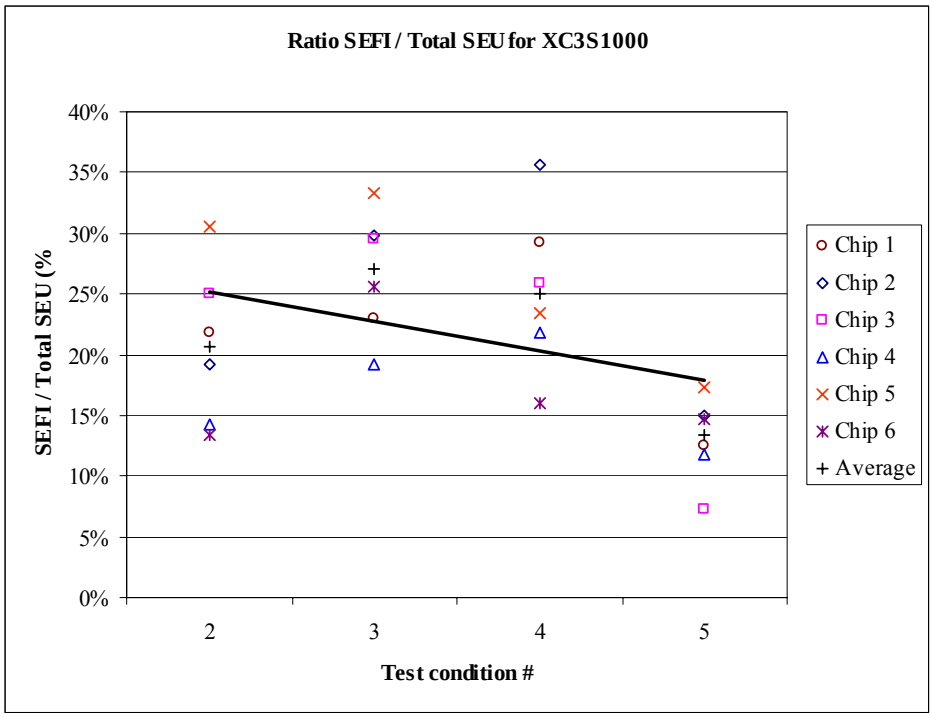


Figure 26. SEFI vs Total SEU XC3S1000

7.4.3 Analysis of single event latchup

Single event latchup (SEL) consists in the neutron induced activation of parasitic thyristor structures in the CMOS process. In case a process is sensitive to latchup, the latchup rate is higher at the higher voltage, temperature and particle energy.

Latchups result in increased current consumption, partial or total configuration memory wipe out, or complete loss of operation. Because the current is limited for protection, latchups lead to voltage shutdown to the DUT. The way the tester detects latchups is by monitoring the DUT supply voltages. In case a latchup is detected, the tester logs the event and switches the power off/on for recovering.

A particular case of latchup is the microlatchup. The microlatchup consists in the activation of a parasitic thyristor structure with weak on-resistance and a low increase of current consumption. In case of microlatchup, the voltage and current can find a stability point that cannot be detected by the tester. In this case, one or more chips are partially or totally wiped out, or experience complete loss of operation during the duration of a test condition.

No latchups were detected for any of the devices and conditions tested. In the following subsections, the voltage and current waveforms, acquired during the experiments, will be presented for each device and test condition. The sensitivity to microlatchup will be analyzed by inspection of the voltage and current waveforms and correlation with the observed number of errors in each chip.

7.4.3.1 AX1000

We observe regular voltage and current waveforms in Figure 27 and Figure 28. No errors were observed for any of the chips and conditions tested. Therefore, there is no indication of latchup.

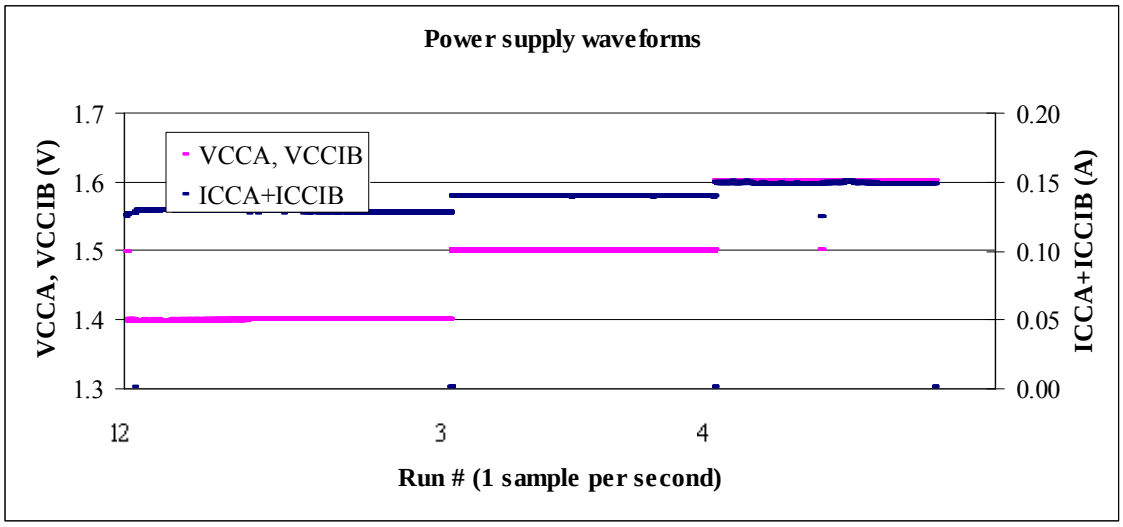


Figure 27. AX1000 VCCA and VCCIB waveforms

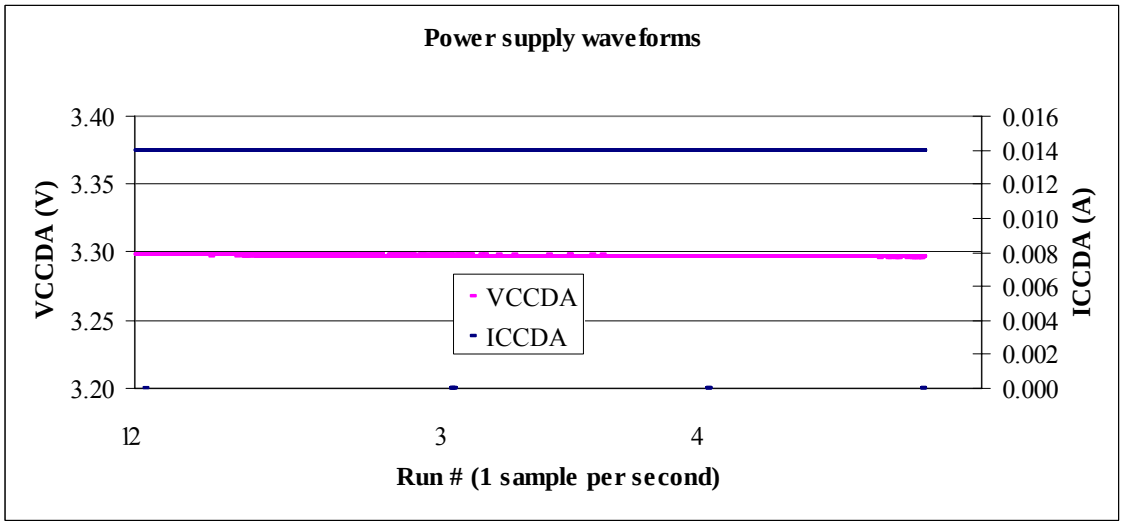


Figure 28. AX1000 VCCDA waveform

7.4.3.2 APA1000

We observe regular voltage and current waveforms in Figure 29 and Figure 30. No errors were observed for any of the chips and conditions tested. Therefore, there is no indication of latchup.

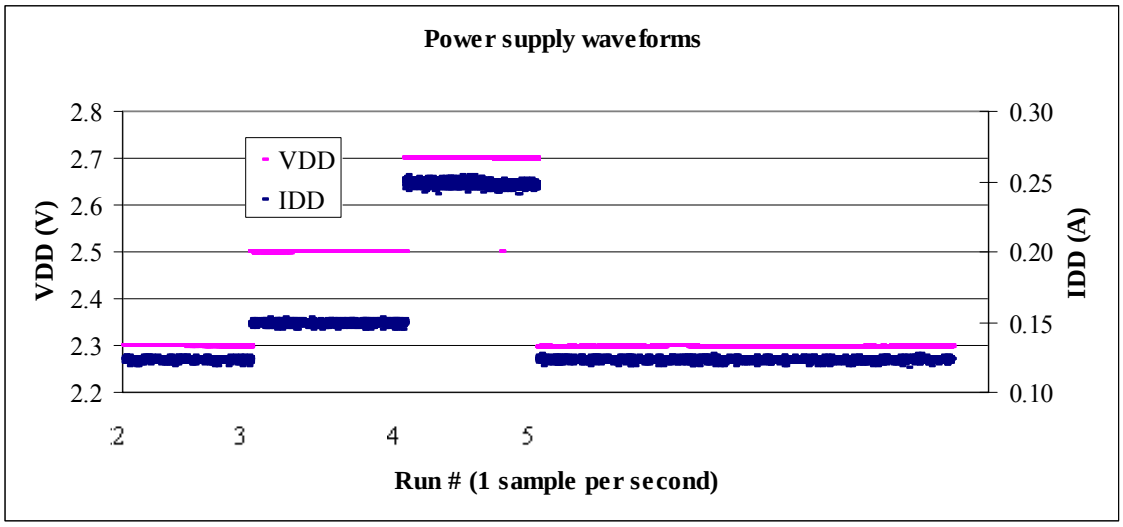


Figure 29. APA1000 VDD waveform

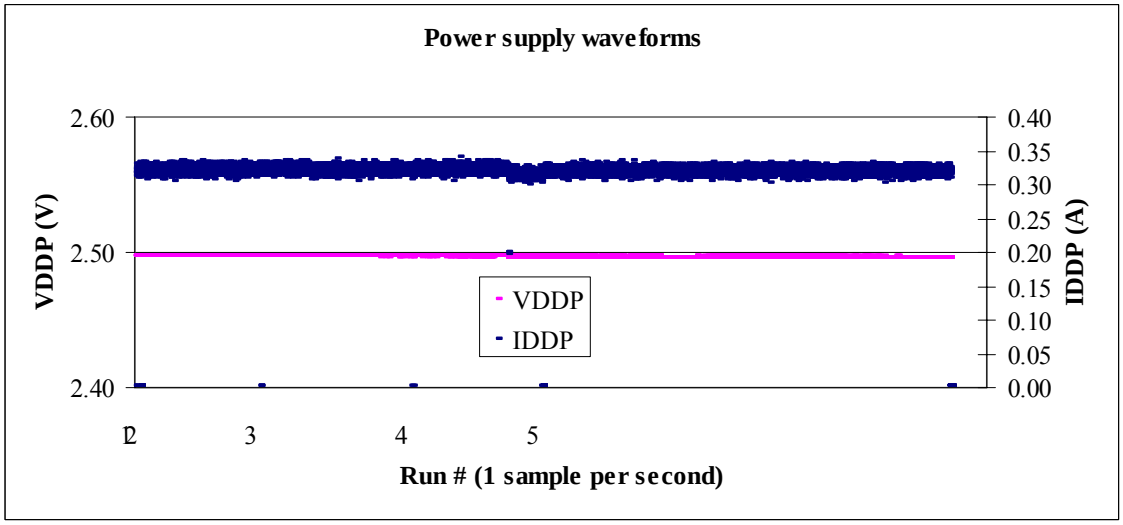


Figure 30. APA1000 VDDP waveform

7.4.3.3 XC2V3000

We observe regular voltage and current waveforms in Figure 31 and Figure 32. The number of errors, presented in the following table is regular across the six chips tested. Therefore, there is no indication of latchup.

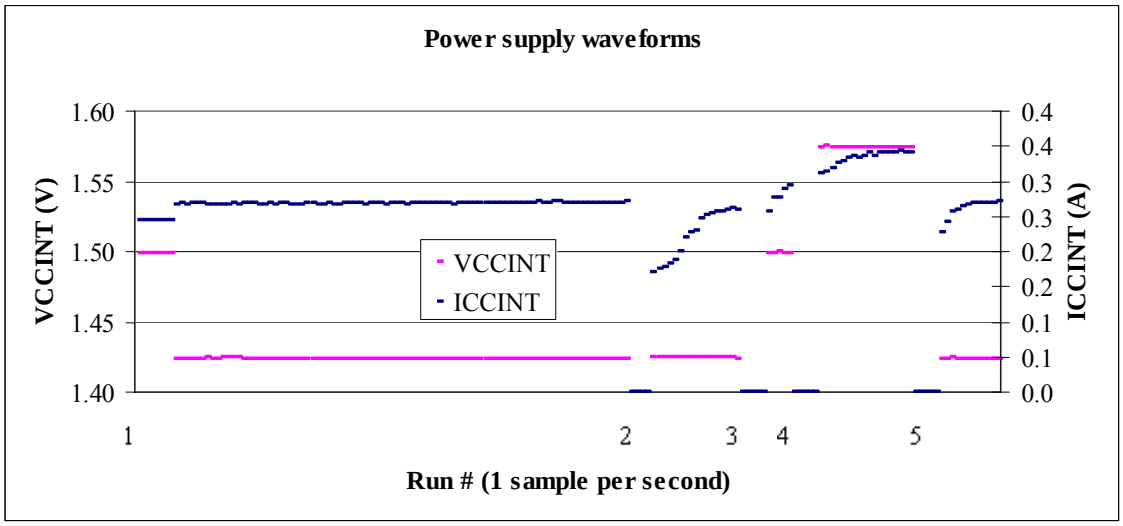


Figure 31. XC2V3000 VCCINT waveform

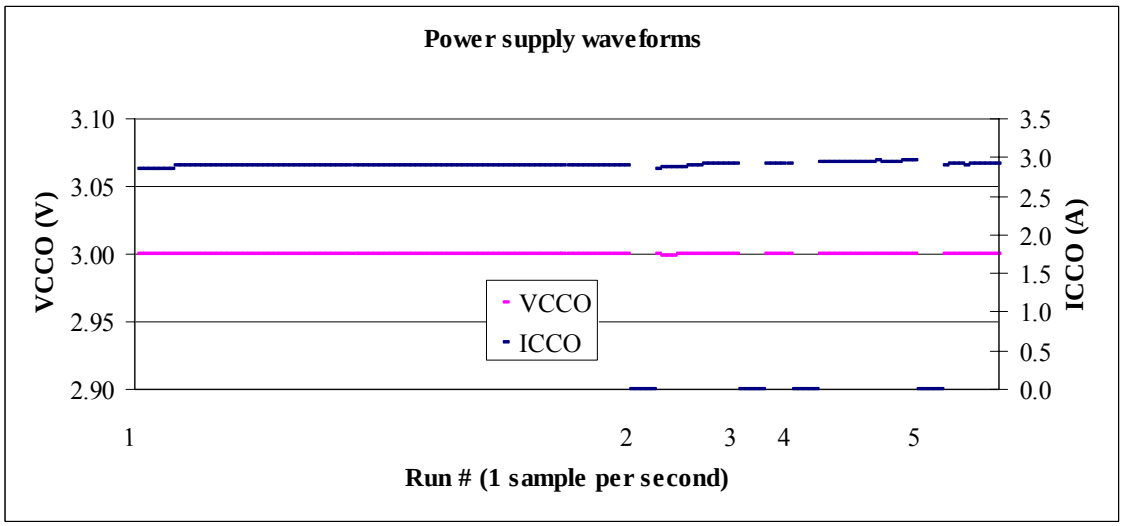


Figure 32. XC2V3000 VCCO waveform

Run #	Condition	Number of SEFI					
	VDD	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6
1	1.425	0	0	0	0	0	0
2	1.425	14	10	10	13	12	17
3	1.500	20	9	16	18	15	14
4	1.575	14	18	13	15	16	13
5	1.425	16	11	16	11	20	18

Table 31. XC2V3000 number of SEFI for each chip

Note: run #1 was a test run with the beam switched off, to test that the tester electronics was working correctly (cf section 6.3).

7.4.3.4 XC3S1000

The voltage and current waveforms could not be acquired during the experiments for the XC3S1000. The number of errors, presented in the following table is regular across the six chips tested. Therefore, there is no indication of latchup.

Run #	Condition	Number of SEFI					
	VDD	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6
1	1.14	0	0	0	0	0	0
2	1.14	21	14	13	10	29	13
3	1.20	20	20	21	9	27	23
4	1.26	26	21	14	17	18	12
5	1.14	13	15	6	11	18	14

Table 32. XC3S1000 number of SEFI for each chip

Note: run #1 was a test run with the beam switched off, to test that the tester electronics was working correctly (cf section 6.3).

7.4.3.5 EP1C20

The voltage and current waveforms could not be acquired during the experiments for the EP1C20. The number of errors, presented in the following table is regular across the six chips tested. Therefore, there is no indication of latchup.

Run #	Condition	Number of SEFI					
	VDD	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6
1	1.425	0	0	0	0	0	0
2	1.425	24	17	10	14	28	14
3	1.500	17	16	6	16	27	22
4	1.575	19	21	21	17	11	19
5	1.425	29	11	21	28	23	22

Table 33. EP1C20 number of SEFI for each chip

Note: run #1 was a test run with the beam switched off, to test that the tester electronics was working correctly (cf section 6.3).

7.4.4 Bitmaps of errors

Bitmaps allow to check the expected random distribution of errors in the configuration memory arrays.

Each point in the bitmap represents a failing address. The bitmaps are logical bitmaps, not physical bitmaps, because the layout of the configuration memory is not available. In the logical bitmaps, the address LSB are mapped in the x-axis and the address MSB are mapped in the y-axis.

7.4.4.1 XC2V3000

The address refers to the location where the verification bitstream is stored in the tester memory. Valid addresses for the XC2V3000 are in the range 0x400069 to 0x5D4329. Each address holds 5 bits. Therefore, the verification bitstream length is 9,588,165 bits.

The bitmaps show the expected random distribution of errors.

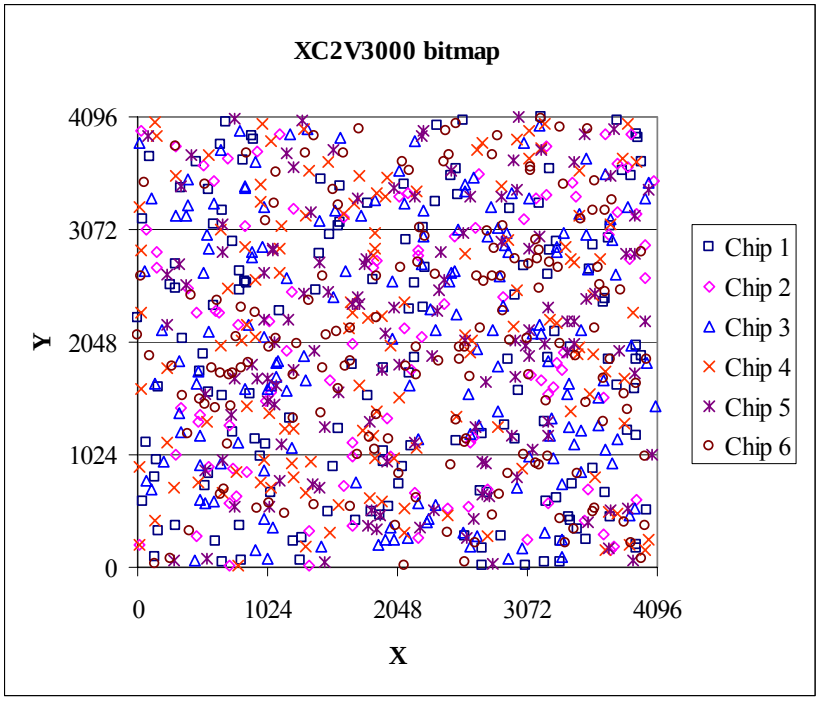


Figure 33. Bitmap for run#2 of XC2V3000

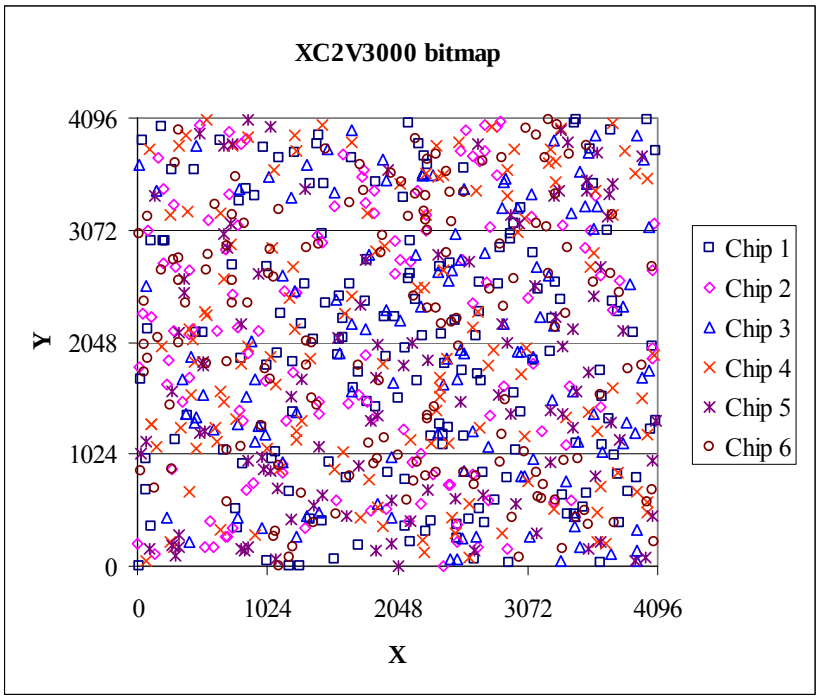


Figure 34. Bitmap for run#3 of XC2V3000

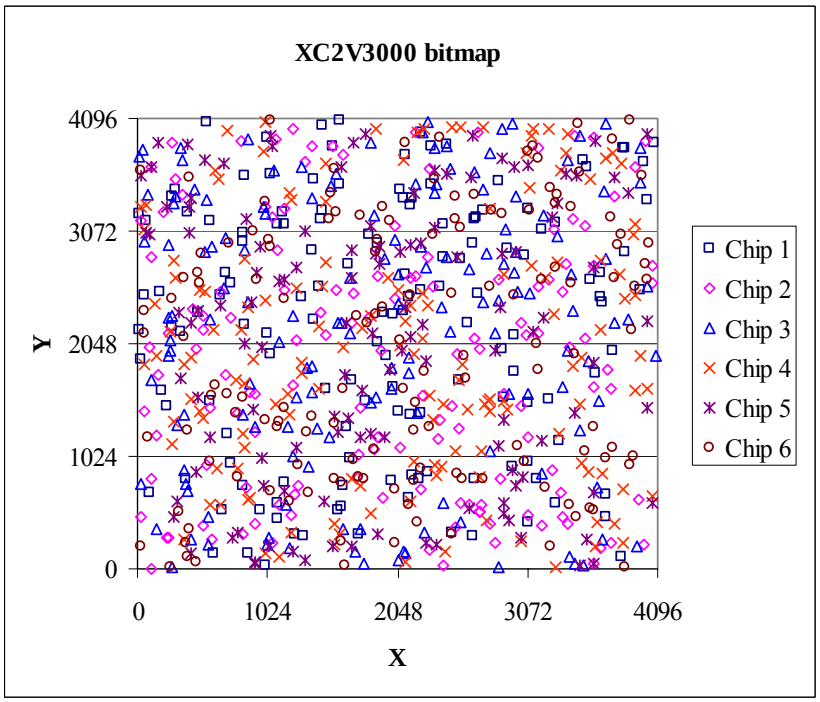


Figure 35. Bitmap for run#4 of XC2V3000

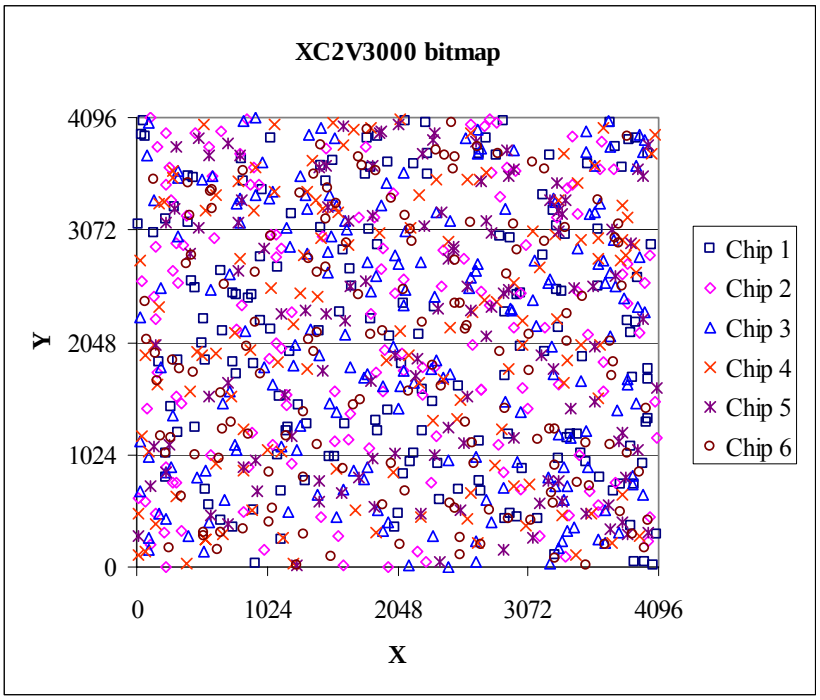


Figure 36. Bitmap for run#5 of XC2V3000

7.4.4.2 XC3S1000

The address refers to the location where the verification bitstream is stored in the tester memory. Valid addresses for the XC3S1000 are in the range 0x400068 to 0x49D349. Each address holds 5 bits. Therefore, the verification bitstream length is 3,219,050 bits.

The bitmaps show the expected random distribution of errors.

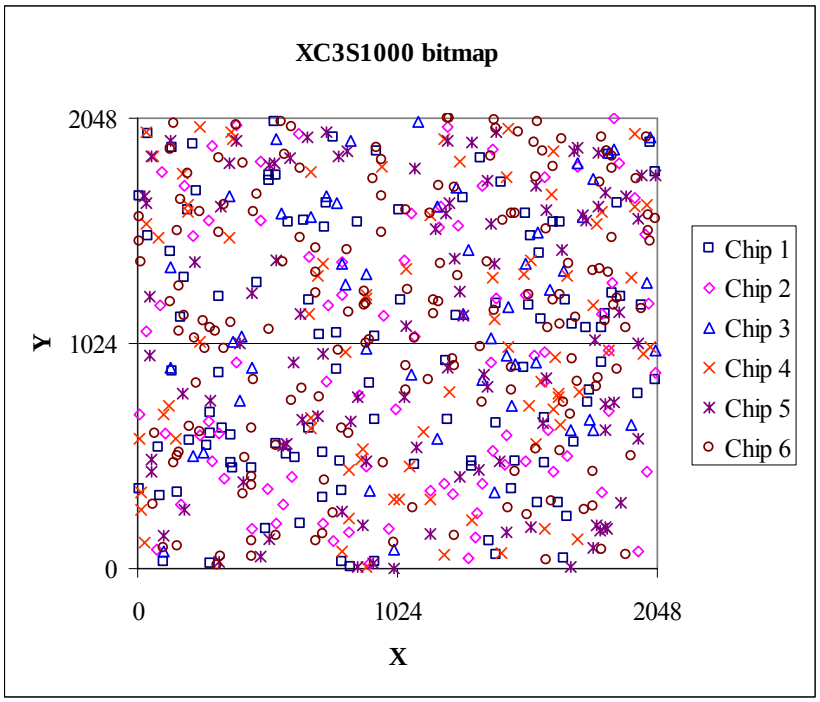


Figure 37. Bitmap for run#2 of XC3S1000

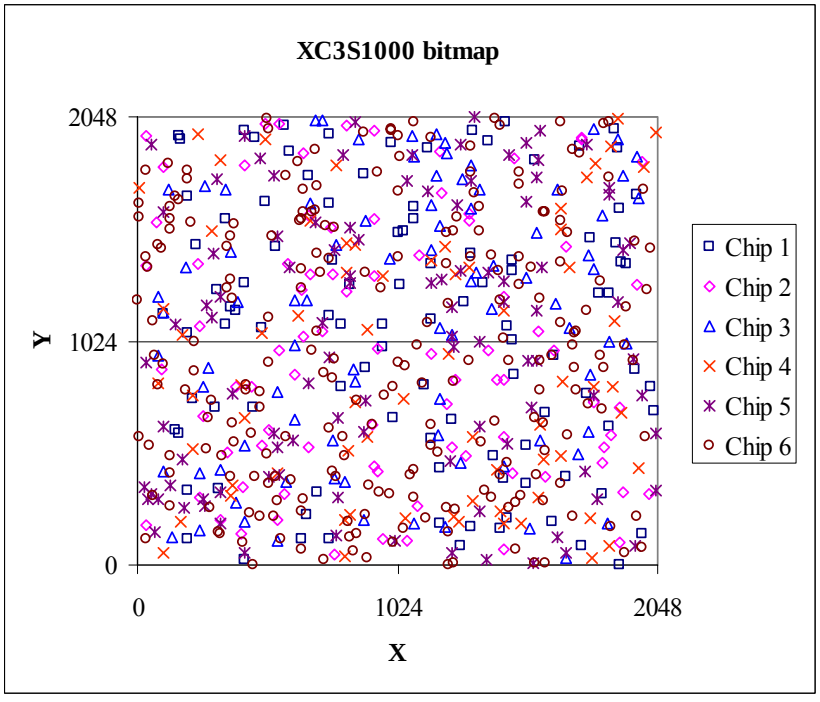


Figure 38. Bitmap for run#3 of XC3S1000

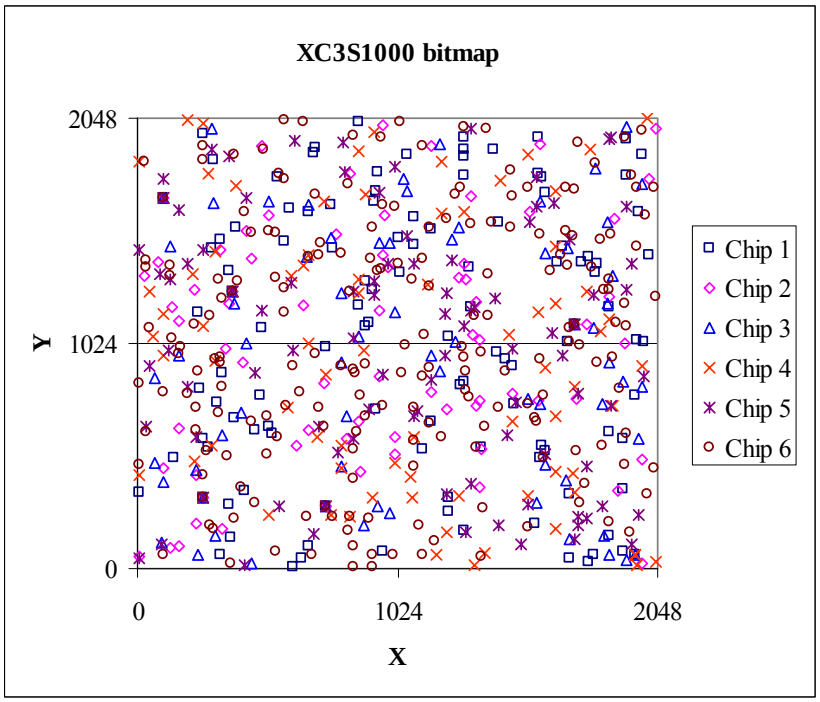


Figure 39. Bitmap for run#4 of XC3S1000

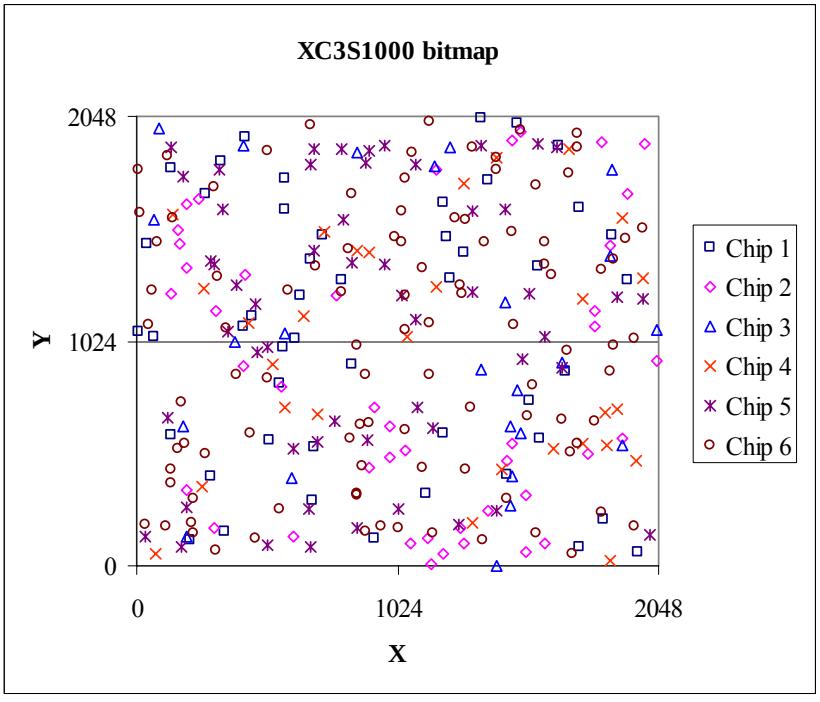


Figure 40. Bitmap for run#5 of XC3S1000

7.4.5 Chip to chip variation

This section presents the chip to chip FIT variations observed. The objective of this section is to check the neutron flux uniformity.

The FIT variations are defined as the variation relative to the average of the 6 chips tested.

$$\text{FIT variation for chip(i)}\,(\%) = \left(\frac{\text{FIT Chip(i)}}{\text{Average FIT Chips(1 to 6)}} - 1 \right) \times 100$$

7.4.5.1 XC2V3000

The FIT variations observed are within the expected statistical uncertainty: –16% to +18%, see Table 29. Therefore, we verify that the neutron flux is uniform.

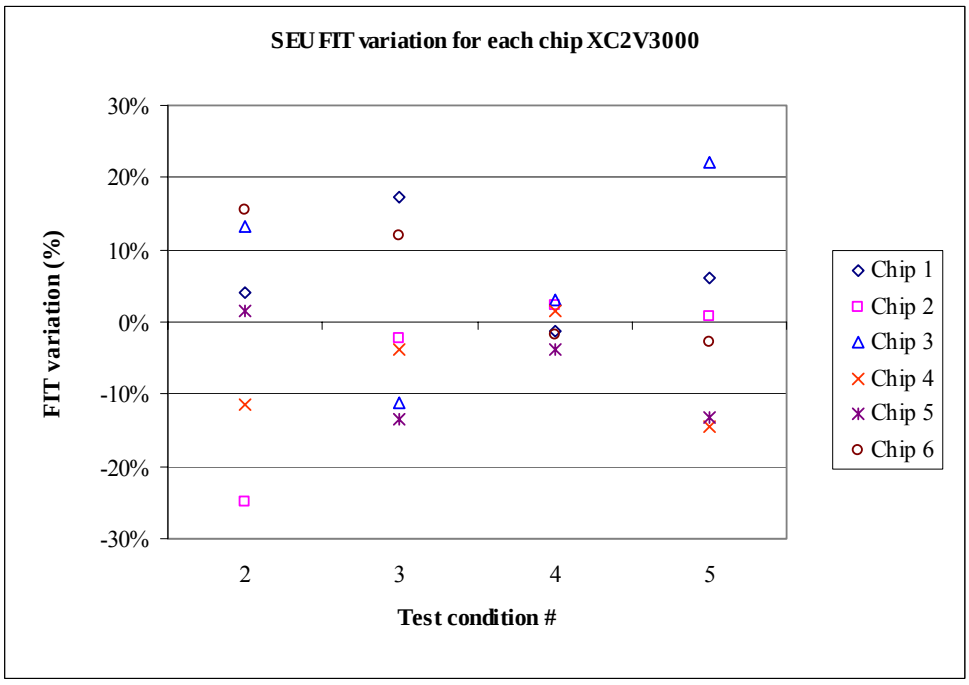


Figure 41. Chip to chip FIT variation for XC2V3000

7.4.5.2 XC3S1000

The FIT variations observed are within the expected statistical uncertainty: –21% to +24%, see Table 29. Therefore, we verify that the neutron flux is uniform.

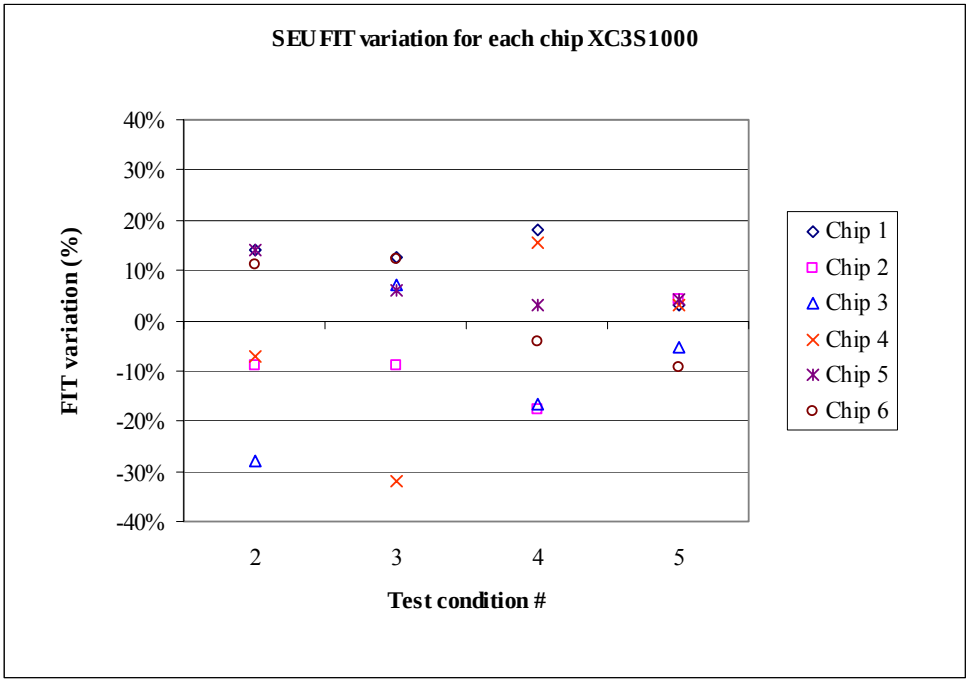


Figure 42. Chip to chip FIT variation for XC3S1000

7.4.5.3 EP1C20

The FIT variations observed are within the expected statistical uncertainty: –40% to +56%, see Table 29. Therefore, we verify that the neutron flux is uniform.

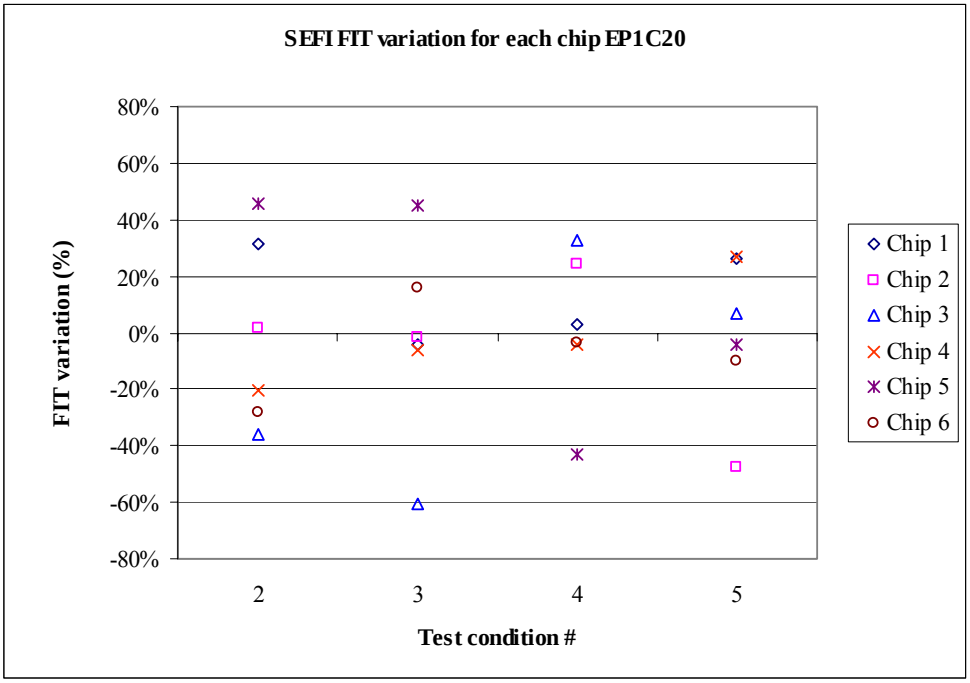


Figure 43. Chip to chip FIT variation for EP1C20

7.4.6 Consistency check

A consistency test (repetition of the first condition) has been carried out at the end of the test sequence. The consistency test verifies the stability of the beam, DUT and tester.

7.4.6.1 XC2V3000

Figure 44 verifies that the results of runs #2 and #5 are consistent, taking into account the statistical uncertainty shown by the error bars.

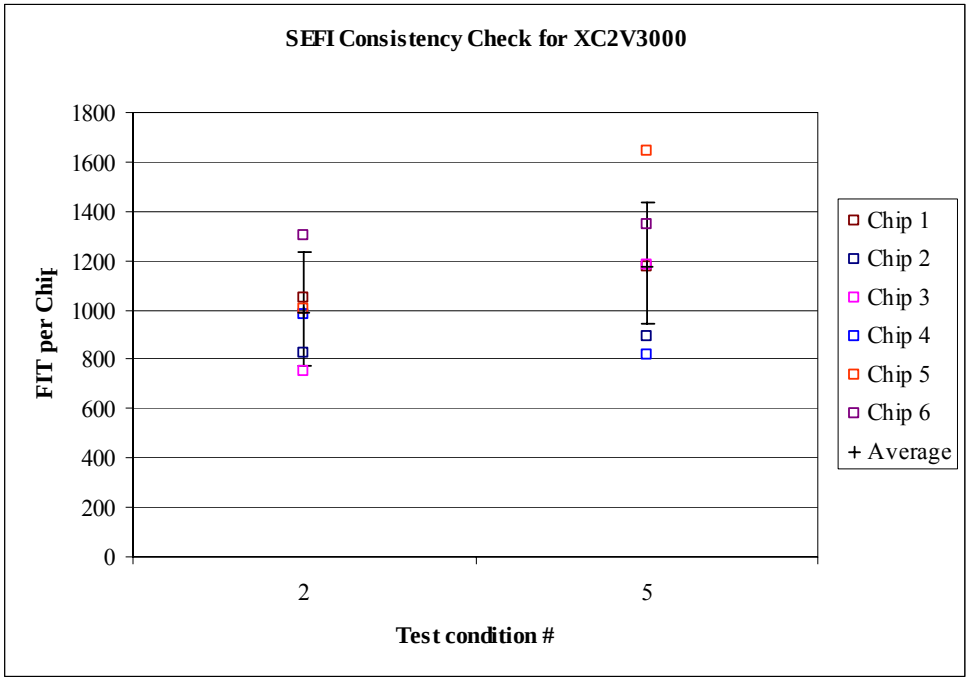


Figure 44. SEFI consistency check for XC2V3000

7.4.6.2 XC3S1000

Figure 45 verifies that the results of runs #2 and #5 are consistent, taking into account the statistical uncertainty shown by the error bars.

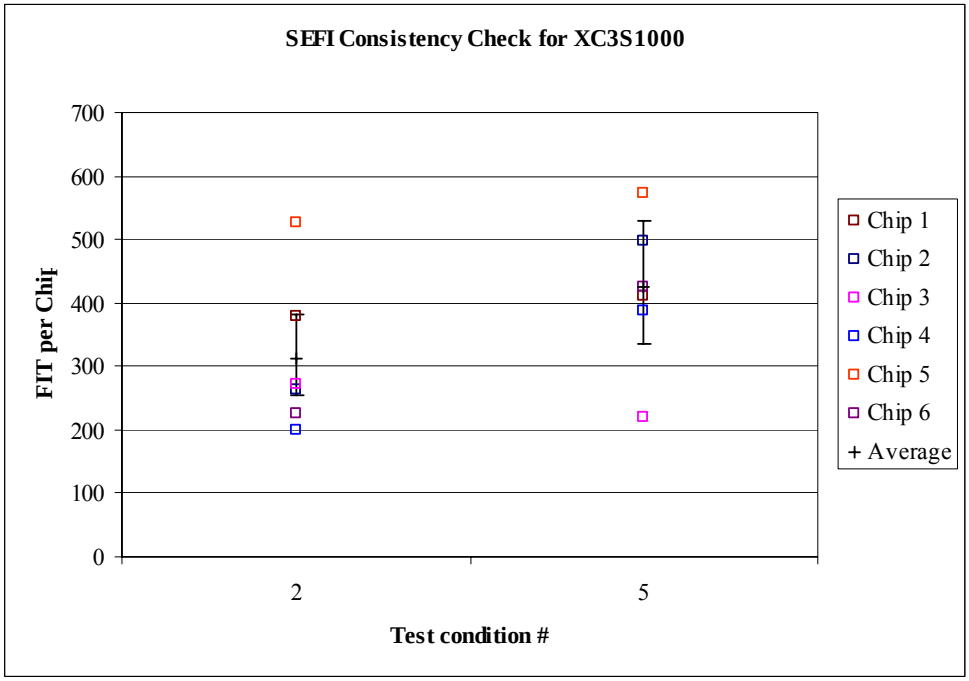


Figure 45. SEFI consistency check for XC3S1000

7.4.6.3 EP1C20

Figure 46 verifies that the results of runs #2 and #5 are consistent, taking into account the statistical uncertainty shown by the error bars.

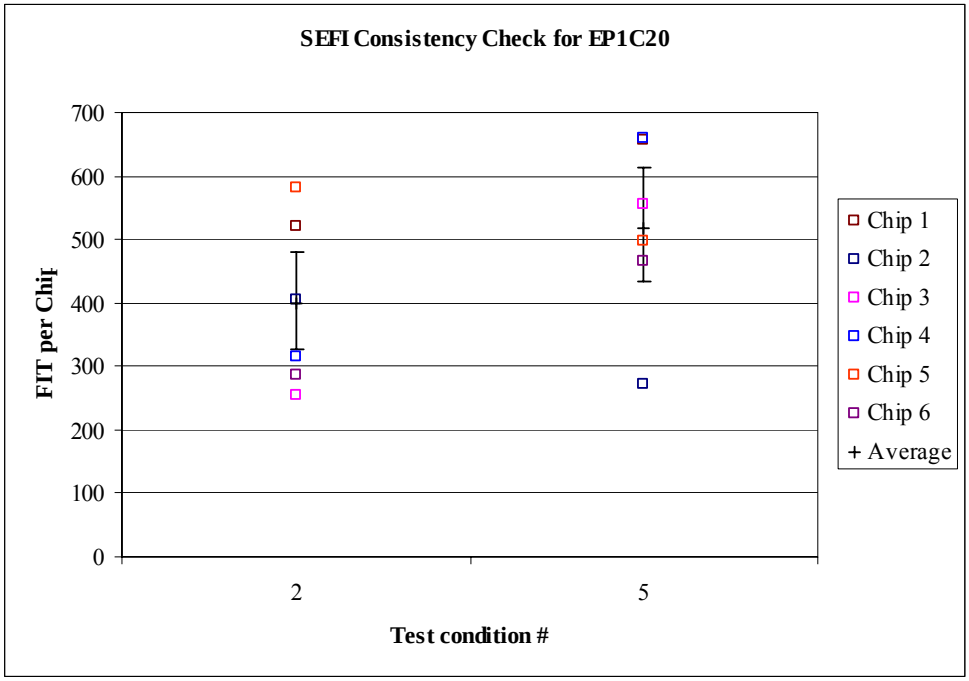


Figure 46. SEFI consistency check for EP1C20

7.4.7 Special observations

iRoC has measured the flux uniformity at LANSCE using a specific test board. The test board consists in a linear array of 18 SRAM chips evenly spaced by 7.7 mm, as shown in Figure 49. The SRAM chips have the same part number and datecode. Since the chips are assumed identical, the error count variations determine the flux uniformity. An error count of 500 errors per chip, for the chips in the center of the board, was targeted in order to have a good statistical accuracy. The measured flux uniformity is shown in Figure 47 and Figure 48 for the x-axis and y-axis respectively. With relation to Figure 49, the positive x-axis is on the left, the positive y-axis is on the top.

The factors in Figure 47 and Figure 48 have been used to correct the fluence for each chip, according to its position on the test board, for the AX1000, APA1000, XC2V3000, XC3S1000 and EP1C20.

A verify operation using the Flash Pro programmer was performed for the APA1000 chips, at the end of the radiation tests performed. The verify operation was successful for all the APA1000 chips.

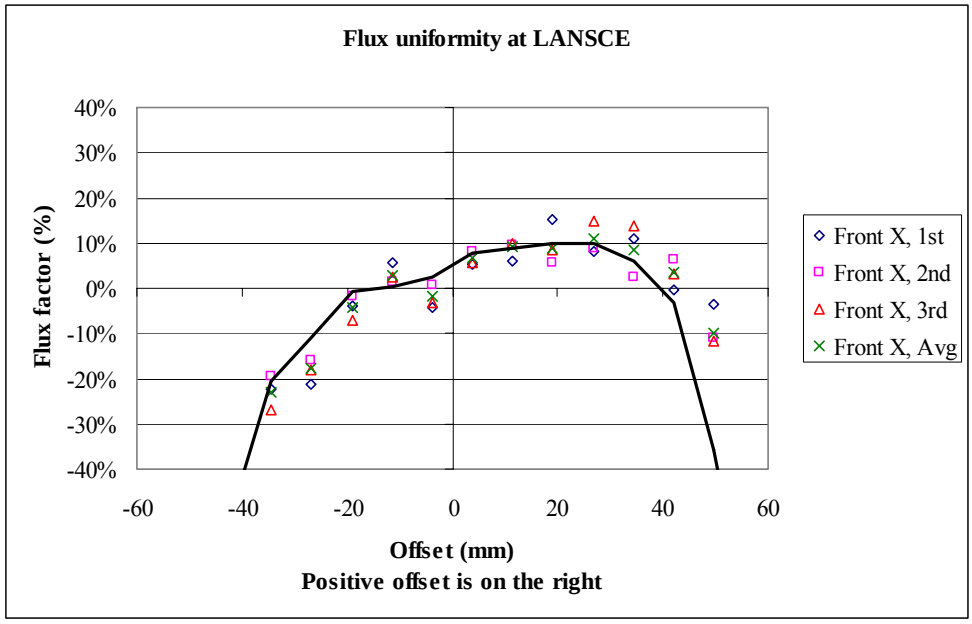


Figure 47. Flux uniformity at LANSCE (x-axis)

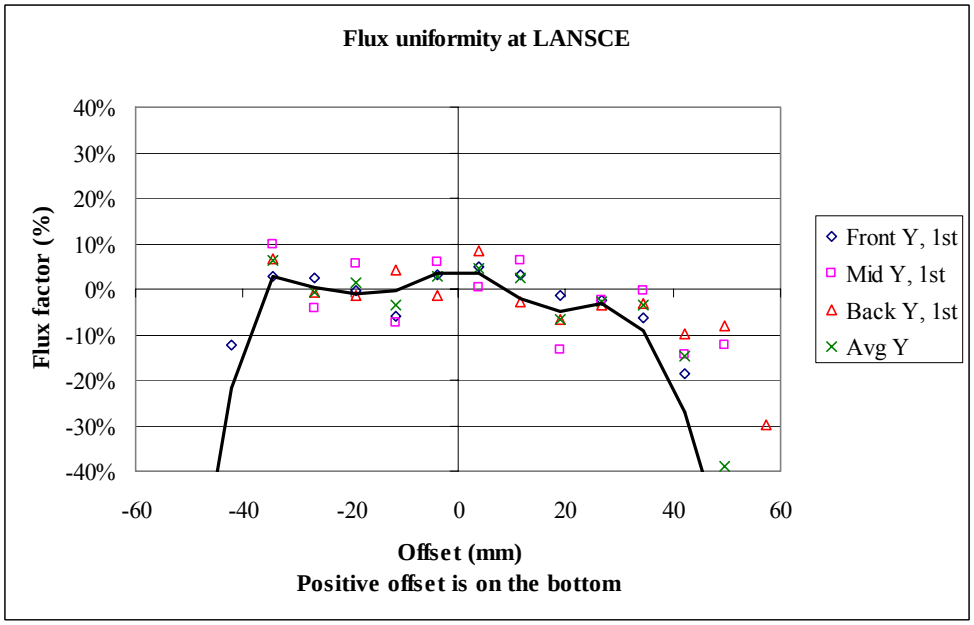


Figure 48. Flux uniformity at LANSCE (y-axis)

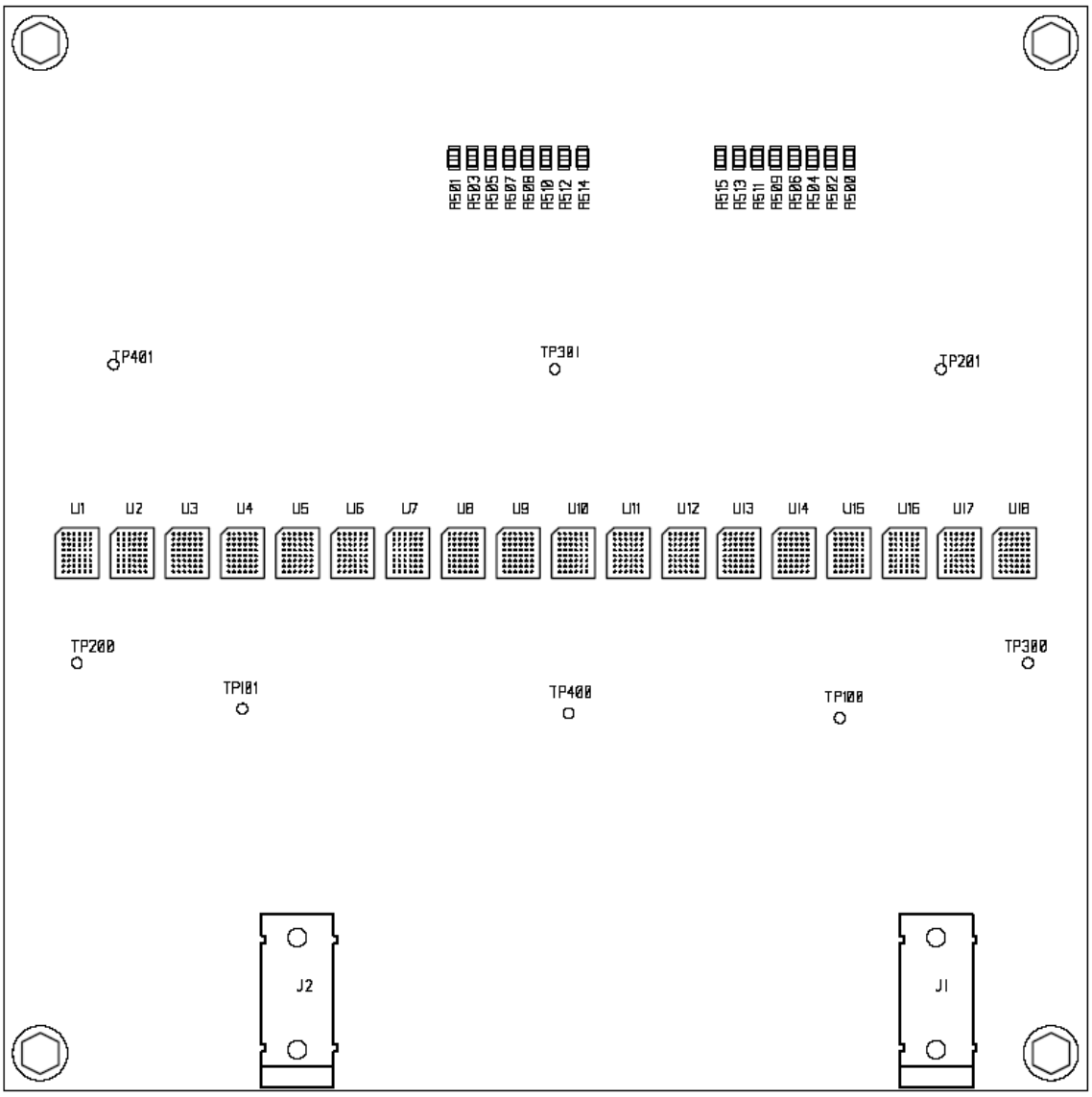


Figure 49. Flux uniformity measurement at LANSCE

8 LANSCE conclusions

This test report provides the cosmic-ray SER of AX1000, APA1000, XC2V3000, XC3S1000 and EP1C20 devices. The cosmic-ray SER was measured at the LANSCE WNR facility at Los Alamos in February 2004.

Table 34 presents the overall cosmic-ray FIT for each device at sea level in NYC. The overall FIT is calculated as the average of all chips and test conditions for the XC2V3000, XC3S1000 and EP1C20 devices. Appendix A details the cross-section and FIT for each chip and test condition.

Device	Overall FIT (SEFI) per Device	Overall FIT (SEU) per Device
AX1000	<0.082	<0.082
APA1000	<0.038	<0.038
XC2V3000	1,150	8,680
XC3S1000	320	1,240
EP1C20	460	n/a

Table 34. Overall cosmic-ray FIT at sea level in NYC

In Table 34, it is important to understand that no errors were observed for the AX1000 and APA1000, for any of the test conditions. The given figure of FIT is an upper bound calculated considering one error for all chips and test conditions. The AX1000 and APA1000, based in Antifuse and Flash processes respectively, are considered insensitive to terrestrial spectrum of neutrons, therefore extending the test for longer periods would still produce no errors, and result in lower bounds of FIT.

The readback of the configuration memory is not available for the EP1C20. Therefore, the SEU FIT could not be measured for the EP1C20.

The neutron flux increases with altitude, and has a maximum at approximately 60,000 ft. The FIT at sea level, 5,000 ft, 30,000 ft and 60,000 ft is provided in Table 35.

Device	FIT (SEFI) at sea level	FIT (SEFI) at 5,000 ft	FIT (SEFI) at 30,000 ft	FIT (SEFI) at 60,000 ft
AX1000	<0.082	<0.28	<12	<39
APA1000	<0.038	<0.13	<5.6	<18
XC2V3000	1,150	3,900	170,000	540,000
XC3S1000	320	1,100	47,000	150,000
EP1C20	460	1,600	67,000	220,000

Table 35. Overall cosmic-ray FIT at different altitudes

No occurrences of latchup have been observed for any of the devices. No errors in the configuration circuitry of the XC2V3000, XC3S1000 or EP1C20 were observed. No hard errors were observed for any of the devices.

9 Alpha tests

9.1 Characteristics of the alpha sources

Alpha tests were conducted at iRoC premises using calibrated sources with the following characteristics:

Source No.	1	2
Isotope	Am241	Am241
Active area diameter	20 mm	44 mm
Flux at the surface	2760 α/cm²/s	21.3 α/cm²/s
Uncertainty	10%	6%

Table 36. Characteristics of the alpha sources

The radioactive sources were directly placed at the package surface, which is at 1 mm or less from the die surface. In addition, the active area is much larger than the die area to ensure that nearly all angles of incidence are enabled.

A geometry factor has been calculated that takes into account the flux reduction resulting from the distance of the source to the die. The calculation of the geometry factor is explained in Appendix C.

For a disk shaped source, the formula is:

$$G_{disk}=1-\frac{h}{\sqrt{h^2+\rho^2}}$$

Where h is the distance from the source to the die, and ρ is the radius of the source.

Device	Source No.	Radius ρ (mm)	Distance h (mm)	G_{disk}
AX1000	1	10	1	0.90
APA1000	1	10	1	0.90
XC2V3000	2	22	0.5	0.98
XC3S1000	2	22	0.5	0.98
EP1C20	2	22	0.5	0.98

Table 37. Alpha source utilization and geometry factors for each device

9.2 Tested conditions and schedule

The following tables provide the sequence of conditions that were tested. Additionally to the test conditions, stability and consistency checks have been performed at the beginning and the end of each test sequence. A stability test (beam off) has been carried out before irradiation (cf. section 9.4). A consistency test (repetition of the first condition) has been carried out at the end of the test sequence The order of the test conditions follows the Test Plan [3].

The tables are extracted from the campaign logbook files in appendix A.3.

Note that chips were irradiated one at a time during alpha tests. Run 21 stands for run 2 and chip 1, run 22 stands for run 2 and chip 2, etc.

Run #	Device	Particle	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	AX1000	α–Am241	9-Apr	10:22:02	9-Apr	10:34:02	200ns	1.4	25°C
21	AX1000	α–Am241	9-Apr	10:50:02	10-Apr	2:50:01	200ns	1.4	25°C
22	AX1000	α–Am241	12-Apr	19:45:04	13-Apr	11:45:03	200ns	1.4	25°C
31	AX1000	α–Am241	10-Apr	2:53:03	10-Apr	18:53:02	200ns	1.5	25°C
32	AX1000	α–Am241	13-Apr	11:48:04	14-Apr	3:48:03	200ns	1.5	25°C
41	AX1000	α–Am241	10-Apr	18:56:03	11-Apr	10:56:02	200ns	1.6	25°C
42	AX1000	α–Am241	14-Apr	3:51:04	14-Apr	19:51:03	200ns	1.6	25°C
51	AX1000	α–Am241	11-Apr	10:59:03	12-Apr	2:59:03	200ns	1.4	25°C
52	AX1000	α–Am241	14-Apr	19:54:05	15-Apr	11:54:04	200ns	1.4	25°C

Table 38. Conditions tested for AX1000

Run #	Device	Particle	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
21	APA1000	α–Am241	27-Apr	17:00:00	30-Apr	9:00:00	200ns	2.3	25°C
22	APA1000	α–Am241	30-Apr	17:00:00	3-May	9:00:00	200ns	2.3	25°C

Table 39. Conditions tested for APA1000

Run #	Device	Particle	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	XC2V3000	α–Am241	8-Oct	12:02:15	8-Oct	14:31:15	200ns	1.43	25°C
21	XC2V3000	α–Am241	8-Oct	19:16:10	8-Oct	22:17:06	200ns	1.43	25°C
22	XC2V3000	α–Am241	9-Oct	11:46:14	9-Oct	14:47:10	200ns	1.43	25°C
31	XC2V3000	α–Am241	8-Oct	22:19:11	9-Oct	1:20:07	200ns	1.50	25°C
32	XC2V3000	α–Am241	10-Oct	12:11:21	10-Oct	15:12:17	200ns	1.50	25°C
41	XC2V3000	α–Am241	9-Oct	1:22:11	9-Oct	4:23:07	200ns	1.58	25°C
42	XC2V3000	α–Am241	10-Oct	15:14:22	10-Oct	18:15:18	200ns	1.58	25°C
51	XC2V3000	α–Am241	9-Oct	4:25:12	9-Oct	7:26:08	200ns	1.43	25°C
52	XC2V3000	α–Am241	10-Oct	18:17:23	10-Oct	21:18:20	200ns	1.43	25°C

Table 40. Conditions tested for XC2V3000

Run #	Device	Particle	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	XC3S1000	α–Am241	9-Apr	11:28:01	9-Apr	11:38:02	200ns	1.14	25°C
24	XC3S1000	α–Am241	9-Apr	12:13:02	9-Apr	18:13:01	200ns	1.14	25°C
25	XC3S1000	α–Am241	10-Apr	12:30:02	10-Apr	18:30:02	200ns	1.14	25°C
26	XC3S1000	α–Am241	11-Apr	12:55:03	11-Apr	18:55:03	200ns	1.14	25°C
34	XC3S1000	α–Am241	9-Apr	18:16:02	10-Apr	0:16:02	200ns	1.20	25°C
35	XC3S1000	α–Am241	10-Apr	18:33:02	11-Apr	0:33:02	200ns	1.20	25°C
36	XC3S1000	α–Am241	11-Apr	18:58:02	12-Apr	0:58:02	200ns	1.20	25°C
44	XC3S1000	α–Am241	10-Apr	0:19:02	10-Apr	6:19:01	200ns	1.26	25°C
45	XC3S1000	α–Am241	11-Apr	0:36:03	11-Apr	6:36:02	200ns	1.26	25°C
46	XC3S1000	α–Am241	12-Apr	1:01:03	12-Apr	7:01:02	200ns	1.26	25°C
54	XC3S1000	α–Am241	10-Apr	6:22:02	10-Apr	12:22:02	200ns	1.14	25°C
55	XC3S1000	α–Am241	11-Apr	6:39:02	11-Apr	12:39:02	200ns	1.14	25°C
56	XC3S1000	α–Am241	12-Apr	7:04:03	12-Apr	13:04:02	200ns	1.14	25°C

Table 41. Conditions tested for XC3S1000

Run #	Device	Particle	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	EP1C20	α–Am241	13-Oct	14:53:38	13-Oct	15:04:27	200ns	1.425	25°C
21	EP1C20	α–Am241	13-Oct	16:11:06	13-Oct	22:01:04	200ns	1.425	25°C
22	EP1C20	α–Am241	14-Oct	17:01:12	14-Oct	23:01:10	200ns	1.425	25°C
31	EP1C20	α–Am241	13-Oct	22:04:07	14-Oct	4:04:06	200ns	1.500	25°C
32	EP1C20	α–Am241	14-Oct	23:04:14	15-Oct	5:04:12	200ns	1.500	25°C
41	EP1C20	α–Am241	14-Oct	4:07:08	14-Oct	10:07:07	200ns	1.575	25°C
42	EP1C20	α–Am241	15-Oct	5:07:16	15-Oct	11:07:14	200ns	1.575	25°C
51	EP1C20	α–Am241	14-Oct	10:10:11	14-Oct	16:10:09	200ns	1.425	25°C
52	EP1C20	α–Am241	15-Oct	11:10:18	15-Oct	17:10:15	200ns	1.425	25°C

Table 42. Conditions tested for EP1C20

9.3 Devices tested

The following tables show the lot codes of the chips that were actually tested:

Chip 1	Chip 2
DOAAJ1 0320	DOJC21 0345

Table 43. Lot codes of the AX1000 chips tested

Chip 1	Chip 2
MF7G7 0247	MF7G7 0247

Table 44. Lot codes of the APA1000 chips tested

Chip 1	Chip 2
AGT0413 A2164275A	AGT0413 A2164275A

Table 45. Lot codes of the XC2V3000 chips tested

Chip 1	Chip 2	Chip 3
FT256AFQ0341 D13989A	FT256AFQ0341 D13989A	FT256AFQ0341 D13990A

Table 46. Lot codes of the XC3S1000 chips tested

Chip 1	Chip 2
AAD9G0413A	AAD9G0413A

Table 47. Lot codes of the EP1C20 chips tested

9.4 Stability without alpha source

An error rate measurement is performed without the alpha source and with the components placed in the target. The die were covered to avoid ambient light. This aims at verifying the robustness of both the tester and the DUT board in the test environment.

This experiment was done during 10 minutes and no error occurred (cf run #1 in Table 38 to Table 42)

10 Alpha results

10.1 Cross-section and FIT calculation

The cross-section defines the sensitivity of a device. The cross-section per chip is defined as $\sigma=N/(F*C)$ where N is the total number of errors, F is the fluence and C is the number of chips tested. In this document, the cross-section is given in cm²/chip.

The FIT is calculated by multiplying the cross-section by the alpha flux emitted by the real package F(package). The FIT rate per chip is:

$$FIT = \sigma(Am241) * F(package) * 10^9 \ (error/10^9 hour/chip)$$

The FIT provided in this report is based on an assumption for package emission F(package) equal to 0.001 α/cm²/hour.

10.2 Overall FIT results

Table 48 presents the overall alpha particle FIT for an emission rate equal to 0.001 α/cm²/hour. The overall FIT is calculated as the average of all chips and test conditions for the XC2V3000, XC3S1000 and EP1C20 devices. Appendix A details the cross-section and FIT for each chip and test condition.

Device	Overall FIT (SEFI) per Device	Overall FIT (SEU) per Device
AX1000	< 0.00087	<0.00087
APA1000	< 0.00087	<0.00087
XC2V3000	140 (note 1)	1040
XC3S1000	260	940
EP1C20	100	n/a

Table 48. Overall alpha particle FIT for 0.001 a/cm²/hour

Note 1: the SEFI FIT of XC2V3000 was extrapolated by multiplying the SEU FIT by the SEFI/SEU FIT ratio measured in cosmic-rays tests, 13.5%.

In Table 48, it is important to understand that no errors were observed for the AX1000 and APA1000, for any of the test conditions. The given figure of FIT is an upper bound calculated considering one error for all chips and test conditions. The AX1000 and APA1000, based in Antifuse and Flash processes respectively, are considered insensitive to alpha particles emitted from the packaging, therefore extending the test for longer periods would still produce no errors, and result in lower bounds of FIT.

The readback of the configuration memory is not available for the EP1C20. Therefore, the SEU FIT could not be measured for the EP1C20.

10.3 Accuracy of results

The accuracy of the cross-section results is assessed in this section. The accuracy of the cross-section is the sum of the error count and fluence measurement accuracies.

10.3.1 Error count statistics

The error count is generally described by a Poisson distribution, cf appendix C.1 in [2]. If N errors occur, the mean error count is approximated by N. The standard deviation is given by √N.

The error count can be bounded using the upper and lower limits in Table 11, extracted from appendix C.2 of [2]. In using this table, the first column is the actual number of events observed in the experiment. The upper and lower limits define the 95% confidence interval for the true mean of the distribution. The upper and lower limits for any number of events can be calculated using the formulas given in appendix B.

The accuracy of the error count is defined in this report using 95% confidence intervals. The 95% confidence limits depend on the number of errors observed. The number of errors is detailed in appendix A for each chip and test condition.

The following table summarizes the 95% confidence intervals for each device. For example, the overall number of SEU per chip and test condition is 235 for the XC2V3000. By using the formulas given in appendix B, we find that the lower and upper limits are 205.9 and 267.0 respectively. The limits in Table 49 are calculated as (Lower limit/Mean error count – 1)*100 = -12%, and (Upper limit/Mean error count – 1)*100 = +14%.

Device	Error type	Errors	Lower limit	Upper limit	Comment
AX1000	SEFI	0	n/a	n/a	No errors observed
APA1000	SEFI	0	n/a	n/a	No errors observed
XC2V3000	SEFI	n/a	n/a	n/a	Errors per chip and test condition
		n/a	n/a	n/a	Errors for all chips per test condition
		n/a	n/a	n/a	Errors for all chips and test conditions
	SEU	235	-12%	+14%	Errors per chip and test condition
		471	-9%	+9%	Errors for all chips per test condition
XC3S1000	SEFI	110	-18%	+21%	Errors per chip and test condition
		329	-11%	+11%	Errors for all chips per test condition
		1315	-6%	+6%	Errors for all chips and test conditions
	SEU	395	-10%	+10%	Errors per chip and test condition
		1186	-6%	+6%	Errors for all chips per test condition
EP1C20	SEFI	45	-27%	+34%	Errors per chip and test condition
		90	-20%	+23%	Errors for all chips per test condition
		359	-10%	+11%	Errors for all chips and test conditions

Table 49. 95% confidence intervals for all devices

10.3.2 Fluence measurement accuracy

The accuracy of the fluence measurement is indicated in Table 50.

Device	Source No.	Accuracy
AX1000	1	10%
APA1000	1	10%
XC2V3000	2	6%
XC3S1000	2	6%
EP1C20	2	6%

Table 50. Alpha source utilization and accuracy for each device

10.4 Detailed analysis

Detailed analysis of the results is presented hereafter. The following table summarizes the analyses presented for each device:

Analysis	AX1000	APA1000	XC2V3000	XC3S1000	EP1C20
Voltage influence on FIT			√	√	√
Analysis of critical vs non critical SEU				√	
Analysis of single event latchup	√		√	√	√
Bitmaps of errors			√	√	
Chip to chip variations			√	√	√
Special observations	√	√	√	√	√

Table 51. Detailed analysis for alpha tests

Many of the detailed analysis cannot be performed for the AX1000 and APA1000 because no errors were observed for these devices.

10.4.1 Voltage influence on FIT

The SEFI and SEU FIT dependence vs VDD is presented in this section. The FIT is plotted separately for each chip. The FIT average of all chips is also plotted, and the average FIT is used to fit an exponential curve.

10.4.1.1 XC2V3000

Figure 50 shows a regular decrease of FIT at the higher VDD.

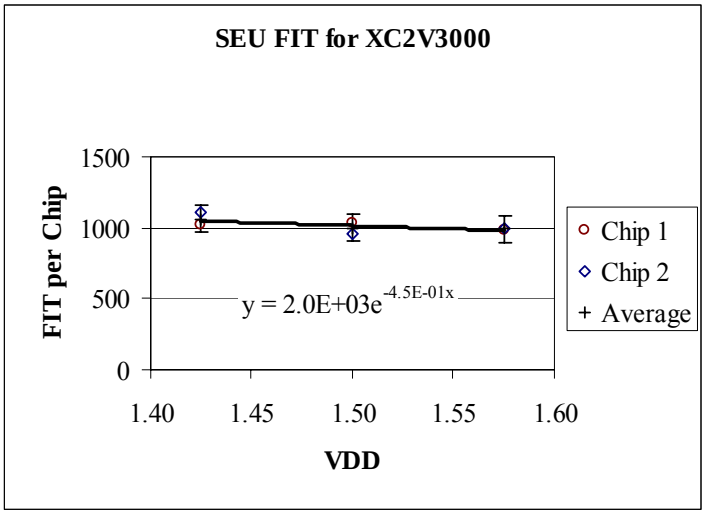


Figure 50. SEU FIT of XC2V3000 vs VDD

10.4.1.2 XC3S1000

Figure 51 and Figure 52 show a regular decrease of FIT at the higher VDD, as expected. The SEU FIT of chip no. 3 is higher than the uncertainty assessment made in section 10.3.1. This dispersion will be studied in section 10.4.5.2.

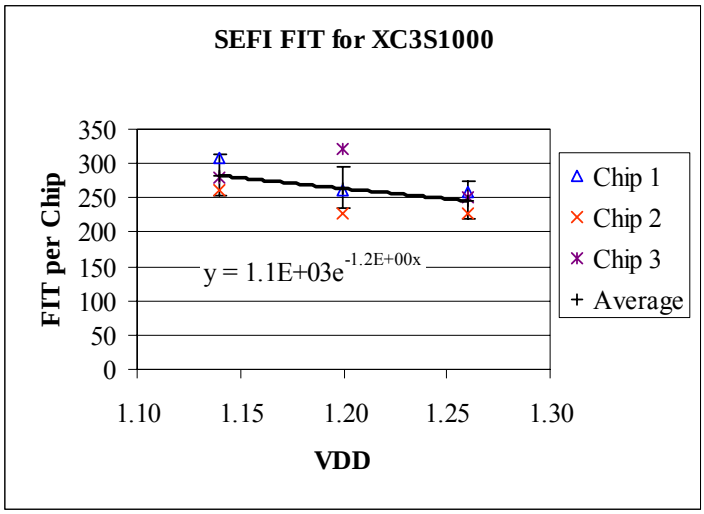


Figure 51. SEFI FIT of XC3S1000 vs VDD

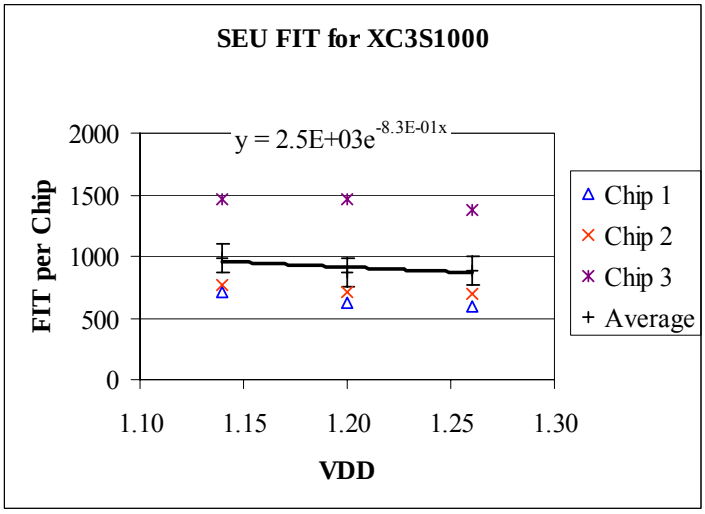


Figure 52. SEU FIT of XC3S1000 vs VDD

10.4.1.3 EP1C20

Figure 53 shows a regular decrease of FIT at the higher VDD.

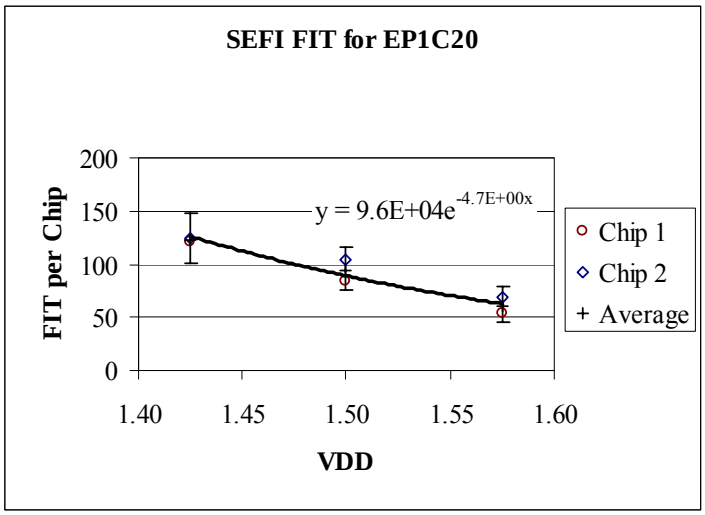


Figure 53. SEFI FIT of EP1C20 vs VDD

10.4.2 Analysis of critical vs non critical SEU

The test strategy enables to identify the critical and the non critical SEU in the configuration memory, that is, those SEU in the configuration memory that create an SEFI, and those that do not create an SEFI.

10.4.2.1 XC3S1000

Figure 54 presents the ratio SEFI / Total SEU for each chip and test condition. The overall ratio is 28% independent of the test condition.

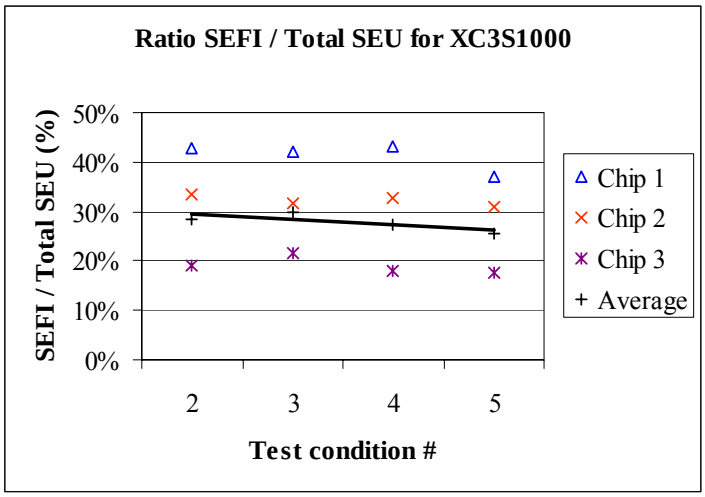


Figure 54. SEFI vs Total SEU XC3S1000

10.4.3 Analysis of single event latchup

Single event latchup (SEL) consists in the radiation induced activation of parasitic thyristor structures in the CMOS process. In case a process is sensitive to latchup, the latchup rate is higher at the higher voltage, temperature and particle energy.

Latchups result in increased current consumption, partial or total configuration memory wipe out, or complete loss of operation. Because the current is limited for protection, latchups lead to voltage shutdown to the DUT. The way the tester detects latchups is by monitoring the DUT supply voltages. In case a latchup is detected, the tester logs the event and switches the power off/on for recovering.

A particular case of latchup is the microlatchup. The microlatchup consists in the activation of a parasitic thyristor structure with weak on-resistance and a low increase of current consumption. In case of microlatchup, the voltage and current can find a stability point that cannot be detected by the tester. In this case, one or more chips are partially or totally wiped out, or experience complete loss of operation during the duration of a test condition.

No latchups were detected for any of the devices and conditions tested. In the following subsections, the voltage and current waveforms, acquired during the experiments, will be presented for each device and test condition. The sensitivity to microlatchup will be analyzed by inspection of the voltage and current waveforms and correlation with the observed number of errors in each chip.

10.4.3.1 AX1000

We observe regular voltage and current waveforms in Figure 55 and Figure 56. No errors were observed for any of the chips and conditions tested. Therefore, there is no indication of latchup.

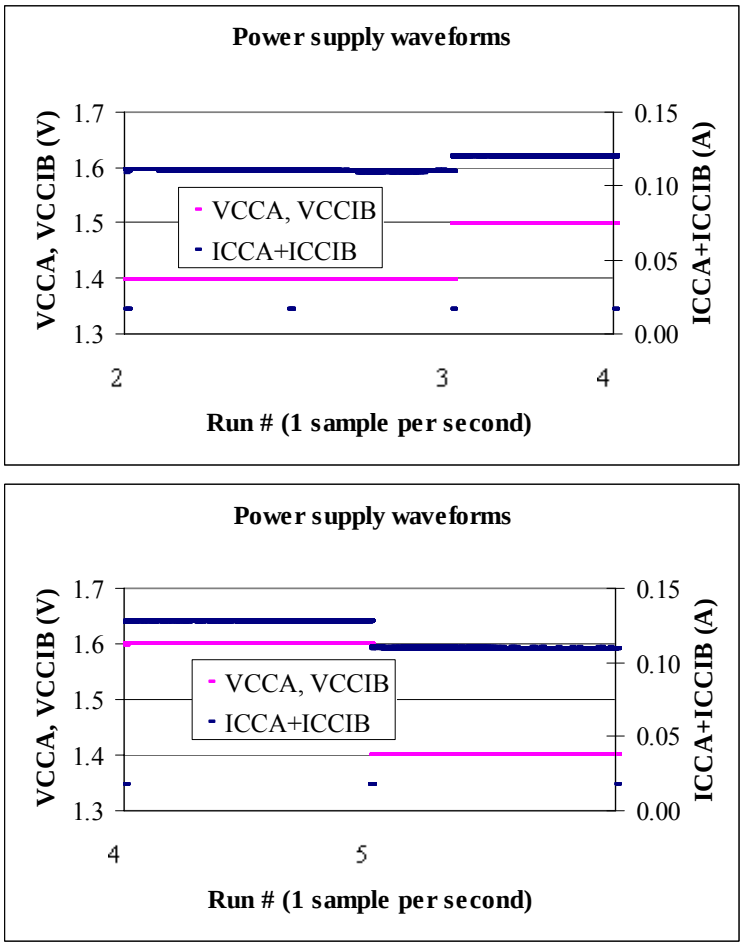


Figure 55. AX1000 VCCA and VCCIB waveforms

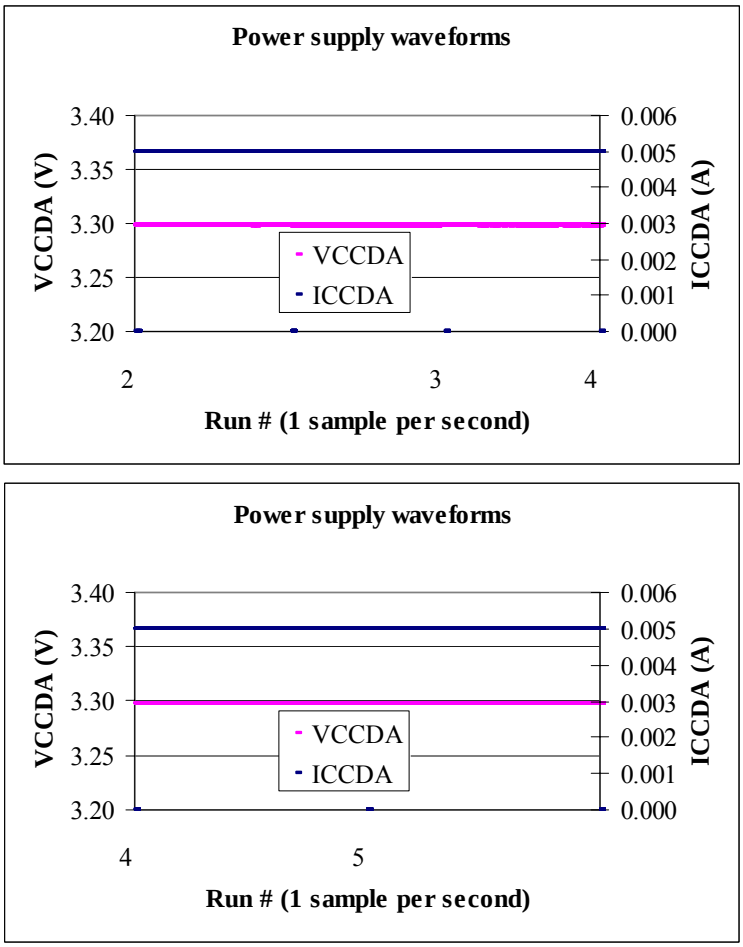


Figure 56. AX1000 VCCDA waveform

10.4.3.2 XC2V3000

The voltage and current waveforms could not be acquired during the experiments for the XC2V3000. The number of SEU errors, presented in the following table is regular across the chips tested. Therefore, there is no indication of latchup.

Run #	Condition	Number of SEU	
	VDD	Chip 1	Chip 2
1	1.425	0	0
2	1.425	230	250
3	1.500	233	218
4	1.575	222	227
5	1.425	251	251

Table 52. XC2V3000 number of SEU for each chip

10.4.3.3 XC3S1000

The voltage and current waveforms could not be acquired during the experiments for the XC3S1000. The number of SEFI errors, presented in the following table is regular across the six chips tested. Therefore, there is no indication of latchup.

Run #	Condition	Number of SEFI		
	VDD	Chip 1	Chip 2	Chip 3
1	1.14	0	0	0
2	1.14	131	112	119
3	1.20	112	97	96
4	1.26	111	98	107
5	1.14	104	114	114

Table 53. XC3S1000 number of SEFI for each chip

Note: run #1 was a test run with the beam switched off, to test that the tester electronics was working correctly (cf section 9.4).

10.4.3.4 EP1C20

The voltage and current waveforms could not be acquired during the experiments for the EP1C20. The number of SEFI errors, presented in the following table is regular across the chips tested. Therefore, there is no indication of latchup.

Run #	Condition	Number of SEFI	
	VDD	Chip 1	Chip 2
1	1.425	0	0
2	1.425	53	56
3	1.500	38	47
4	1.575	24	31
5	1.425	54	56

Table 54. EP1C20 number of SEFI for each chip

10.4.4 Bitmaps of errors

Bitmaps allow to check the expected random distribution of errors in the configuration memory arrays.

Each point in the bitmap represents a failing address. The bitmaps are logical bitmaps, not physical bitmaps, because the layout of the configuration memory is not available. In the logical bitmaps, the address LSB are mapped in the x-axis and the address MSB are mapped in the y-axis.

10.4.4.1 XC2V3000

The address refers to the location where the verification bitstream is stored in the tester memory. Valid addresses for the XC2V3000 are in the range 0x400069 to 0x5D4329. Each address holds 5 bits. Therefore, the verification bitstream length is 9,588,165 bits.

The bitmaps show the expected random distribution of errors.

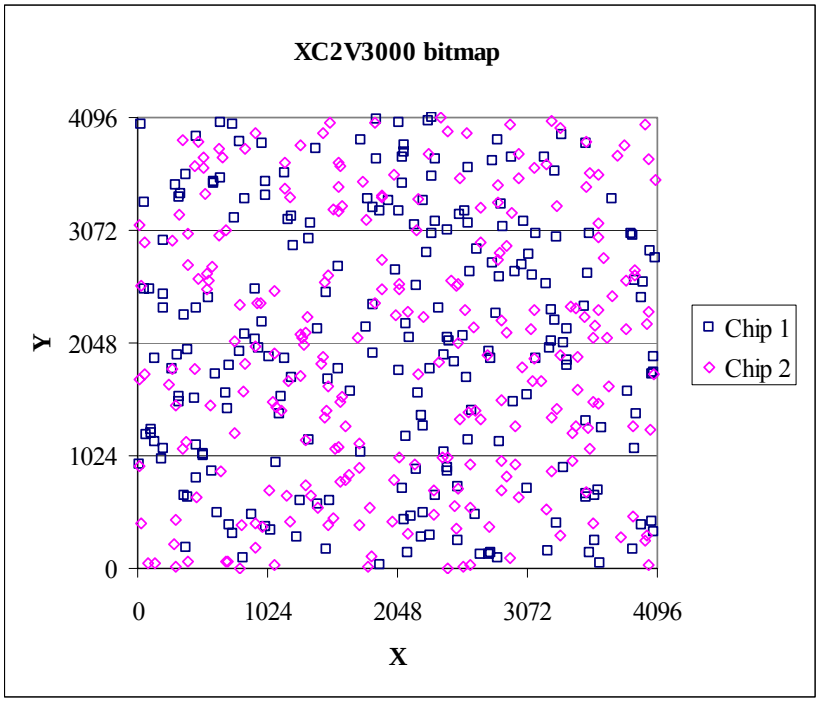


Figure 57. Bitmap for run#2 of XC2V3000

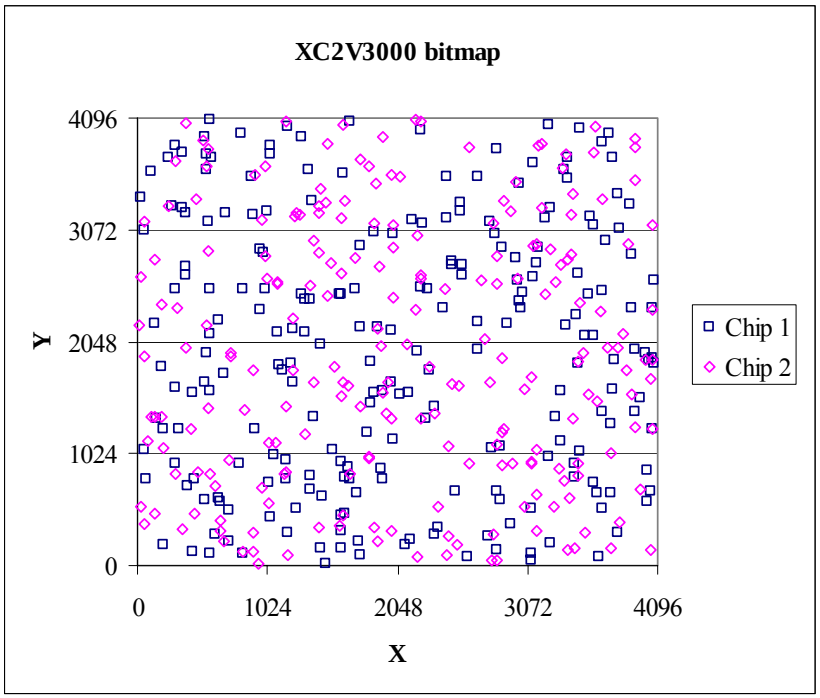


Figure 58. Bitmap for run#3 of XC2V3000

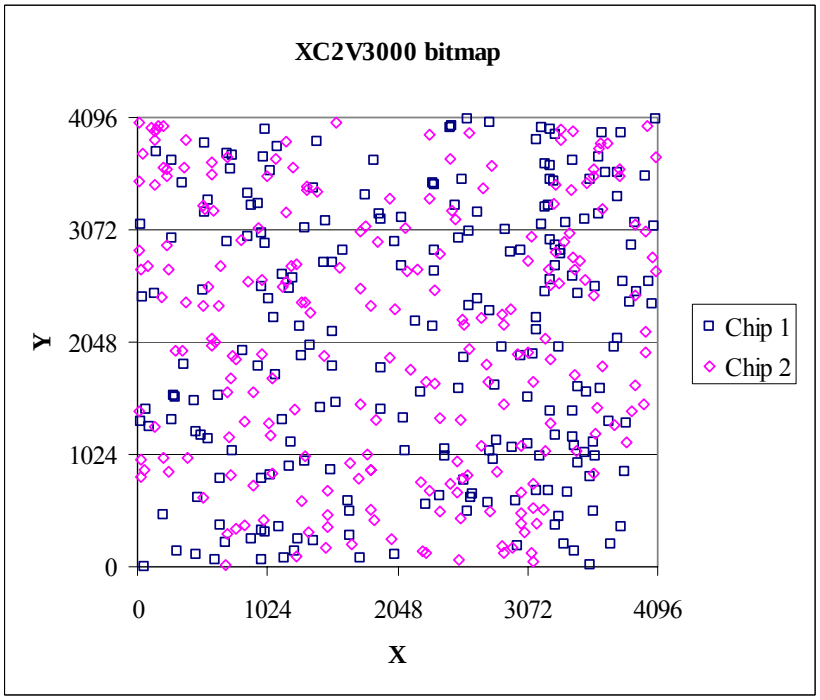


Figure 59. Bitmap for run#4 of XC2V3000

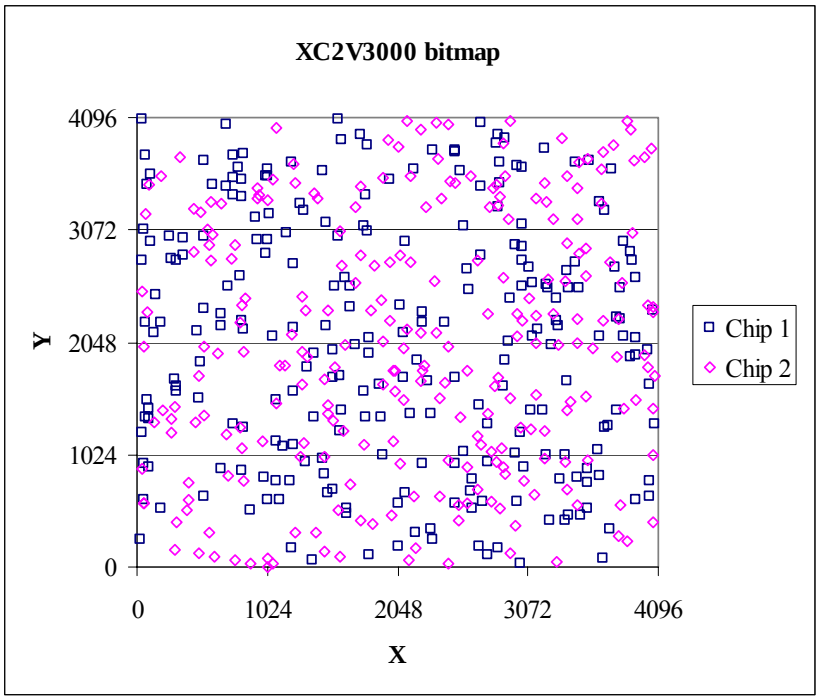


Figure 60. Bitmap for run#5 of XC2V3000

10.4.4.2 XC3S1000

The address refers to the location where the verification bitstream is stored in the tester memory. Valid addresses for the XC3S1000 are in the range 0x400068 to 0x49D349. Each address holds 5 bits. Therefore, the verification bitstream length is 3,219,050 bits.

The bitmaps show the expected random distribution of errors.

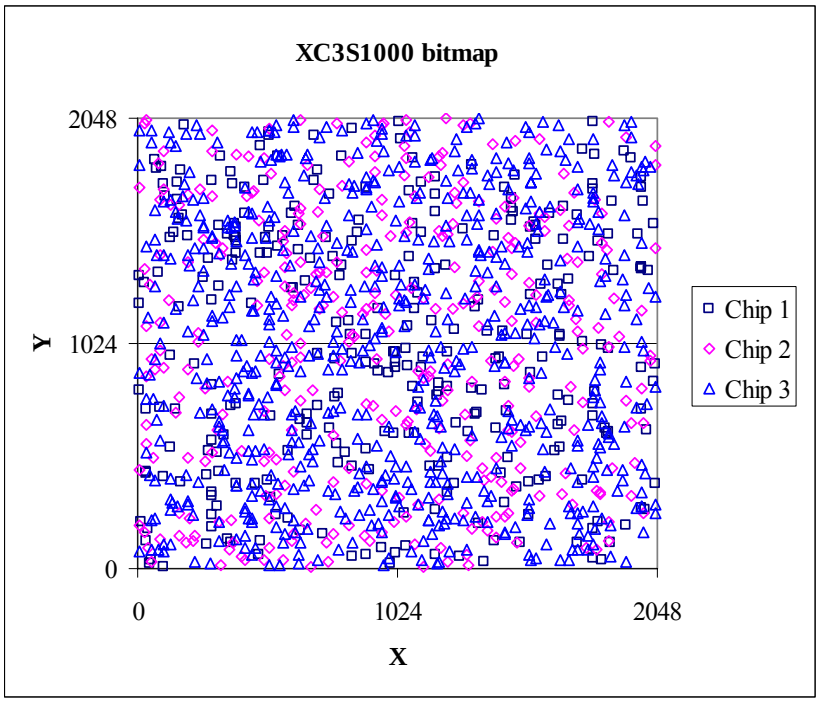


Figure 61. Bitmap for run#2 of XC3S1000

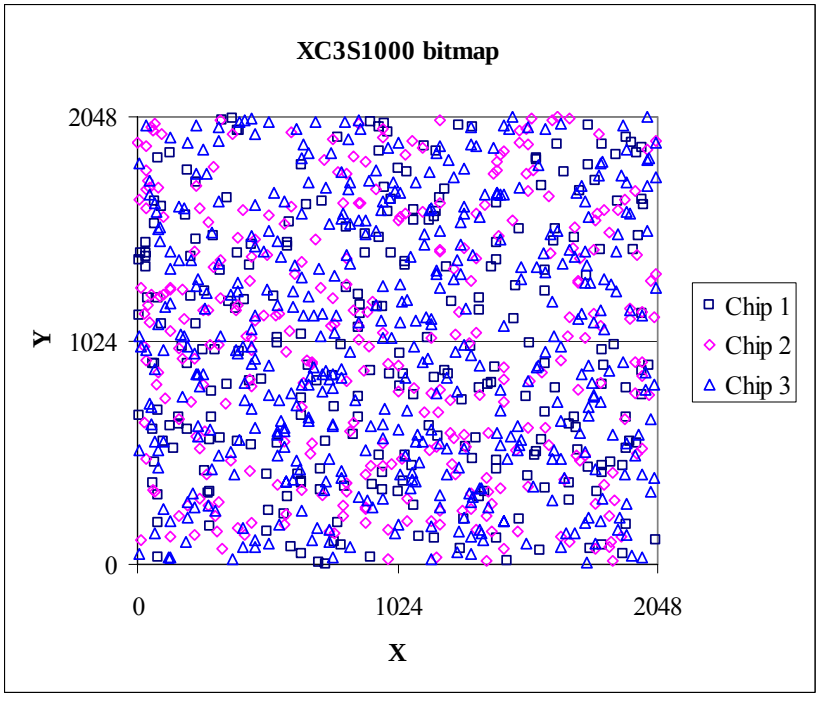


Figure 62. Bitmap for run#3 of XC3S1000

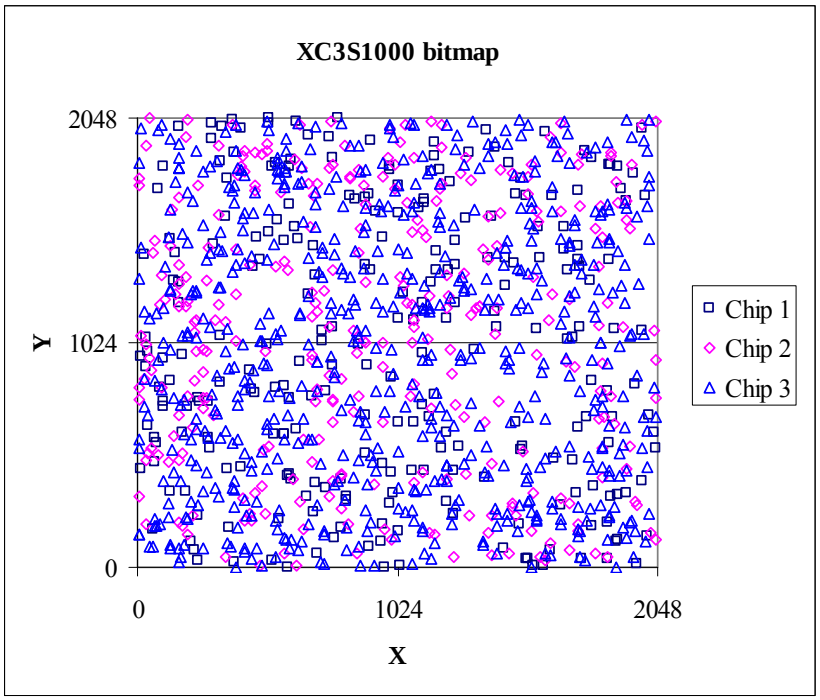


Figure 63. Bitmap for run#4 of XC3S1000

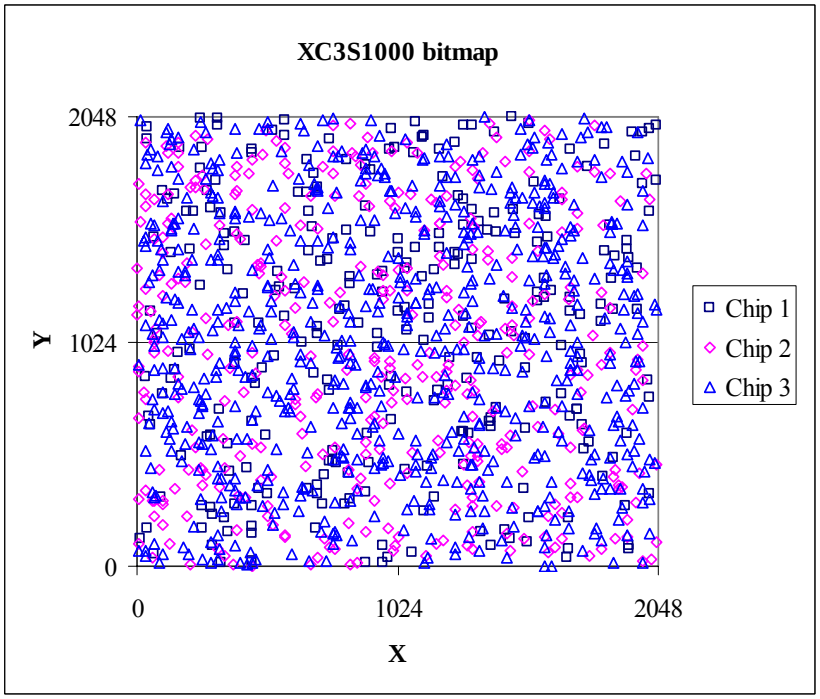


Figure 64. Bitmap for run#5 of XC3S1000

10.4.5 Chip to chip variation

This section presents the chip to chip FIT variations observed. The objective of this section is to compare the sensitivity of different chips.

The FIT variations are defined as the variation relative to the average of the chips tested.

$$\text{FIT variation for chip(i)}\,(\%) = \left(\frac{\text{FIT Chip(i)}}{\text{Average FIT Chips(1 to 3)}} - 1 \right) \times 100$$

10.4.5.1 XC2V3000

The FIT variations observed are within the expected statistical uncertainty: –12% to +14%, see Table 49.

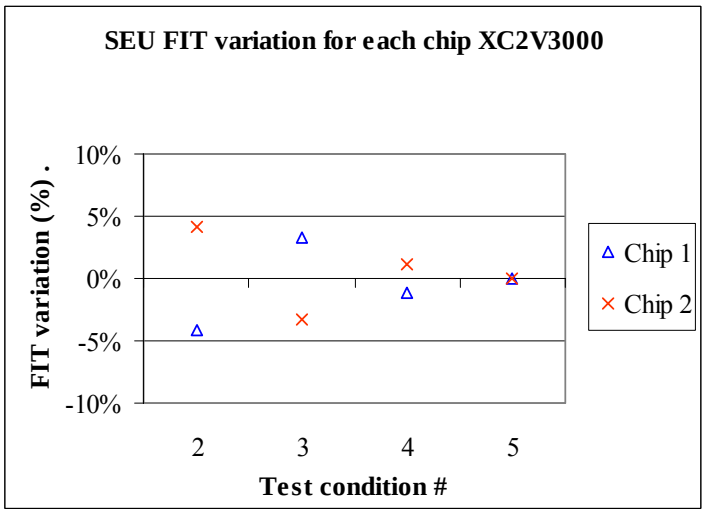


Figure 65. Chip to chip FIT variation for XC2V3000

10.4.5.2 XC3S1000

The FIT variation of chip no. 3 exceeds the assessed statistical uncertainty –10% to +10% (cf Table 49).

In order to explain this phenomenon, we consider that chips no. 1 and 2, and chip no. 3 come from two different lots (cf Table 46). Process or passivation layer thickness differences between the two lots should be assessed to confirm this explanation.

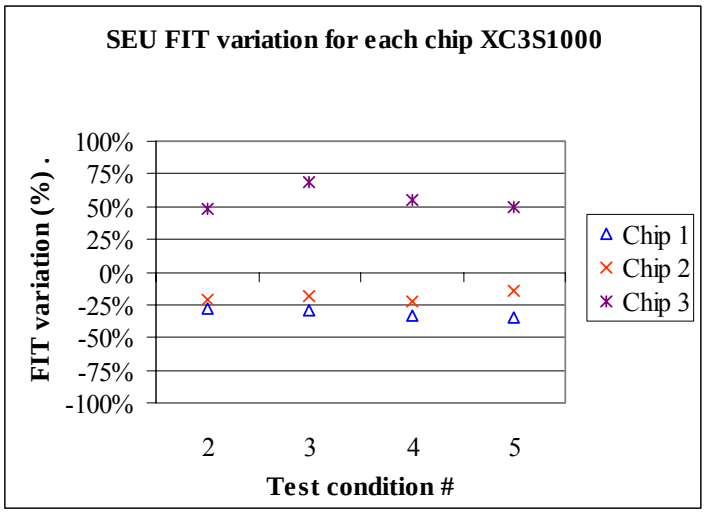


Figure 66. Chip to chip FIT variation for XC3S1000

10.4.5.3 EP1C20

The FIT variations observed are within the expected statistical uncertainty: –27% to +34%, see Table 49.

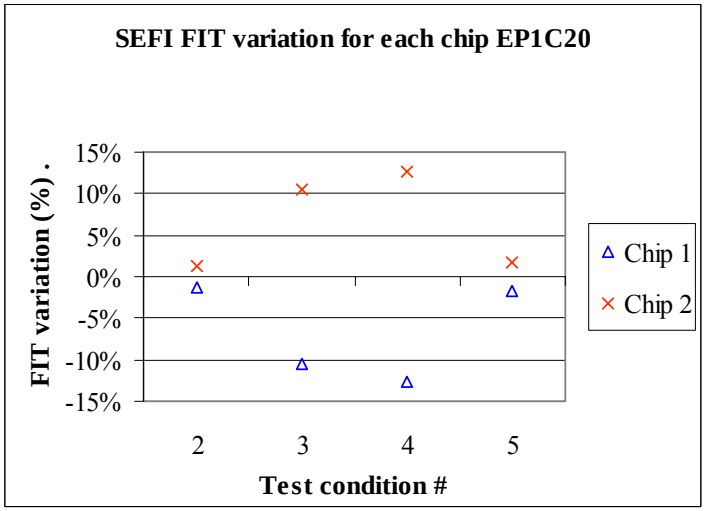


Figure 67. Chip to chip FIT variation for EP1C20

10.4.6 Consistency check

A consistency test (repetition of the first condition) has been carried out at the end of the test sequence. The consistency test verifies the stability of the alpha source, DUT and tester.

10.4.6.1 XC2V3000

Figure 68 verifies that the results of runs #2 and #5 are consistent, taking into account the statistical uncertainty shown by the error bars.

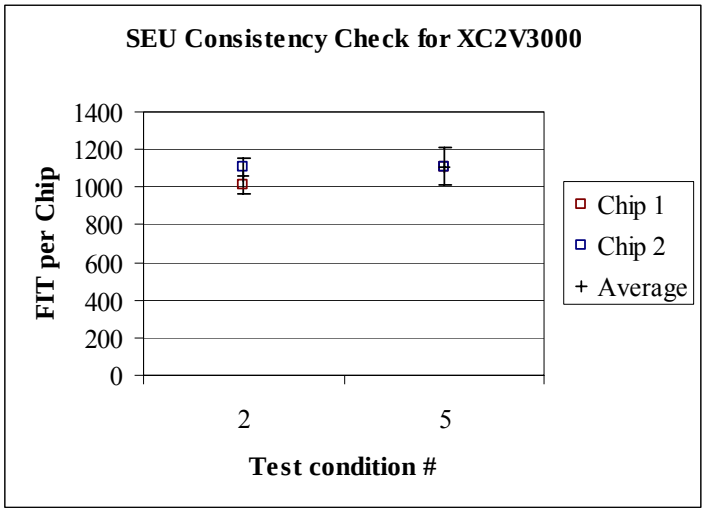


Figure 68. SEU consistency check for XC2V3000

10.4.6.2 XC3S1000

Figure 69 verifies that the results of runs #2 and #5 are consistent, taking into account the statistical uncertainty shown by the error bars.

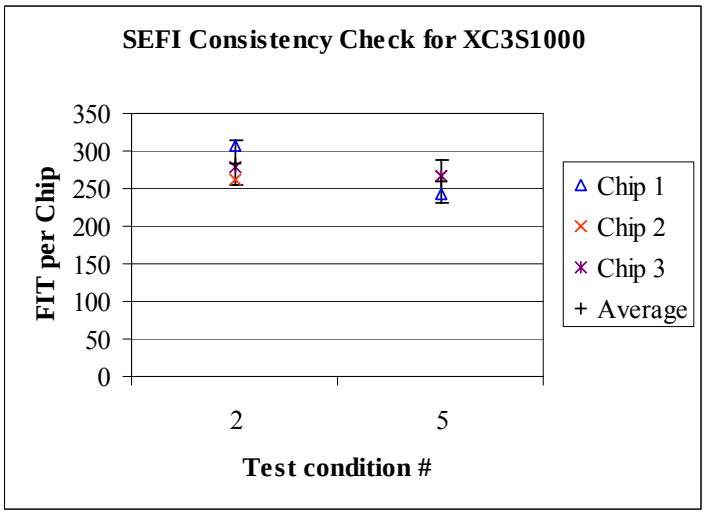


Figure 69. SEFI consistency check for XC3S1000

10.4.6.3 EP1C20

Figure 70 verifies that the results of runs #2 and #5 are consistent, taking into account the statistical uncertainty shown by the error bars.

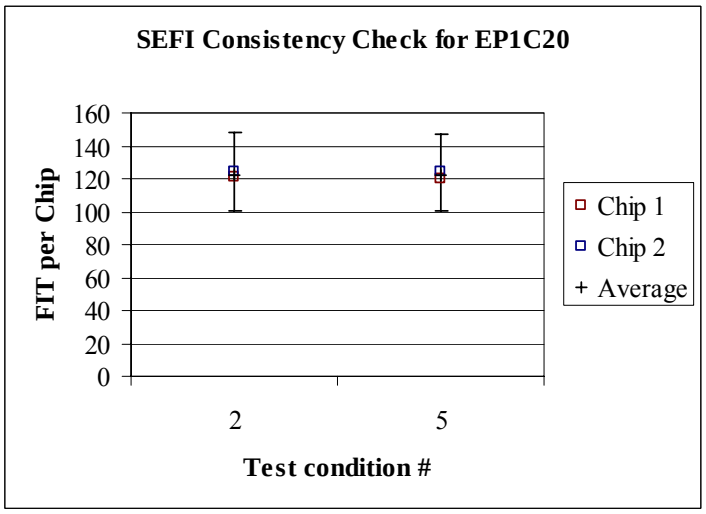


Figure 70. SEFI consistency check for EP1C20

10.4.7 Special observations

One occurrence of an error in the configuration circuitry of XC3S1000 was observed in run no. 3 for chip no 3. As a result, the readback operation failed and the configuration memory appeared to be entirely wiped out. The FIT rate for configuration circuitry failures is calculated using the formula in section 10.1 and considering that the total fluence for XC3S1000 was 5.0E+06 α/cm^2. Therefore, FIT = (1 event / 5.0E+06 α/cm^2) * 0.001 α/cm^2/hour * 1E+09 hour = 0.20.

A verify operation using the Flash Pro programmer was performed for the APA1000 chips, at the end of the radiation tests performed. The verify operation was successful for all the APA1000 chips.

11 Alpha conclusions

This test report provides the alpha particle SER of AX1000, APA1000, XC2V3000, XC3S1000 and EP1C20 devices. The alpha particle SER was measured at iRoC premises using calibrated Am241 foil sources in April and October 2004.

Table 55 presents the overall alpha particle FIT for an emission rate equal to 0.001 α/cm²/hour. The overall FIT is calculated as the average of all chips and test conditions for the XC2V3000, XC3S1000 and EP1C20 devices. Appendix A details the cross-section and FIT for each chip and test condition.

Device	Overall FIT (SEFI) per Device	Overall FIT (SEU) per Device
AX1000	< 0.00087	<0.00087
APA1000	< 0.00087	<0.00087
XC2V3000	140 (note 1)	1040
XC3S1000	260	940
EP1C20	100	n/a

Table 55. Overall alpha particle FIT for 0.001 a/cm²/hour

Note 1: the SEFI FIT of XC2V3000 was extrapolated by multiplying the SEU FIT by the SEFI/SEU FIT ratio measured in cosmic-rays tests, 13.5%.

In Table 55, it is important to understand that no errors were observed for the AX1000 and APA1000, for any of the test conditions. The given figure of FIT is an upper bound calculated considering one error for all chips and test conditions. The AX1000 and APA1000, based in Antifuse and Flash processes respectively, are considered insensitive to alpha particles emitted from the packaging, therefore extending the test for longer periods would still produce no errors, and result in lower bounds of FIT.

The readback of the configuration memory is not available for the EP1C20. Therefore, the SEU FIT could not be measured for the EP1C20.

No occurrences of latchup were observed for any of the devices. One error in the configuration circuitry of XC3S1000 was observed, and the resulting FIT is 0.20. No hard errors were observed for any of the devices.

A Details of cross-sections and FIT

A.1 14 MeV neutrons

AX1000

Run #	Device	Energy (MeV)	Start		Stop	Condition			Fluence 1 (neutron/cm²)	Fluence 2 (neutron/cm²)
			Date	Time	Time	Cycle	VDD	Temp		
1	AX1000	14	Dec-16	14:29:13	14:44:16	200ns	1.4	25°C	0.0E+00	0.0E+00
2	AX1000	14	Dec-16	14:47:15	16:59:27	200ns	1.4	25°C	6.5E+10	4.7E+10
3	AX1000	14	Dec-16	17:00:46	9:08:22	200ns	1.5	25°C	5.4E+10	3.9E+10
4	AX1000	14	Dec-17	9:10:42	10:21:37	200ns	1.6	25°C	6.4E+10	4.7E+10
5	AX1000	14				200ns	1.4	25°C		

Run #	Number of SEFI					FIT (SEFI/10^9hour/chip)					Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	
1	0	0	0	0	0	#	#	#	#	#	stability check
2	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	
3	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	
4	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	
5											consistency check, not done

APA1000

Run #	Device	Energy (MeV)	Start		Stop	Condition			Fluence 1 (neutron/cm²)	Fluence 2 (neutron/cm²)
			Date	Time	Time	Cycle	VDD	Temp		
1	APA1000	14	Dec-16	14:30:26	14:44:14	200ns	2.3	25°C	0.0E+00	0.0E+00
2	APA1000	14	Dec-16	14:47:31	16:59:35	200ns	2.3	25°C	3.6E+10	2.8E+10
3	APA1000	14	Dec-16	17:01:35	9:08:20	200ns	2.5	25°C	3.0E+10	2.3E+10
4	APA1000	14	Dec-17	9:10:45	10:21:34	200ns	2.7	25°C	3.5E+10	2.8E+10
5	APA1000	14				200ns	2.3	25°C		

Run #	Number of SEFI						FIT (SEFI/10^9hour/chip)						Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	
1	0	0	0	0	0	0	#	#	#	#	#	#	stability check
2	0	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	0.0	
3	0	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	0.0	
4	0	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	0.0	
5													consistency check, not done

XC2V3000

Run #	Device	Energy (MeV)	Start		Stop	Condition			Fluence 1 (neutron/cm²)	Fluence 2 (neutron/cm²)
			Date	Time	Time	Cycle	VDD	Temp		
1	XC2V3000	14	Dec-17	13:31:49	13:36:11	200ns	1.425	25°C	0.0E+00	0.0E+00
2	XC2V3000	14	Dec-17	13:36:31	14:29:04	200ns	1.425	25°C	3.5E+08	3.2E+08
3	XC2V3000	14	Dec-17	14:31:12	15:08:02	200ns	1.500	25°C	3.8E+08	3.5E+08
4	XC2V3000	14	Dec-17	15:08:40	15:46:06	200ns	1.575	25°C	3.7E+08	3.4E+08
5	XC2V3000	14	Dec-17	15:52:07	16:34:41	200ns	1.425	25°C	4.0E+08	3.7E+08

Run #	Number of SEFI						FIT (SEFI/10^9hour/chip)						Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	
1	0	0	0	0	0	0	#	#	#	#	#	#	stability check
2	22	17	25	19	11	11	887	685	1007	836	484	484	
3	21	12	18	21	17	18	764	437	655	834	675	715	
4	14	16	15	25	13	18	527	602	564	1027	534	739	
5	14	18	23	20	16	16	491	631	806	765	612	612	consistency check

Run #	Number of SEU						FIT (SEU/10^9hour/chip)						Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	
1	0	0	0	0	0	0	#	#	#	#	#	#	stability check
2	138	116	139	118	93	97	5561	4675	5601	5191	4091	4267	
3	131	124	133	127	111	126	4766	4512	4839	5044	4409	5005	
4	132	117	114	122	108	105	4965	4401	4288	5010	4435	4312	
5	145	137	144	112	101	130	5080	4800	5045	4284	3863	4972	consistency check

A.2 LANSCE

AX1000

Run #	Device	Energy (MeV)	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	AX1000	LANSCE	17-Feb	14:27:15	17-Feb	14:38:02	200ns	1.4	25°C
2	AX1000	LANSCE	17-Feb	15:46:19	17-Feb	22:40:35	200ns	1.4	25°C
3	AX1000	LANSCE	17-Feb	22:41:50	18-Feb	4:27:11	200ns	1.5	25°C
4	AX1000	LANSCE	18-Feb	4:28:29	18-Feb	9:46:52	200ns	1.6	25°C
5									

Run #	Fluence (n/cm²)				
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5
1	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
2	1.2E+10	1.2E+10	1.2E+10	1.3E+10	1.2E+10
3	1.0E+10	1.0E+10	1.0E+10	1.1E+10	1.0E+10
4	1.2E+10	1.1E+10	1.1E+10	1.2E+10	1.1E+10
5					

Run #	Number of SEFI					FIT (SEFI/10^9hour/chip)					Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	
1	0	0	0	0	0	#	#	#	#	#	stability check
2	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	
3	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	
4	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	
5											consistency check not done

APA1000

Run #	Device	Energy (MeV)	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	APA1000	LANSCE	18-Feb	10:36:44	18-Feb	10:46:44	200ns	2.3	25°C
2	APA1000	LANSCE	18-Feb	10:47:46	18-Feb	15:21:14	200ns	2.3	25°C
3	APA1000	LANSCE	18-Feb	15:22:12	18-Feb	21:07:56	200ns	2.5	25°C
4	APA1000	LANSCE	18-Feb	21:09:08	19-Feb	5:55:00	200ns	2.7	25°C
5	APA1000	LANSCE	19-Feb	5:56:33	19-Feb	21:26:26	200ns	2.3	25°C

Run #	Fluence (n/cm²)				
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5
1	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
2	1.2E+10	1.1E+10	1.1E+10	1.2E+10	1.1E+10
3	1.3E+10	1.2E+10	1.2E+10	1.3E+10	1.1E+10
4	1.3E+10	1.2E+10	1.1E+10	1.3E+10	1.1E+10
5	4.1E+10	3.7E+10	3.7E+10	4.0E+10	3.7E+10

Run #	Number of SEFI					FIT (SEFI/10^9hour/chip)					Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	
1	0	0	0	0	0	#	#	#	#	#	stability check
2	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	
3	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	
4	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	
5	0	0	0	0	0	0.0	0.0	0.0	0.0	0.0	consistency check

XC2V3000

Run #	Device	Energy (MeV)	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	XC2V3000	LANSCE	17-Feb	14:28:11	17-Feb	14:38:56	200ns	1.425	25°C
2	XC2V3000	LANSCE	17-Feb	15:46:53	17-Feb	15:57:28	200ns	1.425	25°C
3	XC2V3000	LANSCE	17-Feb	15:59:04	17-Feb	16:09:44	200ns	1.500	25°C
4	XC2V3000	LANSCE	17-Feb	16:10:38	17-Feb	16:22:29	200ns	1.575	25°C
5	XC2V3000	LANSCE	17-Feb	16:23:38	17-Feb	16:35:45	200ns	1.425	25°C

Run #	Fluence SEFI (n/cm²)						Fluence SEU (n/cm²)					
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6
1	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
2	1.9E+08	1.7E+08	1.9E+08	1.8E+08	1.7E+08	1.8E+08	2.4E+08	2.2E+08	2.4E+08	2.4E+08	2.1E+08	2.3E+08
3	1.6E+08	1.5E+08	1.6E+08	1.6E+08	1.5E+08	1.6E+08	2.2E+08	2.0E+08	2.2E+08	2.2E+08	2.0E+08	2.2E+08
4	2.0E+08	1.8E+08	2.0E+08	2.0E+08	1.8E+08	2.0E+08	2.6E+08	2.3E+08	2.5E+08	2.5E+08	2.3E+08	2.5E+08
5	1.9E+08	1.7E+08	1.9E+08	1.9E+08	1.7E+08	1.9E+08	2.5E+08	2.3E+08	2.5E+08	2.5E+08	2.3E+08	2.5E+08

Run #	Number of SEFI						FIT (SEFI/10^9hour/chip)						Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	
1	0	0	0	0	0	0	#	#	#	#	#	#	stability check
2	14	10	10	13	12	17	1045	825	754	984	1003	1299	
3	20	9	16	18	15	14	1723	856	1391	1571	1446	1234	
4	14	18	13	15	16	13	979	1390	918	1064	1253	931	
5	16	11	16	11	20	18	1173	890	1184	817	1640	1350	consistency check

Run #	Number of SEU						FIT (SEU/10^9hour/chip)						Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	
1	0	0	0	0	0	0	#	#	#	#	#	#	stability check
2	155	101	167	130	135	168	9053	6514	9847	7696	8824	10040	
3	168	127	126	136	111	157	10614	8860	8037	8709	7848	10149	
4	146	137	151	148	127	142	7978	8266	8329	8196	7766	7939	
5	171	147	195	136	125	153	9417	8938	10841	7591	7704	8621	consistency check

XC3S1000

Run #	Device	Energy (MeV)	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	XC3S1000	LANSCE	17-Feb	17:16:20	17-Feb	17:25:22	200ns	1.140	25°C
2	XC3S1000	LANSCE	17-Feb	17:25:56	17-Feb	17:51:15	200ns	1.140	25°C
3	XC3S1000	LANSCE	17-Feb	17:52:36	17-Feb	19:40:45	200ns	1.200	25°C
4	XC3S1000	LANSCE	17-Feb	19:41:23	17-Feb	20:07:31	200ns	1.260	25°C
5	XC3S1000	LANSCE	17-Feb	20:08:11	17-Feb	20:23:55	200ns	1.140	25°C

Run #	Fluence SEFI (n/cm²)						Fluence SEU (n/cm²)					
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6
1	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
2	7.8E+08	7.4E+08	6.7E+08	7.0E+08	7.7E+08	8.1E+08	8.4E+08	8.0E+08	7.2E+08	7.5E+08	8.3E+08	8.7E+08
3	8.5E+08	8.1E+08	7.3E+08	7.7E+08	8.5E+08	8.9E+08	9.3E+08	8.9E+08	8.0E+08	8.3E+08	9.2E+08	9.6E+08
4	8.4E+08	8.0E+08	7.2E+08	7.5E+08	8.3E+08	8.7E+08	9.1E+08	8.7E+08	7.8E+08	8.1E+08	9.0E+08	9.4E+08
5	4.4E+08	4.2E+08	3.8E+08	4.0E+08	4.4E+08	4.6E+08	4.9E+08	4.7E+08	4.2E+08	4.4E+08	4.9E+08	5.1E+08

Run #	Number of SEFI						FIT (SEFI/10^9hour/chip)						Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	
1	0	0	0	0	0	0	#	#	#	#	#	#	stability check
2	21	14	13	10	29	13	378	264	273	201	527	225	
3	20	20	21	9	27	23	328	344	401	165	447	363	
4	26	21	14	17	18	12	435	368	273	317	304	193	
5	13	15	6	11	18	14	411	497	221	388	574	426	consistency check

Run #	Number of SEU						FIT (SEU/10^9hour/chip)						Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	
1	0	0	0	0	0	0	#	#	#	#	#	#	stability check
2	96	73	52	70	95	97	1598	1276	1009	1300	1597	1556	
3	87	67	71	47	81	90	1311	1060	1246	790	1232	1307	
4	89	59	54	78	77	75	1371	954	969	1341	1198	1113	
5	104	100	82	93	104	95	2971	2999	2729	2965	3000	2616	consistency check

EP1C20

Run #	Device	Energy (MeV)	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	EP1C20	LANSCE	17-Feb	20:58:26	17-Feb	21:08:40	200ns	1.425	25°C
2	EP1C20	LANSCE	17-Feb	21:09:30	17-Feb	21:27:50	200ns	1.425	25°C
3	EP1C20	LANSCE	17-Feb	21:49:43	17-Feb	22:03:20	200ns	1.500	25°C
4	EP1C20	LANSCE	17-Feb	22:04:36	17-Feb	22:21:21	200ns	1.575	25°C
5	EP1C20	LANSCE	17-Feb	22:22:38	17-Feb	22:39:26	200ns	1.425	25°C

Run #	Fluence SEFI (n/cm²)					
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6
1	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
2	6.4E+08	5.9E+08	5.5E+08	6.2E+08	6.7E+08	6.9E+08
3	4.9E+08	4.5E+08	4.2E+08	4.7E+08	5.1E+08	5.2E+08
4	6.2E+08	5.7E+08	5.3E+08	5.9E+08	6.5E+08	6.6E+08
5	6.2E+08	5.6E+08	5.3E+08	5.9E+08	6.5E+08	6.6E+08

Run #	Number of SEFI						FIT (SEFI/10^9hour/chip)						Comments
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	
1	0	0	0	0	0	0	#	#	#	#	#	#	stability check
2	24	17	10	14	28	14	522	405	254	317	581	285	
3	17	16	6	16	27	22	488	503	201	478	740	592	
4	19	21	21	17	11	19	430	520	555	400	237	403	
5	29	11	21	28	23	22	656	273	555	659	497	467	consistency check

A.3 Alpha

AX1000

Run #	Device	Particle	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	AX1000	α–Am241	9-Apr	10:22:02	9-Apr	10:34:02	200ns	1.4	25°C
21	AX1000	α–Am241	9-Apr	10:50:02	10-Apr	2:50:01	200ns	1.4	25°C
22	AX1000	α–Am241	12-Apr	19:45:04	13-Apr	11:45:03	200ns	1.4	25°C
31	AX1000	α–Am241	10-Apr	2:53:03	10-Apr	18:53:02	200ns	1.5	25°C
32	AX1000	α–Am241	13-Apr	11:48:04	14-Apr	3:48:03	200ns	1.5	25°C
41	AX1000	α–Am241	10-Apr	18:56:03	11-Apr	10:56:02	200ns	1.6	25°C
42	AX1000	α–Am241	14-Apr	3:51:04	14-Apr	19:51:03	200ns	1.6	25°C
51	AX1000	α–Am241	11-Apr	10:59:03	12-Apr	2:59:03	200ns	1.4	25°C
52	AX1000	α–Am241	14-Apr	19:54:05	15-Apr	11:54:04	200ns	1.4	25°C

Run #	Fluence (α/cm²)		Number of SEFI		FIT SEFI		Comments
	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 2	
1	0.0E+00	0.0E+00	0	0	#	#	stability check
21	1.4E+08		0		0		
22		1.4E+08		0		0	
31	1.4E+08		0		0		
32		1.4E+08		0		0	
41	1.4E+08		0		0		
42		1.4E+08		0		0	
51	1.4E+08		0		0		consistency check
52		1.4E+08		0		0	consistency check

APA1000

Run #	Device	Particle	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
21	APA1000	α–Am241	27-Apr	17:00:00	30-Apr	9:00:00	n/a	n/a	n/a
22	APA1000	α–Am241	30-Apr	17:00:00	3-May	9:00:00	n/a	n/a	n/a

Run #	Fluence (α/cm²)		Number of SEFI		FIT SEFI		Comments
	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 2	
21	5.7E+08		0		0	#	
22		5.7E+08		0	#	0	

XC2V3000

Run #	Device	Particle	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	XC2V3000	α–Am241	8-Oct	12:02:15	8-Oct	14:31:15	200ns	1.43	25°C
21	XC2V3000	α–Am241	8-Oct	19:16:10	8-Oct	22:17:06	200ns	1.43	25°C
22	XC2V3000	α–Am241	9-Oct	11:46:14	9-Oct	14:47:10	200ns	1.43	25°C
31	XC2V3000	α–Am241	8-Oct	22:19:11	9-Oct	1:20:07	200ns	1.50	25°C
32	XC2V3000	α–Am241	10-Oct	12:11:21	10-Oct	15:12:17	200ns	1.50	25°C
41	XC2V3000	α–Am241	9-Oct	1:22:11	9-Oct	4:23:07	200ns	1.58	25°C
42	XC2V3000	α–Am241	10-Oct	15:14:22	10-Oct	18:15:18	200ns	1.58	25°C
51	XC2V3000	α–Am241	9-Oct	4:25:12	9-Oct	7:26:08	200ns	1.43	25°C
52	XC2V3000	α–Am241	10-Oct	18:17:23	10-Oct	21:18:20	200ns	1.43	25°C

Run #	Fluence SEU (α/cm²)		Number of SEU		FIT SEU		Comments
	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 2	
1	0.0E+00	0.0E+00	0	0	#	#	stability check
21	2.3E+05		230		1015	#	
22		2.3E+05		250	#	1103	
31	2.3E+05		233		1028	#	
32		2.3E+05		218	#	962	
41	2.3E+05		222		980	#	
42		2.3E+05		227	#	1002	
51	2.3E+05		251		1108	#	consistency check
52		2.3E+05		251	#	1108	consistency check

XC3S1000

Run #	Device	Particle	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	XC3S1000	α–Am241	9-Apr	11:28:01	9-Apr	11:38:02	200ns	1.14	25°C
24	XC3S1000	α–Am241	9-Apr	12:13:02	9-Apr	18:13:01	200ns	1.14	25°C
25	XC3S1000	α–Am241	10-Apr	12:30:02	10-Apr	18:30:02	200ns	1.14	25°C
26	XC3S1000	α–Am241	11-Apr	12:55:03	11-Apr	18:55:03	200ns	1.14	25°C
34	XC3S1000	α–Am241	9-Apr	18:16:02	10-Apr	0:16:02	200ns	1.20	25°C
35	XC3S1000	α–Am241	10-Apr	18:33:02	11-Apr	0:33:02	200ns	1.20	25°C
36	XC3S1000	α–Am241	11-Apr	18:58:02	12-Apr	0:58:02	200ns	1.20	25°C
44	XC3S1000	α–Am241	10-Apr	0:19:02	10-Apr	6:19:01	200ns	1.26	25°C
45	XC3S1000	α–Am241	11-Apr	0:36:03	11-Apr	6:36:02	200ns	1.26	25°C
46	XC3S1000	α–Am241	12-Apr	1:01:03	12-Apr	7:01:02	200ns	1.26	25°C
54	XC3S1000	α–Am241	10-Apr	6:22:02	10-Apr	12:22:02	200ns	1.14	25°C
55	XC3S1000	α–Am241	11-Apr	6:39:02	11-Apr	12:39:02	200ns	1.14	25°C
56	XC3S1000	α–Am241	12-Apr	7:04:03	12-Apr	13:04:02	200ns	1.14	25°C

Run #	Fluence SEFI (α/cm²)			Number of SEFI			FIT SEFI			Comments
	Chip 1	Chip 2	Chip 3	Chip 1	Chip 2	Chip 3	Chip 1	Chip 2	Chip 3	
1	0.0E+00	0.0E+00	0.0E+00	0	0	0	#	#	#	stability check
24	0.0E+00			131			307	#	#	
25		0.0E+00			112		#	262	#	
26			0.0E+00			119	#	#	279	
34	0.0E+00			112			262	#	#	
35		0.0E+00			97		#	226	#	
36			0.0E+00			96	#	#	320	
44	0.0E+00			111			259	#	#	
45		0.0E+00			98		#	229	#	
46			0.0E+00			107	#	#	250	
54	0.0E+00			104			243	#	#	consistency check
55		0.0E+00			114		#	266	#	consistency check
56			0.0E+00			114	#	#	266	consistency check

Run #	Fluence SEU (α/cm²)			Number of SEU			FIT SEU			Comments
	Chip 1	Chip 2	Chip 3	Chip 1	Chip 2	Chip 3	Chip 1	Chip 2	Chip 3	
1	0.0E+00	0.0E+00	0.0E+00	0	0	0	#	#	#	stability check
24	4.3E+05			307			712	#	#	
25		4.3E+05			335		#	775	#	
26			4.3E+05			629	#	#	1457	
34	4.3E+05			267			618	#	#	
35		4.3E+05			307		#	708	#	
36			3.0E+05			445	#	#	1468	
44	4.3E+05			257			594	#	#	
45		4.3E+05			299		#	690	#	
46			4.3E+05			597	#	#	1380	
54	4.3E+05			280			647	#	#	consistency check
55		4.3E+05			369		#	853	#	consistency check
56			4.3E+05			650	#	#	1503	consistency check

EP1C20

Run #	Device	Particle	Start		Stop		Condition		
			Date	Time	Date	Time	Cycle	VDD	Temp
1	EP1C20	α–Am241	13-Oct	14:53:38	13-Oct	15:04:27	200ns	1.425	25°C
21	EP1C20	α–Am241	13-Oct	16:11:06	13-Oct	22:01:04	200ns	1.425	25°C
22	EP1C20	α–Am241	14-Oct	17:01:12	14-Oct	23:01:10	200ns	1.425	25°C
31	EP1C20	α–Am241	13-Oct	22:04:07	14-Oct	4:04:06	200ns	1.500	25°C
32	EP1C20	α–Am241	14-Oct	23:04:14	15-Oct	5:04:12	200ns	1.500	25°C
41	EP1C20	α–Am241	14-Oct	4:07:08	14-Oct	10:07:07	200ns	1.575	25°C
42	EP1C20	α–Am241	15-Oct	5:07:16	15-Oct	11:07:14	200ns	1.575	25°C
51	EP1C20	α–Am241	14-Oct	10:10:11	14-Oct	16:10:09	200ns	1.425	25°C
52	EP1C20	α–Am241	15-Oct	11:10:18	15-Oct	17:10:15	200ns	1.425	25°C

Run #	Fluence SEFI (α/cm²)		Number of SEFI		FIT SEFI		Comments
	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 2	
1	0.0E+00	0.0E+00	0	0	#	#	stability check
21	4.4E+05		53		121	#	
22		4.5E+05		56	#	124	
31	4.5E+05		38		84	#	
32		4.5E+05		47	#	104	
41	4.5E+05		24		53	#	
42		4.5E+05		31	#	69	
51	4.5E+05		54		120	#	consistency check
52		4.5E+05		56	#	124	consistency check

B 95% confidence intervals

Let x be a single observation from a Poisson distribution with mean μ. Then 95% confidence limits for μ are given by the formula:

(CHIINV(0.975, 2*x))/2, CHIINV(0.025, 2*(x+1))/2)

Where CHIINV returns the inverse of the one-tailed probability of the chi-squared distribution.

	95% limits	
x	Lower limit	Upper limit
0	0.0	3.7
1	0.0	5.6
2	0.2	7.2
3	0.6	8.8
4	1.1	10.2
5	1.6	11.7
6	2.2	13.1
7	2.8	14.4
8	3.5	15.8
9	4.1	17.1
10	4.8	18.4
20	12.2	30.9
50	37.1	65.9
100	81.4	121.6

C Geometry factor calculation for alpha tests

A Geometry factor calculation

In the theoretical case that the dimensions of the radiation source are infinitely large or the source is infinitely close to the detector, the geometry factor equals 1. This implies that the radiation flux at the detector equals the flux emitted from the source and that radiation reaches the detector under all possible angles. Because in practice the source has a finite size and there is a finite distance between the source and the detector, the flux emitted from the source has to be corrected by a *geometry factor* to obtain the effective flux at the detector. In the current appendix we derive from first principles the geometry factor that we need for the alpha flux emitted from a solid source onto a chip surface.

We assume the following:

- the source is rectangular,
- the source area is much larger than the chip area,
- the radiation flux is the same for each point on the chip (which is the detector in this case),
- the alpha-emission is isotropic, i.e., the flux of alpha particles does *not* depend on the emission angle.

The situation of a source placed over a detector point is depicted in Fig. 31. The detector point is situated under the center of the source.

A point on the source surface emits alpha particles isotropically. The amount of radiation N_d detected per unit area at a distance R from the source point equals,

$$N_d = \frac{N_{s,\text{single}}}{2\pi R^2},$$

where N_s denotes the alpha flux per unit area emitted from a single point and the denominator equals the area of a semi-sphere with radius R. The distance between the point on the source surface and the detector point equals,

$$R = \sqrt{h^2 + x^2 + y^2}.$$

The radiation reaches the detector point under an angle θ, therefore the flux has to be multiplied by a factor $\cos\theta = h/R$. The total amount of radiation observed at the detector point then equals,

$$\begin{aligned} N_d &= \int_{-L/2}^{L/2}\int_{-W/2}^{W/2} \frac{N_s}{2\pi R^2}\frac{h}{R}\,dx\,dy \\ &= \frac{N_s h}{2\pi}\int_{-L/2}^{L/2}\int_{-W/2}^{W/2}\left(h^2+x^2+y^2\right)^{-3/2}\,dx\,dy. \end{aligned}$$

Therefore, the geometry factor equals,

$$G_{\text{sq}} = \frac{h}{2\pi} \int_{-L/2}^{L/2} \int_{-W/2}^{W/2} \left(h^2 + x^2 + y^2\right)^{-3/2} dx\, dy. \tag{23}$$

The integral in (23) is difficult to solve analytically, but can be computed numerically with the help of, for example, Mathematica. It can be shown easily that if both $L \to \infty$ and $W \to \infty$ or if $h \to 0$, then $G \to 1$, as it should.

In the case of a *disk-shaped* source with radius ρ, see Fig. 32, substitution of $dx\, dy = r\, dr\, d\phi$ and $r^2 = x^2 + y^2$ gives,

$$\begin{aligned} N_d &= \frac{N_s h}{2\pi} \int_{r=0}^{\rho} \int_{\phi=0}^{2\pi} \left(h^2 + r^2\right)^{-3/2} r\, dr\, d\phi \\ &= N_s h \int_0^{\rho} \left(h^2 + r^2\right)^{-3/2} r\, dr = N_s \left[1 - \frac{h}{\sqrt{h^2 + \rho^2}}\right]. \end{aligned}$$

The geometry factor then equals,

$$G_{\text{disk}} = 1 - \frac{h}{\sqrt{h^2 + \rho^2}}. \tag{24}$$

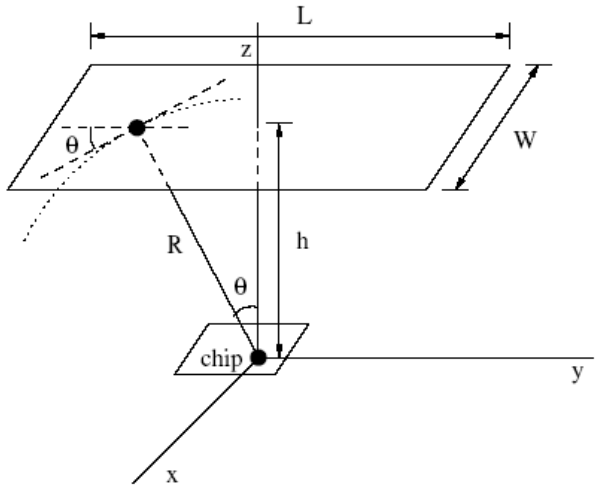


Figure 31: *Source with dimensions $L \times W$ parallel to the xy-plane, at a distance h above the chip.*

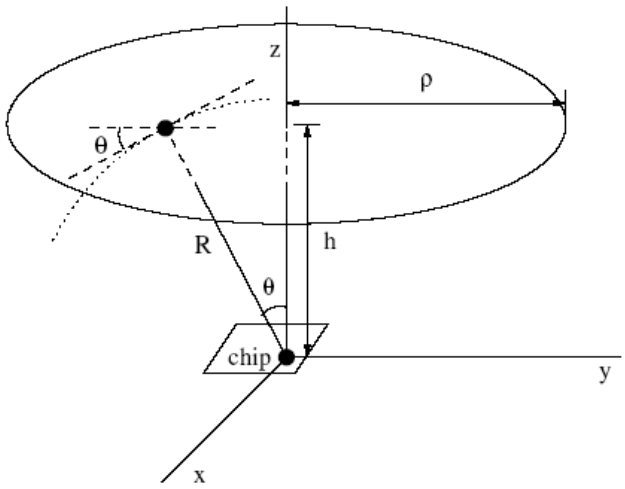
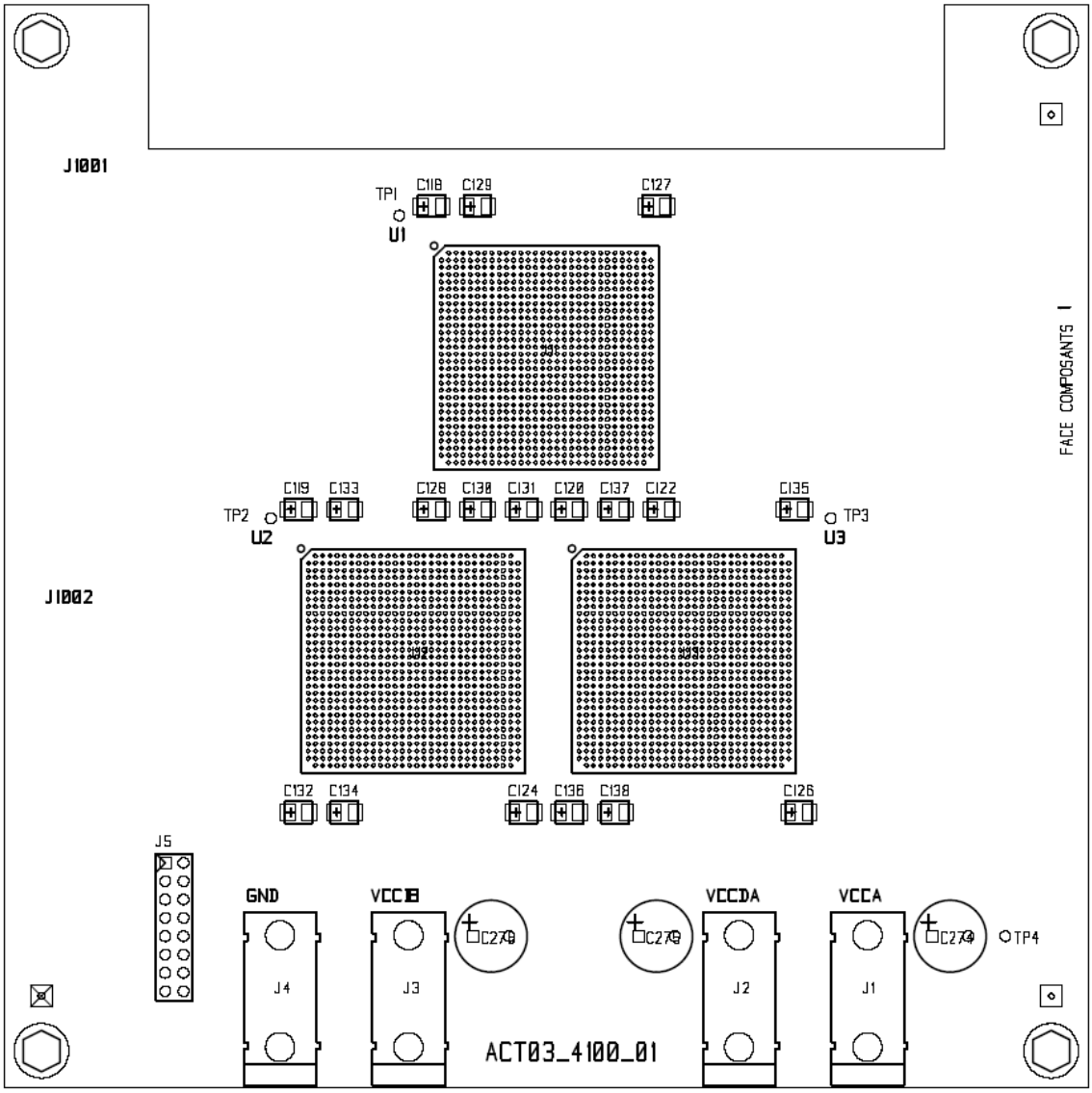


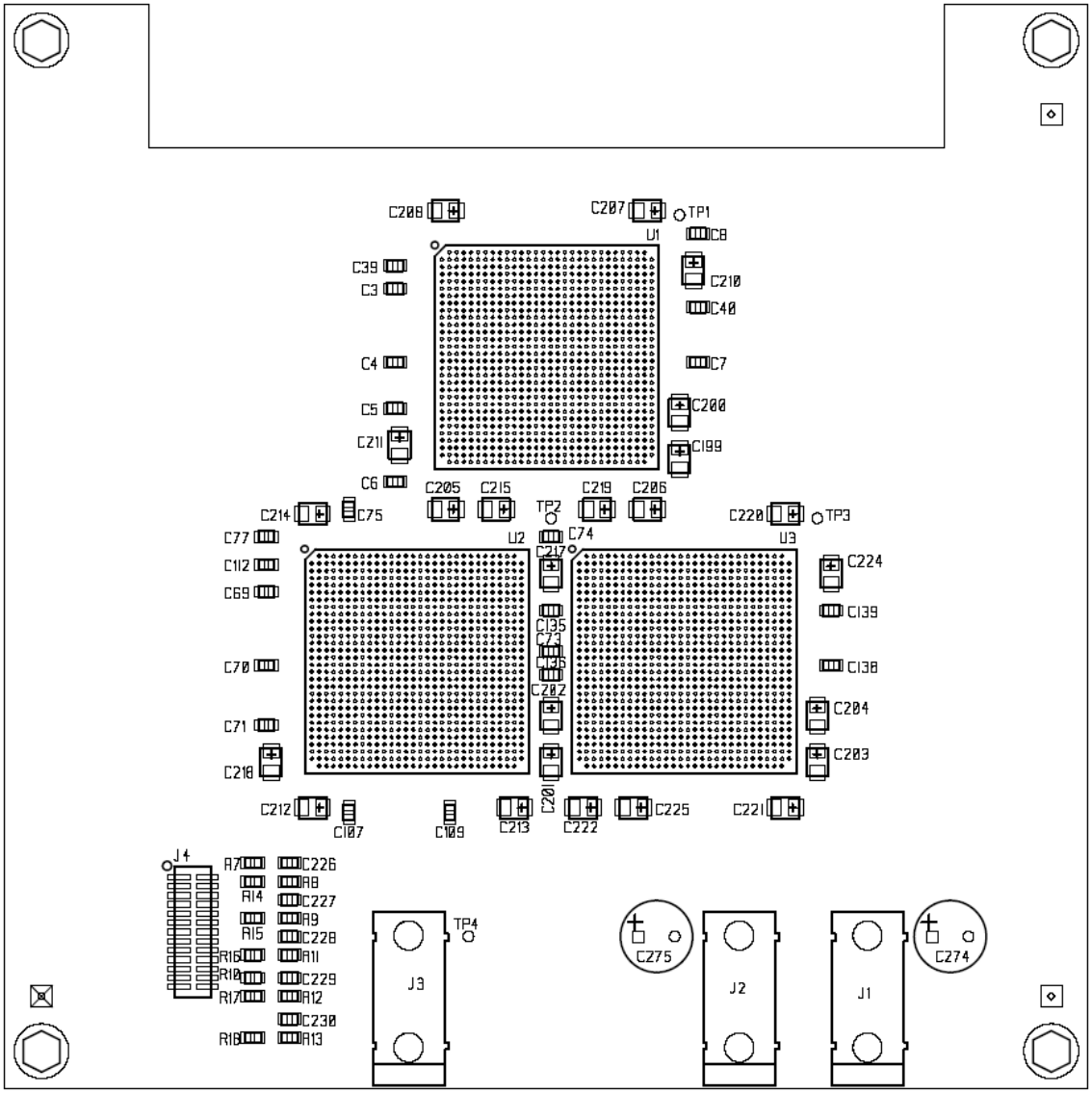
Figure 32: *Disk-shaped source with radius ρ parallel to the xy-plane, at a distance h above the chip.*

D Test board layout

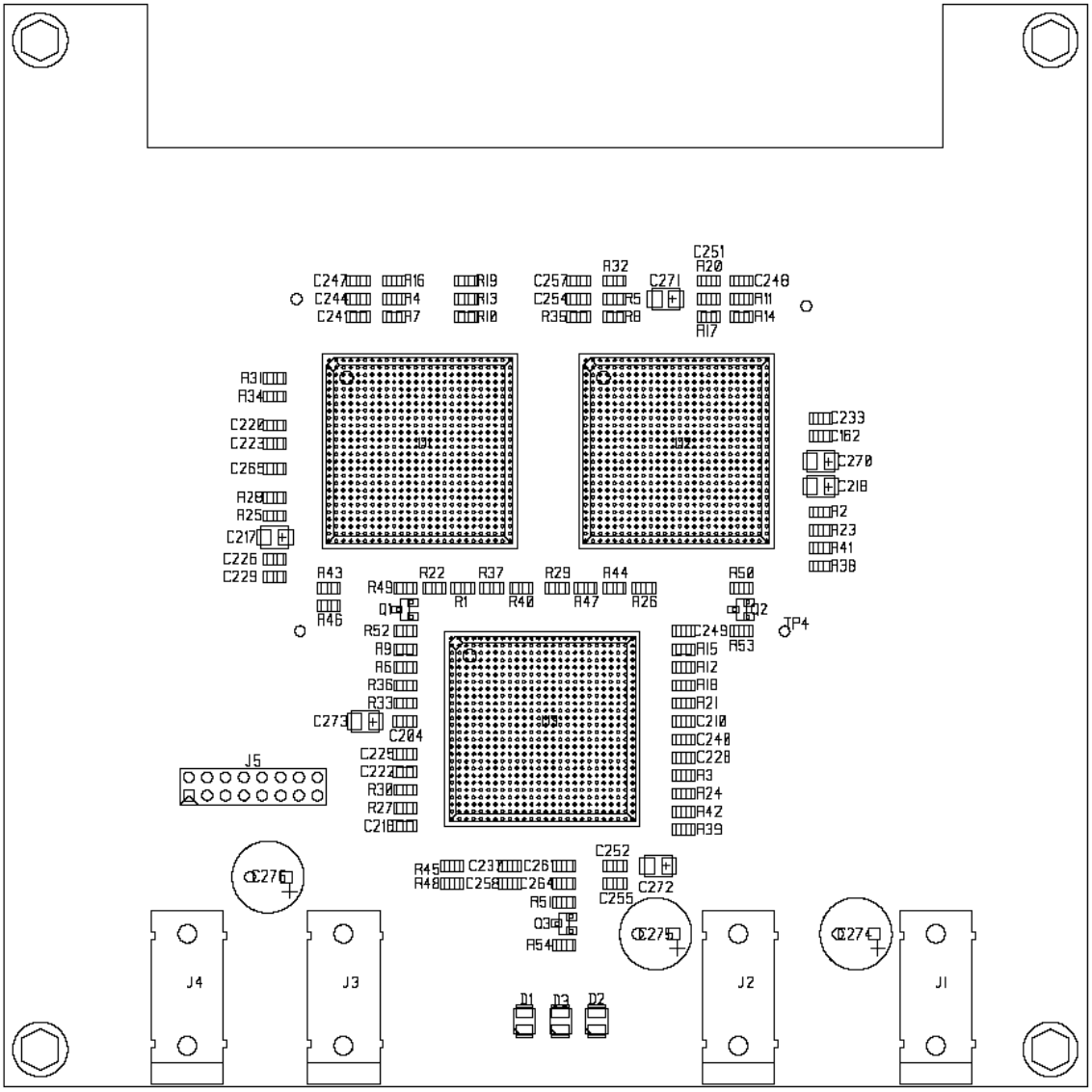
D.1 AX1000



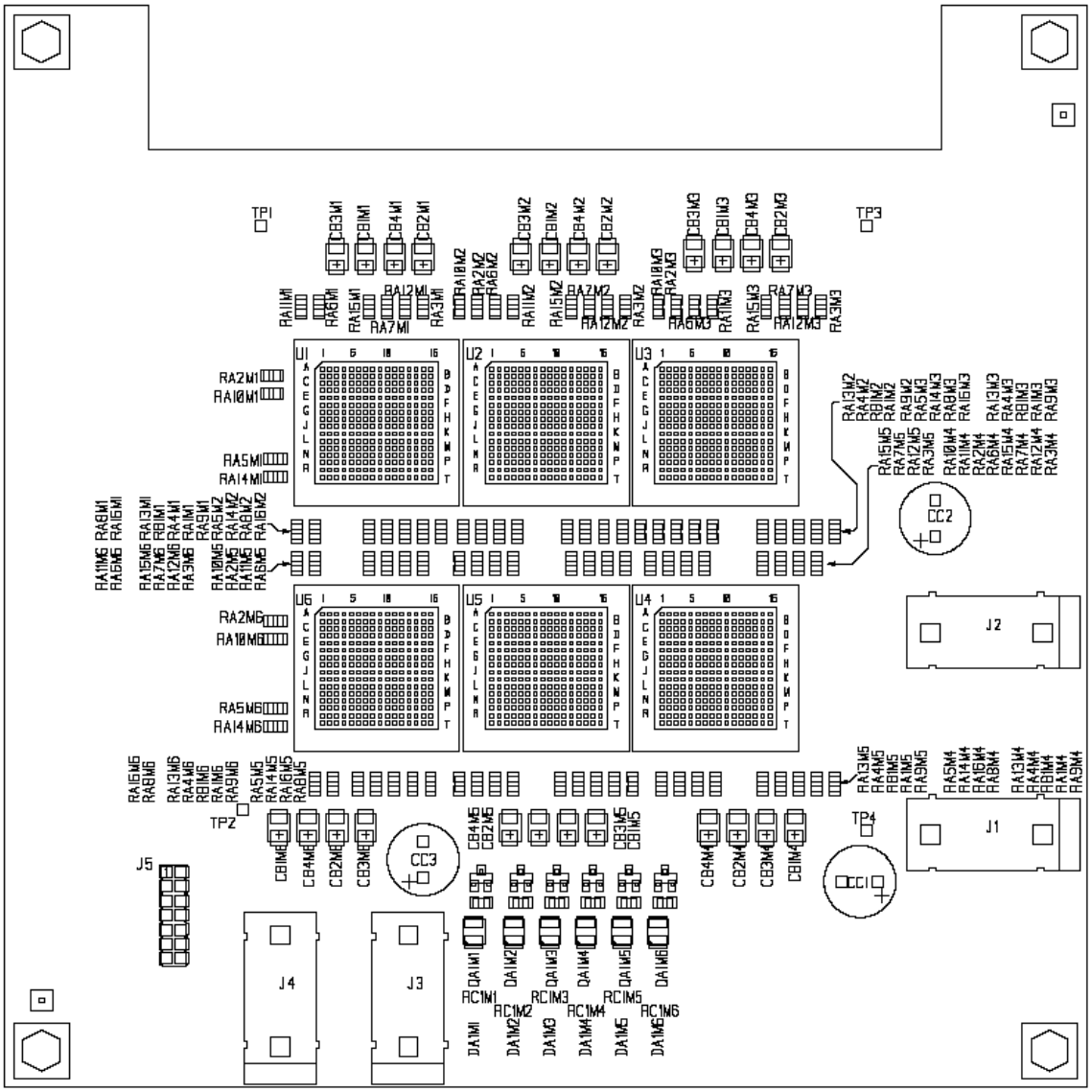
D.2 APA1000



D.3 XC2V3000



D.4 XC3S1000



D.5 EP1C20