

AGLP125 IGL00 PLUS Board

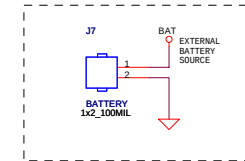
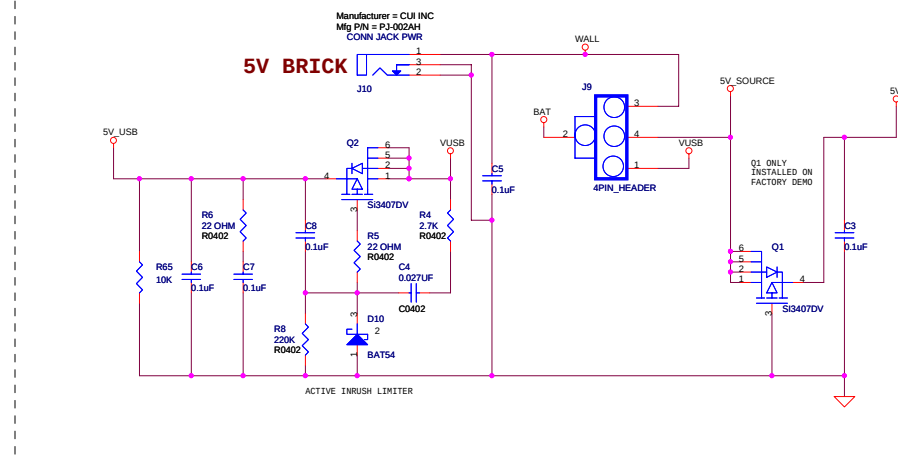
DVP-100-000271-001 RevB

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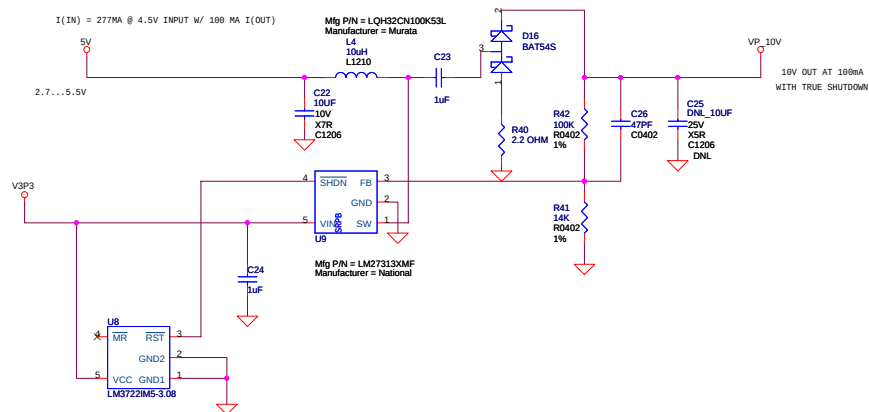
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Title DVP-100-000271-001 Rev B		
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5V SUPPLY

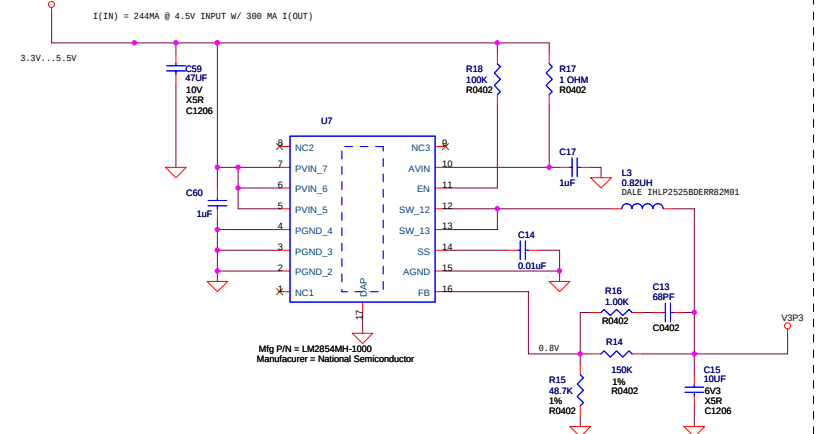
USB ACTIVE IN RUSH LIMITER



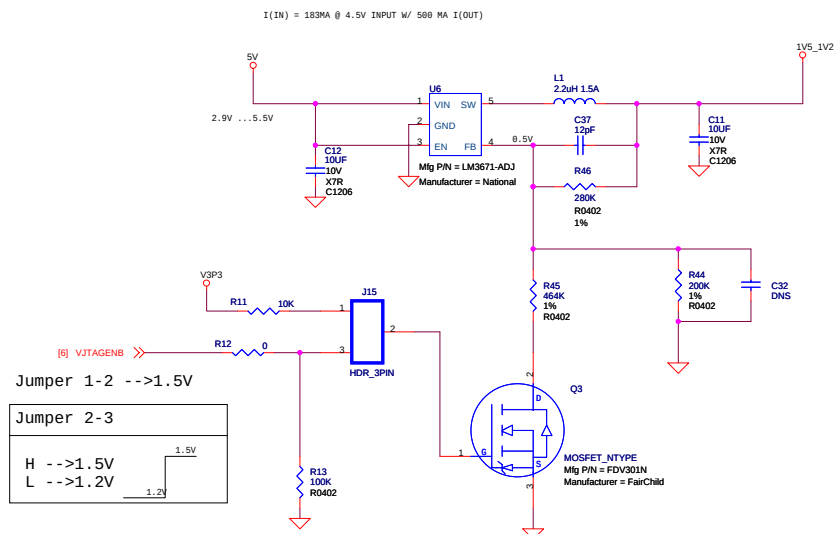
10V SUPPLY WITH TRUE SHUTDOWN



DC IN TO 3.3V AT 4A



National Semiconductor
The Sight & Sound of Information



Jumper 2-3

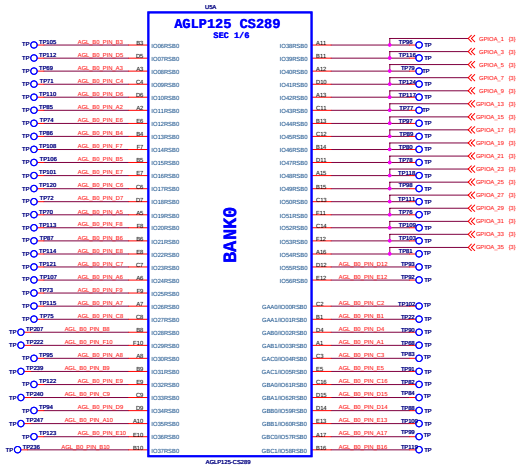
H -->1.5V
L -->1.2V



The diagram shows a signal waveform that starts at a low level (1.2V) and transitions to a high level (1.5V). The transition is labeled with 'H' and 'L' indicating the signal state before and after the jump.

AGLP125 - CSG289

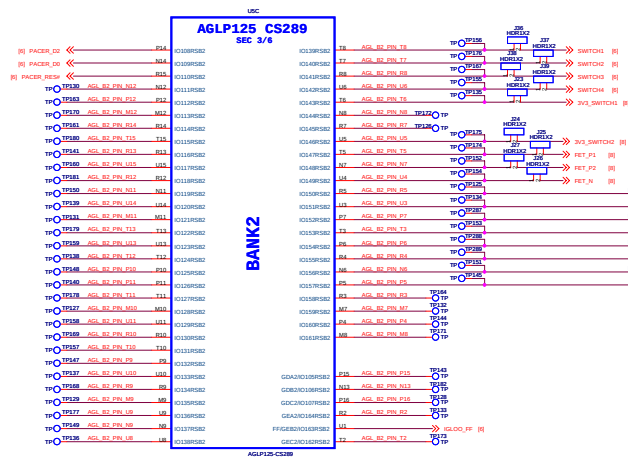
BANK 0 I/O SIGNALS



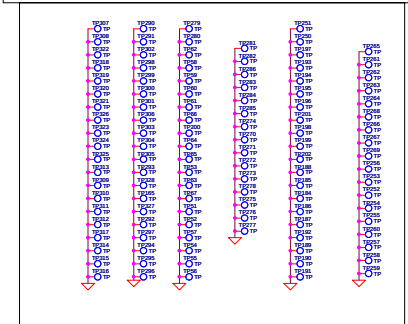
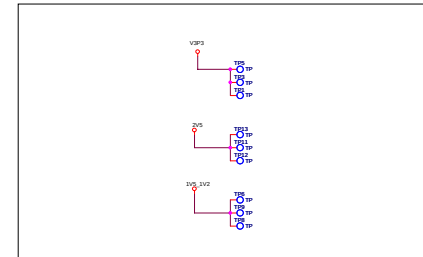
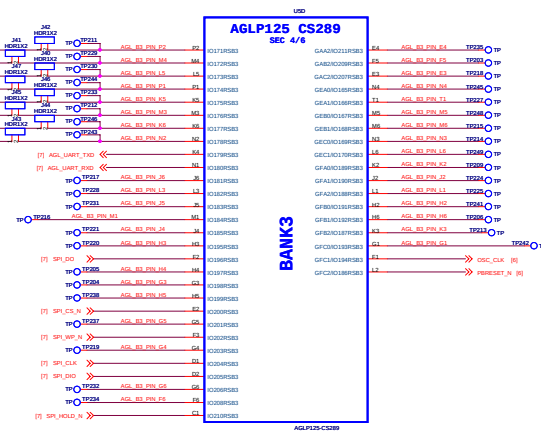
BANK 1 I/O SIGNALS



BANK 2 I/O SIGNALS



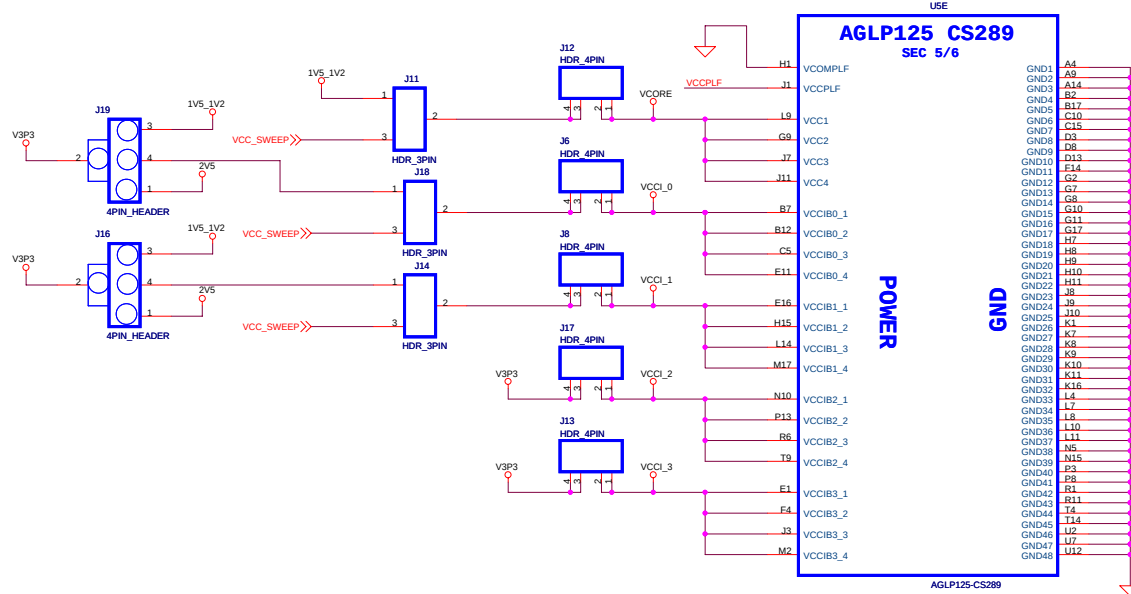
BANK 3 I/O SIGNALS



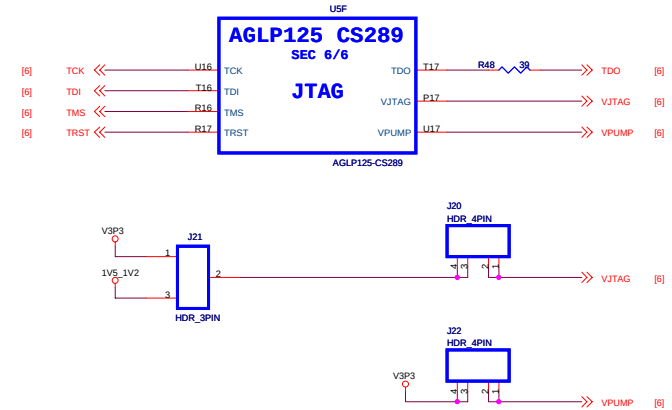
REV: P/W AGLP125-CS289
REV: A0101

AGLP125 - CSG289

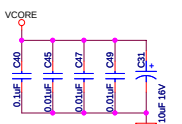
POWER & GND



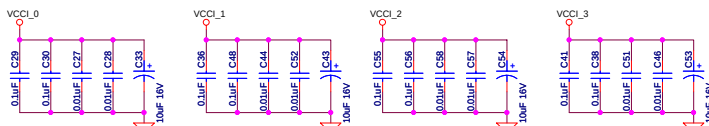
JTAG SIGNALS



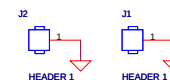
DECAPS FOR VCORE



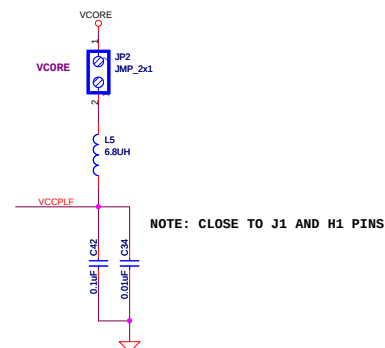
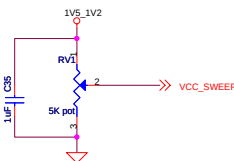
DECAPS FOR I/O BANK0 , BANK1 ,BANK2 & BANK3



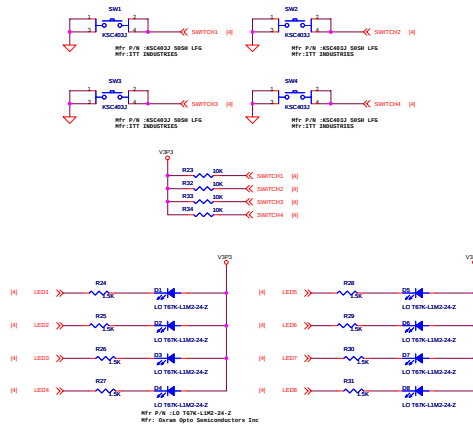
GROUND POST



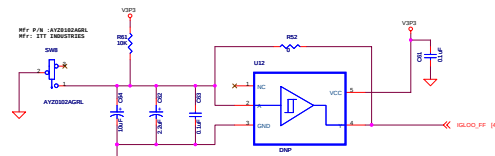
POTENTIOMETER



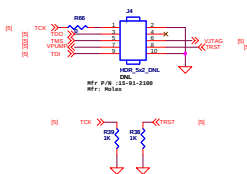
TEST LEDS & TEST SWITCHES



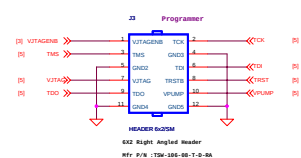
IGL00 FLASH FREEZE (Schmitt Triggered)



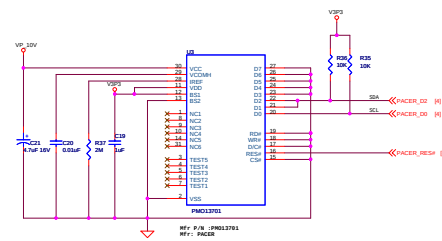
JTAG HEADER



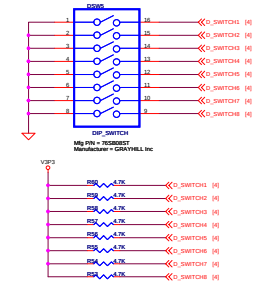
LC_JTAG HEADER



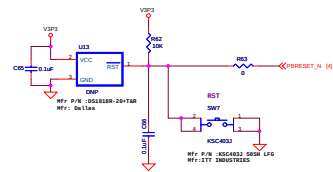
PACER_OLED_DISPLAY



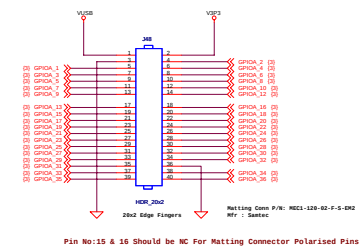
DIP SWITCHES



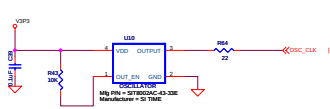
PUSH BUTTON SYSTEM RESET



INTERFACE CONNECTOR

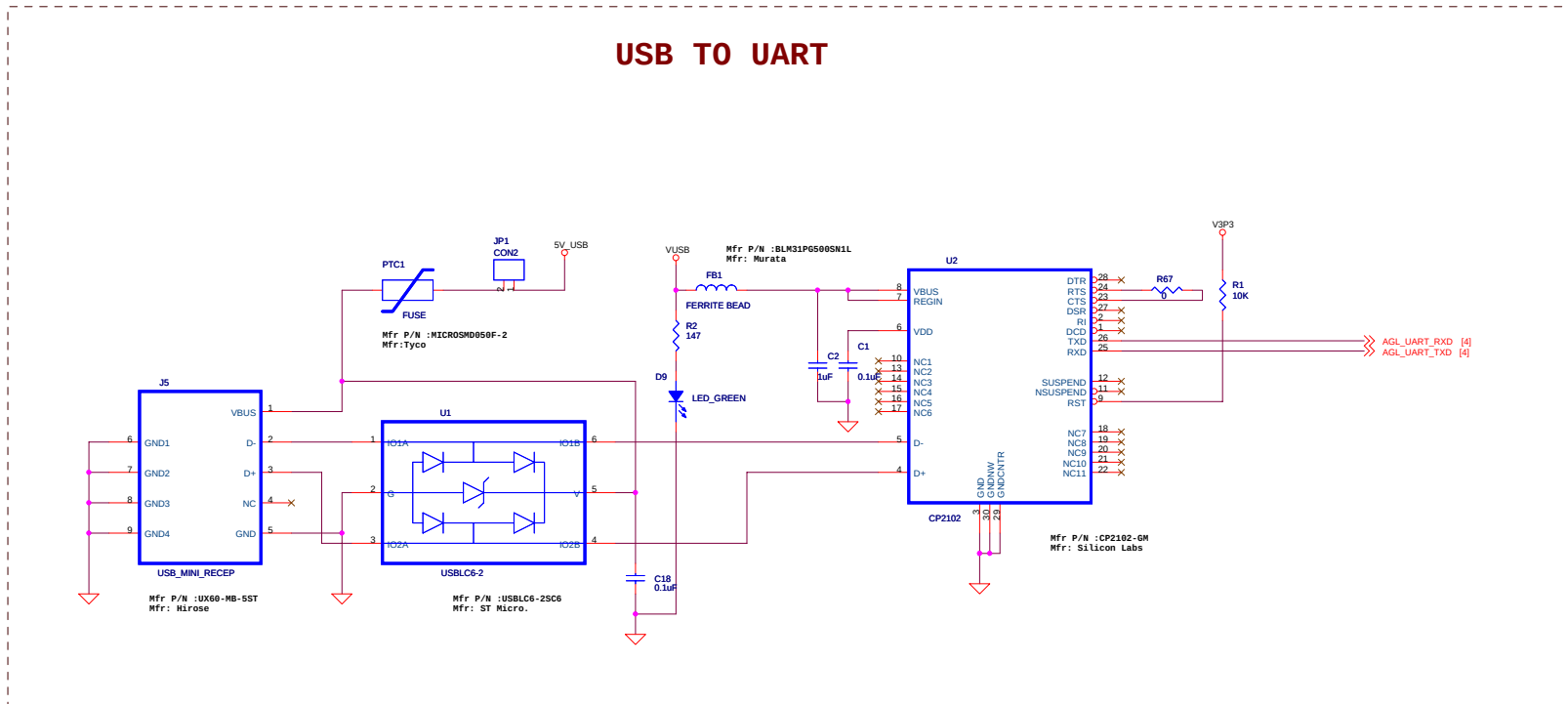


CLK OSCILLATOR CIRCUIT

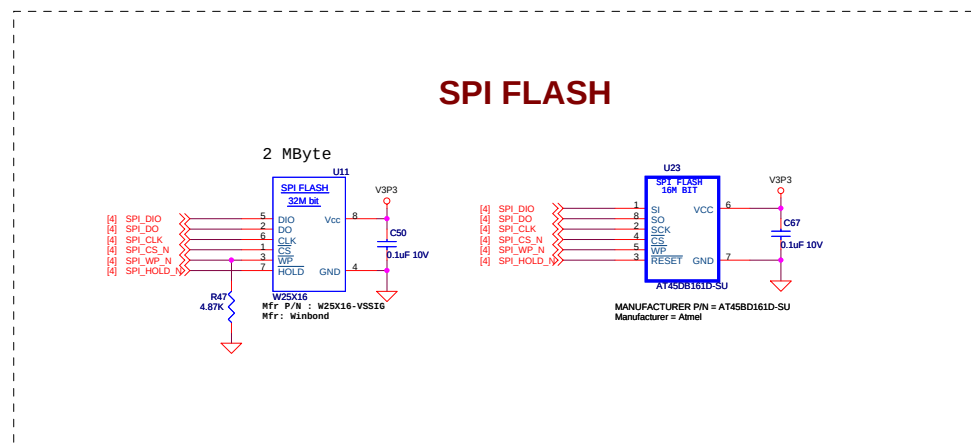


PERIPHERALS

USB TO UART

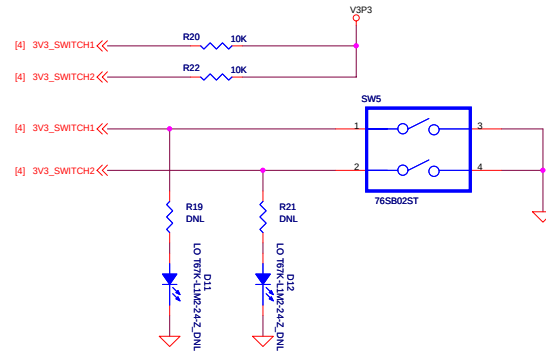


SPI FLASH

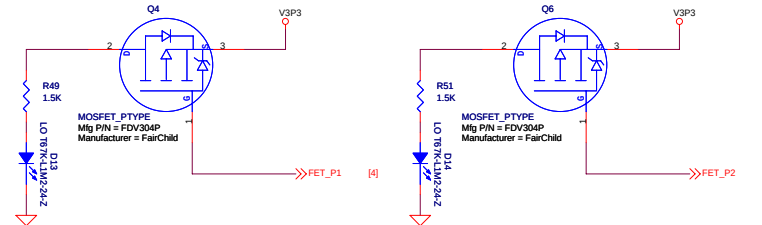


F*F VARIANTS

TWO IO CONTROLLED VIA DIP SWITCH TOGGLING HIGH OR LOW



P TYPE FET



N TYPE FET

