Competitive Programmable Logic Power Comparison

White Paper

April 2008

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Introduction

Today, many applications require low-power programmable logic solutions. For this reason, many programmable logic vendors have focused on minimizing device power consumption. Of these vendors, several claim low-power superiority. However, only one can be the true leader.

In this paper, the power consumption of six competitive programmable logic devices is compared via published vendor datasheets, power-estimation tools, and real silicon measurements. In the end, this paper will prove that Actel's flash-based IGLOO® FPGAs are the undisputed low-power leaders in the industry, regardless of logic density, design configuration, or power mode.

Power Consumption Components

There are five different power components that must be considered when evaluating different FPGA vendors. Figure 1 shows these components.

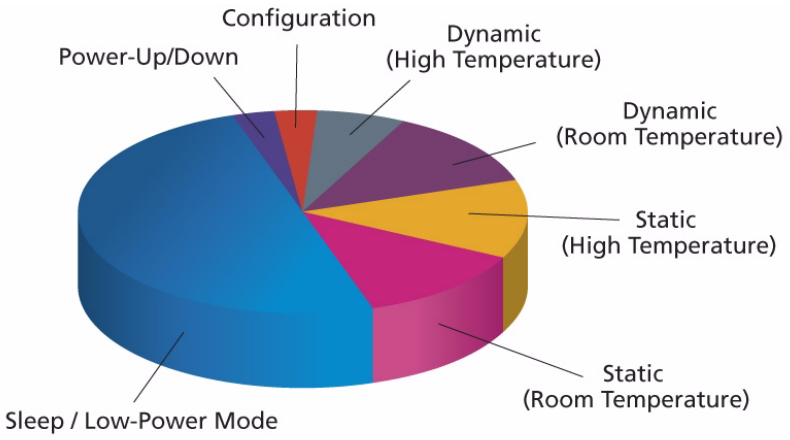


Figure 1: **System Power Profile over Time**

The important power components to consider include the following:

1. Power-up (inrush power)

   Inrush power is the amount of power drawn by the device during power-up.
2. Configuration power

   Configuration power is the amount of power required during the loading of the FPGA upon power-up (specific to SRAM-based programmable logic devices).
3. Static (standby) power

   Static power is the amount of power the device consumes when it is powered-up but not actively performing any operation (i.e., the device is not clocked).
4. Dynamic (active) power

   Dynamic power is the amount of power the device consumes when it is actively operating (i.e., the device is clocked).
5. Sleep power (low-power mode)

   Some FPGA devices offer low-power or sleep modes. In some cases, this may be different from static power.

Power Analysis Overview

For this paper, static power and dynamic power were evaluated using devices from different programmable logic vendors. For many battery-powered applications, the device may reside in static mode a large percentage of the time. Handheld devices, for example, are in static mode when not being used. Static power contributes to battery drain and determines how long the device can be powered. For this reason, evaluating static power was our primary concern.

Dynamic power was also evaluated on devices from different vendors over multiple frequencies. To simplify our comparison across vendors, we focused on FPGA core power, the main contributor to programmable logic devices (PLD) power consumption. Power contributions from I/Os were not evaluated for power comparison. In addition, this study did not analyze inrush or configuration power across vendors. Unlike SRAM-based FPGAs, flash-based FPGAs do not suffer the additional power spikes due to inrush power or configuration power. For more information regarding power, inrush, and configuration, refer to Actel's *Total System Power* brochure.

We gathered from the following three sources to evaluate competitive device and design power consumption:

1. Vendor's datasheet
2. Vendor's power-estimation tools
3. Silicon measurements (taken on Actel-created power comparison board)

Power Comparison Board

Today, programmable logic vendors offer evaluation and development boards for their silicon products. Some boards offer mechanisms to measure and evaluate power consumption. However, boards from each vendor are designed differently with different configurations. To fairly evaluate power consumption between different vendors using actual silicon, we developed a power comparison board. This board was designed so that two devices could be compared against each other, side-by-side, under the same operating conditions.

The baseboard, shown in Figure 2 on page 5, consists of two sockets with a simple interface that will allow daughtercards (Figure 3 on page 5) to be plugged into the baseboard for power analysis. The baseboard has different power rails that can be selected for each socket. This enables two devices with different power rails to be compared side-by-side. In addition, the baseboard has a socket for different crystal oscillators that can be interchanged to modify the frequency of the digital clock.

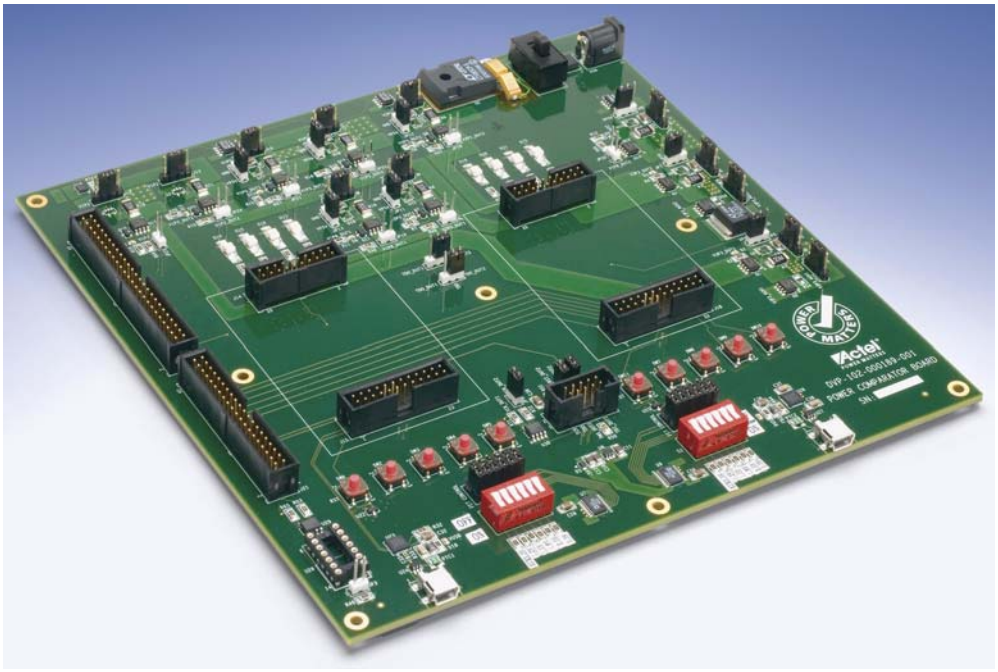


Figure 2: **Power Comparison Baseboard**

Figure 3: **Example of Daughtercards – Actel IGLOO Daughtercard and Xilinx® CoolRunner™-II Daughtercard**

The daughtercards were designed specifically for the FPGA or CPLD being evaluated. Power, clock, and I/O pins were routed from the socket to the specific power, clock, and I/O pins on the device being evaluated. Figure 4 shows the daughtercards plugged into the baseboard.

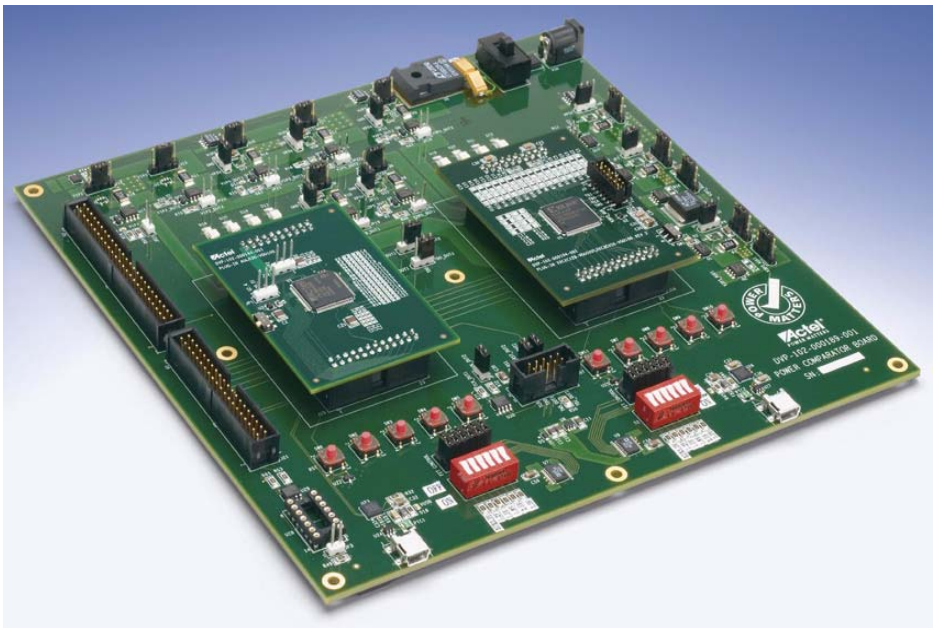


Figure 4: **Daughtercards Plugged into Baseboard**

Devices Analyzed

For this paper, devices were grouped into two different logic densities: small density devices, which consist of approximately 30 k system gates (approximately 256 macrocells or 300 equivalent logic elements) and large density devices, which consist of approximately 600 k system gates (approximately 6,000 equivalent logic elements). Note that identifying a logic density that is similar between vendors is challenging. As a result, the 30 k and 600 k gate logic density devices were chosen because most programmable logic vendors support these densities.

Table 1 lists the smaller density devices that were used in the power comparison.

Table 1: **Small Density Devices (~ 30 k system gates)**

Vendor	Device Family	Part Number
Actel Corporation	IGLOO FPGA	AGL030
Altera® Corporation	MAX® IIZ CPLD	EPM240Z
Xilinx, Inc.	CoolRunner-II CPLD	XC2C256

Table 2 lists the larger density devices that were used in the power comparison.

Table 2: **Large Density FPGA Devices (~ 600 k system gates)**

Vendor	Device Family	Part Number
Actel Corporation	IGLOO FPGA	AGL600
Altera Corporation	Cyclone® III FPGA	EP3C5
Xilinx, Inc.	Spartan™-3AN FPGA	XC3S400AN

Power Analysis

Static Power Analysis

Comparing static power consumption between different programmable logic devices is straightforward, since all vendors publish typical static or standby current numbers in their datasheets. To calculate the static power, we multiplied the static current numbers by the supply voltage.

Static Power Analysis Using Small Densities (~ 30 k gates)

The first set of devices analyzed were the Actel IGLOO AGL030 FPGA, the Altera MAX IIZ EPM240Z CPLD, and the Xilinx CoolRunner-II XC2C256 CPLD. Table 3 summarizes the static/standby current numbers taken from each vendor's datasheet with the calculated static power for each device.

Table 3: **Static Power Using Small Density Devices – Datasheet Values**

Vendor	Device Family	Part Number	Static/Standby Current	Supply Voltage	Static Power
Actel Corporation	IGLOO FPGA	AGL030	4 µA [1]	1.2 V	4.8 µW
Altera Corporation	MAX IIZ CPLD	EPM240Z	29 µA [2]	1.8 V	52.2 µW
Xilinx, Inc.	CoolRunner-II CPLD	XC2C256	33 µA [3]	1.8 V	59.4 µW

Notes:

1. *I_{DD} (quiescent supply current in IGLOO Flash*Freeze mode) from the DC and Switching Characteristics section of the IGLOO Low-Power Flash FPGAs datasheet (Advanced v0.1). I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, V_{JTAG}, V_{CCPLL}, and VMV.*
2. *$I_{CCSTANDBY}$ (V_{CCINT} supply current—standby) from the DC and Switching Characteristics section of the MAX II Device Family datasheet (MII51005-2.1)*
3. *I_{CCSB} (standby current commercial) from the DC Electrical Characteristics section of the XC2C256 CoolRunner-II Product Specification (DS094 v3.2)*

We used the power comparison board and off-the-shelf devices from these vendors to measure and compare the static power. Table 4 lists the static measurements taken on the small density devices. Static power is calculated as the product of supply voltage and the static current measured on each device.

Table 4: **Static Power Using Small Density Devices – Measured Values**

Vendor	Device Family	Part Number	Static/Standby Current	Supply Voltage	Static Power
Actel Corporation	IGLOO FPGA	AGL030	2.1 µA	1.2 V	2.5 µW
Actel Corporation	IGLOO FPGA	AGL030	1.7 µA*	1.2 V	2.0 µW
Altera Corporation	MAX IIZ CPLD	EPM240Z	24.5 µA	1.8 V	44.1 µW
Xilinx, Inc.	CoolRunner-II CPLD	XC2C256	20.3 µA	1.8 V	36.5 µW

Note: **In Flash*Freeze mode*

Static Power Summary – Small Density Devices

The static or standby power information from each vendor's datasheet shows that Actel's IGLOO FPGA consumes less than 5 µW, whereas the Altera MAX IIZ and Xilinx CoolRunner-II devices consume more than 10 times that amount (52.5 µW and 59.4 µW, respectively). Also, when measuring an off-the-shelf device from each vendor on the power comparison board, Actel confirmed the IGLOO tenfold power advantage. The measured static power for the AGL030 device was 2.5 µW (2.0 µW in Flash*Freeze mode), whereas the EPM240Z device consumed 44.1 µW and the XC2C256 consumed 36.5 µW. Figure 5 summarizes the results of the static power comparison for CPLD density devices.

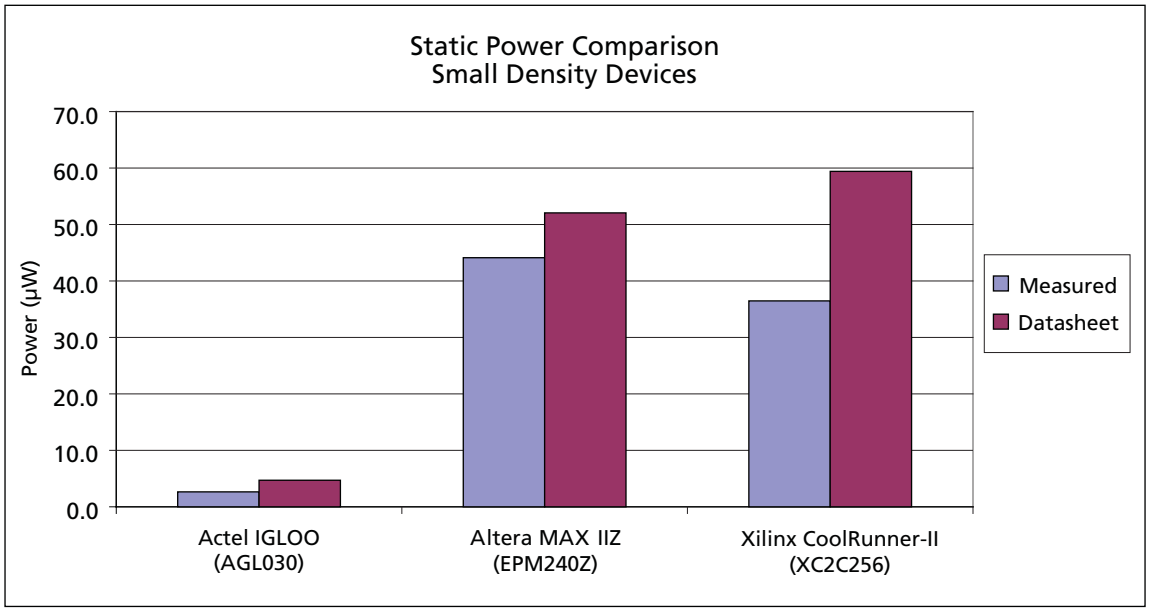


Figure 5: **Static Power Summary – Small Density Devices (measured versus datasheet)**

Static Power Analysis Using Large Density Devices (~ 600 k gates)

The second set of devices analyzed were the Actel IGLOO AGL600 FPGA, the Altera Cyclone III EP3C5 FPGA, and the Xilinx Spartan-3AN XC3S400AN FPGA. Static power calculation is not as straightforward for these devices as it was for the small density devices. For the Altera Cyclone III EP3C5 and the Xilinx Spartan-3AN XC3S400AN SRAM-based FPGAs, in addition to the static power consumed by the core, power from other auxiliary voltage supplies must also be added to the core static power to calculate the total static power of the device. These auxiliary power supplies are required for the SRAM-based FPGAs during operation. Table 5 summarizes the static current numbers taken from each vendor's datasheet and the calculated static power for each device.

Table 5: **Static Power Using Large Density FPGA Devices – Datasheet Values**

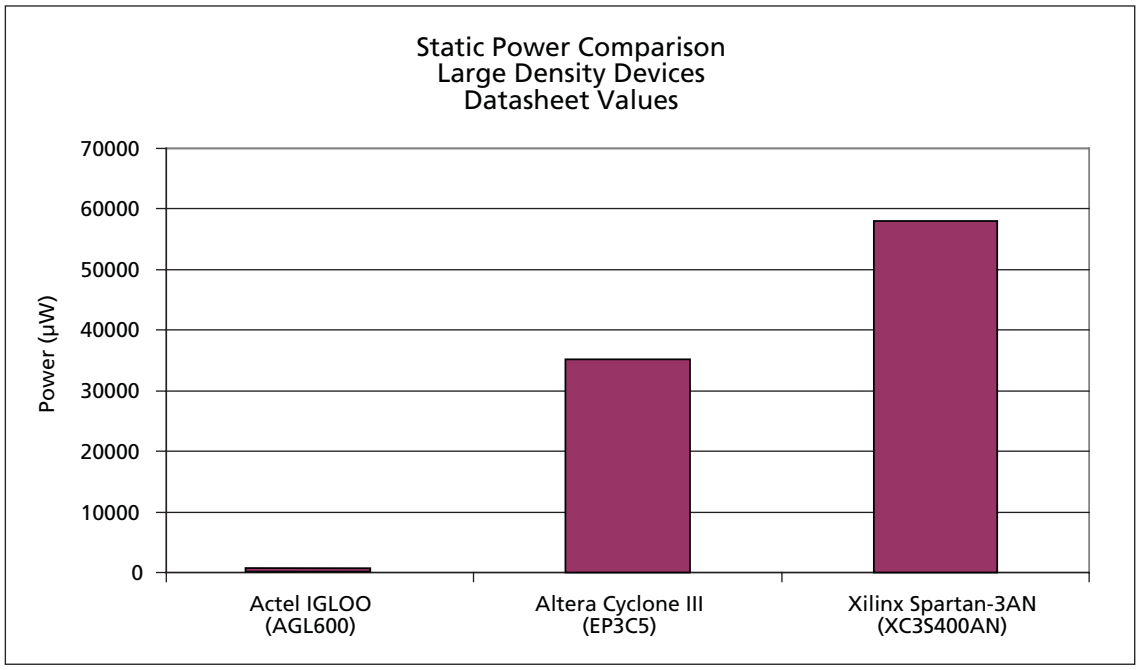
Vendor	**Actel Corporation**		**Altera Corporation**		**Xilinx, Inc.**	
Device Family	IGLOO FPGA		Cyclone III FPGA		Spartan-3AN FPGA	
Part Number	AGL600		EP3C5		XC3S400AN	
Core Static Power	28 µA at 1.2 V [1]	33.6 µW	1,700 µA at 1.2 V [2]	2,040 µW	15,000 µA at 1.2 V [5]	18,000 µW
Auxiliary Static Power	None		11,300 µA at 2.5 V [3]	28,250 µW	12,100 µA at 3.3 V [6]	39,930 µW
PLL Static Power	None		4,100 µA at 1.2 V [4]	4,920 µW	None	
Total Static Power	33.6 µW		35,210 µW		57,930 µW	

Notes:

1. *I_{DD} (quiescent supply current) from the IGLOO DC and Switching Characteristics section of the IGLOO Low-Power Flash FPGAs datasheet (Advanced v0.1).*
2. *I_{CCINT} (V_{CCINT} supply current—standby) from the DC and Switching Characteristics section of the Cyclone III Device Datasheet (CIII52001-1.5). V_{CCINT} —supply voltage for internal logic and input buffers.*
3. *I_{CCA} (V_{CCA} supply current—standby) from the DC and Switching Characteristics section of the Cyclone III Device datasheet (CIII52001-1.5). V_{CCA}—supply (analog) voltage for PLL regulator. All V_{CCA} pins must powered to 2.5 V (even when PLLs are not used).*
4. *I_{CCD_PLL} (V_{CCD_PLL} supply current—standby) from the DC and Switching Characteristics section of the Cyclone III Device datasheet (CIII52001-1.5). V_{CCD_PLL}—supply (digital) voltage for PLL regulator. V_{CCD_PLL} must be connected to V_{CCINT} during operation.*
5. *I_{CCINTQ} (quiescent V_{CCINT} supply current) from the DC and Switching Characteristics section of the Spartan3-AN FPGA Family datasheet (DS557-3 (v3.0)). V_{CCINT}—internal supply voltage.*
6. *I_{CCAUXQ} (quiescent V_{CCAUX} supply current) from the DC and Switching Characteristics section of the Spartan3-AN FPGA Family datasheet (DS557-3 (v3.0)). V_{CCAUX}—auxiliary supply voltage.*

Static Power Summary – Large Density Devices

All the supply voltages contributing to static power must be captured when comparing the different FPGA devices. For Altera Cyclone III devices, static power from V_{CCINT}, V_{CCA}, and V_{CCD_PLL} power supplies must be added together to calculate the total static power of the device. Similarly, for Xilinx Spartan-3AN devices, static power from V_{CCINTQ} and V_{CCAUXQ} power supplies must be added together to calculate total static power. In the comparison study, the Altera EP3C5 device consumed over 1,000 times more static power than the Actel IGLOO AGL600 device. The Xilinx XC3S400AN device consumed over 1,700 times more standby power than the Actel IGLOO AGL600 device. Figure 6 summarizes the results of the static power comparison for large density devices.



Note: *Actel's IGLOO AGL600 device static power consumption is 33.6 µW.*

Figure 6: **Static Power Summary – Large Density Devices (datasheet)**

Static Power over Temperature

Table 6 captures the static current and respective calculated static power over temperature values for small density devices, using the information from vendor datasheets and/or power estimator tools. Table 7 on page 12 lists the calculated static power over temperature values for large density devices. Figure 7 and Figure 8 on page 12 are graphical representations of the data from Table 6 and Table 7 on page 12, respectively.

Table 6: **Static Power Using Small Density Devices over Temperature—Source: Vendor Datasheets, Power Estimator Tools**

Device	Temperature at 25ºC (ambient)		Temperature at 70ºC (ambient)	
	Current (µA)	Power (µW)	Current (µA)	Power (µW)
Actel IGLOO AGL030[1]	4	4.8	7	8.4
Altera MAX IIZ EPM240Z[2]	29	52.2	150	270
Xilinx CoolRunner-II XC2C256[3]	33	59.4	150	270

Notes:

1. *Data came from the* IGLOO Power Calculator*.*
2. *Data came from DC and Switching Characteristics section of the* MAX II Device Family Datasheet *(MII51005-2.1).*
3. *Data came from DC and Switching Characteristics section of the DC Electrical Characteristics section of the* XC2C256 CoolRunner-II Product Specification *(DS094 v3.2).*

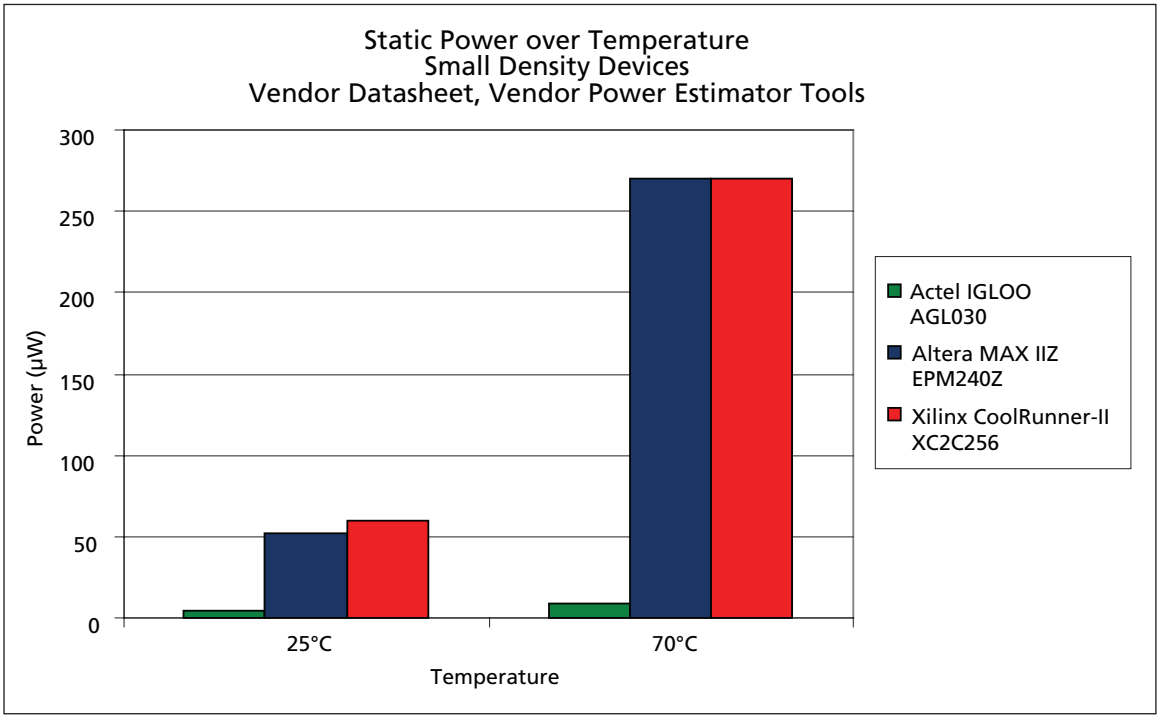


Figure 7: **Static Power over Temperature – Small Density Devices**

Table 7: **Static Power Using Large Density Devices—Source: Power Estimator Tools**

Device	Temperature – 25ºC (ambient) Power (µW)	Temperature – 70ºC (ambient) Power (µW)	Temperature – 85ºC (ambient) Power (µW)
Actel IGLOO AGL600[1]	33.6	60	101
Altera Cyclone III EP3C5[2]	35,210	42,000	45,600
Xilinx Spartan-3AN XC3S400AN[3]	57,930	91,000	107,000

Notes:

1. *Data derived from the* IGLOO Power Calculator*.*
2. *Data derived from Cyclone III using Altera PowerPlay Early Power Estimator v7.2 SP1.*
3. *Data derived from Spartan-3 using Xilinx Xpower™ Estimator (XPE) 9.1.03.*

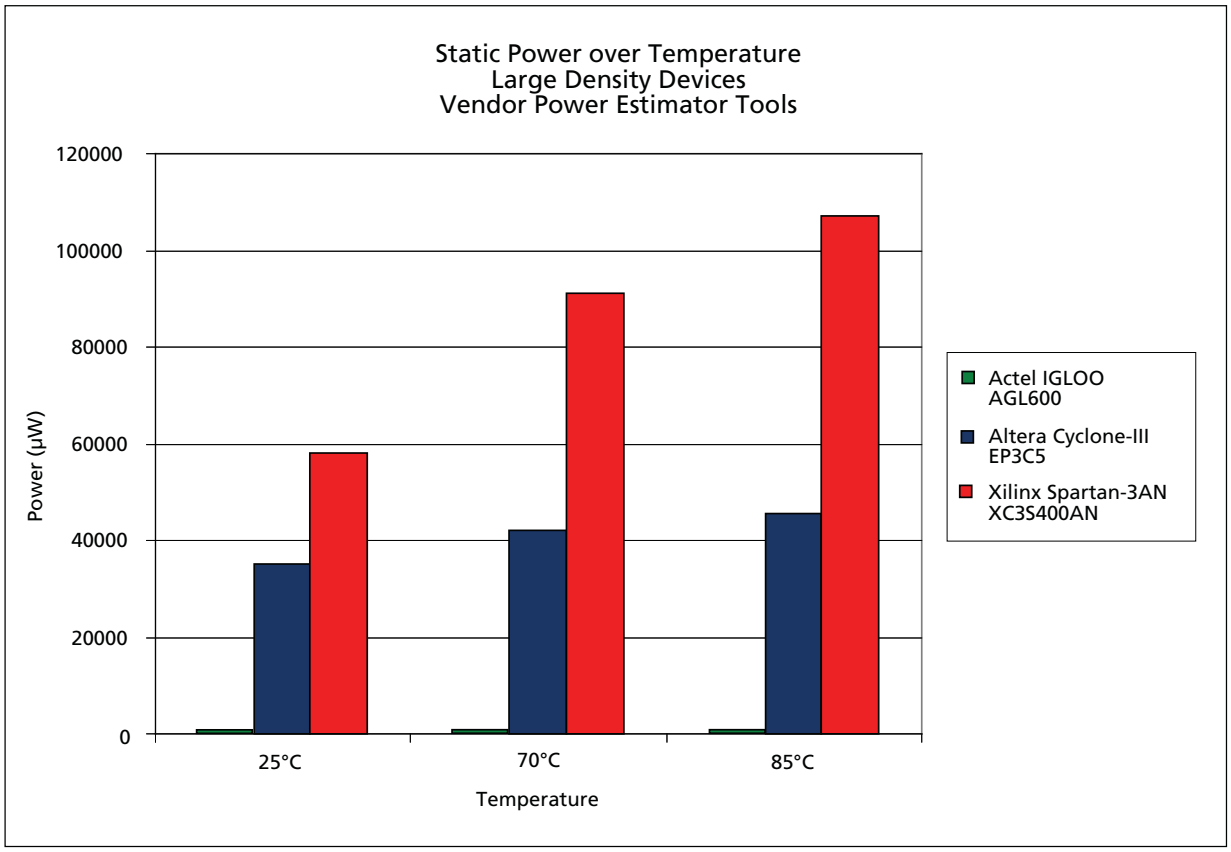


Figure 8: **Static Power over Temperature – FPGA Density Devices**

Static Power over Temperature – Summary

After analyzing the static power information from either vendor datasheets or vendor power estimator tools, it is evident that Actel IGLOO FPGAs are orders of magnitude better than the competition.

- For small density devices, Actel IGLOO FPGAs consume over 30 times lower power at 70°C compared to Xilinx and Altera CPLDs.
- For large density devices, Actel IGLOO FPGAs consume as much as 1,000 times lower static power than Cyclone III and Spartan-3AN FPGAs.

Dynamic Power

Dynamic or active power is the amount of power consumed when the device is operating. Many vendors offer power estimators or calculator tools that enable engineers to estimate the amount of power consumed by the device during operation. For comparison purposes, we will use results taken from vendor power estimation tools. For the small density devices, we will also measure the power using silicon.

Dynamic Power Comparison Designs

Dynamic power consumption is dependent on the design programmed into the programmable logic device. To compare one programmable logic device against another, the same design was used. The design chosen consists of an 8-bit gray-code counter that was instantiated several times to fill the device. The gray-code counter design was chosen because it uses a ratio of combinatorial and sequential logic that is typical of many designs. For this design, the proportion of registers to combinatorial logic is approximately 50%. Figure 9 shows a graphical representation of the 8-bit gray-code counter design.

When comparing devices against each other, the 8-bit gray-code counter was instantiated as many times as possible into the smaller of the two devices being compared. That design was then used in both devices to compare results.

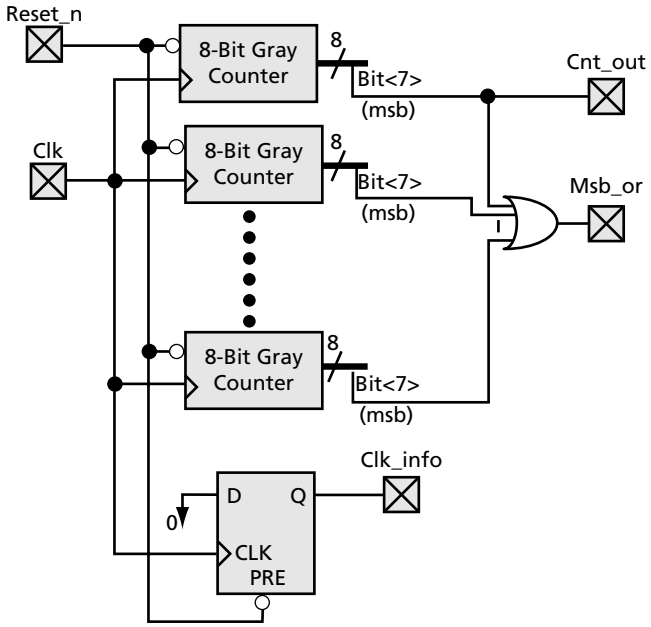


Figure 9: **8-Bit Gray-Code Counter Design**

Actel IGLOO (AGL030) FPGA versus Altera MAX IIZ (EPM240Z) CPLD

The device closest in density to the Actel IGLOO AGL030 is the Altera MAX IIZ EPM240Z device. Since the EPM240Z is the smaller of the two devices, the 8-bit gray-code counter was instantiated 14 times to utilize 95% of the EPM240Z. Taking that same design (14 instantiations of the gray-code counter) and programming it into the Actel IGLOO device, the design consumed 61% of the AGL030.

Actel IGLOO (AGL030) FPGA versus Xilinx CoolRunner-II (XC2C256) CPLD

The Actel IGLOO AGL030 device was also compared against the Xilinx CoolRunner-II XC2C256 device. The 8-bit gray-code counter was instantiated 22 times into both the XC2C256 and AGL030 devices. The design occupied 87% of the XC2C256 and 99% of the AGL030.

Actel IGLOO (AGL600) FPGA versus Altera Cyclone III (EP3C5) FPGA

Comparing the Actel IGLOO AGL600 device against the Altera Cyclone III EP3C5 device, the EP3C5 was the smaller of the two devices, and the 8-bit gray-code counter was instantiated 290 times and utilized 98% of the EP3C5. Programming the same design into the Actel IGLOO device, the design consumed 71% of the AGL600.

Actel IGLOO (AGL600) FPGA versus Xilinx Spartan-3AN (XC3S400AN) FPGA

Comparing the Actel IGLOO AGL600 device against the Xilinx Spartan-3AN XC3S400AN device, the gray-code counter design was instantiated 390 times and utilized 93% of the XC3S400AN and 98% of the AGL600.

Table 8 summarizes the device utilization of the different designs for both small and large density devices.

Table 8: **Design Information for Dynamic Power Comparison**

Vendor	Device	Number of 8-Bit Gray-Code Counters	Percent Utilization
Actel Corporation	IGLOO AGL030	14, 22	61%, 99%
Altera Corporation	MAX IIZ EPM240Z	14	95%
Xilinx, Inc.	CoolRunner-II XC2C256	22	87%
Actel Corporation	IGLOO AGL600	290, 390	71%, 98%
Altera Corporation	Cyclone III EP3C5	290	98%
Xilinx, Inc.	Spartan-3AN XC3S400AN	390	93%

Dynamic Power Calculated Using Vendor Tools

Most FPGA vendors have a power calculator or estimator tools that can be used to find a preliminary estimate of power consumed by the device. These estimator tools allow users to enter key parameters for their design, including number of flip-flops in the design, number of combinatorial logic cells, clocks, and toggle rates. Note that these estimator tools are pre-synthesis tools that are used primarily for power consumption approximation. These tools are not as accurate as timing-driven estimation tools, which provide a more precise power consumption estimation. Table 9 lists power estimator tools from different vendors that were used for dynamic power analysis. Using each vendor's tools, we calculated the power consumed by the design under nominal voltage and temperature conditions.

Table 9: **Power Estimator Tools by Vendor**

Vendor	Device Family	Power Estimator Tool	Version
Actel Corporation	IGLOO	IGLOO Power Calculator	v3d (Advanced)
Altera Corporation	MAX IIZ	PowerPlay Early Power Estimator	v7.2 SP1
Altera Corporation	Cyclone III	PowerPlay Early Power Estimator	v7.2 SP1
Xilinx, Inc.	CoolRunner-II	None	None
Xilinx, Inc.	Spartan-3AN	Xpower Estimator	9.1.03

Note: *Xilinx does not offer a power estimator tool for the CoolRunner-II family of devices.*

Dynamic Power – Actel IGLOO versus Altera MAX IIZ

Table 10 lists the current and corresponding calculated power results taken from Actel's and Altera's power estimator tools over frequency for the 14 instantiations of the gray-code design in the Actel IGLOO AGL030 FPGA and the Altera MAX IIZ EPM240Z CPLD. Xilinx does not offer a power estimator tool for the CoolRunner-II family of devices. Figure 10 shows a graphical representation of the data.

Table 10: **Dynamic Power Vendor Tools – Small Density Devices**

	AGL030		EPM240Z	
Frequency	**Current (mA)**	**Power (mW)**	**Current (mA)**	**Power (mW)**
0 MHz	0.006	0.007	0.030	0.054
10 MHz	0.525	0.630	2.250	4.050
20 MHz	1.044	1.253	4.460	8.028
30 MHz	1.563	1.876	6.680	12.024
40 MHz	2.082	2.498	8.890	16.002
50 MHz	2.601	3.121	11.100	19.980
60 MHz	3.121	3.745	13.320	23.976
70 MHz	3.641	4.370	15.540	27.972
80 MHz	4.162	4.994	17.760	31.968

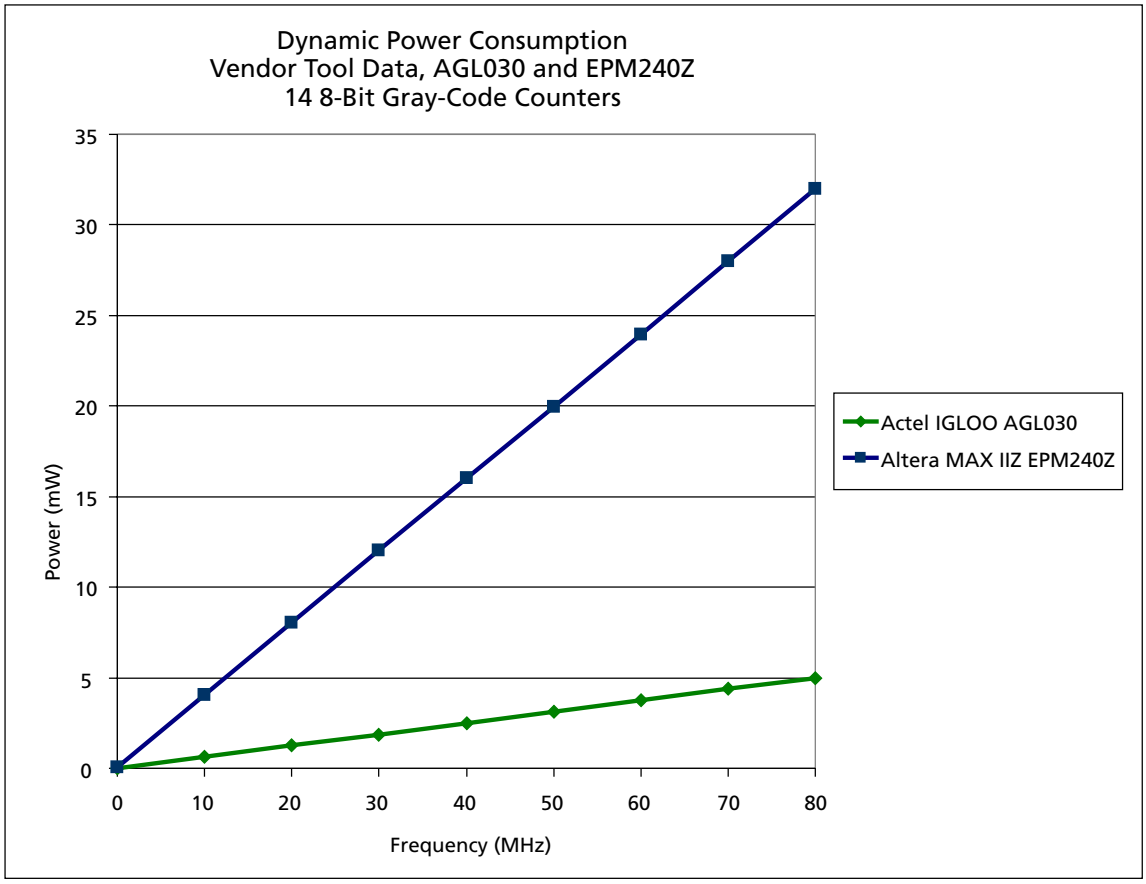


Figure 10: **Dynamic Power Consumption – Vendor Estimator Tool – Small Density Devices**

Dynamic Power – Actel IGLOO versus Altera Cyclone III FPGAs

Table 11 lists the dynamic power calculated using vendor tools for the Actel IGLOO AGL600 FPGA and the Altera Cyclone III EP3C5 FPGA. For this calculation, 290 counters were used in both devices. Figure 11 shows a graphical representation of the data.

Table 11: **Dynamic Power, Actel IGLOO (AGL600) versus Altera Cyclone III (EP3C5) – 290 Counters, Vendor Estimator Tool**

	AGL600		EP3C5		
Frequency	**1.2 V Current (mA)**	**Total Power (mW)**	**1.2 V Current (mA)**	**2.5 V V_{CCA} Current (mA)**	**Total Power (mW)**
0 MHz	0.028	0.034	6.000	11.000	34.700
10 MHz	9.436	11.323	15.000	11.000	45.500
20 MHz	18.845	22.614	25.000	11.000	57.500
30 MHz	28.253	33.904	35.000	11.000	69.500
40 MHz	37.662	45.194	45.000	11.000	81.500
50 MHz	47.070	56.484	54.000	11.000	92.300
60 MHz	56.478	67.774	64.000	11.000	104.300
70 MHz	65.887	79.064	74.000	11.000	116.300
80 MHz	75.295	90.354	83.000	11.000	127.100

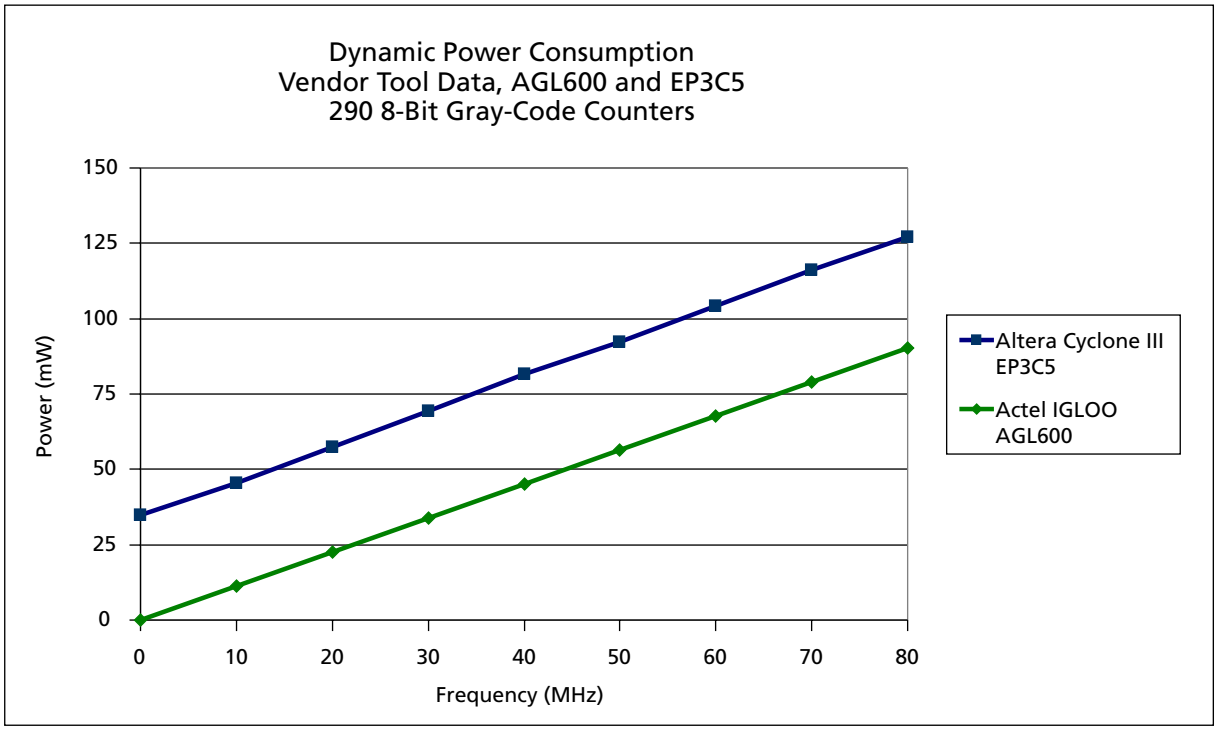


Figure 11: **Dynamic Power, Actel IGLOO and Altera Cyclone III, Vendor Estimator Tool**

Dynamic Power – Actel IGLOO versus Xilinx Spartan-3AN FPGAs

Table 12 lists the dynamic power calculated using vendor tools for the Actel IGLOO AGL600 FPGA and the Xilinx Spartan-3AN XC3S400AN FPGA, using 390 instantiations of the 8-bit gray-code counter. Figure 12 shows a graphical representation of the data.

Table 12: **Dynamic Power, Actel IGLOO (AGL600) versus Xilinx Spartan-3AN (XC3S400AN) – 390 Counters, Vendor Estimator Tool**

	AGL600		XC3S400AN		
Frequency	**1.2 V Current (mA)**	**Total Power (mW)**	**1.2 V Current (mA)**	**3.3 V V_{CCAUX} Current (mA)**	**Total Power (mW)**
0 MHz	0.028	0.034	15.000	12.000	57.600
10 MHz	9.726	11.671	38.000	12.000	85.200
20 MHz	19.425	23.310	61.000	12.000	112.800
30 MHz	29.123	34.948	84.000	12.000	140.400
40 MHz	38.821	46.585	106.000	12.000	166.800
50 MHz	48.519	58.223	129.000	12.000	194.400
60 MHz	58.218	69.862	152.000	12.000	222.000
70 MHz	67.916	81.499	174.000	12.000	248.400
80 MHz	77.614	93.137	197.000	12.000	276.000

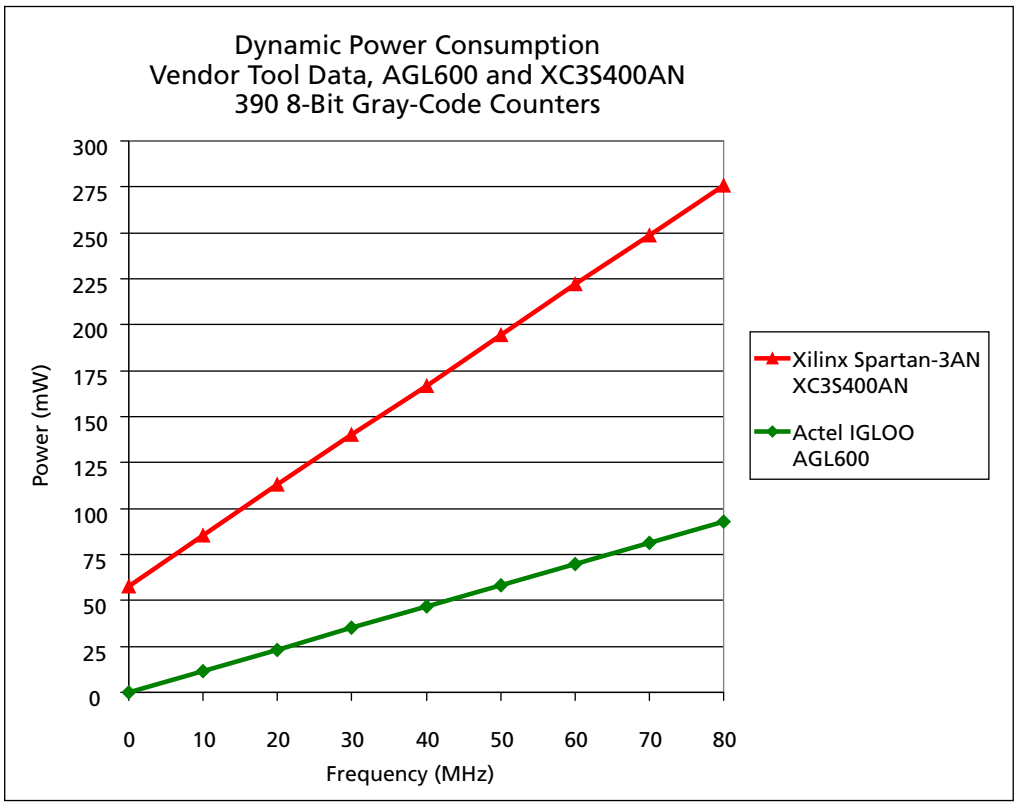


Figure 12: **Dynamic Power, Actel IGLOO and Xilinx Spartan-3AN, Vendor Estimator Tool**

Dynamic Power – Large Density Device Comparison

For the large density device comparison, we compared Actel's AGL600 FPGA against Altera's EP3C5 FPGA, and we also compared Actel's AGL600 FPGA against Xilinx's Spartan-3AN FPGA. These two comparisons used different designs (290 counters and 390 counters, respectively) due to the different densities of the devices we were comparing. As stated earlier, the method used for the dynamic power comparison test was to fill the smaller of the two devices being compared and use that design for both devices. To compare all three devices at the same time with the same design, we used the 290-counter design across all three devices. Figure 13 shows the dynamic power consumed for all three large devices using the 290-counter design.

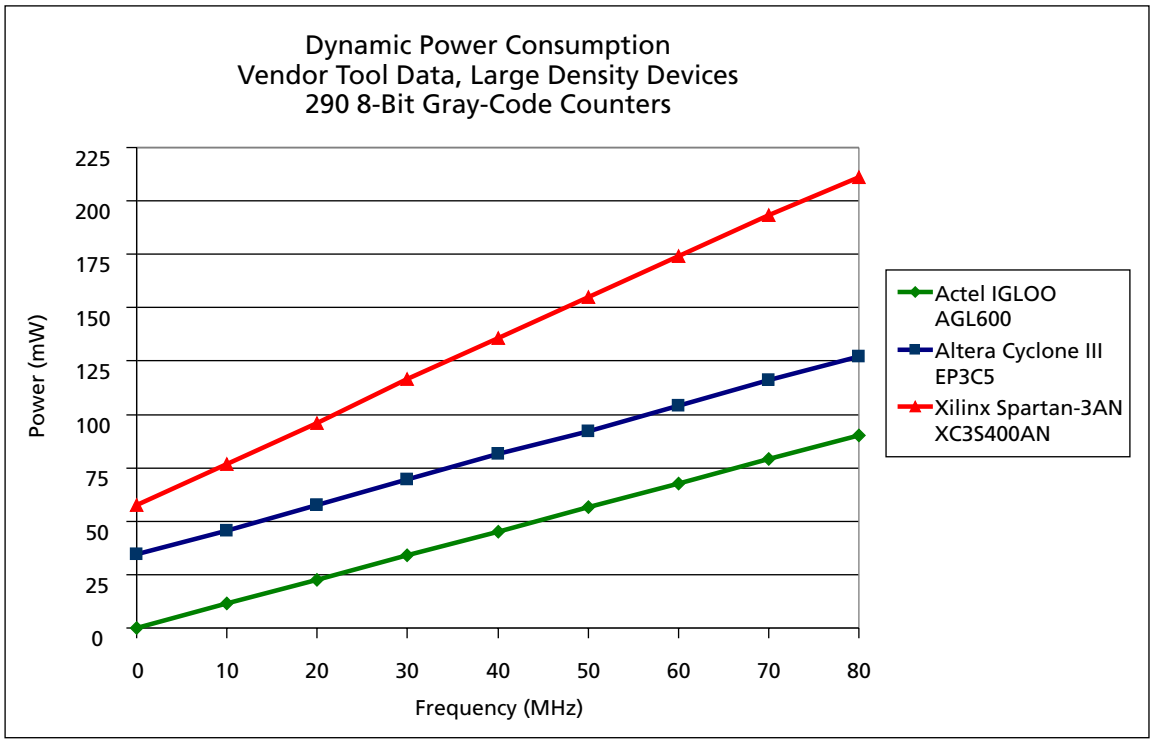


Figure 13: **Dynamic Power, Actel IGLOO (AGL600), Altera Cyclone III (EP3C5), Xilinx Spartan-3AN (XC3S400AN) – 290 Counters, Vendor Estimator Tool**

Dynamic Power Measured

Dynamic power measurements were taken on the small density devices using the power comparison board. The designs used in the tool comparisons for dynamic data were programmed into the devices and measured over frequency. Since there are no estimation tools available for the Xilinx CoolRunner-II CPLDs, power measurements with taken with silicon to perform the dynamic power comparison.

Measured Dynamic Power – Small Density Devices

Table 13 shows the dynamic power consumption of the Actel IGLOO AGL030 FPGA and the Altera MAX IIZ EPM240Z CPLD (14 counters in both devices). Figure 14 shows a graphical representation of the data.

Table 13: **Dynamic Power Measured – Small Density Devices**

	AGL030		EPM240Z	
Frequency	**Current (mA)**	**Power (mW)**	**Current (mA)**	**Power (mW)**
0 MHz	0.002	0.003	0.025	0.044
10 MHz	0.730	0.876	1.678	3.020
20 MHz	1.460	1.752	3.230	5.814
30 MHz	2.190	2.628	4.980	8.964
40 MHz	2.770	3.324	6.620	11.916
50 MHz	3.460	4.152	8.250	14.850
60 MHz	4.160	4.992	9.880	17.784
70 MHz	4.850	5.820	11.510	20.718
80 MHz	5.520	6.624	13.120	23.616

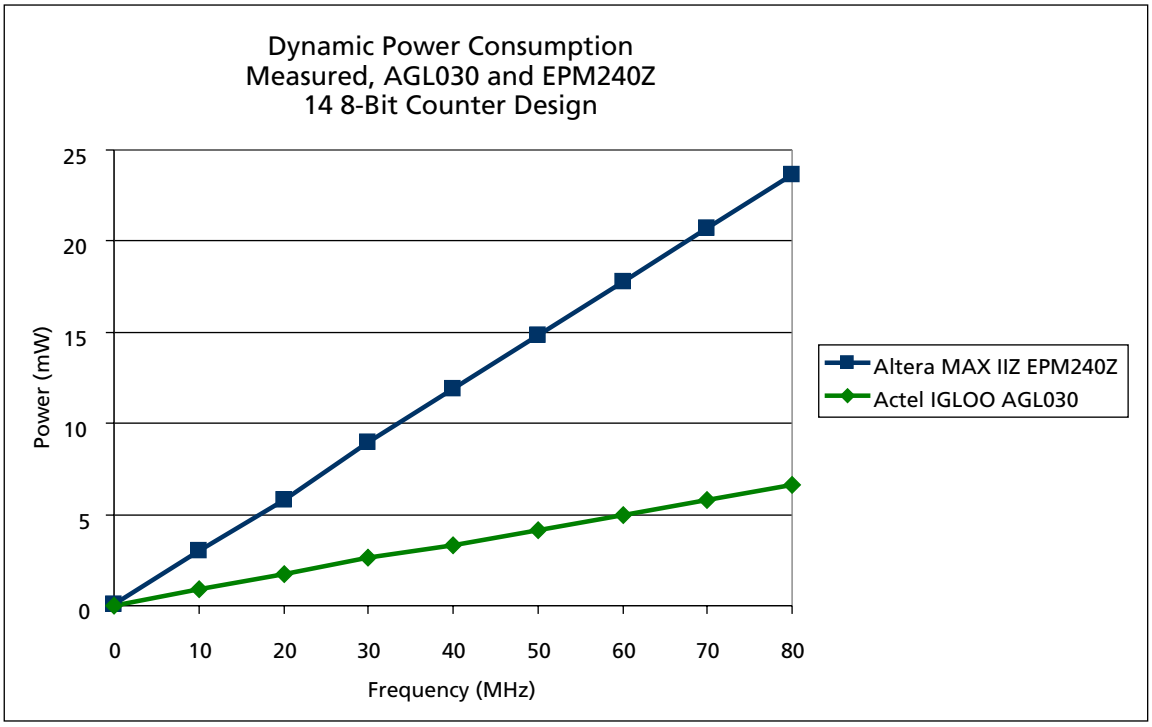


Figure 14: **Dynamic Power Measured – Actel IGLOO AGL030 and Altera EPM240Z (14 counters)**

Table 14 shows the dynamic power consumption of the Actel IGLOO AGL030 FPGA and the Xilinx CoolRunner-II XC2C256 CPLD (22 counters in both devices). Figure 15 shows a graphical representation of the data.

Table 14: **Dynamic Power Measured – Actel IGLOO AGL030 and Xilinx CoolRunner-II XC2C256 (22 counters)**

	AGL030		XC2C256	
Frequency	**Current (mA)**	**Power (mW)**	**Current (mA)**	**Power (mW)**
0 MHz	0.002	0.003	0.020	0.037
10 MHz	0.870	1.044	4.539	8.170
20 MHz	1.740	2.088	9.026	16.247
30 MHz	2.910	3.492	13.340	24.012
40 MHz	3.880	4.656	17.980	32.364
50 MHz	4.850	5.820	22.440	40.392
60 MHz	5.830	6.996	26.760	48.168
70 MHz	6.780	8.136	31.000	55.800
80 MHz	7.710	9.252	35.190	63.342

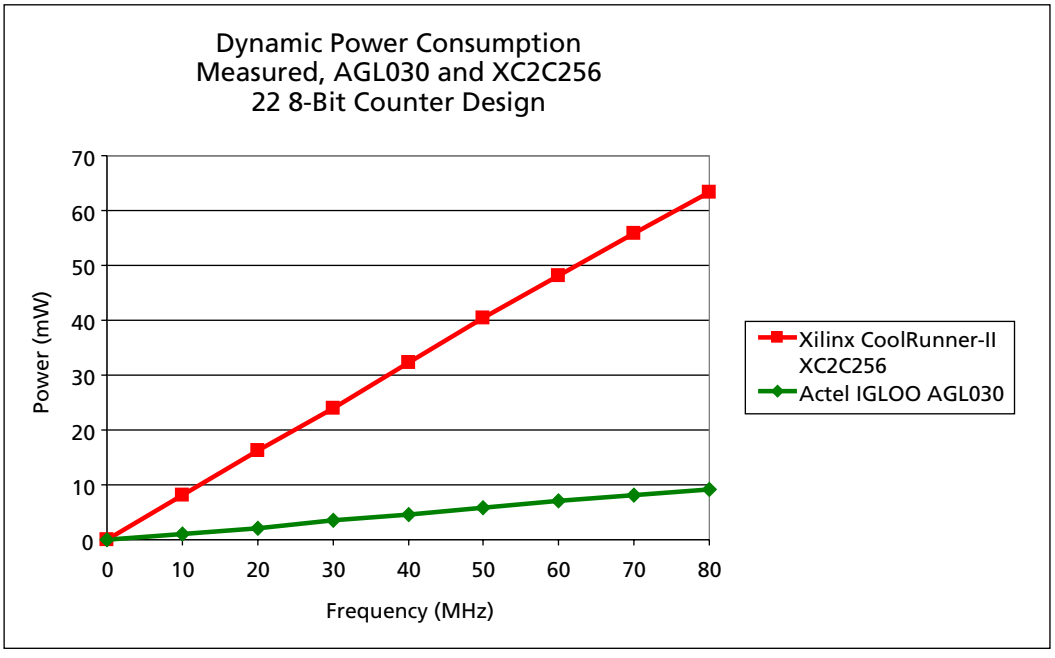


Figure 15: **Dynamic Power Measured – Actel IGLOO AGL030 and Xilinx CoolRunner-II XC2C256 (22 counters)**

Measured Dynamic Power Summary– Small Density Devices

Comparing small density devices over different frequencies using the gray-code counter design makes it clear that at any frequency, the Actel IGLOO AGL030 FPGA consumes less power than the Altera MAX IIZ EPM240Z CPLD and the Xilinx CoolRunner-II XC2C256 CPLD. As frequency increases, Actel's IGLOO power advantage increases.

Conclusion

This paper proves that Actel's flash-based IGLOO FPGAs are the undisputed low-power leaders in the industry, regardless of logic density, design configuration, or power mode.

Comparing small density devices (30 k system gates) by analyzing vendor-generated data, we concluded that Actel IGLOO FPGAS had a dominant power advantage over Xilinx CoolRunner-II and Altera MAX IIZ CPLDs. With over 10 times lower power in static mode, static over temperature, dynamic, and total power, the IGLOO FPGA is the clear winner in the small density space.

Analyzing the power consumption of large density FPGAs (600 k system gates) by looking at vendor-generated data also shows a consistent power advantage for IGLOO FPGAs versus Xilinx Spartan-3AN and Altera Cyclone III FPGAs. With 1,000 to 1,700 times better static power in typical conditions and over a range of temperatures, and more than 100 mW difference in dynamic power, the IGLOO FPGA is the clear winner in the large density space.

After comparing datasheets, vendor power-estimation tools, and real silicon measurements, Actel's IGLOO FPGAs have been proven to have 10 to 1,700 times lower power than competitive programmable logic offerings across logic densities.

Referenced Documents

Actel IGLOO Low-Power Flash FPGAs datasheet (Advanced v0.1)

http://www.actel.com/documents/IGLOO_DS.pdf

Actel’s Total System Power brochure

http://www.actel.com/documents/Power_PIB.pdf

Altera Cyclone III Device Datasheet: DC and Switching Characteristics (CIII52001-1.5)

http://www.altera.com/literature/hb/cyc3/cyc3_ciii52001.pdf

Altera MAX II Device Family DC and Switching Characteristics (MII51005-2.1)

http://www.altera.com/literature/hb/max2/max2_mii51005.pdf

Xilinx XC2C256 CoolRunner-II CPLD datasheet (DS094 v3.2)

http://www.xilinx.com/support/documentation/data_sheets/ds094.pdf

Xilinx Spartan3-AN FPGA Family datasheet (DS557-3 (v3.0)

http://www.xilinx.com/support/documentation/data_sheets/ds557.pdf

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