SmartTime Tutorial

Libero SoC for ProASIC3

NOTE: PDF files are intended to be viewed on the printed page; links and cross-references in this PDF file may point to external files and generate an error when clicked. **View the online help included with software to enable all linked content.**

Microsemi

Table of Contents

The following tutorials explore common SmartTime features with example designs:

- 32-Bit Shift Register with Clock Enable
- Design Using Both Clock Edges
- 16-Bit Binary Counter
- False Path Constraints
- Cross Clock Domain Analysis

Many actions described in the tutorials can be performed from the menus or in the SmartTime Toolbar. The table below lists all the SmartTime Toolbar actions.

Table 1 · SmartTime Toolbar

Icon	Description
	Commits the changes
	Prints the contents of the constraints editor
	Copies data to the clipboard
	Pastes data from the clipboard
	Modifies the selected object from the constraints editor
	Deletes the selected object from the constraints editor
	Undoes previous changes
	Redoes previous changes
	Opens the maximum delay analysis view
	Opens the minimum delay analysis view
	Opens the manage clock domains manager
	Opens the path set manager
	Recalculates all
	Opens the constraints editor
	Opens the add clock constraint dialog box
	Opens the add generated clock constraint dialog box
	Opens the set input delay clock constraint dialog box
	Opens the set output delay clock constraint dialog box

Icon	Description
	Opens the set false path constraint dialog box
	Opens the set maximum delay constraint dialog box
	Opens the set minimum delay constraint dialog box
	Opens the set multicycle constraint dialog box
	Opens the set clock source latency dialog box
	Opens the set constraint to disable timing arcs dialog box
	Opens the set clock-to-clock uncertainty constraint dialog box
	Checks timing constraints
	Opens the constraint wizard

32-Bit Shift Register

Set Up Your Libero Project for 32-Bit Shift Register with Clock Enable

This tutorial section describes how to enter a clock constraint for the 32-bit shift register shown in the figure below. You will use the SmartTime Constraints Editor and perform post-layout timing analysis using the SmartTime Timing Analyzer.

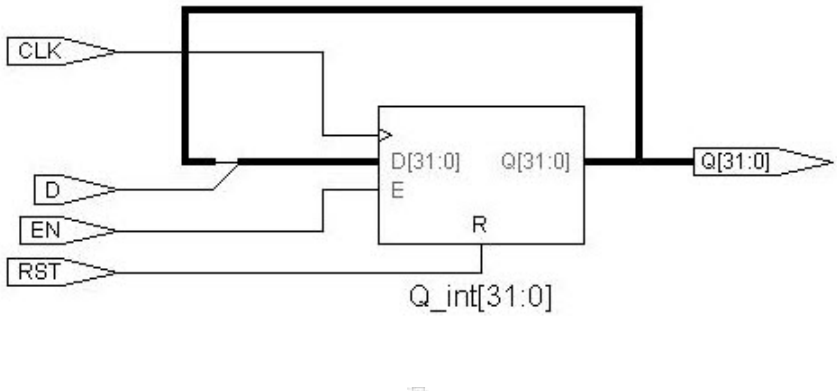

Figure 1 · 32-Bit Shift Registers

Use the links below to go directly to a topic:

- Add a Clock Constraint - 32 Bit Example
- Run Place and Route
- Maximum Delay Analysis with Timing Analyzer- 32-Bit Example
- Minimum Delay Analysis with Timing Analyzer - 32-Bit Example
- Changing Constraints and Observing Results - 32-Bit Example

To set up your project:

1. Invoke Libero SoC. From the **Project** menu, choose **New Project**.
2. Enter Shift32 for your new project name and browse to a folder for your project location. Enter the following values for the project settings (as shown in the figure below):

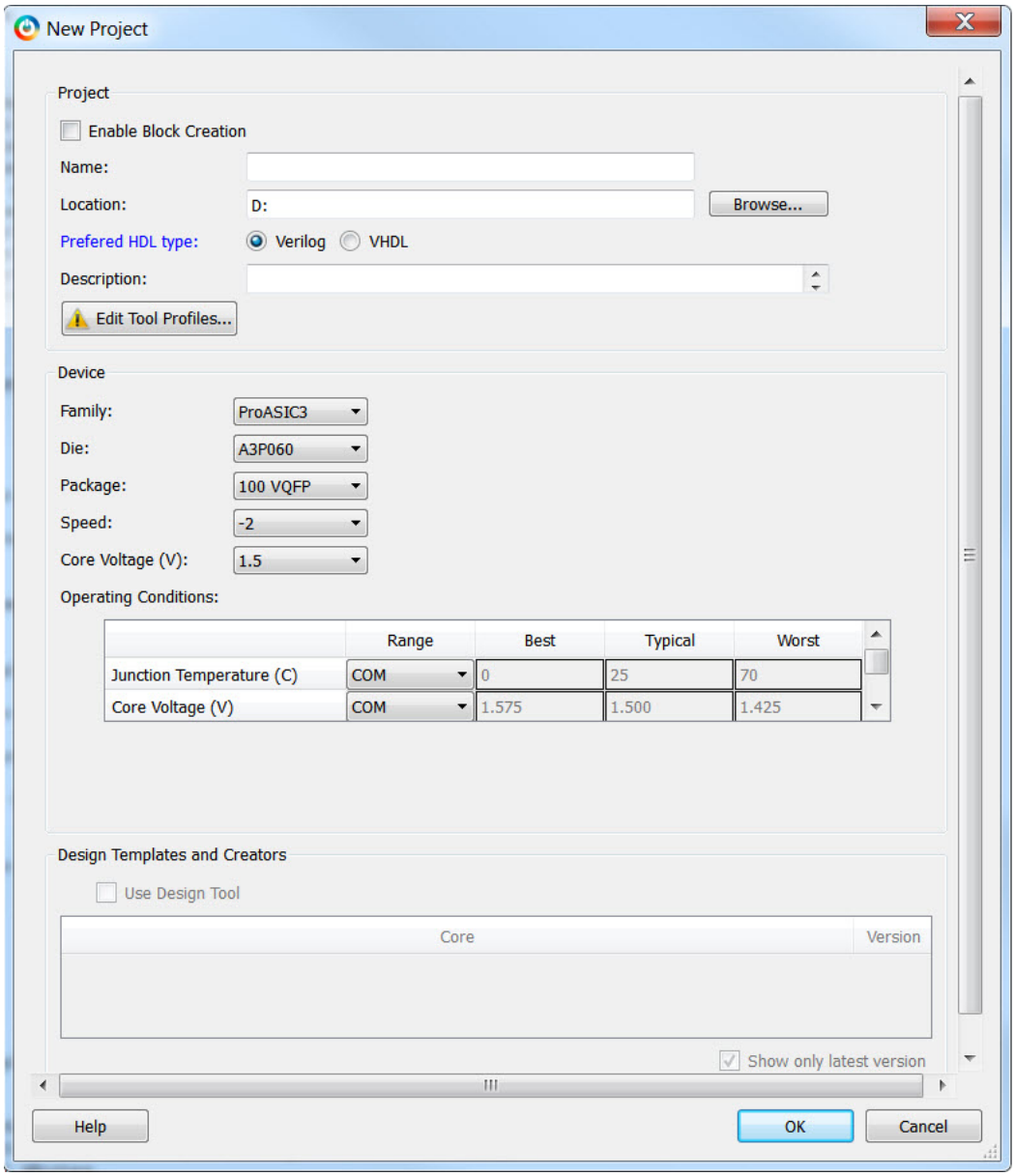

Figure 2 · 32 Bit Shift Register Project Settings

- **Family**: ProAsic3
- **Die**: A3P060
- **Package**: 100 VQFP
- **Speed**: -2
- **Die Voltage**: 1.5 V
- All other fields: Use default values

3. Click **OK** to continue.
4. From the View menu, display the following windows (**View > Windows > <window name>**):

- Design Flow
- Design Hierarchy
- Files
- Log

- Search Results
- HDL Source Files

5. From the **File** menu, choose **Import > HDL Source File**s and import the Verilog file **shift_reg32.v** for the 32-bit Shift Register.

After you import the file, confirm that the imported file appears in the Files window, as shown in the figure below.

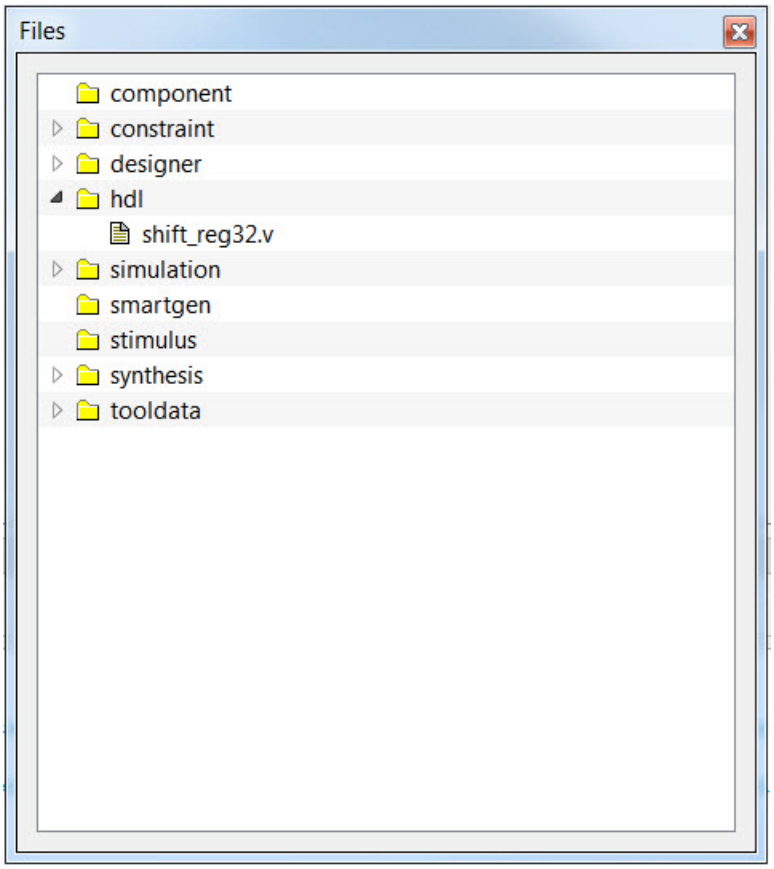

Figure 3 · HDL File shift_reg32.v in the Libero SoC File Window

Confirm that the shift_reg32 design appears in the Design Hierarchy window, as shown in the figure below.

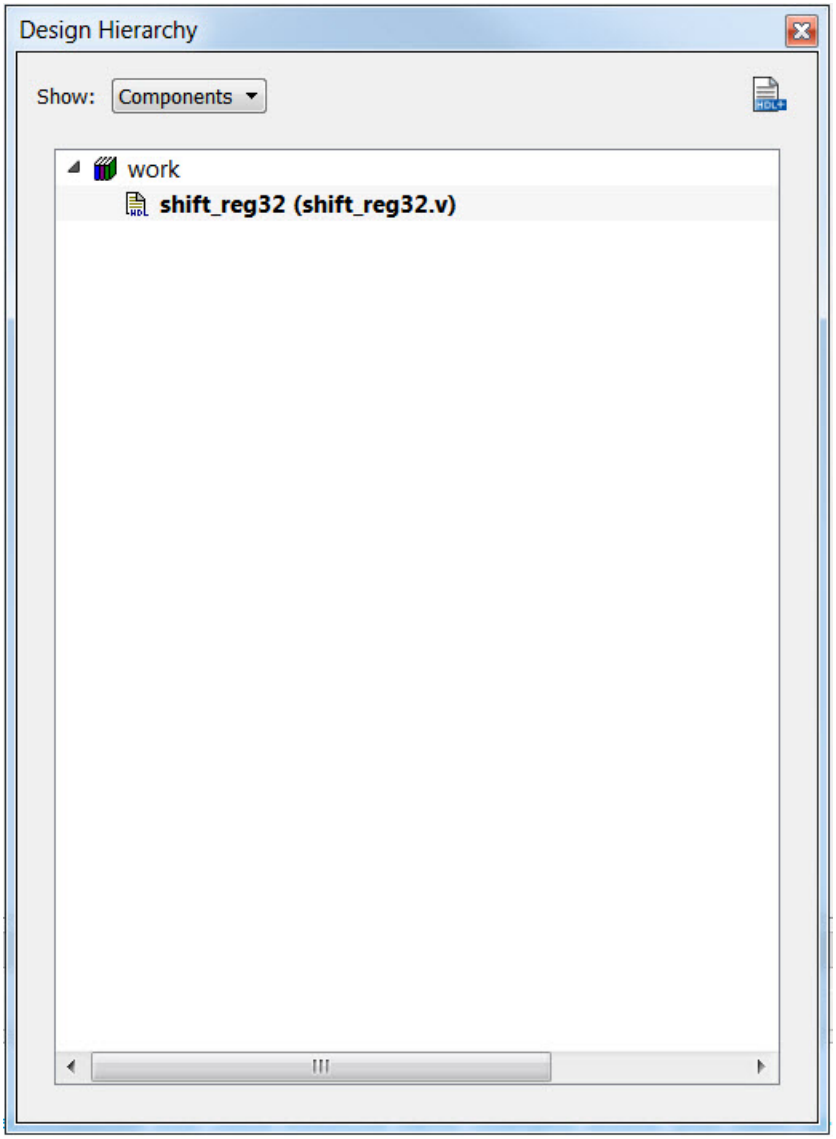

Figure 4 · shift_reg32 in the Design Hierarchy Window

6. In the Design Flow window, double-click **Synthesize** to run Synplify Pro with default settings. A green check marks appears next to Synthesize when Synthesis is successful (as shown in the figure below).
7. Double-click **Compile** in the Design Flow window to run Compile with default settings. A green check mark appears next to Compile when it completes successfully (as shown in the figure below).

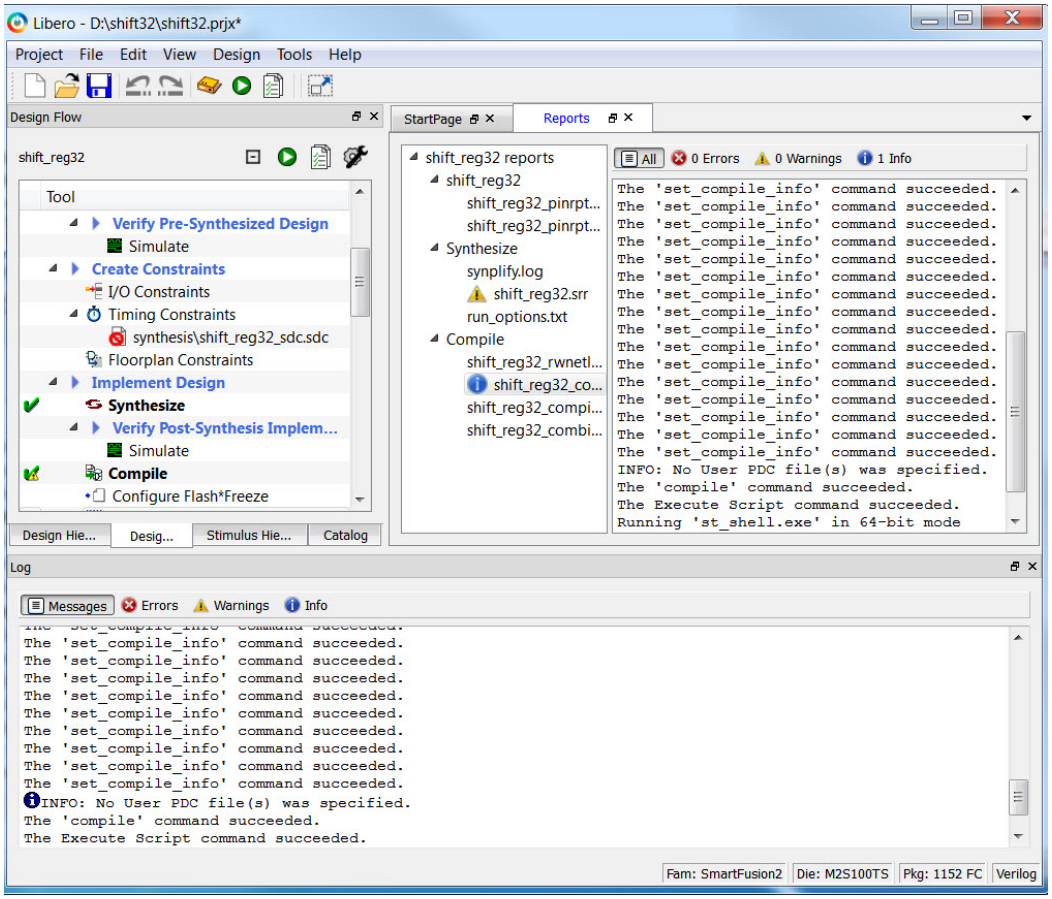

Figure 5 · Synthesis and Compile Complete - 32-Bit Shift Register with Clock Enable

Add a Clock Constraint - 32 Bit Example

To add a clock constraint to your design:

1. In the **Design Flow** window double-click **Create/Edit Timing Constraints** to open the Constraints Editor (as shown in the figure below). Designer opens before the Constraints Editor appears; minimize Designer and continue in the **Constraints Editor**.

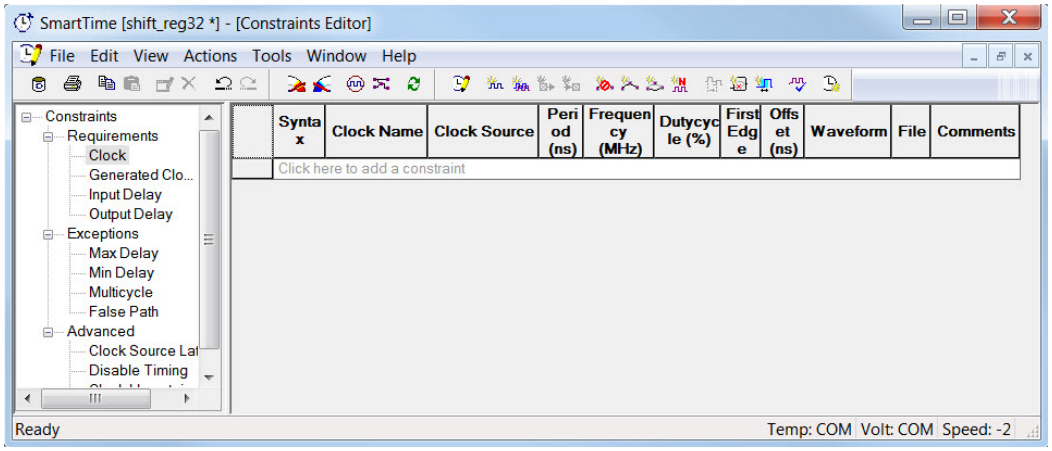

Figure 6 · SmartTime Constraints Editor

2. From the **Actions** menu, choose **Constraints > Clock** to open the Create Clock Constraint Editor, as shown in the figure below.

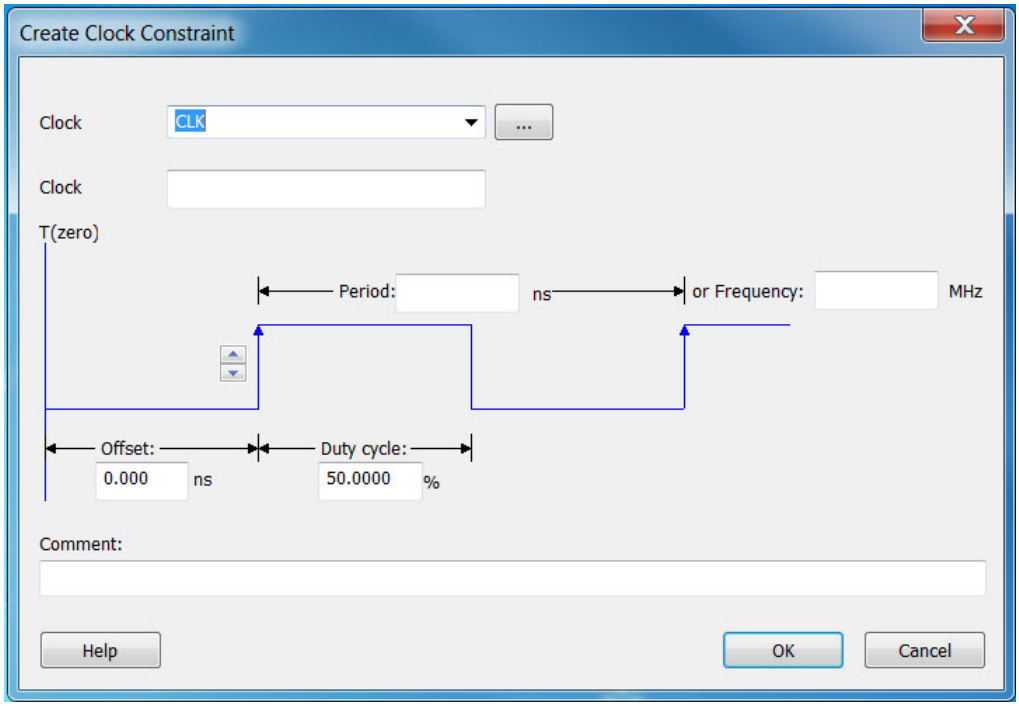

Figure 7 · Create Clock Constraint Dialog Box

3. Set the **Frequency** to **150 MHz** (as shown in the figure below) and leave all other values at the default setting. Click **OK** to continue.

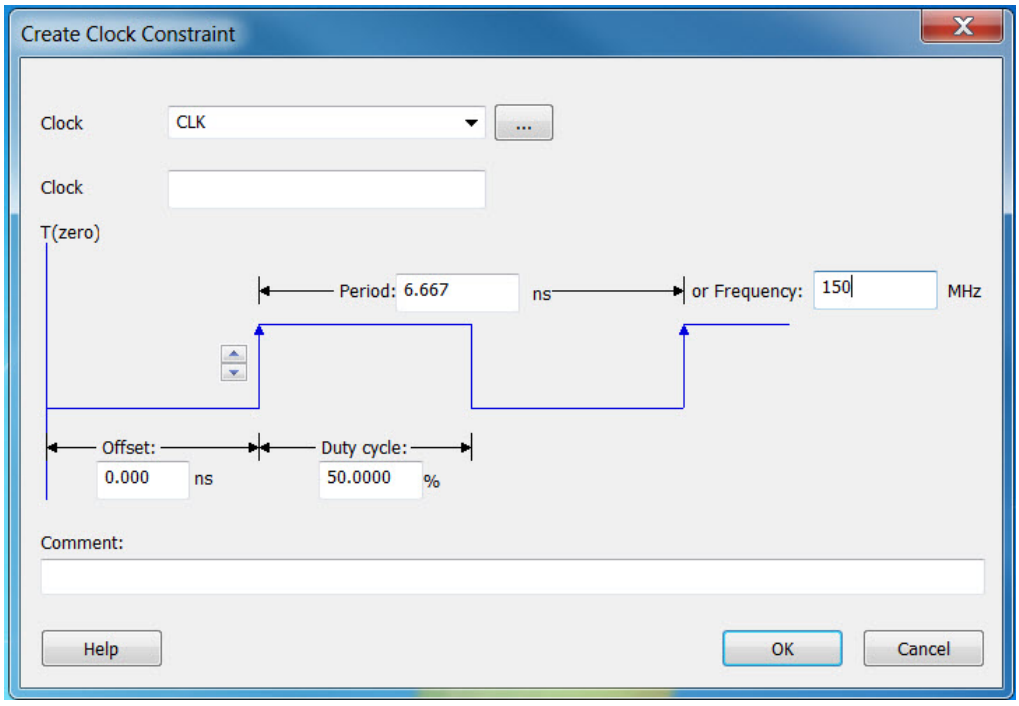

Figure 8 · Add a 150 MHz Clock Constraint

The clock constraint appears in the SmartTime Constraints Editor (as shown in the figure below).

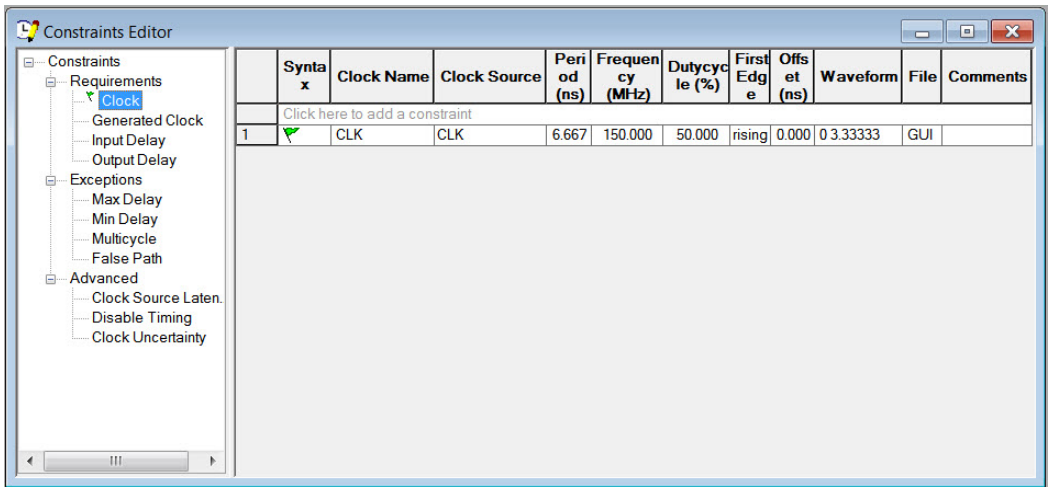

Figure 9 · 150 MHz Clock Constraint in the Constraint Editor

5. From the **File** menu, choose **Commit** to save the constraints.
6. From the SmartTime **File** menu, choose **Exit** to continue.

Run Place and Route

You must run Place and Route from Designer. To do so:

1. View Designer, as shown in the figure below.

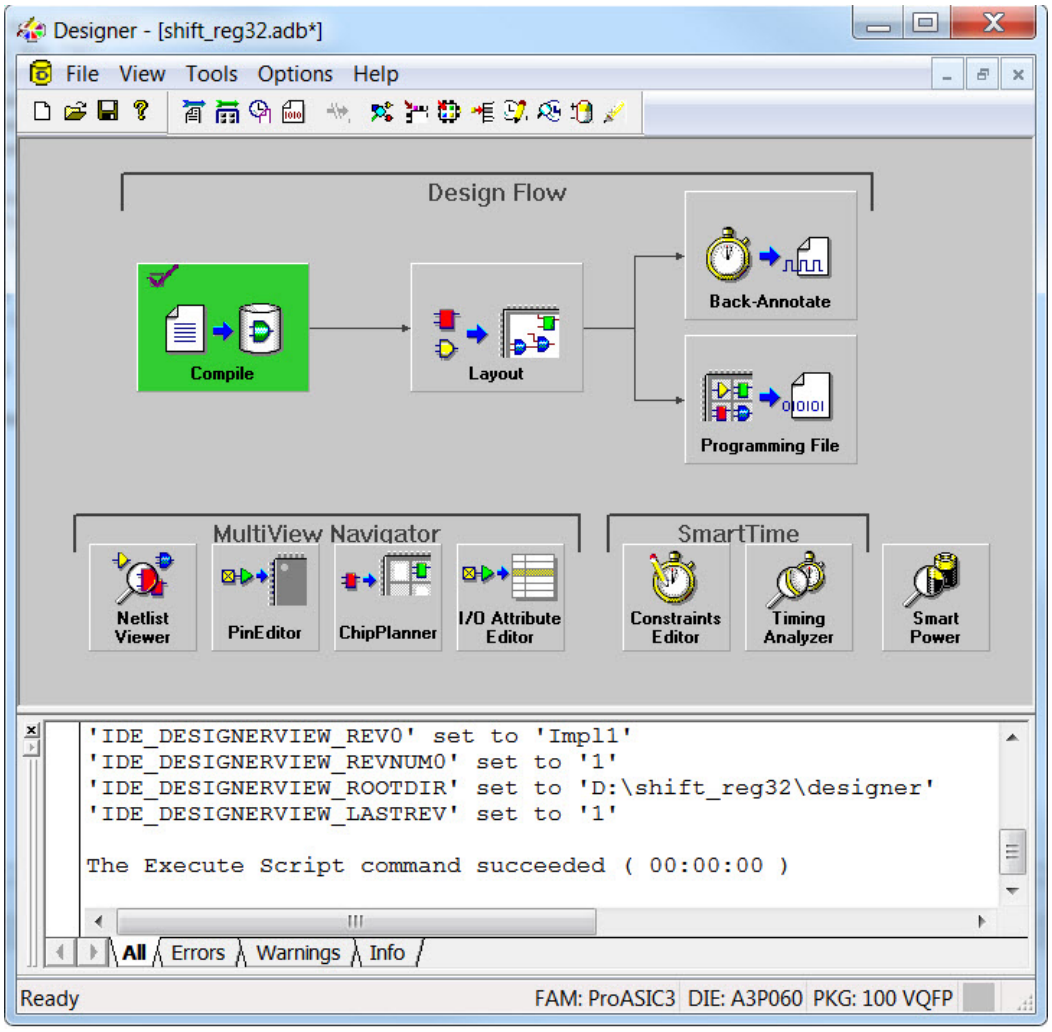

Figure 10 · Compile Complete, Ready for Layout

2. Click **Layout**.
3. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings (as shown in the figure below). Click **OK** to continue.

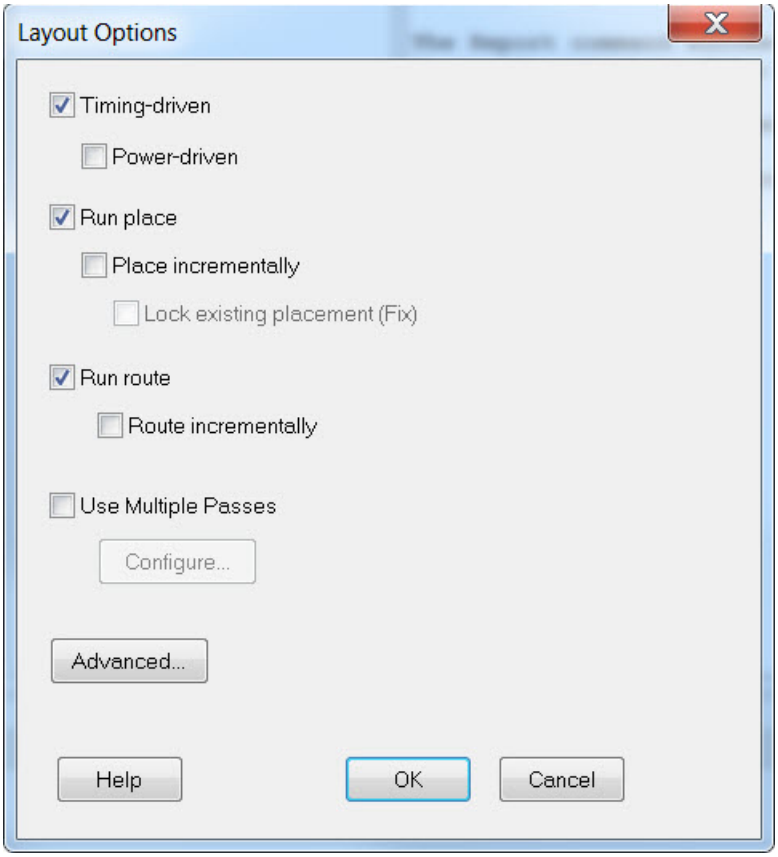

Figure 11 · Layout Options Dialog Box

The Layout button turns green to indicate that Layout has completed successfully.

Maximum Delay Analysis with Timing Analyzer- 32-Bit Example

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. Click the **Timing Analyzer** button in Designer to open SmartTime. The Maximum Delay analysis window appears (as shown in the figure below). A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.

The Maximum Delay Analysis Summary displays the:

- Maximum operating frequency for the design
- External setup and hold requirements
- Maximum and minimum clock-to-out times. In this example, the maximum clock frequency for CLK is 250 MHz.

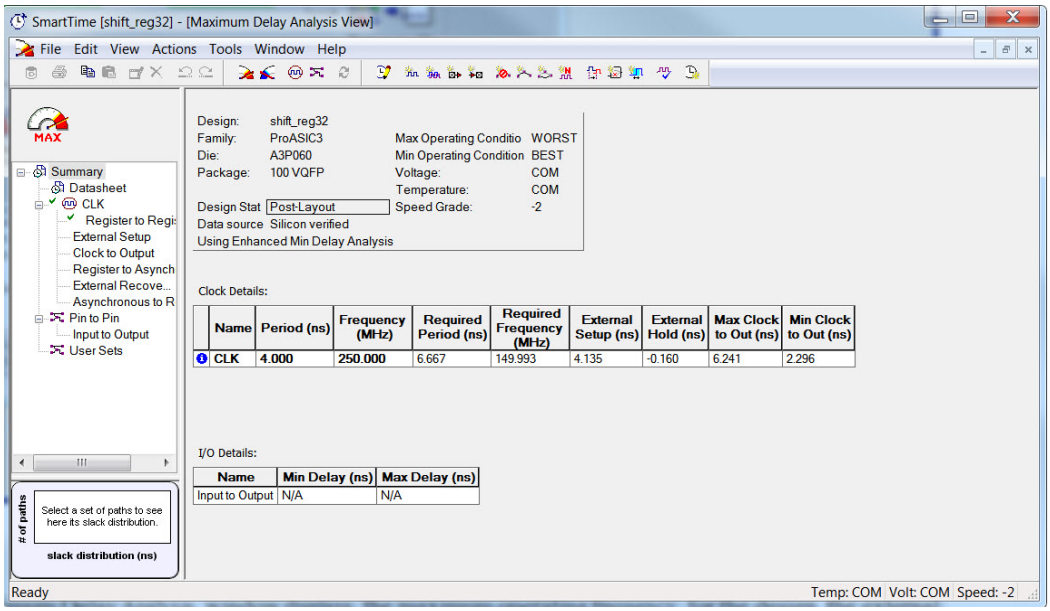

Figure 12 · Maximum Delay Analysis - Summary

2. Click the + sign next to CLK to expand the display and show the Register to Register, Input to Register and Register to Output path sets.
3. Select **Register to Register** to display the register-to-register paths. The window displays a list of register-to-register paths and detailed timing analysis for the selected path (as shown in the figure below). Note that all the slack values are positive, indicating that there are no setup time violations.

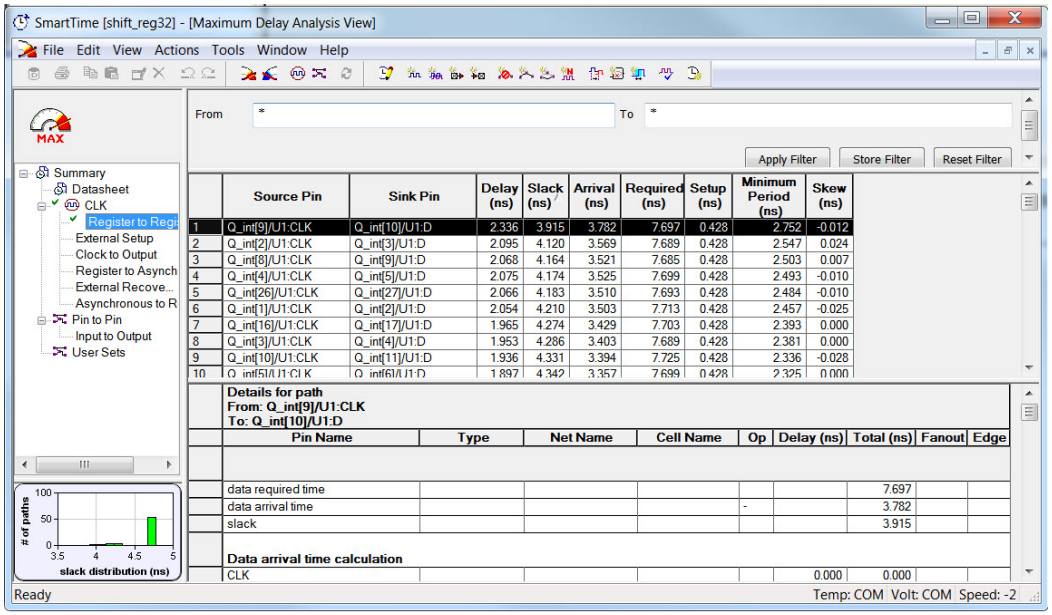

Figure 13 · SmartTime Register to Register Delay

4. Double-click a path row to open the **Expanded Path Window**. The window shows a calculation of the data arrival and required times along with a schematic of the path (as shown in the figure below).

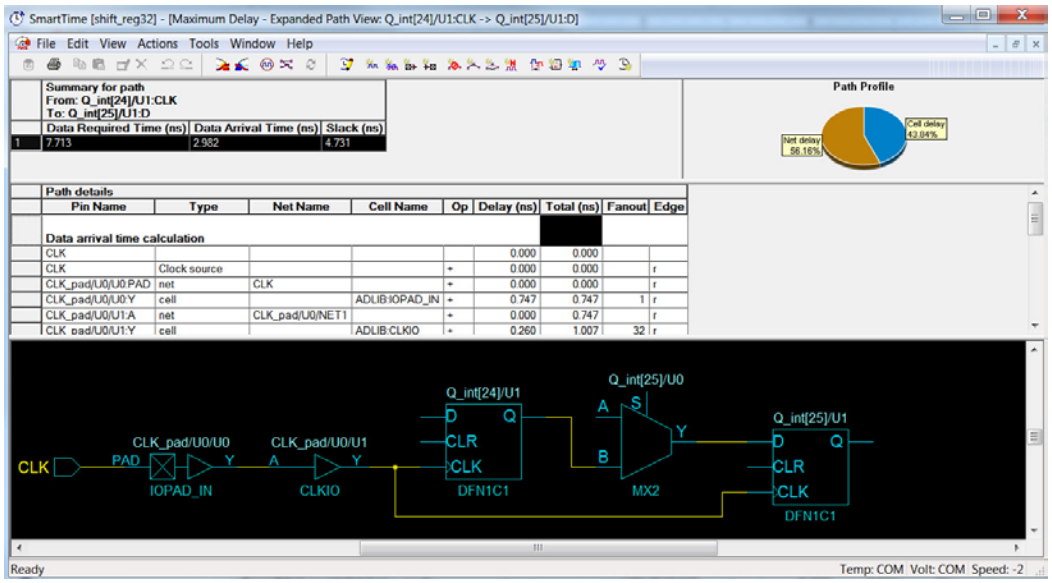

Figure 14 · Register-to-Register Expanded Path View

5. Select **External Setup** to display the Input to Register timing. Select **Path 24**. The Input Arrival time from the EN pin to Q_int[29]/UI:D is 3.162 ns, as shown in the figure below.

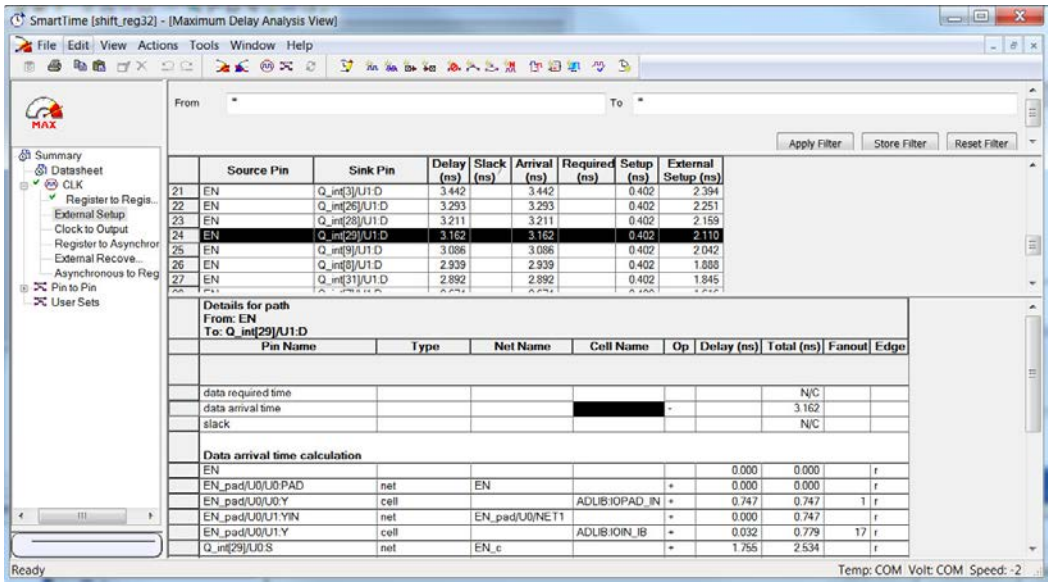

Figure 15 · SmartTime - Input to Register Path Analysis

6. Select **Clock to Output** to display the register to output timing. Select Path 14. The maximum clock to output time from CLK to Q[27] is 5.790 ns, as shown in the figure below.

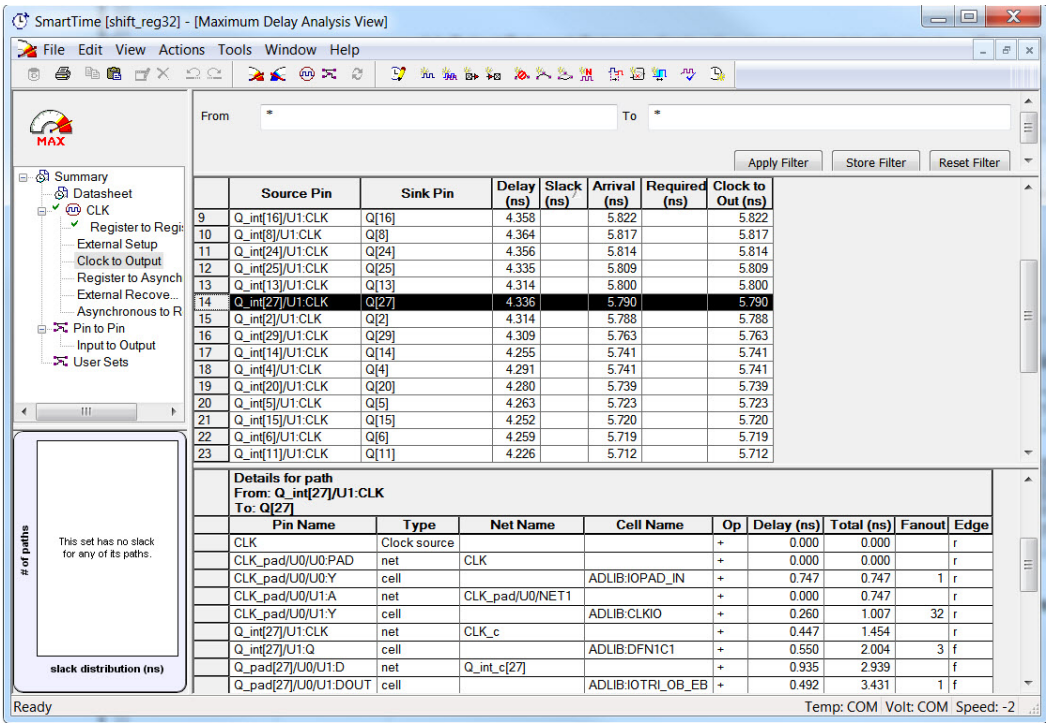

Figure 16 · SmartTime Clock to Output Path Analysis

Minimum Delay Analysis with Timing Analyzer - 32-Bit Example

The SmartTime Minimum Delay Analysis window identifies any hold violations that exist in the design.

To perform Minimum Delay Analysis:

1. From the SmartTime **Tools** menu, choose **Timing Analyzer > Minimum Delay Analysis**. The Minimum Delay Analysis window appears, as shown in the figure below.

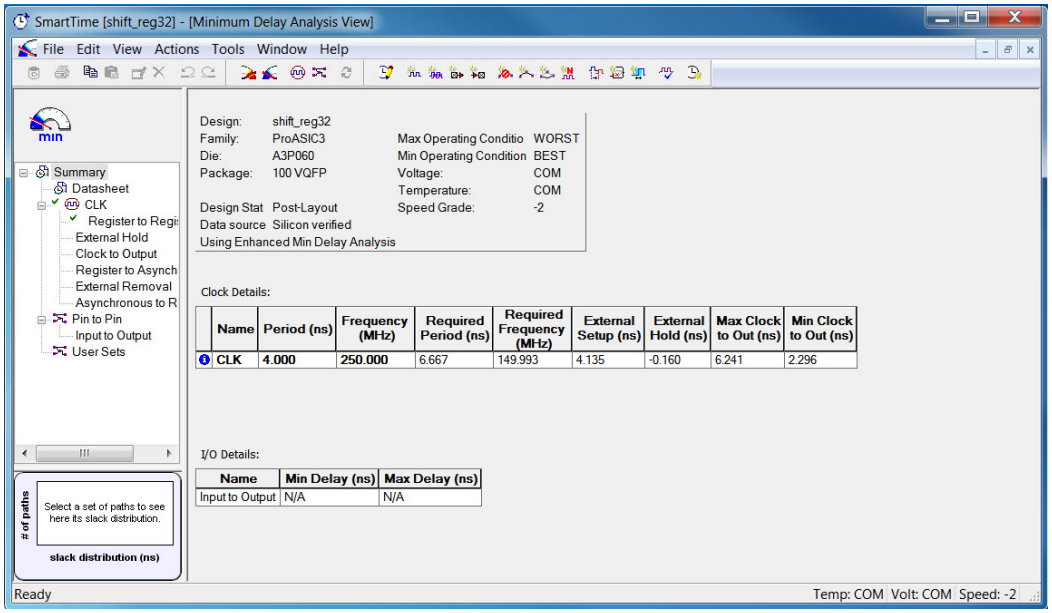

Figure 18 · SmartTime Minimum Delay Analysis View- Summary

2. Click the + next to CLK to expand the list and display Register to Register, External Hold, Clock to Output, Register to Asynchronous, External Removal and Asynchronous to Reset path sets.

3. Click **Register to Register** to display the reg to reg paths. The window displays a list of register to register paths and detailed timing analysis for the selected path. Note that all slack value are positive, indicating that there are no hold time violations.
4. Click to select the first path and observe the hold analysis calculation details, as shown in the figure below.

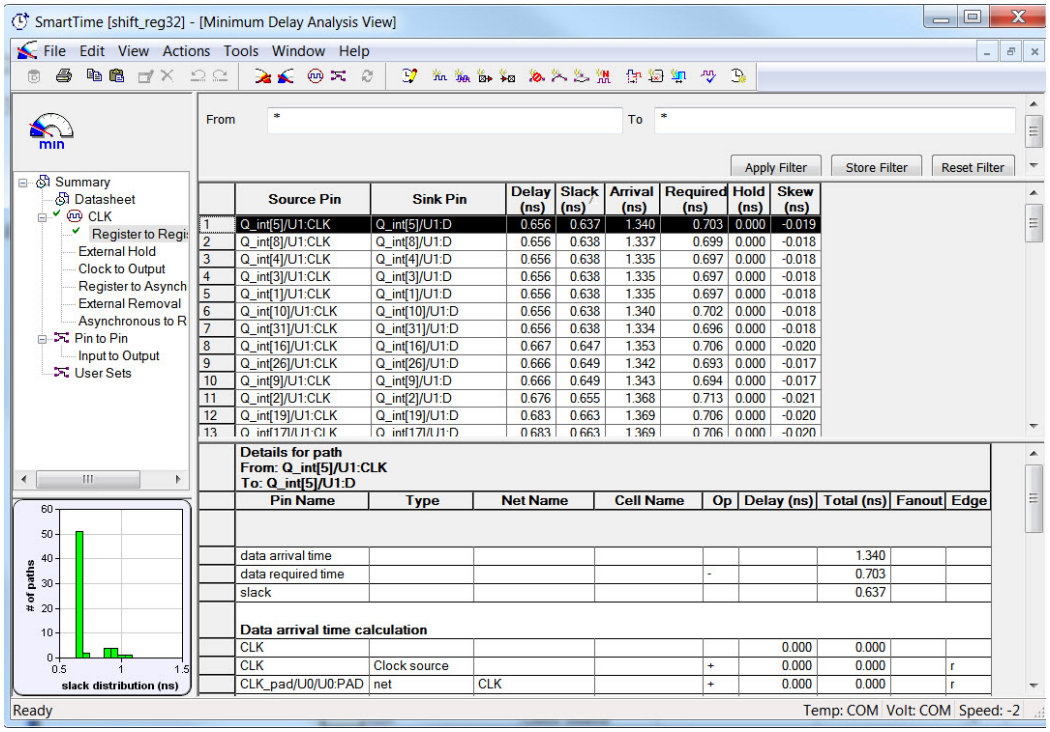

Figure 19 · SmartTime Minimum Delay Analysis

Changing Constraints and Observing Results - 32-Bit Example

You can use SmartTime to adjust constraints and view the results in your design. To do so:

1. Open the SmartTime Constraints Editor. From the **Tools** menu, choose **Constraints Editor > Primary**. The Constraints Editor displays the clock constraint at 150 MHz that you entered earlier, as shown in the figure below.

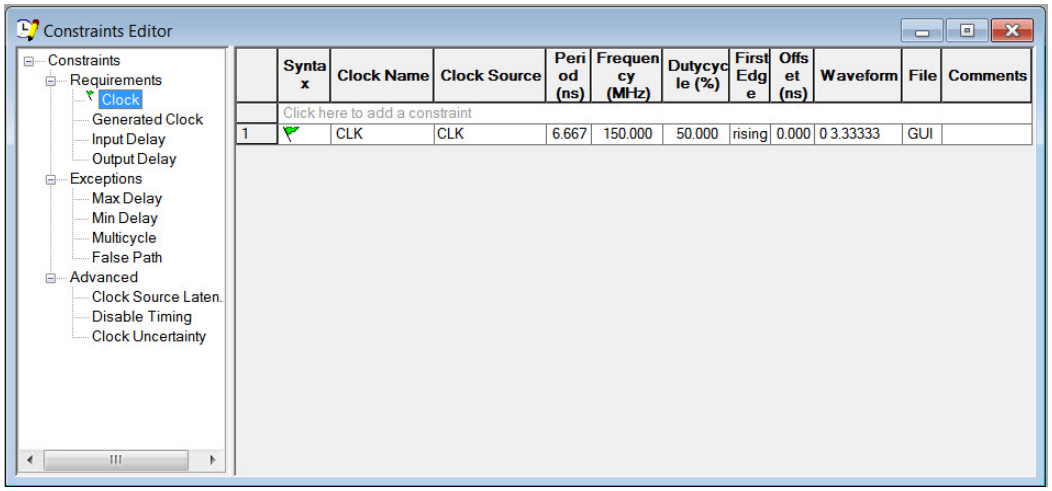

Figure 20 · Clock Constraint Set to 150 MHz

2. Double-click the first row to open the Edit Clock Constraint dialog box. Change the clock constraint from **150 MHz** to **600 MHz** and click **OK** to continue.
3. From the **View** menu, choose **Recalculate All** to recalculate the delays using your new clock constraint.
4. From the **Tools** menu, choose **Timing Analyzer > Maximum Delay Analysis View** to view the max delay analysis.
5. Expand the **CLK** in the Maximum Delay Analysis window. Click **Register to Register** to observe the timing information. Note that the negative slack (timing violations) are shown in red (as shown in the figure below).

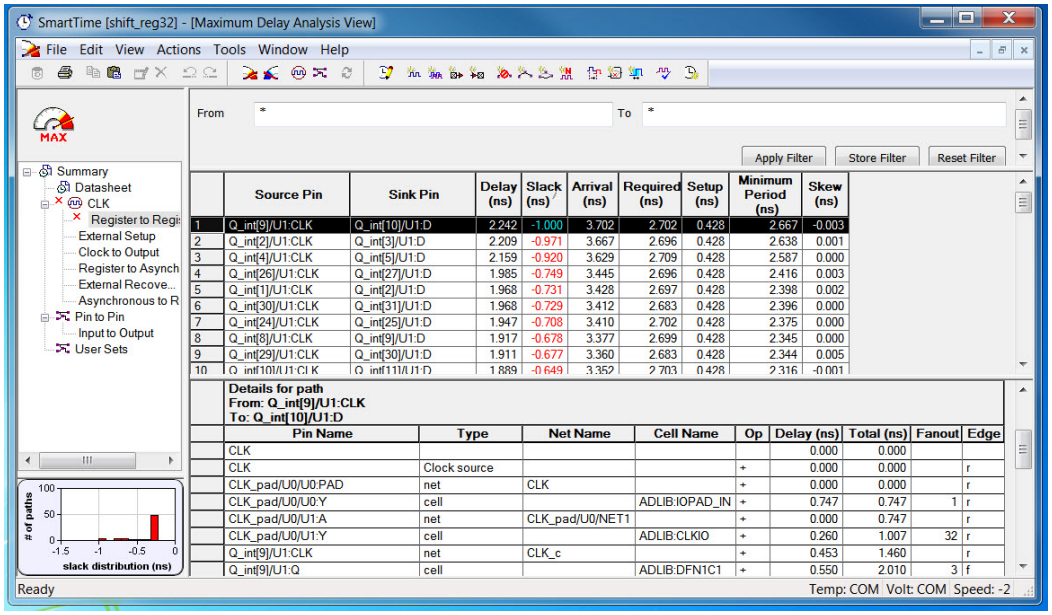

Figure 21 · Maximum Delay Analysis After Setting Clock Constraint to 600 MHz

6. Close SmartTime. Click **No** when prompted to commit your unsaved edits.
7. Close Designer. Click **Yes** if asked to save changes to shift_reg32adb.

Design Using Both Clock Edges

This example analyzes SmartTime reports that include both rising and falling edges of a clock in the same design. The design (as shown in the figure below) consists of a 16-bit serial-in parallel-out (SIPO) shift register, a control block and a 16-bit output register. The control block enables the output register after 16 bits of data have been shifted in. The shift register and the control block are clocked on the rising edge of the clock. The output register is clocked on the falling edge of the clock.

You will import the EDIF netlist (shifter.edn) and enter a clock constraint of 100 MHz. After routing the design you will analyze the timing to determine the maximum operating frequency and export a timing report.

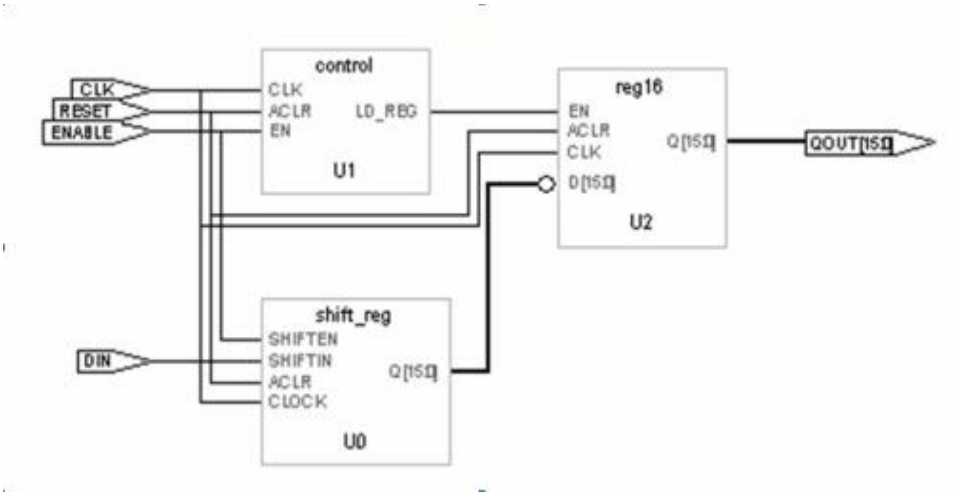

Figure 22 · Example Design that Uses Both Clock Edges

Set Up Your Example Design Project

1. Open Libero and create a new project (from the **Project** menu, choose **New Project**).
2. Name the project **Shifter** and set the project location according to your preferences. Enter the following values for your new project:

- **Family**: ProASIC3
- **Die**: A3P060
- **Package**: 100 VQFP
- **Speed**: -2
- **Die Voltage**: 1.5 V

Import the EDIF Netlist - Design Uses Both Clock Edges

You must import the shifter.edn file into your design for this tutorial. Download the design files from the Microsemi website.

To import the EDN file:

1. From the **File** menu, choose **Import > Others**.
2. Choose **EDIF Netlists** from the file type dropdown list in the Import Files dialog box.
3. Browse to the location of the **shifter.edn** file and select it. Click **Open** to import the file.
4. Verify that the file appears in your project, as shown in the figure below.

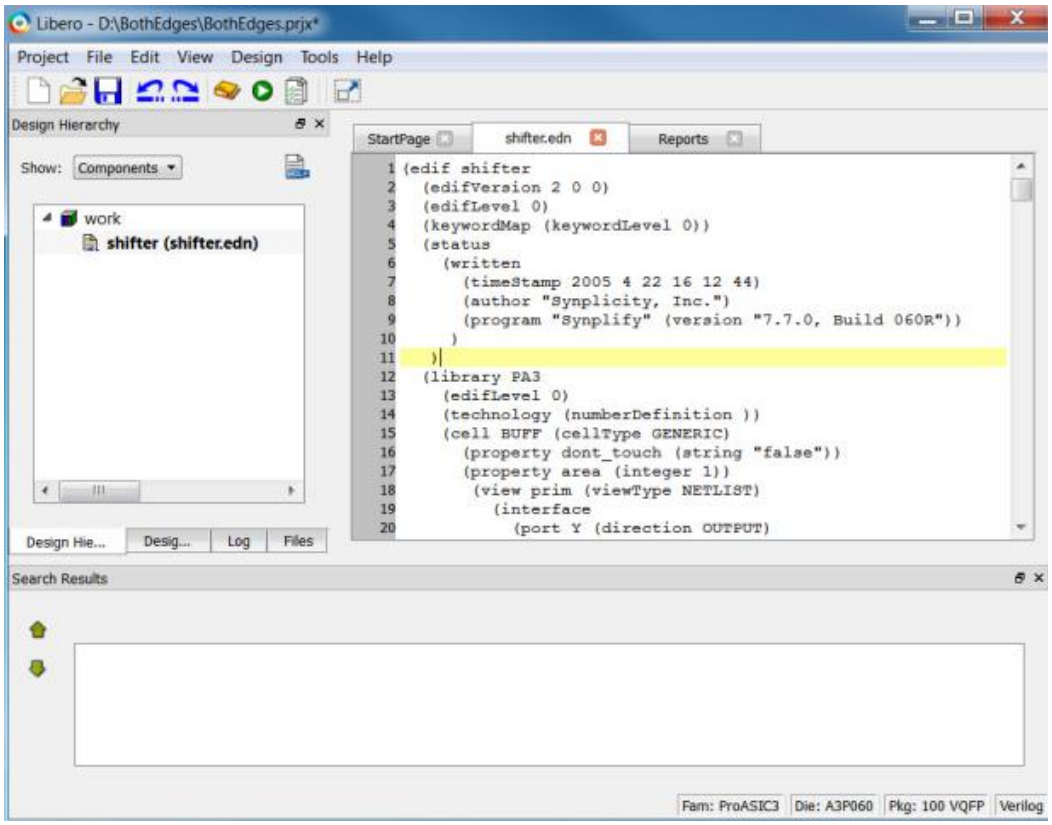

Figure 23 · shifter.edn in the Design Hierarchy

Add a Clock Constraint - Design Uses Both Clock Edges

To add a clock constraint to your example design:

1. In the Design Flow window, right-click **Create/Edit Timing Constraint** and choose **Open Interactively**. Designer opens and runs Compile with the default settings. After Compile is complete the Compile button in Designer turns green and the SmartTime Constraints Editor opens.
2. Click the Clock Constraint tab and enter a constraint for the clock source (CLK) of 100 MHz at a 50% duty cycle.

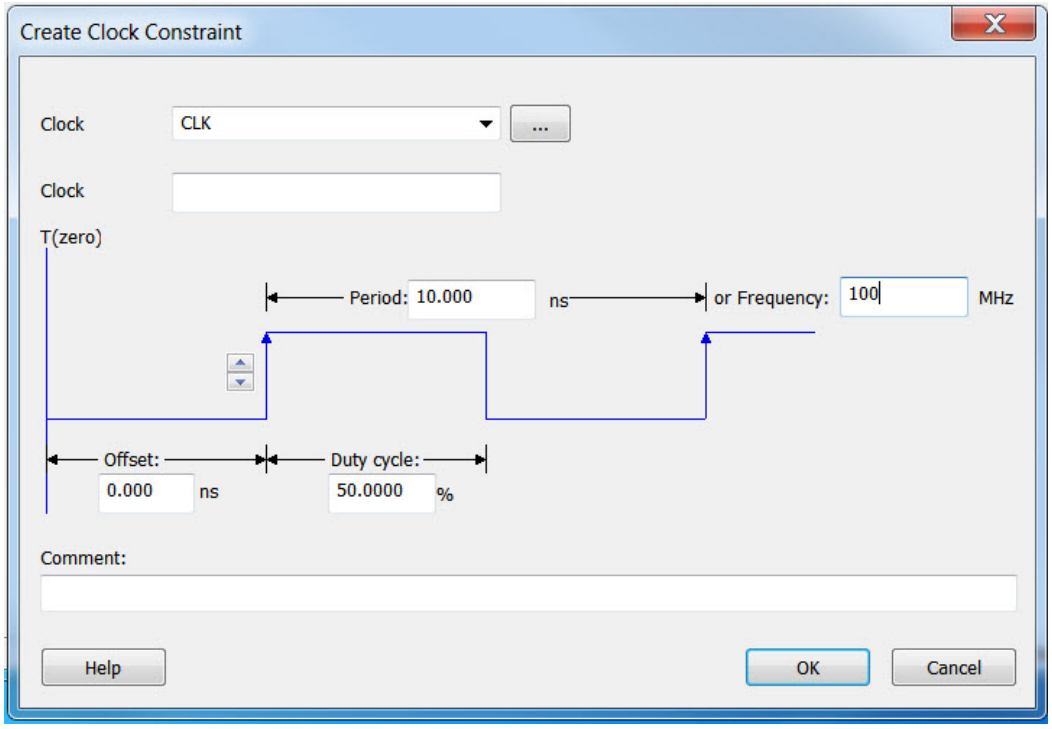

Figure 24 · Add 100 MHz Clock Constraint

The new constraint appears in the Constraints Editor, as shown in the figure below.

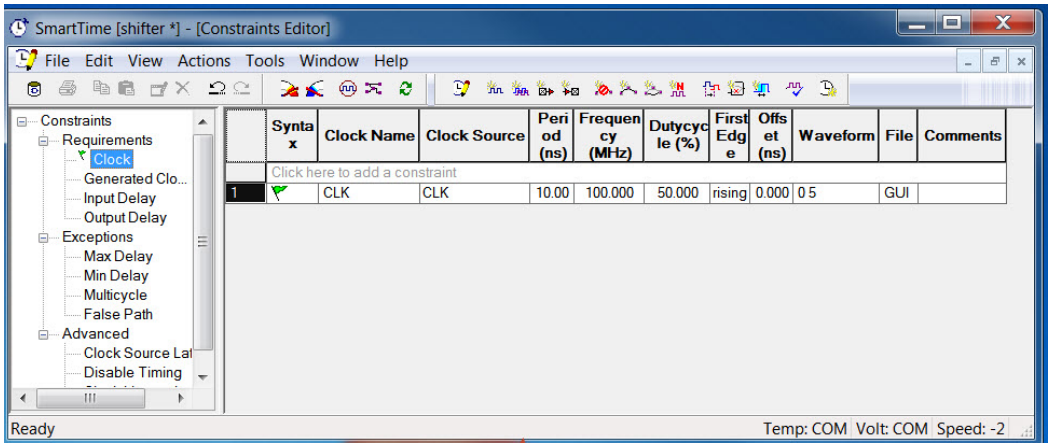

Figure 25 · 100 MHz Clock Constraint in the Design shifter

3. From the SmartTime **File** menu, choose **Commit** to save the constraints.
4. From the SmartTime **File** menu, choose **Exit** to proceed to Place and Route step.

Run Place and Route for a Design that Uses Both Clock Edges

To run Layout on the design 'shifter':

1. In Designer, click **Layout**.
2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings. Click **OK** to continue. The Layout button in Designer turns green when Layout has completed successfully.

Maximum Delay Analysis with Timing Analyzer - Design Using Both Clock Edges

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. Click the **Timing Analyzer** button in Designer to open SmartTime. The Maximum Delay analysis window appears (as shown in the figure below). A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.

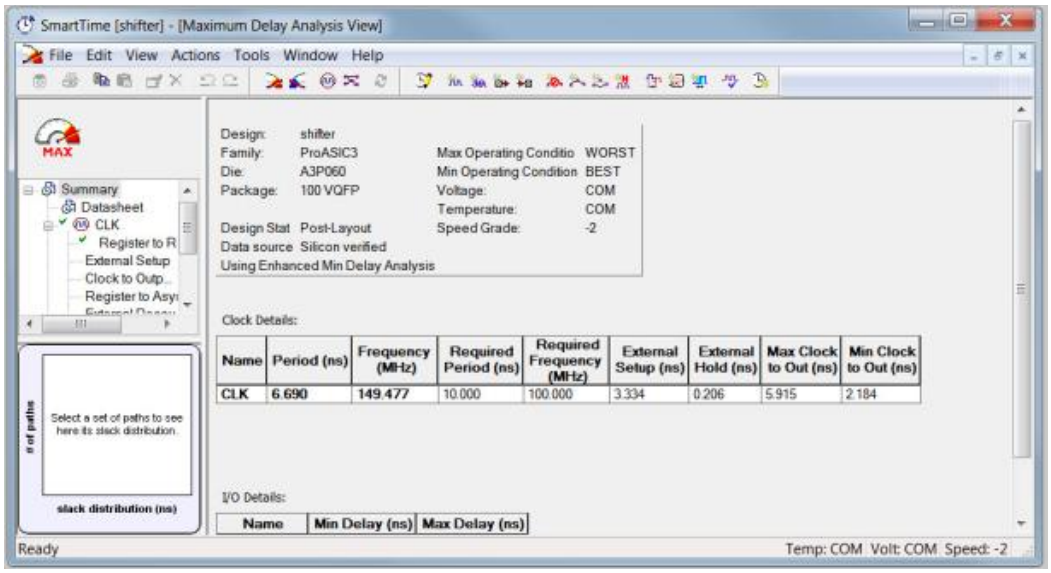

Figure 26 · Maximum Delay Analysis for Design shifter

The Summary in the Maximum Delay Analysis window indicates the maximum operating frequency for this design is 149.477 MHz.

2. Click the + sign next to CLK to expand the display and show the Register to Register, Input to Register and Register to Output path sets.
3. Select **Register to Register** to display the register-to-register paths. The window displays a list of register-to-register paths and detailed timing analysis for the selected path (as shown in the figure below). Note that all the slack values are positive, indicating that there are no setup time violations.
4. Click to select row 1 and study the timing analysis (resize the Maximum Delay Analysis window as required). The path is from the control block (U1) to the output register (U2). Note that SmartTime uses 5 ns in the data required calculation (as shown in the figure below). This is because the source flip flop uses the rising edge of the clock and the destination flip-flop used the falling edge of the clock.

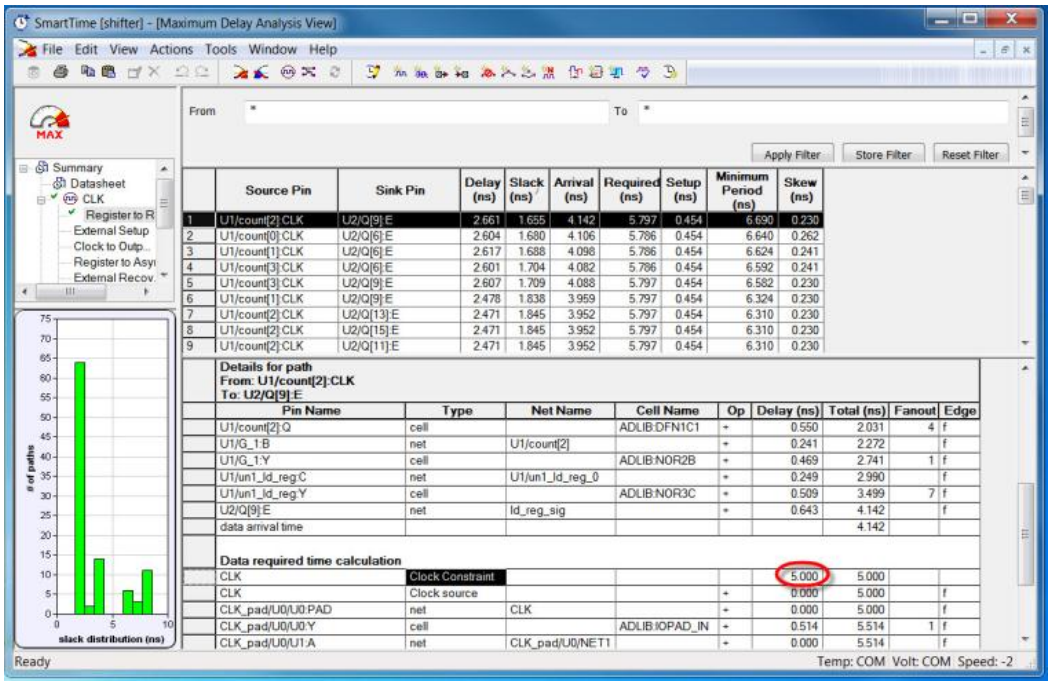

Figure 27 · Slack Calculation in Maximum Delay Analysis View

Cross Probing with SmartTime - Design Using Both Clock Edges

You can use SmartTime to cross probe in Designer and analyze your design.

To cross probe with SmartTime:

1. Double-click the first row in the Maximum Delay Analysis view to open the **Expanded Path** window (as shown in the figure below). The window shows the required data and arrival time calculation and a schematic of the path.

Click and drag in the schematic to view the selected area.

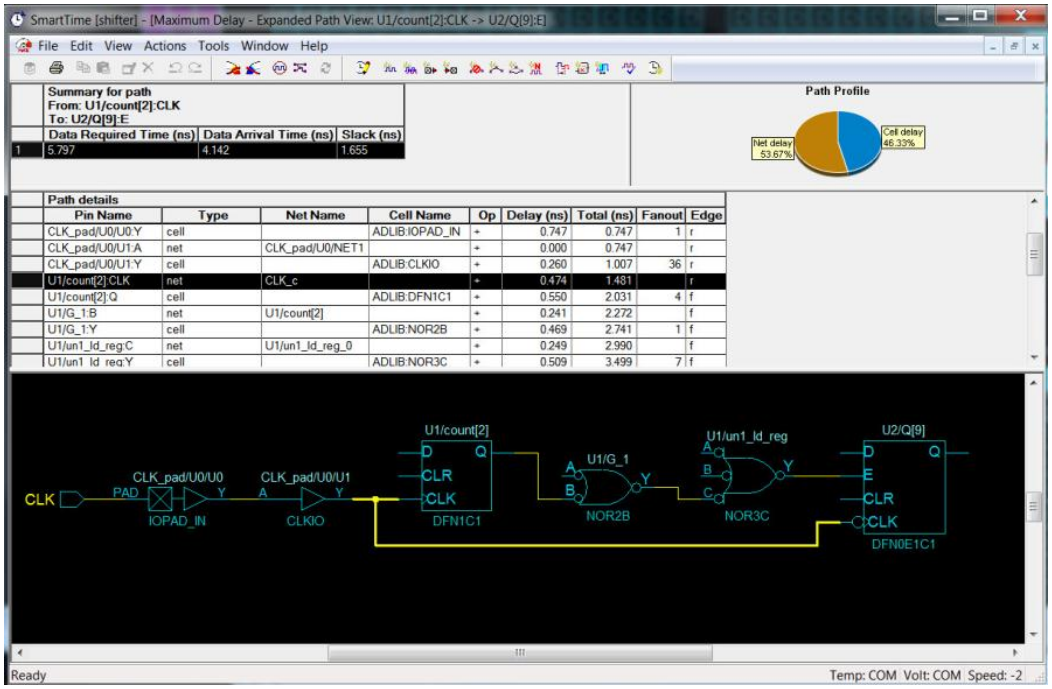

Figure 28 · Cross-Probing a Path in the SmartTime Expanded Path Window

2. In Designer, click **ChipPlanner** to open the tool.
3. In the SmartTime Expanded Path window select an object (such as a net), right-click it and choose **Cross-probe path**, as shown in the figure below.

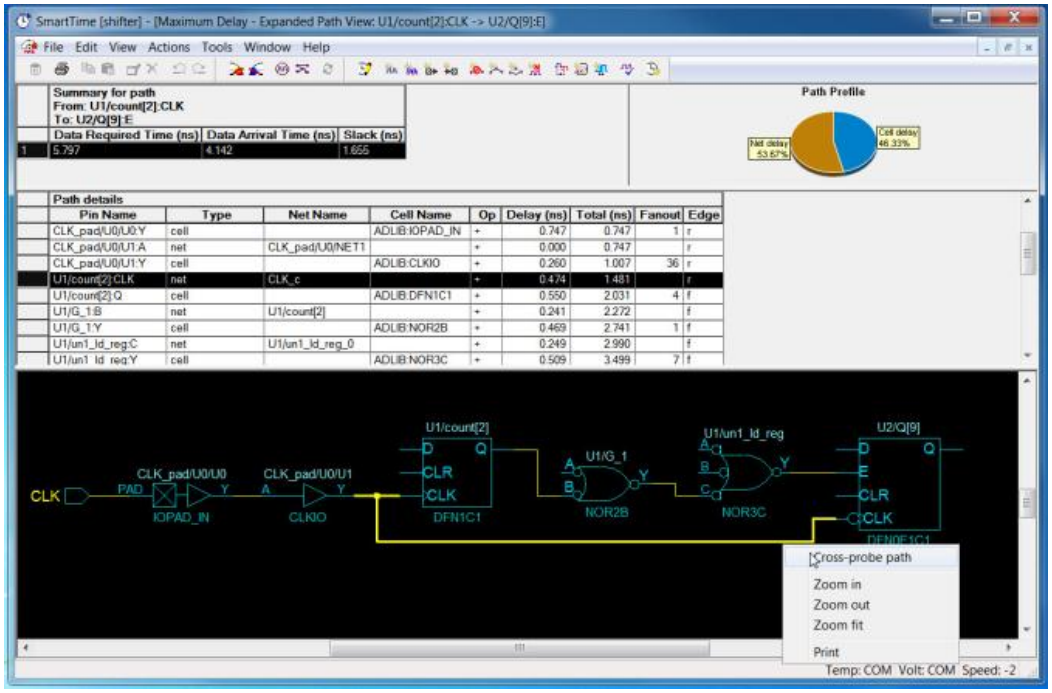

Figure 29 · Cross-probe path in SmartTime

View **ChipPlanner** and notice that the path you selected in SmartTime is highlighted in ChipPlanner, as shown in the figure below. See the ChipPlanner online help for more information on using the tool.

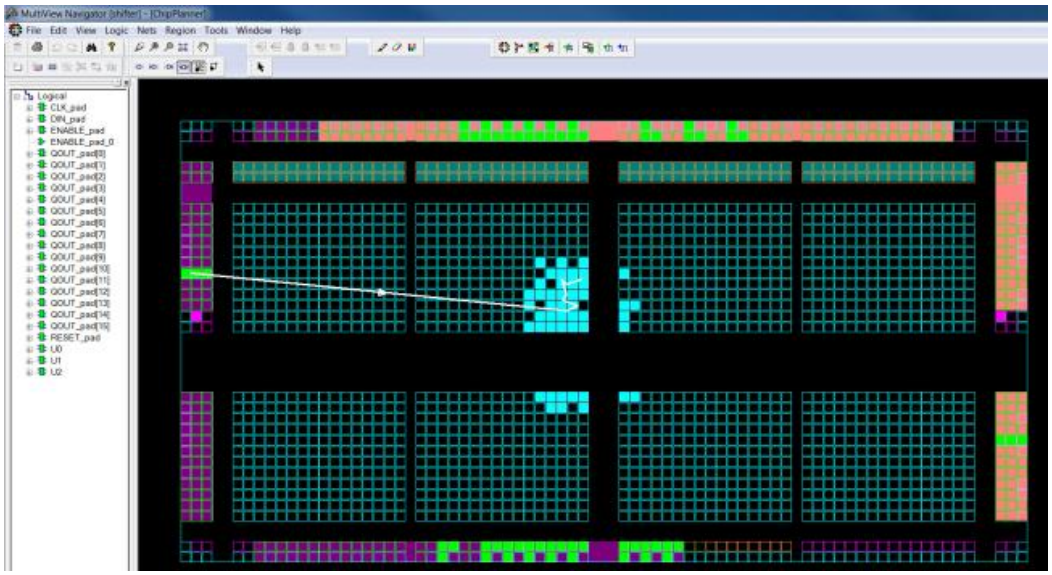

Figure 30 · Cross-Probe Path in ChipPlanner

4. Close ChipPlanner to continue.

Generate a Timing Report - Design Uses Both Clock Edges

Timing reports can be generated from SmartTime. Timing reports enable you to quickly determine if there are any timing problems. The timing report lists the following information:

- Design information including device, speed grade and operating conditions.
- Design performance summary (maximum frequency, external setup and hold, minimum and maximum clock-to-out)
- Clock domain details.
- Inter clock domain details.
- Pin to pin timing

The timing report can be printed and saved.

To generate a Timing Report:

1. In SmartTime from the **Tools** menu, choose **Reports > Report Paths** to open the Timing Report Options Dialog box, as shown in the figure below.

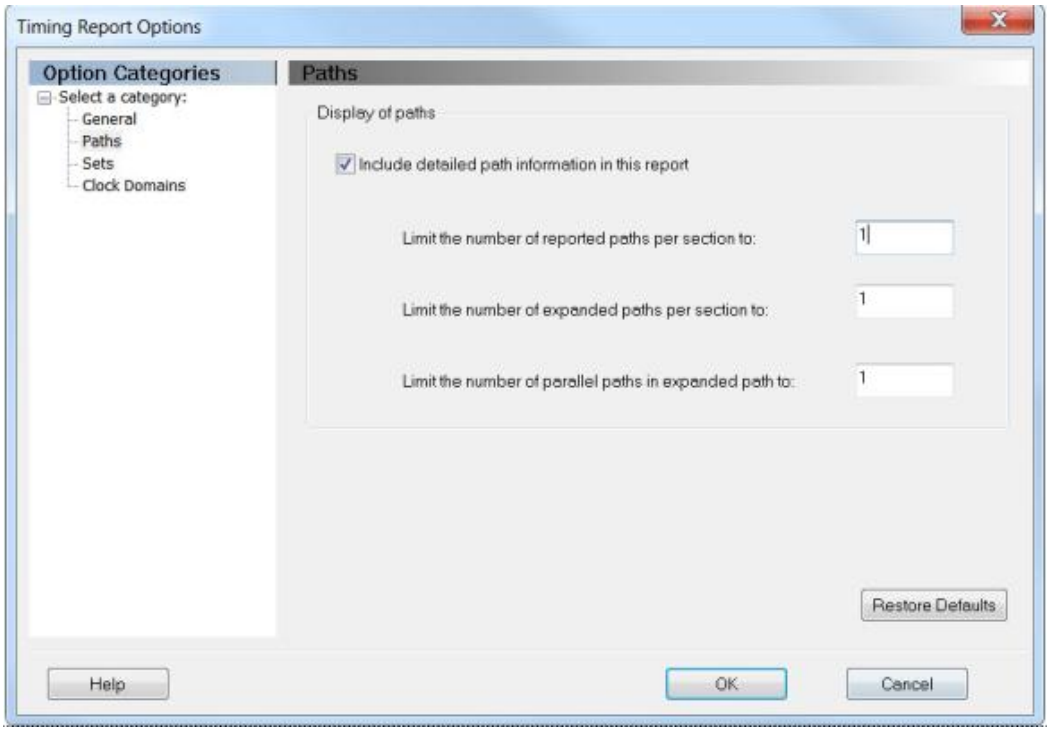

Figure 31 · Timing Report Options Dialog Box

2. Click the **Paths** category. Limit the number of reported paths to **1**, and click **OK**. The timing report opens in a new window, as shown in the figure below.

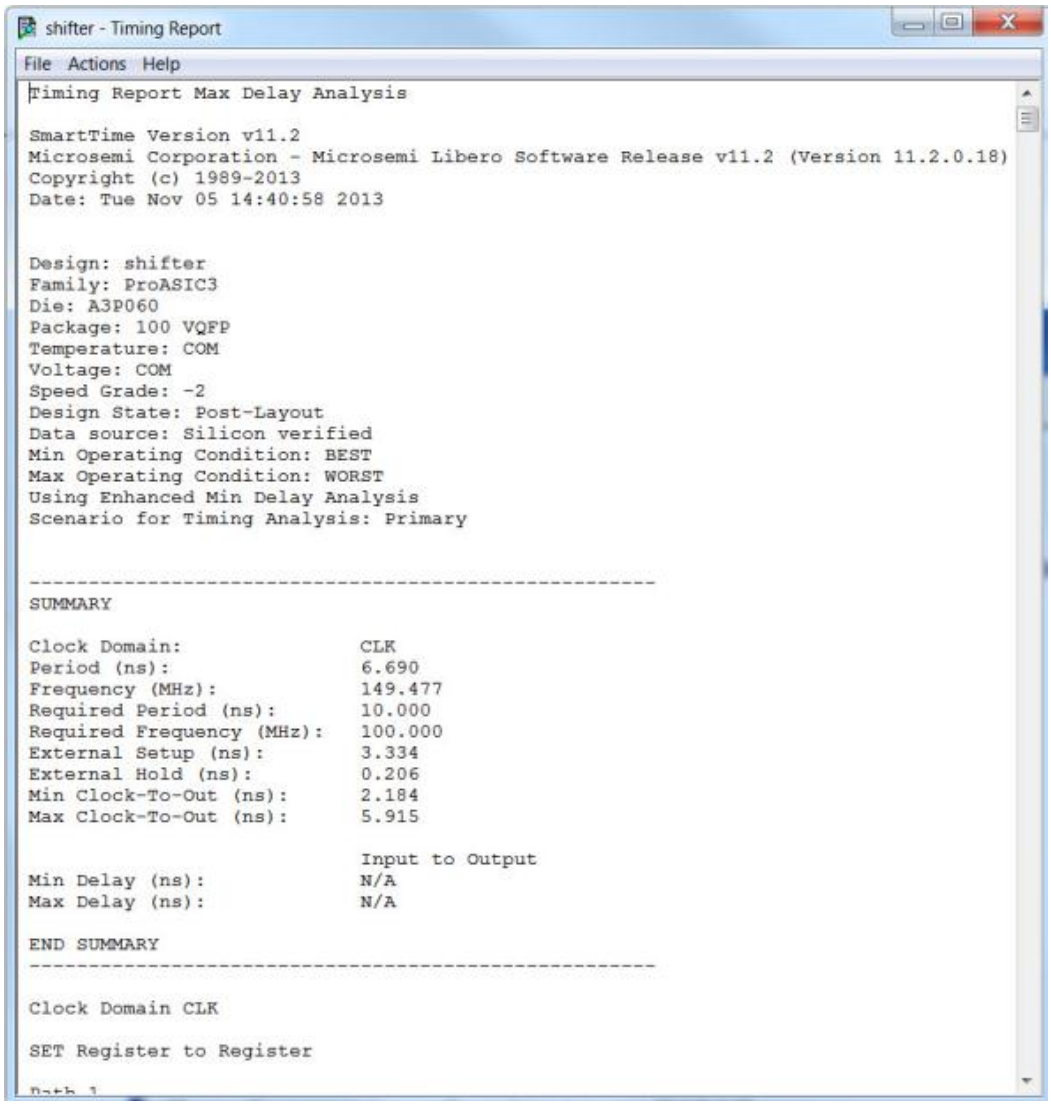

Figure 32 · Timing Report for shifter

The timing report contains the following sections:

- Header
- Summary
- Clock domain details for CLK and expanded path information
- External setup information
- Clock to output delay information

3. Save the timing report as shifter_timing.rpt and close the report window.
4. Close SmartTime and Designer.

16-Bit Binary Counter Example

This example describes how to enter a clock constraint, input delay and output delay constraints for the 16-bit counter pictured in the figure below. You will import an SDC file with a clock constraint of 200 MHz and add input delay constraints of 8 ns and an output delay constraint of 5 ns using SmartTime . After routing the design you will analyze the timing and set multi-cycle path constraints to determine the maximum operating frequency.

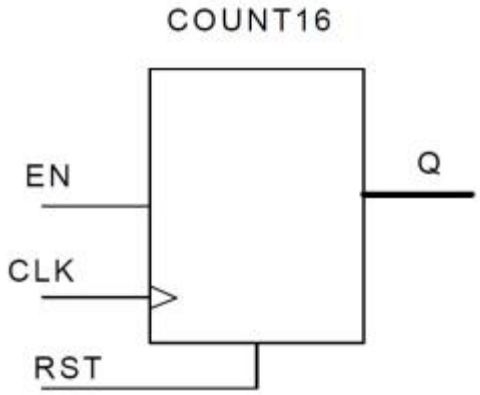

Figure 33 · 16-Bit Counter Design

Set Up Your 16-Bit Binary Counter Example Design Project

1. Open Libero and create a new project (from the **Project** menu, choose **New Project**).
2. Name the project **Counter16** and set the project location according to your preferences. Enter the following values for your new project:

- **Family**: ProASIC3
- **Die**: A3P060
- **Package**: 100 VQFP
- **Speed**: -2
- **Die Voltage**: 1.5 V

Import the 16-Bit Binary Counter Example Design Source File

You must import the count16.edn file into your design for this tutorial. Download the design files from the Microsemi website.

To import the EDN file:

1. From the **File** menu, choose **Import > Others**.
2. Choose **EDIF Netlists** from the file type dropdown list in the Import Files dialog box.
3. Browse to the location of the **counter16.edn** file and select it. Click **Open** to import the file.
4. Verify that the file appears in your project, as shown in the figure below.

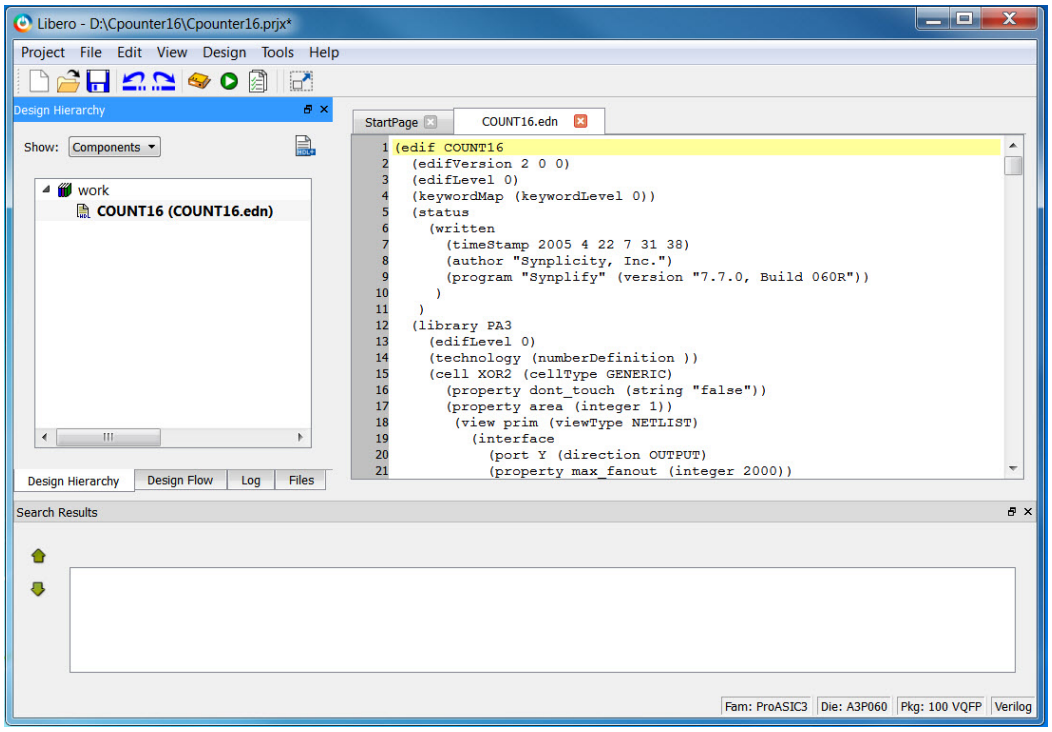

Figure 34 · COUNT16 (COUNT16.edn) in the Design Hierarchy Window

Import a Timing Constraint File

The SDC file contains a Timing Constraint of 5.714 ns for the CLK of the COUNT16 design.

To import the Timing Constraint:

1. From the **File** menu, choose **Import > Timing Constraint (SDC) Files**.
2. Navigate to the folder that contains the file COUNT16.sdc. Click to select it and click Open.
3. A pop-up dialog appears to ask if you want to organize the constraint files for your current root (COUNT16). Click **Yes** to continue.
4. In the Libero SoC Files window, check that the COUNT16.sdc file appears in the constraint directory and that COUNT16.edn appears in the synthesis directory, as shown in the figure below.

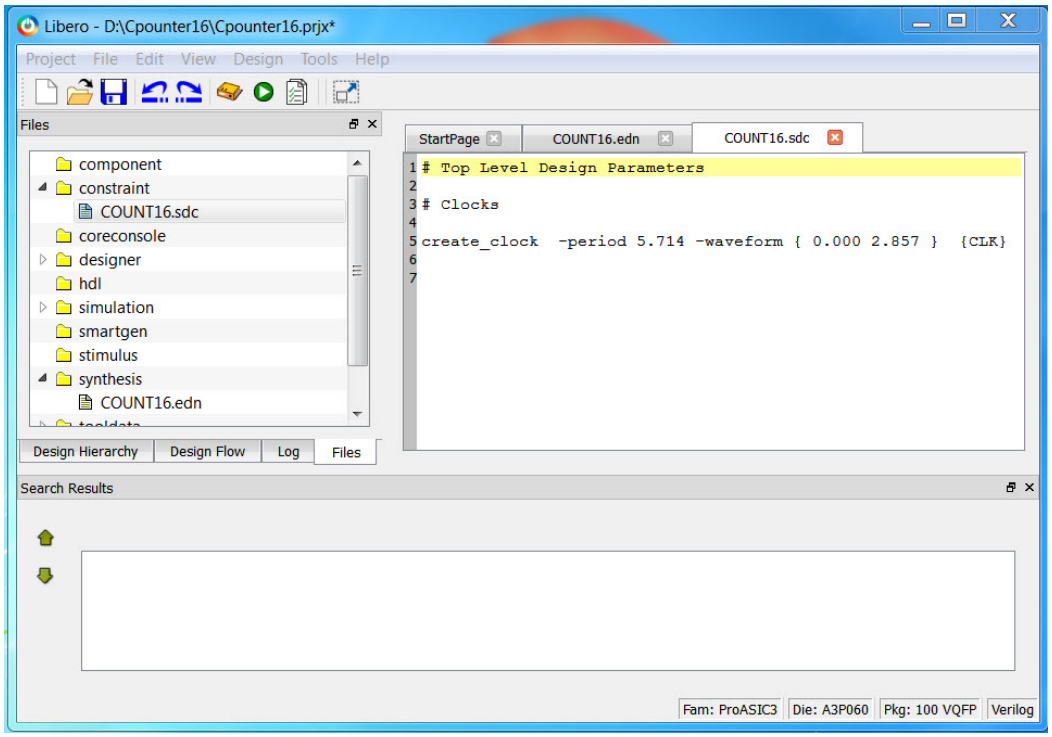

Figure 35 · COUNT16.edn and COUNT16.sdc in the Libero SoC File Window

5. In the Design Flow window, right-click **Create/Edit Timing Constraint** and choose **Open Interactively**. Designer opens and runs Compile with the default settings. After Compile is complete the Compile button in Designer turns green and the SmartTime Constraints Editor opens.
6. Expand **Requirements** and click **Clock**. Notice the CLK Constraint of 5.714 ns. The File column lists the SDC file you have imported as the source of the Constraint, as shown in the figure below.

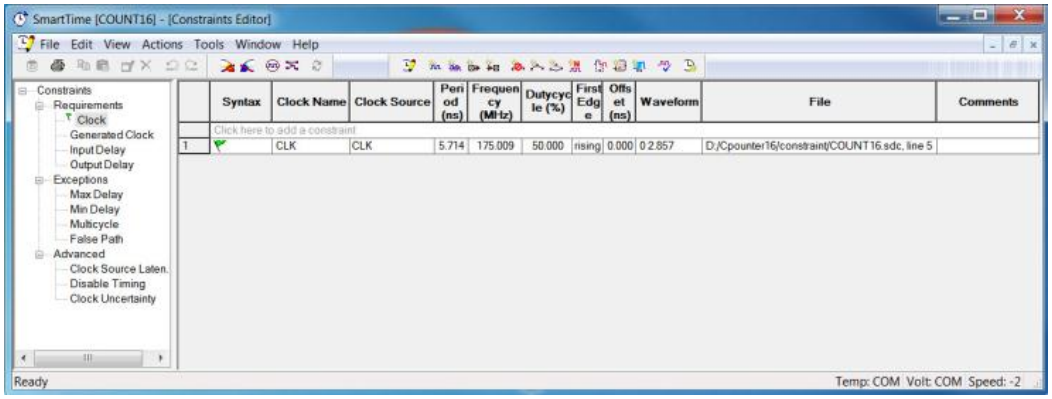

Figure 36 · SmartTime Constraint Editor with SDC Clock Constraint

Add an Input Delay Constraint

Input Delay is part of the path delay budgeting. It makes allowances for delays external to the FPGA so that the external setup requirements to the FPGA can be met. If external setup requirements are not met, the design may not work on the board.

To add an input delay constraint for the EN and RST ports:

1. From the **Actions** menu, choose **Constraint > Input Delay**. The Set Input Delay Constraint dialog box opens, as shown in the figure below.

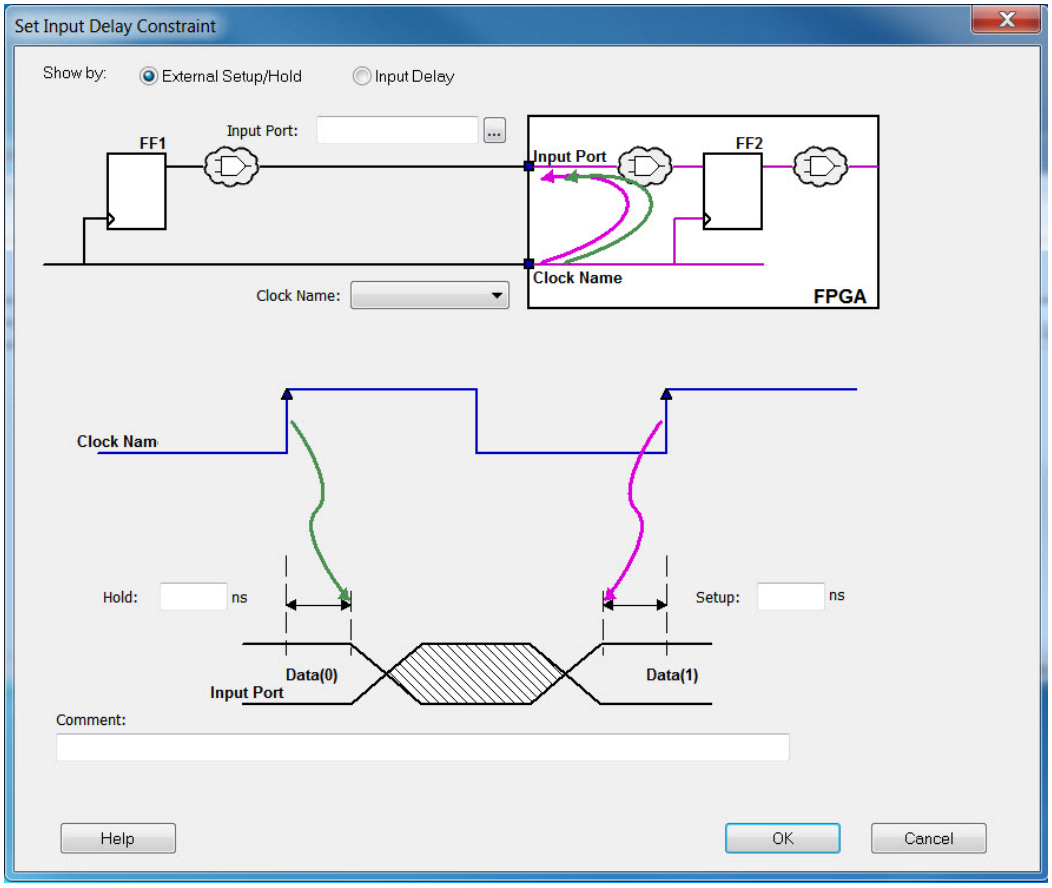

Figure 37 · Set Input Delay Constraint Dialog Box

2. Click **Show by: External/Setup Hold**.
3. Select the Input port for the input delay constraint. Click the **Browse** button to open the Select Ports for Input Delay dialog box.
4. Select the ports **EN** and **RST** and click **Add** to move the pins to Assigned Pins list (as shown in the figure below). Click **OK** to continue.

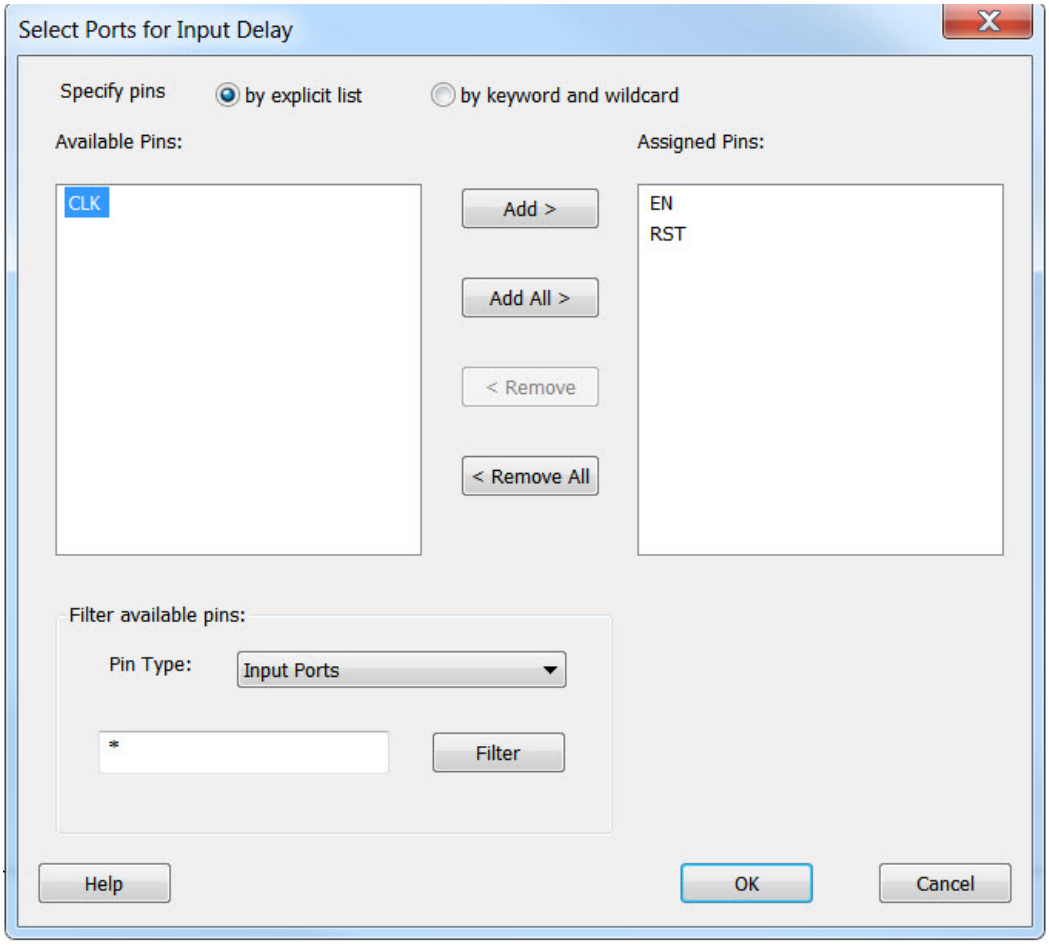

Figure 38 · Select Input Ports EN and RST

5. Enter the following values in the **Set Input Delay Constraint** dialog box (as shown in the figure below):

- **Clock Port**: Select CLK from the drop down menu.
- **Hold**: 1 ns
- **Setup**: 0.5 ns

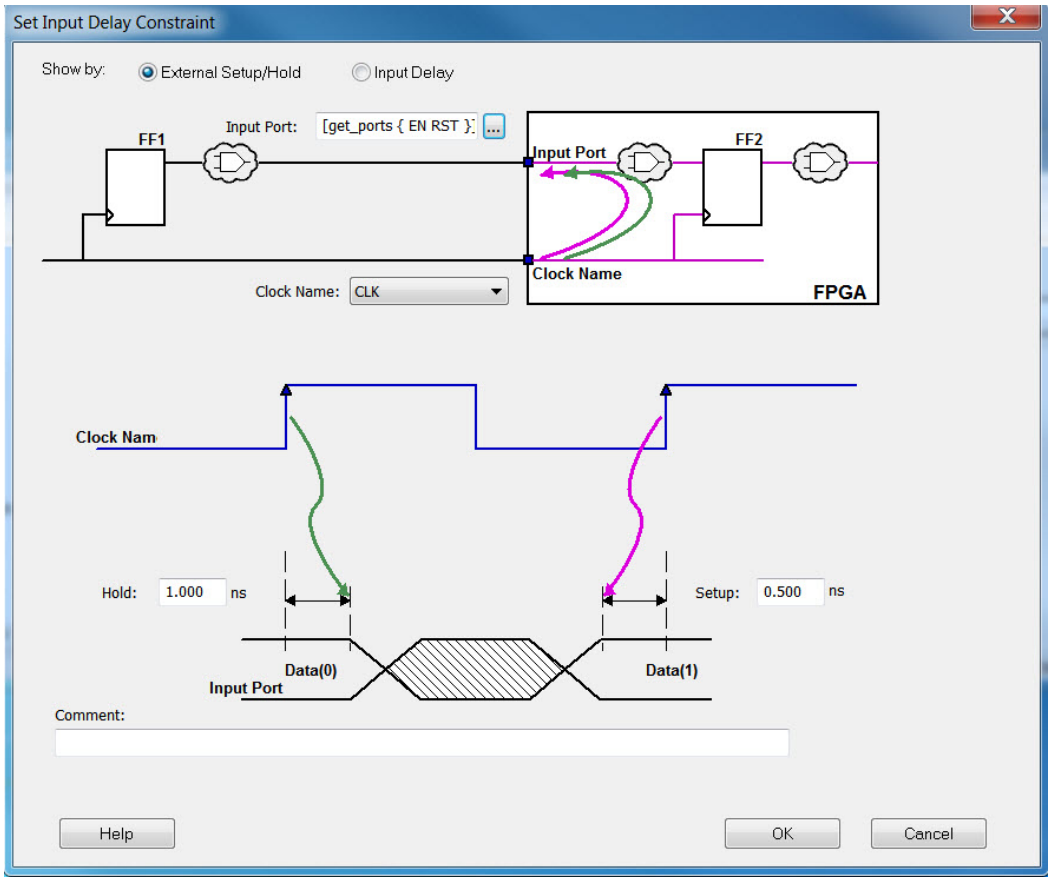

Figure 39 · Select Input Ports and Add a Delay Constraint

6. Click **OK** to continue.

Your new Input Delay constraints are visible in the SmartTime Constraints Editor, as shown in the figure below. Notice that the editor displays the external setup/hold requirement.

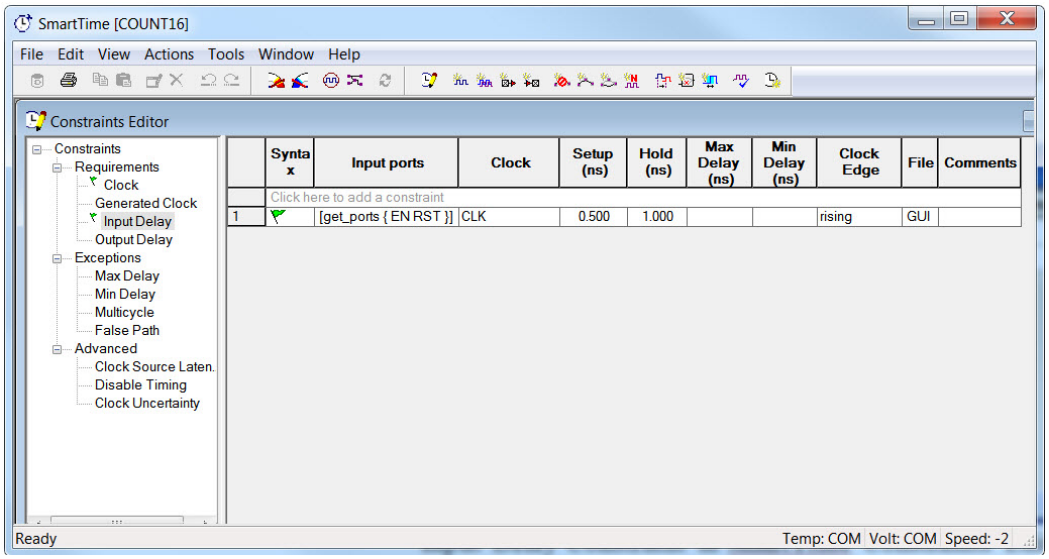

Figure 40 · Input Delay in the SmartTime Constraints Editor

Add an Output Delay Constraint

Output Delay is part of the path delay budgeting. It makes allowances for delays external to the FPGA for the output ports of the design. If external output delay requirements are not met, the design may not work on the board.

To add an output delay constraint:

1. From the **Actions** menu, choose **Constraint > Output Delay**. The Set Output Delay Constraint dialog box opens, as shown in the figure below.
2. Click **Show by: Output Delay**.

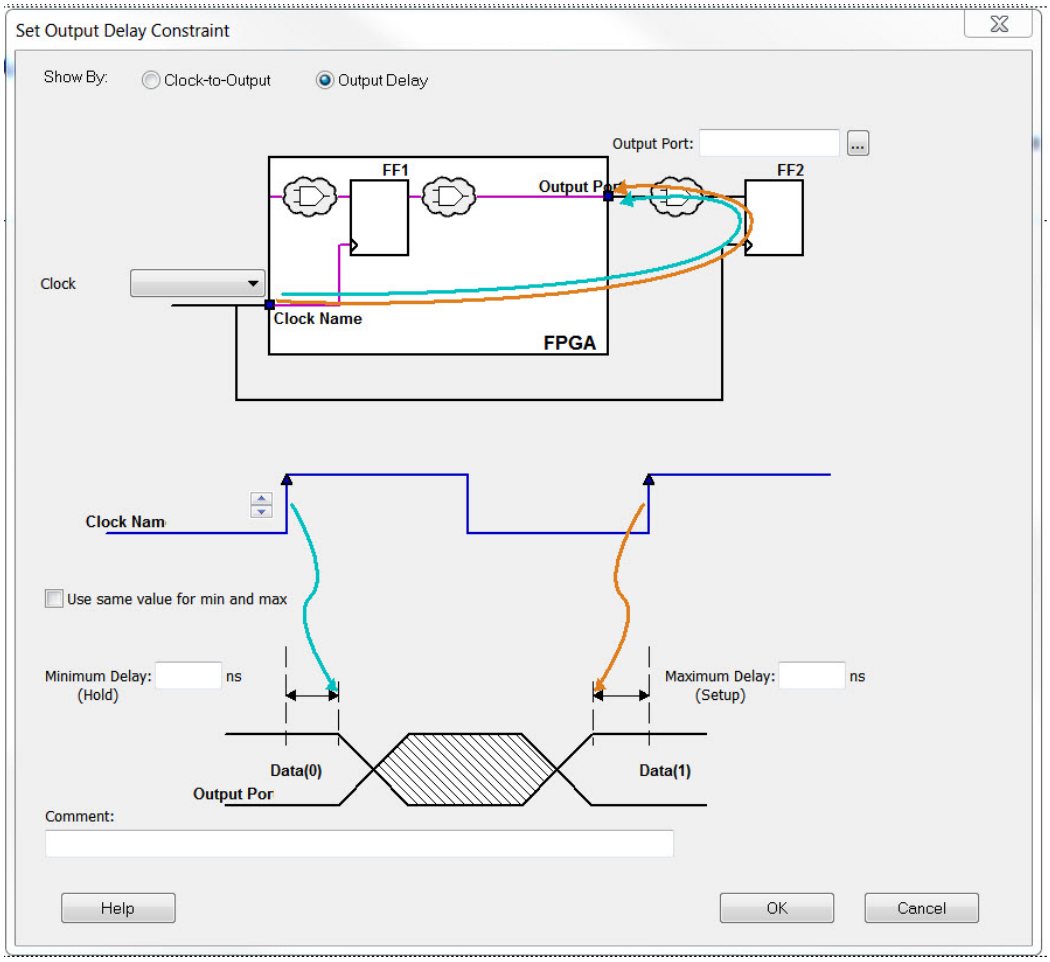

Figure 41 · Set Output Delay Dialog Box

3. Click the **Browse** button to select the ports for the Output Delay Constraint. The Select Ports for Output Delay dialog box appears, as shown in the figure below. Click **Add All** to add all ports to the Assigned Pins list. Click **OK** to continue.

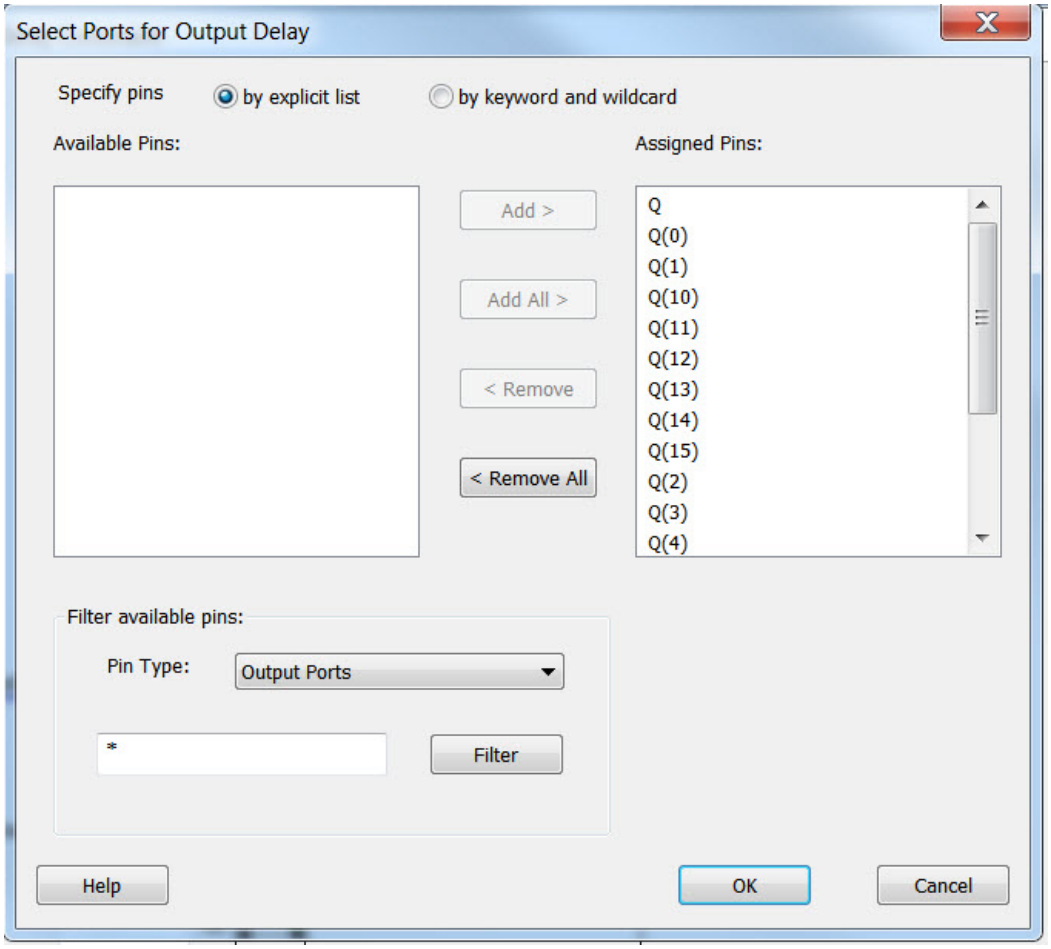

Figure 42 · Select Output Ports and Add Output Delay Constraints

4. Enter the following values in the Set Output Delay Constraint dialog box (as shown in the figure above):

- **Clock Port**: Select **CLK** from the drop down menu
- Enable **Use same value for min and max**
- **Maximum Delay (Setup)**: 1.25 ns

5. Click **OK** to continue. The Output Delay constraint appears in the SmartTime Constraints Editor, as shown in the figure below.

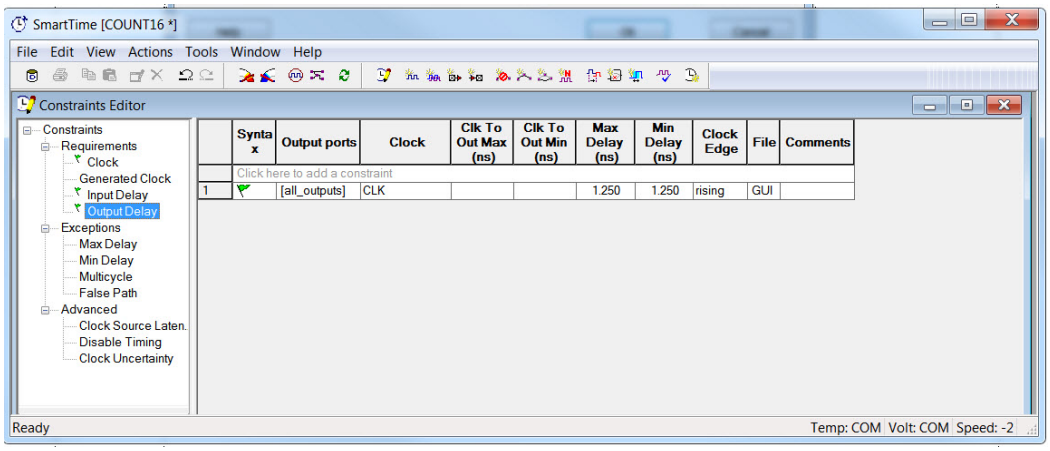

Figure 43 · SmartTime Constraints Editor with Output Delay Constraint

6. From the **File** menu, choose **Commit** to save your changes.
7. From **File** menu, choose **Exit** to close SmartTime.

Place and Route the 16-Bit Binary Counter Design

To run Layout on the design 'Counter16':

1. In Designer, click **Layout** .
2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings. Click **OK** to continue. The Layout button in Designer turns green when Layout has completed successfully.

Using Filters and Creating Analysis Sets - 16-Bit Binary Counter Example

Filters can be used and saved to display analysis sets in the Maximum Delay Analysis window and the Minimum Delay Analysis window.

To create a filter:

1. When Layout is complete, click **Timing Analyzer** in Designer to open the SmartTime Timing Analyzer.
2. Select the **Register to Register path** in the Maximum Delay Analysis View. Enter the following in the Filter fields (as shown in the figure below) then click **Apply Filter**:

From: Q[0]:CLK

To: *:D

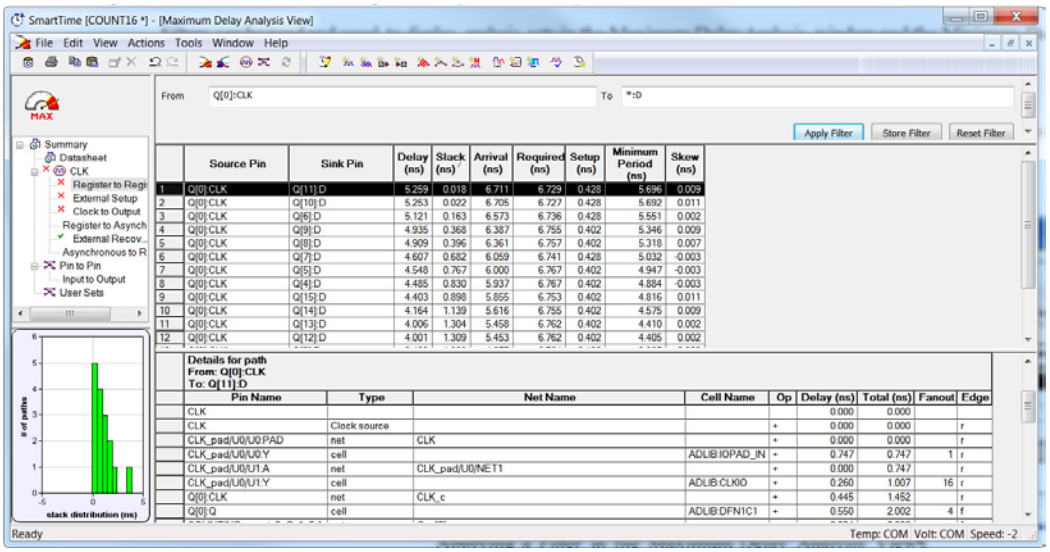

Figure 44 · Applying a Filter in the Maximum Delay Analysis View

3. Click **Store Filter** to save the filter. Enter **Q0_filter** in the Store Filter as Analysis Set dialog box. The set will be visible in the Maximum Delay Analysis View under Register to Register, as shown in the figure below.

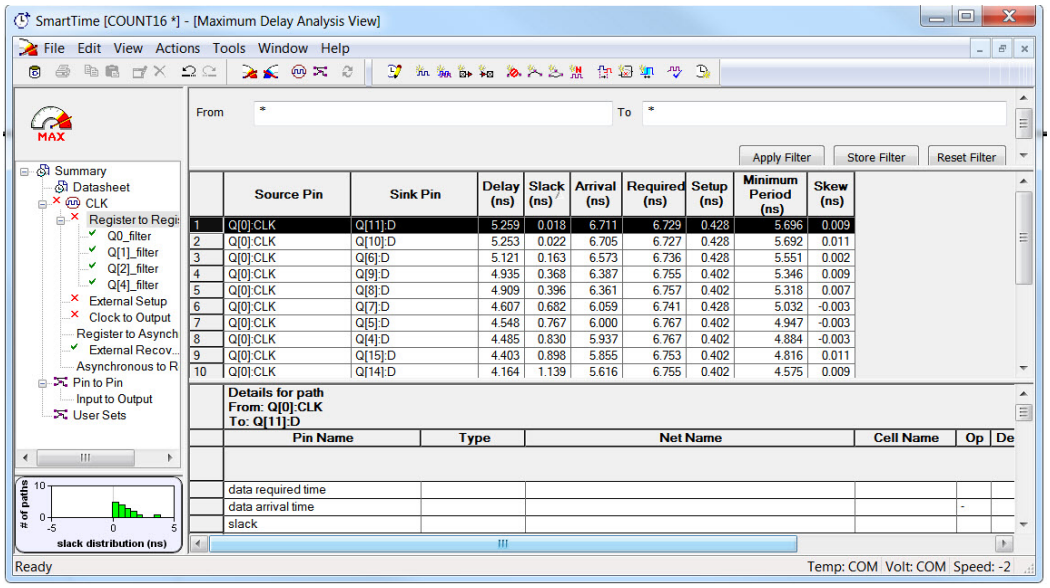

Figure 45 · Store Filter as Analysis Set

4. Click the **Reset Filter** button.
5. Repeat the steps above using the following filter values to create the sets listed in the table below.

From	To	Name
Q[1]:CLK	*:D	Q1_filter
Q[2]:CLK	*:D	Q2_filter
Q[3]:CLK	*:D	Q3_filter
Q[4]:CLK	*:D	Q4_filter

The path sets appear under Register to Register in the Maximum Delay Analysis View, as shown in the figure above.

6. Close SmartTime, Designer, and Libero SoC.

False Path Constraints

This section describes how to enter false path constraints in SmartTime. You will import an EDIF netlist from the design shown below. After routing the design you will analyze the timing and set false path constraints and observe the maximum operating frequency in the SmartTime Timing Analysis window.

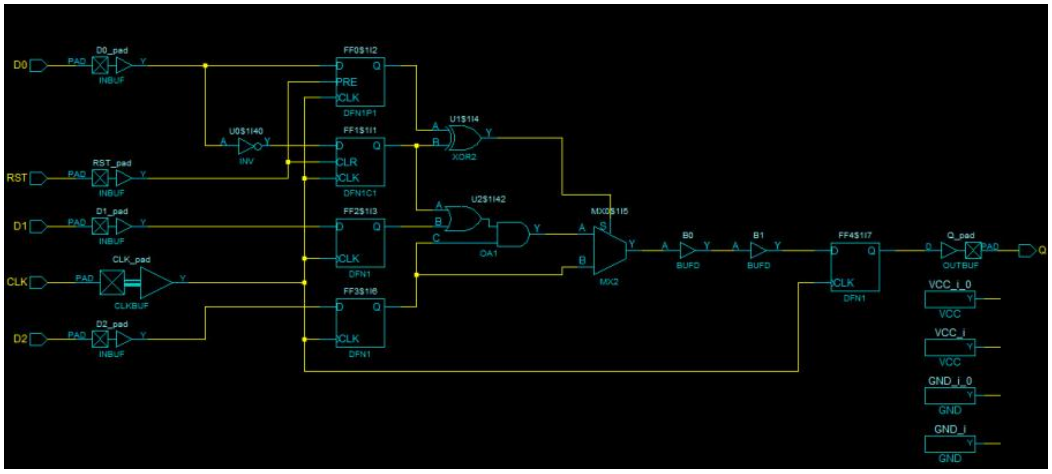

Figure 46 · Example Design with False Paths

Set Up Your False Path Example Design Project

1. Open Libero and create a new project (from the **Project** menu, choose **New Project**).
2. Name the project **FALSE_PATHS** and set the project location according to your preferences. Enter the following values for your new project:

- **Family**: ProASIC3
- **Die**: A3P060
- **Package**: 100 VQFP
- **Speed**: STD
- **Die Voltage**: 1.5 V

Import the FALSE_PATH File and Add A Constraint

You must import the FALSE_PATH design file into your design for this tutorial. Download the design files from the Microsemi website.

To import and constrain the design:

1. From the **File** menu, choose **Import > HDL Source Files**.
2. Browse to the location of the **FALSE_PATHS** design file (Verilog or VHDL) file and select it. Click **Open** to import the file.
3. Verify that the file appears in your project, as shown in the figure below.

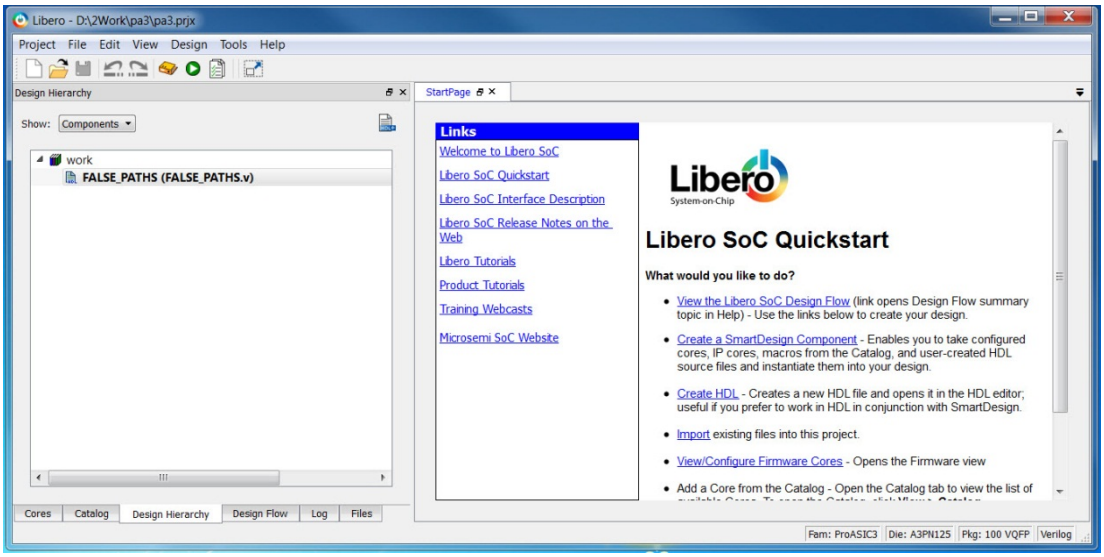

Figure 47 · FALSE_PATHS Design in Design Hierarchy

4. In the Design Flow window double-click **Compile** to Compile with default settings. A green check mark appears next to Compile to indicate that it has completed successfully.
5. Click to access the **Design Flow** window in Libero SoC. Right-click **Create/Edit Timing Constraints** and choose **Open Interactively**. Designer opens along with the SmartTime Constraint Editor. Minimize Designer.
6. In the SmartTime Constraints Editor, enter a constraint for the clock source (**CLK**) of **100 MHz** (50% duty cycle), as shown in the figure below.

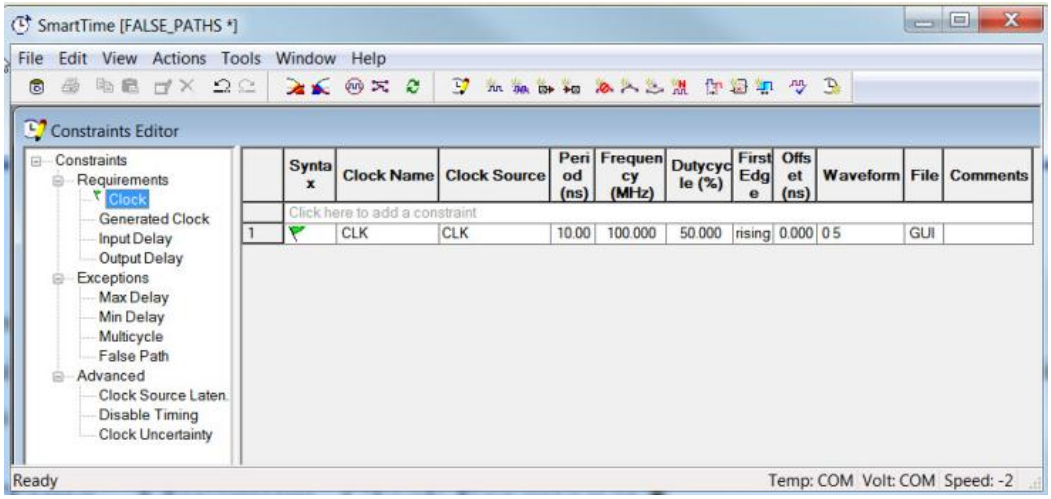

Figure 48 · Clock Constraint of 100 MHz in FALSE_PATHS

8. Commit your changes and close SmartTime.

Place and Route Your FALSE_PATH Design

To run Layout on FALSE_PATH:

1. In Designer, click **Layout** .
2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings. Click **OK** to continue. The Layout button in Designer turns green when Layout has completed successfully.

Timing Analysis - Maximum Clock Frequency

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. Click the **Timing Analyzer** button in Designer to open SmartTime. The Maximum Delay analysis window appears (as shown in the figure below). The Maximum Delay Analysis View displays a summary of design performance and indicates that the design will operate at 188.679 MHz.

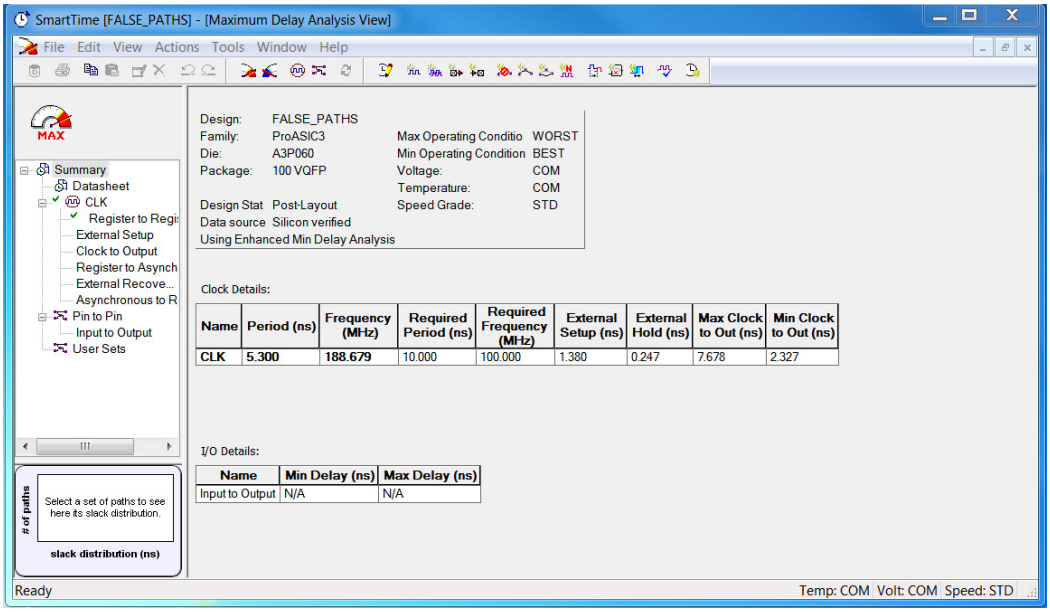

Figure 49 · Maximum Delay Analysis Summary

2. Click the + sign next to CLK to expand the display and show the Register to Register path sets.
3. Select **Register to Register** to display the register-to-register paths. Notice that the slack values are positive.
4. Click to select the first row in the path list. The path is from the clock pin flip flop FF1 to the D input of flip flop FF4. Note that the path goes through the A input of multiplexer MX0.

The design schematic shows that the S input of MX0 will always be logic 1; consequently, all the paths through the A input of MX0 and the S input of MX0 are false paths. You must set a false path on these paths in order to determine the true maximum operating frequency.

5. To set the path from FF1$1I1:CLK to FF4$1I7:D as false, select the row containing this path in the Register to Register path set, right-click and choose **Add False Path Constraint** (as shown in the figure below). The Set False Path Constraint dialog box appears.

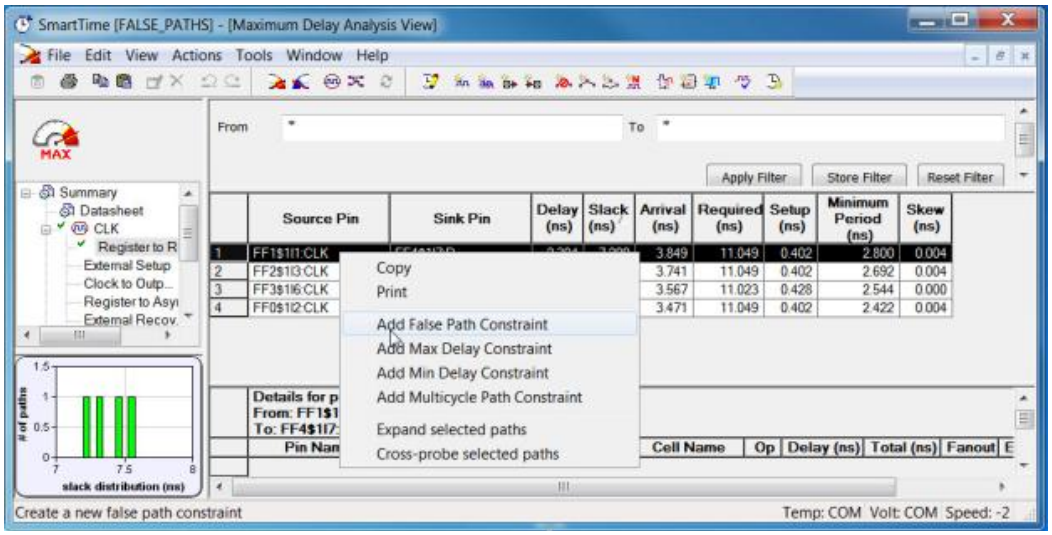

Figure 50 · Right-Click and Choose Add False Path Constraint

6. Click the **Browse** button in the Set False Path Constraint dialog box.
7. In the **Select Through Pins for False Path Constraint** window, select MX0$1I5:A from the list of Available Pins, then click **Add**. Click **OK** to close the dialog box.
8. Click **OK** to close the Set False Path Constraint dialog box.
9. From the **View** menu, choose **Recalculate All** to recalculate the delays.
10. The next longest delay, from: FF1$1I1:CLK to: FF4$1I7:D is also a false path. Repeat the steps above to set a false path constraint from FF1$1I1:CLK to: FF4$1I7:D through MX0$1I5:S, using the values as shown in the table below.

From	To	Through
FF1$1I1:CLK	FF4$1I7:D	MX0$1I5:A
FF1$1I1:CLK	FF4$1I7:D	MX0$1I5:S
FF2$1I3:CLK	FF4$1I7:D	MX0$1I5:A
FF3$1I6:CLK	FF4$1I7:D	MX0$1I5:A
FF0$1I2:CLK	FF4$1I7:D	MX0$1I5:S

11. Open the Constraint Editor and click **False Paths > Exceptions**. The False Path constraints are listed as shown in the figure below.

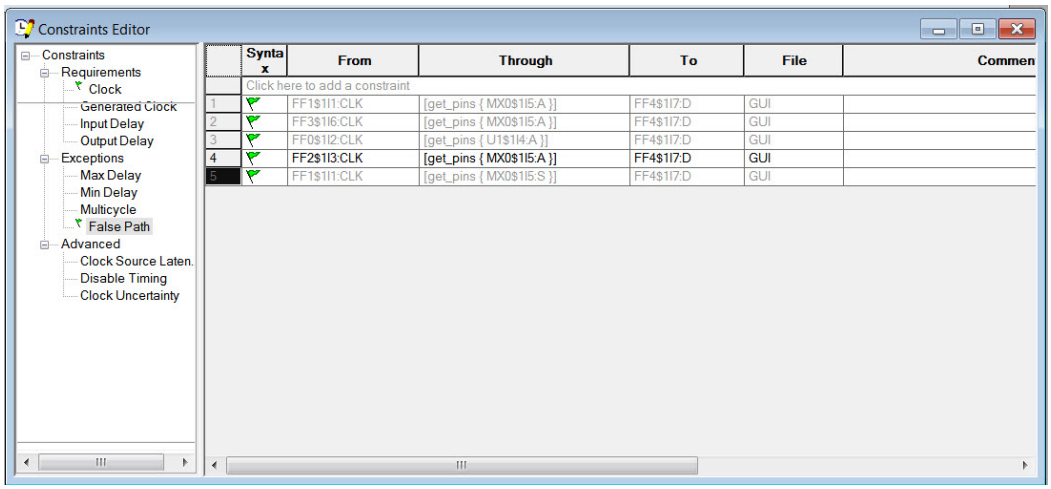

Figure 51 · False Path Constraints in the SmartTime Constraint Editor

12. Recalculate the delays and view the summary in the **Maximum Delay Analysis View**. Note that SmartTime now reports the maximum operating frequency as 232.396 MHz, as shown in the figure below.

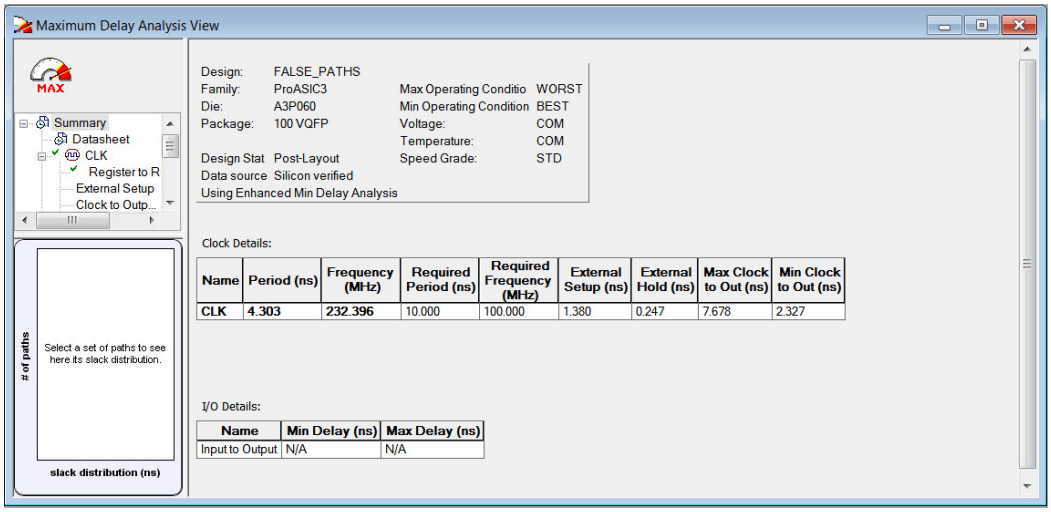

Figure 52 · Maximum Delay Analysis View - Summary

13. Select the **Register to Register** set for CLK. Observe that only one path is visible from F3:CLK to F4:D. This is the only path that propagates a signal (as shown in the figure below).

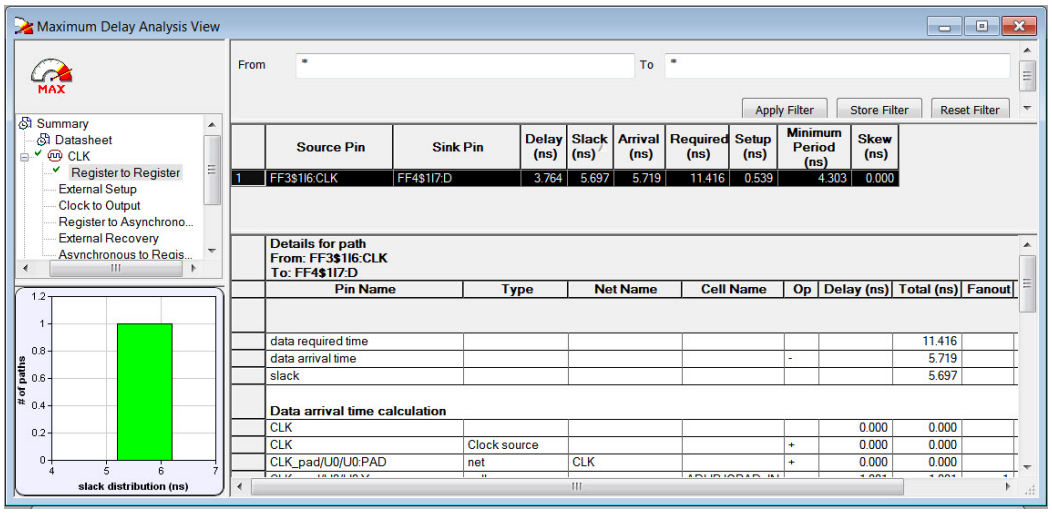

Figure 53 · Maximum Delay Analysis View - Register to Register

14. Close SmartTime and Designer.
15. Close Libero SoC.

Cross Clock Domain Analysis

SmartTime performs inter-clock domain timing checks for designs that contain functional paths that cross two clock domains (the register launching the data and the register capturing the data are clocked by two different clock sources). Accurate specification of both clocks is required to allow a valid inter-clock domain timing check.

SmartTime analyzes each inter-clock domain by determining a common period equal to the least common multiple of the two clock periods.

For setup check, the tightest launch-capture time period is considered to ensure that the data arrives before the capture edge (as shown in the figure below). The hold check verifies that a setup relationship is not overwritten by a following data launch.

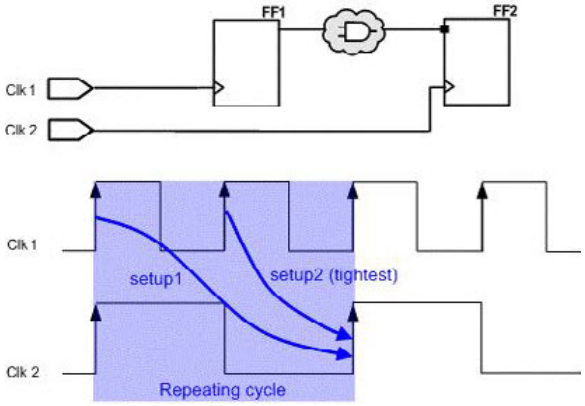

Figure 54 · Tightest Launch - Capture Relation for Setup Check in SmartTime

In this tutorial you will:

1. Create a new Libero project.
2. Import an EDIF netlist for the design shown in the figure below.
3. Enter timing constraints for the two clock domains.
4. Use SmartTime to analyze the inter-clock domain timing.

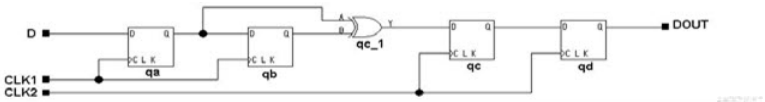

Figure 55 · Inter-Clock Domain Example Design Diagram

Set Up Your Cross Clock Domain Analysis Example Design Project

1. Open Libero and create a new project (from the **Project** menu, choose **New Project**).
2. Name the project **multi_clocks** and set the project location according to your preferences. Enter the following values for your new project:

- **Family**: ProASIC3
- **Die**: A3P060
- **Package**: 100 VQFP
- **Speed**: STD
- **Die Voltage**: 1.5 V

Leave all other fields at their default values.

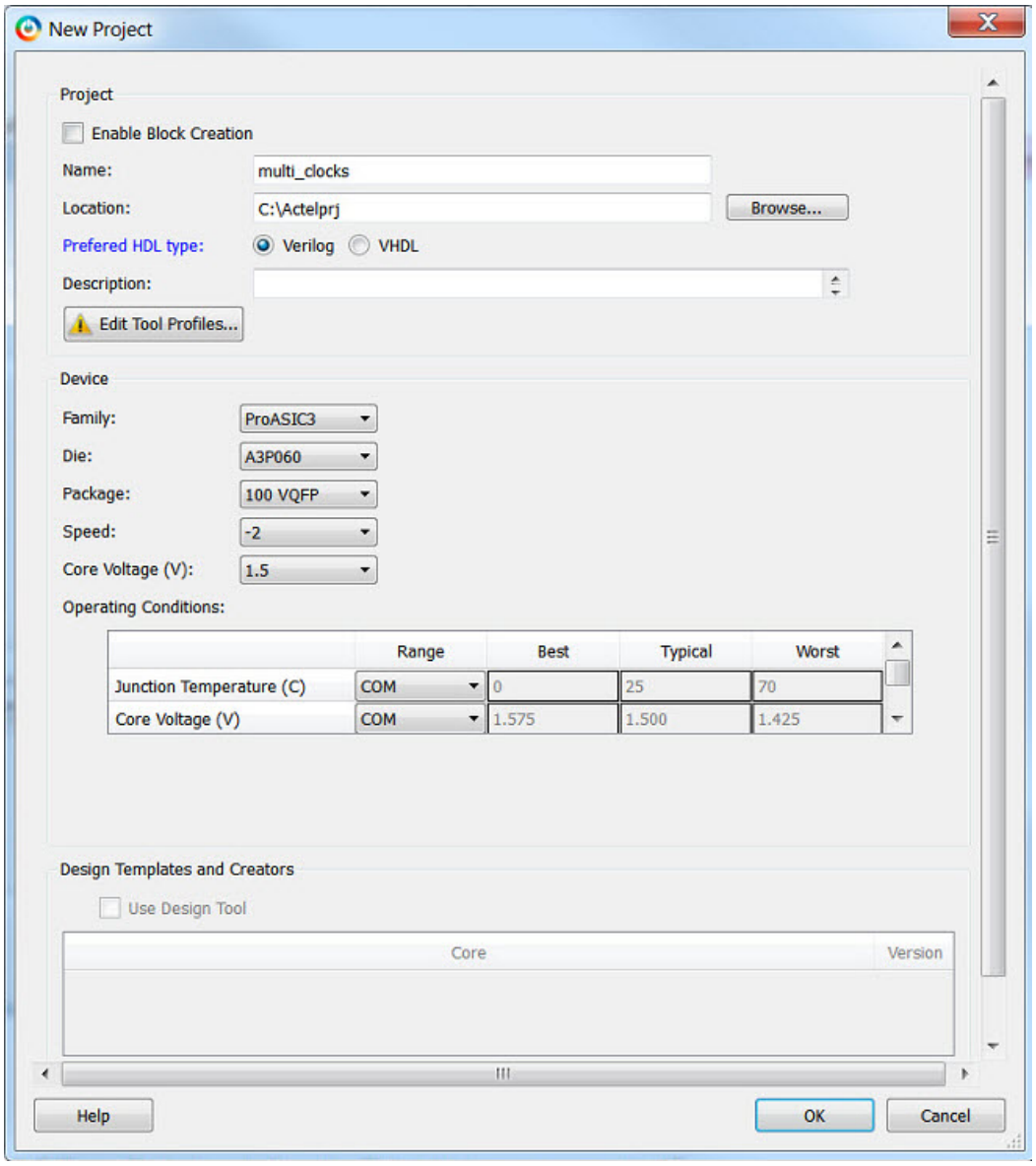

Figure 56 · multi_clocks Project Settings

Import EDN File and Run Compile for Cross Clock Domain Analysis Example

You must import the multi_clocks.edn file into your design for this tutorial. Download the design files from the Microsemi website.

To import and constrain the EDN file:

1. From the **File** menu, choose **Import > Others**.
2. Choose **EDIF Netlists** from the file type dropdown list in the Import Files dialog box.
3. Browse to the location of the **multi_clocks.edn** file and select it. Click **Open** to import the file.
4. Verify that the file appears in your project, as shown in the figure below.

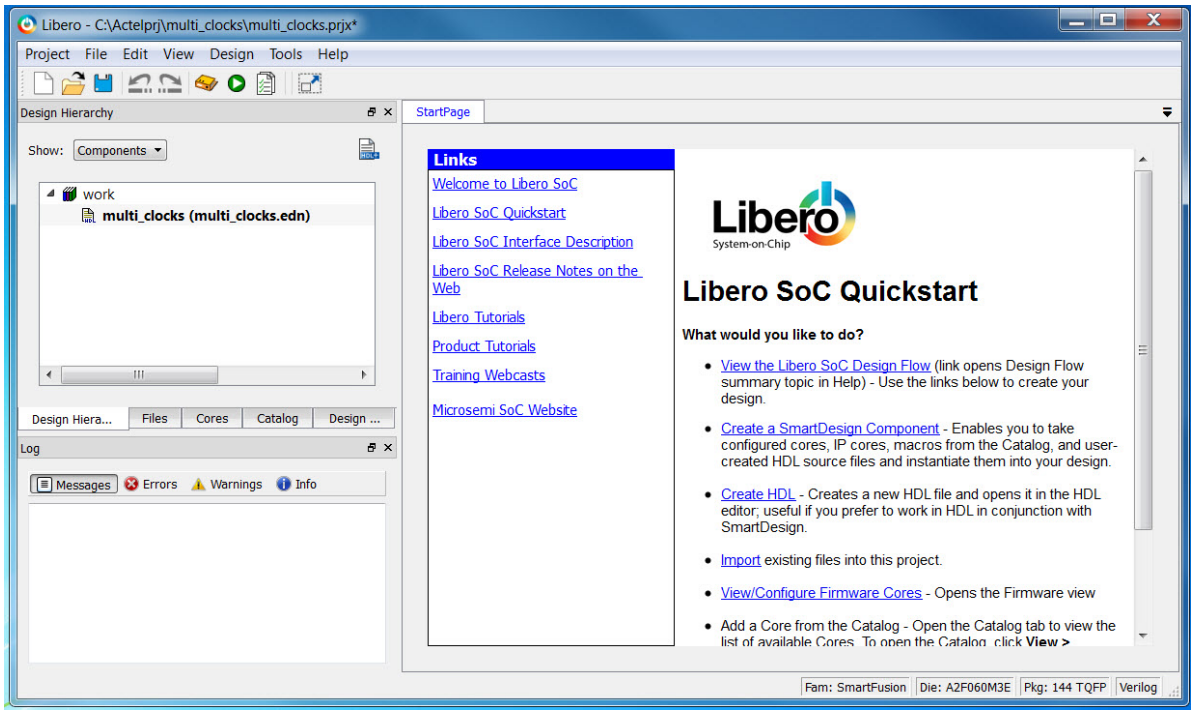

Figure 57 · multi_clocks Design in the Design Hierarchy Window

5. Double-click **Compile** in the Design Hierarchy window to run Compile with default settings. A green check mark appears next to Compile when it has run successfully, as shown in the figure below.

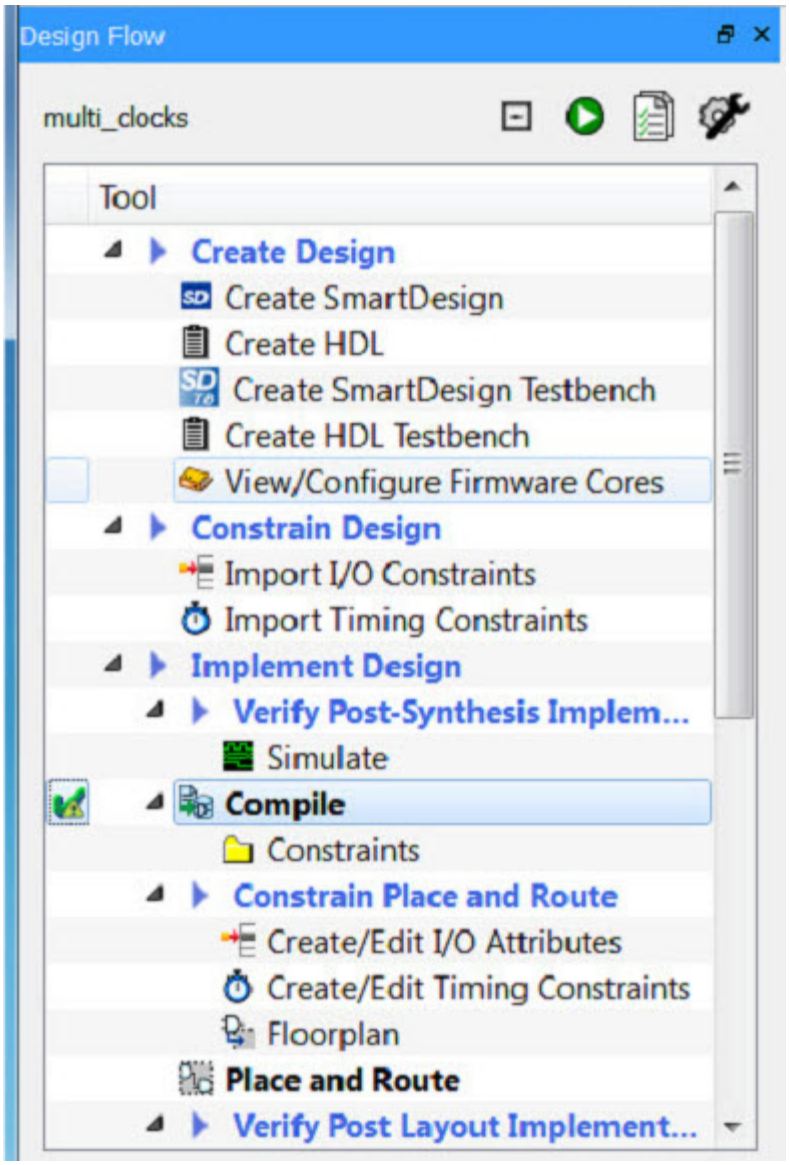

Figure 58 · Design Flow Window - Compile Successful

Enter Timing Constraints for the Cross Clock Domain Analysis Example

To add a clock constraint to your example design:

1. In the Design Flow window, right-click **Create/Edit Timing Constraint** and choose **Open Interactively**. Designer opens and then the SmartTime Constraints Editor opens.
2. Minimize Designer.
3. Use the **Constraints Editor** to enter the following constraints:

- **CLK1**: 250 MHz
- **CLK2**: 100 MHz

4. Verify that your new constraints are listed in the Constraints Editor, as shown in the figure below.

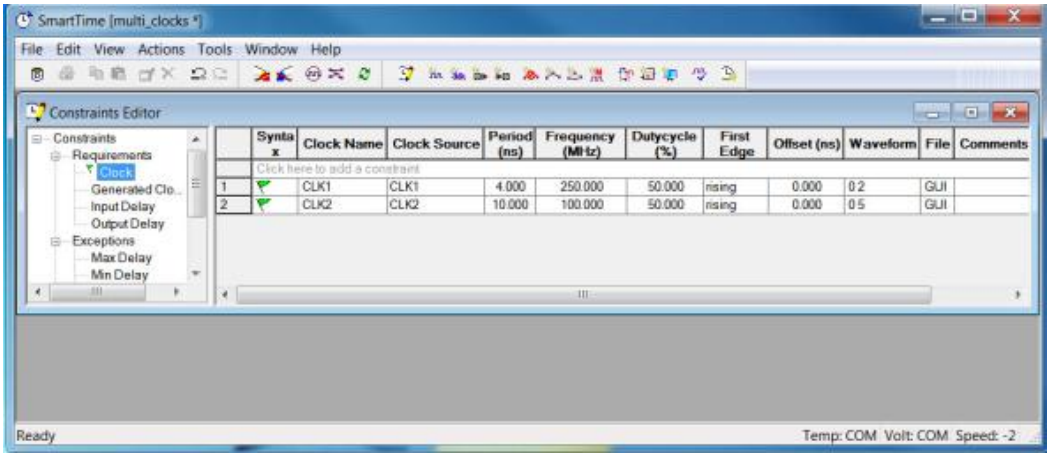

Figure 59 · Clock Constraints in the SmartTime Constraints Editor

5. Click **Commit** to save your constraints.
6. From the **Tools** menu, choose **Options**. Click the checkbox to enable Inter-Clock domain analysis, as shown in the figure below.

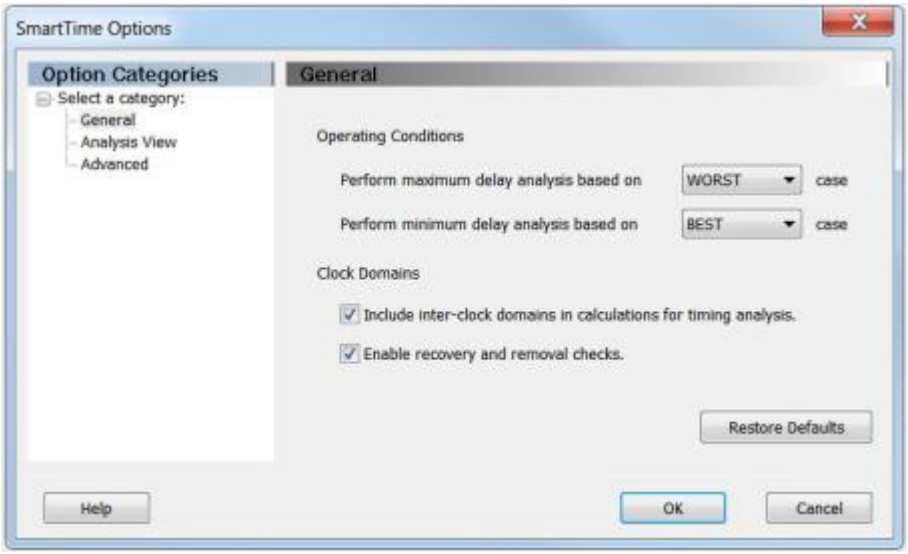

Figure 60 · Inter-Clock Domain Analysis Enabled in the SmartTime Options Dialog Box

Place and Route Your Cross Clock Domain Analysis Example

To run Layout on multi_clocks:

1. View Designer and click **Layout**.
2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings, as shown in the figure below. Click **OK** to continue. The Layout button in Designer turns green when Layout has completed successfully.

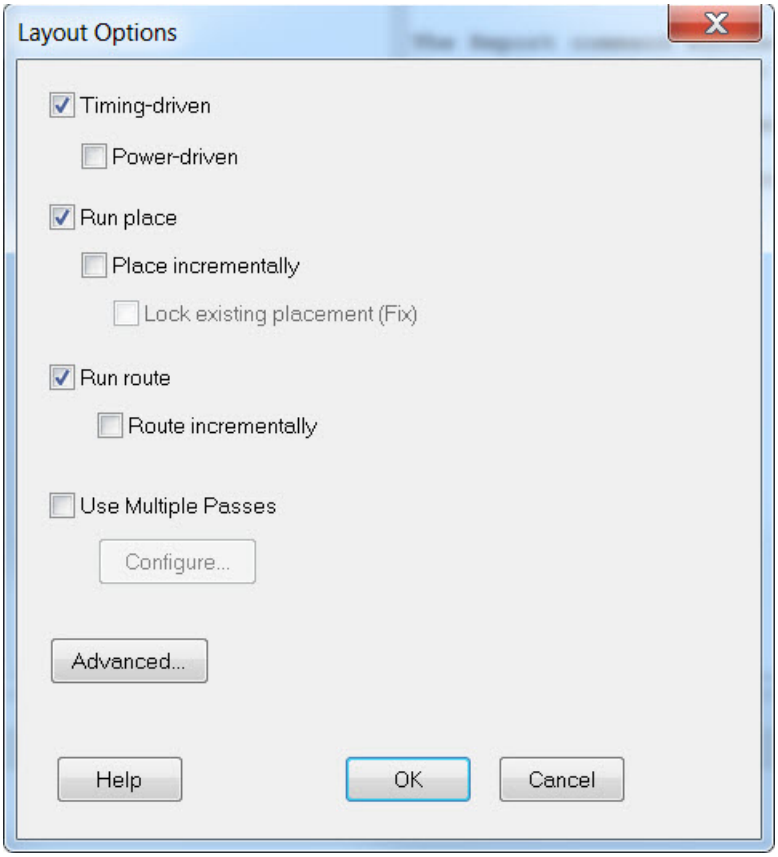

Figure 61 · Layout Options - multi_clocks

Analyze Inter-Clock Domain Timing

Inter-clock domain timing enables you to analyze timing for designs that contain functional paths that cross two clock domains.

To analyze inter-clock domain timing:

1. Click the **Timing Analyzer** button in Designer. SmartTime opens and displays the Maximum Delay Analysis View.
2. Click + to expand the CLK2 paths in the Maximum Delay Analysis View. Click to select the **CLK1 to CLK2** path and observe the inter-clock domain path timing (as shown in the figure below).

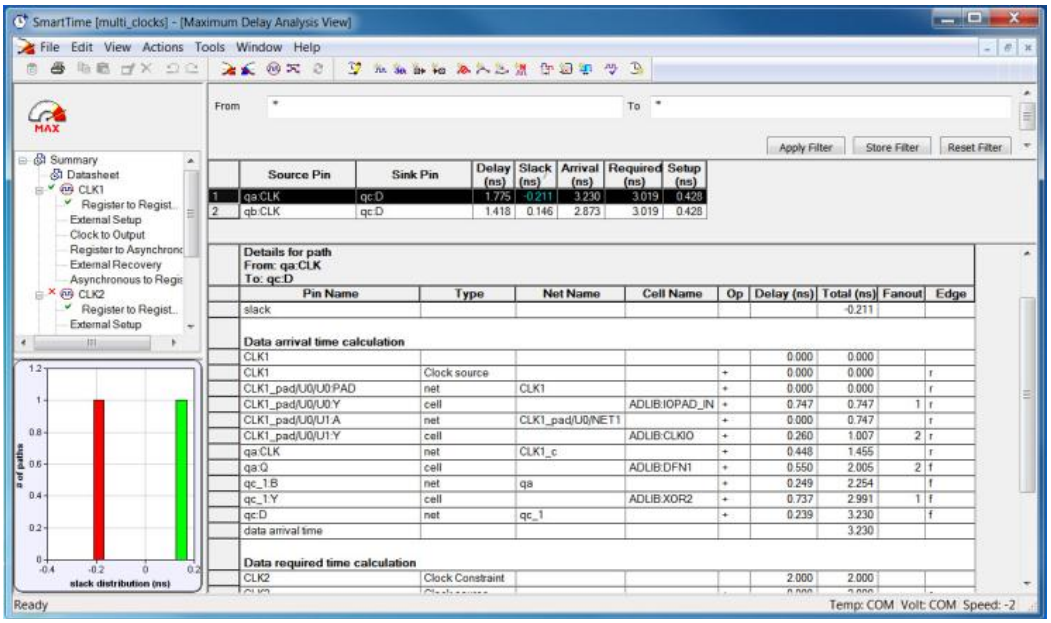

Figure 62 · Maximum Delay Inter-Clock Domain Timing Analysis - multi_clocks Example Design

The Paths list shows the detailed timing analysis. The longest reported path is from qa:clk to qc:d, as shown in the figure below. This path has a negative slack of 0.211 ns. The clock edges used in the calculation are shown in the timing diagram below.

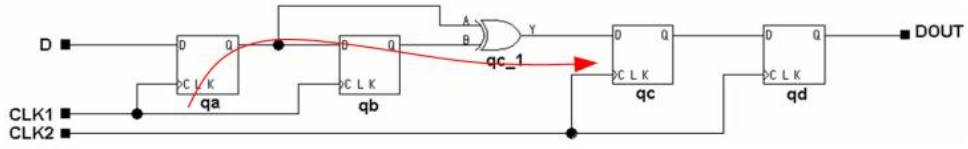

Figure 63 · Longest Reported Inter-Clock Domain Path - multi_clocks Example Design

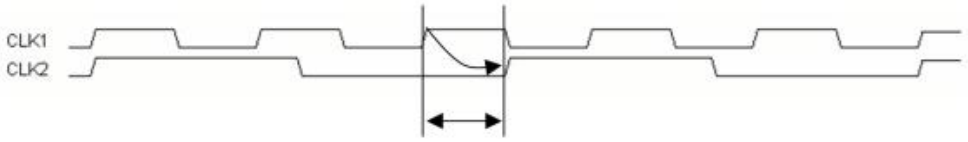

Figure 64 · Clock Edges Used in Inter-Clock Domain Max Delay Calculation - multi_clocks Example Design

3. From the **Tools** menu, choose **Timing Analyzer > Minimum Delay Analysis**.
4. Expand the CLK2 paths in the Minimum Delay Analysis View. Click to select the **CLK1 to CLK2** path and observe the inter-clock domain path timing, as shown in the figure below.

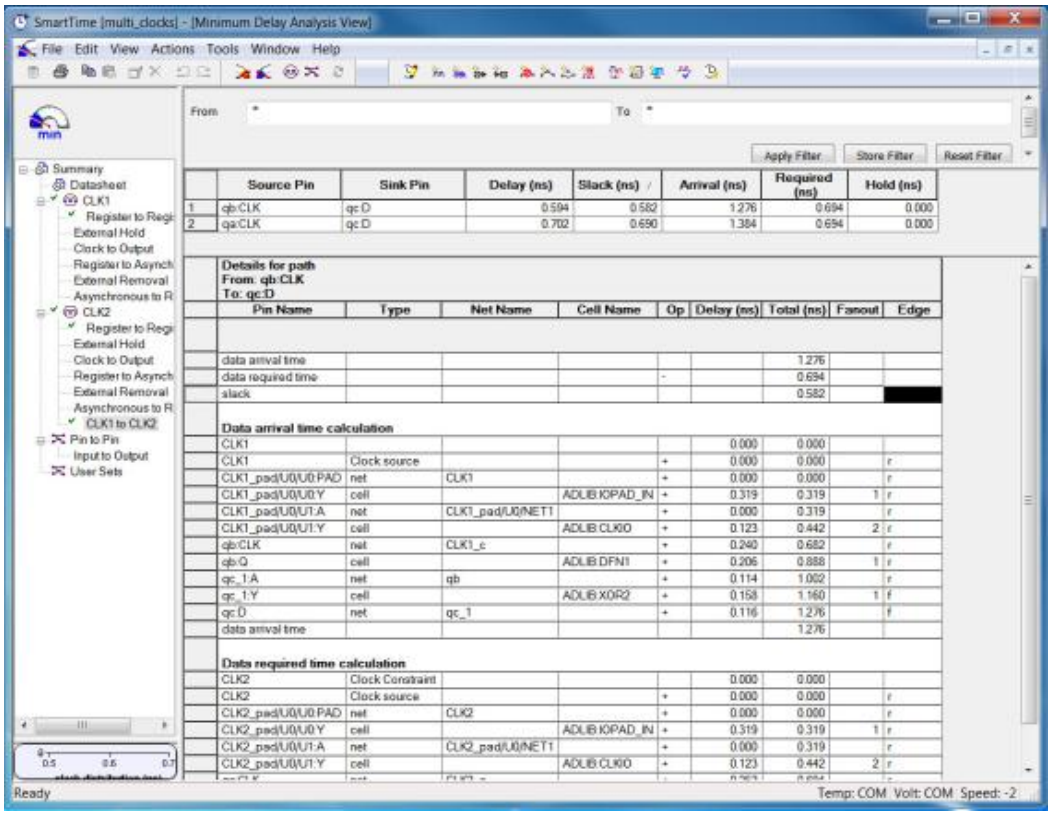

Figure 65 · Minimum Delay Inter-Clock Domain Timing Analysis - multi_clocks Example Design

The Paths list shows the detailed timing analysis. The shortest reported path is from qb:clk to qc:d, as shown in the figure below. This path has a positive slack of 0.582 ns. The clock edges used in the calculation are shown in the timing diagram below.

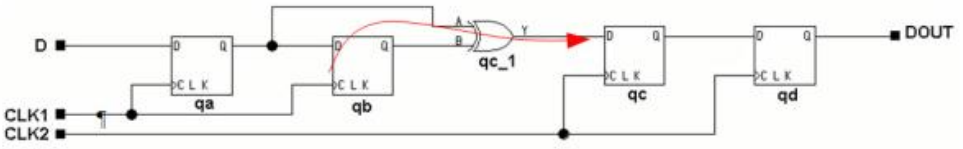

Figure 66 · Shortest Reported Inter-Clock Domain Path - multi_clocks Example Design

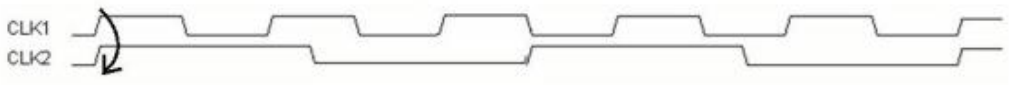

Figure 67 · Clock Edges Used in Inter-Clock Domain Min Delay Calculation - multi_clocks Example Design

Product Support

The Microsemi SoC Products Group backs its products with various support services including a Customer Technical Support Center and Non-Technical Customer Service. This appendix contains information about contacting the SoC Products Group and using these support services.

Contacting the Customer Technical Support Center

Microsemi staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Microsemi customers can receive technical support on Microsemi SoC products by calling Technical Support Hotline anytime Monday through Friday. Customers also have the option to interactively submit and track cases online at My Cases or submit questions through email anytime during the week.

Web: www.actel.com/mycases

Phone (North America): 1.800.262.1060

Phone (International): +1 650.318.4460

Email: soc_tech@microsemi.com

ITAR Technical Support

Microsemi customers can receive ITAR technical support on Microsemi SoC products by calling ITAR Technical Support Hotline: Monday through Friday, from 9 AM to 6 PM Pacific Time. Customers also have the option to interactively submit and track cases online at My Cases or submit questions through email anytime during the week.

Web: www.actel.com/mycases

Phone (North America): 1.888.988.ITAR

Phone (International): +1 650.318.4900

Email: soc_tech_itar@microsemi.com

Non-Technical Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

Microsemi's customer service representatives are available Monday through Friday, from 8 AM to 5 PM Pacific Time, to answer non-technical questions.

Phone: +1 650.318.2470

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.

5-02-00086-2/10.14