Creating Analog Testbenches

for Fusion Designs

Actel®

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Introduction

This tutorial demonstrates how to create analog testbenches for Fusion FPGAs using Libero® IDE and WaveFormer Lite.™

To create an analog testbench, follow the steps below:

1. Chapter 1 – Setting Up the Example Files
2. Chapter 2 – Configuring the Voltage/Temperature Monitor
3. Chapter 3 – Creating the Analog Testbench
4. Chapter 4 – Simulating the Fusion Design

This tutorial assumes basic knowledge and experience with the Libero IDE design flow and WaveFormer Lite testbench generation tool. For more information about Libero, refer to the *Libero User's Guide*, available at the Actel web site (www.actel.com).

1 Setting Up the Example Files

In this step, you will set up the project files for the Fusion design used in this tutorial.

1. Download the *Creating an Analog Testbench* tutorial supplemental files from the Actel website.
2. Create a new folder on your C drive named *VT_Mon* (*C:\Actelprj\VT_Mon*).
3. Unzip the supplemental files to the *C:\Actelprj\VT_Mon* folder.
4. From the **Start** menu, choose **Actel Libero IDE** or double-click the **Actel Libero IDE** icon on the desktop.
5. From the **File** menu, choose **Open Project**.
6. Browse to *C:\Actelprj\VT_Mon* and click **OK**. This opens the VT_Mon project in Libero IDE (see Figure 1-1).

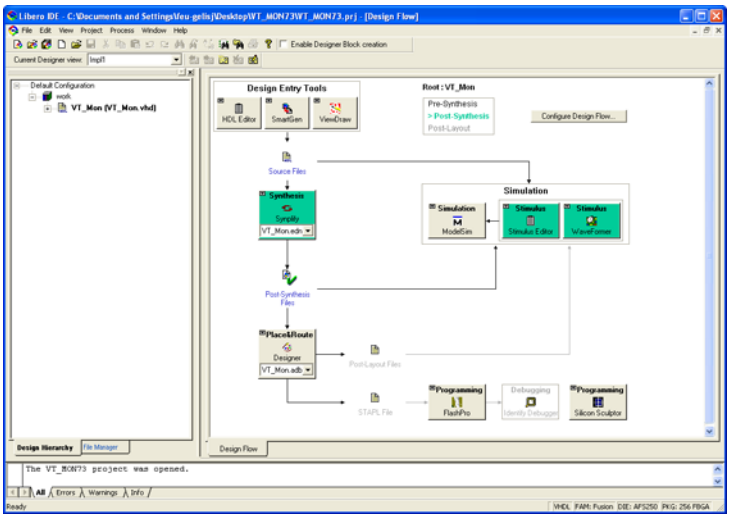

Figure 1-1 · Libero IDE Design Flow Window with VT_Mon Project

Note: If the Tool Profile Conflict dialog box appears, select **Use the profile currently selected in Libero IDE** and click **OK**.

2 Configuring the Voltage/Temperature Monitor

This step uses SmartGen to configure the voltage and temperature monitor Fusion peripherals and implements them in the design HDL code. The intended function for this design is to monitor a supply voltage and a temperature, and send flags to the Fusion system when the voltage rises above 5.25 V or falls below 4.75 V, and when the monitored temperature exceeds 70° C.

In this step, you will configure a voltage monitor, a temperature monitor, and two gate drivers. The gate driver functions are responsible for sending flags to the Fusion system, which could then either control the input environment or sound alarms, or both.

1. Launch SmartGen by clicking the **SmartGen** button from the Libero IDE interface. This opens the SmartGen tool (Figure 2-1).

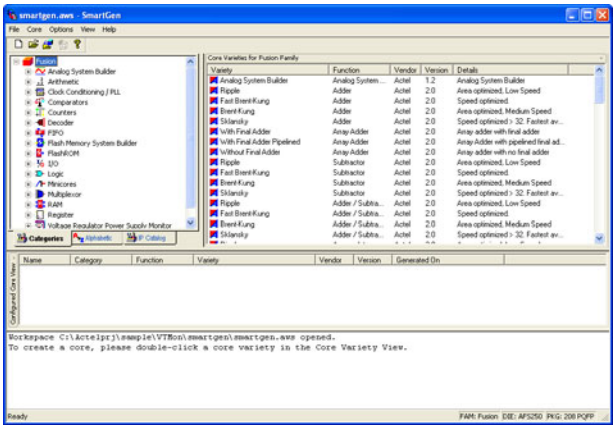

Figure 2-1 · SmartGen Window

2. Under the **Categories** tab, click the **Analog System Builder** category.
3. In the **Variety** window, double-click **Analog System Builder**. The Analog System Builder (ASB) core configurator (Figure 2-2) allows you to select the required analog functions, the analog inputs that need to be configured, and the specific threshold values required to send event flags to the system logic.

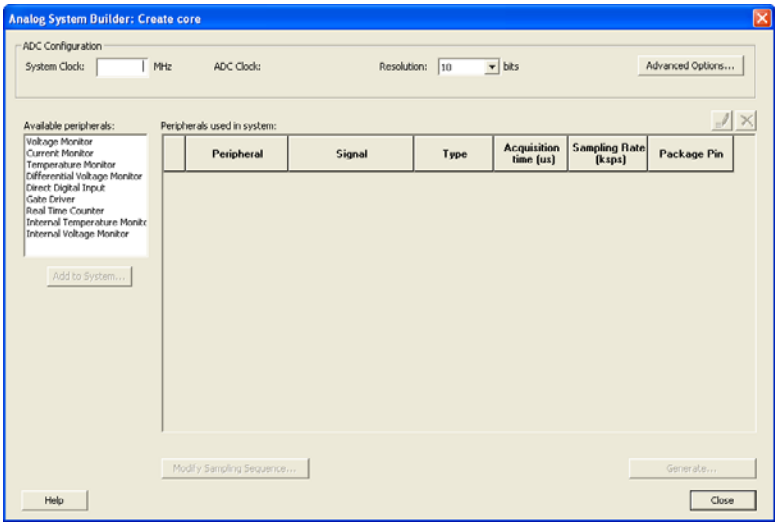

Figure 2-2 · Analog System Builder Configurator for Fusion

4. In the **ADC Configuration** panel, enter **40.0** as the **System Clock** frequency and **10.0** as the **Resolution**.
5. From the **Available peripherals** list, select **Voltage Monitor** and click **Add to System**. This opens the **Configure Voltage Monitor Peripheral** window.

   This input signal configuration will signal the system when the voltage on the AV5V input pin is 5.25 V or higher for one sample, or 4.75 V or lower for the other sample. The ASB will deassert (remove) the system flag after two consecutive samples when the signal falls under 5.25 V or rises above 4.75 V.
6. Enter the following information (as shown in Figure 2-3) :
   - **Signal name**: AV5V
   - **Acquisition time**: 1.0
   - **Maximum voltage**: 5.5

   Enter the following information for Flag 1:
   - **Flag Name**: over5p25
   - **Flag Type**: over
   - **Threshold (V)**: 5.25
   - **Assert Samples**: 1
   - **Deassert Samples**: 2

   Enter the following information for Flag 2:
   - **Flag Name**: under4p75
   - **Flag Type**: under
   - **Threshold (V)**: 4.75
   - **Assert Samples**: 1
   - **Deassert Samples**: 2

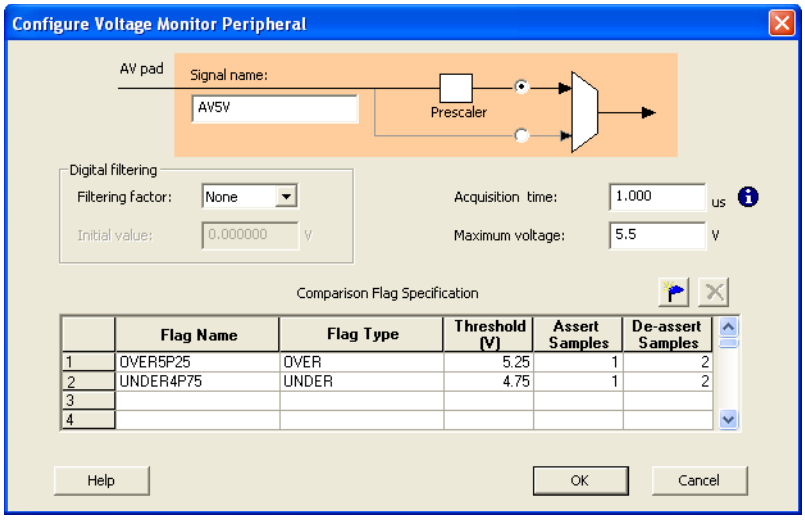

Figure 2-3 · Configure Voltage Monitor Peripheral Window

7. Click **OK**. This adds the voltage monitor peripheral to the list of peripherals used in the system.
8. From the **Available peripherals** list, select **Temperature Monitor** and click **Add to System**. This opens the Configure Temperature Monitor Peripheral window.

   This signal will send a flag to the system when one sampling of the input is 70° C or higher. Fusion will remove the system flag when the temperature is lower than 70° C for two samples.

9. Enter the following information (as shown in Figure 2-4) :
   - **Signal name**: Temp
   - **Acquisition time**: 10.0

   Enter the following information for Flag 1:
   - **Flag Name**: over70C
   - **Flag Type**: over
   - **Threshold (C)**: 70
   - **Assert Samples**: 1
   - **Deassert Samples**: 2

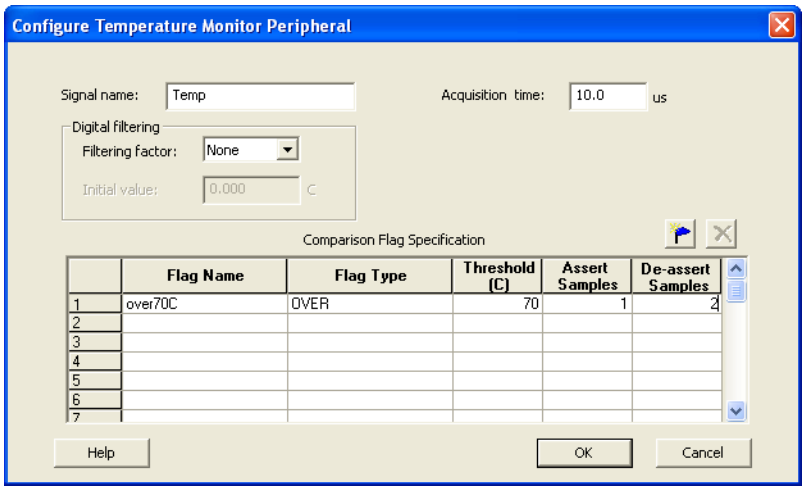

Figure 2-4 · Configure Temperature Monitor Peripheral Window

10. Click **OK**. This adds the temperature monitor peripheral to the list of peripherals used in the system.
11. From the **Available peripherals** list, select **Gate Driver** and click **Add to System**. This opens the Configure Gate Driver Peripheral window.

    You will configure the gate driver function for the voltage monitor. The gate driver enable in this case is designed to be the logical NOR of the over and under threshold flags.
12. Enter the following information (as shown in Figure 2-5 on page 12) :
    - **Signal name**: Supply_good
    - **Enable signal name**: Supply_good_en
    - **Source current**: 1.000

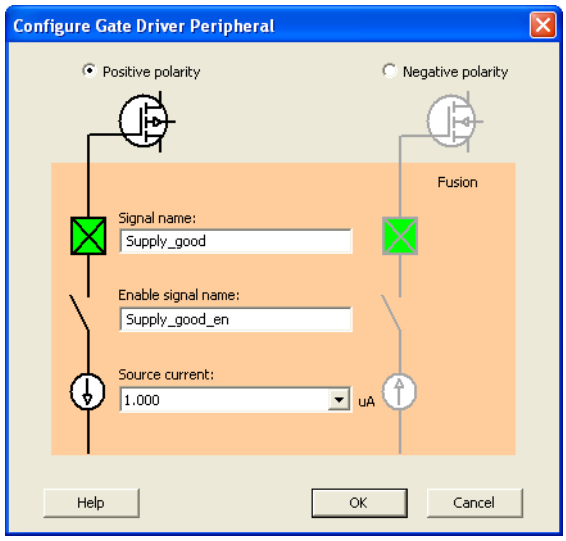

Figure 2-5 · Configure Gate Driver Peripheral Window

13. Click **OK**. This adds the gate driver peripheral to the list of peripherals used in the system.
14. From the **Available peripherals** list, select **Gate Driver** and click **Add to System**. This opens the **Configure Gate Driver Peripheral** window.

    You will configure the gate driver function for the temperature system output flag when the temperature exceeds 70° C. In this design, the Over_temp flag is used as the gate driver enable.
15. Enter the following information (as shown in Figure 2-6 on page 13):
    - **Signal name**: Over_temp
    - **Enable signal name**: Over_temp_en
    - **Source current**: 1.000

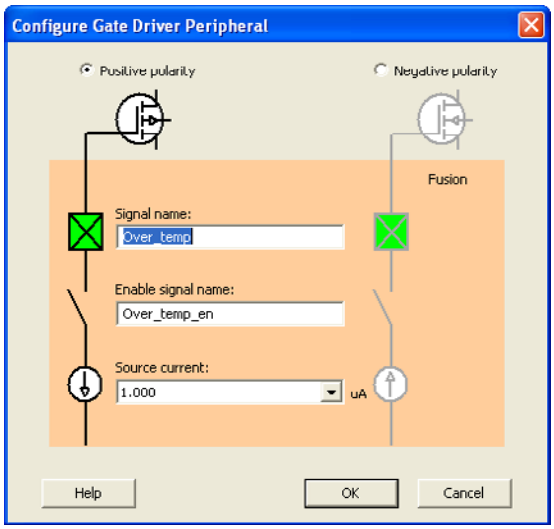

Figure 2-6 · Configure Gate Driver Peripheral Window

16. Click **OK**. This adds the gate driver peripheral to the list of peripherals used in the system.
17. Click **Generate**. This brings up the Generate Core dialog box (Figure 2-7).

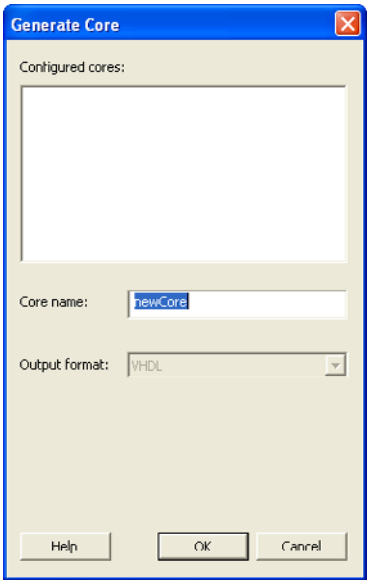

Figure 2-7 · Generate Core Dialog Box

18. Enter *VT_Mon* as the **Core name** and click **OK**.
19. Click **Close** to close the Analog System Builder window.
20. From the **File** menu, choose **Exit** to close SmartGen.

To complete this design you will need to configure and make proper connections to the Flash Memory System Builder. Doing so is beyond the scope of this tutorial.

3 Creating the Analog Testbench

The next step in a Fusion design flow is to synthesize your design and create a testbench.

SynaptiCAD's WaveFormer Lite v11.11d provides the capability to create and generate a testbench with analog and digital signals. The input signals for the voltage and temperature inputs for the VT_Mon design can easily be drawn using the WaveFormer Lite user interface.

1. Click the **Stimulus WaveFormer** button in the Libero IDE design flow window to launch WaveFormer Lite. This opens the WaveFormer Lite user interface.

   Libero IDE finds the clock and respective input/output signals of the VT_Mon design. Clock and signal names are already identified in the waveform window. The SYS_CLK, SYS_RESET, and INIT_POWER_UP input signal names have already been entered in the GUI (Figure 3-1).

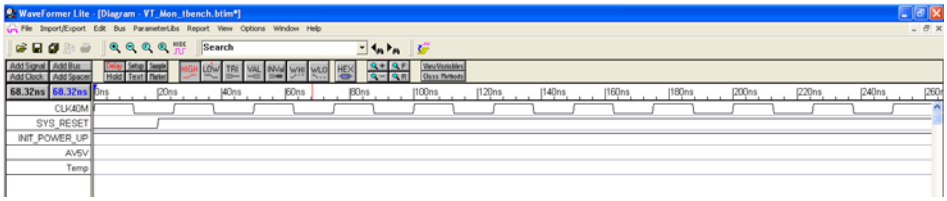

Figure 3-1 · Initial WaveFormer Lite Timing Diagram

   The VT_Mon testbench in WaveFormer Lite has already been configured with a 40 MHz clock, the Initial_Power_Up signal goes active high at 10 ns, and the System Reset signal goes active high at 40 ns. The analog inputs AV5V and Temp can now be configured in the WaveFormer window.

2. From the **Options** menu, choose **Display Unit** > **1µs**.
3. Double-click the **AV5V** signal name to open the Signal Properties dialog box.
4. In the **Signal Properties** dialog box, set the following information:
   - **Direction**: **output** (default)
   - **Size Ratio**: Enter **3** to increase the vertical height of the waveform display row.
   - **Signal Type**: **actel_voltage**
   - **Radix**: **real**
   - **Label Eqn** (Equation): Use the arrow to open a pop-up list of waveform types. For this testbench, select **Ramp (StartV,EndV,Duration)**. This option enables you to easily insert a ramp of beginning and ending voltages over a specified duration. A ramp waveform equation is perfect for creating a long, slow voltage variation that might be experienced by a voltage monitor input signal in this particular design.

     Note: When starting a new waveform, be sure the window is clear of any other equations.

For the initial AV5V signal, edit the ramp equation to **Ramp(0,0,500)** and click **Label Eqn** (Figure 3-2) . The AV5V data shows a steady state zero voltage for 500 µs.

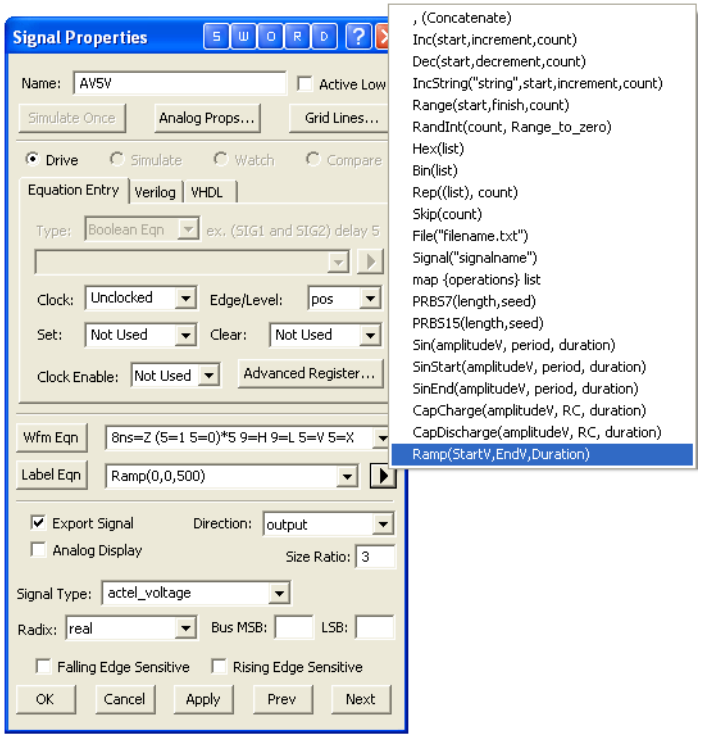

Figure 3-2 · WaveFormer Lite Signal Properties Dialog Box

You can add a subsequent value to the ramp equation that specifies the number of increments to be used in the duration. In the AV5V testbench example, to complete the waveform, each ramp and duration is required to be implemented in five or eight increments (see Step 5 below). More increments would have the effect of providing a smoother waveform.

5. With the **Signal Properties** dialog box still open, insert the following series of ramp equations, and click the **Label Eqn** button:
   - Ramp(0,0,500) – Zero voltage for 500 µs
   - Ramp(1,5,200,8) – Ramps from 1.0 V to 5.0 V in 200 µs, in 25 µs increments
   - Ramp(5,5,100,5) – Voltage stays steady at 5.0 V for 100 µs
   - Ramp(5,5.5,200,8) – Ramps from 5.0 V to 5.5 V in 200 µs, in 25 µs increments
   - Ramp(5.5,5.5,100,5) – Voltage stays steady at 5.5 V for 100 µs
   - Ramp(5.5,5,200,8) – Ramps from 5.5 V to 5.0 V in 200 µs, in 25 µs increments
   - Ramp(5,5,100,5) – Voltage stays steady at 5.0 V for 100 µs
   - Ramp(5,4.6,200,8) – Ramps from 5.0 V to 4.6 V in 200 µs, in 25 µs increments
   - Ramp(4.6,4.6,100,5) – Voltage stays steady at 4.6 V for 100 µs
   - Ramp(4.6,5,200,8) – Ramps from 4.6 V to 5.0 V in 200 µs, in 25 µs increments
   - Ramp(5,5,200,5) – Voltage stays steady at 5 V for 200 µs

   Note: Clear the **Label Eqn** field prior to entering each equation to avoid duplicating the same equation for the next segment of the waveform.

The total signal duration is 2100 µs.

WaveFormer easily concatenates the new data waveform to the preceding waveform so that a continuous waveform is created.

6. Click **OK**.
7. Right-click the **Temp** signal name to open the Signal Properties dialog box for the Temp signal.
8. In the **Signal Properties** dialog box, set the following information:
   - **Direction**: **output** (default)
   - **Size Ratio**: Enter **3** to increase the vertical height of the waveform display row.
   - **Signal Type**: **actel_temperature**
   - **Radix**: **real**
   - **Label Eqn** (Equation): Use the arrow  to open a pop-up list of waveform types, and select **Ramp (StartV,EndV,Duration)**. In the case of temperature, use values in degrees Celsius, starting with 70° C.
9. Enter the following series of ramp equations, incorporating each by clicking the **Label Eqn** button:
   - Ramp(50,50,500) – Temperature stays steady at 50° C for 500 µs
   - Ramp(50,70,400,16) – Temperature increases from 50° C to 70° C in 400 µs in 25 µs increments
   - Ramp(70,72,200,8) – Temperature increases from 70° C to 72° C in 200 µs in 25 µs increments
   - Ramp(72,72,200,10) – Temperature stays steady at 72° C for 200 µs
   - Ramp(72,70,200,8) – Temperature drops from 72° C to 70° C in 200 µs in 25 µs increments
   - Ramp(70,68,200,8) – Temperature drops from 70° C to 68° C in 200 µs in 25 µs increments
   - Ramp(68,72,200,8) – Temperature ramps from 68° C to 72° C in 200 µs in 25 µs increments
   - Ramp(72,71,200,8) – Temperature drops from 72° C to 71° C in 200 µs in 25 µs increments

   The total signal duration is 2100 µs.
10. Click **OK**. The resulting data for the AV5V and Temp signals is shown in the WaveFormer window as individual pulses or increments with the analog values for each increment (Figure 3-3).

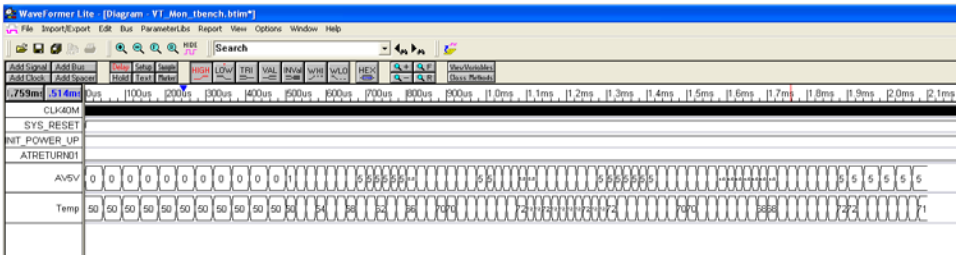

Figure 3-3 · Resulting Waveform for AV5V Voltage Monitor Signal

If you use SynaptiCAD WaveFormer Pro software, check **Analog Display** in the **Signal Properties** dialog box to provide a visual representation of the analog signal (Figure 3-4).

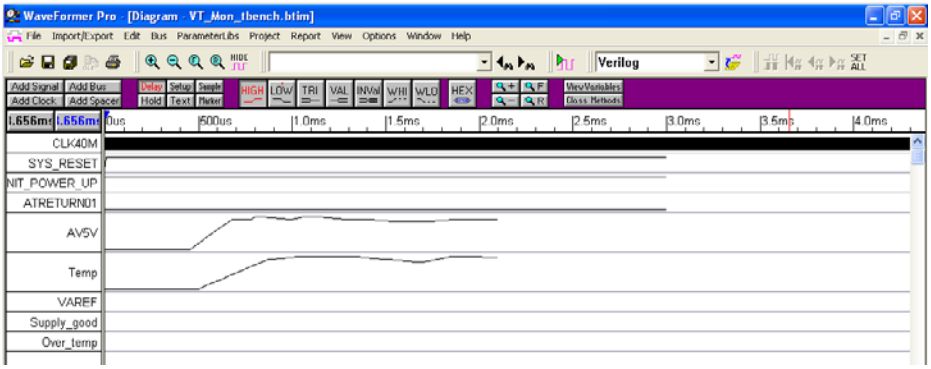

Figure 3-4 · Resulting WaveForm Pro Waveform for AV5V Voltage Monitor Signal

11. From the **File** menu, choose **Save**.
12. From the **Import/Export** menu, choose **Export Timing Diagram As**. In the **Export** dialog box, select **VHDL w/Top Level Test Bench (.vhd)** and click **OK**.

4 Simulating the Fusion Design

In this step, you will simulate the design.

1. Right-click the **Stimulus Editor** button in the Libero IDE interface and choose **Organize Stimulus**. This opens the Organize Stimulus dialog box.
2. Select your testbench file and click **Add**. This adds your testbench to the Associated Files list (Figure 4-1) .

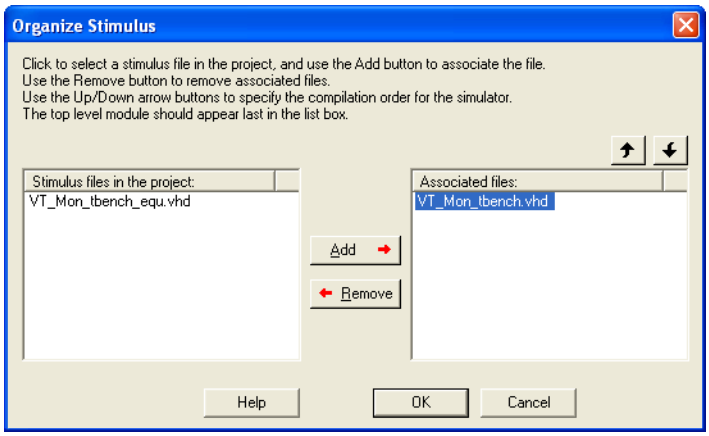

Figure 4-1 · Organize Stimulus Dialog Box

3. Click **OK**.
4. Click the **Simulation ModelSim** button. This opens the ModelSim user interface. The results of the simulation for the VT_Mon design are shown in Figure 4-2 and Figure 4-3 on page 20.

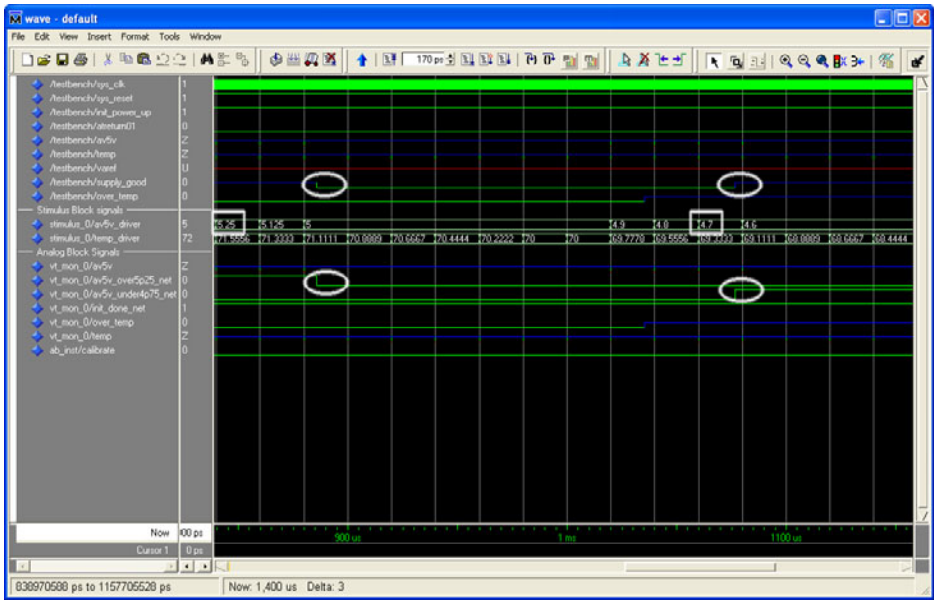

Figure 4-2 · Effect of the AV5V Input Testbench after Simulation

Figure 4-2 demonstrates the effect of the varying voltage on the AV5V input. The stimulus_0/av5v_driver line shows that part of the waveform where the voltage is initially 5.25 V and ramps down below 4.75 V between 800 and 1100 µs. As specified by the AV5V maximum voltage threshold flag, and visualized by the /testbench/supply_good

output signal, the Fusion logic asserts the overvoltage flag where the voltage is exceeding 5.25 V and deasserts it as the voltage drops below 5.25 V. The threshold flag remains deasserted until the voltage drops below 4.75 V, where it reasserts, as indicated by the vt_mon_0/av5v_under4.75v logic and /testbench/supply_good output signal, at approximately 1080 µs. Any delay between the input voltage signal and the respective flag threshold value is a function of the specified sampling rate, resolution of the analog to digital converter, and number of samples taken before assert/deassert flag is set. The AV5V testbench works as desired, clearly showing the assert/deassert of the flags based on the requested thresholds.

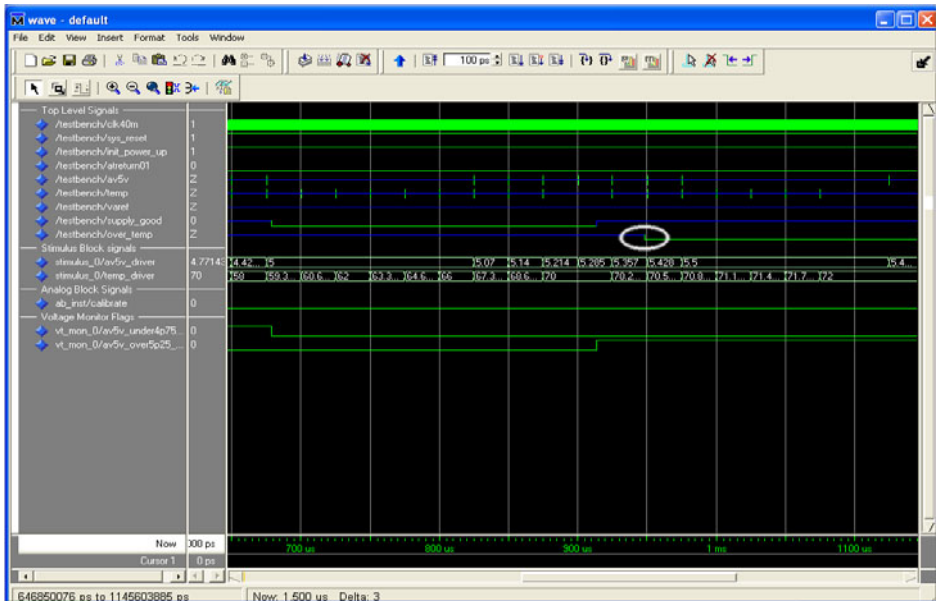

Figure 4-3 · Effect of the Temp Input Testbench after Simulation

The temperature monitoring threshold flag in the Fusion ASB has been set to assert when the temperature exceeds 70° C and will deassert when the temperature is less than or equal to 70° C. Figure 4-3 demonstrates the effect of a varying temperature on the Temp input of the design, where the temperature is rising from 50° C and passes through 70° C. Note that the testbench/over_temp signal, which has been deasserted, asserts as the temperature passes above 70° C, and the /testbench/over_temp output simultaneously asserts as directed by the threshold detection logic. Any delay in the actual assertion or deassertion as compared to the input temperature is a function of the specified sampling rate and resolution of the analog to digital converter. The Temp testbench shows the over_temp assertion/assertion as the temperature rises above the specified threshold of 70° C.

5 Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

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From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
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From Europe, call **650.318.4252** or **+44 (0) 1276 609 300**
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From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650.318.8044**

Actel Customer Technical Support Center

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Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

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