Total Ionizing Dose Test Report

No. 12T-RTAX2000S-CG624-D5HK31

October 11, 2012

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TOTAL IONIZING DOSE TEST REPORT

No. 12T-RTAX2000S-CG624-D5HK31

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 200 krad (SiO_2)
3. Input Threshold (VIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
6. Transition Characteristics	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation and annealing, each input is grounded.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000S
Package	CG624
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	rtax2000_CG624_Top
Die Lot Number	D5HK31
Quantity Tested	6
Serial Number	300 krad(SiO_2): 5852, 5858 200 krad(SiO_2): 5860, 5877, 5895
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	7.5 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V/1.5 V

B. Test Method

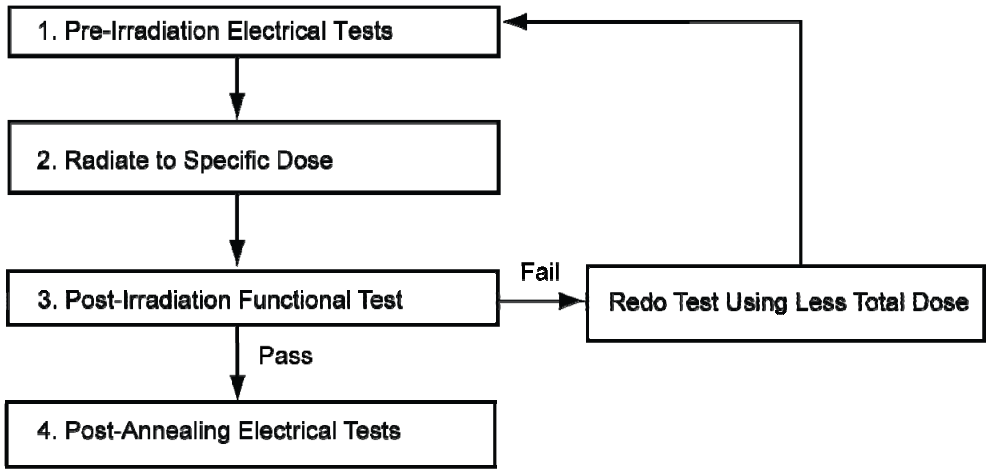


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTAX2000S are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 1 week.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design, rtax2000_CG624_Top, for testing total dose effects. These logic designs are described in the following subsections. Appendix A shows the block diagram.

Generally, the functional test is performed on every design; most inputs are tested for threshold voltage and leakage current, including global clocks; the standby I_{CC} includes I_{CCI} and I_{CCA}. Except propagation delay and the transition characteristic, which is measured on the output O_BS, all other parameter measurements are done on a tester. Also note that, due to logistics limitation, the post-irradiation but pre-room-temperature-annealing functional test is performed on bench; the tested designs are shift registers and long buffer string, which are design 5 and 6 described in the following.

1. Embedded SRAM

This design is to test the function of the embedded SRAM. It uses all the RAM blocks available in the DUT. This design enables an automatic testing sequence that every bit is written and then read. Any error will be reported as a signal in the output.

2. Unidirectional LVTTL Input and Output

This is for testing radiation effects on unidirectional input and output threshold, leakage, and buffer fan-out. There are 3 sub-designs: a) a logic-core buffer with 8 fan-outs; b) a logic-core buffer with 3 fan-outs; c) 6 channels of input buffer directly connected to output buffer without core logic. LVTTL is used because it is the worst case among all the single-ended standards.

3. Bidirectional LVTTL IO

This design is for testing the radiation effects on the input/output characteristic of the bidirectional IO. There are 7 channels of bidirectional IO for radiation effects testing.

4. LVPECL Input

This design is for testing the radiation effects on the LVPECL differential inputs. 3.3V-LVPECL is considered the worst case differential input standard in the DUT. There are 7 channels.

5. Shift Registers

This design is to test the radiation effects on the function of flip-flops, which are configured R-Cells. There are 4 shift registers and each using a different global clock; one has 3,584 bits and the other three each has 2,048 bits.

6. Long Buffer String

This design is to measure the radiation effects on the propagation delay. The input of the design using a clock feeding a toggle flip-flop to generate a checkerboard signal; this signal is then fed into a buffer string with 10,000 stages. The time delay between the input clock edge at CLOCK_IN and the output switching due to this clock edge at O_BS is defined as propagation delay high to low (T_{pdhl}) or low to high (T_{pdlh}); the percentage change of the average of T_{pdhl} and T_{pdlh} is used to determine the radiation effects. A more than 10% of propagation change is considered as failure.

III. Test Results

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests. The as-irradiated DUT is functionally tested on the output (O_FF_HCLKA) of the largest shift register.

B. Power Supply Current (ICCA and ICCI)

Figure 2 through Figure 6 plot the influx standby ICCA and ICCI versus total dose for each DUT. The post-annealing ICC for four different bit patterns, all '0', all '1', checkerboard and inverted-checkerboard, in the RAM are basically the same.

In compliance with TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCI in this test is defined as the addition of highest ICCI, ICCDA and ICCDIFFA values in Table 2-4 of *the RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs* datasheet:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

For ICCA, the PIPL is 500 mA; the PIPL of ICCI equals to 35 + 10 + 3.13 × 7 = 66.91 (mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT.

Table 2 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 2 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
5852	300 krad	5	104	8	25	311	174
5858	300 krad	3	94	7	24	310	184
5860	200 krad	6	8	6	25	125	52
5877	200 krad	3	4	3	23	134	45
5895	200 krad	3	6	3	24	111	47

Based on these PIPL, post-annealed DUT passes both the ICCA and ICCI spec for 200 krad (SiO2).

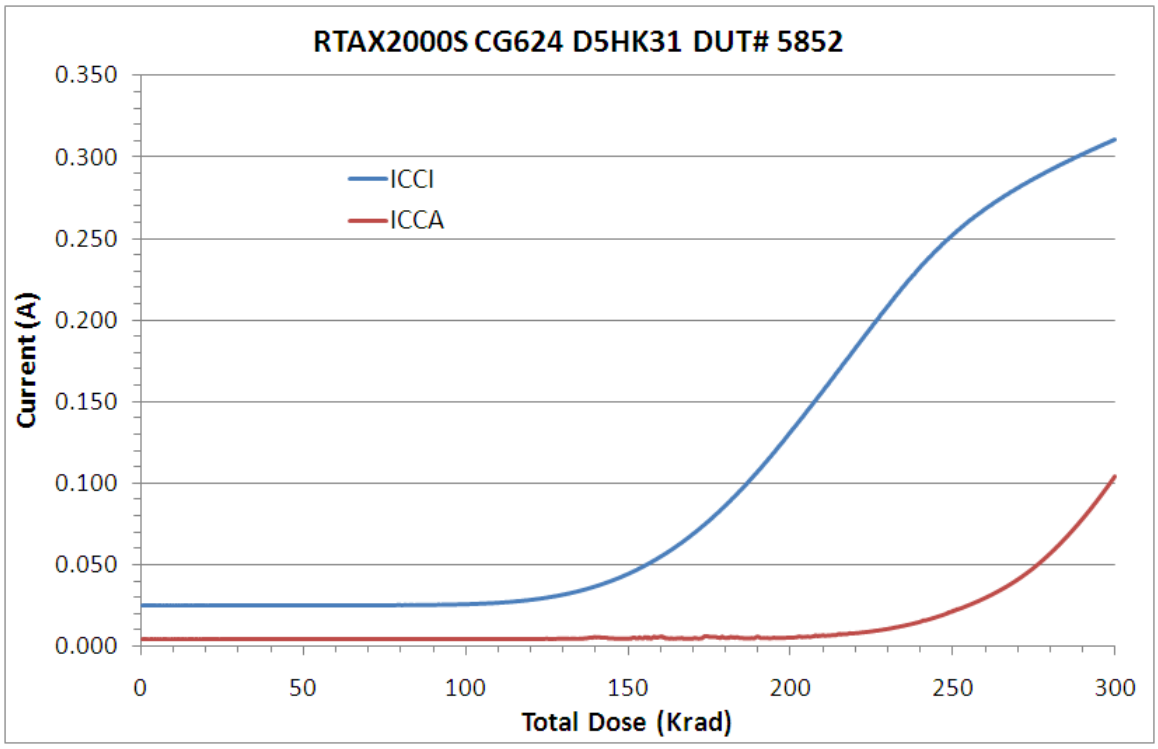


Figure 2 DUT 5852 Influx ICCA and ICCI

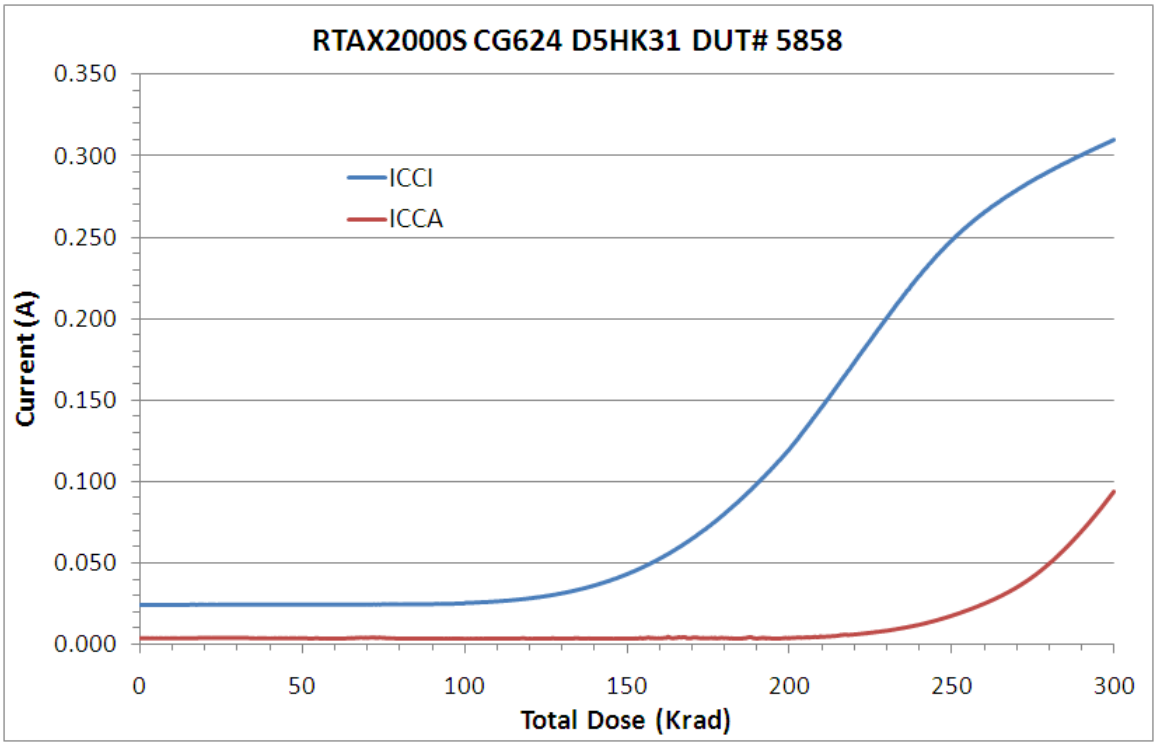


Figure 3 DUT 5858 Influx ICCA and ICCI

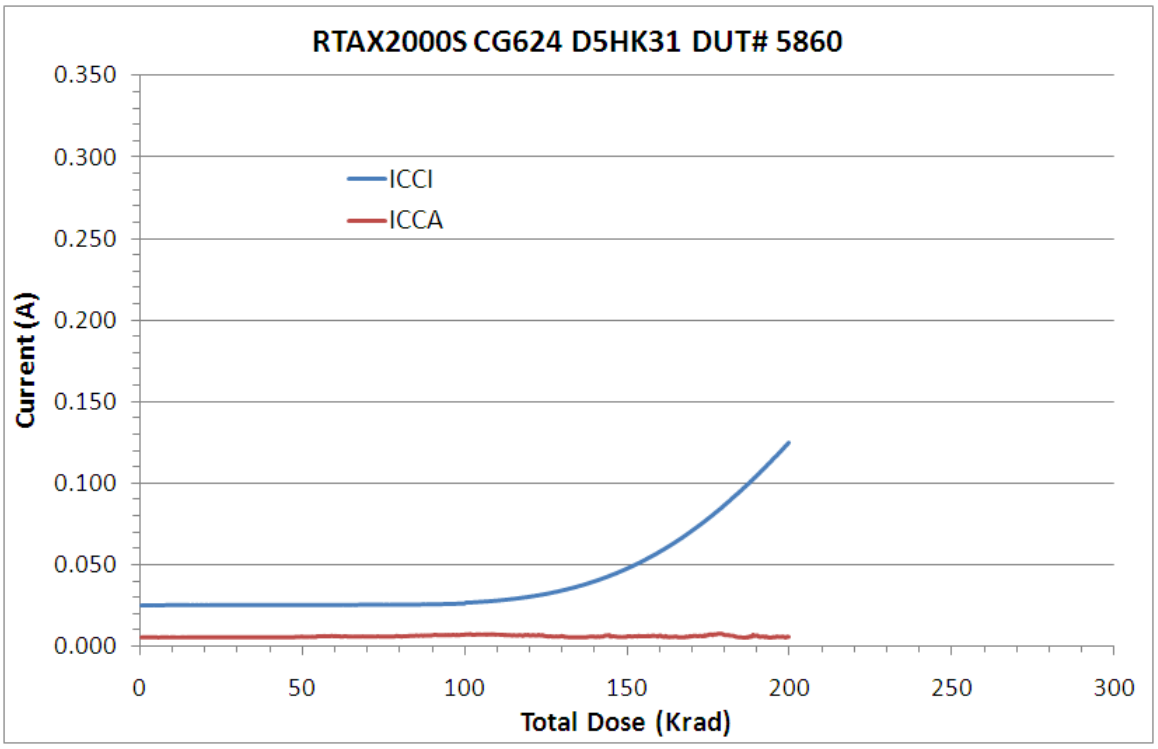


Figure 4 DUT 5860 Influx ICCA and ICCI

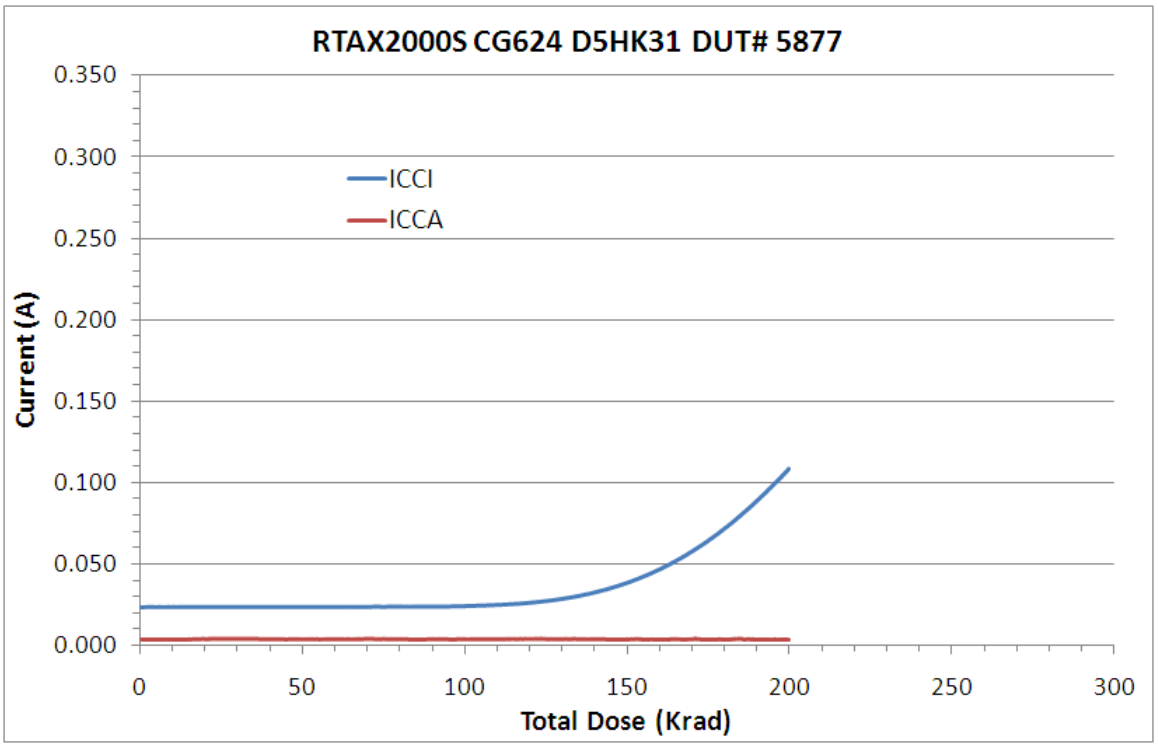


Figure 5 DUT 5877 Influx ICCA and ICCI

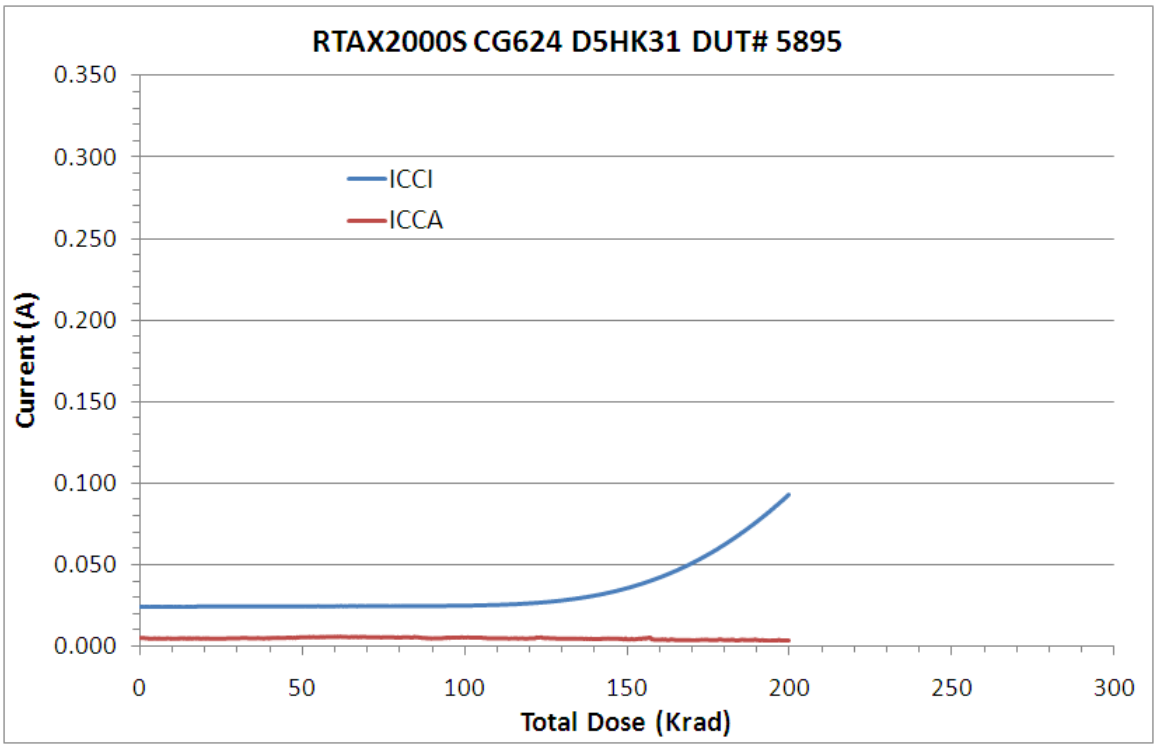


Figure 6 DUT 5895 Influx ICCA and ICCI

C. Single-Ended Input Logic Threshold (VIL/VIH)

Table 3a through Table 3c list the pre-irradiation and post-annealing single-ended input logic thresholds. All data are within the specification limits. The post-annealing shift in every case is very small.

Table 3a Pre-Irradiation and Post-Annealing Input Thresholds

DUT	5852 (300 krad)				5858 (300 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
Bi_D_7	1370	1365	1370	1365	1370	1365	1370	1365
Bi_D_6	1355	1355	1380	1375	1350	1345	1380	1370
Bi_D_5	1365	1360	1375	1370	1360	1355	1370	1365
Bi_D_4	1370	1360	1370	1365	1365	1360	1365	1360
Bi_D_3	1365	1365	1380	1380	1365	1360	1380	1370
Bi_D_2	1360	1355	1380	1375	1355	1350	1375	1370
Bi_D_1	1360	1350	1375	1370	1355	1350	1375	1370
DA	1360	1365	1395	1400	1360	1355	1380	1390
EN8	1325	1335	1440	1425	1325	1330	1440	1430
IO_I_6	1335	1345	1415	1410	1350	1335	1415	1410
IO_I_5	1335	1345	1430	1420	1335	1355	1420	1405
IO_I_4	1390	1390	1385	1385	1390	1390	1385	1380
IO_I_3	1365	1385	1395	1390	1360	1385	1390	1395
IO_I_2	1390	1390	1385	1385	1390	1385	1385	1380
IO_I_1	1395	1385	1385	1390	1385	1385	1390	1390
RCLK1P	1435	1435	1425	1425	1435	1430	1425	1420
RCLK2P	1430	1435	1430	1435	1430	1430	1430	1430

Table 3b Pre-Irradiation and Post-Annealing Input Thresholds

DUT	5860 (200 krad)				5877 (200 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
Bi_D_7	1380	1360	1380	1365	1380	1370	1380	1370
Bi_D_6	1365	1345	1390	1370	1365	1355	1390	1380
Bi_D_5	1375	1355	1385	1365	1370	1365	1385	1375
Bi_D_4	1375	1360	1375	1360	1375	1365	1375	1365
Bi_D_3	1375	1355	1390	1370	1375	1370	1390	1385
Bi_D_2	1360	1350	1380	1370	1360	1355	1380	1380
Bi_D_1	1370	1350	1380	1365	1370	1360	1380	1375
DA	1385	1355	1400	1380	1385	1365	1400	1395
EN8	1355	1325	1445	1440	1345	1335	1445	1445
IO_I_6	1345	1340	1425	1405	1345	1350	1425	1365
IO_I_5	1345	1335	1440	1395	1340	1355	1440	1415
IO_I_4	1400	1380	1395	1375	1395	1390	1395	1390
IO_I_3	1375	1380	1405	1385	1375	1365	1405	1395
IO_I_2	1395	1385	1395	1375	1395	1395	1395	1385
IO_I_1	1390	1385	1400	1385	1390	1385	1400	1395
RCLK1P	1440	1430	1430	1420	1440	1435	1430	1425
RCLK2P	1435	1430	1435	1425	1435	1435	1440	1435

Table 3c Pre-Irradiation and Post-Annealing Input Thresholds

DUT	5895 (200 krad)							
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
Bi_D_7	1370	1365	1370	1365				
Bi_D_6	1355	1350	1380	1370				
Bi_D_5	1365	1355	1375	1365				
Bi_D_4	1365	1360	1370	1360				
Bi_D_3	1365	1360	1380	1375				
Bi_D_2	1360	1350	1375	1365				
Bi_D_1	1355	1350	1370	1365				
DA	1360	1355	1390	1390				
EN8	1330	1325	1415	1440				
IO_I_6	1340	1355	1420	1410				
IO_I_5	1330	1340	1420	1395				
IO_I_4	1395	1390	1385	1380				
IO_I_3	1365	1360	1380	1390				
IO_I_2	1395	1385	1390	1385				
IO_I_1	1385	1385	1395	1385				
RCLK1P	1430	1425	1425	1420				
RCLK2P	1430	1430	1430	1425				

D. Differential Input (LVPECL) Threshold Voltage (VIL/VIH)

Table 4a through Table 4c list the LVPECL differential input threshold voltage changes due to irradiations. All pins show negligible changes, and all the data are within the specification.

Table 4a Pre-Irradiation and Post-Annealing Differential Input Thresholds

DUT	5852 (300 krad)				5858 (300 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DIO_IP_7	110	95	105	95	110	90	110	90
DIO_IP_6	105	95	105	95	105	90	105	90
DIO_IP_5	105	70	105	65	105	85	105	85
DIO_IP_4	85	75	80	75	95	65	90	60
DIO_IP_3	75	55	75	55	75	55	70	55
DIO_IP_2	95	80	95	75	90	75	85	75
DIO_IP_1	80	55	80	55	80	55	85	60

Table 4b Pre-Irradiation and Post-Annealing Differential Input Thresholds

DUT	5860 (200 krad)				5877 (200 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DIO_IP_7	105	100	105	100	105	95	105	95
DIO_IP_6	110	95	110	95	110	105	110	100
DIO_IP_5	105	95	100	90	105	95	100	95
DIO_IP_4	80	80	80	80	80	75	80	70
DIO_IP_3	80	60	80	60	80	75	80	75
DIO_IP_2	110	75	105	75	105	100	105	95
DIO_IP_1	70	70	65	75	70	65	65	55

Table 4c Pre-Irradiation and Post-Annealing Differential Input Thresholds

DUT	5895 (200 krad)							
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DIO_IP_7	105	95	100	90				
DIO_IP_6	115	105	110	105				
DIO_IP_5	105	95	100	95				
DIO_IP_4	90	85	90	80				
DIO_IP_3	90	80	90	80				
DIO_IP_2	95	85	90	80				
DIO_IP_1	75	75	80	75				

E. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Table 5a through Table 5c. The post-annealing data are within the specification limits.

Table 5a Pre-Irradiation and Post-Annealing VOL and VOH

DUT	5852 (300 krad)				5858 (300 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VOL (mV)		VOH (mV)		VOL (mV)		VOH (mV)	
Bi_IO_7	35	35	2970	2965	35	35	2965	2965
Bi_IO_6	30	30	2965	2965	35	30	2965	2965
Bi_IO_5	40	35	2960	2965	40	35	2960	2965
Bi_IO_4	35	35	2965	2960	35	35	2965	2965
Bi_IO_3	35	30	2965	2965	35	35	2965	2965
Bi_IO_2	35	35	2965	2965	35	30	2965	2965
Bi_IO_1	35	35	2965	2960	35	35	2965	2960
Bi_Y_7	25	30	2980	2980	25	30	2980	2980
Bi_Y_6	25	25	2980	2980	25	25	2980	2985
Bi_Y_5	30	25	2980	2980	30	25	2980	2980
Bi_Y_4	25	25	2980	2980	25	25	2980	2980
Bi_Y_3	30	25	2980	2980	30	25	2980	2980
Bi_Y_2	30	25	2980	2980	25	25	2980	2980
Bi_Y_1	30	30	2980	2980	30	30	2980	2980
CLOCK	20	20	2970	2970	20	20	2970	2970
CLOCK	25	25	2970	2970	20	25	2970	2970
QA_2	20	20	2970	2965	20	20	2965	2965
QA_1	20	20	2970	2965	20	20	2970	2965
QA_0	20	20	2970	2970	20	20	2970	2970

Table 5b Pre-Irradiation and Post-Annealing VOL and VOH

DUT	5860 (200 krad)				5877 (200 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VOL (mV)		VOH (mV)		VOL (mV)		VOH (mV)	
Bi_IO_7	35	35	2965	2970	35	35	2965	2970
Bi_IO_6	35	30	2965	2965	35	30	2965	2965
Bi_IO_5	40	35	2960	2965	40	35	2960	2965
Bi_IO_4	35	35	2965	2965	35	35	2965	2960
Bi_IO_3	35	35	2965	2965	35	30	2965	2965
Bi_IO_2	35	30	2965	2965	35	30	2965	2965
Bi_IO_1	35	35	2965	2965	35	35	2965	2965
Bi_Y_7	25	25	2980	2980	25	30	2980	2985
Bi_Y_6	25	25	2980	2985	25	25	2980	2985
Bi_Y_5	30	25	2980	2985	30	30	2980	2985
Bi_Y_4	25	25	2980	2980	25	25	2980	2980
Bi_Y_3	30	25	2980	2980	25	25	2980	2980
Bi_Y_2	25	25	2980	2980	25	25	2980	2980
Bi_Y_1	30	30	2980	2980	30	30	2980	2980
CLOCK	20	20	2970	2970	20	20	2970	2970
CLOCK	20	25	2970	2970	25	25	2970	2970
QA_2	20	20	2970	2970	20	20	2970	2970
QA_1	20	20	2965	2970	20	20	2965	2970
QA_0	20	20	2970	2970	20	20	2970	2970

Table 5c Pre-Irradiation and Post-Annealing VOL and VOH

DUT	5895 (200 krad)							
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VOL (mV)		VOH (mV)		VOL (mV)		VOH (mV)	
Bi_IO_7	35	35	2965	2970				
Bi_IO_6	30	30	2965	2965				
Bi_IO_5	40	35	2960	2965				
Bi_IO_4	35	35	2965	2965				
Bi_IO_3	35	30	2965	2965				
Bi_IO_2	35	35	2965	2970				
Bi_IO_1	35	35	2965	2965				
Bi_Y_7	25	25	2980	2985				
Bi_Y_6	25	25	2980	2985				
Bi_Y_5	30	30	2980	2985				
Bi_Y_4	25	25	2980	2980				
Bi_Y_3	30	25	2980	2980				
Bi_Y_2	30	25	2980	2980				
Bi_Y_1	30	30	2980	2980				
CLOCK	20	20	2970	2970				
CLOCK	20	25	2970	2970				
QA_2	20	20	2970	2970				
QA_1	20	20	2970	2970				
QA_0	0	20	2970	2970				

F. Propagation Delay

The propagation delay was measured in-situ, post-irradiation, and post-annealing. The irradiation was temporarily stopped at each total-dose increment of 100 krad for the measurement (however, the post-irradiation data of this lot are accidentally erased, only data before irradiation and after anneal are presented). The results are plotted in Figure 7, and listed in Table 6. As shown in Figure 7, the propagation delay initially decreases with the total dose, but the change is small throughout the irradiation. Referring to influx static current plots (Figure 2 through Figure 6), a device probably heats up as the dose increases. The rising temperature could be the root cause of the increasing trend at high doses. The post-annealing data, on the other hand, show decreased delay in every case.

The radiation delta in every case is well within the 10% degradation criterion. User can take the worst case for the design-margin consideration.

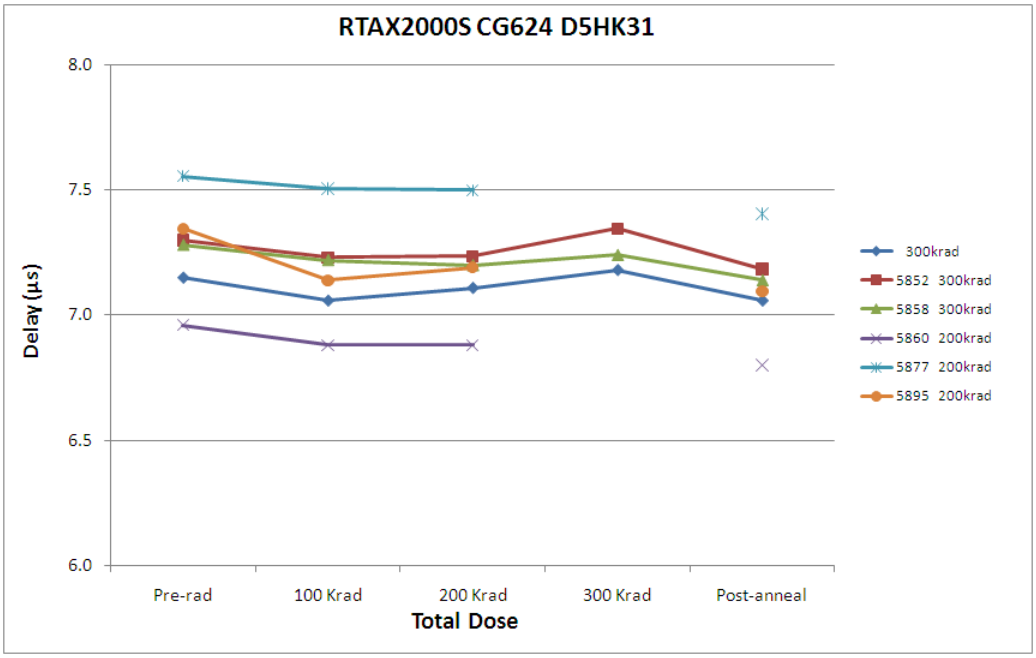


Figure 7 In-Situ Propagation Delay versus Total Dose.

Table 6 Radiation-Induced Propagation Delay Degradations

	RTAX2000S CG624 D5HK31						
Delay (µs)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	5852	300 krad	7.15	7.06	7.11	7.18	7.06
	5858	300 krad	7.30	7.23	7.24	7.35	7.19
	5860	200 krad	6.96	6.88	6.88	-	6.80
	5877	200 krad	7.56	7.51	7.50	-	7.41
	5895	200 krad	7.35	7.14	7.19	-	7.10
Radiation Δ (%)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	5852	300 krad	-	-1.26%	-0.56%	0.42%	-1.26%
	5858	300 krad	-	-0.96%	-0.89%	0.62%	-1.58%
	5860	200 krad	-	-1.15%	-1.15%	-	-2.30%
	5877	200 krad	-	-0.66%	-0.73%	-	-1.99%
	5895	200 krad	-	-2.79%	-2.11%	-	-3.40%

G. Transition Characteristics

Figure 8a to Figure 17b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

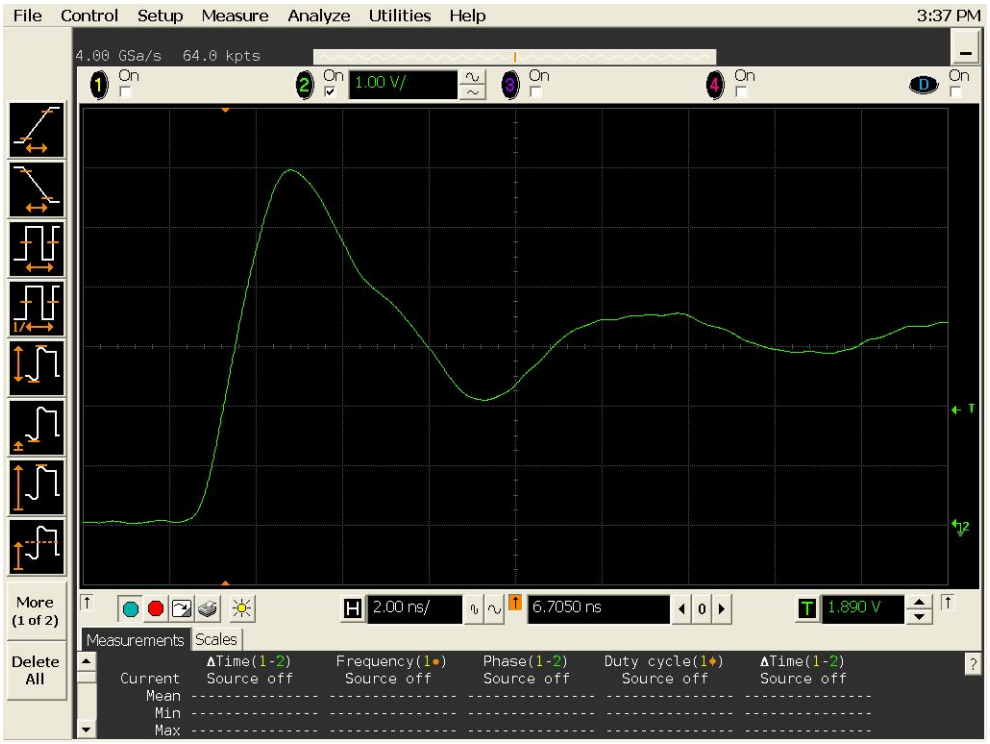


Figure 8a DUT 5852 Pre-Irradiation Rising Edge

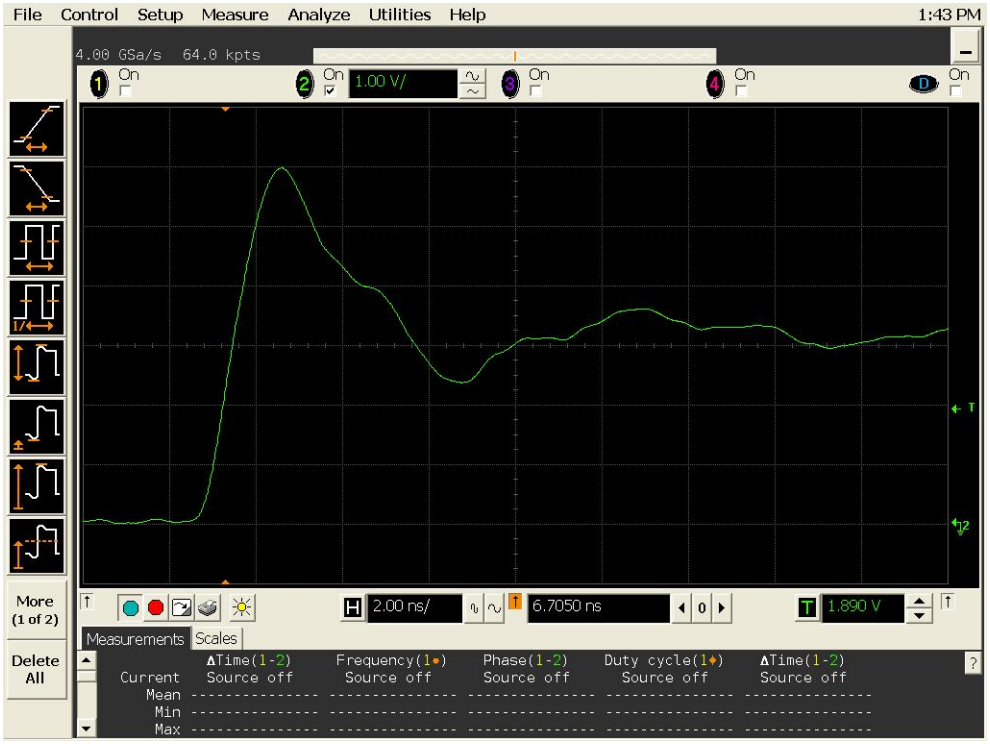


Figure 8b DUT 5852 Post-Annealing Rising Edge

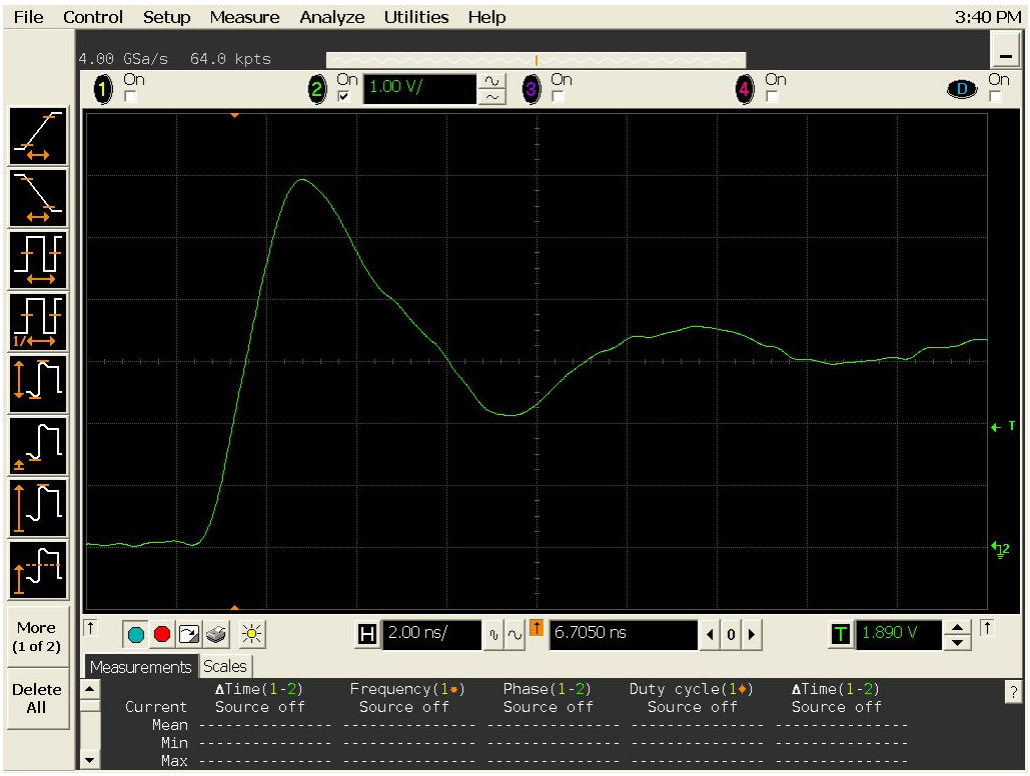


Figure 9a DUT 5858 Pre-Irradiation Rising Edge

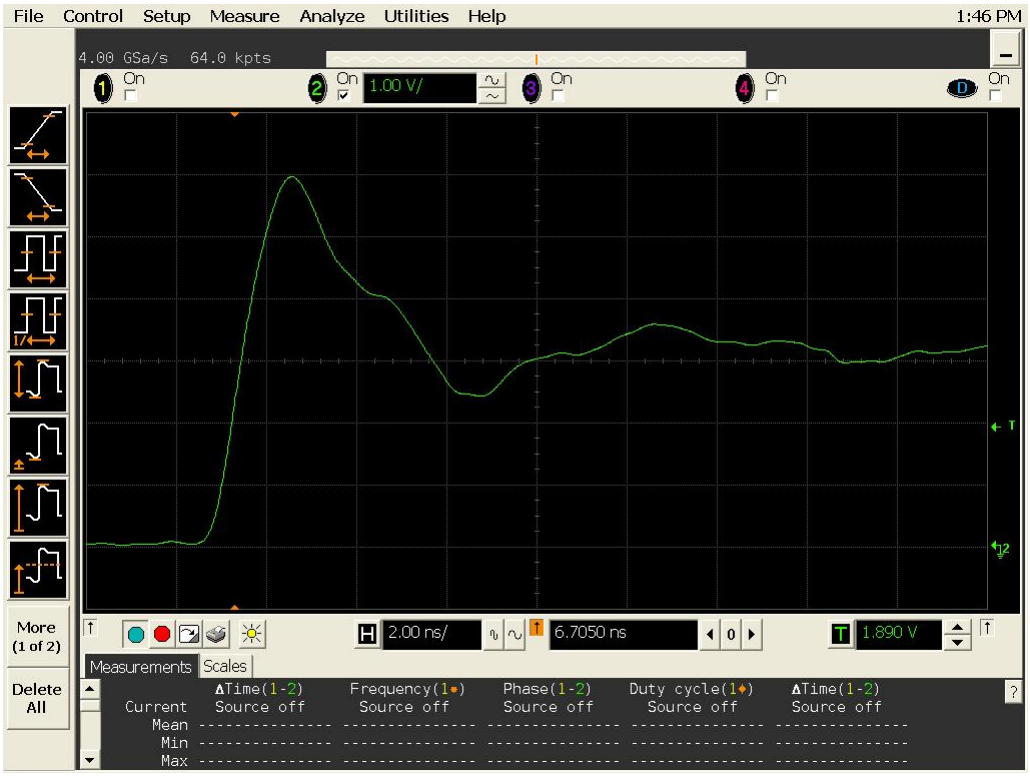


Figure 9b DUT 5852 Post-Annealing Rising Edge

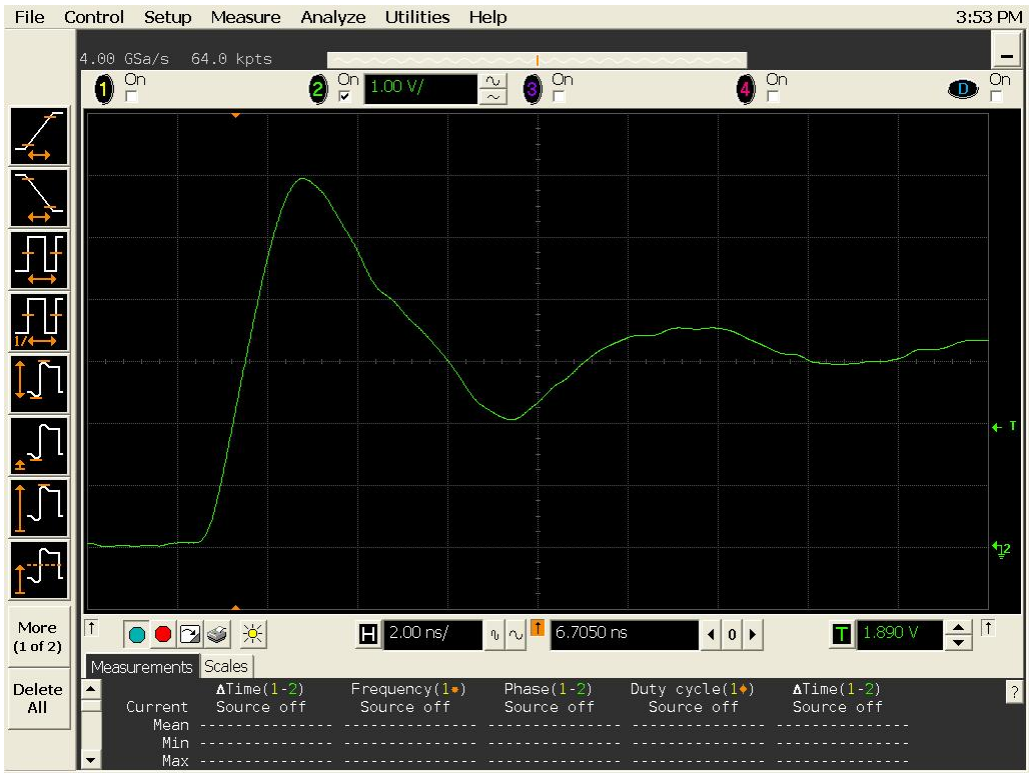


Figure 10a DUT 5860 Pre-Radiation Rising Edge

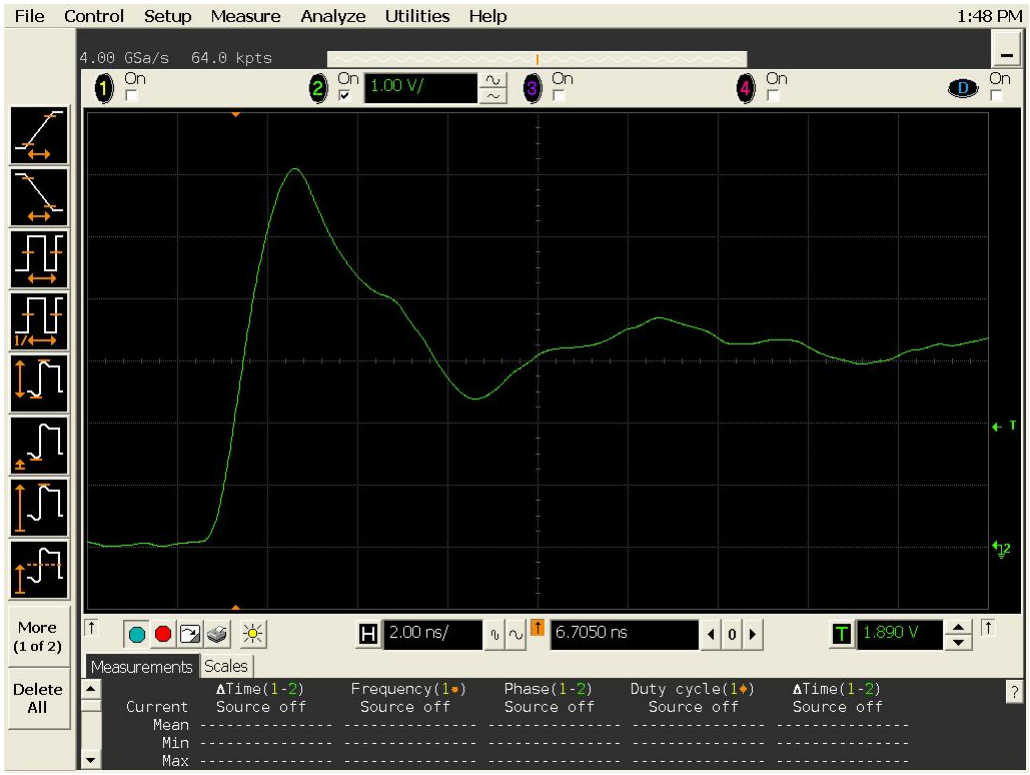


Figure 10b DUT 5860 Post-Annealing Rising edge

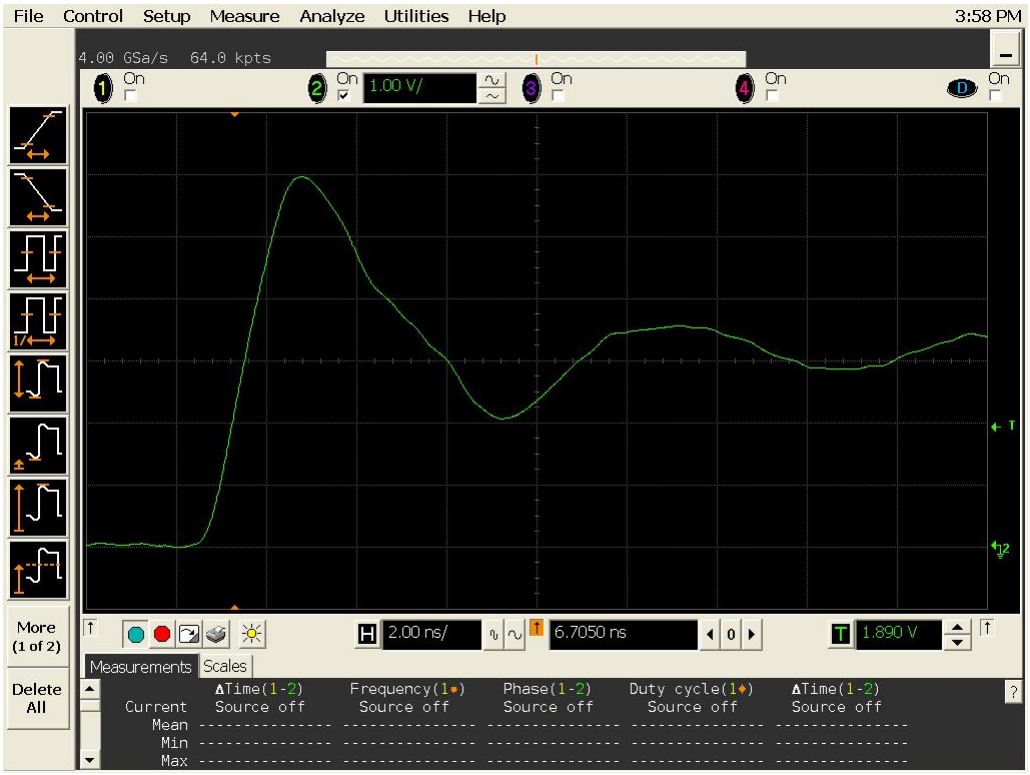


Figure 11a DUT 5877 Pre-Irradiation Rising Edge

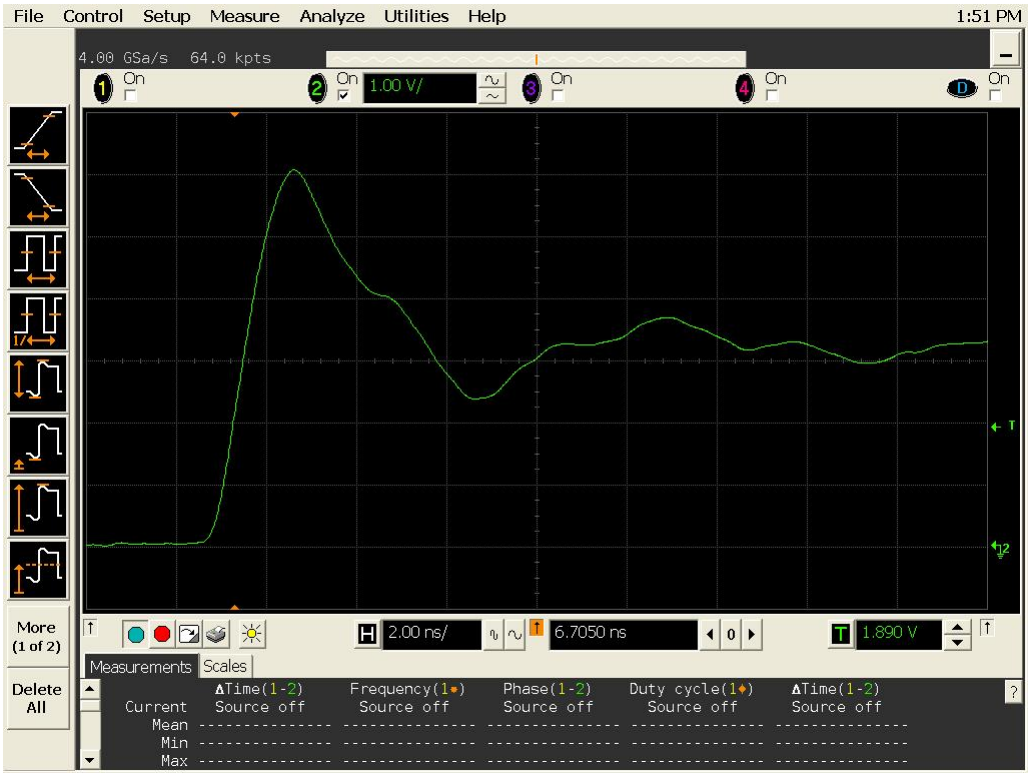


Figure 11b DUT 5877 Post-Annealing Rising Edge

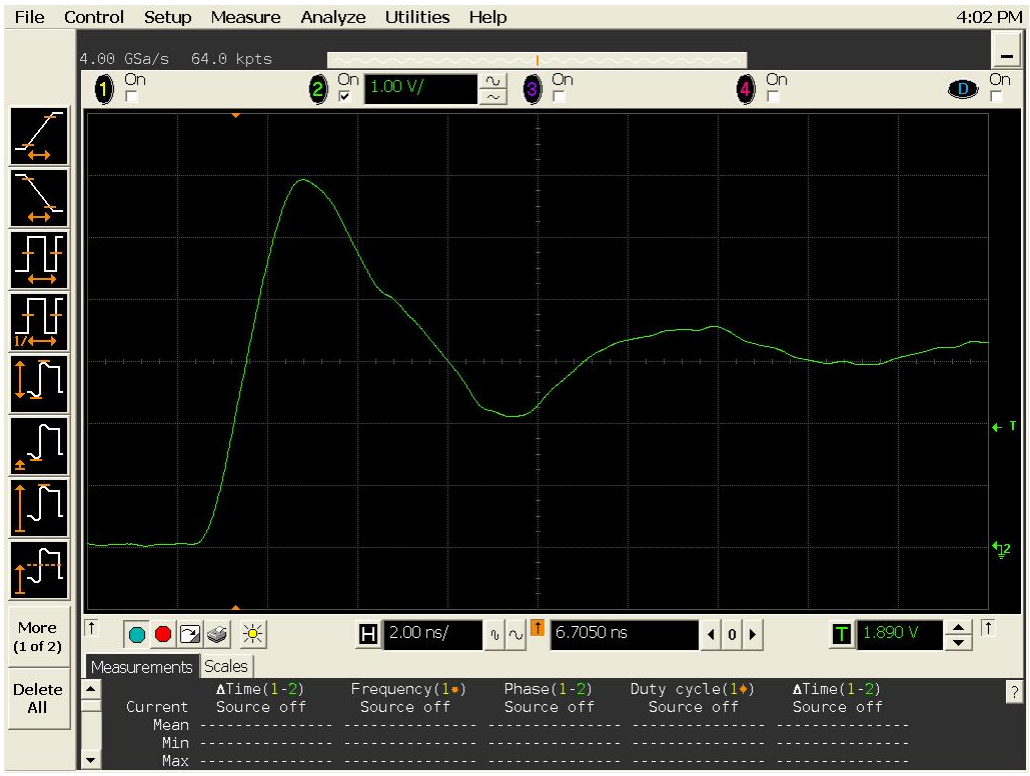


Figure 12a DUT 5895 Pre-Irradiation Rising Edge

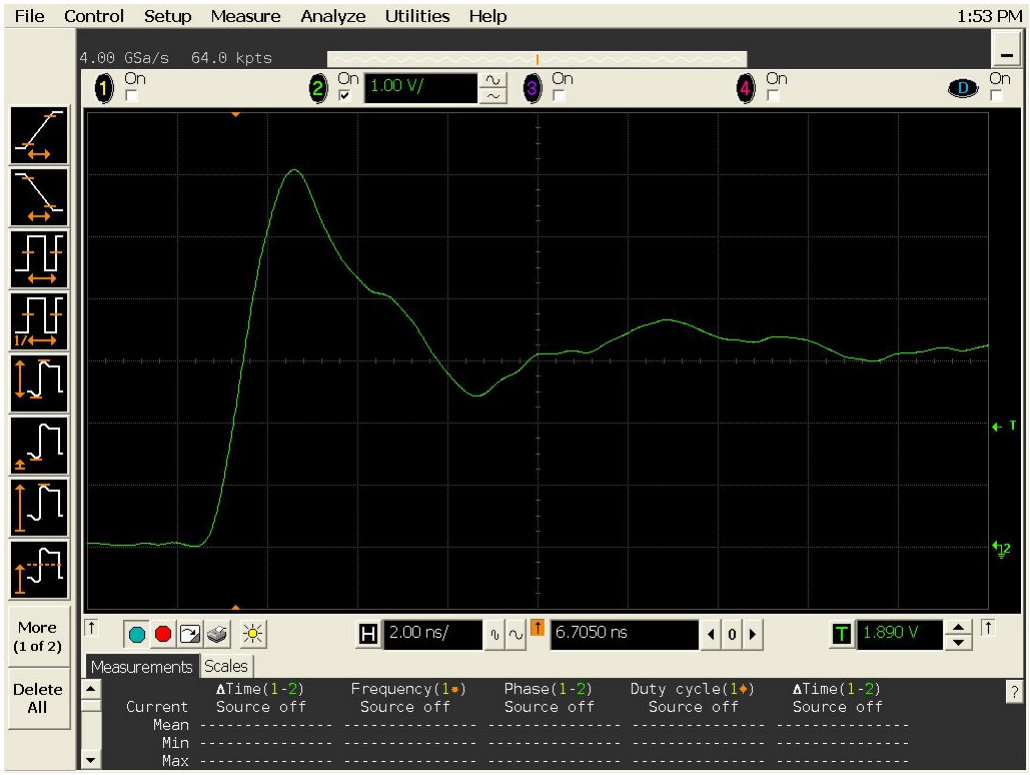


Figure 12b DUT 5895 Post-Annealing Rising Edge

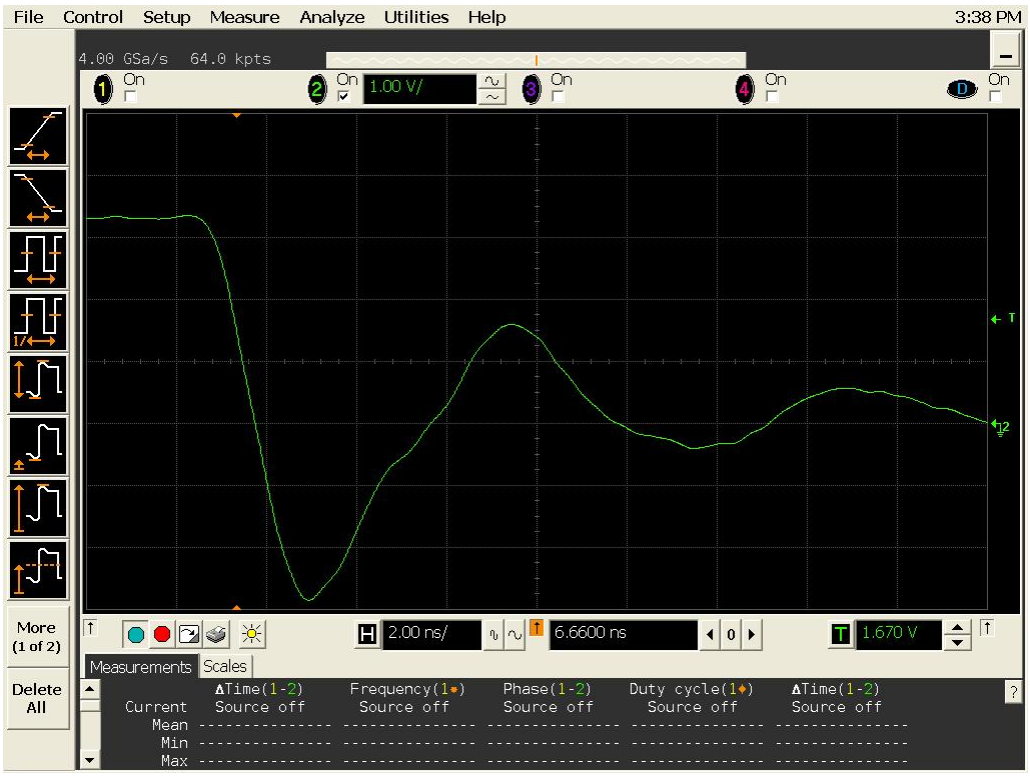


Figure 13a DUT 5852 Pre-Radiation Falling Edge

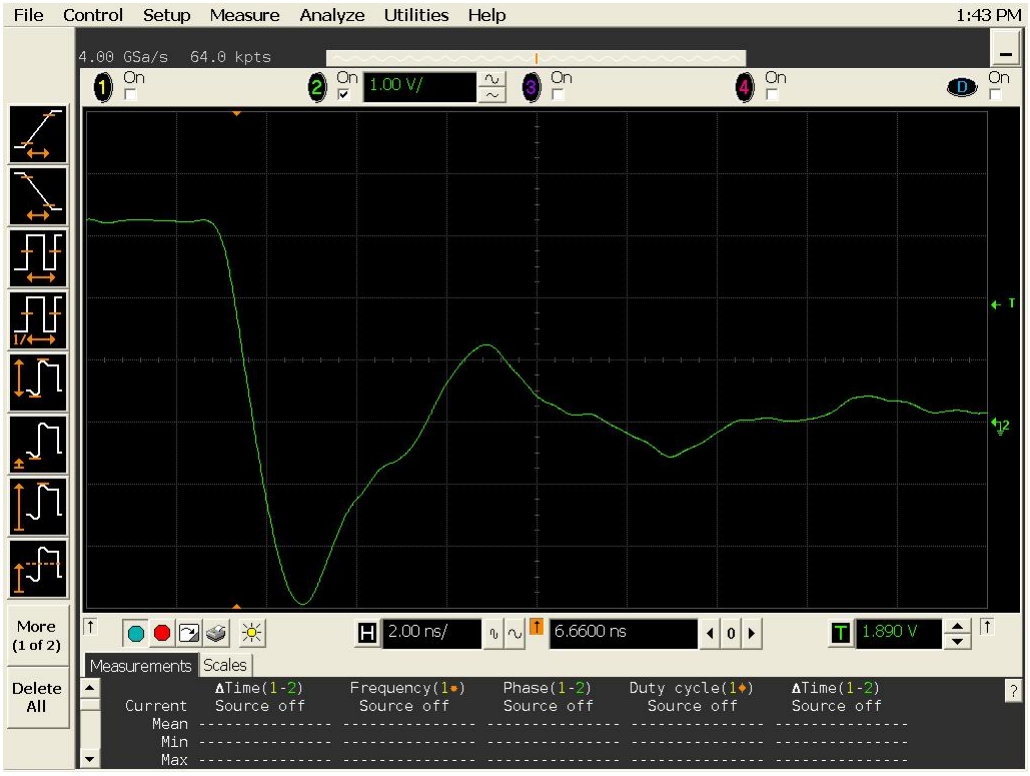


Figure 13b DUT 5852 Post-Annealing Falling Edge

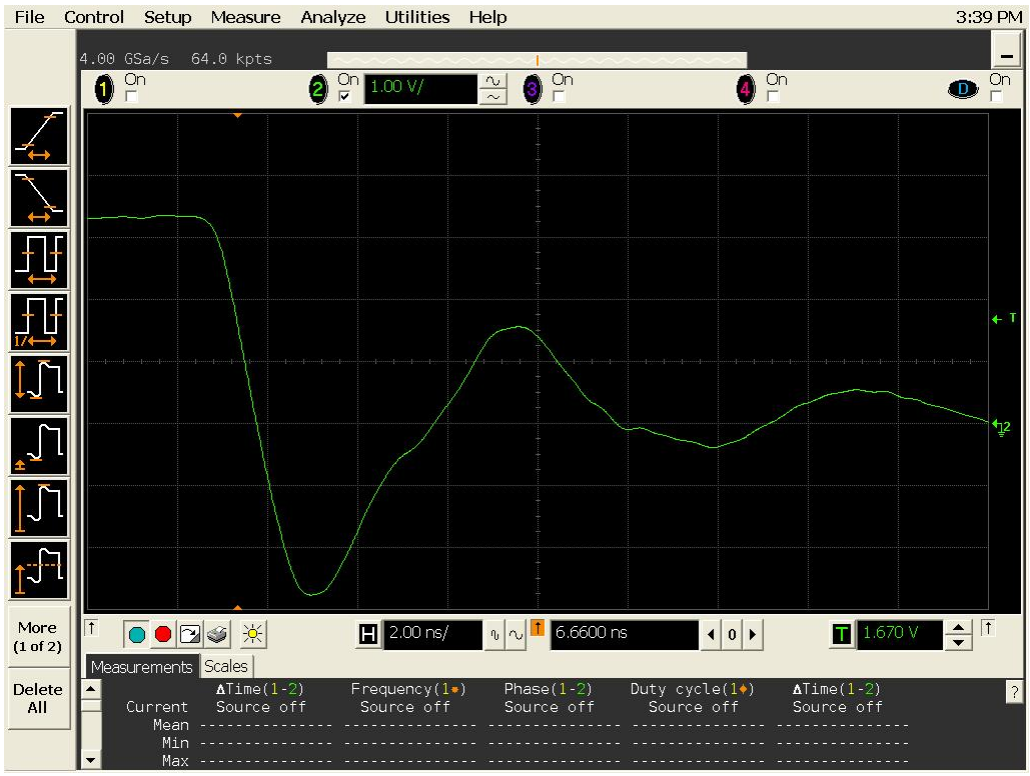


Figure 14a DUT 5858 Pre-Irradiation Falling Edge

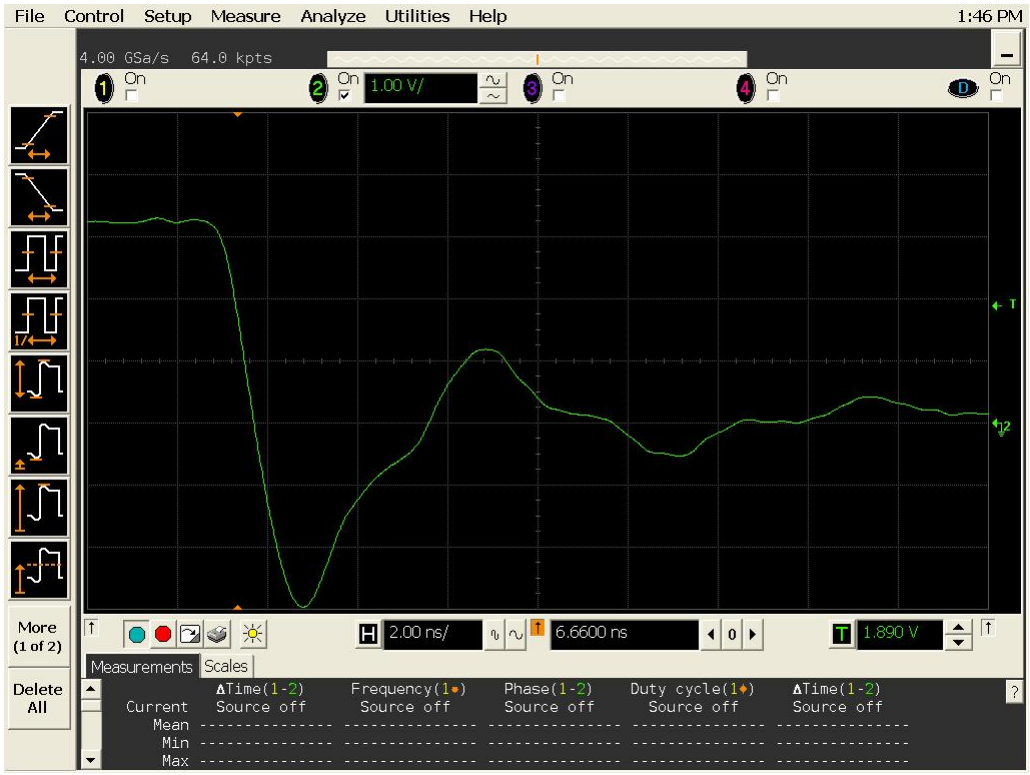


Figure 14b DUT 5858 Post-Annealing Falling Edge

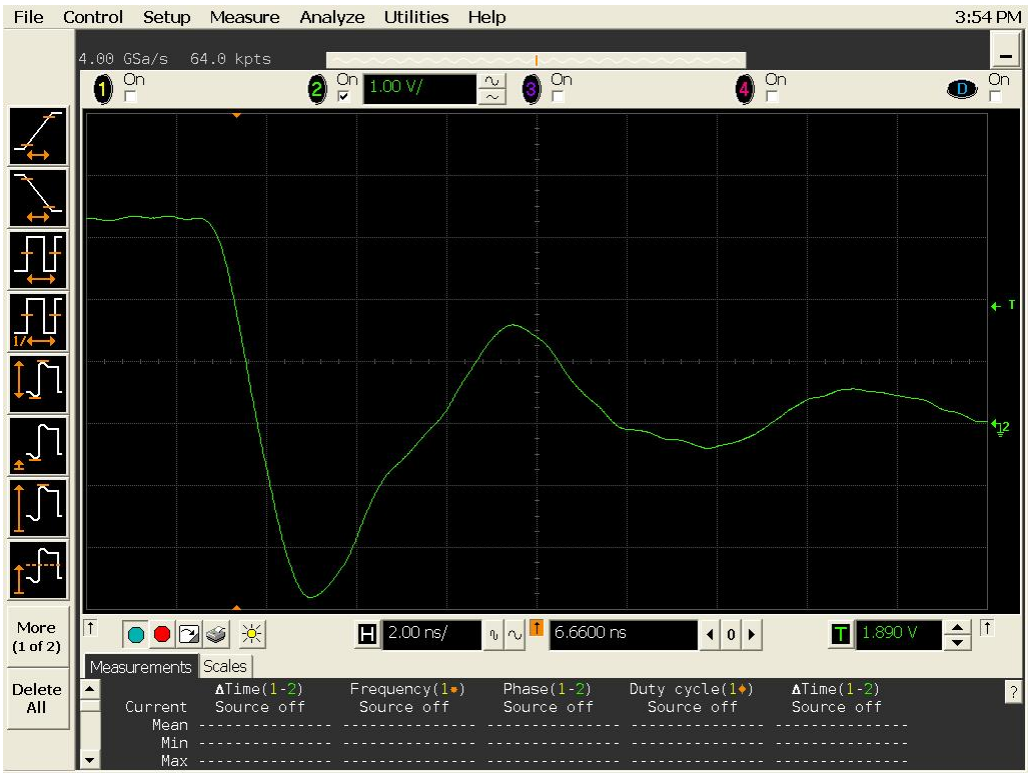


Figure 15a DUT 5860 Pre-Irradiation Falling Edge

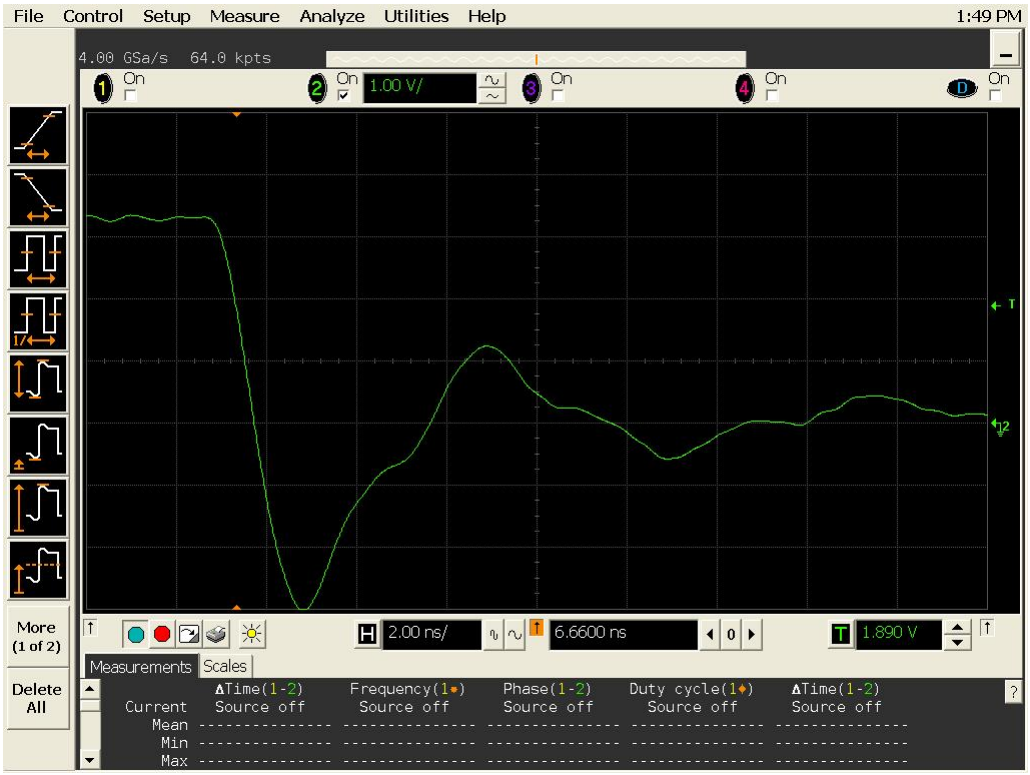


Figure 15b DUT 5860 Post-Annealing Falling Edge

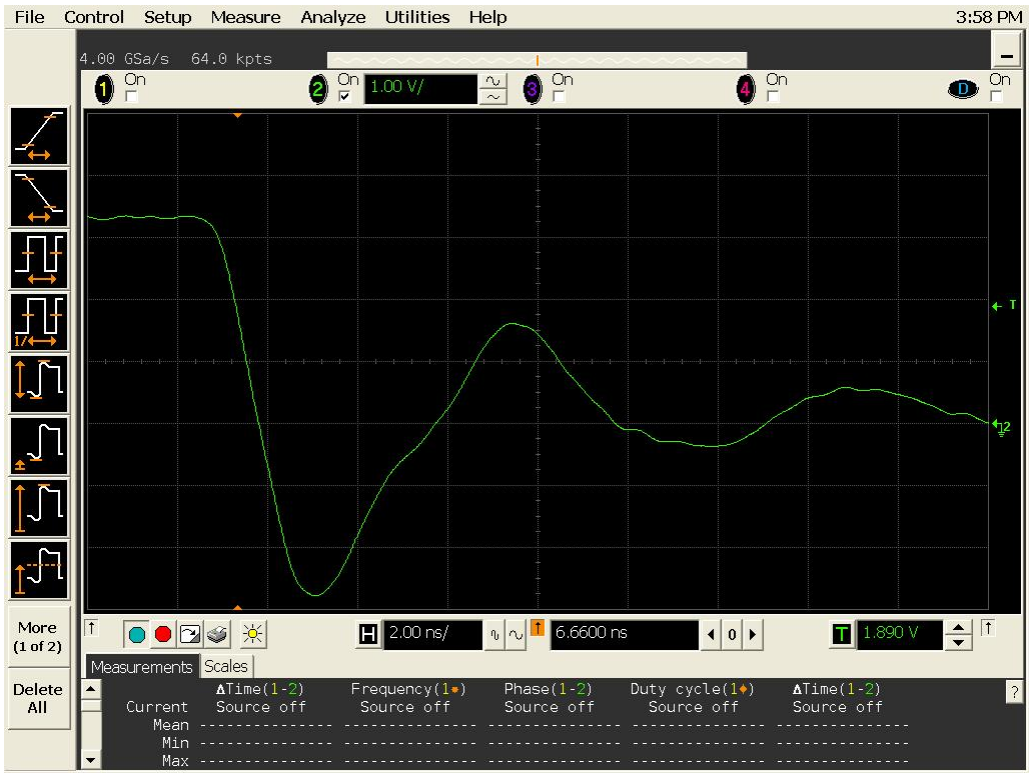


Figure 16a DUT 5877 Pre-Irradiation Falling Edge

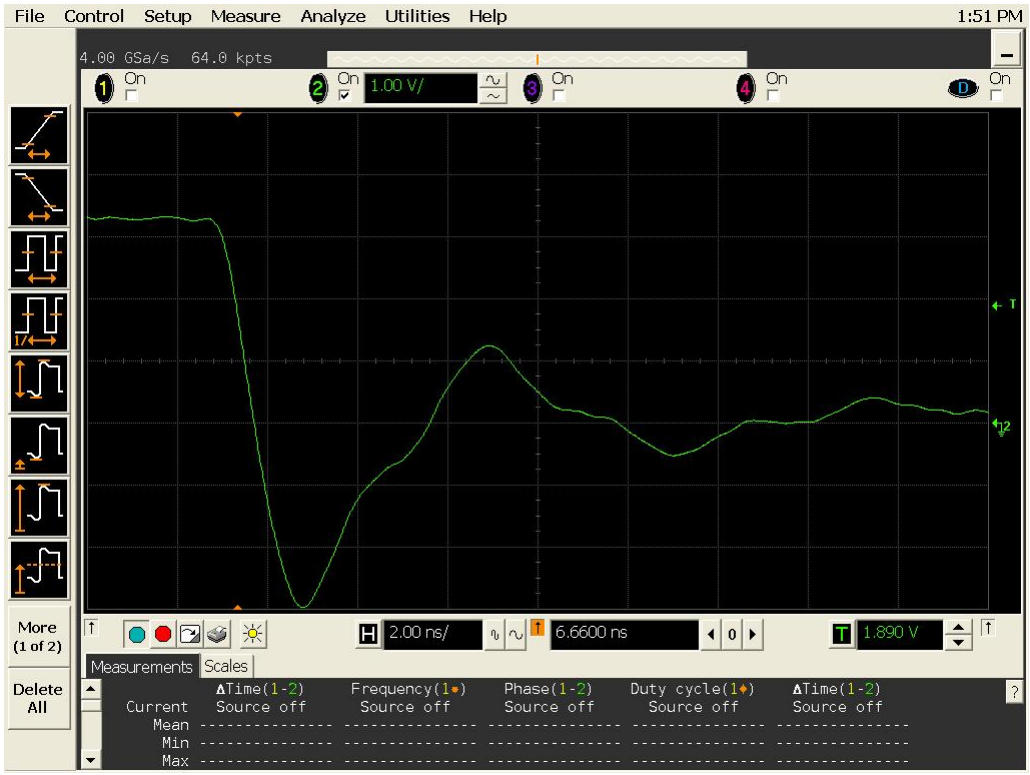


Figure 16b DUT 5877 Post-Annealing Falling Edge

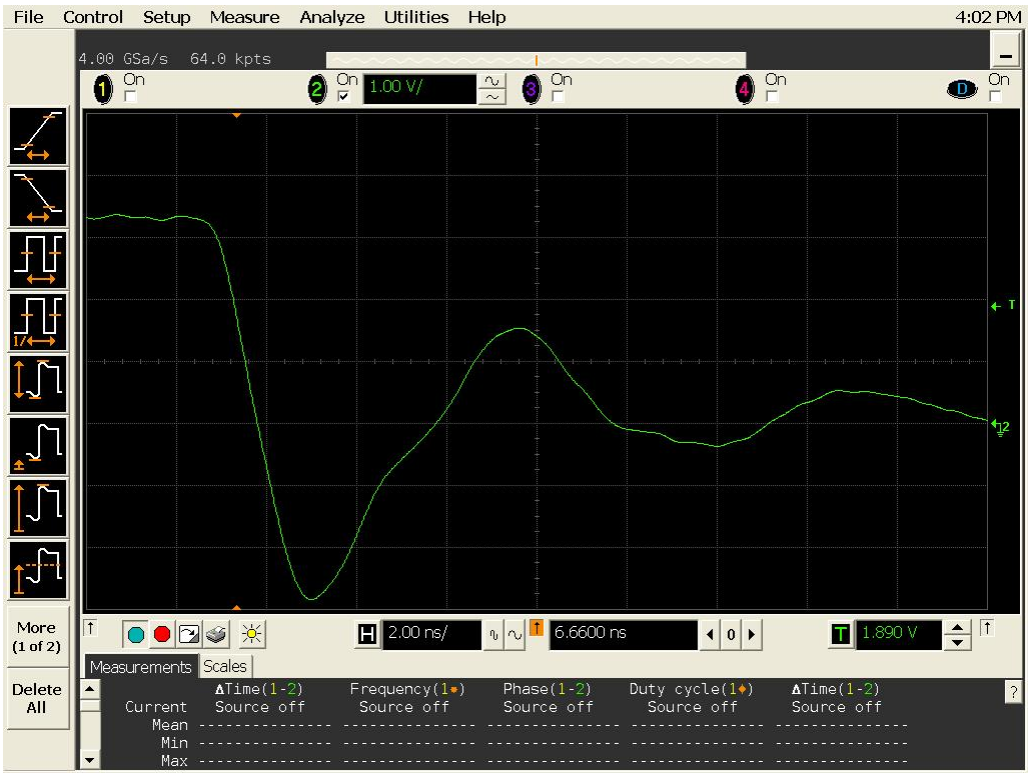


Figure 17a DUT 5895 Pre-Irradiation Falling Edge

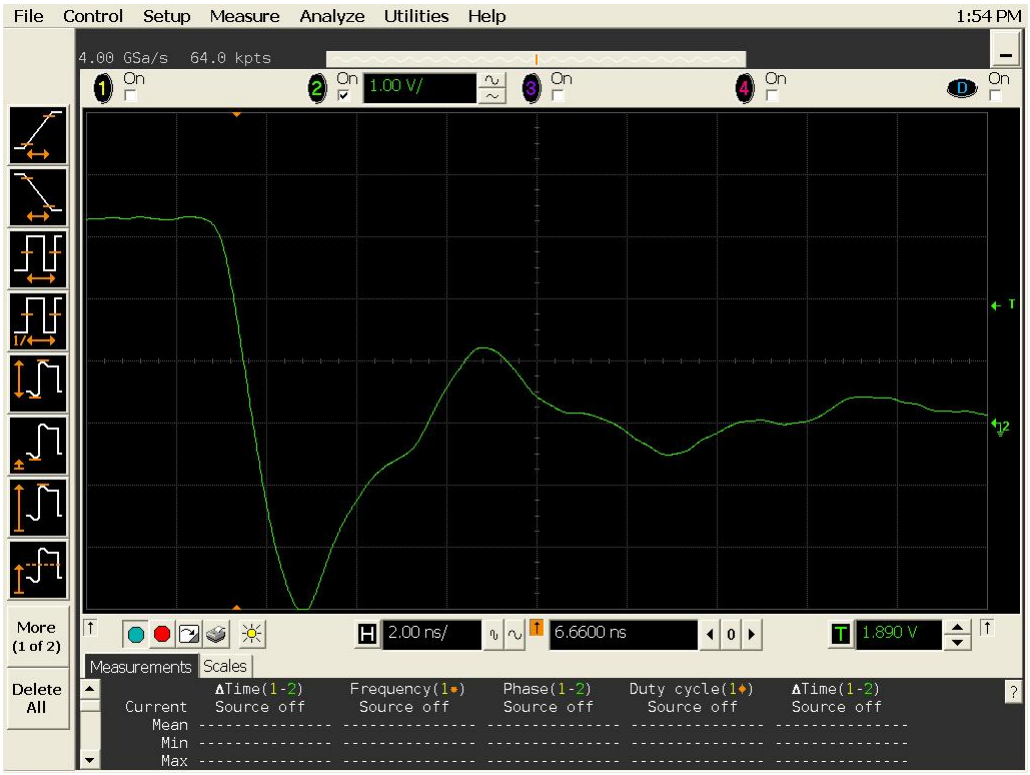
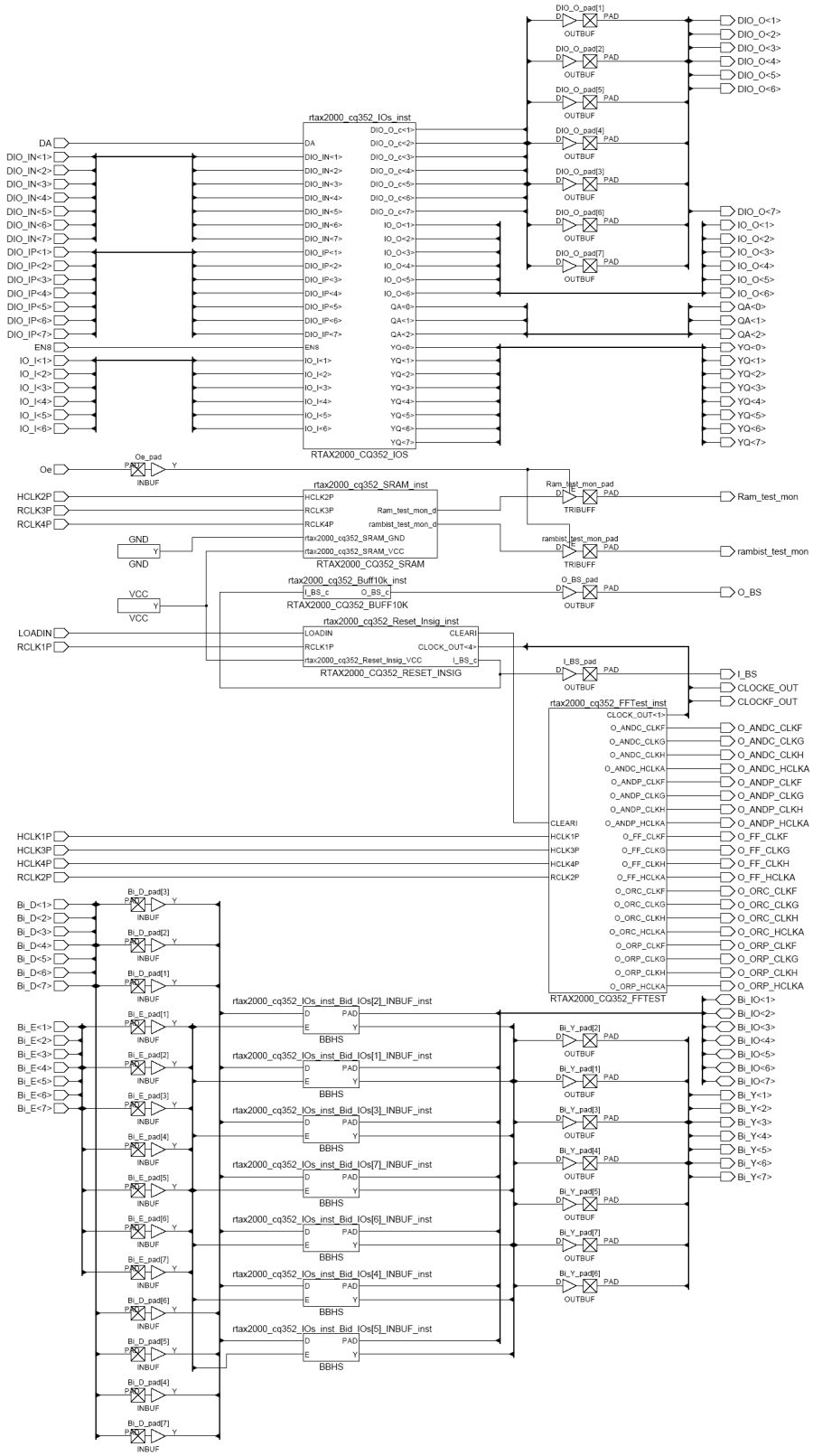


Figure 17b DUT 5895 Post-Annealing Falling Edge

Appendix A: DUT Design Schematics



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