

## TOTAL IONIZING DOSE TEST REPORT

*No. 07T-RTAX2000S-D2T2A1*  
*Sept. 5, 2007*  
*J.J. Wang*  
*(650) 318-4576*  
*[jih-jong.wang@actel.com](mailto:jih-jong.wang@actel.com)*

### I. SUMMARY TABLE

<b>Parameter</b>	<b>Tolerance</b>
1. Functionality	Passed 300 krad(SiO <sub>2</sub> )
2. Standby Power Supply Current (I <sub>CCA</sub> /I <sub>CCI</sub> )	Passed 200 krad(SiO <sub>2</sub> )
3. Input Threshold (V <sub>TIL</sub> /V <sub>IH</sub> )	Passed 300 krad(SiO <sub>2</sub> )
4. Output Threshold (V <sub>OL</sub> /V <sub>OH</sub> )	Passed 300 krad(SiO <sub>2</sub> )
5. Propagation Delay	Passed 300 krad(SiO <sub>2</sub> ) for ±10% degradation criterion
6. Transition Characteristic	Passed 300 krad(SiO <sub>2</sub> )

### II. TOTAL IONIZING DOSE (TID) TESTING

The design of the following testing is based on an extensive, published database accumulated from the TID testing of many generations of antifuse-based FPGAs; the link of the database is in below.

<http://www.actel.com/products/milaero/hireldata.aspx#tid>

#### A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. Each input is grounded during irradiation and annealing.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000S
Package	CG624
Foundry	United Microelectronics Corp.
Technology	0.15 μm CMOS
DUT Design	rtax2000(CG624)_Top
Die Lot Number	D2T2A1
Quantity Tested	6
Serial Number	300 krad(SiO <sub>2</sub> ): 3095, 3124, 3147 200 krad(SiO <sub>2</sub> ): 3148, 3149, 3176
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	5 krad(SiO <sub>2</sub> )/min
Irradiation Temperature	Room
Irradiation and Annealing Bias V <sub>CCI</sub> /V <sub>CCA</sub>	Static at 3.3 V/1.5 V
IO Configuration	Single ended: LVTTL Differential pair: LVPECL

## B. Test Method

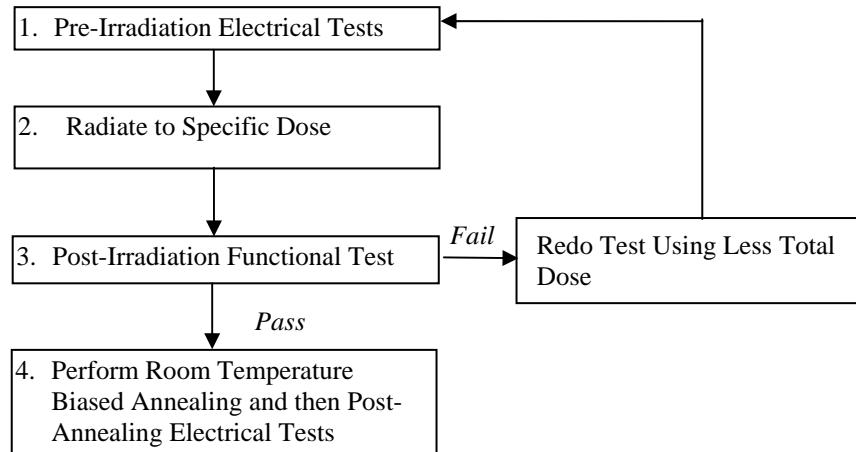


Figure 1 Parametric test flow chart

The test method basically is in compliance with the military standard TM1019.6. Figure 1 is the flow chart of the testing sequence. The accelerated annealing test in section 3.12 is not performed lot-to-lot. This is because for a deep-submicron CMOS technology used by the RTAXS product, the adverse effects due to interface state at the gate  $\text{SiO}_2/\text{Si}$  interface are negligible. The function of commercial non-irradiated transistors would be unreliable if the degradation of interface plays an important role. In other words, the  $\text{SiO}_2/\text{Si}$  interface in deep submicron CMOS transistors has to be radiation hard for even commercial applications. Thus the dominant annealing effect in RTAXS device is the reduction of trapped holes in the  $\text{SiO}_2$ ; this basically alleviates the radiation effects on the DUT. Separate report on the accelerated annealing test will be provided to justify the omission of it in the lot testing; the justification testing will follow section 3.12.1.b.5.

Section 3.11 extended room temperature anneal test is also applied; room temperature annealing for 5 days was done on each device before the final parameter measurements.

## C. Logic Design and Electrical Parameter Measurements

The DUT uses a high utilization generic design, rtax2000\_CG624\_Top, for testing total dose effects. These logic designs are described in the following subsections. Figure 2 shows the block diagram and the Verilog file (rtax2000\_CG624\_Top.v) is in the link:

<http://www.actel.com/products/milaero/hireldata.aspx#tid>

Generally, the functional test is performed on every design; most inputs are tested for threshold voltage and leakage current, including global clocks; the standby  $I_{\text{CC}}$  includes  $I_{\text{CCI}}$  and  $I_{\text{CCA}}$ . Except propagation delay and the transition characteristic, which is measured on the output  $O_{\text{BS}}$ , all other parameter measurements are done on a tester. Also note that, due to logistics limitation, the post-irradiation but pre-room-temperature-annealing functional test is performed on bench; the tested designs are shift registers and long buffer string, which are design 5 and 6 described in the following.

### 1. Embedded SRAM

This design is to test the function of the embedded SRAM. It uses all the RAM blocks available in the DUT. This design enables an automatic testing sequence that every bit is written and then read. Any error will be reported as a signal in the output.

### 2. Unidirectional LVTTL Input and Output

This is for testing radiation effects on unidirectional input and output threshold, leakage, and buffer fan-out. There are 3 sub-designs: a) a logic-core buffer with 8 fan-outs; b) a logic-core buffer with 3 fan-outs; c) 6 channels of input buffer directly connected to output buffer without core logic. LVTTL is used because it is the worst case among all the single-ended standards.

### 3. Bidirectional LVTTL IO

This design is for testing the radiation effects on the input/output characteristic of the bidirectional IO. There are 7 channels of bidirectional IO for radiation effects testing.

### 4. LVPECL Input

This design is for testing the radiation effects on the LVPECL differential inputs. 3.3V-LVPECL is considered the worst case differential input standard in the DUT. There are 7 channels.

### 5. Shift Registers

This design is to test the radiation effects on the function of flip-flops, which are configured R-Cells. There are 4 shift registers and each using a different global clock; one has 3,584 bits and the other three each has 2,048 bits.

### 6. Long Buffer String

This design is to measure the radiation effects on the propagation delay. The input of the design using a clock feeding a toggle flip-flop to generate a checkerboard signal; this signal is then fed into a buffer string with 10,000 stages. The time delay between the input clock edge at CLOCK\_IN and the output switching due to this clock edge at O\_BS is defined as propagation delay high to low ( $T_{pdhl}$ ) or low to high ( $T_{pdlh}$ ); the percentage change of the average of  $T_{pdhl}$  and  $T_{pdlh}$  is used to determine the radiation effects. A more than 10% of propagation change is considered as failure.

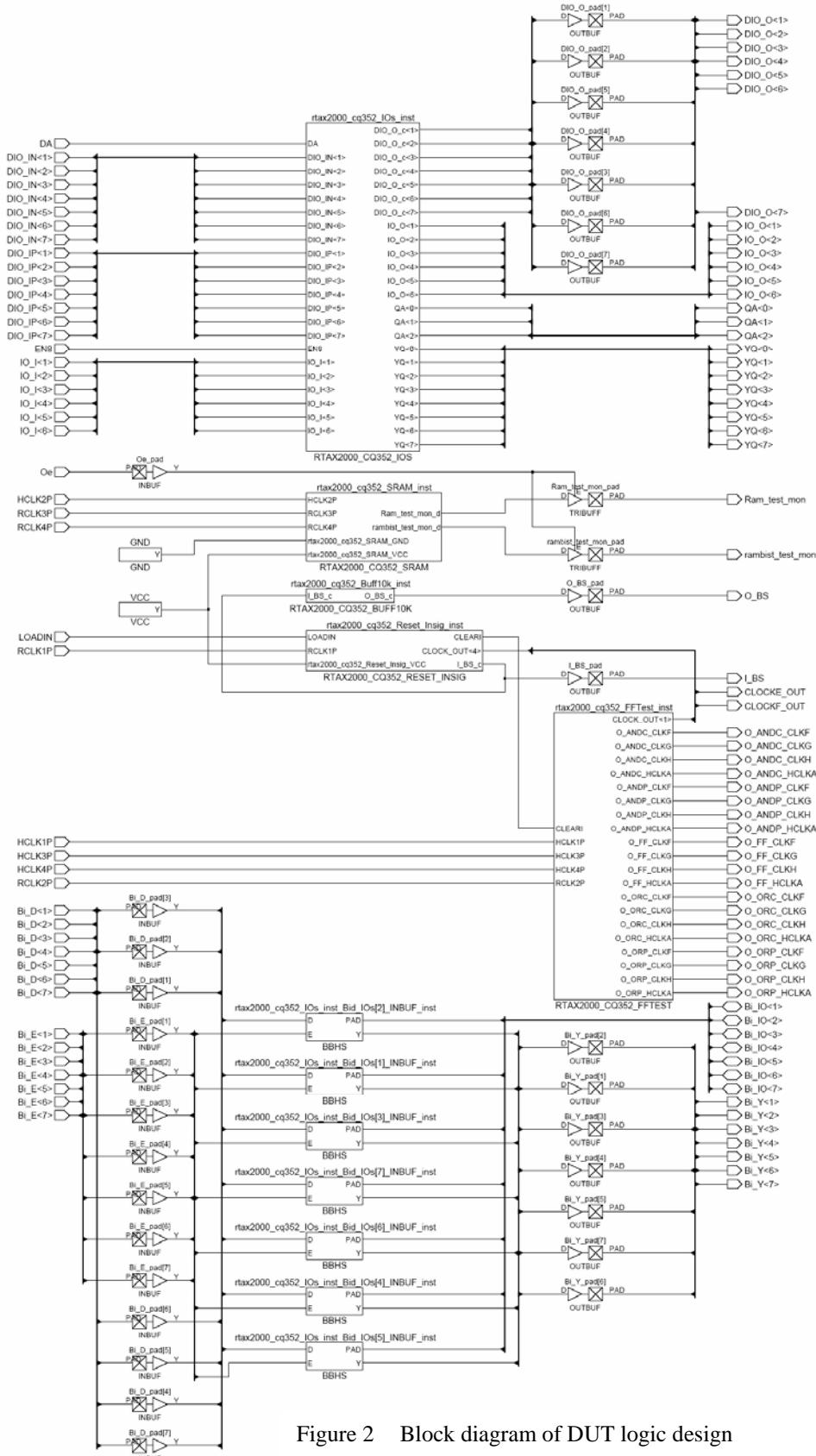


Figure 2 Block diagram of DUT logic design

### III. TEST RESULTS

#### A. Functional Test

Every DUT passed the pre-irradiation and post-annealing functional tests on the tester; it also passed post-irradiation test on-bench.

#### B. Standby Power Supply Current ( $I_{CCA}$ and $I_{CCI}$ )

Figure 3-8 show the in-flux standby  $I_{CCA}$  and  $I_{CCI}$  versus total dose of every DUT.

In compliance with TM1019.6 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing  $I_{CC}$  in this test is defined as the addition of highest  $I_{CCI}$ ,  $I_{CCDA}$  and  $I_{CCDIFFA}$  values in Table 2-4 of the RTAXS spec sheet:

[http://www.actel.com/documents/RTAXS\\_DS.pdf](http://www.actel.com/documents/RTAXS_DS.pdf)

Thus for  $I_{CCA}$ , the PIPL is 500 mA; the PIPL of  $I_{CCI}$  equals to  $35+10+3.13\times7 = 66.91$ (mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT.

Table 2 summarizes the pre-irradiation, post-irradiation and post-annealing  $I_{CC}$  data: the post-annealing  $I_{CCA}$  of every DUT pass the PIPL easily; the post-annealing  $I_{CCI}$  of DUTs irradiated to 200 krad( $\text{SiO}_2$ ) all pass the PIPL, while the  $I_{CCI}$  of DUTs irradiated to 300 krad( $\text{SiO}_2$ ) all exceed the PIPL.

Table 2 Pre-irradiation, Post Irradiation and Post-Annealing  $I_{CC}$

DUT	Total Dose krad ( $\text{SiO}_2$ )	$I_{CCA}$ (mA)			$I_{CCI}$ (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
3095	300	9.6	30.2	9.1	25.6	255	112
3124	300	4.5	140	12.2	25.5	289	233
3147	300	9.0	40	9.0	26.0	267	136
3148	200	7.6	7.9	7.8	25.5	80	40.1
3149	200	2.0	2.35	1.4	24.5	139	60.0
3176	200	7.5	7.1	8.5	25.2	94	44.1

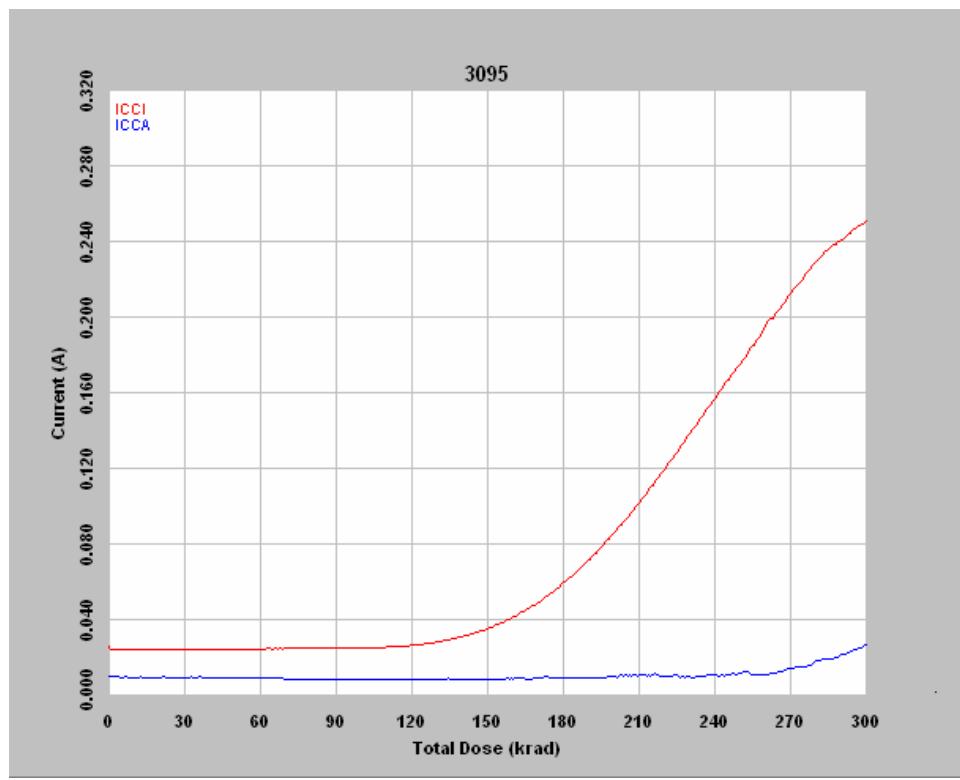


Figure 3 DUT 3095 in-flux  $I_{CCA}$  and  $I_{CCI}$ . The spikes are due to bad contacts.

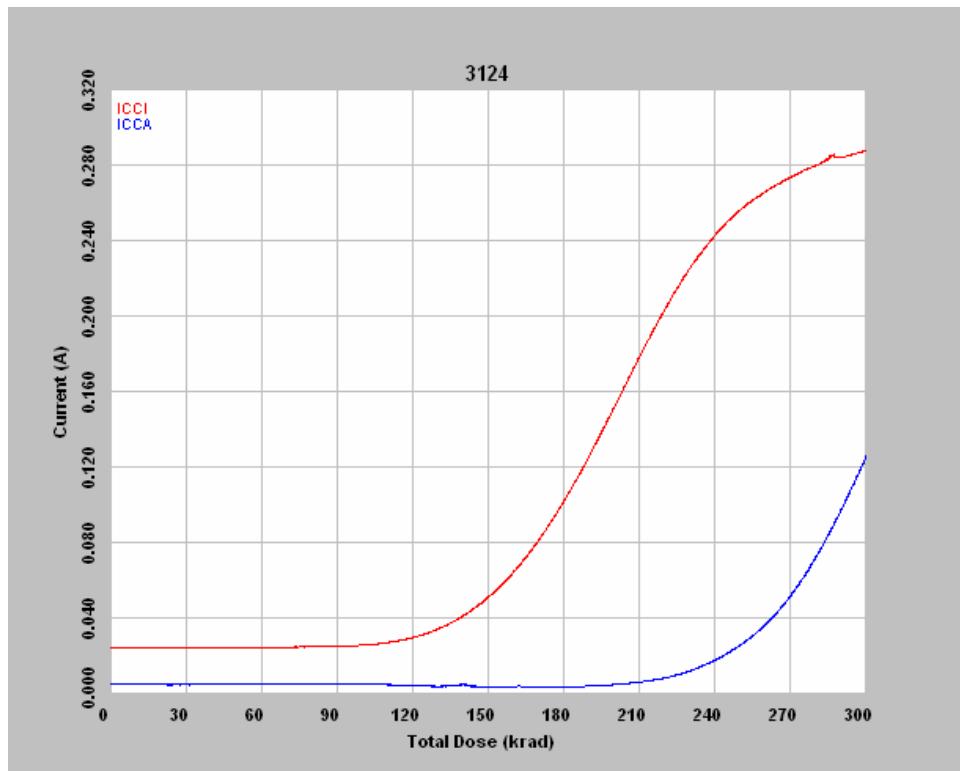


Figure 4 DUT 3124 in-flux  $I_{CCA}$  and  $I_{CCI}$

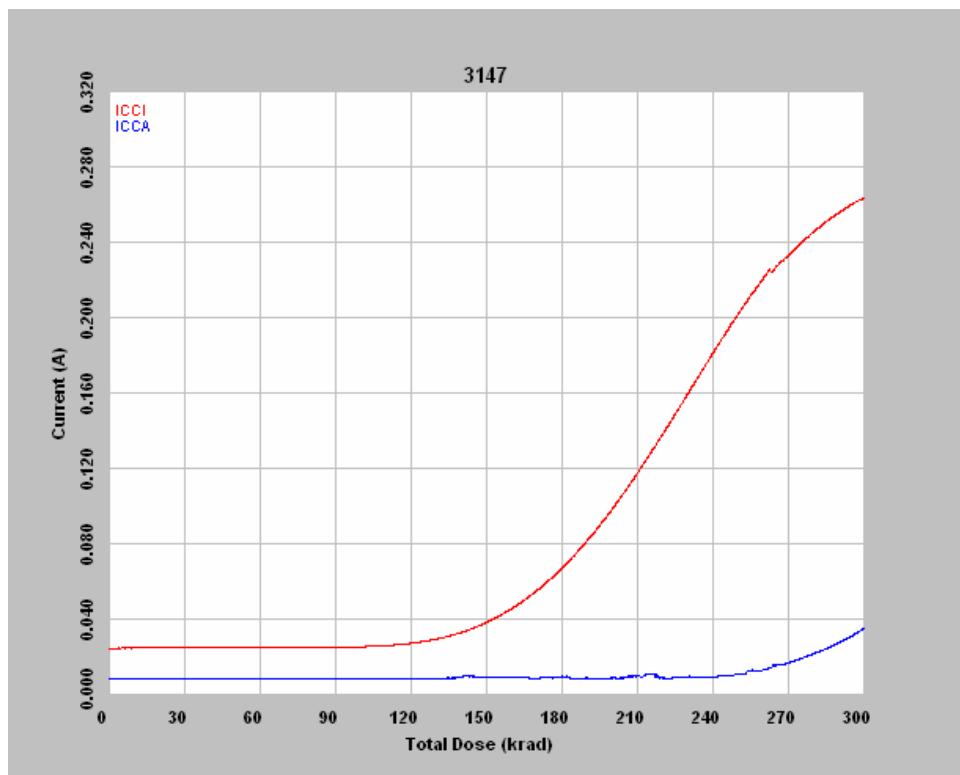


Figure 5 DUT 3147 in-flux I<sub>CCA</sub> and I<sub>CCI</sub>

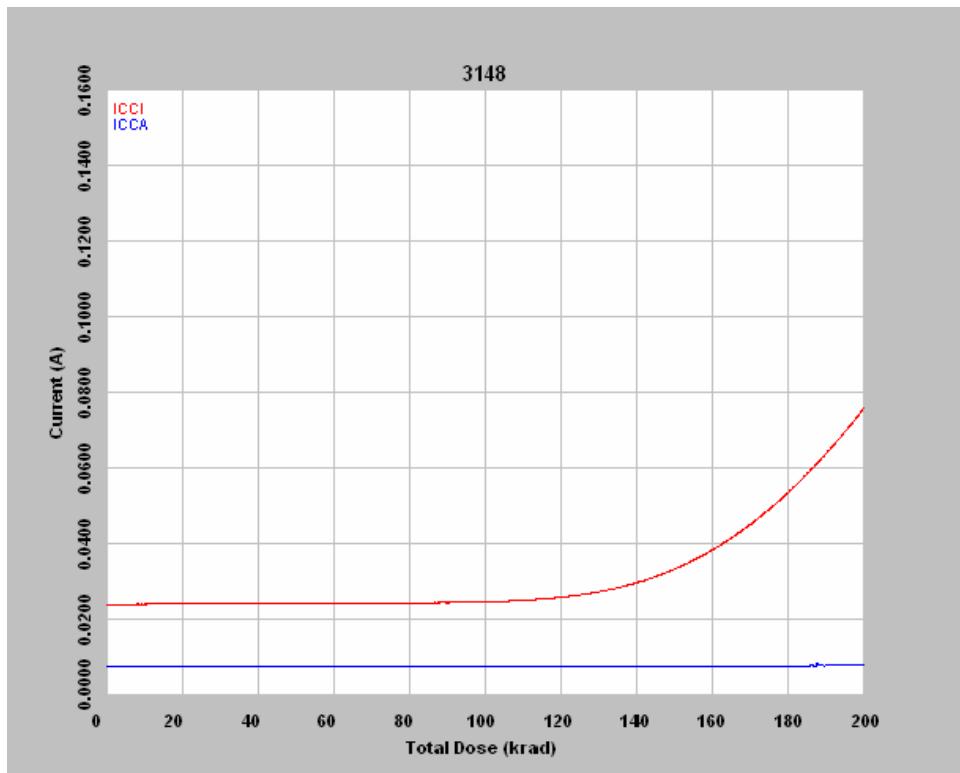


Figure 6 DUT 3148 in-flux I<sub>CCA</sub> and I<sub>CCI</sub>

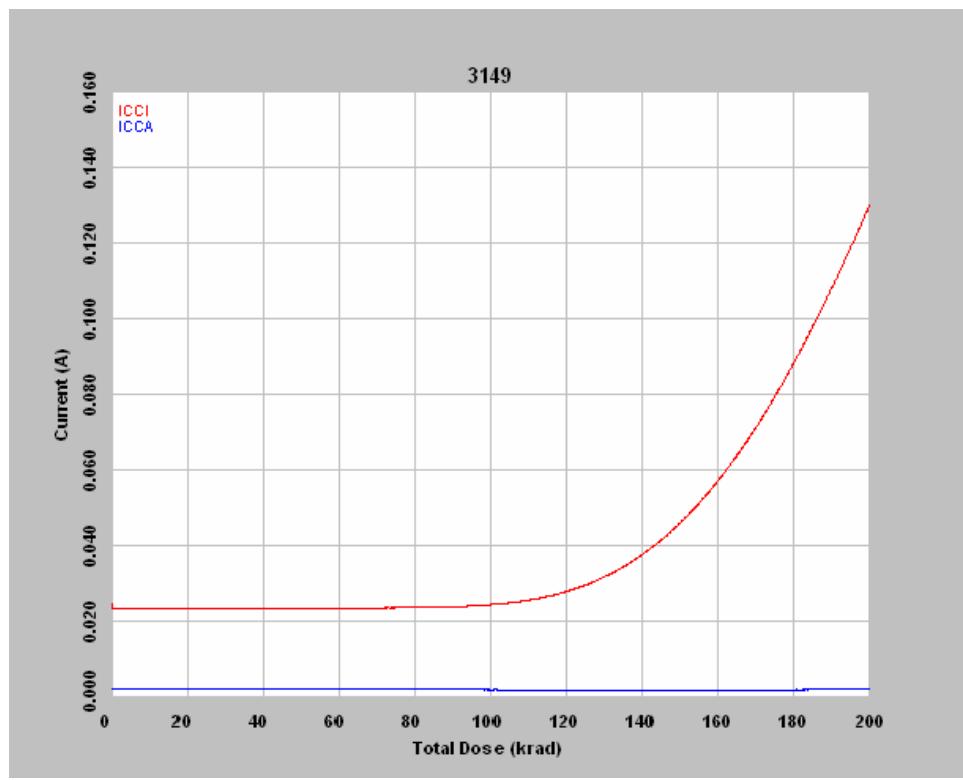


Figure 7 DUT 3149 in-flux I<sub>CCA</sub> and I<sub>cci</sub>

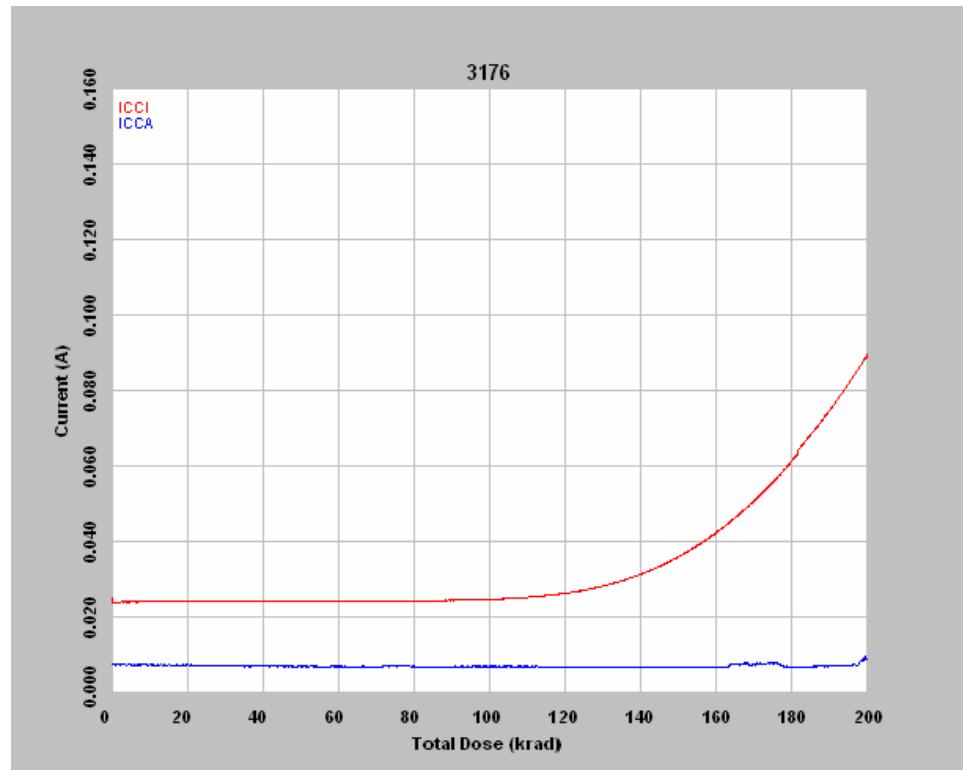


Figure 8 DUT 3176 in-flux I<sub>CCA</sub> and I<sub>cci</sub>

### C. Single-Ended $V_{IL}/V_{IH}$ and $I_{IL}/I_{IH}$

Table 3 displays the pre-irradiation and post-annealing single-ended  $V_{IL}$ ; every data in this table passes the spec. Table 4 displays the pre-irradiation and post-annealing single-ended  $V_{IH}$ ; every data in this table passes the spec.

Table 5 displays the pre-irradiation and post-annealing single-ended  $I_{IL}$ ; every data in the table passes the spec. Table 6 displays the pre-irradiation and post-annealing single-ended  $I_{IH}$ ; every data in the table passes the spec. The PIPL for both  $I_{IL}$  and  $I_{IH}$  is 5  $\mu$ A.

Table 3a

DUT		3095		3124		3147	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	Bi_D_7	1.38	1.37	1.385	1.375	1.375	1.37
bi_levels_vil	Bi_D_6	1.36	1.355	1.365	1.36	1.36	1.355
bi_levels_vil	Bi_D_5	1.37	1.365	1.375	1.365	1.375	1.365
bi_levels_vil	Bi_D_4	1.38	1.37	1.38	1.37	1.375	1.365
bi_levels_vil	Bi_D_3	1.37	1.365	1.375	1.365	1.37	1.365
bi_levels_vil	Bi_D_2	1.37	1.365	1.37	1.365	1.37	1.36
bi_levels_vil	Bi_D_1	1.365	1.36	1.37	1.36	1.365	1.355
bi_levels_vil	DA	1.385	1.385	1.385	1.385	1.385	1.37
bi_levels_vil	EN8	1.355	1.355	1.355	1.345	1.345	1.335
bi_levels_vil	IO_I_6	1.365	1.355	1.36	1.355	1.36	1.355
bi_levels_vil	IO_I_5	1.355	1.355	1.355	1.355	1.34	1.345
bi_levels_vil	IO_I_4	1.405	1.395	1.4	1.39	1.395	1.39
bi_levels_vil	IO_I_3	1.395	1.395	1.38	1.39	1.395	1.385
bi_levels_vil	IO_I_2	1.4	1.395	1.4	1.395	1.395	1.39
bi_levels_vil	IO_I_1	1.395	1.39	1.4	1.39	1.39	1.395
bi_levels_vil	RCLK1P	1.445	1.44	1.445	1.44	1.44	1.435
bi_levels_vil	RCLK2P	1.445	1.44	1.445	1.44	1.44	1.435

Table 3b

DUT		3148		3149		3176	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	Bi_D_7	1.38	1.37	1.38	1.37	1.38	1.37
bi_levels_vil	Bi_D_6	1.365	1.355	1.365	1.355	1.36	1.355
bi_levels_vil	Bi_D_5	1.375	1.365	1.375	1.365	1.37	1.365
bi_levels_vil	Bi_D_4	1.38	1.375	1.375	1.37	1.375	1.37
bi_levels_vil	Bi_D_3	1.37	1.365	1.375	1.365	1.37	1.36
bi_levels_vil	Bi_D_2	1.37	1.365	1.365	1.36	1.365	1.36
bi_levels_vil	Bi_D_1	1.37	1.36	1.365	1.36	1.365	1.36
bi_levels_vil	DA	1.38	1.385	1.385	1.385	1.385	1.365
bi_levels_vil	EN8	1.345	1.34	1.345	1.34	1.355	1.335
bi_levels_vil	IO_I_6	1.365	1.36	1.355	1.355	1.355	1.36
bi_levels_vil	IO_I_5	1.355	1.35	1.345	1.35	1.345	1.345
bi_levels_vil	IO_I_4	1.4	1.395	1.39	1.39	1.39	1.39
bi_levels_vil	IO_I_3	1.4	1.395	1.385	1.395	1.395	1.385
bi_levels_vil	IO_I_2	1.4	1.395	1.395	1.39	1.395	1.39
bi_levels_vil	IO_I_1	1.405	1.395	1.395	1.395	1.395	1.385
bi_levels_vil	RCLK1P	1.445	1.44	1.44	1.435	1.445	1.44
bi_levels_vil	RCLK2P	1.445	1.44	1.44	1.435	1.445	1.44

Table 4a

DUT		3095		3124		3147	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	Bi_D_7	1.38	1.37	1.38	1.375	1.375	1.365
bi_levels_vih	Bi_D_6	1.385	1.38	1.385	1.38	1.385	1.38
bi_levels_vih	Bi_D_5	1.38	1.375	1.385	1.365	1.38	1.375
bi_levels_vih	Bi_D_4	1.38	1.37	1.38	1.37	1.375	1.365
bi_levels_vih	Bi_D_3	1.385	1.38	1.385	1.38	1.385	1.38
bi_levels_vih	Bi_D_2	1.385	1.38	1.385	1.38	1.385	1.375
bi_levels_vih	Bi_D_1	1.385	1.375	1.38	1.375	1.38	1.37
bi_levels_vih	DA	1.4	1.395	1.4	1.39	1.39	1.39
bi_levels_vih	EN8	1.455	1.445	1.45	0	1.445	1.44
bi_levels_vih	IO_I_6	1.415	1.41	1.42	1.45	1.415	1.41
bi_levels_vih	IO_I_5	1.43	1.42	1.43	1.415	1.43	1.395
bi_levels_vih	IO_I_4	1.395	1.39	1.395	1.43	1.39	1.385
bi_levels_vih	IO_I_3	1.405	1.4	1.405	1.385	1.4	1.395
bi_levels_vih	IO_I_2	1.395	1.39	1.395	1.4	1.39	1.385
bi_levels_vih	IO_I_1	1.405	1.395	1.405	1.39	1.4	1.395
bi_levels_vih	RCLK1P	1.44	1.43	1.435	1.4	1.435	1.425
bi_levels_vih	RCLK2P	1.445	1.435	1.445	1.43	1.44	1.43

Table 4b

DUT		3148		3149		3176	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	Bi_D_7	1.38	1.37	1.38	1.37	1.38	1.37
bi_levels_vih	Bi_D_6	1.365	1.355	1.365	1.355	1.36	1.355
bi_levels_vih	Bi_D_5	1.375	1.365	1.375	1.365	1.37	1.365
bi_levels_vih	Bi_D_4	1.38	1.375	1.375	1.37	1.375	1.37
bi_levels_vih	Bi_D_3	1.37	1.365	1.375	1.365	1.37	1.36
bi_levels_vih	Bi_D_2	1.37	1.365	1.365	1.36	1.365	1.36
bi_levels_vih	Bi_D_1	1.37	1.36	1.365	1.36	1.365	1.36
bi_levels_vih	DA	1.38	1.385	1.385	1.385	1.385	1.365
bi_levels_vih	EN8	1.345	1.34	1.345	1.34	1.355	1.335
bi_levels_vih	IO_I_6	1.365	1.36	1.355	1.355	1.355	1.36
bi_levels_vih	IO_I_5	1.355	1.35	1.345	1.35	1.345	1.345
bi_levels_vih	IO_I_4	1.4	1.395	1.39	1.39	1.39	1.39
bi_levels_vih	IO_I_3	1.4	1.395	1.385	1.395	1.395	1.385
bi_levels_vih	IO_I_2	1.4	1.395	1.395	1.39	1.395	1.39
bi_levels_vih	IO_I_1	1.405	1.395	1.395	1.395	1.395	1.385
bi_levels_vih	RCLK1P	1.445	1.44	1.44	1.435	1.445	1.44
bi_levels_vih	RCLK2P	1.445	1.44	1.44	1.435	1.445	1.44

Table 5a

DUT		3095		3124		3147							
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann						
IIL_Inputs_Max_	Bi_D_1	2.0	nA	-506.2	pA	-1.3	nA	-1.6	nA	-2.4	nA	-1.3	nA
IIL_Inputs_Max_	Bi_D_2	2.4	nA	-296.9	pA	2.6	nA	749.4	pA	-506.2	pA	958.7	pA
IIL_Inputs_Max_	Bi_D_3	3.1	nA	330.9	pA	1.8	nA	3.9	nA	3.1	nA	2.6	nA
IIL_Inputs_Max_	Bi_D_4	-3.0	nA	-3.4	nA	-4.1	nA	-7.0	nA	-2.6	nA	-2.4	nA
IIL_Inputs_Max_	Bi_D_5	-2.6	nA	-4.1	nA	-77.4	pA	-2.8	nA	-3.6	nA	-3.6	nA
IIL_Inputs_Max_	Bi_D_6	-3.6	nA	-5.1	nA	-4.0	nA	-3.2	nA	-4.4	nA	-4.2	nA
IIL_Inputs_Max_	Bi_D_7	-3.0	nA	-4.3	nA	-2.8	nA	-5.1	nA	-4.1	nA	-3.9	nA
IIL_Inputs_Max_	Bi_E_1	-1.8	nA	-1.4	nA	-3.4	nA	-2.4	nA	-1.1	nA	-1.8	nA
IIL_Inputs_Max_	Bi_E_2	-97.5	pA	-2.6	nA	-1.4	nA	-1.6	nA	-2.4	nA	-3.4	nA
IIL_Inputs_Max_	Bi_E_3	-516.4	pA	-1.6	nA	-1.8	nA	-4.1	nA	-935.2	pA	-1.4	nA
IIL_Inputs_Max_	Bi_E_4	-935.2	pA	-2.0	nA	-2.2	nA	-1.8	nA	-3.0	nA	-4.1	nA
IIL_Inputs_Max_	Bi_E_5	-2.0	nA	-2.6	nA	-2.8	nA	-2.8	nA	-1.6	nA	-2.2	nA
IIL_Inputs_Max_	Bi_E_6	-2.6	nA	-3.7	nA	-935.2	pA	-4.1	nA	-3.4	nA	-4.3	nA
IIL_Inputs_Max_	Bi_E_7	-2.2	nA	-2.6	nA	-2.4	nA	-3.4	nA	-2.0	nA	-4.5	nA
IIL_Inputs_Max_	DA	-4.2	nA	-3.3	nA	-5.2	nA	-4.8	nA	-4.6	nA	-4.8	nA
IIL_Inputs_Max_	DIO_IN_1	792.8	pA	-2.8	nA	-1.7	nA	-1.1	nA	2.0	nA	583.5	pA
IIL_Inputs_Max_	DIO_IN_2	-3.9	nA	-4.8	nA	-3.9	nA	-1.4	nA	-4.6	nA	-2.7	nA
IIL_Inputs_Max_	DIO_IN_3	-3.9	nA	-2.9	nA	-1.8	nA	-2.3	nA	-3.1	nA	-2.5	nA
IIL_Inputs_Max_	DIO_IN_4	-1.3	nA	-672.2	pA	374.2	pA	583.5	pA	583.5	pA	-2.6	nA
IIL_Inputs_Max_	DIO_IN_5	-2.9	nA	-3.1	nA	-1.8	nA	-3.1	nA	-3.1	nA	-1.8	nA
IIL_Inputs_Max_	DIO_IN_6	-3.1	nA	-5.4	nA	-2.5	nA	-2.9	nA	-3.3	nA	-1.2	nA
IIL_Inputs_Max_	DIO_IN_7	-2.1	nA	-802.2	pA	-3.7	nA	-3.7	nA	-2.9	nA	-3.1	nA
IIL_Inputs_Max_	DIO_IP_1	-3.2	nA	-2.1	nA	1.4	nA	-3.0	nA	164.9	pA	-1.7	nA
IIL_Inputs_Max_	DIO_IP_2	-3.7	nA	-1.4	nA	-3.3	nA	-2.9	nA	-4.6	nA	-174.0	pA
IIL_Inputs_Max_	DIO_IP_3	1.0	nA	1.0	nA	583.5	pA	-2.1	nA	-1.3	nA	-1.9	nA
IIL_Inputs_Max_	DIO_IP_4	-3.5	nA	-3.1	nA	-1.4	nA	-802.2	pA	-174.0	pA	-3.5	nA
IIL_Inputs_Max_	DIO_IP_5	-2.3	nA	-3.5	nA	-1.8	nA	-1.6	nA	-2.5	nA	-802.2	pA
IIL_Inputs_Max_	DIO_IP_6	-2.5	nA	-3.3	nA	-2.5	nA	-3.1	nA	-3.3	nA	-1.6	nA
IIL_Inputs_Max_	DIO_IP_7	-2.3	nA	-2.3	nA	-1.6	nA	-383.4	pA	-1.4	nA	-2.1	nA
IIL_Inputs_Max_	EN8	-2.7	nA	-1.6	nA	873.1	pA	-2.5	nA	-1.0	nA	-1.4	nA
IIL_Inputs_Max_	HCLK1P	-3.2	nA	-3.7	nA	-4.7	nA	-3.4	nA	-2.4	nA	-4.5	nA
IIL_Inputs_Max_	HCLK2P	792.8	pA	-253.6	pA	-672.2	pA	2.7	nA	-881.4	pA	-672.2	pA
IIL_Inputs_Max_	HCLK3P	3.5	nA	1.4	nA	4.3	nA	3.9	nA	2.2	nA	2.4	nA
IIL_Inputs_Max_	HCLK4P	-1.3	nA	-2.8	nA	-705.4	pA	-2.4	nA	-1.8	nA	-914.7	pA
IIL_Inputs_Max_	IO_I_1	1.4	nA	583.5	pA	1.4	nA	-2.3	nA	792.8	pA	-2.8	nA
IIL_Inputs_Max_	IO_I_2	3.5	nA	1.6	nA	2.8	nA	3.5	nA	3.7	nA	2.6	nA
IIL_Inputs_Max_	IO_I_3	1.0	nA	-462.9	pA	164.9	pA	-253.6	pA	374.2	pA	-462.9	pA
IIL_Inputs_Max_	IO_I_4	-296.9	pA	1.4	nA	3.7	nA	2.8	nA	2.8	nA	1.4	nA
IIL_Inputs_Max_	IO_I_5	1.6	nA	164.9	pA	164.9	pA	-1.7	nA	2.3	nA	-3.8	nA
IIL_Inputs_Max_	IO_I_6	-2.1	nA	-802.2	pA	-2.9	nA	-2.3	nA	-2.9	nA	-1.4	nA
IIL_Inputs_Max_	LOADIN	-4.0	nA	-6.3	nA	-4.5	nA	-7.6	nA	-6.1	nA	-6.1	nA
IIL_Inputs_Max_	RCLK1P	1.0	nA	-672.2	pA	-253.6	pA	-4.6	nA	-1.7	nA	-881.4	pA
IIL_Inputs_Max_	RCLK2P	1.4	nA	-2.0	nA	-1.1	nA	-2.8	nA	-2.0	nA	-1.8	nA
IIL_Inputs_Max_	RCLK3P	3.3	nA	2.8	nA	2.4	nA	2.2	nA	3.1	nA	3.9	nA
IIL_Inputs_Max_	RCLK4P	-1.1	nA	-3.2	nA	-1.4	nA	-2.0	nA	-2.0	nA	-3.0	nA

Table 5b

DUT		3148		3149		3176	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIL_Inputs_Max_	Bi_D_1	-87.6 pA	-296.9 pA	-506.2 pA	-506.2 pA	-924.7 pA	-1.6 nA
IIL_Inputs_Max_	Bi_D_2	2.6 nA	121.6 pA	1.8 nA	1.8 nA	958.7 pA	2.0 nA
IIL_Inputs_Max_	Bi_D_3	1.6 nA	2.2 nA	958.7 pA	958.7 pA	2.0 nA	958.7 pA
IIL_Inputs_Max_	Bi_D_4	-2.2 nA	-4.3 nA	-3.6 nA	-3.0 nA	-4.7 nA	-4.3 nA
IIL_Inputs_Max_	Bi_D_5	-2.6 nA	-2.4 nA	-496.0 pA	-3.6 nA	-77.4 pA	-2.8 nA
IIL_Inputs_Max_	Bi_D_6	-5.5 nA	-6.7 nA	-3.2 nA	-6.3 nA	-1.7 nA	-5.3 nA
IIL_Inputs_Max_	Bi_D_7	-6.4 nA	-6.4 nA	-3.2 nA	-5.5 nA	-4.9 nA	-5.3 nA
IIL_Inputs_Max_	Bi_E_1	-2.0 nA	-2.6 nA	-1.1 nA	-935.2 pA	-1.8 nA	-516.4 pA
IIL_Inputs_Max_	Bi_E_2	-2.4 nA	-2.8 nA	-2.2 nA	-2.2 nA	-725.8 pA	-3.7 nA
IIL_Inputs_Max_	Bi_E_3	-1.8 nA	-3.0 nA	-4.3 nA	-1.6 nA	-2.6 nA	-1.8 nA
IIL_Inputs_Max_	Bi_E_4	-2.0 nA	-2.6 nA	-1.8 nA	-2.0 nA	-2.6 nA	-2.6 nA
IIL_Inputs_Max_	Bi_E_5	-3.0 nA	-2.8 nA	-2.8 nA	-2.0 nA	-306.9 pA	-97.5 pA
IIL_Inputs_Max_	Bi_E_6	-1.4 nA	-1.8 nA	-2.6 nA	-935.2 pA	-2.2 nA	-3.7 nA
IIL_Inputs_Max_	Bi_E_7	-1.8 nA	-2.0 nA	-2.6 nA	-2.2 nA	-2.6 nA	-2.8 nA
IIL_Inputs_Max_	DA	-5.8 nA	-5.0 nA	-5.6 nA	-3.1 nA	-6.5 nA	-4.6 nA
IIL_Inputs_Max_	DIO_IN_1	-1.5 nA	-1.5 nA	792.8 pA	-1.1 nA	-1.9 nA	-3.6 nA
IIL_Inputs_Max_	DIO_IN_2	-3.9 nA	-2.7 nA	-4.6 nA	454.3 pA	-5.2 nA	-1.6 nA
IIL_Inputs_Max_	DIO_IN_3	-3.3 nA	-5.2 nA	-4.2 nA	-1.4 nA	-1.8 nA	-1.8 nA
IIL_Inputs_Max_	DIO_IN_4	792.8 pA	-1.5 nA	-253.6 pA	374.2 pA	-672.2 pA	-44.3 pA
IIL_Inputs_Max_	DIO_IN_5	-2.5 nA	-2.9 nA	-3.9 nA	-2.9 nA	-3.3 nA	-802.2 pA
IIL_Inputs_Max_	DIO_IN_6	-3.9 nA	-4.6 nA	-4.8 nA	-3.3 nA	-3.1 nA	-1.6 nA
IIL_Inputs_Max_	DIO_IN_7	-3.3 nA	-4.8 nA	-2.7 nA	-3.5 nA	-2.1 nA	-3.9 nA
IIL_Inputs_Max_	DIO_IP_1	-1.7 nA	164.9 pA	-462.9 pA	-1.9 nA	2.5 nA	-2.1 nA
IIL_Inputs_Max_	DIO_IP_2	-1.8 nA	-2.5 nA	-2.7 nA	-3.3 nA	-2.7 nA	-2.5 nA
IIL_Inputs_Max_	DIO_IP_3	3.9 nA	-462.9 pA	1.0 nA	-253.6 pA	1.6 nA	-1.9 nA
IIL_Inputs_Max_	DIO_IP_4	-1.8 nA	-1.8 nA	-3.3 nA	-2.3 nA	-4.4 nA	-3.1 nA
IIL_Inputs_Max_	DIO_IP_5	-592.8 pA	-3.1 nA	-3.7 nA	-2.7 nA	-3.1 nA	-2.5 nA
IIL_Inputs_Max_	DIO_IP_6	-2.5 nA	-4.2 nA	-802.2 pA	-2.7 nA	-2.9 nA	-2.7 nA
IIL_Inputs_Max_	DIO_IP_7	-2.7 nA	-1.8 nA	-1.0 nA	-2.9 nA	-1.8 nA	-1.4 nA
IIL_Inputs_Max_	EN8	-3.3 nA	-2.9 nA	-3.5 nA	-2.5 nA	-2.5 nA	-1.8 nA
IIL_Inputs_Max_	HCLK1P	-4.3 nA	-2.4 nA	-3.2 nA	-2.4 nA	-3.4 nA	-2.0 nA
IIL_Inputs_Max_	HCLK2P	-1.3 nA	-672.2 pA	583.5 pA	164.9 pA	-881.4 pA	1.4 nA
IIL_Inputs_Max_	HCLK3P	3.1 nA	1.6 nA	2.8 nA	2.6 nA	1.6 nA	3.5 nA
IIL_Inputs_Max_	HCLK4P	-1.3 nA	-2.2 nA	-914.7 pA	-4.5 nA	-705.4 pA	-2.8 nA
IIL_Inputs_Max_	IO_I_1	-1.1 nA	-1.5 nA	-253.6 pA	-2.1 nA	1.4 nA	-1.5 nA
IIL_Inputs_Max_	IO_I_2	2.2 nA	2.8 nA	3.1 nA	1.6 nA	958.7 pA	4.1 nA
IIL_Inputs_Max_	IO_I_3	1.4 nA	1.4 nA	-462.9 pA	-462.9 pA	-462.9 pA	164.9 pA
IIL_Inputs_Max_	IO_I_4	2.4 nA	2.0 nA	3.3 nA	2.0 nA	2.4 nA	2.8 nA
IIL_Inputs_Max_	IO_I_5	-44.3 pA	-672.2 pA	2.0 nA	-44.3 pA	-1.3 nA	-672.2 pA
IIL_Inputs_Max_	IO_I_6	-3.3 nA	-592.8 pA	-1.8 nA	-2.3 nA	-383.4 pA	454.3 pA
IIL_Inputs_Max_	LOADIN	-5.5 nA	-6.8 nA	-3.6 nA	-4.7 nA	-4.5 nA	-7.6 nA
IIL_Inputs_Max_	RCLK1P	1.8 nA	-1.7 nA	-1.5 nA	-462.9 pA	-2.6 nA	374.2 pA
IIL_Inputs_Max_	RCLK2P	131.9 pA	-3.2 nA	-1.5 nA	-77.4 pA	-286.7 pA	-914.7 pA
IIL_Inputs_Max_	RCLK3P	2.6 nA	1.2 nA	4.1 nA	1.4 nA	4.5 nA	2.4 nA
IIL_Inputs_Max_	RCLK4P	-725.8 pA	-2.2 nA	-2.0 nA	-935.2 pA	-3.9 nA	-2.0 nA

Table 5c

<b>DUT</b>		<b>3095</b>		<b>3124</b>		<b>3147</b>	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIL_BiOuts_Max_	Bi_IO_1	-4.0 nA	-4.6 nA	-3.6 nA	-5.7 nA	-4.9 nA	-5.3 nA
IIL_BiOuts_Max_	Bi_IO_2	-4.5 nA	-7.0 nA	-5.3 nA	-5.1 nA	-4.1 nA	-5.3 nA
IIL_BiOuts_Max_	Bi_IO_3	-2.4 nA	-2.6 nA	-2.6 nA	-2.0 nA	-2.2 nA	-914.7 pA
IIL_BiOuts_Max_	Bi_IO_4	-44.3 pA	-2.3 nA	-3.2 nA	-3.2 nA	-1.5 nA	-1.7 nA
IIL_BiOuts_Max_	Bi_IO_5	-496.0 pA	-1.1 nA	-2.8 nA	-2.2 nA	-286.7 pA	-2.2 nA
IIL_BiOuts_Max_	Bi_IO_6	-2.6 nA	-5.3 nA	-2.4 nA	-2.2 nA	-3.4 nA	-3.4 nA
IIL_BiOuts_Max_	Bi_IO_7	-3.0 nA	-3.0 nA	-1.1 nA	-1.9 nA	-3.0 nA	-4.5 nA

Table 5d

<b>DUT</b>		<b>3148</b>		<b>3149</b>		<b>3176</b>	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIL_BiOuts_Max_	Bi_IO_1	-1.5 nA	-4.2 nA	-2.6 nA	-3.2 nA	-1.3 nA	280.0 nA
IIL_BiOuts_Max_	Bi_IO_2	-4.5 nA	-4.7 nA	-4.3 nA	-6.1 nA	-2.4 nA	-366.6 nA
IIL_BiOuts_Max_	Bi_IO_3	-705.4 pA	-3.0 nA	-2.8 nA	-2.6 nA	-77.4 pA	218.4 nA
IIL_BiOuts_Max_	Bi_IO_4	-3.0 nA	-44.3 pA	-2.6 nA	-1.1 nA	-1.5 nA	-19.9 uA
IIL_BiOuts_Max_	Bi_IO_5	-914.7 pA	-1.1 nA	-1.8 nA	-4.1 nA	969.2 pA	-12.4 uA
IIL_BiOuts_Max_	Bi_IO_6	-2.6 nA	-3.4 nA	-4.7 nA	-2.4 nA	-2.8 nA	28.0 nA
IIL_BiOuts_Max_	Bi_IO_7	-3.4 nA	-5.3 nA	-4.7 nA	-3.4 nA	-1.9 nA	-3.0 nA

Table 6a

DUT		3095		3124		3147	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_Inputs_Max_	Bi_D_1	8.9	nA	9.5	nA	7.2	nA
IIH_Inputs_Max_	Bi_D_2	2.6	nA	5.8	nA	7.7	nA
IIH_Inputs_Max_	Bi_D_3	5.4	nA	6.0	nA	3.7	nA
IIH_Inputs_Max_	Bi_D_4	3.5	nA	550.5	pA	3.7	nA
IIH_Inputs_Max_	Bi_D_5	-286.7	pA	1.6	nA	2.0	nA
IIH_Inputs_Max_	Bi_D_6	4.8	nA	7.3	nA	4.8	nA
IIH_Inputs_Max_	Bi_D_7	530.9	pA	2.0	nA	3.0	nA
IIH_Inputs_Max_	Bi_E_1	949.7	pA	1.8	nA	4.9	nA
IIH_Inputs_Max_	Bi_E_2	321.4	pA	-1.6	nA	2.6	nA
IIH_Inputs_Max_	Bi_E_3	2.0	nA	112.0	pA	1.4	nA
IIH_Inputs_Max_	Bi_E_4	-1.1	nA	740.3	pA	2.2	nA
IIH_Inputs_Max_	Bi_E_5	1.4	nA	530.9	pA	2.2	nA
IIH_Inputs_Max_	Bi_E_6	949.7	pA	-516.4	pA	-935.2	pA
IIH_Inputs_Max_	Bi_E_7	321.4	pA	949.7	pA	-1.8	nA
IIH_Inputs_Max_	DA	1.5	nA	454.3	pA	2.3	nA
IIH_Inputs_Max_	DIO_IN_1	3.7	nA	4.8	nA	5.0	nA
IIH_Inputs_Max_	DIO_IN_2	-174.0	pA	873.1	pA	2.1	nA
IIH_Inputs_Max_	DIO_IN_3	1.3	nA	2.1	nA	-174.0	pA
IIH_Inputs_Max_	DIO_IN_4	5.6	nA	2.0	nA	5.0	nA
IIH_Inputs_Max_	DIO_IN_5	2.5	nA	1.1	nA	-1.4	nA
IIH_Inputs_Max_	DIO_IN_6	663.7	pA	-1.2	nA	-802.2	pA
IIH_Inputs_Max_	DIO_IN_7	1.9	nA	873.1	pA	1.5	nA
IIH_Inputs_Max_	DIO_IP_1	3.1	nA	1.6	nA	2.7	nA
IIH_Inputs_Max_	DIO_IP_2	-383.4	pA	-1.6	nA	454.3	pA
IIH_Inputs_Max_	DIO_IP_3	5.4	nA	3.7	nA	2.5	nA
IIH_Inputs_Max_	DIO_IP_4	873.1	pA	-802.2	pA	244.9	pA
IIH_Inputs_Max_	DIO_IP_5	-174.0	pA	-1.6	nA	35.5	pA
IIH_Inputs_Max_	DIO_IP_6	35.5	pA	-592.8	pA	35.5	pA
IIH_Inputs_Max_	DIO_IP_7	-2.3	nA	244.9	pA	-1.4	nA
IIH_Inputs_Max_	EN8	244.9	pA	873.1	pA	-383.4	pA
IIH_Inputs_Max_	HCLK1P	-1.6	nA	-725.8	pA	-3.2	nA
IIH_Inputs_Max_	HCLK2P	1.2	nA	583.5	pA	4.4	nA
IIH_Inputs_Max_	HCLK3P	3.3	nA	3.7	nA	4.1	nA
IIH_Inputs_Max_	HCLK4P	1.4	nA	341.2	pA	-77.4	pA
IIH_Inputs_Max_	IO_I_1	2.7	nA	2.9	nA	1.6	nA
IIH_Inputs_Max_	IO_I_2	4.7	nA	2.8	nA	3.1	nA
IIH_Inputs_Max_	IO_I_3	792.8	pA	1.4	nA	2.5	nA
IIH_Inputs_Max_	IO_I_4	4.3	nA	4.5	nA	6.0	nA
IIH_Inputs_Max_	IO_I_5	2.9	nA	1.4	nA	3.9	nA
IIH_Inputs_Max_	IO_I_6	-1.6	nA	-1.6	nA	-802.2	pA
IIH_Inputs_Max_	LOADIN	2.0	nA	2.0	nA	3.7	nA
IIH_Inputs_Max_	RCLK1P	2.7	nA	2.0	nA	2.5	nA
IIH_Inputs_Max_	RCLK2P	-1.1	nA	-77.4	pA	341.2	pA
IIH_Inputs_Max_	RCLK3P	4.7	nA	3.5	nA	7.7	nA
IIH_Inputs_Max_	RCLK4P	-3.2	nA	-2.4	nA	-1.4	nA

Table 6b

DUT		3148		3149		3176	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_Inputs_Max_	Bi_D_1	6.6	nA	7.2	nA	8.7	nA
IIH_Inputs_Max_	Bi_D_2	7.2	nA	6.6	nA	7.7	nA
IIH_Inputs_Max_	Bi_D_3	5.8	nA	6.6	nA	6.6	nA
IIH_Inputs_Max_	Bi_D_4	2.0	nA	3.3	nA	3.1	nA
IIH_Inputs_Max_	Bi_D_5	1.8	nA	969.2	pA	1.8	nA
IIH_Inputs_Max_	Bi_D_6	3.3	nA	3.7	nA	7.3	nA
IIH_Inputs_Max_	Bi_D_7	1.8	nA	2.4	nA	1.2	nA
IIH_Inputs_Max_	Bi_E_1	1.8	nA	1.4	nA	1.2	nA
IIH_Inputs_Max_	Bi_E_2	-516.4	pA	-2.6	nA	3.5	nA
IIH_Inputs_Max_	Bi_E_3	1.2	nA	2.0	nA	-1.6	nA
IIH_Inputs_Max_	Bi_E_4	3.3	nA	-2.8	nA	-306.9	pA
IIH_Inputs_Max_	Bi_E_5	-1.1	nA	-725.8	pA	1.4	nA
IIH_Inputs_Max_	Bi_E_6	321.4	pA	-306.9	pA	-1.8	nA
IIH_Inputs_Max_	Bi_E_7	1.4	nA	-935.2	pA	-725.8	pA
IIH_Inputs_Max_	DA	454.3	pA	3.2	nA	1.9	nA
IIH_Inputs_Max_	DIO_IN_1	3.1	nA	5.6	nA	1.2	nA
IIH_Inputs_Max_	DIO_IN_2	1.1	nA	3.8	nA	1.5	nA
IIH_Inputs_Max_	DIO_IN_3	2.1	nA	35.5	pA	-1.0	nA
IIH_Inputs_Max_	DIO_IN_4	3.9	nA	583.5	pA	1.4	nA
IIH_Inputs_Max_	DIO_IN_5	-1.0	nA	1.3	nA	-2.5	nA
IIH_Inputs_Max_	DIO_IN_6	35.5	pA	-1.2	nA	-1.6	nA
IIH_Inputs_Max_	DIO_IN_7	2.1	nA	873.1	pA	1.3	nA
IIH_Inputs_Max_	DIO_IP_1	2.7	nA	2.0	nA	3.5	nA
IIH_Inputs_Max_	DIO_IP_2	663.7	pA	-2.3	nA	-174.0	pA
IIH_Inputs_Max_	DIO_IP_3	4.4	nA	1.4	nA	2.7	nA
IIH_Inputs_Max_	DIO_IP_4	663.7	pA	-592.8	pA	-802.2	pA
IIH_Inputs_Max_	DIO_IP_5	663.7	pA	-802.2	pA	-1.6	nA
IIH_Inputs_Max_	DIO_IP_6	35.5	pA	-802.2	pA	-1.0	nA
IIH_Inputs_Max_	DIO_IP_7	244.9	pA	1.5	nA	454.3	pA
IIH_Inputs_Max_	EN8	1.9	nA	-592.8	pA	663.7	pA
IIH_Inputs_Max_	HCLK1P	-306.9	pA	-1.8	nA	-2.2	nA
IIH_Inputs_Max_	HCLK2P	2.9	nA	1.0	nA	2.5	nA
IIH_Inputs_Max_	HCLK3P	3.3	nA	5.8	nA	5.1	nA
IIH_Inputs_Max_	HCLK4P	1.8	nA	-2.6	nA	131.9	pA
IIH_Inputs_Max_	IO_I_1	2.9	nA	1.2	nA	1.4	nA
IIH_Inputs_Max_	IO_I_2	4.7	nA	3.5	nA	3.9	nA
IIH_Inputs_Max_	IO_I_3	1.0	nA	3.9	nA	583.5	pA
IIH_Inputs_Max_	IO_I_4	4.5	nA	4.7	nA	4.9	nA
IIH_Inputs_Max_	IO_I_5	3.5	nA	1.8	nA	3.7	nA
IIH_Inputs_Max_	IO_I_6	873.1	pA	-383.4	pA	-802.2	pA
IIH_Inputs_Max_	LOADIN	3.3	nA	3.5	nA	2.7	nA
IIH_Inputs_Max_	RCLK1P	1.8	nA	583.5	pA	374.2	pA
IIH_Inputs_Max_	RCLK2P	-286.7	pA	-496.0	pA	-914.7	pA
IIH_Inputs_Max_	RCLK3P	4.5	nA	3.7	nA	2.8	nA
IIH_Inputs_Max_	RCLK4P	-97.5	pA	-1.8	nA	1.8	nA
				-2.2	nA	112.0	pA
						1.6	nA

Table 6c

DUT		3095		3124		3147	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_BiOuts_Max	Bi_IO_1	-253.6 pA	1.2 nA	1.6 nA	1.6 nA	3.1 nA	374.2 pA
IIH_BiOuts_Max	Bi_IO_2	-3.2 nA	-2.0 nA	131.9 pA	550.5 pA	-1.5 nA	-2.0 nA
IIH_BiOuts_Max	Bi_IO_3	1.2 nA	-1.1 nA	1.6 nA	-2.6 nA	-496.0 pA	-2.6 nA
IIH_BiOuts_Max	Bi_IO_4	792.8 pA	1.0 nA	2.9 nA	-881.4 pA	-253.6 pA	-1.3 nA
IIH_BiOuts_Max	Bi_IO_5	-496.0 pA	20.6 uA	550.5 pA	20.6 uA	-1.8 nA	1.2 nA
IIH_BiOuts_Max	Bi_IO_6	-56.5 pA	1.7 uA	-1.3 nA	3.4 uA	-894.9 pA	-3.6 nA
IIH_BiOuts_Max	Bi_IO_7	-894.9 pA	-1.5 nA	-4.0 nA	-2.4 nA	-266.1 pA	-1.1 nA

Table 6d

DUT		3148		3149		3176	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_BiOuts_Max	Bi_IO_1	2.0 nA	-881.4 pA	2.0 nA	1.8 nA	-44.3 pA	164.9 pA
IIH_BiOuts_Max	Bi_IO_2	-1.3 nA	-914.7 pA	759.8 pA	-705.4 pA	-914.7 pA	-286.7 pA
IIH_BiOuts_Max	Bi_IO_3	1.6 nA	-1.5 nA	550.5 pA	-496.0 pA	341.2 pA	-1.8 nA
IIH_BiOuts_Max	Bi_IO_4	2.0 nA	792.8 pA	1.6 nA	583.5 pA	1.4 nA	1.4 nA
IIH_BiOuts_Max	Bi_IO_5	969.2 pA	-77.4 pA	-1.8 nA	20.6 uA	2.2 nA	20.6 uA
IIH_BiOuts_Max	Bi_IO_6	-266.1 pA	-894.9 pA	-1.5 nA	8.2 uA	-475.7 pA	1.9 uA
IIH_BiOuts_Max	Bi_IO_7	-266.1 pA	-1.9 nA	-1.7 nA	-2.4 nA	-1.3 nA	153.0 pA

#### D. Differential Input (LVPECL) Threshold Voltage ( $V_{IL}/V_{IH}$ )

Table 7 and 8 show the pre-irradiation and post-annealing threshold-voltages of the LVPECL input. Every data passes the spec.

Table 7a

DUT		3095		3124		3147	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DIO_IP_7	95	65	115	90	110	80
bi_levels_vil	DIO_IP_6	100	75	100	70	115	90
bi_levels_vil	DIO_IP_5	115	90	100	70	100	75
bi_levels_vil	DIO_IP_4	80	60	80	55	95	75
bi_levels_vil	DIO_IP_3	75	55	80	50	75	55
bi_levels_vil	DIO_IP_2	80	55	80	50	75	50
bi_levels_vil	DIO_IP_1	65	45	55	30	70	50

Table7b

<b>DUT</b>		<b>3148</b>		<b>3149</b>		<b>3176</b>	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DIO_IP_7	115	100	100	90	105	90
bi_levels_vil	DIO_IP_6	110	95	110	100	95	85
bi_levels_vil	DIO_IP_5	110	95	110	95	115	100
bi_levels_vil	DIO_IP_4	85	70	95	85	90	80
bi_levels_vil	DIO_IP_3	70	60	75	65	65	55
bi_levels_vil	DIO_IP_2	80	70	90	80	80	70
bi_levels_vil	DIO_IP_1	70	55	70	60	60	50

Table 8a

<b>DUT</b>		<b>3095</b>		<b>3124</b>		<b>3147</b>	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DIO_IP_7	95	65	115	85	105	80
bi_levels_vih	DIO_IP_6	100	70	95	70	110	85
bi_levels_vih	DIO_IP_5	115	90	95	70	100	70
bi_levels_vih	DIO_IP_4	80	55	75	50	90	70
bi_levels_vih	DIO_IP_3	75	50	75	50	70	50
bi_levels_vih	DIO_IP_2	80	55	75	45	70	45
bi_levels_vih	DIO_IP_1	70	50	55	0	75	55

Table 8b

<b>DUT</b>		<b>3148</b>		<b>3149</b>		<b>3176</b>	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DIO_IP_7	115	95	100	90	100	85
bi_levels_vih	DIO_IP_6	105	95	110	100	95	80
bi_levels_vih	DIO_IP_5	110	95	105	95	110	100
bi_levels_vih	DIO_IP_4	85	70	95	80	90	75
bi_levels_vih	DIO_IP_3	70	60	75	65	65	55
bi_levels_vih	DIO_IP_2	80	65	85	75	75	65
bi_levels_vih	DIO_IP_1	70	55	70	60	65	50

### E. Output-Drive Voltage ( $V_{OL}/V_{OH}$ )

The pre-irradiation and post-annealing  $V_{OL}/V_{OH}$  are listed in Tables 9 and 10. Every post-annealing data passes the spec.

Table 9a

DUT		3095		3124		3147	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vol	Bi_IO_7	35	35	35	35	35	35
bi_levels_vol	Bi_IO_6	30	30	35	35	35	30
bi_levels_vol	Bi_IO_5	35	35	35	35	35	35
bi_levels_vol	Bi_IO_4	35	35	35	35	35	35
bi_levels_vol	Bi_IO_3	35	35	35	35	35	35
bi_levels_vol	Bi_IO_2	30	30	30	35	35	35
bi_levels_vol	Bi_IO_1	35	35	35	35	35	35
bi_levels_vol	Bi_Y_7	25	25	25	25	25	25
bi_levels_vol	Bi_Y_6	25	25	25	25	25	25
bi_levels_vol	Bi_Y_5	25	25	25	25	25	25
bi_levels_vol	Bi_Y_4	25	25	25	25	25	25
bi_levels_vol	Bi_Y_3	30	25	30	30	30	30
bi_levels_vol	Bi_Y_2	25	25	25	25	25	25
bi_levels_vol	Bi_Y_1	25	25	25	25	30	25
bi_levels_vol	CLOCKE_OUT	20	20	20	20	20	20
bi_levels_vol	CLOCKF_OUT	25	25	20	25	25	25
bi_levels_vol	QA_2	20	20	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20	20	20
bi_levels_vol	QA_0	20	20	20	20	20	20

Table 9b

DUT		3148		3149		3176	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vol	Bi_IO_7	35	35	35	35	35	35
bi_levels_vol	Bi_IO_6	30	30	35	30	30	30
bi_levels_vol	Bi_IO_5	35	35	35	35	35	35
bi_levels_vol	Bi_IO_4	35	35	35	35	35	35
bi_levels_vol	Bi_IO_3	35	35	35	35	35	35
bi_levels_vol	Bi_IO_2	30	30	30	35	30	30
bi_levels_vol	Bi_IO_1	35	35	35	35	35	35
bi_levels_vol	Bi_Y_7	25	25	25	25	25	25
bi_levels_vol	Bi_Y_6	25	25	25	25	25	25
bi_levels_vol	Bi_Y_5	25	25	25	25	25	25
bi_levels_vol	Bi_Y_4	25	25	25	25	25	25
bi_levels_vol	Bi_Y_3	30	25	25	25	25	25
bi_levels_vol	Bi_Y_2	25	25	25	25	25	25
bi_levels_vol	Bi_Y_1	25	25	30	25	30	25
bi_levels_vol	CLOCKE_OUT	20	20	20	20	20	20
bi_levels_vol	CLOCKF_OUT	25	25	20	25	25	20
bi_levels_vol	QA_2	20	20	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20	20	20
bi_levels_vol	QA_0	20	20	20	20	20	20

Table 10a

DUT		3095		3124		3147	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_voh	Bi_IO_7	2.97	2.97	2.97	2.97	2.97	2.97
bi_levels_voh	Bi_IO_6	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_5	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_4	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_3	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_2	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_1	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_Y_7	2.98	2.98	2.98	2.98	2.985	2.98
bi_levels_voh	Bi_Y_6	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_5	2.985	2.98	2.98	2.98	2.985	2.98
bi_levels_voh	Bi_Y_4	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_3	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_2	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_1	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	CLOCKE_OUT	2.975	2.97	2.97	2.965	2.975	2.97
bi_levels_voh	CLOCKF_OUT	2.975	2.97	2.975	2.97	2.975	2.97
bi_levels_voh	QA_2	2.97	2.965	2.97	2.965	2.97	2.965
bi_levels_voh	QA_1	2.97	2.965	2.97	2.965	2.97	2.965
bi_levels_voh	QA_0	2.975	2.97	2.97	2.97	2.97	2.97

Table 10b

DUT		3148		3149		3176	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_voh	Bi_IO_7	2.97	2.97	2.97	2.97	2.97	2.97
bi_levels_voh	Bi_IO_6	2.965	2.965	2.965	2.965	2.965	2.97
bi_levels_voh	Bi_IO_5	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_4	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_3	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_2	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_1	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_Y_7	2.985	2.98	2.98	2.98	2.985	2.98
bi_levels_voh	Bi_Y_6	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_5	2.985	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_4	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_3	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_2	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_1	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	CLOCKE_OUT	2.97	2.97	2.975	2.97	2.975	2.97
bi_levels_voh	CLOCKF_OUT	2.975	2.97	2.975	2.97	2.975	2.97
bi_levels_voh	QA_2	2.97	2.97	2.97	2.965	2.97	2.97
bi_levels_voh	QA_1	2.97	2.97	2.97	2.97	2.97	2.97
bi_levels_voh	QA_0	2.97	2.97	2.97	2.97	2.97	2.97

### *F. Propagation Delay*

Table 11 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case the percentage change is well below  $\pm 10\%$ .

Table 11 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose krad(SiO <sub>2</sub> )	Pre-Irradiation ( $\mu$ s)	Post-Annealing ( $\mu$ s)	Degradation
3095	300	6.794	6.757	-0.54%
3124	300	7.135	7.266	1.84%
3147	300	6.784	6.775	-0.13%
3148	200	6.837	6.743	-1.37%
3149	200	7.340	7.273	-0.92%
3176	200	6.806	6.719	-1.29%

### G. Transition Characteristic

Figures 9 to 20 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

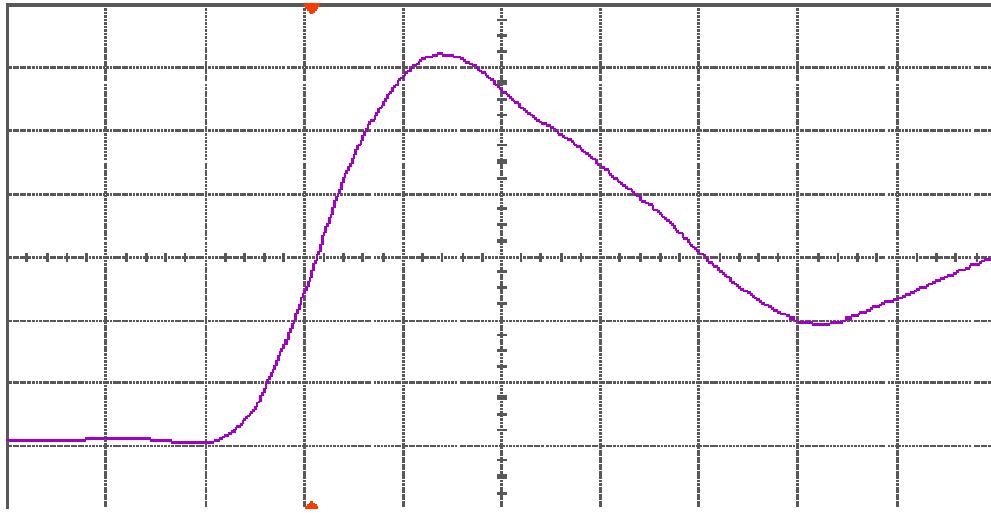


Figure 9(a) DUT 3095 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

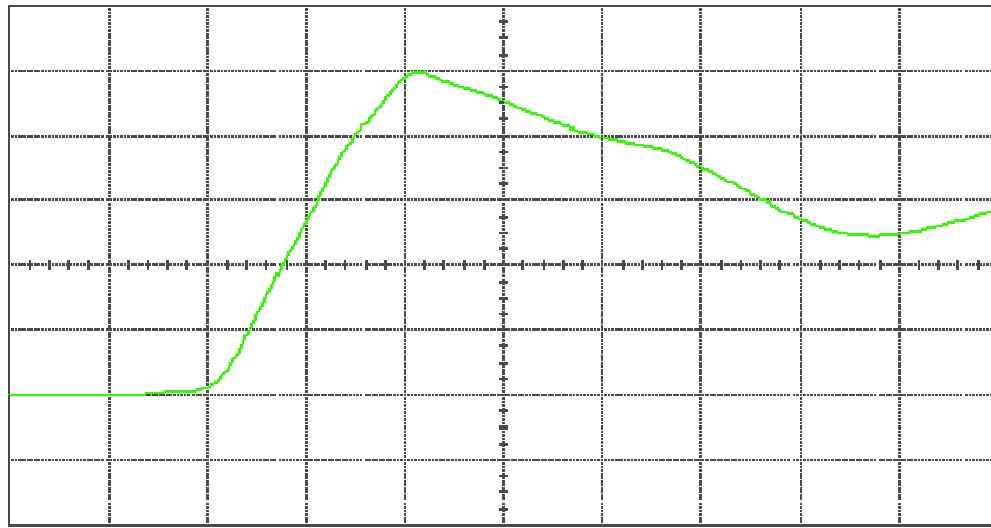


Figure 9(b) DUT 3095 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

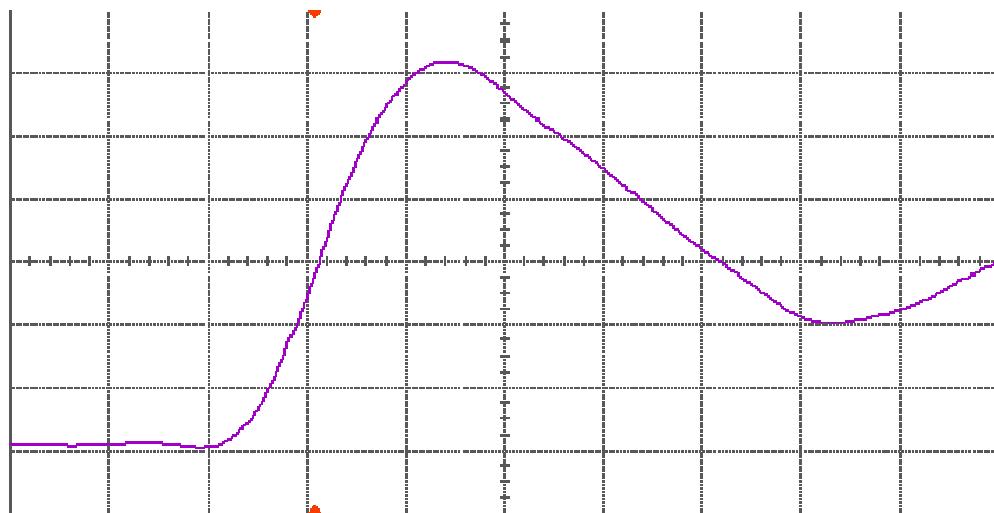


Figure 10(a) DUT 3124 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

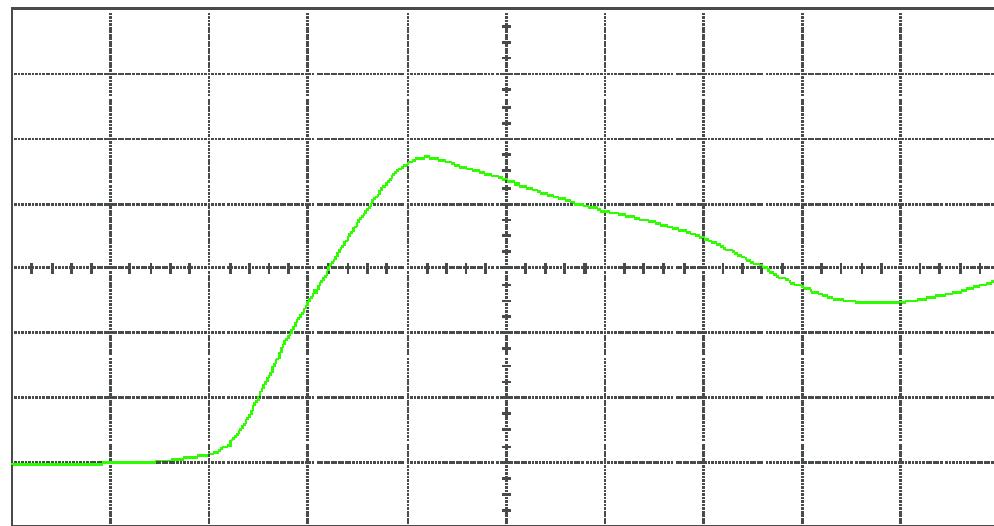


Figure 10(b) DUT 3124 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

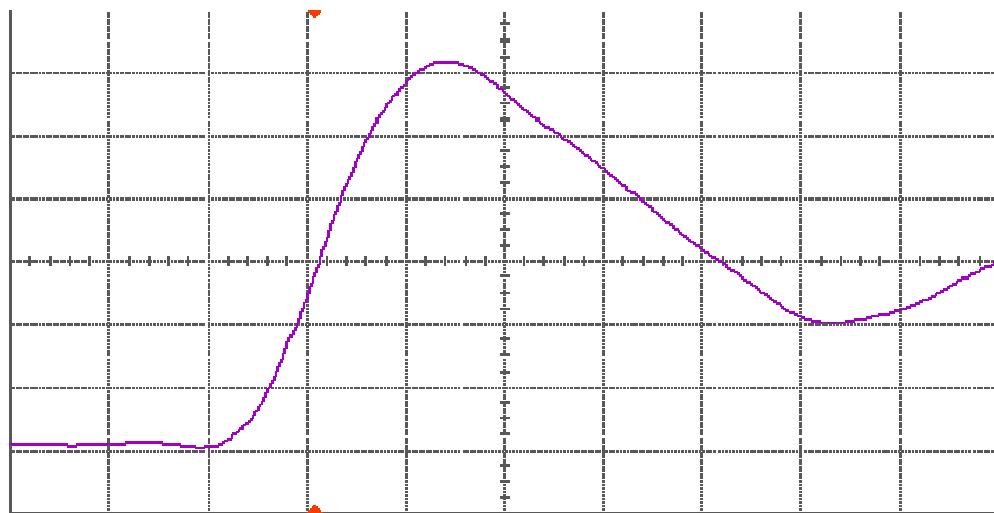


Figure 11(a) DUT 3147 pre-radiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

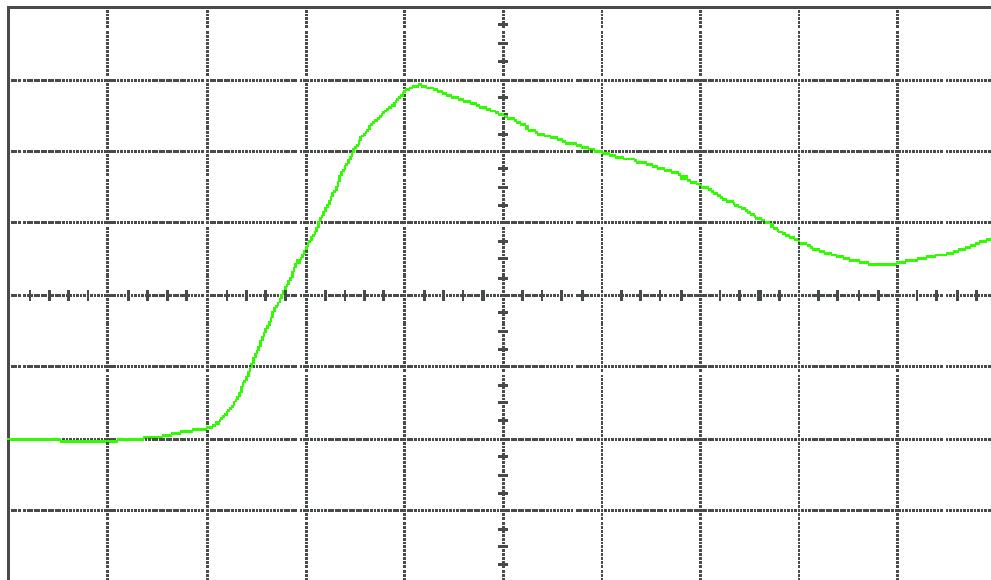


Figure 11(b) DUT 3147 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

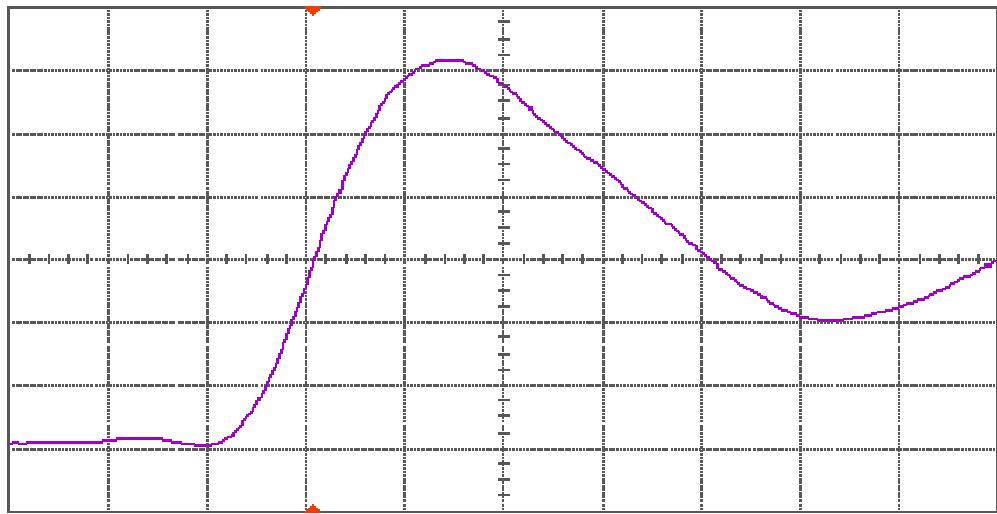


Figure 12(a) DUT 3148 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

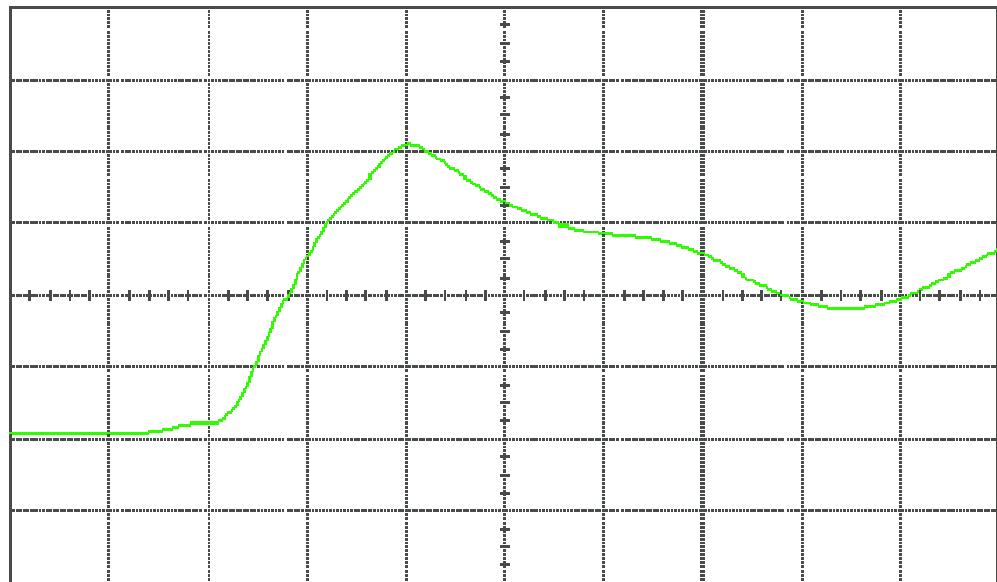


Figure 12(b) DUT 3148 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

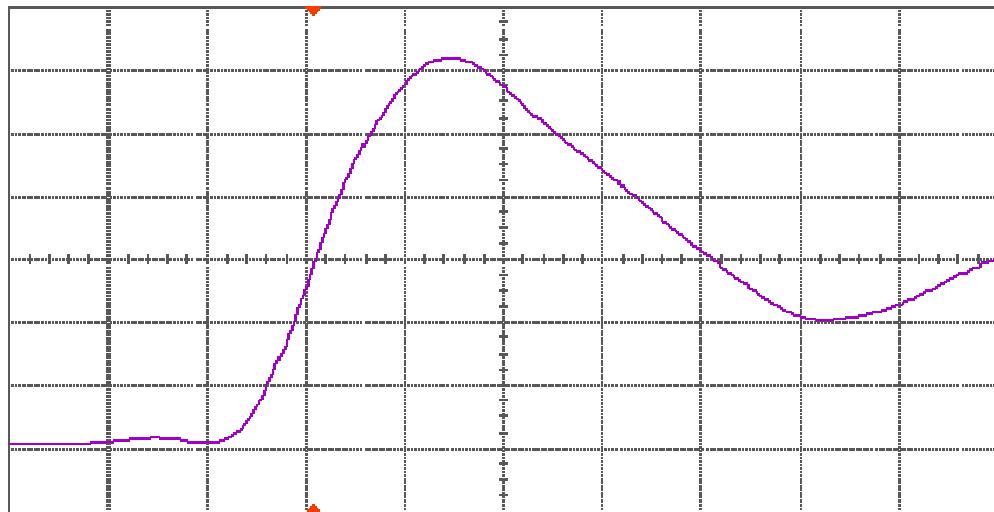


Figure 13(a) DUT 3149 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

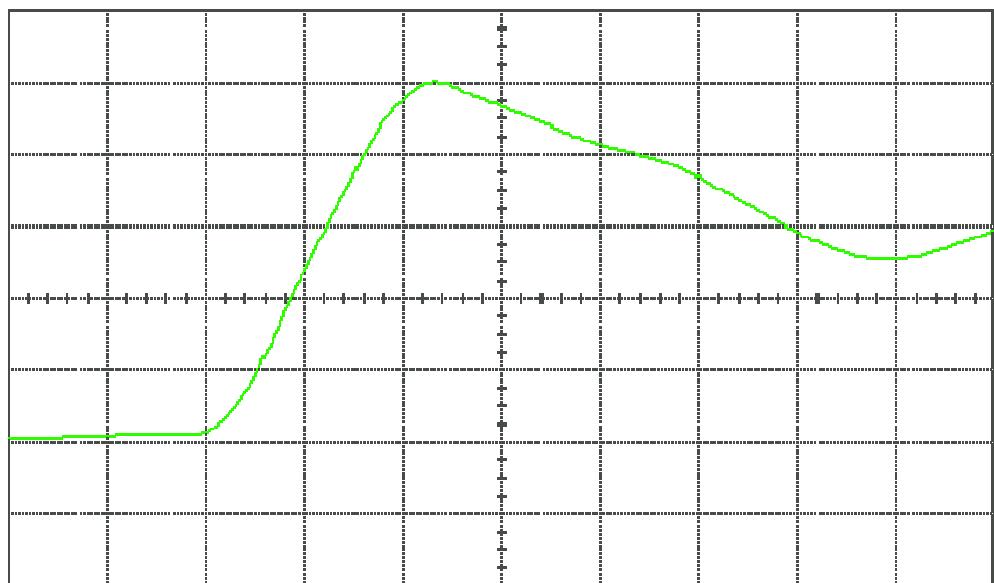


Figure 13(b) DUT 3149 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

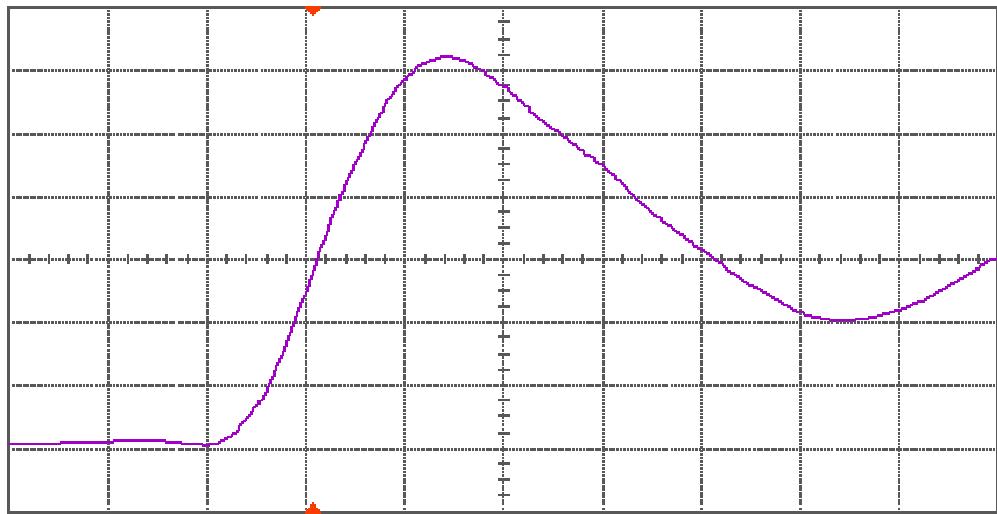


Figure 14(a) DUT 3176 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

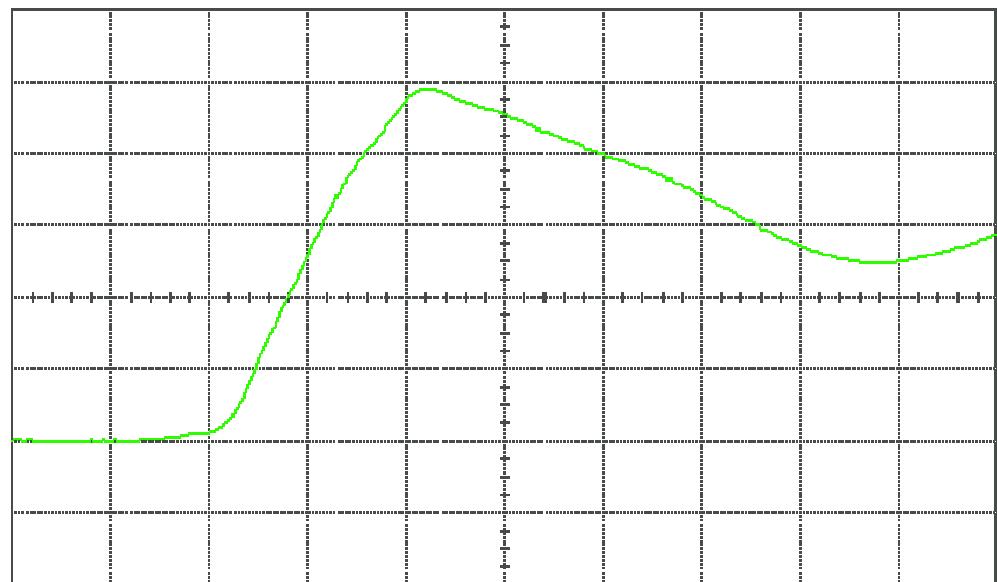


Figure 14(b) DUT 3176 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

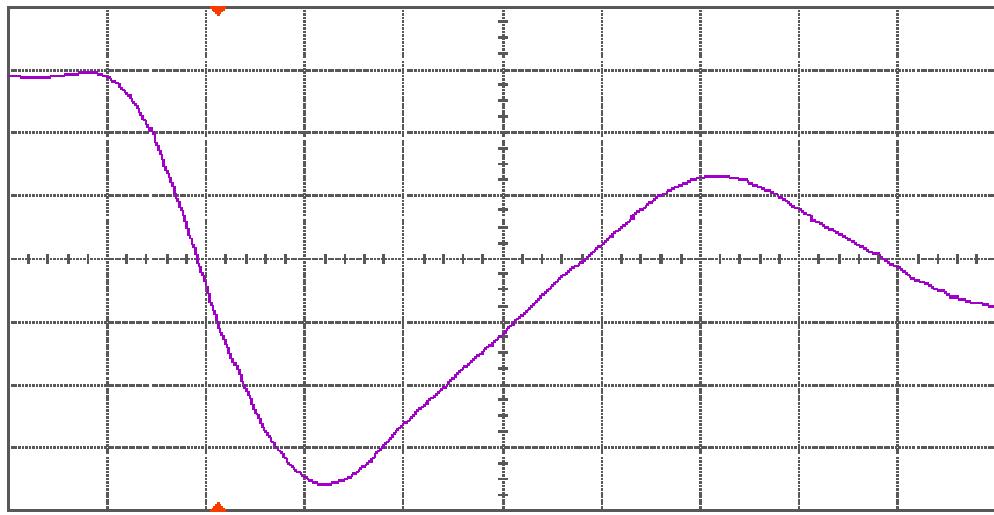


Figure 15(a) DUT 3095 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

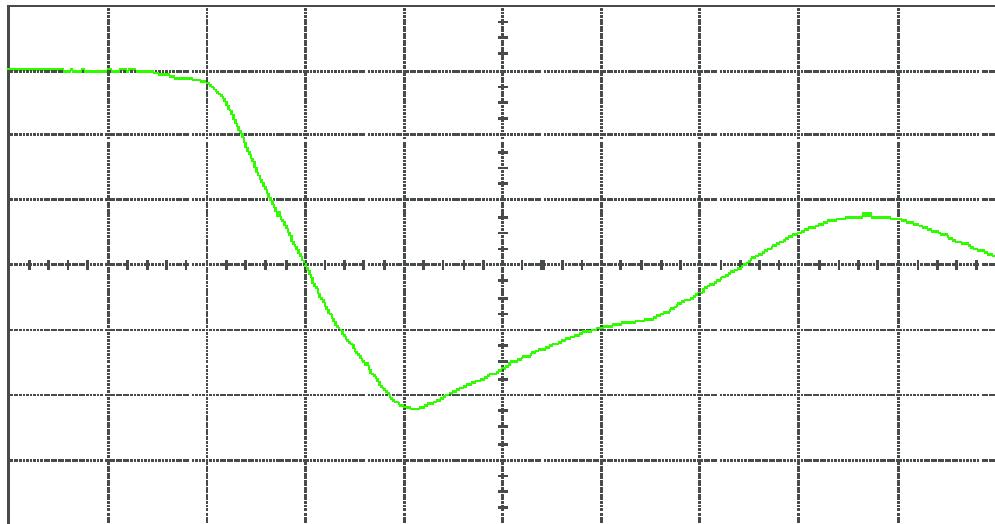


Figure 15(b) DUT 3095 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

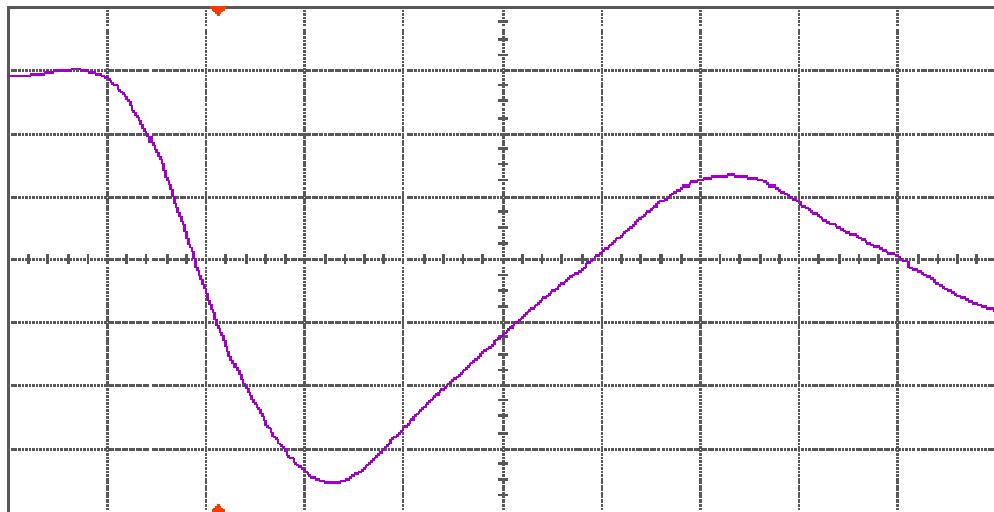


Figure 16(a) DUT 3124 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

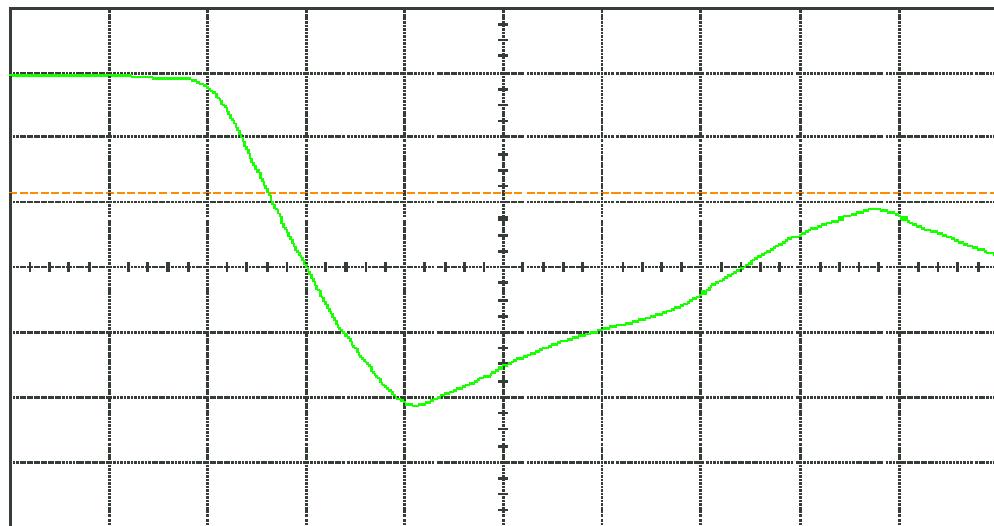


Figure 16(b) DUT 3124 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

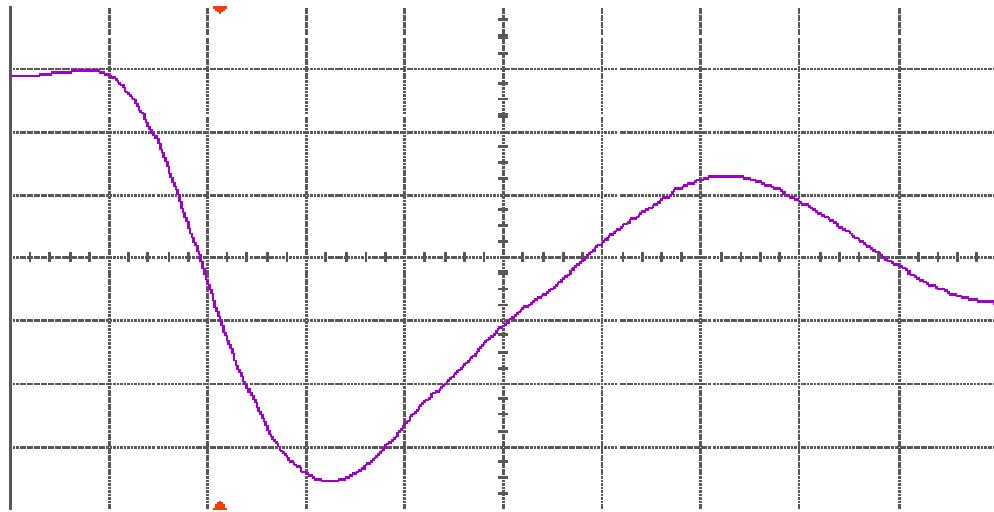


Figure 17(a) DUT 3147 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

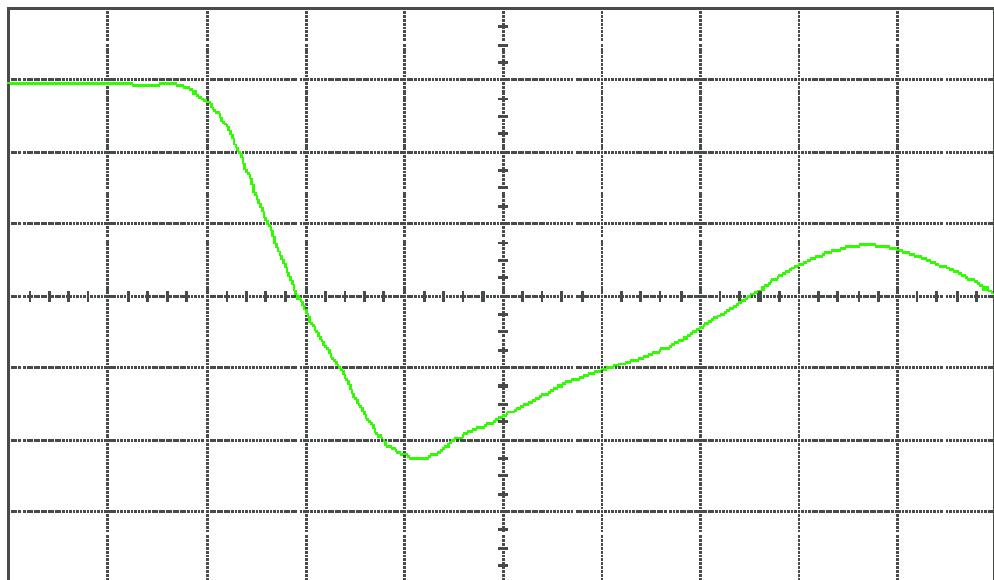


Figure 17(b) DUT 3147 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

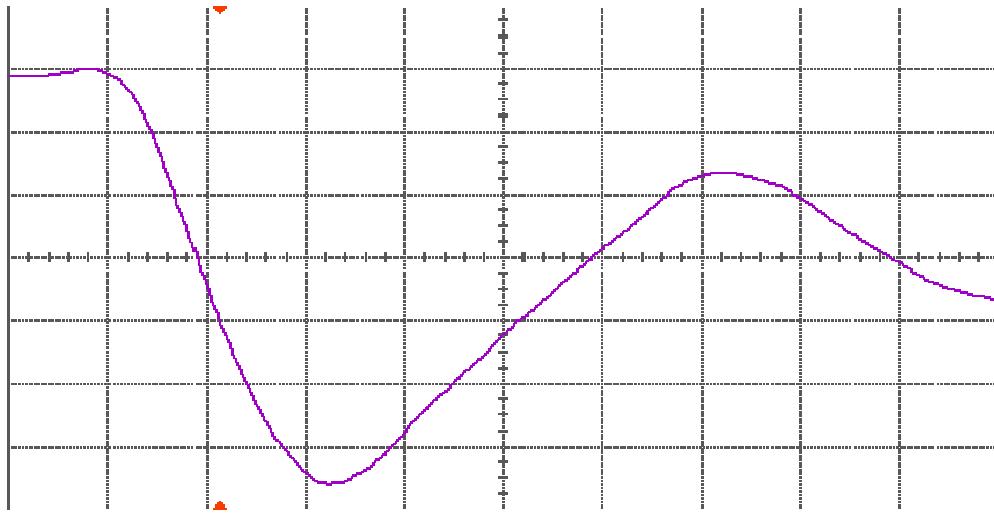


Figure 18(a) DUT 3148 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

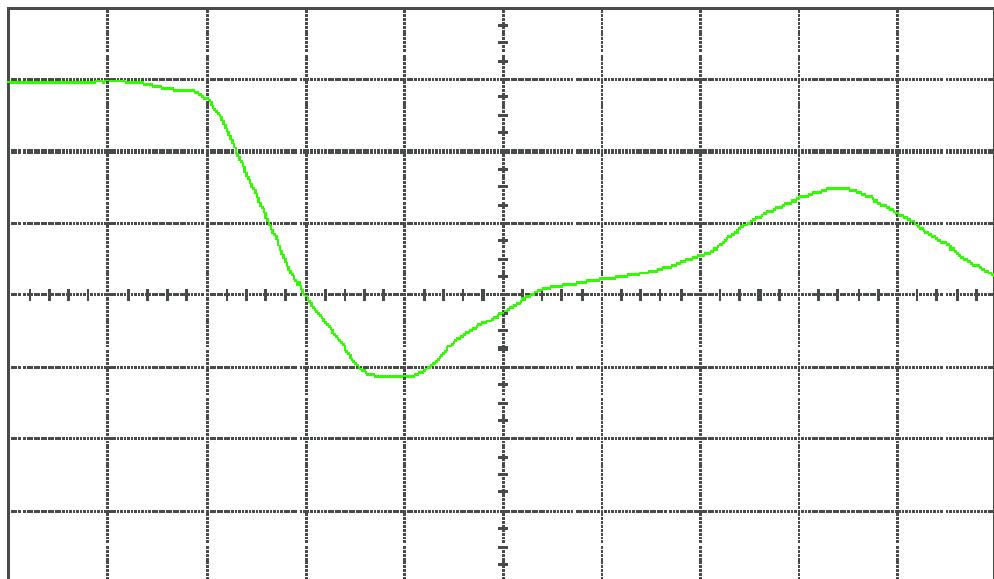


Figure 18(b) DUT 3148 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

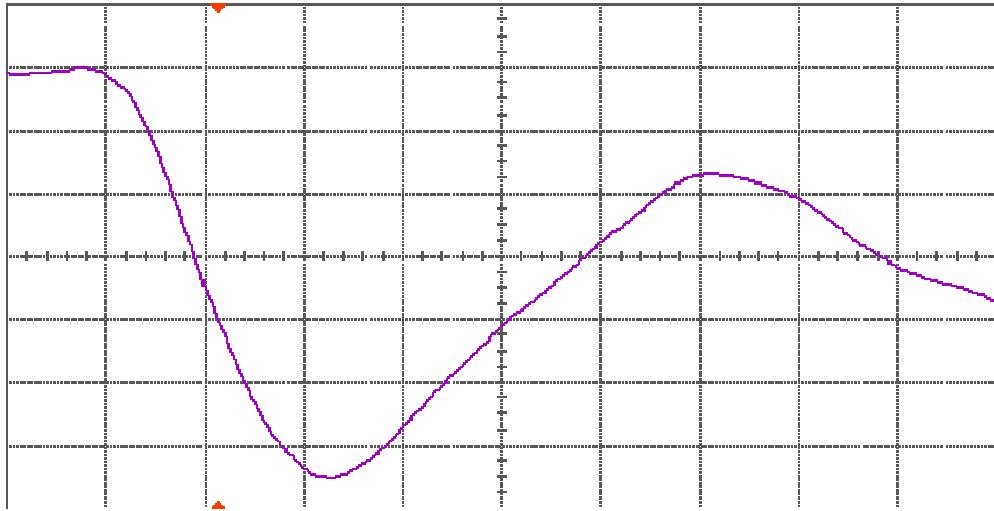


Figure 19(a) DUT 3149 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

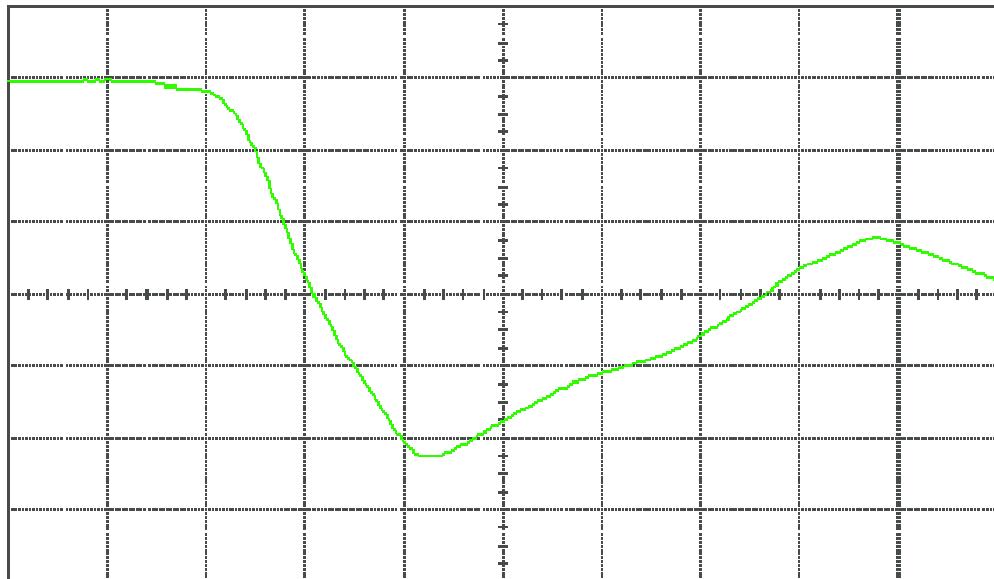


Figure 19(b) DUT 3149 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

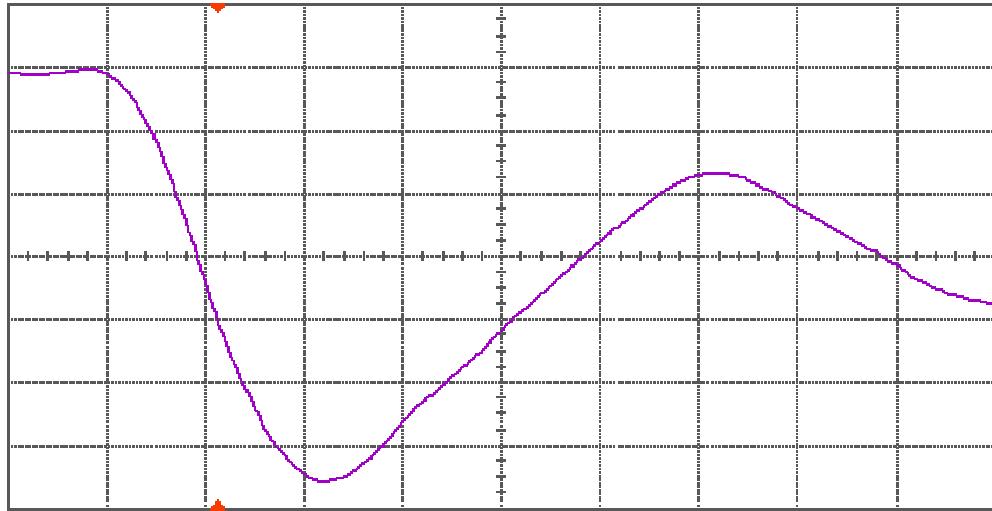


Figure 20(a) DUT 3176 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

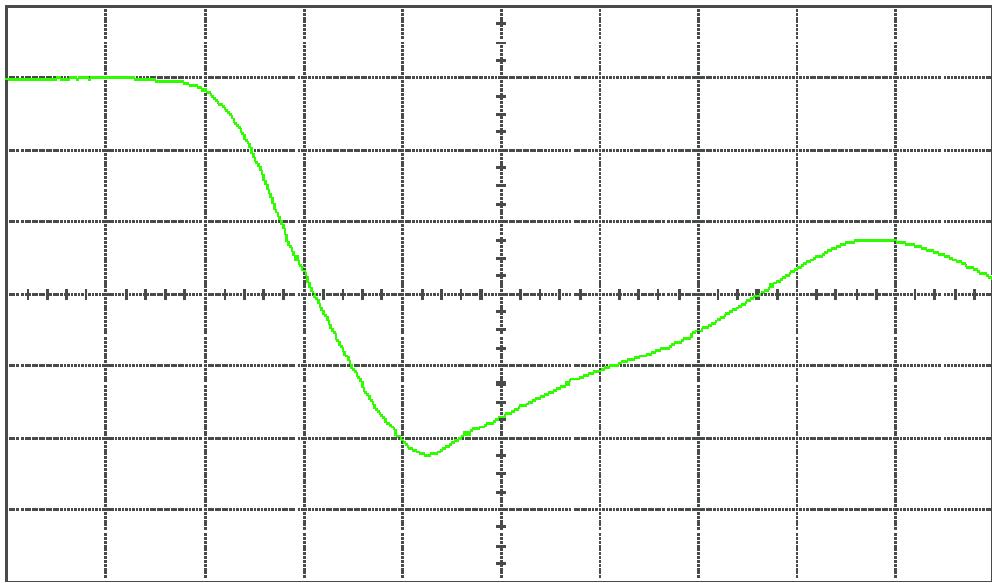


Figure 20(b) DUT 3176 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.