

TOTAL IONIZING DOSE TEST REPORT

No. 07T-RTAX2000S-D2S8M1

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I. SUMMARY TABLE

Parameter	Tolerance
1. Functionality	Passed 300 krad(SiO ₂)
2. Standby Power Supply Current (I _{CCA} /I _{CCI})	Passed 200 krad(SiO ₂)
3. Input Threshold (V _{TIL} /V _{IH})	Passed 300 krad(SiO ₂)
4. Output Threshold (V _{OL} /V _{OH})	Passed 300 krad(SiO ₂)
5. Propagation Delay	Passed 300 krad(SiO ₂) for ±10% degradation criterion
6. Transition Characteristic	Passed 300 krad(SiO ₂)

II. TOTAL IONIZING DOSE (TID) TESTING

The design of the following testing is based on an extensive, published database accumulated from the TID testing of many generations of antifuse-based FPGAs; the link of the database is in below.

<http://www.actel.com/products/milaero/hireldata.aspx#tid>

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. Each input is grounded during irradiation and annealing.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000S
Package	CG624
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	rtax2000(CG624)_Top
Die Lot Number	D2S8M1
Quantity Tested	6
Serial Number	300 krad(SiO ₂): 4140, 4142, 4151 200 krad(SiO ₂): 4095, 4096, 4152
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	5 krad(SiO ₂)/min
Irradiation Temperature	Room
Irradiation and Annealing Bias V _{CCI} /V _{CCA}	Static at 3.3 V/1.5 V
IO Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

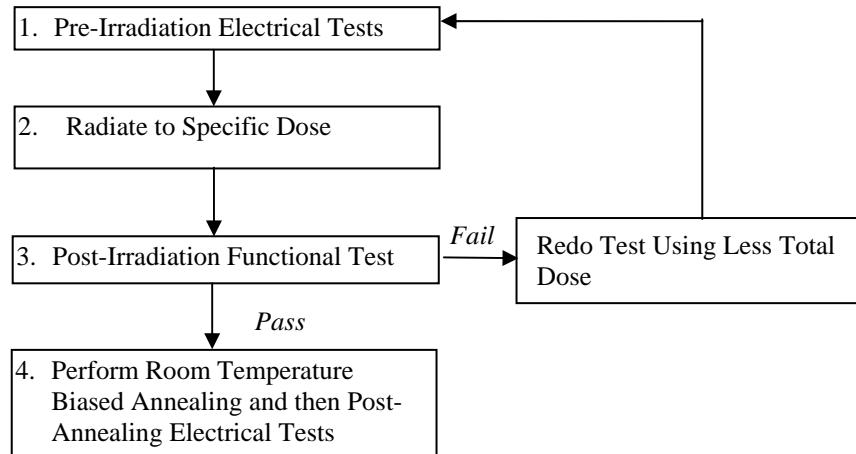


Figure 1 Parametric test flow chart

The test method basically is in compliance with the military standard TM1019.6. Figure 1s is the flow chart of the testing sequence. The accelerated annealing test in section 3.12 is not performed lot-to-lot. This is because for a deep-submicron CMOS technology used by the RTAXS product, the adverse effects due to interface state at the gate SiO₂/Si interface are negligible. The function of commercial non-irradiated transistors would be unreliable if the degradation of interface plays an important role. In other words, the SiO₂/Si interface in deep submicron CMOS transistors has to be radiation hard for even commercial applications. Thus the dominant annealing effect in RTAXS device is the reduction of trapped holes in the SiO₂; this basically alleviates the radiation effects on the DUT. Separate report on the accelerated annealing test will be provided to justify the omission of it in the lot testing; the justification testing will follow section 3.12.1.b.5.

Section 3.11 extended room temperature anneal test is also applied; room temperature annealing for 5 days was done on each device before the final parameter measurements.

C. Logic Design and Electrical Parameter Measurements

The DUT uses a high utilization generic design, rtax2000_CG624_Top, for testing total dose effects. These logic designs are described in the following subsections. Figure 2 shows the block diagram and the Verilog file (rtax2000_CG624_Top.v) is in the link:

<http://www.actel.com/products/milaero/hireldata.aspx#tid>

Generally, the functional test is performed on every design; most inputs are tested for threshold voltage and leakage current, including global clocks; the standby I_{CC} includes I_{CCI} and I_{CCA}. Except propagation delay and the transition characteristic, which is measured on the output O_BS, all other parameter measurements are done on a tester. Also note that, due to logistics limitation, the post-irradiation but pre-room-temperature-annealing functional test is performed on bench; the tested designs are shift registers and long buffer string, which are design 5 and 6 described in the following.

1. Embedded SRAM

This design is to test the function of the embedded SRAM. It uses all the RAM blocks available in the DUT. This design enables an automatic testing sequence that every bit is written and then read. Any error will be reported as a signal in the output.

2. Unidirectional LVTTL Input and Output

This is for testing radiation effects on unidirectional input and output threshold, leakage, and buffer fan-out. There are 3 sub-designs: a) a logic-core buffer with 8 fan-outs; b) a logic-core buffer with 3 fan-outs; c) 6 channels of input buffer directly connected to output buffer without core logic. LVTTL is used because it is the worst case among all the single-ended standards.

3. Bidirectional LVTTL IO

This design is for testing the radiation effects on the input/output characteristic of the bidirectional IO. There are 7 channels of bidirectional IO for radiation effects testing.

4. LVPECL Input

This design is for testing the radiation effects on the LVPECL differential inputs. 3.3V-LVPECL is considered the worst case differential input standard in the DUT. There are 7 channels.

5. Shift Registers

This design is to test the radiation effects on the function of flip-flops, which are configured R-Cells. There are 4 shift registers and each using a different global clock; one has 3,584 bits and the other three each has 2,048 bits.

6. Long Buffer String

This design is to measure the radiation effects on the propagation delay. The input of the design using a clock feeding a toggle flip-flop to generate a checkerboard signal; this signal is then fed into a buffer string with 10,000 stages. The time delay between the input clock edge at CLOCK_IN and the output switching due to this clock edge at O_BS is defined as propagation delay high to low (T_{pdhl}) or low to high (T_{pdlh}); the percentage change of the average of T_{pdhl} and T_{pdlh} is used to determine the radiation effects. A more than 10% of propagation change is considered as failure.

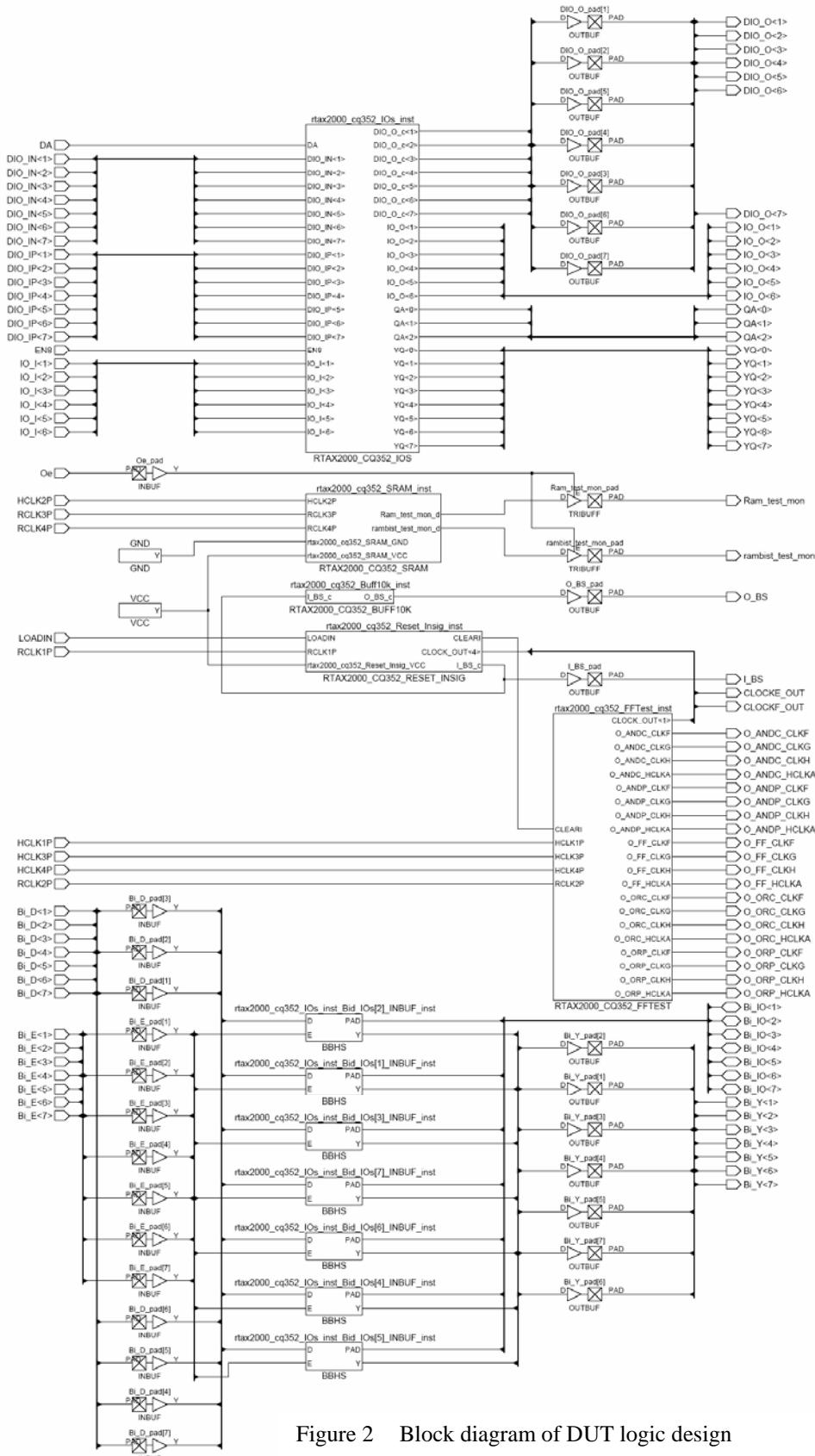


Figure 2 Block diagram of DUT logic design

III. TEST RESULTS

A. Functional Test

Every DUT passed the pre-irradiation and post-annealing functional tests on the tester; it also passed post-irradiation test on-bench.

B. Standby Power Supply Current (I_{CCA} and I_{CCI})

Figure 3-8 show the in-flux standby I_{CCA} and I_{CCI} versus total dose of every DUT.

In compliance with TM1019.6 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing I_{CC} in this test is defined as the addition of highest I_{CCI} , I_{CCDA} and $I_{CCDIFFA}$ values in Table 2-4 of the RTAXS spec sheet:

http://www.actel.com/documents/RTAXS_DS.pdf

Thus for I_{CCA} , the PIPL is 500 mA; the PIPL of I_{CCI} equals to $35+10+3.13\times7 = 66.91$ (mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT.

Table 2 summarizes the pre-irradiation, post-irradiation and post-annealing I_{CC} data: the post-annealing I_{CCA} of every DUT pass the PIPL easily; the post-annealing I_{CCI} of DUTs irradiated to 200 krad(SiO_2) all pass the PIPL, while the I_{CCI} of DUTs irradiated to 300 krad(SiO_2) all exceed the PIPL.

Table 2 Pre-irradiation, Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose krad (SiO_2)	I_{CCA} (mA)			I_{CCI} (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
4140	300	1.7	32	1.4	25.5	259	138
4142	300	2.3	26.7	1.7	26	267	124
4151	300	1.5	15.8	1.2	24.8	250	116
4095	200	3.7	2.8	3.3	25.7	112	46.5
4096	200	4.6	4.9	4.8	26	110	44.9
4152	200	3.0	3.5	2.5	26.5	100	42.5

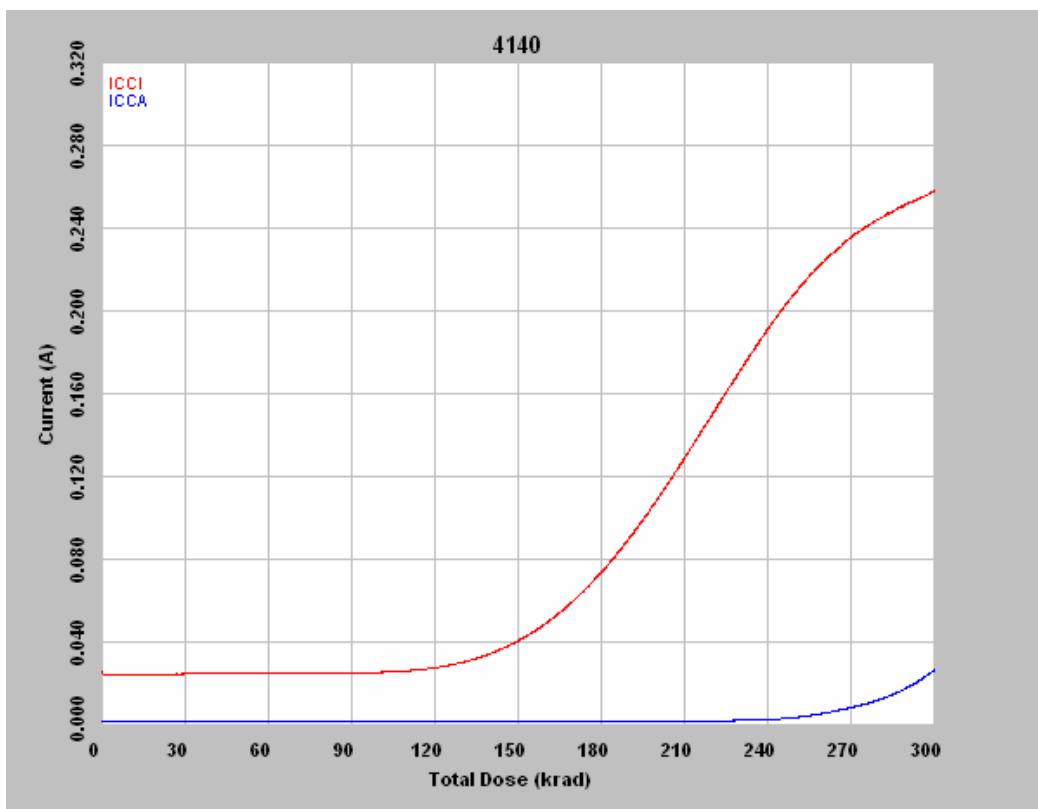


Figure 3 DUT 4140 in-flux I_{CCA} and I_{CCI} . The spikes are due to bad contacts.

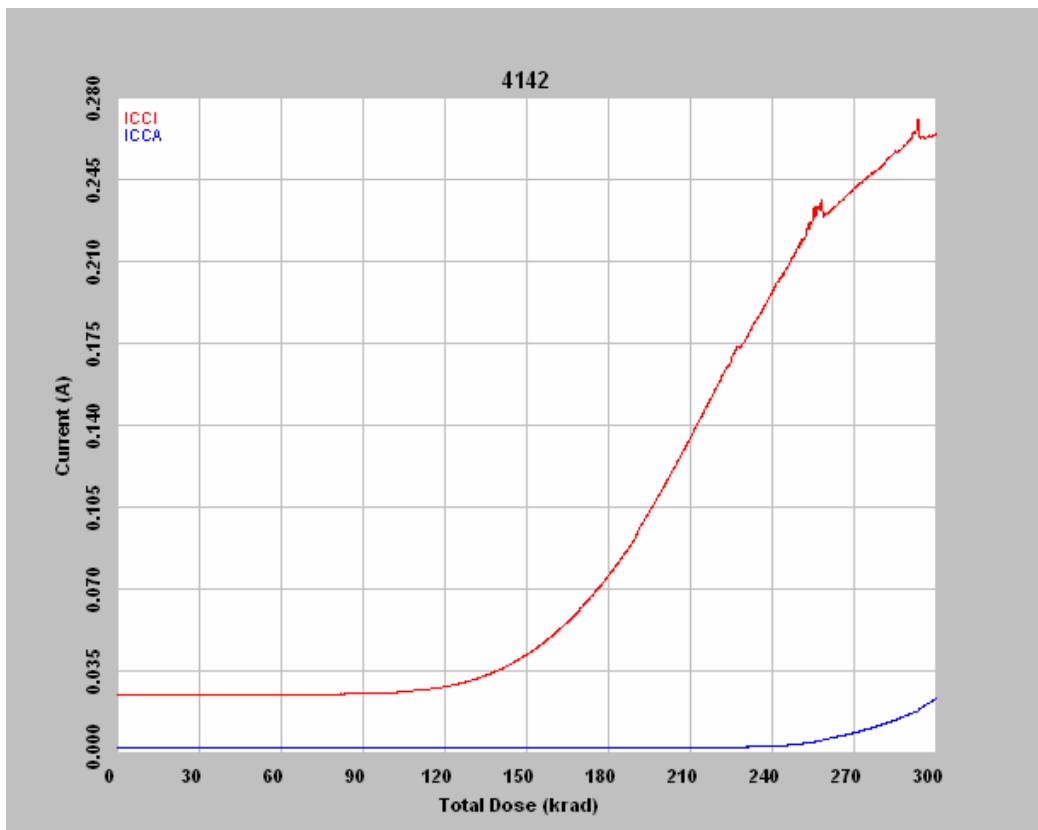


Figure 4 DUT 4142 in-flux I_{CCA} and I_{CCI}

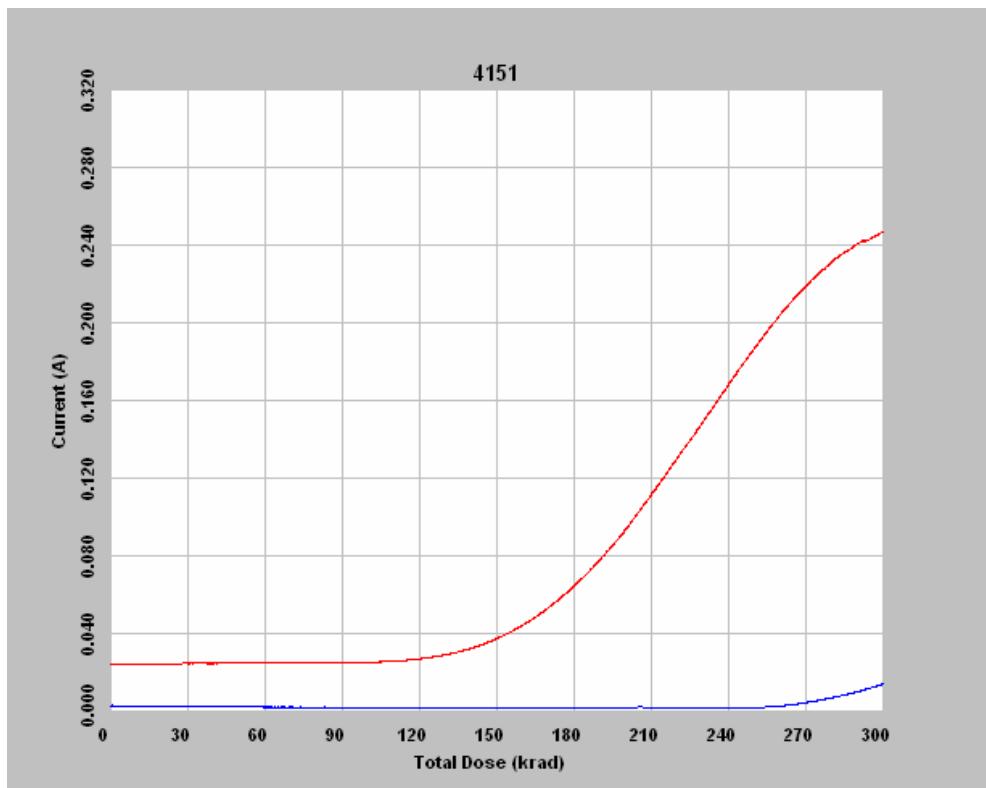


Figure 5 DUT 4151 in-flux I_{CCA} and I_{CCI}

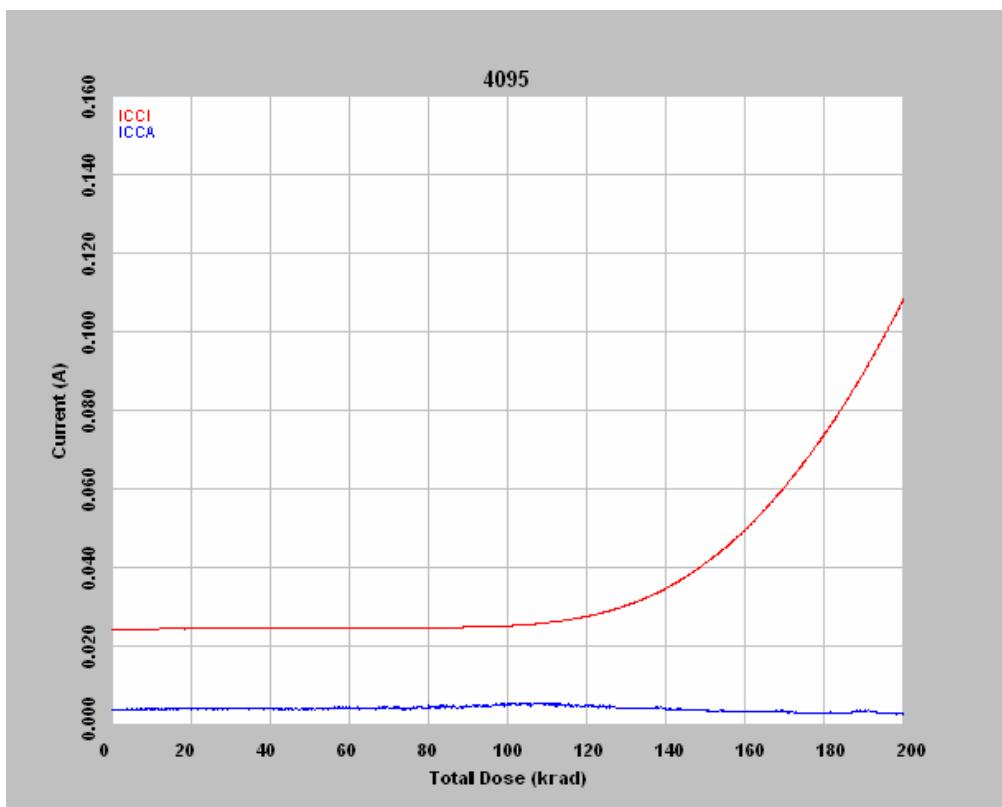


Figure 6 DUT 4095 in-flux I_{CCA} and I_{CCI}

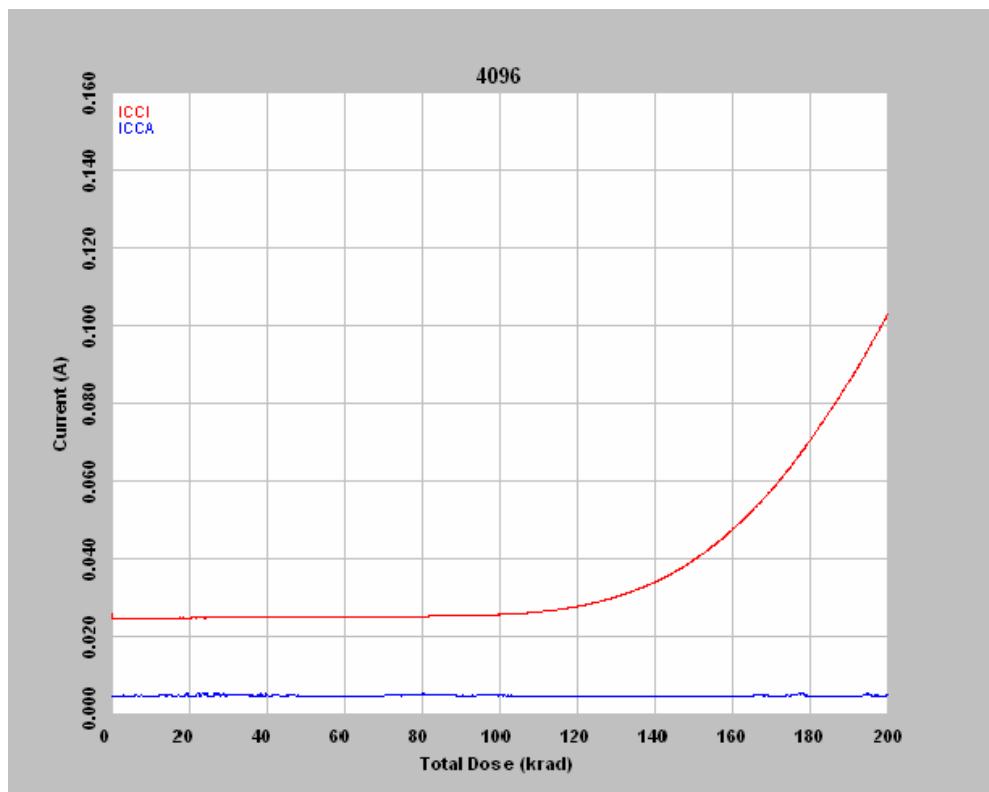


Figure 7 DUT 4096 in-flux I_{CCA} and I_{CCI}

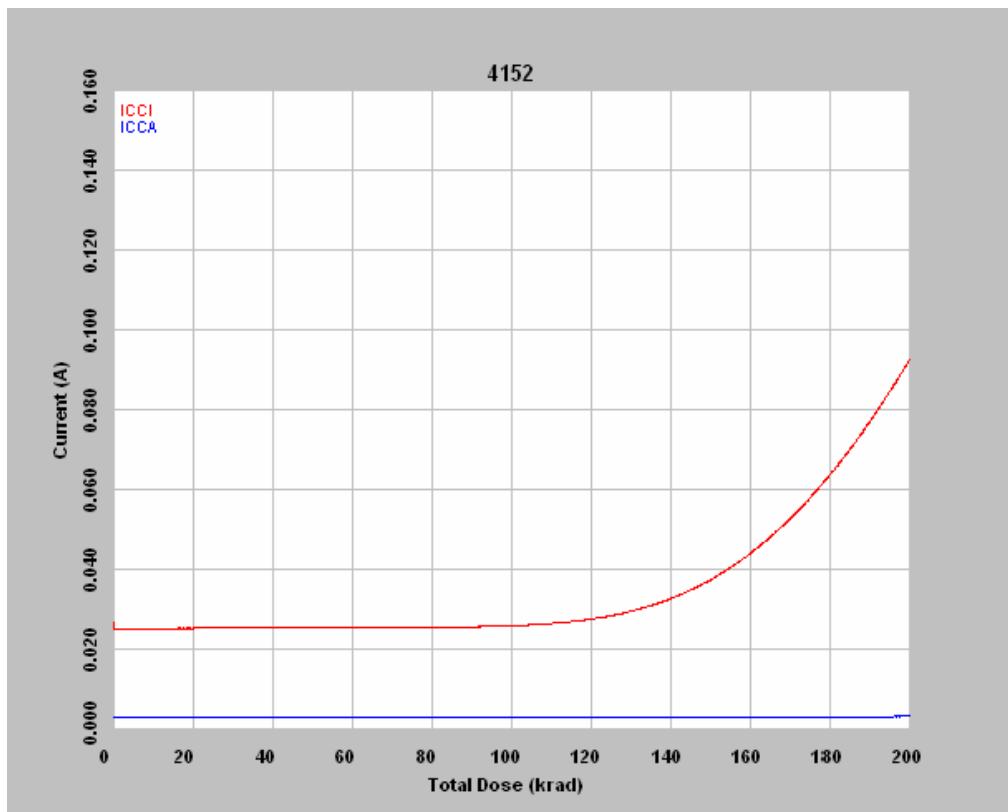


Figure 8 DUT 4152 in-flux I_{CCA} and I_{CCI}

C. Single-Ended V_{IL}/V_{IH} and I_{IL}/I_{IH}

Table 3 displays the pre-irradiation and post-annealing single-ended V_{IL} ; every data in this table passes the spec. Table 4 displays the pre-irradiation and post-annealing single-ended V_{IH} ; every data in this table passes the spec.

Table 5 displays the pre-irradiation and post-annealing single-ended I_{IL} ; every data in the table passes the spec. Table 6 displays the pre-irradiation and post-annealing single-ended I_{IH} ; every data in the table passes the spec. The PIPL for both I_{IL} and I_{IH} is 5 μ A.

Table 3a

DUT		4140		4142		4151	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	Bi_D_7	1.375	1.365	1.37	1.365	1.375	1.365
bi_levels_vil	Bi_D_6	1.36	1.35	1.355	1.35	1.365	1.35
bi_levels_vil	Bi_D_5	1.365	1.355	1.365	1.355	1.365	1.355
bi_levels_vil	Bi_D_4	1.37	1.36	1.365	1.355	1.37	1.355
bi_levels_vil	Bi_D_3	1.365	1.36	1.365	1.36	1.37	1.36
bi_levels_vil	Bi_D_2	1.36	1.355	1.36	1.355	1.36	1.355
bi_levels_vil	Bi_D_1	1.36	1.355	1.35	1.35	1.365	1.35
bi_levels_vil	DA	1.385	1.365	1.365	1.36	1.385	1.36
bi_levels_vil	EN8	1.355	1.335	1.33	1.325	1.34	1.325
bi_levels_vil	IO_I_6	1.355	1.35	1.35	1.34	1.355	1.34
bi_levels_vil	IO_I_5	1.34	1.345	1.345	1.34	1.34	1.34
bi_levels_vil	IO_I_4	1.395	1.39	1.39	1.385	1.39	1.385
bi_levels_vil	IO_I_3	1.385	1.385	1.385	1.38	1.385	1.38
bi_levels_vil	IO_I_2	1.395	1.39	1.39	1.385	1.395	1.385
bi_levels_vil	IO_I_1	1.385	1.38	1.385	1.375	1.39	1.375
bi_levels_vil	RCLK1P	1.43	1.425	1.43	1.425	1.435	1.425
bi_levels_vil	RCLK2P	1.43	1.425	1.43	1.425	1.435	1.425

Table 3b

DUT		4095		4096		4152	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	Bi_D_7	1.375	1.37	1.375	1.37	1.37	1.365
bi_levels_vil	Bi_D_6	1.365	1.355	1.365	1.355	1.35	1.345
bi_levels_vil	Bi_D_5	1.37	1.36	1.365	1.36	1.36	1.355
bi_levels_vil	Bi_D_4	1.37	1.36	1.37	1.365	1.365	1.36
bi_levels_vil	Bi_D_3	1.37	1.365	1.37	1.36	1.36	1.355
bi_levels_vil	Bi_D_2	1.36	1.355	1.365	1.355	1.36	1.355
bi_levels_vil	Bi_D_1	1.365	1.36	1.365	1.355	1.36	1.35
bi_levels_vil	DA	1.385	1.385	1.385	1.365	1.385	1.365
bi_levels_vil	EN8	1.34	1.335	1.34	1.335	1.335	1.33
bi_levels_vil	IO_I_6	1.355	1.385	1.355	1.35	1.355	1.35
bi_levels_vil	IO_I_5	1.345	1.35	1.35	1.35	1.35	1.34
bi_levels_vil	IO_I_4	1.395	1.39	1.395	1.39	1.39	1.385
bi_levels_vil	IO_I_3	1.395	1.385	1.375	1.385	1.385	1.37
bi_levels_vil	IO_I_2	1.395	1.395	1.395	1.39	1.395	1.39
bi_levels_vil	IO_I_1	1.39	1.39	1.385	1.385	1.39	1.38
bi_levels_vil	RCLK1P	1.435	1.43	1.435	1.43	1.43	1.425
bi_levels_vil	RCLK2P	1.435	1.43	1.435	1.43	1.43	1.425

Table 4a

DUT		4140		4142		4151	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	Bi_D_7	1.375	1.365	1.37	1.365	1.375	1.365
bi_levels_vih	Bi_D_6	1.375	1.37	1.38	1.37	1.38	1.37
bi_levels_vih	Bi_D_5	1.37	1.36	1.37	1.355	1.375	1.355
bi_levels_vih	Bi_D_4	1.37	1.36	1.365	1.355	1.37	1.355
bi_levels_vih	Bi_D_3	1.38	1.375	1.38	1.375	1.385	1.375
bi_levels_vih	Bi_D_2	1.375	1.37	1.375	1.37	1.375	1.37
bi_levels_vih	Bi_D_1	1.37	1.365	1.37	1.365	1.375	1.365
bi_levels_vih	DA	1.39	1.385	1.385	1.38	1.395	1.38
bi_levels_vih	EN8	1.44	1.435	1.435	1.43	1.41	1.43
bi_levels_vih	IO_I_6	1.41	1.41	1.405	1.4	1.41	1.4
bi_levels_vih	IO_I_5	1.425	1.395	1.425	1.415	1.435	1.415
bi_levels_vih	IO_I_4	1.39	1.385	1.385	1.375	1.39	1.375
bi_levels_vih	IO_I_3	1.395	1.39	1.395	1.385	1.395	1.385
bi_levels_vih	IO_I_2	1.39	1.385	1.385	1.375	1.39	1.375
bi_levels_vih	IO_I_1	1.39	1.385	1.39	1.38	1.395	1.38
bi_levels_vih	RCLK1P	1.42	1.415	1.425	1.415	1.425	1.415
bi_levels_vih	RCLK2P	1.43	1.415	1.43	1.425	1.435	1.425

Table 4b

DUT		4095		4096		4152	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	Bi_D_7	1.375	1.37	1.375	1.365	1.37	1.365
bi_levels_vih	Bi_D_6	1.38	1.375	1.385	1.375	1.375	1.37
bi_levels_vih	Bi_D_5	1.38	1.37	1.375	1.37	1.375	1.365
bi_levels_vih	Bi_D_4	1.37	1.365	1.37	1.365	1.365	1.36
bi_levels_vih	Bi_D_3	1.38	1.38	1.385	1.375	1.375	1.37
bi_levels_vih	Bi_D_2	1.375	1.37	1.38	1.375	1.375	1.37
bi_levels_vih	Bi_D_1	1.38	1.37	1.375	1.37	1.37	1.365
bi_levels_vih	DA	1.395	1.385	1.39	1.385	1.39	1.39
bi_levels_vih	EN8	1.4	1.4	1.445	1.44	1.44	1.435
bi_levels_vih	IO_I_6	1.415	1.41	1.415	1.41	1.415	1.41
bi_levels_vih	IO_I_5	1.43	1.43	1.43	1.42	1.43	1.395
bi_levels_vih	IO_I_4	1.385	1.385	1.39	1.385	1.385	1.38
bi_levels_vih	IO_I_3	1.4	1.395	1.395	1.39	1.395	1.39
bi_levels_vih	IO_I_2	1.39	1.385	1.39	1.385	1.39	1.385
bi_levels_vih	IO_I_1	1.395	1.39	1.395	1.39	1.395	1.39
bi_levels_vih	RCLK1P	1.43	1.42	1.425	1.42	1.42	1.415
bi_levels_vih	RCLK2P	1.435	1.425	1.435	1.43	1.43	1.425

Table 5a

DUT		4140		4142		4151	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIL_Inputs_Max_	Bi_D_1	330.9 pA	< 1 uA	-3.2 nA	< 1 uA	-2.2 nA	< 1 uA
IIL_Inputs_Max_	Bi_D_2	121.6 pA	< 1 uA	121.6 pA	< 1 uA	958.7 pA	< 1 uA
IIL_Inputs_Max_	Bi_D_3	2.4 nA	< 1 uA	958.7 pA	< 1 uA	1.6 nA	< 1 uA
IIL_Inputs_Max_	Bi_D_4	-1.8 nA	< 1 uA	-2.6 nA	< 1 uA	-3.4 nA	966.4 nA
IIL_Inputs_Max_	Bi_D_5	-2.0 nA	< 1 uA	-1.5 nA	966.4 nA	-1.1 nA	< 1 uA
IIL_Inputs_Max_	Bi_D_6	-1.9 nA	< 1 uA	-2.8 nA	< 1 uA	-4.4 nA	< 1 uA
IIL_Inputs_Max_	Bi_D_7	-4.5 nA	< 1 uA	-3.7 nA	< 1 uA	-2.8 nA	< 1 uA
IIL_Inputs_Max_	Bi_E_1	-3.2 nA	< 1 uA	-3.0 nA	911.1 nA	-2.8 nA	994.6 nA
IIL_Inputs_Max_	Bi_E_2	-3.4 nA	765.0 nA	740.3 pA	660.7 nA	-2.2 nA	806.8 nA
IIL_Inputs_Max_	Bi_E_3	-2.4 nA	326.7 nA	-2.4 nA	326.7 nA	-3.7 nA	243.2 nA
IIL_Inputs_Max_	Bi_E_4	-2.0 nA	493.7 nA	-1.1 nA	243.2 nA	-2.8 nA	243.2 nA
IIL_Inputs_Max_	Bi_E_5	-2.4 nA	451.9 nA	-2.8 nA	347.6 nA	-1.6 nA	368.4 nA
IIL_Inputs_Max_	Bi_E_6	-725.8 pA	326.7 nA	-1.6 nA	201.5 nA	321.4 pA	347.6 nA
IIL_Inputs_Max_	Bi_E_7	-1.8 nA	222.3 nA	-3.9 nA	347.6 nA	-2.0 nA	326.7 nA
IIL_Inputs_Max_	DA	-2.5 nA	205.5 nA	-2.5 nA	-3.3 nA	-4.8 nA	38.5 nA
IIL_Inputs_Max_	DIO_IN_1	-1.7 nA	115.7 nA	-1.9 nA	32.2 nA	-672.2 pA	74.0 nA
IIL_Inputs_Max_	DIO_IN_2	-2.5 nA	163.7 nA	-1.8 nA	38.5 nA	-5.0 nA	17.6 nA
IIL_Inputs_Max_	DIO_IN_3	-2.7 nA	80.2 nA	-2.7 nA	59.4 nA	-592.8 pA	38.5 nA
IIL_Inputs_Max_	DIO_IN_4	2.5 nA	-218.2 nA	2.3 nA	-9.5 nA	583.5 pA	-51.2 nA
IIL_Inputs_Max_	DIO_IN_5	-1.6 nA	101.1 nA	-3.1 nA	17.6 nA	-3.7 nA	205.5 nA
IIL_Inputs_Max_	DIO_IN_6	-2.5 nA	205.5 nA	-2.5 nA	122.0 nA	-2.3 nA	-24.1 nA
IIL_Inputs_Max_	DIO_IN_7	-3.3 nA	101.1 nA	-2.7 nA	38.5 nA	-2.5 nA	101.1 nA
IIL_Inputs_Max_	DIO_IP_1	1.8 nA	53.1 nA	-1.3 nA	11.4 nA	-44.3 pA	32.2 nA
IIL_Inputs_Max_	DIO_IP_2	-1.0 nA	163.7 nA	-3.1 nA	38.5 nA	-2.5 nA	163.7 nA
IIL_Inputs_Max_	DIO_IP_3	-881.4 pA	94.9 nA	-672.2 pA	32.2 nA	-1.1 nA	32.2 nA
IIL_Inputs_Max_	DIO_IP_4	-1.8 nA	80.2 nA	-1.2 nA	163.7 nA	-1.4 nA	17.6 nA
IIL_Inputs_Max_	DIO_IP_5	-2.3 nA	101.1 nA	-2.5 nA	142.9 nA	-3.1 nA	101.1 nA
IIL_Inputs_Max_	DIO_IP_6	-2.3 nA	-24.1 nA	-2.7 nA	-3.3 nA	-1.2 nA	226.4 nA
IIL_Inputs_Max_	DIO_IP_7	-2.1 nA	17.6 nA	-2.5 nA	268.1 nA	-802.2 pA	17.6 nA
IIL_Inputs_Max_	EN8	-3.1 nA	38.5 nA	-4.4 nA	-3.3 nA	-1.8 nA	80.2 nA
IIL_Inputs_Max_	HCLK1P	-3.4 nA	13.6 nA	-2.0 nA	-69.9 nA	-3.2 nA	-69.9 nA
IIL_Inputs_Max_	HCLK2P	-1.5 nA	178.3 nA	-1.3 nA	178.3 nA	583.5 pA	-72.1 nA
IIL_Inputs_Max_	HCLK3P	6.2 nA	69.7 nA	2.0 nA	194.9 nA	2.0 nA	90.6 nA
IIL_Inputs_Max_	HCLK4P	1.4 nA	173.6 nA	-286.7 pA	152.8 nA	-914.7 pA	278.0 nA
IIL_Inputs_Max_	IO_I_1	-1.1 nA	199.2 nA	-672.2 pA	94.9 nA	-2.6 nA	-72.1 nA
IIL_Inputs_Max_	IO_I_2	3.9 nA	153.2 nA	1.6 nA	111.5 nA	1.6 nA	153.2 nA
IIL_Inputs_Max_	IO_I_3	374.2 pA	32.2 nA	-462.9 pA	74.0 nA	374.2 pA	199.2 nA
IIL_Inputs_Max_	IO_I_4	2.8 nA	111.5 nA	749.4 pA	7.1 nA	749.4 pA	153.2 nA
IIL_Inputs_Max_	IO_I_5	164.9 pA	94.9 nA	-462.9 pA	115.7 nA	1.0 nA	-9.5 nA
IIL_Inputs_Max_	IO_I_6	-1.6 nA	122.0 nA	-2.3 nA	38.5 nA	-2.1 nA	38.5 nA
IIL_Inputs_Max_	LOADIN	-6.3 nA	25.9 nA	-5.1 nA	25.9 nA	-5.9 nA	172.2 nA
IIL_Inputs_Max_	RCLK1P	2.3 nA	282.7 nA	-881.4 pA	387.0 nA	792.8 pA	345.3 nA
IIL_Inputs_Max_	RCLK2P	-1.1 nA	382.3 nA	550.5 pA	465.7 nA	-705.4 pA	486.6 nA
IIL_Inputs_Max_	RCLK3P	3.1 nA	-97.2 nA	2.6 nA	90.6 nA	3.5 nA	132.3 nA
IIL_Inputs_Max_	RCLK4P	-3.2 nA	-90.7 nA	-4.1 nA	76.2 nA	-2.2 nA	-7.3 nA

Table 5b

DUT		4095		4096		4152	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIL_Inputs_Max_	Bi_D_1	-506.2 pA	< 1 uA	-924.7 pA	< 1 uA	-3.2 nA	< 1 uA
IIL_Inputs_Max_	Bi_D_2	1.8 nA	< 1 uA	-1.1 nA	< 1 uA	2.0 nA	< 1 uA
IIL_Inputs_Max_	Bi_D_3	2.6 nA	< 1 uA	4.5 nA	< 1 uA	3.7 nA	< 1 uA
IIL_Inputs_Max_	Bi_D_4	-1.8 nA	820.4 nA	-3.2 nA	966.4 nA	-1.3 nA	< 1 uA
IIL_Inputs_Max_	Bi_D_5	-914.7 pA	< 1 uA	-496.0 pA	862.1 nA	341.2 pA	966.4 nA
IIL_Inputs_Max_	Bi_D_6	-881.4 pA	< 1 uA	-5.3 nA	< 1 uA	583.5 pA	< 1 uA
IIL_Inputs_Max_	Bi_D_7	-4.9 nA	< 1 uA	-4.5 nA	< 1 uA	-4.5 nA	-883.9 nA
IIL_Inputs_Max_	Bi_E_1	-3.9 nA	869.4 nA	-2.4 nA	869.4 nA	-1.8 nA	911.1 nA
IIL_Inputs_Max_	Bi_E_2	-725.8 pA	618.9 nA	-2.4 nA	765.0 nA	-306.9 pA	744.1 nA
IIL_Inputs_Max_	Bi_E_3	-4.7 nA	285.0 nA	-1.1 nA	243.2 nA	-3.2 nA	305.8 nA
IIL_Inputs_Max_	Bi_E_4	-2.0 nA	285.0 nA	-3.7 nA	347.6 nA	-2.6 nA	431.1 nA
IIL_Inputs_Max_	Bi_E_5	-1.6 nA	347.6 nA	-4.1 nA	326.7 nA	-1.4 nA	285.0 nA
IIL_Inputs_Max_	Bi_E_6	-4.1 nA	222.3 nA	-3.4 nA	285.0 nA	-2.2 nA	222.3 nA
IIL_Inputs_Max_	Bi_E_7	-3.0 nA	451.9 nA	-725.8 pA	305.8 nA	-2.2 nA	243.2 nA
IIL_Inputs_Max_	DA	-5.6 nA	101.1 nA	-5.0 nA	38.5 nA	-4.2 nA	-3.3 nA
IIL_Inputs_Max_	DIO_IN_1	164.9 pA	74.0 nA	-462.9 pA	115.7 nA	792.8 pA	94.9 nA
IIL_Inputs_Max_	DIO_IN_2	-3.9 nA	-128.5 nA	-3.1 nA	38.5 nA	-1.2 nA	80.2 nA
IIL_Inputs_Max_	DIO_IN_3	-1.8 nA	-65.9 nA	-1.0 nA	184.6 nA	-1.6 nA	-45.0 nA
IIL_Inputs_Max_	DIO_IN_4	-672.2 pA	115.7 nA	374.2 pA	53.1 nA	2.5 nA	-9.5 nA
IIL_Inputs_Max_	DIO_IN_5	-1.6 nA	-65.9 nA	-2.3 nA	59.4 nA	-1.6 nA	17.6 nA
IIL_Inputs_Max_	DIO_IN_6	-592.8 pA	80.2 nA	-1.6 nA	101.1 nA	-1.8 nA	80.2 nA
IIL_Inputs_Max_	DIO_IN_7	454.3 pA	163.7 nA	-2.3 nA	-3.3 nA	-2.3 nA	122.0 nA
IIL_Inputs_Max_	DIO_IP_1	-462.9 pA	53.1 nA	-672.2 pA	115.7 nA	1.8 nA	53.1 nA
IIL_Inputs_Max_	DIO_IP_2	-2.9 nA	-170.3 nA	-1.8 nA	80.2 nA	-2.1 nA	101.1 nA
IIL_Inputs_Max_	DIO_IP_3	164.9 pA	11.4 nA	-253.6 pA	-51.2 nA	-672.2 pA	115.7 nA
IIL_Inputs_Max_	DIO_IP_4	-2.3 nA	142.9 nA	-592.8 pA	-24.1 nA	-1.4 nA	-3.3 nA
IIL_Inputs_Max_	DIO_IP_5	-802.2 pA	-24.1 nA	-1.0 nA	17.6 nA	-2.5 nA	101.1 nA
IIL_Inputs_Max_	DIO_IP_6	-2.3 nA	-3.3 nA	-2.9 nA	17.6 nA	-2.3 nA	38.5 nA
IIL_Inputs_Max_	DIO_IP_7	-3.9 nA	163.7 nA	-802.2 pA	226.4 nA	-1.8 nA	-3.3 nA
IIL_Inputs_Max_	EN8	-3.3 nA	59.4 nA	-1.2 nA	101.1 nA	-1.8 nA	-3.3 nA
IIL_Inputs_Max_	HCLK1P	-2.4 nA	34.5 nA	-1.4 nA	13.6 nA	-1.4 nA	34.5 nA
IIL_Inputs_Max_	HCLK2P	792.8 pA	94.9 nA	2.0 nA	74.0 nA	-44.3 pA	136.6 nA
IIL_Inputs_Max_	HCLK3P	4.5 nA	28.0 nA	2.4 nA	-34.6 nA	3.9 nA	174.0 nA
IIL_Inputs_Max_	HCLK4P	-1.5 nA	215.4 nA	-286.7 pA	152.8 nA	-496.0 pA	152.8 nA
IIL_Inputs_Max_	IO_I_1	1.0 nA	53.1 nA	1.2 nA	94.9 nA	-44.3 pA	32.2 nA
IIL_Inputs_Max_	IO_I_2	1.8 nA	48.9 nA	3.1 nA	48.9 nA	2.8 nA	132.3 nA
IIL_Inputs_Max_	IO_I_3	-881.4 pA	32.2 nA	-672.2 pA	-51.2 nA	374.2 pA	53.1 nA
IIL_Inputs_Max_	IO_I_4	2.4 nA	111.5 nA	4.1 nA	69.7 nA	1.6 nA	153.2 nA
IIL_Inputs_Max_	IO_I_5	1.2 nA	53.1 nA	-44.3 pA	53.1 nA	-253.6 pA	303.6 nA
IIL_Inputs_Max_	IO_I_6	-1.0 nA	122.0 nA	-1.2 nA	80.2 nA	-383.4 pA	101.1 nA
IIL_Inputs_Max_	LOADIN	-6.8 nA	46.8 nA	-6.3 nA	5.1 nA	-1.3 nA	-99.4 nA
IIL_Inputs_Max_	RCLK1P	583.5 pA	407.9 nA	-1.9 nA	261.8 nA	-44.3 pA	345.3 nA
IIL_Inputs_Max_	RCLK2P	341.2 pA	319.7 nA	341.2 pA	570.0 nA	759.8 pA	507.4 nA
IIL_Inputs_Max_	RCLK3P	2.2 nA	-34.6 nA	2.2 nA	-76.3 nA	3.3 nA	111.5 nA
IIL_Inputs_Max_	RCLK4P	-2.0 nA	34.5 nA	-2.6 nA	-49.0 nA	-3.7 nA	-69.9 nA

Table 5c

DUT		4140		4142		4151	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIL_BiOuts_Max_	Bi_IO_1	316.8 nA	-51.2 nA	-4.2 nA	32.2 nA	-2.3 nA	178.3 nA
IIL_BiOuts_Max_	Bi_IO_2	-13.5 nA	27.6 nA	-4.5 nA	-14.1 nA	-4.7 nA	111.0 nA
IIL_BiOuts_Max_	Bi_IO_3	-2.8 nA	48.5 nA	-1.1 nA	173.6 nA	-705.4 pA	194.5 nA
IIL_BiOuts_Max_	Bi_IO_4	-1.7 nA	94.9 nA	164.9 pA	220.1 nA	-1.1 nA	32.2 nA
IIL_BiOuts_Max_	Bi_IO_5	-2.0 nA	-35.0 nA	-1.8 nA	< 1 uA	-914.7 pA	194.5 nA
IIL_BiOuts_Max_	Bi_IO_6	-4.2 nA	-266.5 nA	-5.5 nA	-287.4 nA	-3.6 nA	-141.2 nA
IIL_BiOuts_Max_	Bi_IO_7	-3.4 nA	214.0 nA	-1.9 nA	172.2 nA	-3.2 nA	88.6 nA

Table 5d

DUT		4095		4096		4152	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIL_BiOuts_Max_	Bi_IO_1	-2.1 nA	136.6 nA	-3.0 nA	136.6 nA	334.0 nA	303.6 nA
IIL_BiOuts_Max_	Bi_IO_2	-3.0 nA	48.5 nA	-4.5 nA	-14.1 nA	-133.2 nA	27.6 nA
IIL_BiOuts_Max_	Bi_IO_3	131.9 pA	6.7 nA	-2.2 nA	173.6 nA	260.3 nA	611.8 nA
IIL_BiOuts_Max_	Bi_IO_4	-881.4 pA	74.0 nA	374.2 pA	94.9 nA	NA	< 1 uA
IIL_BiOuts_Max_	Bi_IO_5	-1.8 nA	90.2 nA	341.2 pA	48.5 nA	NA	< 1 uA
IIL_BiOuts_Max_	Bi_IO_6	-3.6 nA	-433.6 nA	-3.2 nA	-203.8 nA	NA	-120.3 nA
IIL_BiOuts_Max_	Bi_IO_7	-2.2 nA	-57.6 nA	-1.3 nA	67.7 nA	NA	402.0 nA

Table 6a

DUT		4140		4142		4151	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_Inputs_Max_	Bi_D_1	8.1 nA	< 1 uA	9.3 nA	< 1 uA	7.9 nA	< 1 uA
IIH_Inputs_Max_	Bi_D_2	7.2 nA	< 1 uA	8.3 nA	< 1 uA	5.6 nA	< 1 uA
IIH_Inputs_Max_	Bi_D_3	1.4 nA	< 1 uA	4.9 nA	< 1 uA	5.6 nA	< 1 uA
IIH_Inputs_Max_	Bi_D_4	2.6 nA	424.0 nA	3.9 nA	486.6 nA	3.3 nA	674.4 nA
IIH_Inputs_Max_	Bi_D_5	550.5 pA	528.3 nA	1.2 nA	403.1 nA	759.8 pA	403.1 nA
IIH_Inputs_Max_	Bi_D_6	5.2 nA	< 1 uA	6.4 nA	< 1 uA	5.2 nA	< 1 uA
IIH_Inputs_Max_	Bi_D_7	2.4 nA	744.1 nA	3.3 nA	890.2 nA	4.5 nA	848.5 nA
IIH_Inputs_Max_	Bi_E_1	3.0 nA	618.9 nA	2.4 nA	431.1 nA	4.3 nA	514.5 nA
IIH_Inputs_Max_	Bi_E_2	321.4 pA	326.7 nA	949.7 pA	326.7 nA	949.7 pA	368.4 nA
IIH_Inputs_Max_	Bi_E_3	1.2 nA	389.3 nA	112.0 pA	368.4 nA	-97.5 pA	368.4 nA
IIH_Inputs_Max_	Bi_E_4	-306.9 pA	577.2 nA	2.8 nA	556.3 nA	1.2 nA	451.9 nA
IIH_Inputs_Max_	Bi_E_5	949.7 pA	451.9 nA	1.6 nA	347.6 nA	-1.8 nA	285.0 nA
IIH_Inputs_Max_	Bi_E_6	1.8 nA	451.9 nA	321.4 pA	264.1 nA	2.4 nA	410.2 nA
IIH_Inputs_Max_	Bi_E_7	1.6 nA	-28.1 nA	949.7 pA	-7.3 nA	-935.2 pA	13.6 nA
IIH_Inputs_Max_	DA	873.1 pA	142.9 nA	1.7 nA	289.0 nA	2.1 nA	205.5 nA
IIH_Inputs_Max_	DIO_IN_1	5.6 nA	178.3 nA	1.6 nA	74.0 nA	2.0 nA	115.7 nA
IIH_Inputs_Max_	DIO_IN_2	-383.4 pA	80.2 nA	663.7 pA	142.9 nA	663.7 pA	163.7 nA
IIH_Inputs_Max_	DIO_IN_3	-802.2 pA	247.3 nA	1.3 nA	59.4 nA	-1.4 nA	163.7 nA
IIH_Inputs_Max_	DIO_IN_4	3.1 nA	178.3 nA	3.3 nA	32.2 nA	2.9 nA	74.0 nA
IIH_Inputs_Max_	DIO_IN_5	-383.4 pA	122.0 nA	-383.4 pA	142.9 nA	-592.8 pA	247.3 nA
IIH_Inputs_Max_	DIO_IN_6	454.3 pA	184.6 nA	1.9 nA	122.0 nA	244.9 pA	205.5 nA
IIH_Inputs_Max_	DIO_IN_7	2.3 nA	184.6 nA	244.9 pA	142.9 nA	1.5 nA	101.1 nA
IIH_Inputs_Max_	DIO_IP_1	2.3 nA	282.7 nA	2.9 nA	220.1 nA	1.6 nA	-30.4 nA
IIH_Inputs_Max_	DIO_IP_2	1.9 nA	122.0 nA	1.5 nA	101.1 nA	35.5 pA	122.0 nA
IIH_Inputs_Max_	DIO_IP_3	2.3 nA	11.4 nA	792.8 pA	136.6 nA	164.9 pA	115.7 nA
IIH_Inputs_Max_	DIO_IP_4	873.1 pA	163.7 nA	-592.8 pA	226.4 nA	663.7 pA	226.4 nA
IIH_Inputs_Max_	DIO_IP_5	454.3 pA	247.3 nA	1.9 nA	163.7 nA	1.5 nA	142.9 nA
IIH_Inputs_Max_	DIO_IP_6	2.5 nA	268.1 nA	244.9 pA	309.9 nA	873.1 pA	247.3 nA
IIH_Inputs_Max_	DIO_IP_7	1.5 nA	226.4 nA	873.1 pA	163.7 nA	-1.4 nA	205.5 nA
IIH_Inputs_Max_	EN8	1.5 nA	184.6 nA	1.1 nA	59.4 nA	873.1 pA	142.9 nA
IIH_Inputs_Max_	HCLK1P	-306.9 pA	-7.3 nA	-2.0 nA	55.4 nA	1.2 nA	13.6 nA
IIH_Inputs_Max_	HCLK2P	2.0 nA	74.0 nA	3.5 nA	-113.9 nA	1.6 nA	157.5 nA
IIH_Inputs_Max_	HCLK3P	3.9 nA	-13.7 nA	2.8 nA	132.3 nA	4.7 nA	174.0 nA
IIH_Inputs_Max_	HCLK4P	-1.1 nA	27.6 nA	-705.4 pA	27.6 nA	2.2 nA	131.9 nA
IIH_Inputs_Max_	IO_I_1	2.7 nA	-30.4 nA	374.2 pA	303.6 nA	4.1 nA	94.9 nA
IIH_Inputs_Max_	IO_I_2	2.8 nA	132.3 nA	1.6 nA	153.2 nA	3.5 nA	153.2 nA
IIH_Inputs_Max_	IO_I_3	2.3 nA	178.3 nA	2.0 nA	-51.2 nA	792.8 pA	282.7 nA
IIH_Inputs_Max_	IO_I_4	4.7 nA	132.3 nA	4.9 nA	153.2 nA	4.3 nA	69.7 nA
IIH_Inputs_Max_	IO_I_5	3.5 nA	-9.5 nA	3.1 nA	178.3 nA	3.5 nA	94.9 nA
IIH_Inputs_Max_	IO_I_6	-1.0 nA	122.0 nA	-802.2 pA	142.9 nA	663.7 pA	205.5 nA
IIH_Inputs_Max_	LOADIN	362.6 pA	67.7 nA	1.8 nA	-36.7 nA	2.7 nA	-15.8 nA
IIH_Inputs_Max_	RCLK1P	3.5 nA	470.5 nA	3.7 nA	512.3 nA	3.5 nA	-72.1 nA
IIH_Inputs_Max_	RCLK2P	-1.5 nA	403.1 nA	759.8 pA	403.1 nA	-286.7 pA	382.3 nA
IIH_Inputs_Max_	RCLK3P	4.1 nA	153.2 nA	5.6 nA	194.9 nA	3.3 nA	48.9 nA
IIH_Inputs_Max_	RCLK4P	-97.5 pA	-28.1 nA	-725.8 pA	34.5 nA	-1.6 nA	-28.1 nA

Table 6b

DUT		4095		4096		4152	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_Inputs_Max_	Bi_D_1	7.7 nA	< 1 uA	6.6 nA	< 1 uA	8.5 nA	< 1 mA
IIH_Inputs_Max_	Bi_D_2	2.0 nA	< 1 uA	6.0 nA	< 1 uA	6.0 nA	< 1 uA
IIH_Inputs_Max_	Bi_D_3	5.4 nA	< 1 uA	3.7 nA	< 1 uA	4.1 nA	< 1 uA
IIH_Inputs_Max_	Bi_D_4	3.5 nA	486.6 nA	2.2 nA	570.0 nA	3.9 nA	528.3 nA
IIH_Inputs_Max_	Bi_D_5	2.4 nA	382.3 nA	759.8 pA	319.7 nA	3.5 nA	236.2 nA
IIH_Inputs_Max_	Bi_D_6	3.5 nA	< 1 uA	4.6 nA	< 1 uA	5.0 nA	971.4 nA
IIH_Inputs_Max_	Bi_D_7	2.4 nA	< 1 uA	3.5 nA	827.6 nA	4.5 nA	973.7 nA
IIH_Inputs_Max_	Bi_E_1	530.9 pA	431.1 nA	3.0 nA	347.6 nA	949.7 pA	472.8 nA
IIH_Inputs_Max_	Bi_E_2	4.9 nA	347.6 nA	1.4 nA	305.8 nA	1.2 nA	514.5 nA
IIH_Inputs_Max_	Bi_E_3	2.2 nA	305.8 nA	1.8 nA	431.1 nA	-97.5 pA	431.1 nA
IIH_Inputs_Max_	Bi_E_4	-306.9 pA	514.5 nA	321.4 pA	514.5 nA	-1.4 nA	702.4 nA
IIH_Inputs_Max_	Bi_E_5	1.8 nA	368.4 nA	-97.5 pA	368.4 nA	321.4 pA	431.1 nA
IIH_Inputs_Max_	Bi_E_6	112.0 pA	347.6 nA	321.4 pA	431.1 nA	1.4 nA	222.3 nA
IIH_Inputs_Max_	Bi_E_7	112.0 pA	264.1 nA	-97.5 pA	118.0 nA	-3.0 nA	744.1 nA
IIH_Inputs_Max_	DA	1.7 nA	142.9 nA	2.3 nA	122.0 nA	663.7 pA	122.0 nA
IIH_Inputs_Max_	DIO_IN_1	3.7 nA	240.9 nA	2.5 nA	136.6 nA	3.3 nA	136.6 nA
IIH_Inputs_Max_	DIO_IN_2	-802.2 pA	184.6 nA	-592.8 pA	205.5 nA	873.1 pA	122.0 nA
IIH_Inputs_Max_	DIO_IN_3	-592.8 pA	142.9 nA	1.1 nA	247.3 nA	663.7 pA	142.9 nA
IIH_Inputs_Max_	DIO_IN_4	1.6 nA	115.7 nA	-672.2 pA	178.3 nA	3.1 nA	178.3 nA
IIH_Inputs_Max_	DIO_IN_5	1.5 nA	59.4 nA	-174.0 pA	184.6 nA	2.5 nA	17.6 nA
IIH_Inputs_Max_	DIO_IN_6	2.5 nA	247.3 nA	2.1 nA	142.9 nA	663.7 pA	142.9 nA
IIH_Inputs_Max_	DIO_IN_7	1.9 nA	163.7 nA	1.5 nA	226.4 nA	2.5 nA	122.0 nA
IIH_Inputs_Max_	DIO_IP_1	1.8 nA	136.6 nA	5.8 nA	240.9 nA	3.5 nA	11.4 nA
IIH_Inputs_Max_	DIO_IP_2	2.8 nA	184.6 nA	-383.4 pA	163.7 nA	-1.0 nA	163.7 nA
IIH_Inputs_Max_	DIO_IP_3	2.9 nA	74.0 nA	4.1 nA	115.7 nA	4.6 nA	11.4 nA
IIH_Inputs_Max_	DIO_IP_4	35.5 pA	122.0 nA	35.5 pA	163.7 nA	-1.4 nA	247.3 nA
IIH_Inputs_Max_	DIO_IP_5	-174.0 pA	247.3 nA	-592.8 pA	205.5 nA	35.5 pA	163.7 nA
IIH_Inputs_Max_	DIO_IP_6	2.8 nA	184.6 nA	873.1 pA	163.7 nA	244.9 pA	247.3 nA
IIH_Inputs_Max_	DIO_IP_7	1.7 nA	142.9 nA	2.1 nA	59.4 nA	-1.2 nA	101.1 nA
IIH_Inputs_Max_	EN8	35.5 pA	142.9 nA	454.3 pA	184.6 nA	-1.0 nA	289.0 nA
IIH_Inputs_Max_	HCLK1P	-97.5 pA	180.6 nA	112.0 pA	-49.0 nA	1.4 nA	34.5 nA
IIH_Inputs_Max_	HCLK2P	2.5 nA	11.4 nA	4.6 nA	11.4 nA	3.5 nA	53.1 nA
IIH_Inputs_Max_	HCLK3P	3.5 nA	90.6 nA	4.5 nA	28.0 nA	2.8 nA	111.5 nA
IIH_Inputs_Max_	HCLK4P	131.9 pA	27.6 nA	550.5 pA	27.6 nA	1.6 nA	48.5 nA
IIH_Inputs_Max_	IO_I_1	2.5 nA	-51.2 nA	792.8 pA	32.2 nA	3.7 nA	157.5 nA
IIH_Inputs_Max_	IO_I_2	4.9 nA	90.6 nA	2.4 nA	278.4 nA	6.4 nA	132.3 nA
IIH_Inputs_Max_	IO_I_3	2.5 nA	94.9 nA	1.8 nA	-9.5 nA	1.6 nA	11.4 nA
IIH_Inputs_Max_	IO_I_4	4.3 nA	7.1 nA	3.7 nA	132.3 nA	4.7 nA	-34.6 nA
IIH_Inputs_Max_	IO_I_5	2.9 nA	11.4 nA	2.5 nA	74.0 nA	1.6 nA	261.8 nA
IIH_Inputs_Max_	IO_I_6	-1.4 nA	38.5 nA	-1.8 nA	163.7 nA	-1.6 nA	38.5 nA
IIH_Inputs_Max_	LOADIN	2.2 nA	5.1 nA	991.4 pA	5.1 nA	2.0 nA	-36.7 nA
IIH_Inputs_Max_	RCLK1P	2.3 nA	-9.5 nA	1.2 nA	115.7 nA	2.3 nA	595.7 nA
IIH_Inputs_Max_	RCLK2P	1.6 nA	340.5 nA	-914.7 pA	361.4 nA	759.8 pA	507.4 nA
IIH_Inputs_Max_	RCLK3P	3.7 nA	111.5 nA	2.6 nA	111.5 nA	3.3 nA	28.0 nA
IIH_Inputs_Max_	RCLK4P	-2.2 nA	34.5 nA	-1.8 nA	76.2 nA	-306.9 pA	-7.3 nA

Table 6c

DUT		4140		4142		4151	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_BiOuts_Max	Bi_IO_1	-705.4 pA	157.5 nA	-1.3 nA	-9.5 nA	2.7 nA	178.3 nA
IIH_BiOuts_Max	Bi_IO_2	1.4 nA	< 1 uA	-1.1 nA	< 1 uA	341.2 pA	69.3 nA
IIH_BiOuts_Max	Bi_IO_3	-1.1 nA	6.7 nA	-77.4 pA	90.2 nA	-77.4 pA	173.6 nA
IIH_BiOuts_Max	Bi_IO_4	1.8 nA	115.7 nA	1.0 nA	11.4 nA	583.5 pA	11.4 nA
IIH_BiOuts_Max	Bi_IO_5	1.8 nA	111.0 nA	341.2 pA	111.0 nA	-496.0 pA	< 1 uA
IIH_BiOuts_Max	Bi_IO_6	362.6 pA	< 1 uA	-1.7 nA	< 1 uA	362.6 pA	109.5 nA
IIH_BiOuts_Max	Bi_IO_7	-1.1 nA	67.7 nA	-2.2 nA	-162.1 nA	-2.8 nA	25.9 nA

Table 6d

DUT		4095		4096		4152	
Parameter	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
IIH_BiOuts_Max	Bi_IO_1	2.3 nA	74.0 nA	2.7 nA	136.6 nA		178.3 nA
IIH_BiOuts_Max	Bi_IO_2	1.8 nA	69.3 nA	-286.7 pA	-76.7 nA		< 1 uA
IIH_BiOuts_Max	Bi_IO_3	1.4 nA	111.0 nA	-2.4 nA	48.5 nA		48.5 nA
IIH_BiOuts_Max	Bi_IO_4	1.6 nA	74.0 nA	3.1 nA	94.9 nA		53.1 nA
IIH_BiOuts_Max	Bi_IO_5	-1.1 nA	< 1 uA	-914.7 pA	< 1 uA		111.0 nA
IIH_BiOuts_Max	Bi_IO_6	-3.2 nA	-78.5 nA	-3.0 nA	25.9 nA		< 1 uA
IIH_BiOuts_Max	Bi_IO_7	-2.6 nA	-120.3 nA	-2.8 nA	-36.7 nA		-57.6 nA

D. Differential Input (LVPECL) Threshold Voltage (V_{IL}/V_{IH})

Table 7 and 8 show the pre-irradiation and post-annealing threshold-voltages of the LVPECL input. Every data passes the spec.

Table 7a

DUT		4140		4142		4151	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DIO_IP_7	100	75	95	75	105	75
bi_levels_vil	DIO_IP_6	105	80	120	90	95	90
bi_levels_vil	DIO_IP_5	105	75	110	85	95	85
bi_levels_vil	DIO_IP_4	100	80	95	65	90	65
bi_levels_vil	DIO_IP_3	95	70	95	70	90	70
bi_levels_vil	DIO_IP_2	100	80	90	70	95	70
bi_levels_vil	DIO_IP_1	85	65	80	55	80	55

Table7b

DUT		4095		4096		4152	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DIO_IP_7	100	90	90	75	95	80
bi_levels_vil	DIO_IP_6	100	90	105	90	105	95
bi_levels_vil	DIO_IP_5	110	100	110	100	110	100
bi_levels_vil	DIO_IP_4	90	80	95	80	95	80
bi_levels_vil	DIO_IP_3	95	85	90	80	90	75
bi_levels_vil	DIO_IP_2	85	70	110	95	90	80
bi_levels_vil	DIO_IP_1	75	70	70	65	85	75

Table 8a

DUT		4140		4142		4151	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DIO_IP_7	100	75	95	70	105	70
bi_levels_vih	DIO_IP_6	100	75	115	90	95	90
bi_levels_vih	DIO_IP_5	100	75	105	80	90	80
bi_levels_vih	DIO_IP_4	100	75	90	65	90	65
bi_levels_vih	DIO_IP_3	95	70	95	70	90	70
bi_levels_vih	DIO_IP_2	95	75	90	65	90	65
bi_levels_vih	DIO_IP_1	90	65	85	60	85	60

Table 8b

DUT		4095		4096		4152	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DIO_IP_7	95	85	90	75	90	75
bi_levels_vih	DIO_IP_6	100	85	100	85	105	90
bi_levels_vih	DIO_IP_5	105	95	110	95	110	95
bi_levels_vih	DIO_IP_4	90	80	90	75	90	80
bi_levels_vih	DIO_IP_3	95	85	90	80	90	75
bi_levels_vih	DIO_IP_2	80	70	105	95	90	75
bi_levels_vih	DIO_IP_1	80	70	80	65	95	80

E. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 9 and 10. Every post-annealing data passes the spec.

Table 9a

DUT		4140		4142		4151	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vol	Bi_IO_7	35	35	35	35	35	35
bi_levels_vol	Bi_IO_6	30	30	30	30	30	30
bi_levels_vol	Bi_IO_5	35	35	35	35	35	35
bi_levels_vol	Bi_IO_4	35	35	35	35	35	35
bi_levels_vol	Bi_IO_3	35	35	35	35	35	35
bi_levels_vol	Bi_IO_2	30	35	30	30	30	30
bi_levels_vol	Bi_IO_1	35	35	35	35	35	35
bi_levels_vol	Bi_Y_7	25	25	25	25	25	25
bi_levels_vol	Bi_Y_6	25	25	25	25	25	25
bi_levels_vol	Bi_Y_5	25	25	25	25	25	25
bi_levels_vol	Bi_Y_4	25	25	25	25	25	25
bi_levels_vol	Bi_Y_3	25	25	30	25	30	25
bi_levels_vol	Bi_Y_2	25	25	25	25	25	25
bi_levels_vol	Bi_Y_1	30	25	30	30	30	30
bi_levels_vol	CLOCKE_OUT	20	20	20	20	20	20
bi_levels_vol	CLOCKF_OUT	20	25	20	20	25	20
bi_levels_vol	QA_2	20	20	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20	20	20
bi_levels_vol	QA_0	20	20	20	20	20	20

Table 9b

DUT		4095		4096		4152	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vol	Bi_IO_7	35	35	35	35	35	35
bi_levels_vol	Bi_IO_6	35	30	30	30	30	30
bi_levels_vol	Bi_IO_5	35	35	35	35	35	35
bi_levels_vol	Bi_IO_4	35	35	35	35	35	35
bi_levels_vol	Bi_IO_3	35	35	35	35	35	35
bi_levels_vol	Bi_IO_2	35	30	30	30	30	30
bi_levels_vol	Bi_IO_1	35	35	35	35	35	35
bi_levels_vol	Bi_Y_7	25	25	25	25	25	25
bi_levels_vol	Bi_Y_6	25	25	25	25	25	25
bi_levels_vol	Bi_Y_5	25	25	25	25	25	25
bi_levels_vol	Bi_Y_4	25	25	25	25	25	25
bi_levels_vol	Bi_Y_3	25	25	25	25	25	25
bi_levels_vol	Bi_Y_2	25	25	25	25	25	25
bi_levels_vol	Bi_Y_1	25	25	30	25	25	25
bi_levels_vol	CLOCKE_OUT	20	20	20	20	20	20
bi_levels_vol	CLOCKF_OUT	20	20	20	20	20	20
bi_levels_vol	QA_2	20	20	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20	20	20
bi_levels_vol	QA_0	20	125.8	20	20	20	20

Table 10a

DUT		4140		4142		4151	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_voh	Bi_IO_7	2.97	2.97	2.97	2.97	2.97	2.97
bi_levels_voh	Bi_IO_6	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_5	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_4	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_3	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_2	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_1	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_Y_7	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_6	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_5	2.985	2.98	2.98	2.98	2.985	2.98
bi_levels_voh	Bi_Y_4	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_3	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_2	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_1	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	CLOCKE_OUT	2.97	2.97	2.975	2.97	2.975	2.97
bi_levels_voh	CLOCKF_OUT	2.975	2.97	2.975	2.97	2.975	2.97
bi_levels_voh	QA_2	2.97	2.965	2.97	2.965	2.97	2.965
bi_levels_voh	QA_1	2.97	2.965	2.97	2.965	2.97	2.965
bi_levels_voh	QA_0	2.97	2.97	2.97	2.97	2.97	2.97

Table 10b

DUT		4095		4096		4152	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_voh	Bi_IO_7	2.97	2.97	2.97	2.97	2.97	2.97
bi_levels_voh	Bi_IO_6	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_5	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_4	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_3	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_2	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_1	2.965	2.965	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_Y_7	2.985	2.98	2.98	2.98	2.985	2.98
bi_levels_voh	Bi_Y_6	2.985	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_5	2.98	2.98	2.985	2.98	2.985	2.98
bi_levels_voh	Bi_Y_4	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_3	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_2	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_1	2.98	2.98	2.98	2.98	2.98	2.98
bi_levels_voh	CLOCKE_OUT	2.97	2.97	2.975	2.97	2.975	2.97
bi_levels_voh	CLOCKF_OUT	2.975	2.97	2.975	2.97	2.975	2.97
bi_levels_voh	QA_2	2.97	2.965	2.97	2.97	2.97	2.97
bi_levels_voh	QA_1	2.97	2.97	2.97	2.97	2.97	2.97
bi_levels_voh	QA_0	2.97	2.97	2.97	2.97	2.97	2.97

F. Propagation Delay

Table 11 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case the percentage change is well below $\pm 10\%$.

Table 11 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose krad(SiO ₂)	Pre-Irradiation (μ s)	Post-Annealing (μ s)	Degradation
4140	300	7.363	7.365	0.02%
4142	300	7.201	7.177	-0.33%
4151	300	7.485	7.464	-0.29%
4095	200	7.436	7.360	-1.02%
4096	200	7.190	7.116	-1.03%
4152	200	7.042	6.968	-1.06%

G. Transition Characteristic

Figures 9 to 20 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

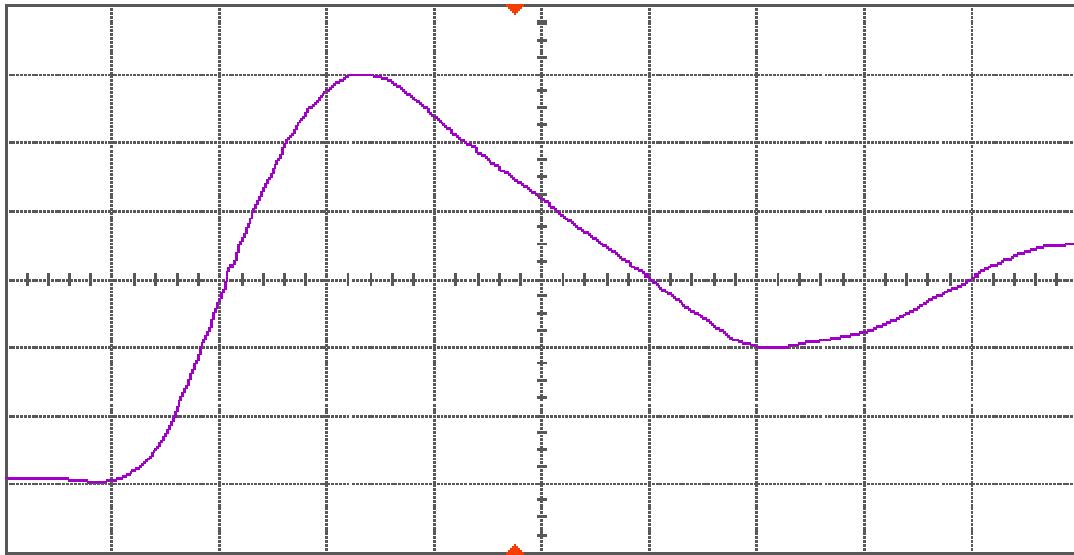


Figure 9(a) DUT 4140 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

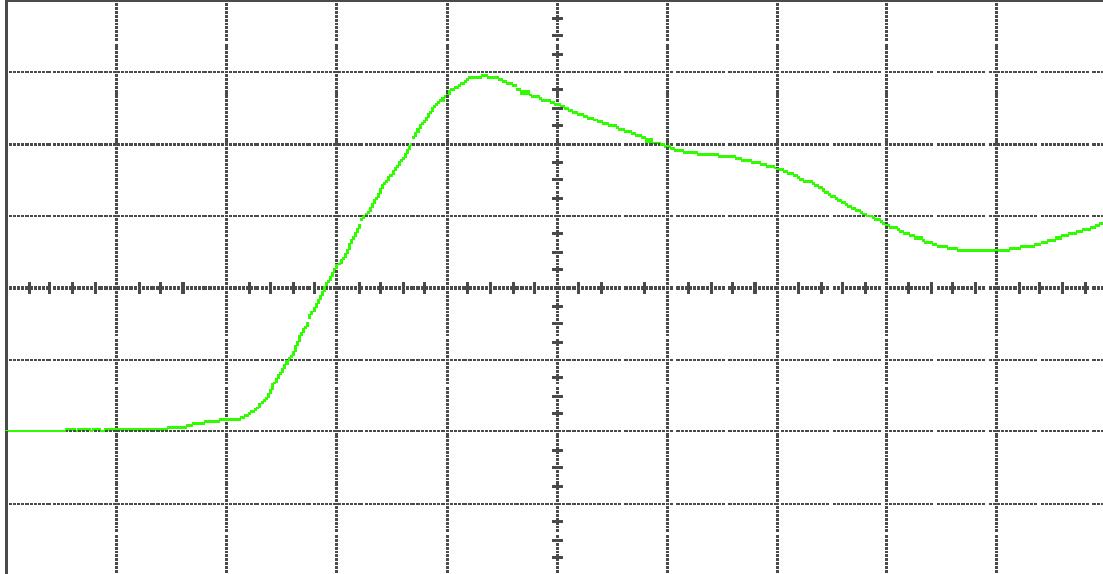


Figure 9(b) DUT 4140 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

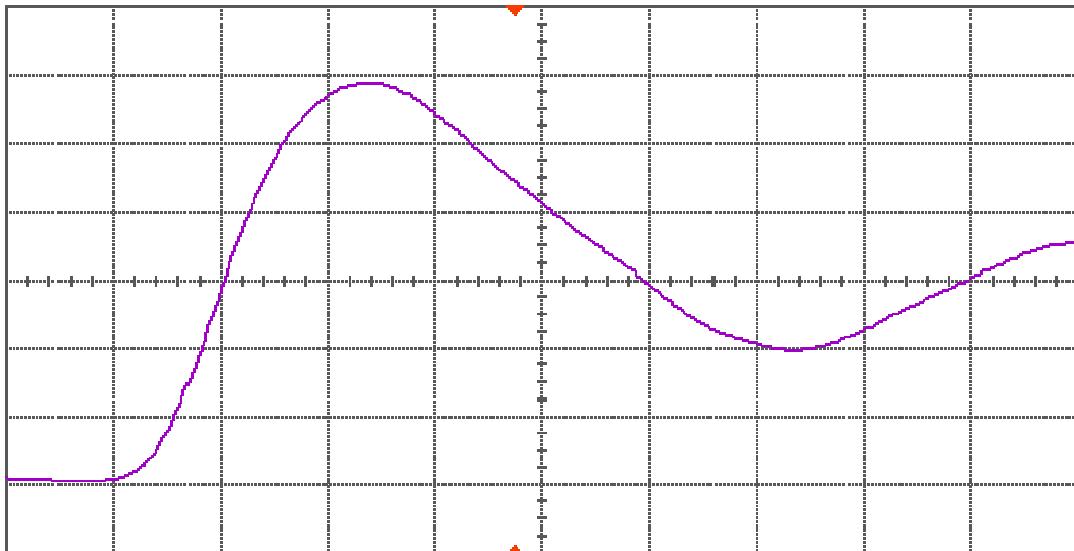


Figure 10(a) DUT 4142 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

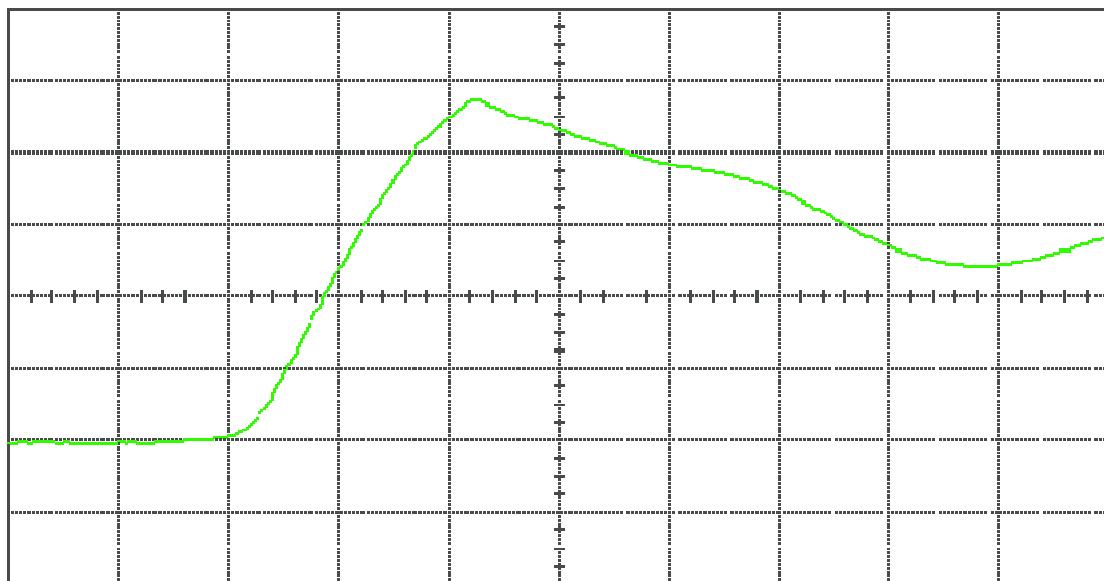


Figure 10(b) DUT 4142 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

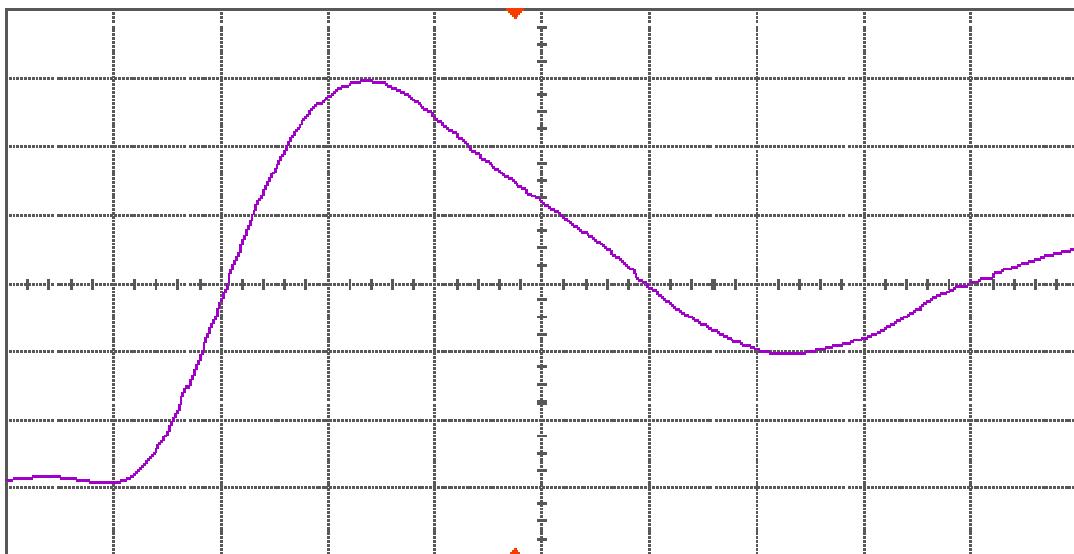


Figure 11(a) DUT 4151 pre-radiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

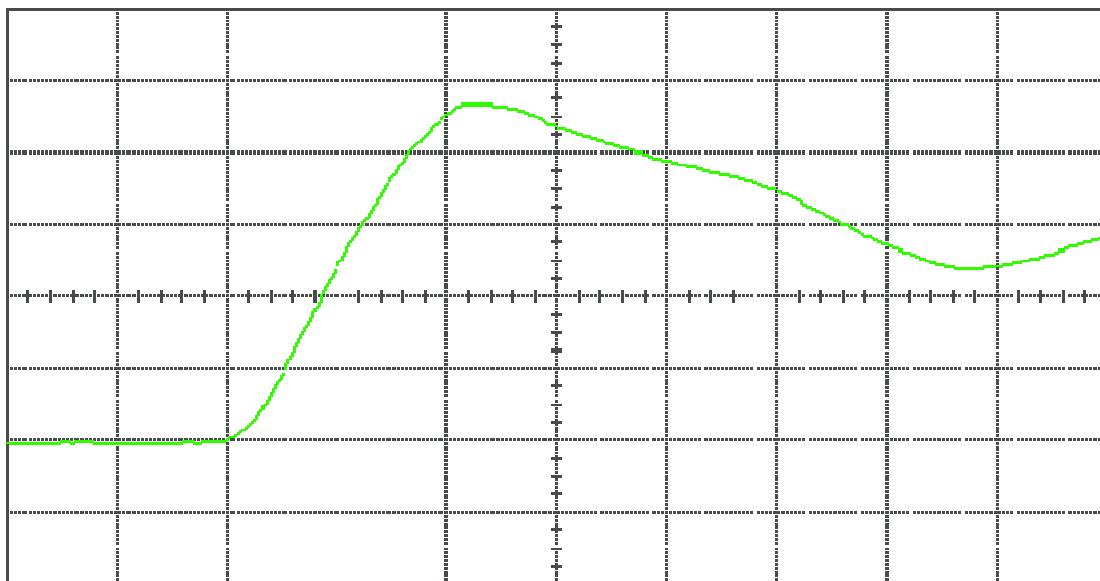


Figure 11(b) DUT 4151 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

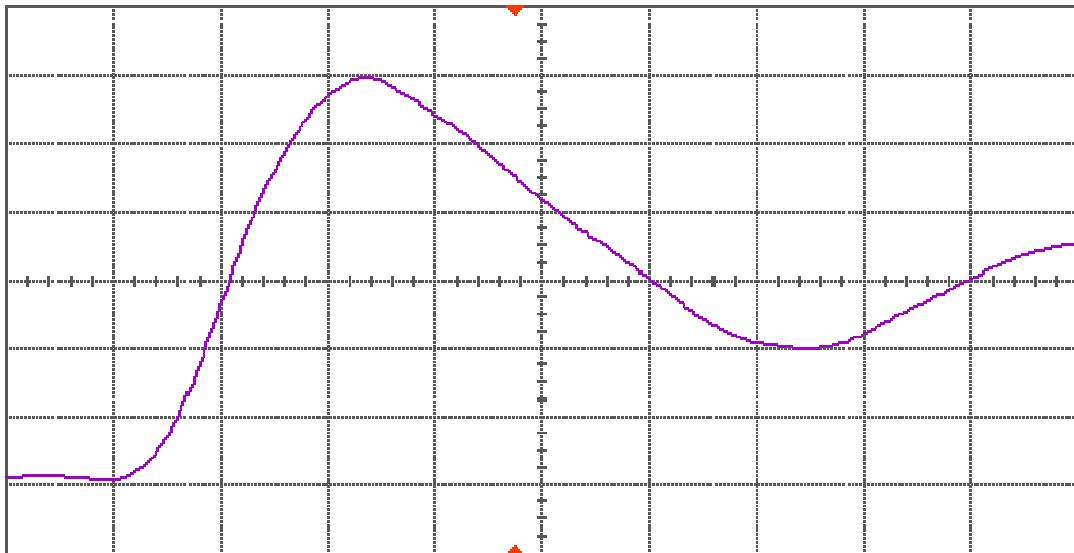


Figure 12(a) DUT 4095 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

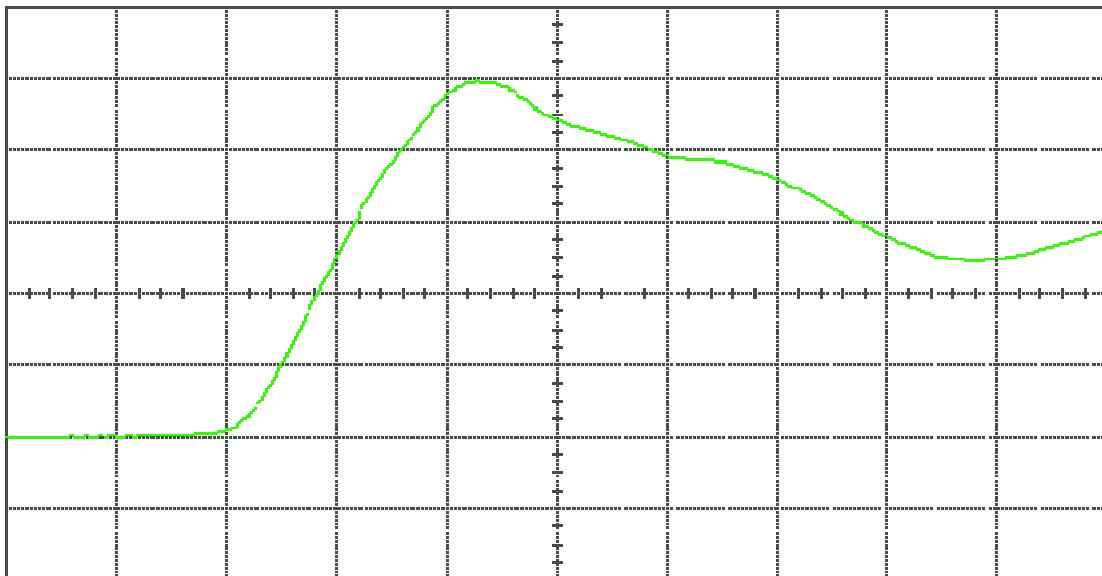


Figure 12(b) DUT 4095 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

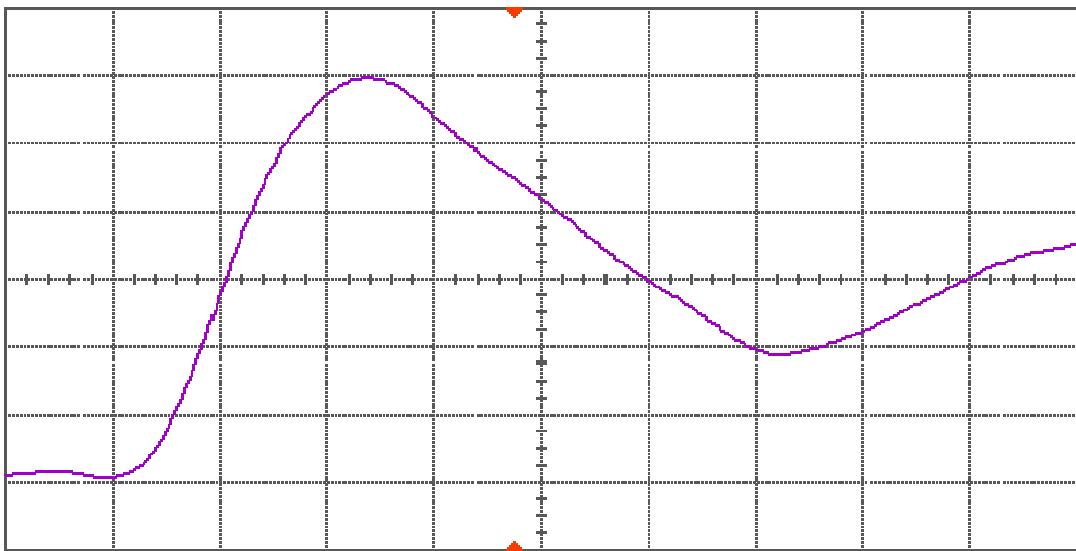


Figure 13(a) DUT 4096 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

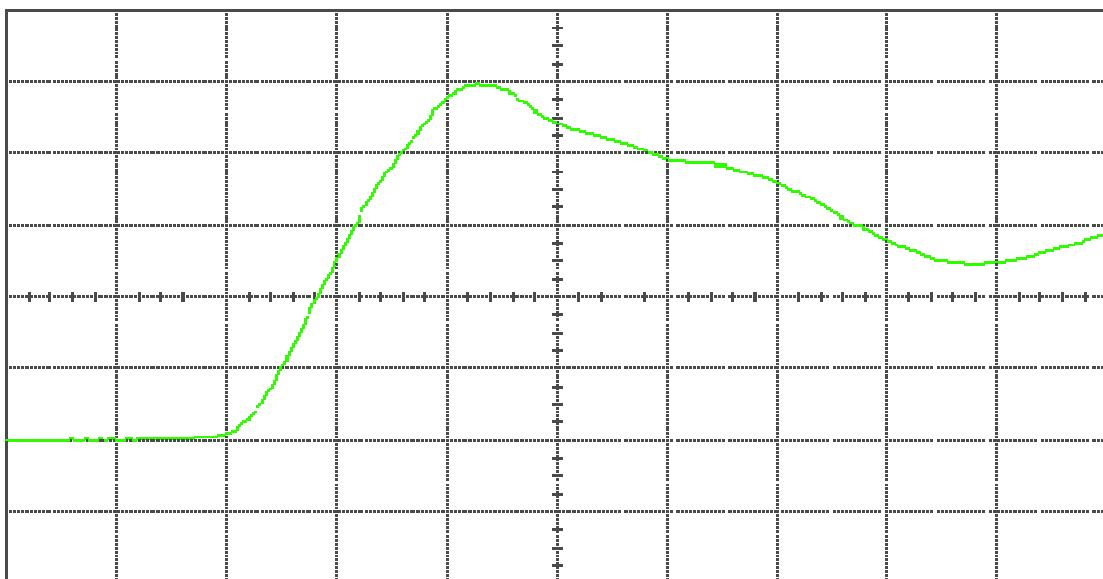


Figure 13(b) DUT 4096 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

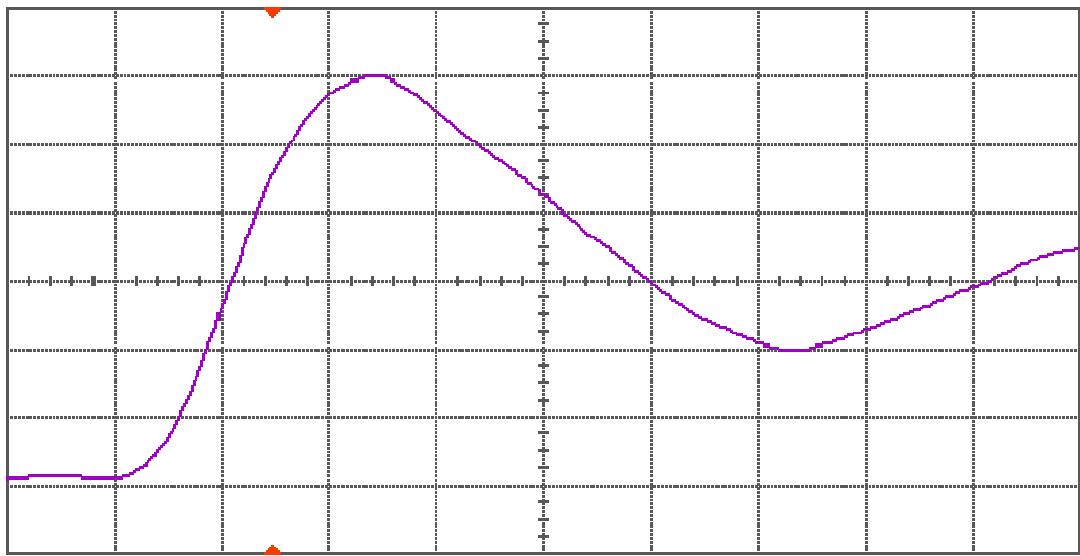


Figure 14(a) DUT 4152 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

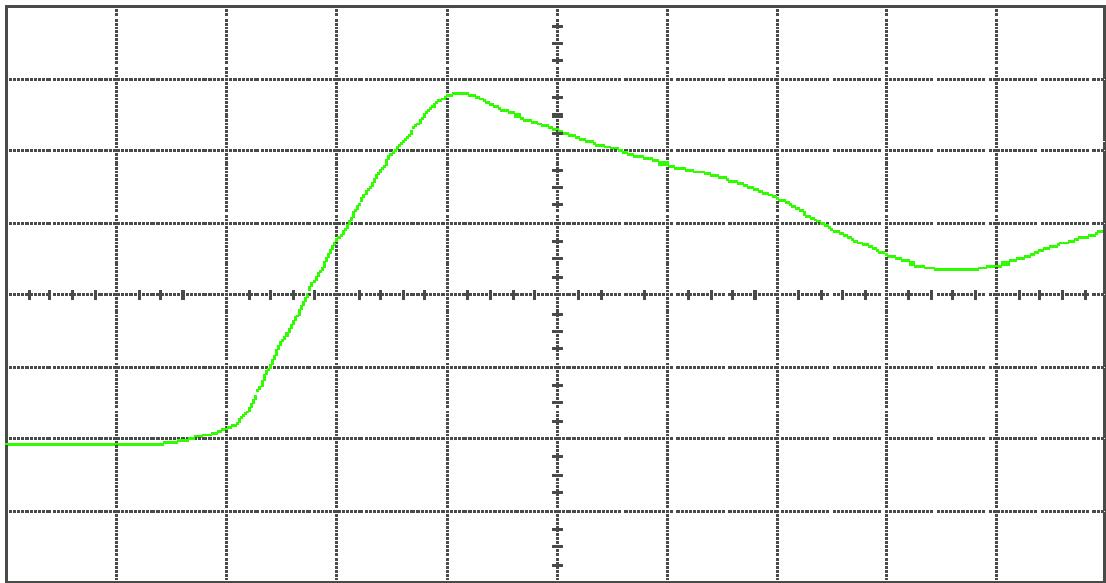


Figure 14(b) DUT 4152 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

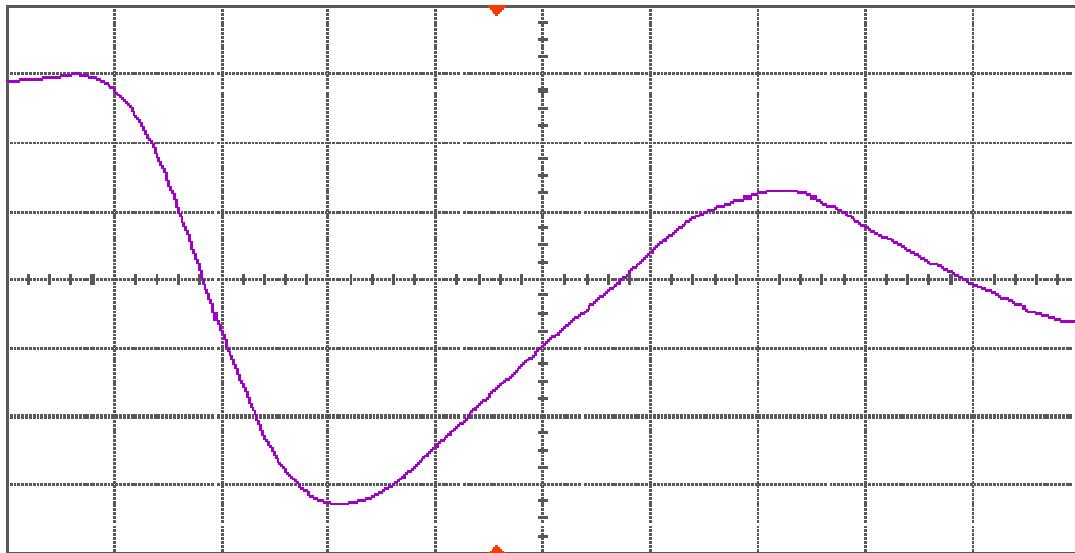


Figure 15(a) DUT 4140 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

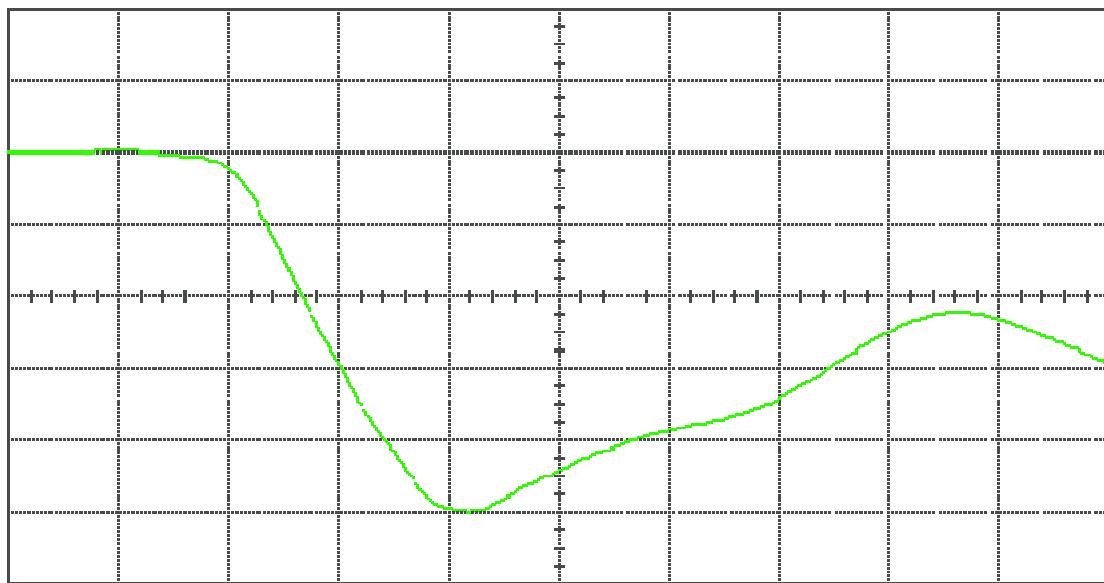


Figure 15(b) DUT 4140 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

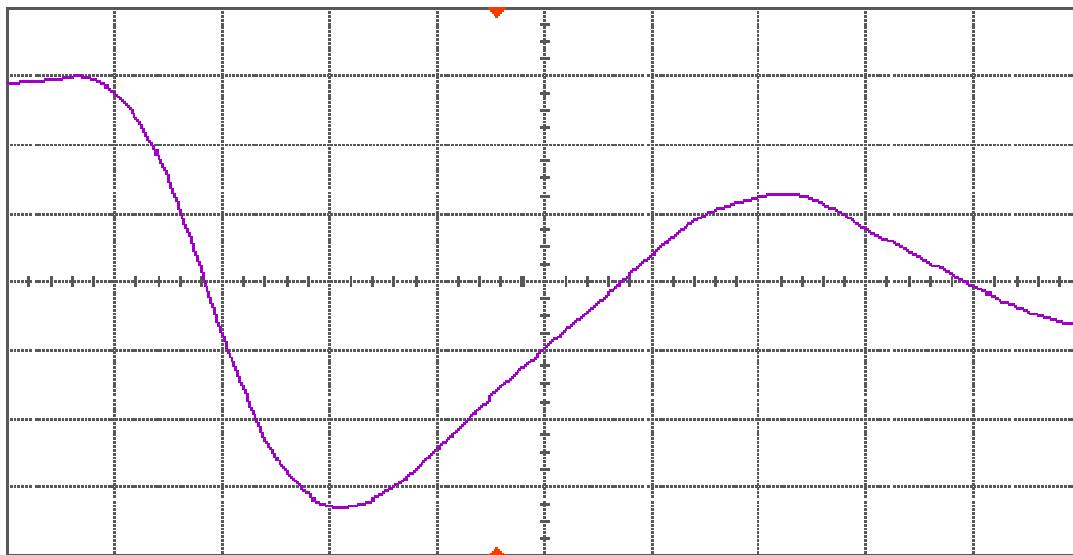


Figure 16(a) DUT 4142 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

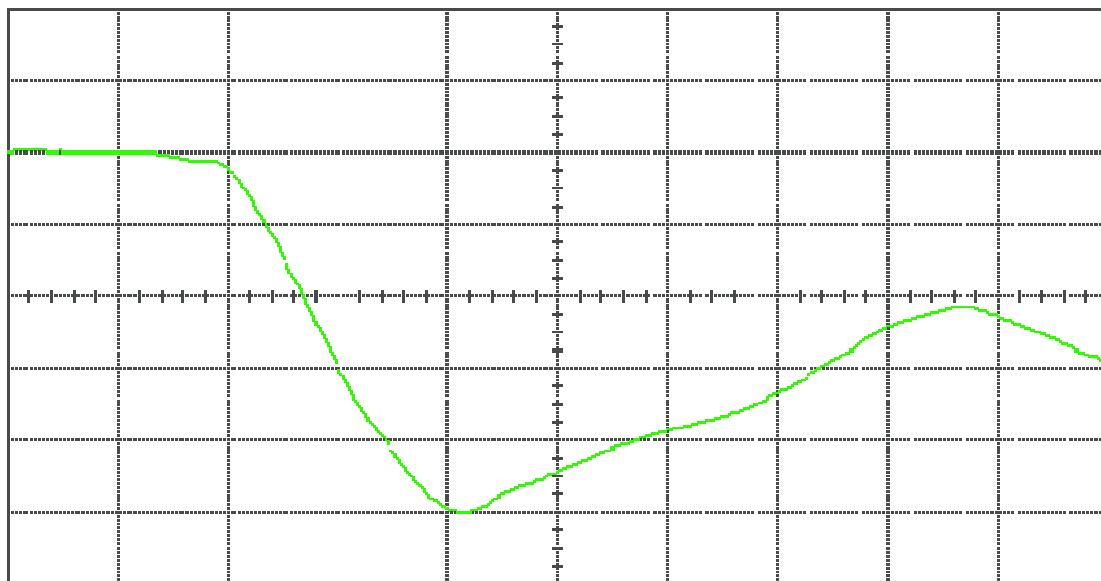


Figure 16(b) DUT 4142 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

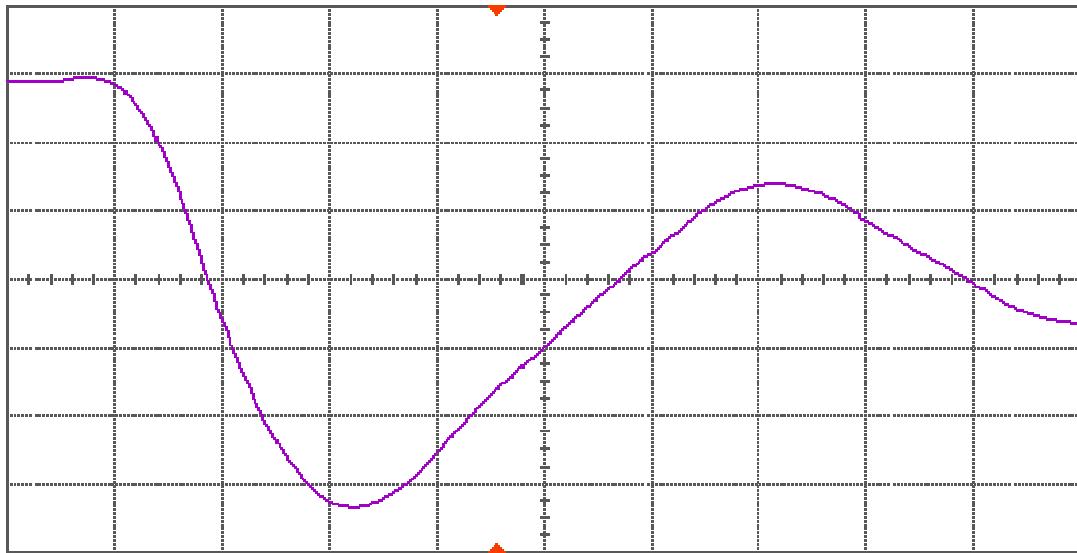


Figure 17(a) DUT 4151 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

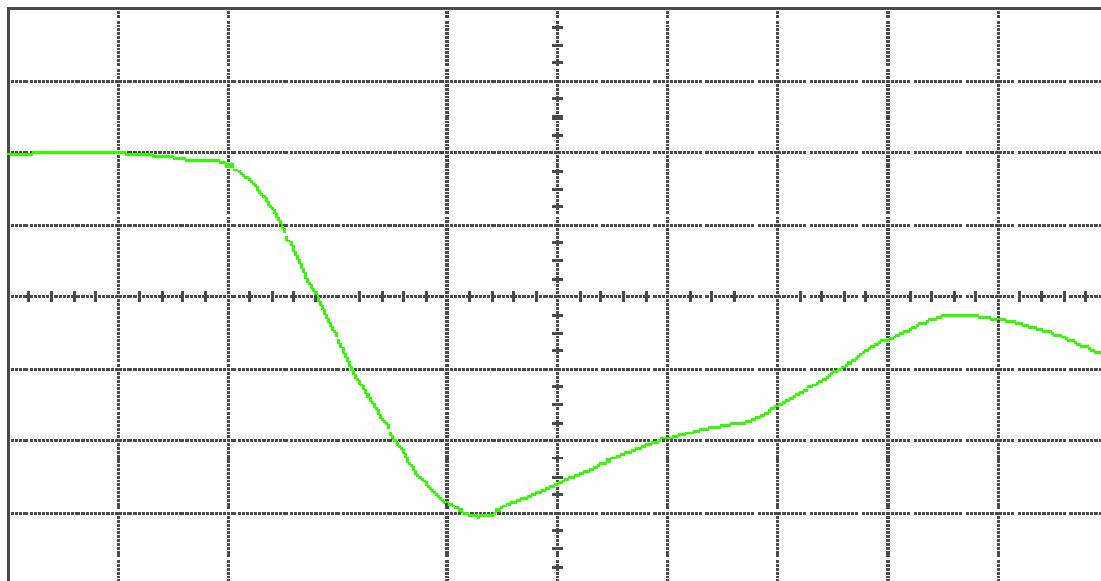


Figure 17(b) DUT 4151 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

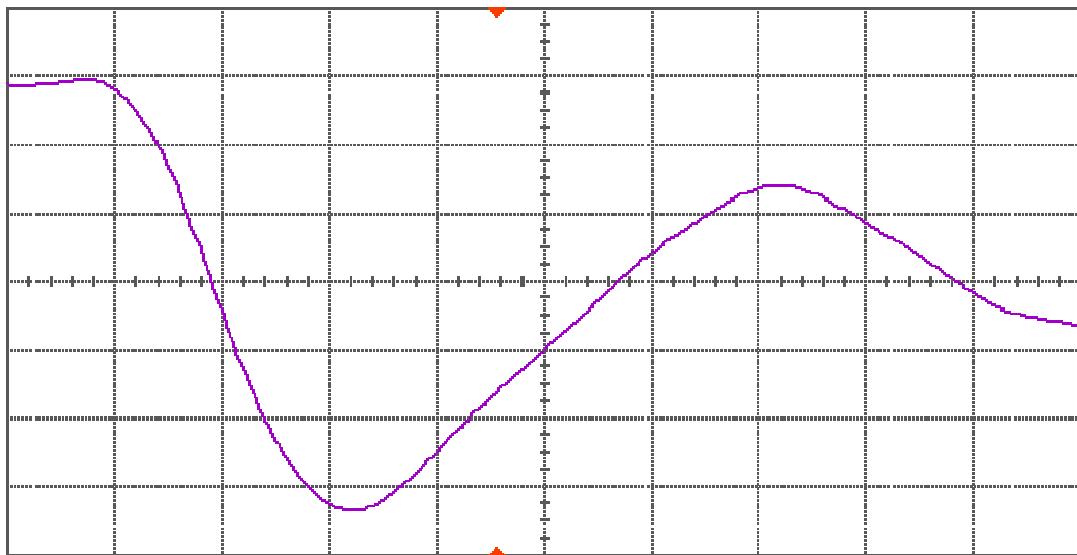


Figure 18(a) DUT 4095 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

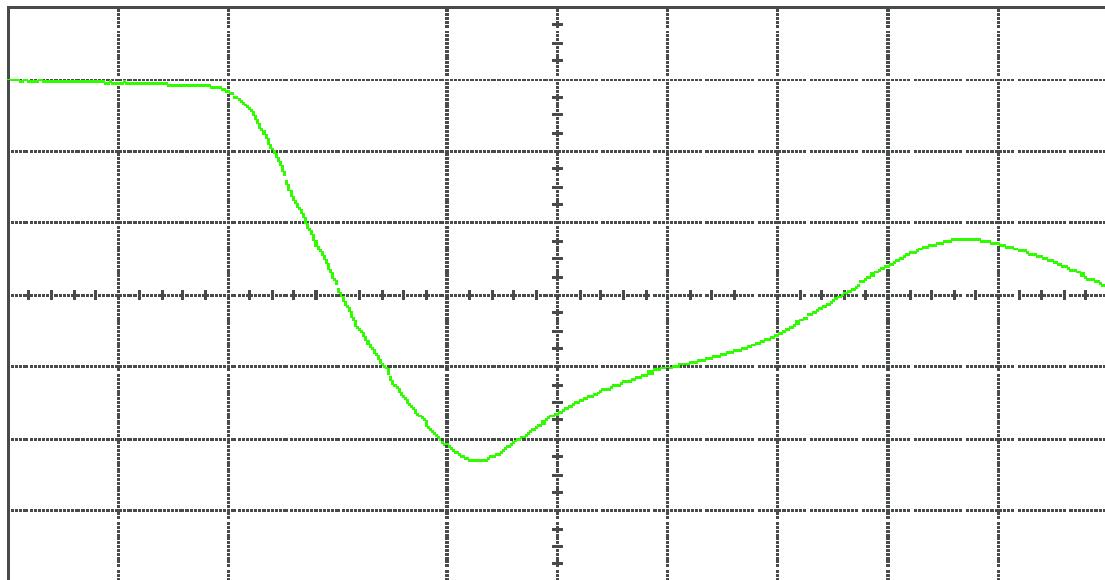


Figure 18(b) DUT 4095 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

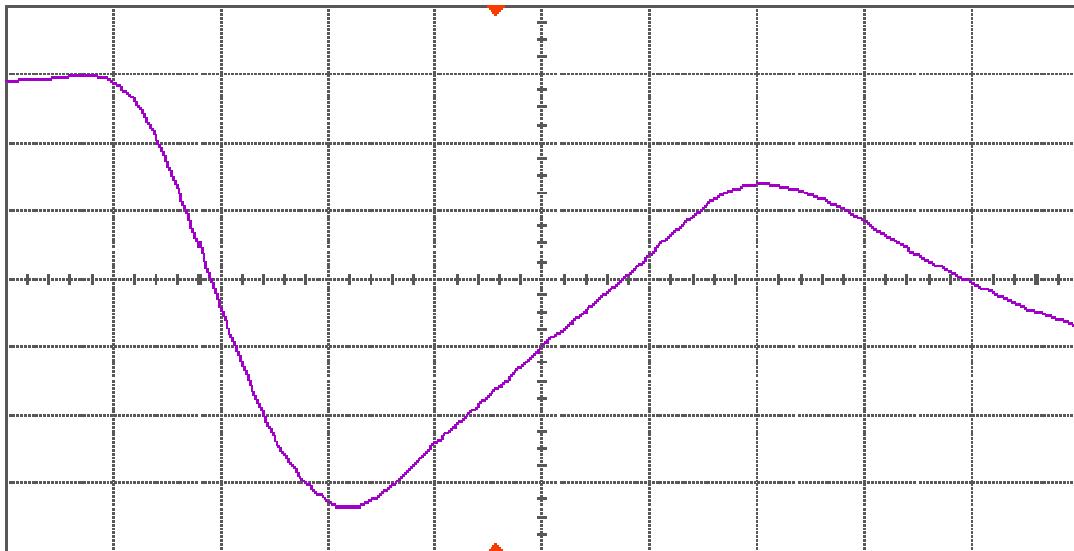


Figure 19(a) DUT 4096 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

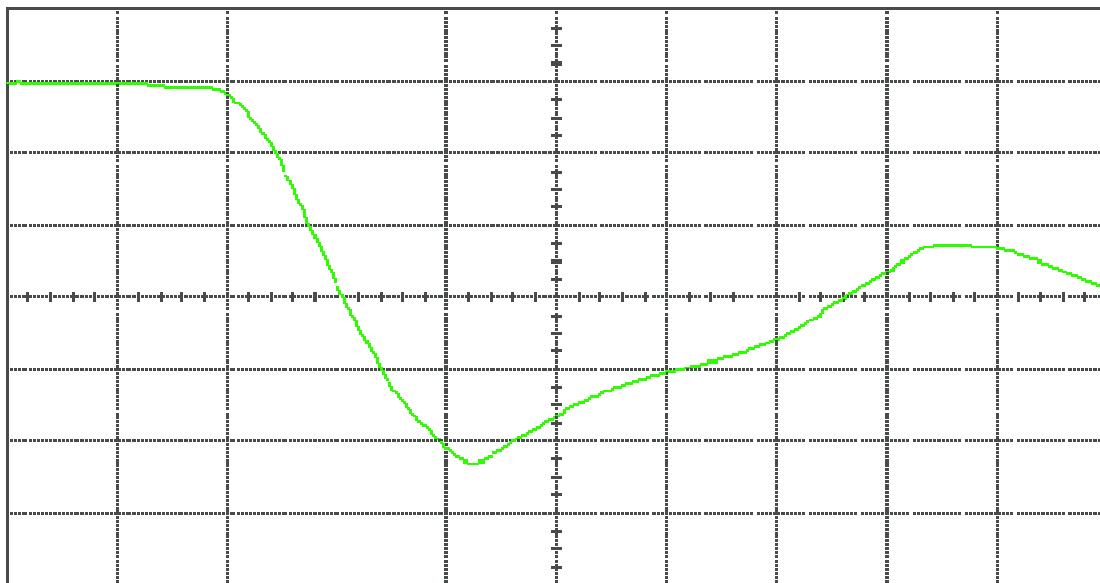


Figure 19(b) DUT 4096 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

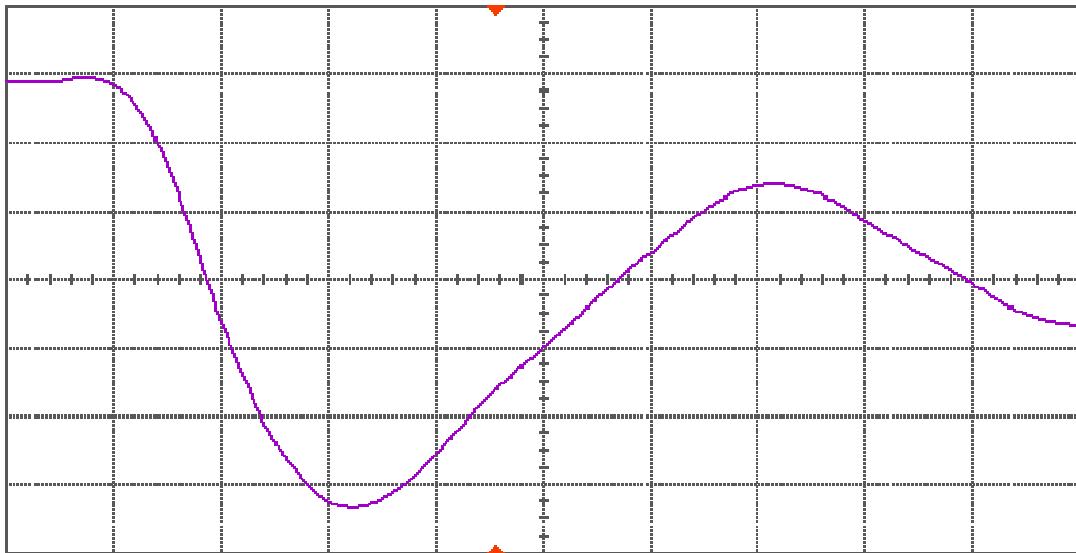


Figure 20(a) DUT 4152 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

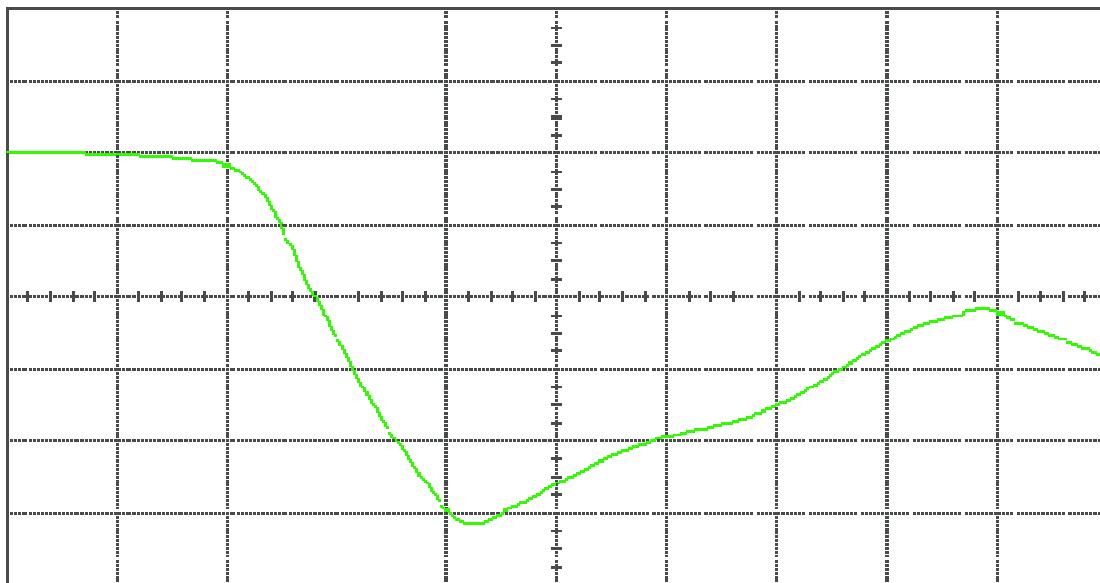


Figure 20(b) DUT 4152 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.