Actel

TOTAL IONIZING DOSE TEST REPORT

No. 05T-RTSX72SU-D1MM91
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 90 krad (Si) per 25-mA spec. Post 100 krad (Si) and after 14 days room temperature annealing: average I_{CCA} = 127.3 mA; average I_{CCI} = 54.8 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) per 10% degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to the automatic-tester measurement, the bench measurement provides lower noise, better accuracy and more flexibility. The bench measurement samples pins for some measurements. However, since the tolerance is usually determined by the most degraded parameter, which is often either I_{CC} or propagation delay, sampling the pins for measuring non-critical parameters is appropriate.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings
Die Lot Number	D1MM91
Quantity Tested	6
Serial Number	76531, 76539, 76552, 76594, 76622, 76664
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

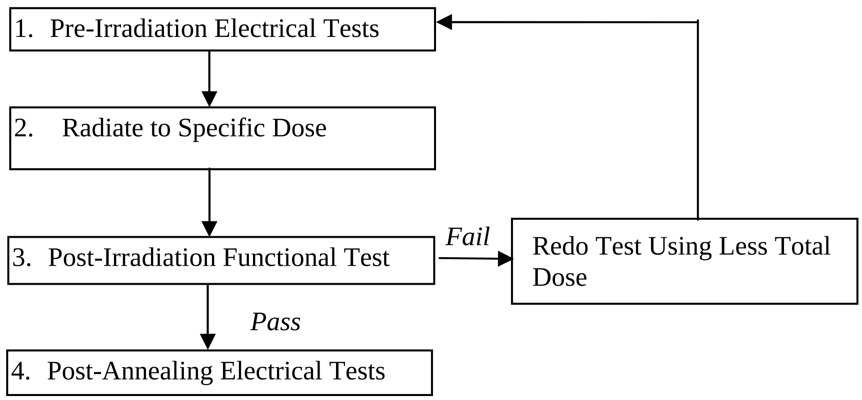


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. Both 60 krad-irradiated and 100 krad-irradiated group are annealed for approximately 14 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNTR/YO0, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. *Functionality*

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. *Power Supply Current (I_{CCA} and I_{CCI})*

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 7 basically show the radiation-induced leakage current. The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data compares with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)		I_{CCI} (mA)	
		Post-rad	Post-ann	Post-rad	Post-ann
76531	100 krad	372	149	282	77
76539	100 krad	298	178	224	66
76552	100 krad	268	124	206	56
76594	100 krad	322	152	235	66
76622	100 krad	266	22	210	4
76664	100 krad	334	139	241	60

A semi-log empirical equation is used to extrapolate the room temperature annealing for 10 years. Using the worst case, DUT 76531, the tolerance is extracted as 90 krad for 10 years mission.

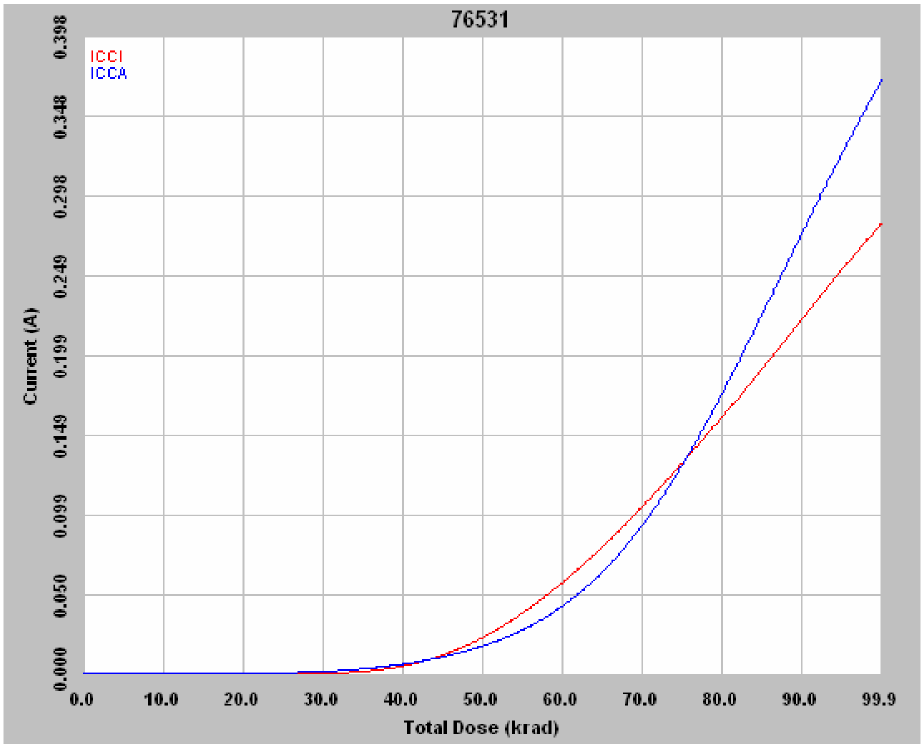


Figure 2 DUT 76531 in-flux I_{CCA} and I_{CCI}

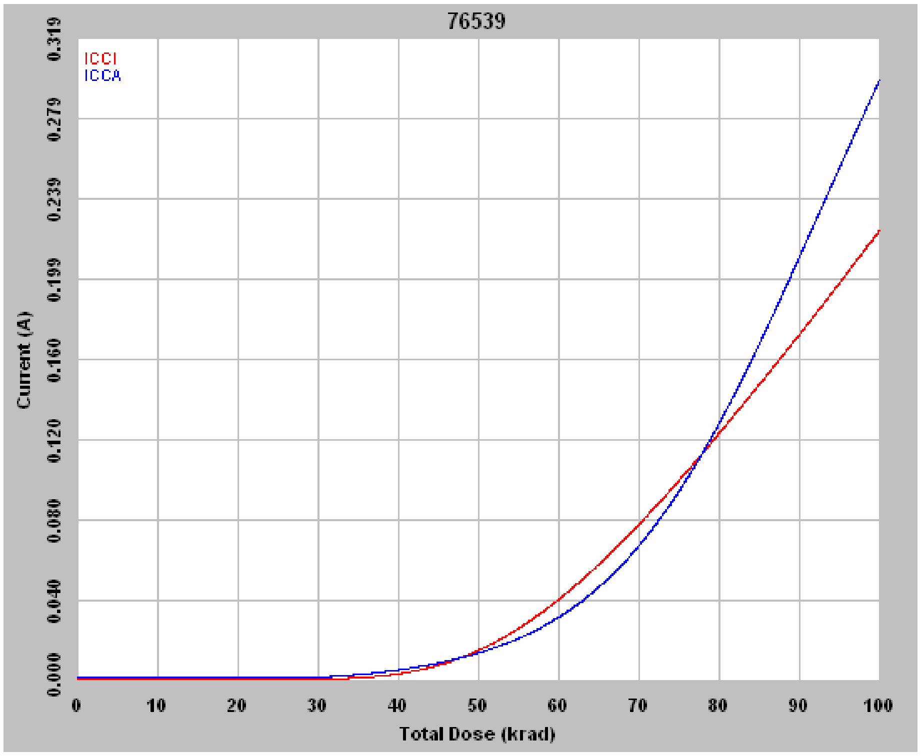


Figure 3 DUT 76539 in-flux I_{CCA} and I_{CCI}

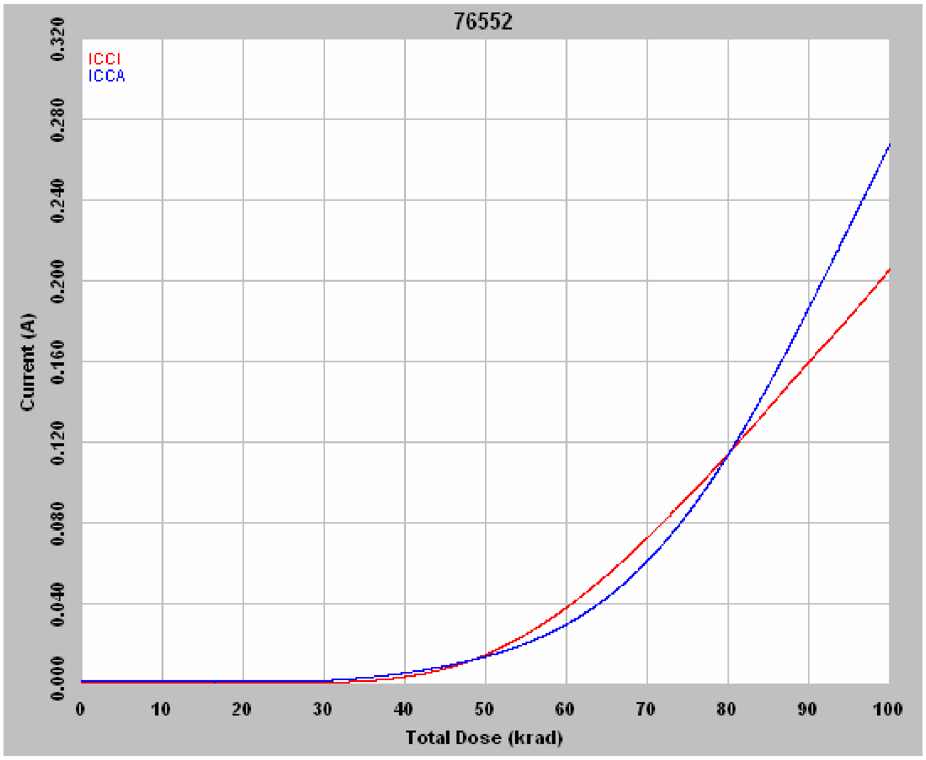


Figure 4 DUT 76552 in-flux I_{CCA} and I_{CCI}

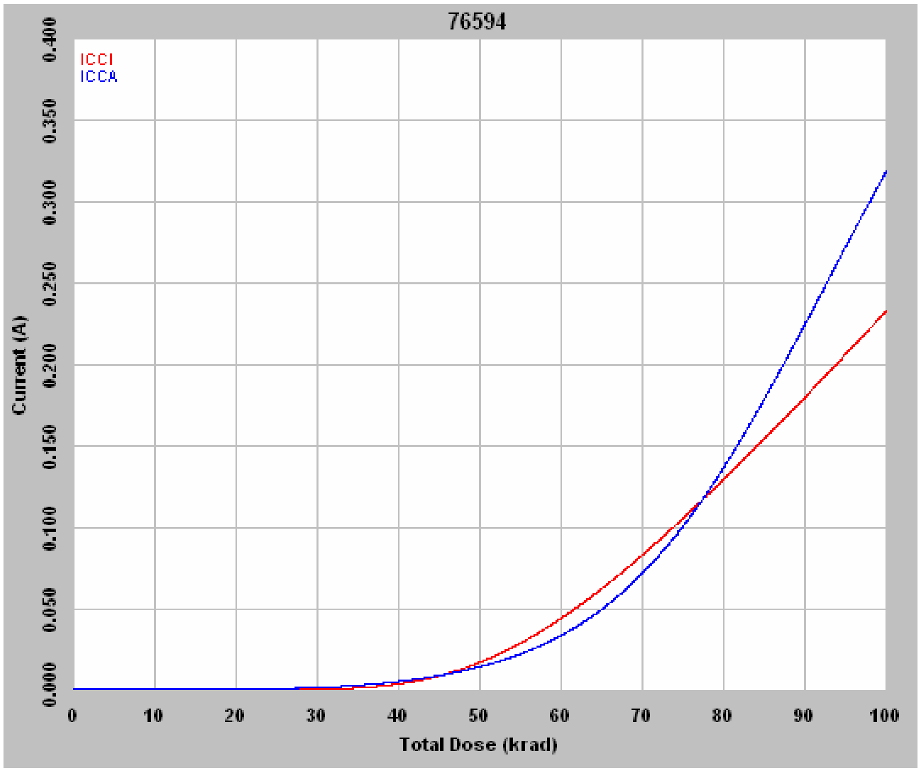


Figure 5 DUT 76594 in-flux I_{CCA} and I_{CCI}

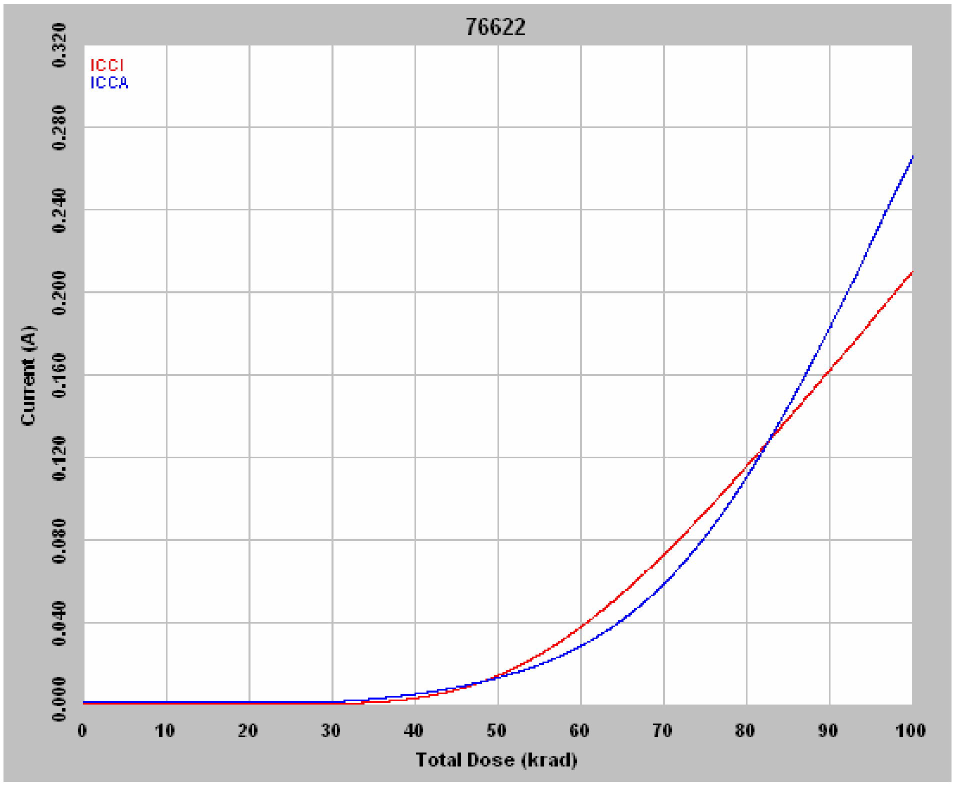


Figure 6 DUT 76622 in-flux I_{CCA} and I_{CCI}

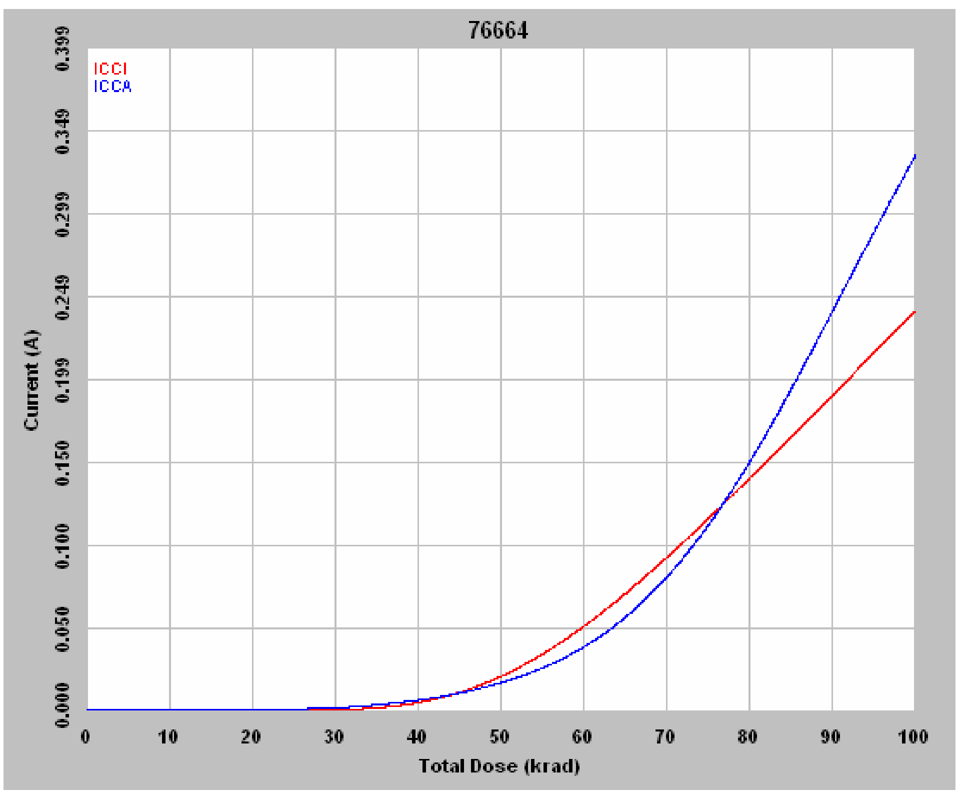


Figure 7 DUT 76664 in-flux I_{CCA} and I_{CCI}

C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		DA / QA0				DAH / QA0H			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
76531	100krad	1.37	1.37	1.54	1.45	1.41	1.39	1.41	1.44
76539	100krad	1.36	1.35	1.43	1.41	1.37	1.40	1.43	1.45
76552	100krad	1.33	1.42	1.47	1.46	1.37	1.46	1.43	1.46
76594	100krad	1.33	1.38	1.46	1.43	1.37	1.39	1.43	1.44
76622	100krad	1.34	1.36	1.46	1.42	1.34	1.41	1.41	1.44
76664	100krad	1.34	1.38	1.47	1.44	1.34	1.42	1.44	1.46

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		ENCNTR / YO0				ENCNTRH / YO3H			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
76531	100krad	1.37	1.38	1.47	1.43	1.37	1.39	1.47	1.43
76539	100krad	1.36	1.34	1.46	1.41	1.35	1.37	1.46	1.42
76552	100krad	1.37	1.42	1.47	1.47	1.35	1.38	1.47	1.45
76594	100krad	1.33	1.39	1.48	1.46	1.34	1.37	1.47	1.43
76622	100krad	1.34	1.38	1.48	1.43	1.36	1.37	1.47	1.43
76664	100krad	1.34	1.38	1.47	1.43	1.34	1.37	1.45	1.44

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII0 / IDIO0				IDII1/ IDIO1			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
76531	100krad	1.37	1.38	1.48	1.44	1.38	1.39	1.47	1.44
76539	100krad	1.37	1.36	1.47	1.42	1.39	1.37	1.46	1.41
76552	100krad	1.35	1.43	1.47	1.49	1.44	1.62	1.46	1.62
76594	100krad	1.33	1.41	1.47	1.47	1.33	1.40	1.46	1.46
76622	100krad	1.35	1.38	1.47	1.43	1.35	1.36	1.47	1.43
76664	100krad	1.35	1.38	1.45	1.44	1.34	1.33	1.46	1.43

Table 4d Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII2 / IDIO2				IDII3 / IDIO3			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
76531	100krad	1.38	1.38	1.47	1.44	1.38	1.40	1.48	1.46
76539	100krad	1.36	1.38	1.47	1.46	1.37	1.35	1.46	1.49
76552	100krad	1.36	1.42	1.46	1.48	1.36	1.40	1.46	1.46
76594	100krad	1.33	1.37	1.46	1.43	1.34	1.39	1.45	1.45
76622	100krad	1.35	1.40	1.47	1.47	1.35	1.38	1.48	1.45
76664	100krad	1.34	1.37	1.44	1.42	1.36	1.38	1.46	1.43

Table 4e Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII4 / IDIO4				IDII5 / IDIO5			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
76531	100krad	1.39	1.38	1.47	1.43	1.38	1.36	1.46	1.41
76539	100krad	1.36	1.32	1.46	1.47	1.36	1.16	1.47	1.40
76552	100krad	1.34	1.39	1.47	1.45	1.36	1.36	1.47	1.41
76594	100krad	1.33	1.38	1.47	1.45	1.33	1.37	1.46	1.42
76622	100krad	1.35	1.37	1.48	1.44	1.34	1.36	1.45	1.41
76664	100krad	1.36	1.37	1.46	1.44	1.34	1.35	1.46	1.41

Table 4f Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII6 / IDIO6				IDII7 / IDIO7			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
76531	100krad	1.39	1.33	1.44	1.40	1.37	1.35	1.47	1.44
76539	100krad	1.36	1.30	1.41	1.33	1.36	1.39	1.45	1.45
76552	100krad	1.34	1.35	1.47	1.42	1.35	1.41	1.47	1.47
76594	100krad	1.52	1.49	1.54	1.50	1.34	1.37	1.45	1.42
76622	100krad	1.34	1.37	1.43	1.41	1.36	1.39	1.48	1.43
76664	100krad	1.34	1.35	1.40	1.40	1.33	1.48	1.46	1.48

D. *Output-Drive Voltage (V_{OL}/V_{OH})*

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
76531	100krad	0.009	0.009	0.102	0.107	0.171	0.178	0.432	0.450	0.888	0.927
76539	100krad	0.009	0.010	0.104	0.110	0.173	0.184	0.438	0.464	0.900	0.957
76552	100krad	0.009	0.009	0.104	0.108	0.174	0.180	0.439	0.453	0.904	0.934
76594	100krad	0.009	0.009	0.102	0.105	0.171	0.176	0.430	0.443	0.885	0.914
76622	100krad	0.009	0.010	0.105	0.114	0.175	0.191	0.441	0.481	0.906	0.991
76664	100krad	0.009	0.009	0.104	0.106	0.173	0.177	0.436	0.447	0.898	0.921

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
76531	100krad	4.98	4.98	4.86	4.85	4.64	4.63	4.06	4.00	2.71	2.49
76539	100krad	4.98	4.98	4.86	4.85	4.64	4.62	4.05	4.00	2.70	2.57
76552	100krad	4.98	4.98	4.86	4.85	4.64	4.61	4.05	3.96	2.69	2.37
76594	100krad	4.98	4.98	4.86	4.86	4.64	4.63	4.05	4.01	2.68	2.52
76622	100krad	4.98	4.98	4.86	4.86	4.64	4.65	4.06	4.08	2.74	2.89
76664	100krad	4.98	4.98	4.86	4.86	4.64	4.63	4.04	4.01	2.65	2.51

E. *Propagation Delay*

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. In the 100-krad group, DUT 76531 has the worst degradation of 4.81%.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation (µs)	Post-Annealing (µs)	Degradation
76531	100krad	1.171	1.228	4.81%
76539	100krad	1.170	1.221	4.30%
76552	100krad	1.173	1.216	3.65%
76594	100krad	1.164	1.215	4.39%
76622	100krad	1.173	1.186	1.14%
76664	100krad	1.173	1.220	4.01%

F. Transition Time

Figures 8 to 19 show the pre-irradiation and post-annealing transition edges. In each case, the radiation effect is not significant.

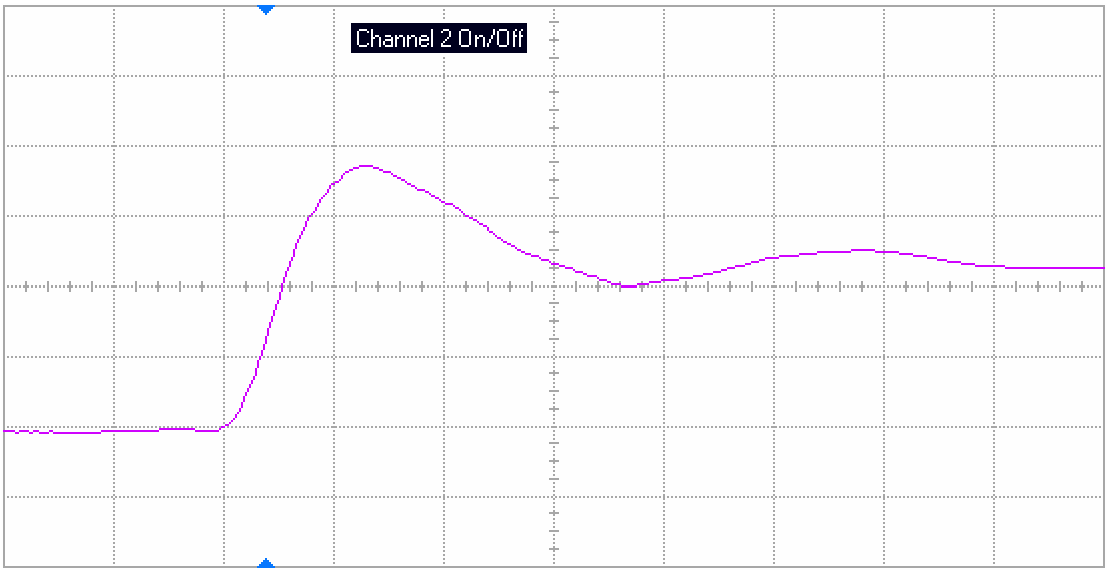


Figure 8(a) DUT 76531 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

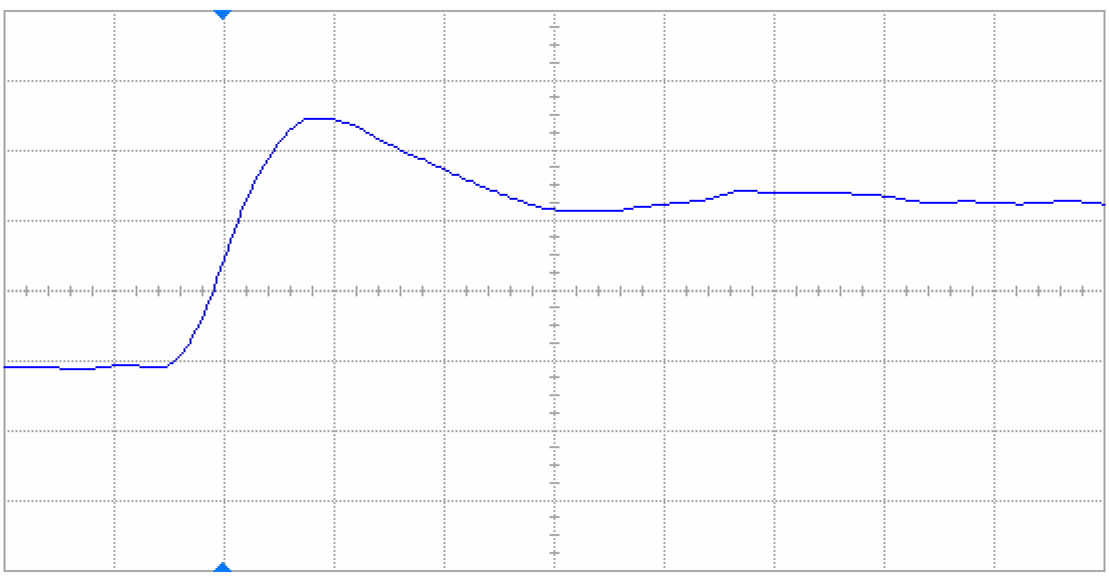


Figure 8(b) DUT 76531 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

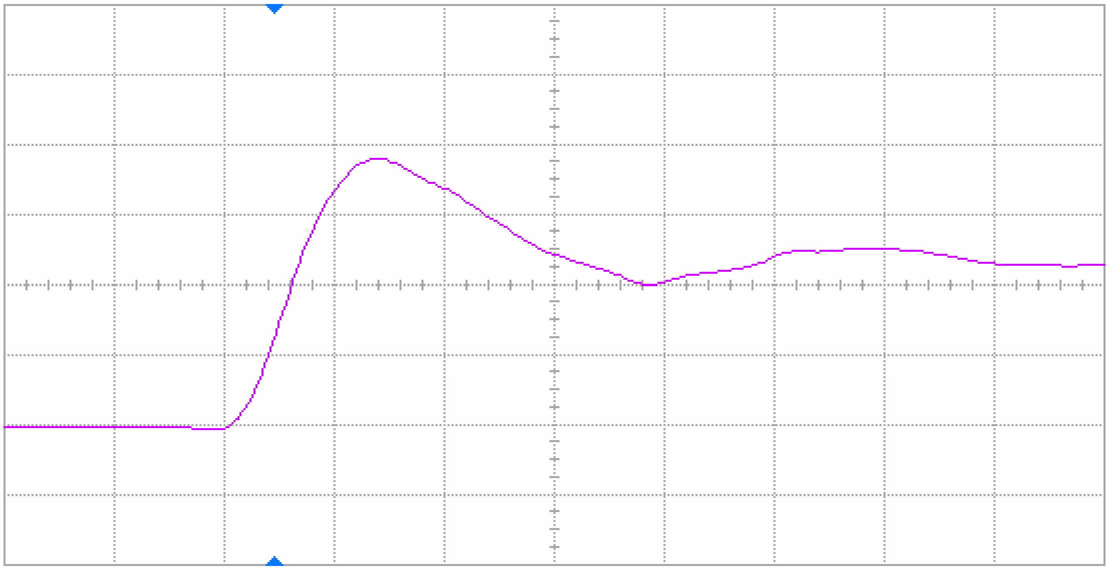


Figure 9(a) DUT 76539 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

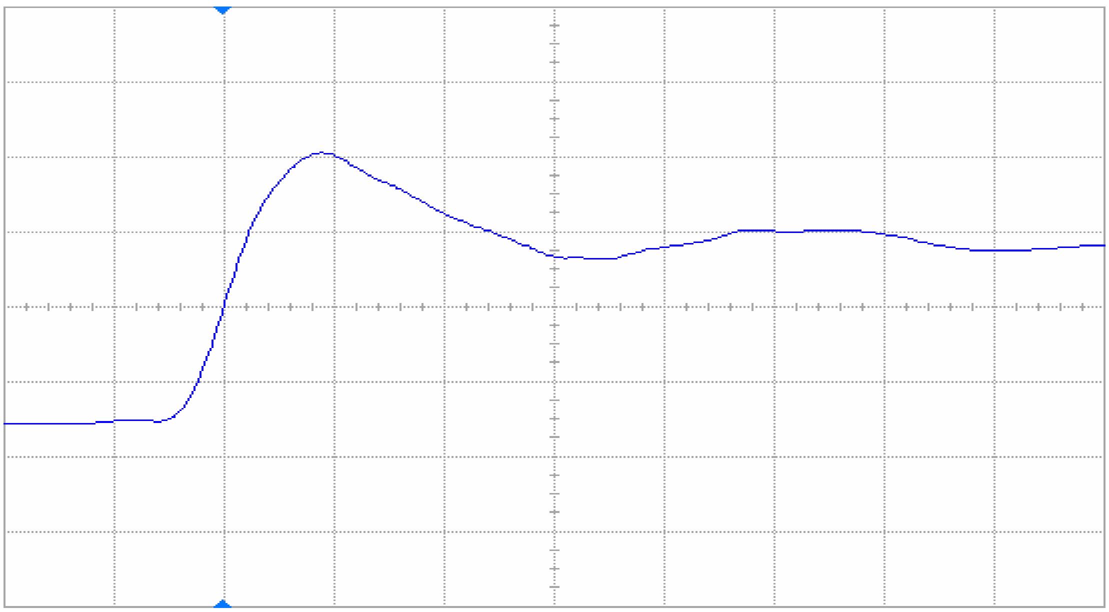


Figure 9(b) DUT 76539 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

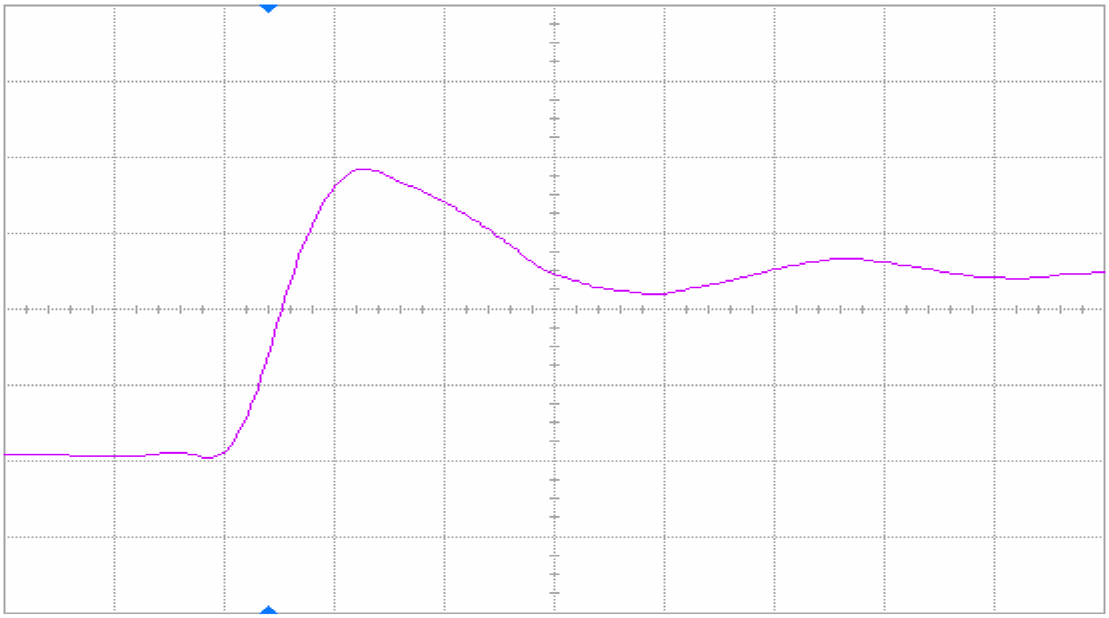


Figure 10(a) DUT 76552 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

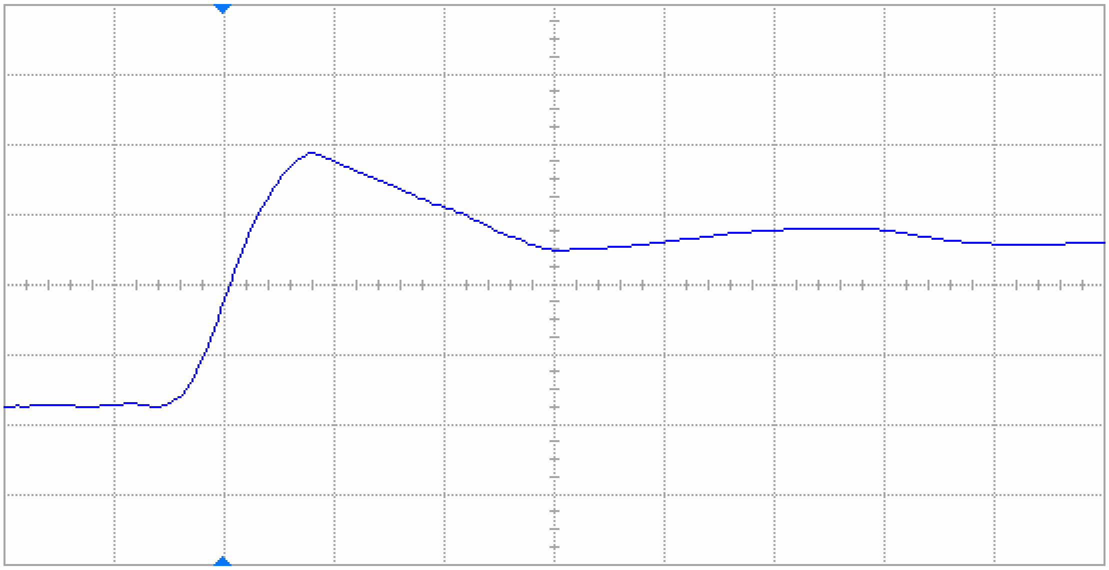


Figure 10(b) DUT 76552 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

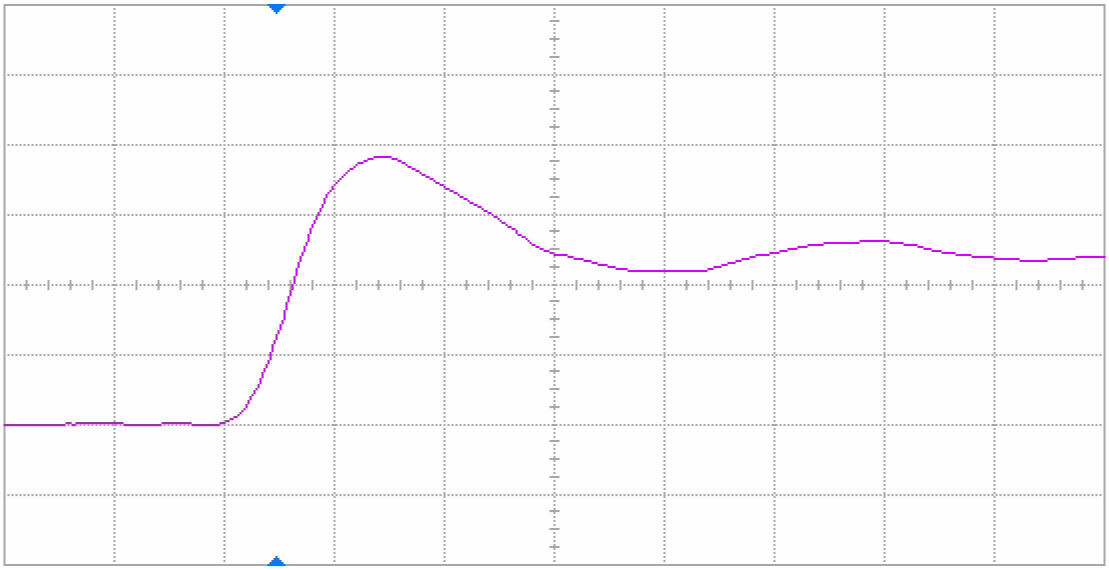


Figure 11(a) DUT 76594 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

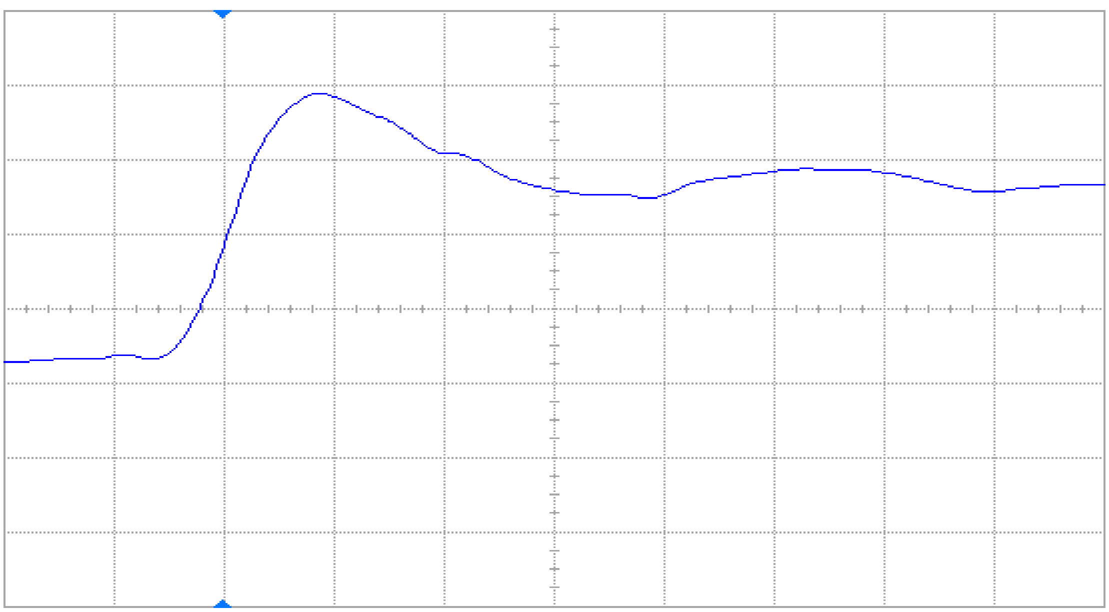


Figure 11(b) DUT 76594 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

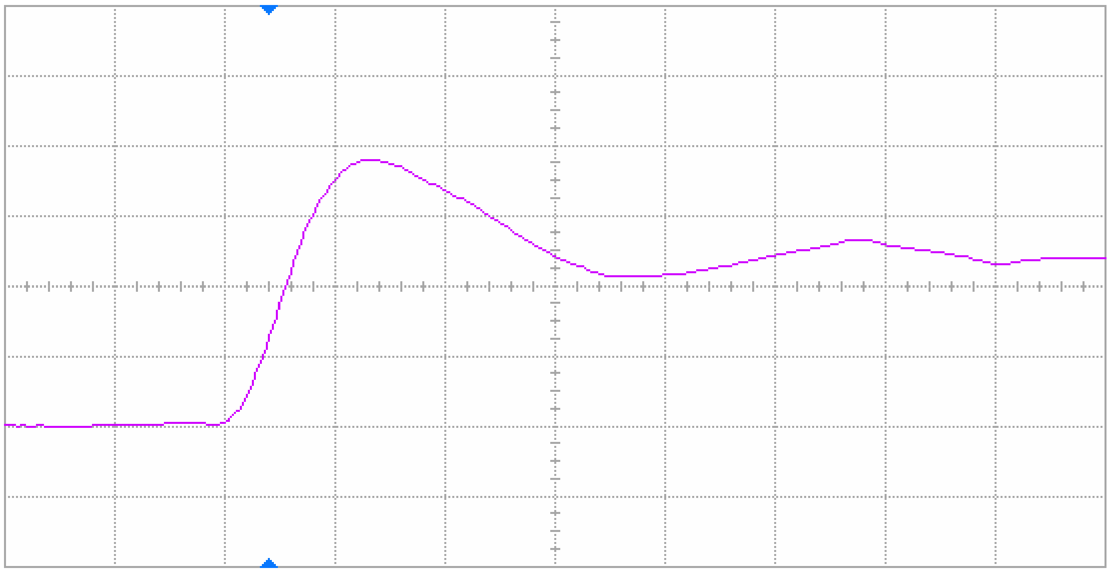


Figure 12(a) DUT 76622 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

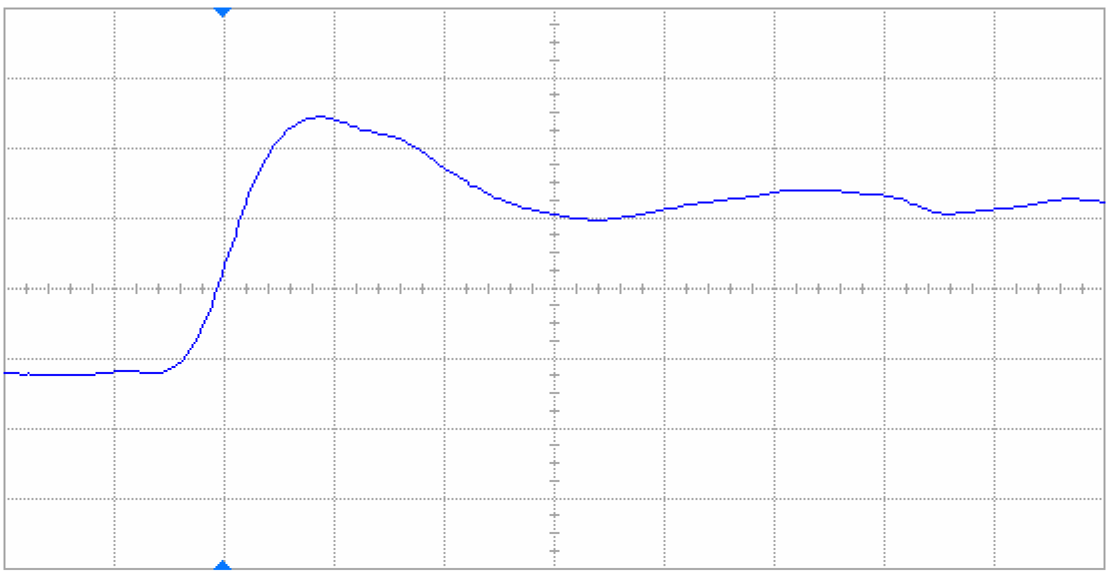


Figure 12(b) DUT 76622 post-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

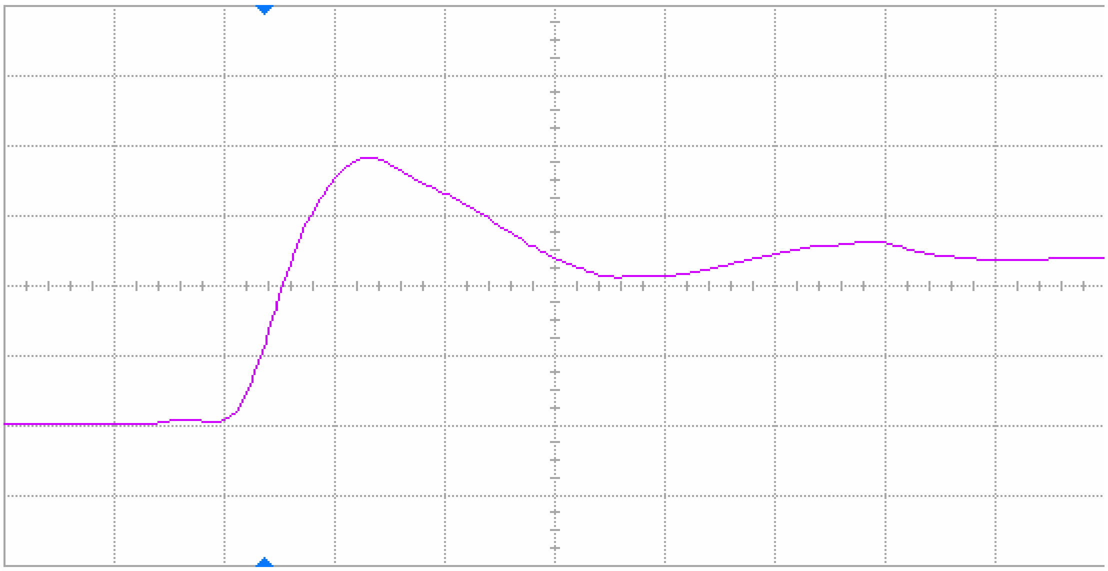


Figure 13(a) DUT 76664 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

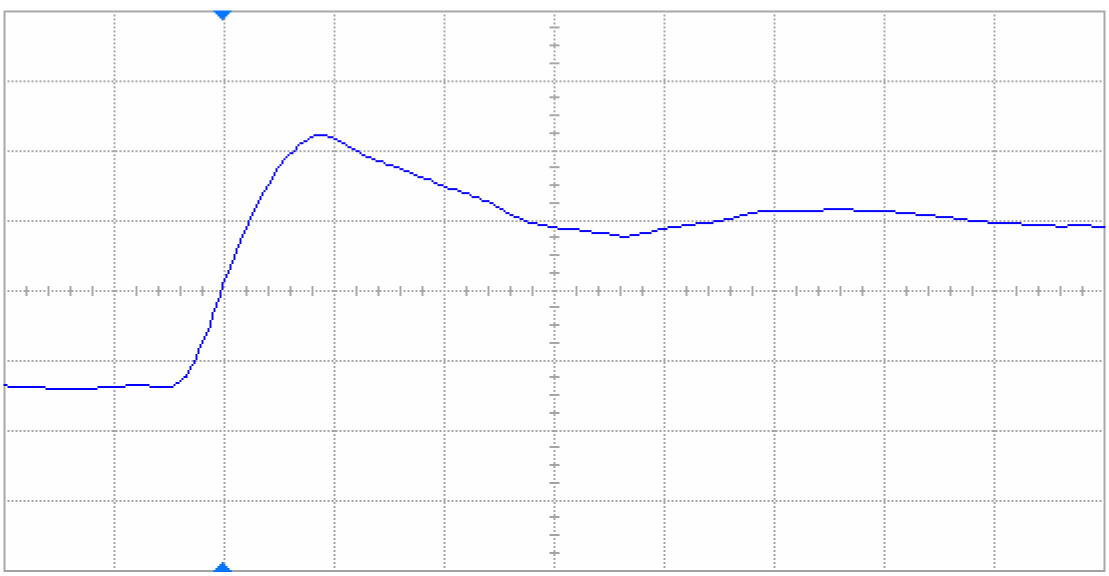


Figure 13(b) DUT 76664 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

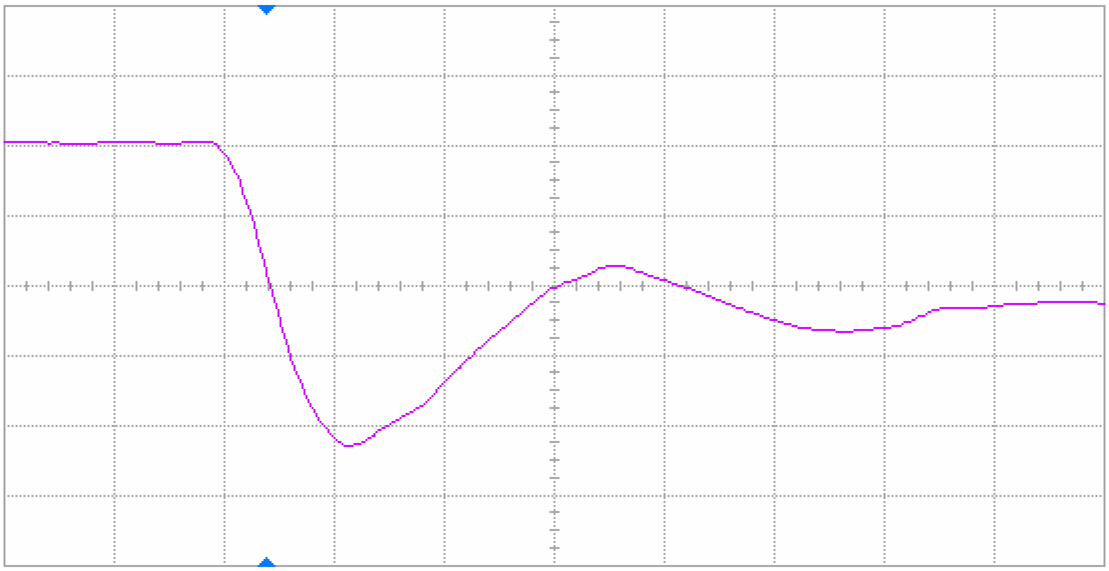


Figure 14(a) DUT 76531 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

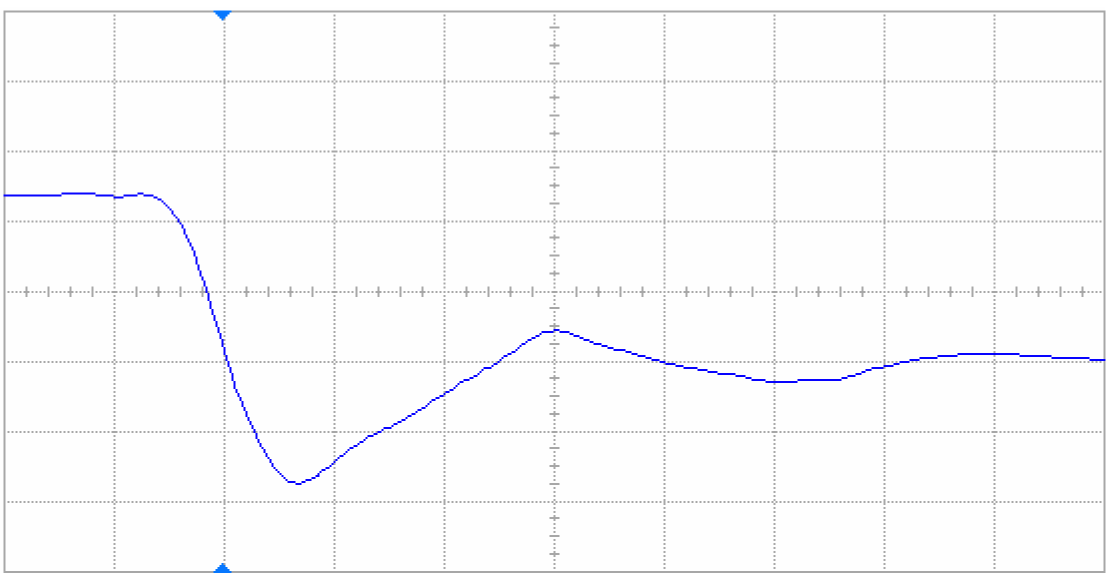


Figure 14(b) DUT 76531 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

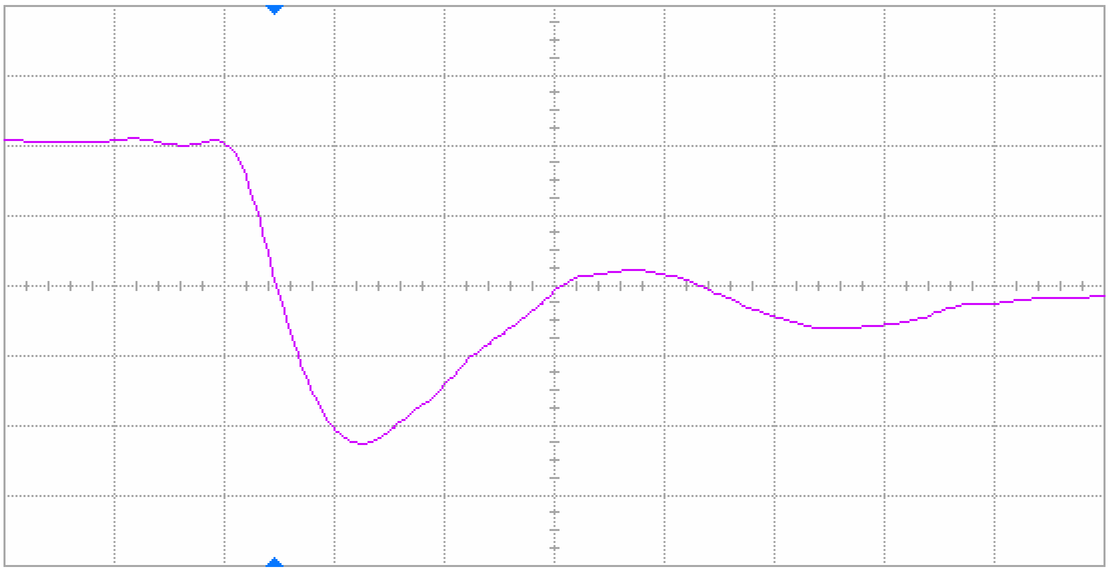


Figure 15(a) DUT 76539 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

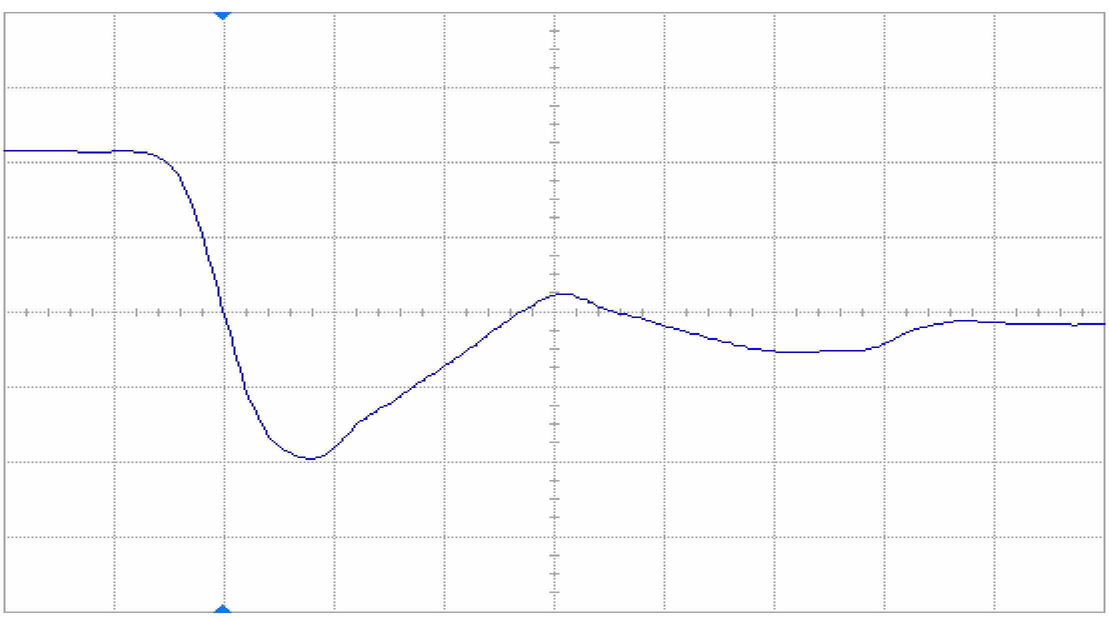


Figure 15(b) DUT 76539 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

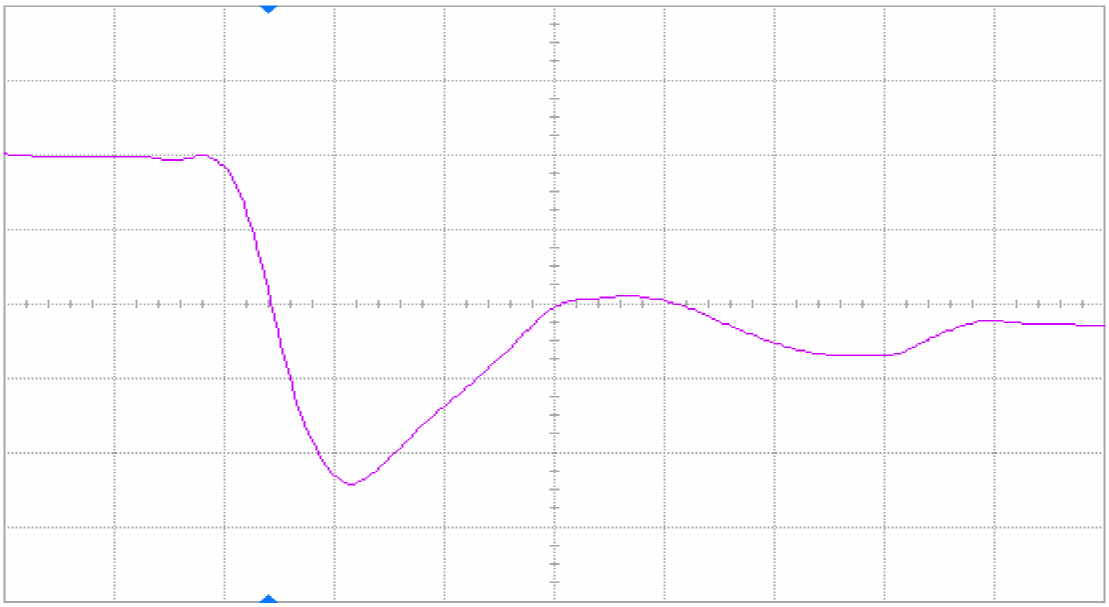


Figure 16(a) DUT 76552 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

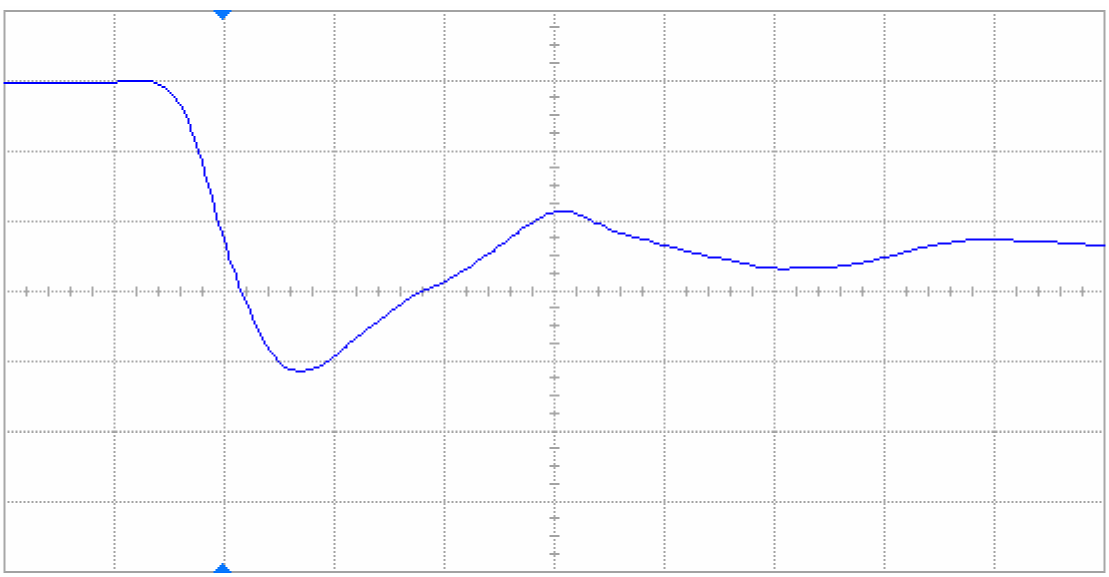


Figure 16(b) DUT 76552 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

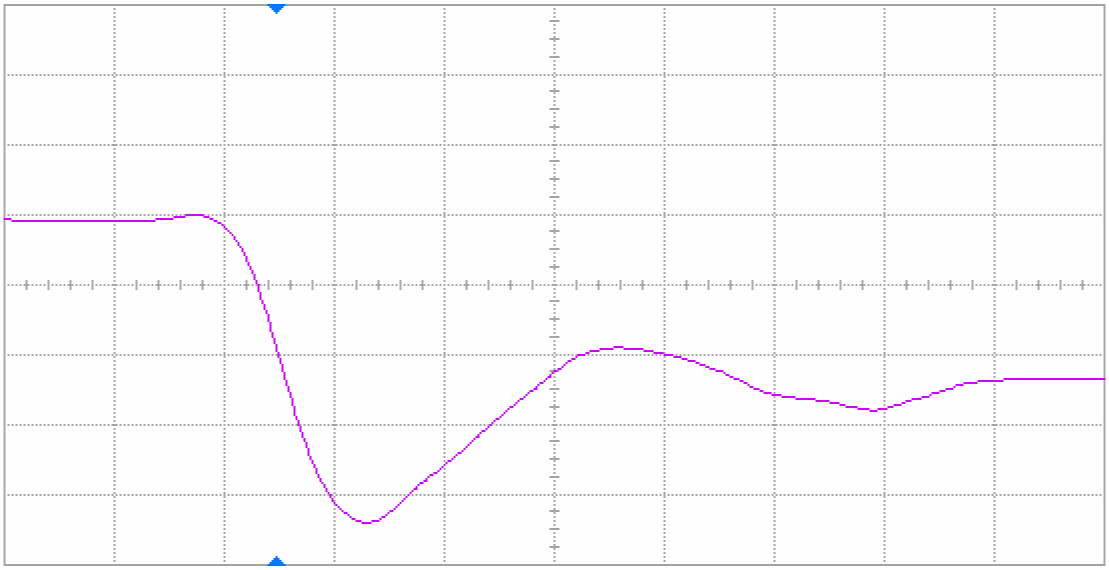


Figure 17(a) DUT 76594 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

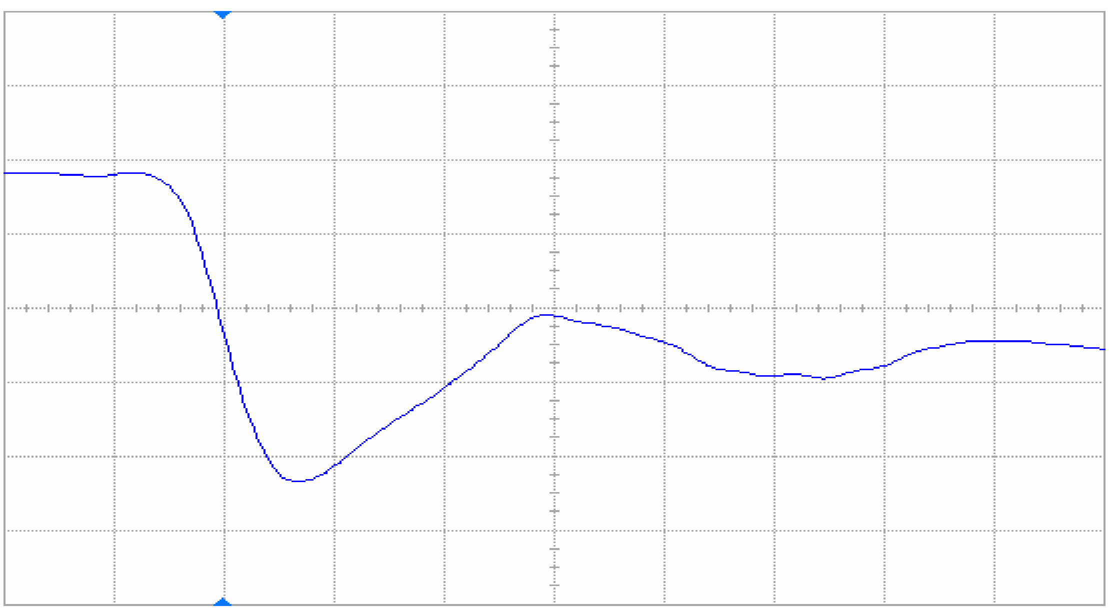


Figure 17(b) DUT 76594 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

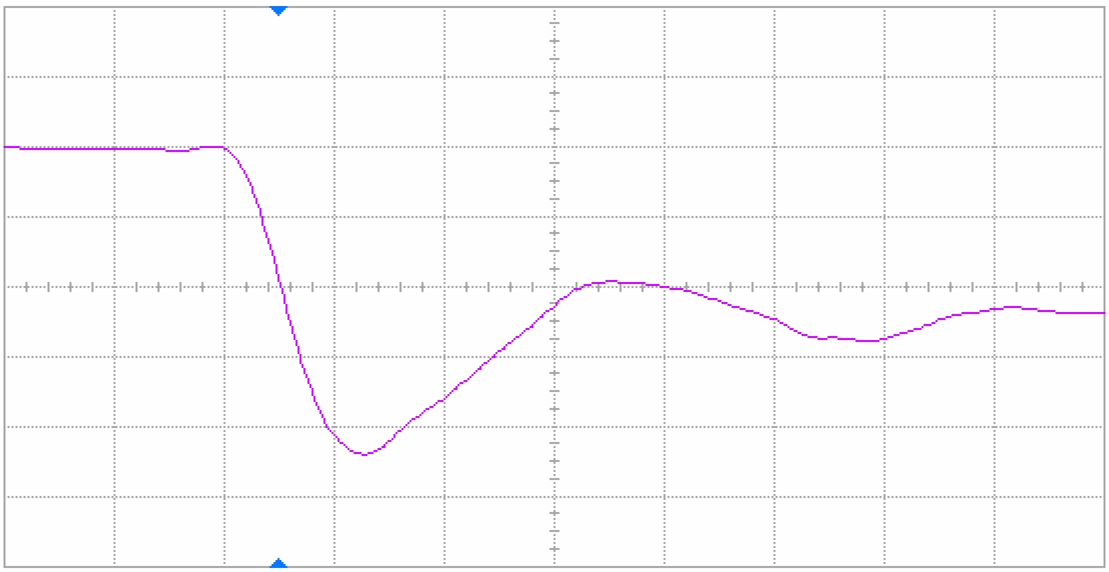


Figure 18(a) DUT 76622 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

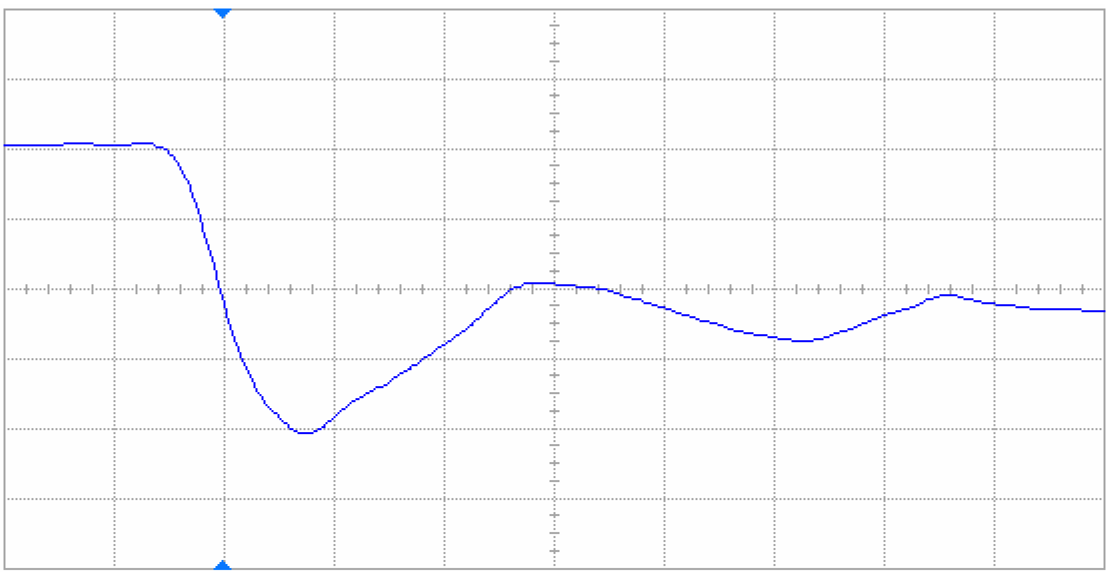


Figure 18(b) DUT 76622 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

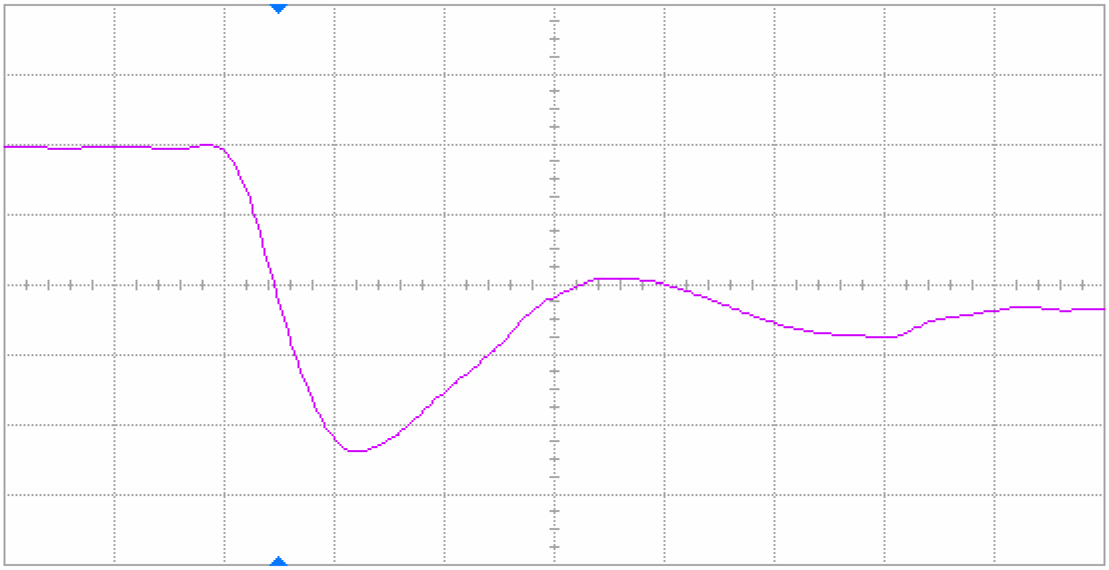


Figure 19(a) DUT 76664 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

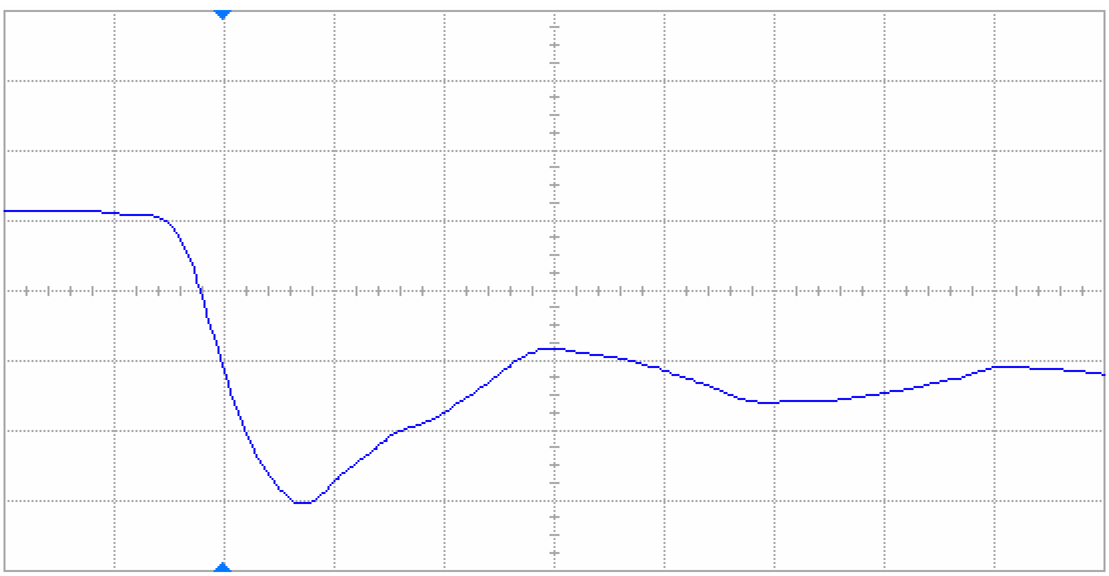
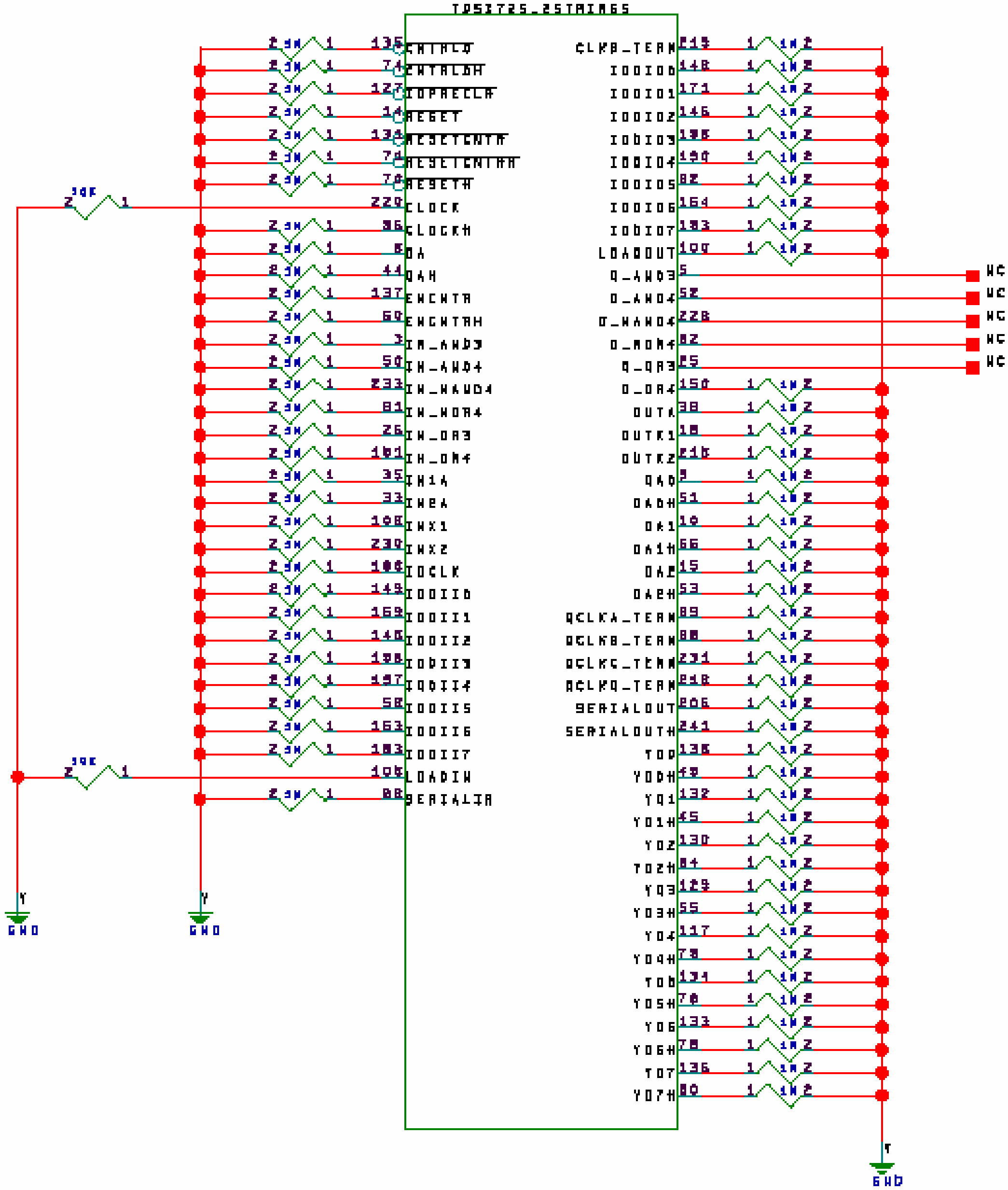
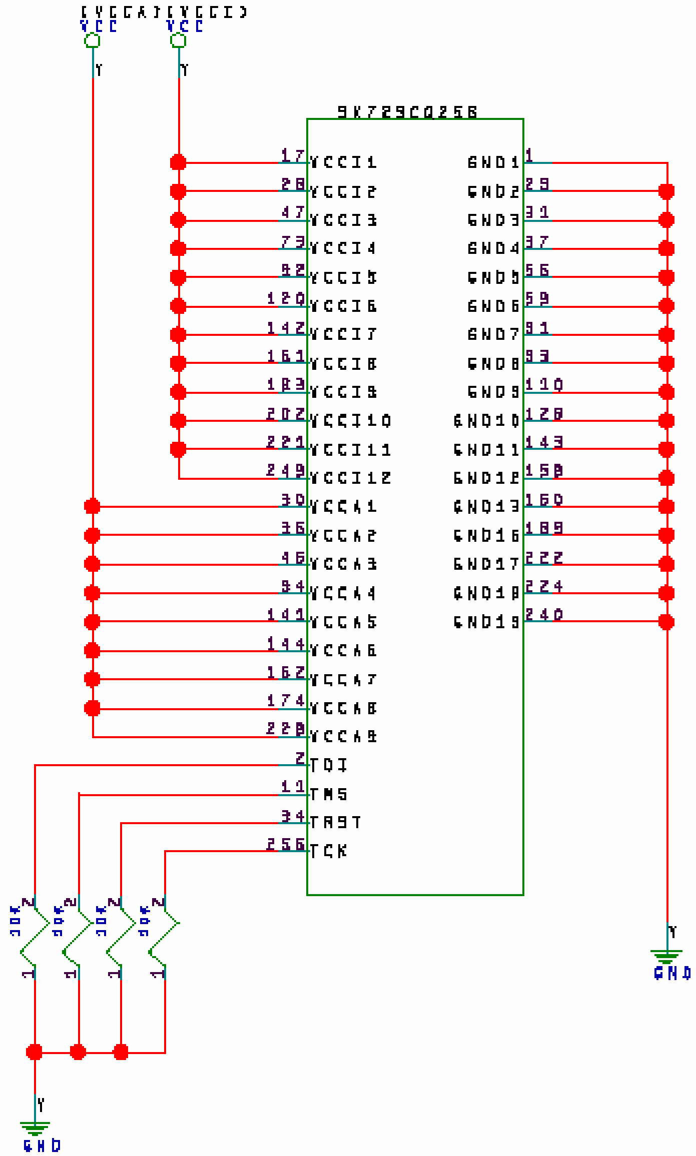


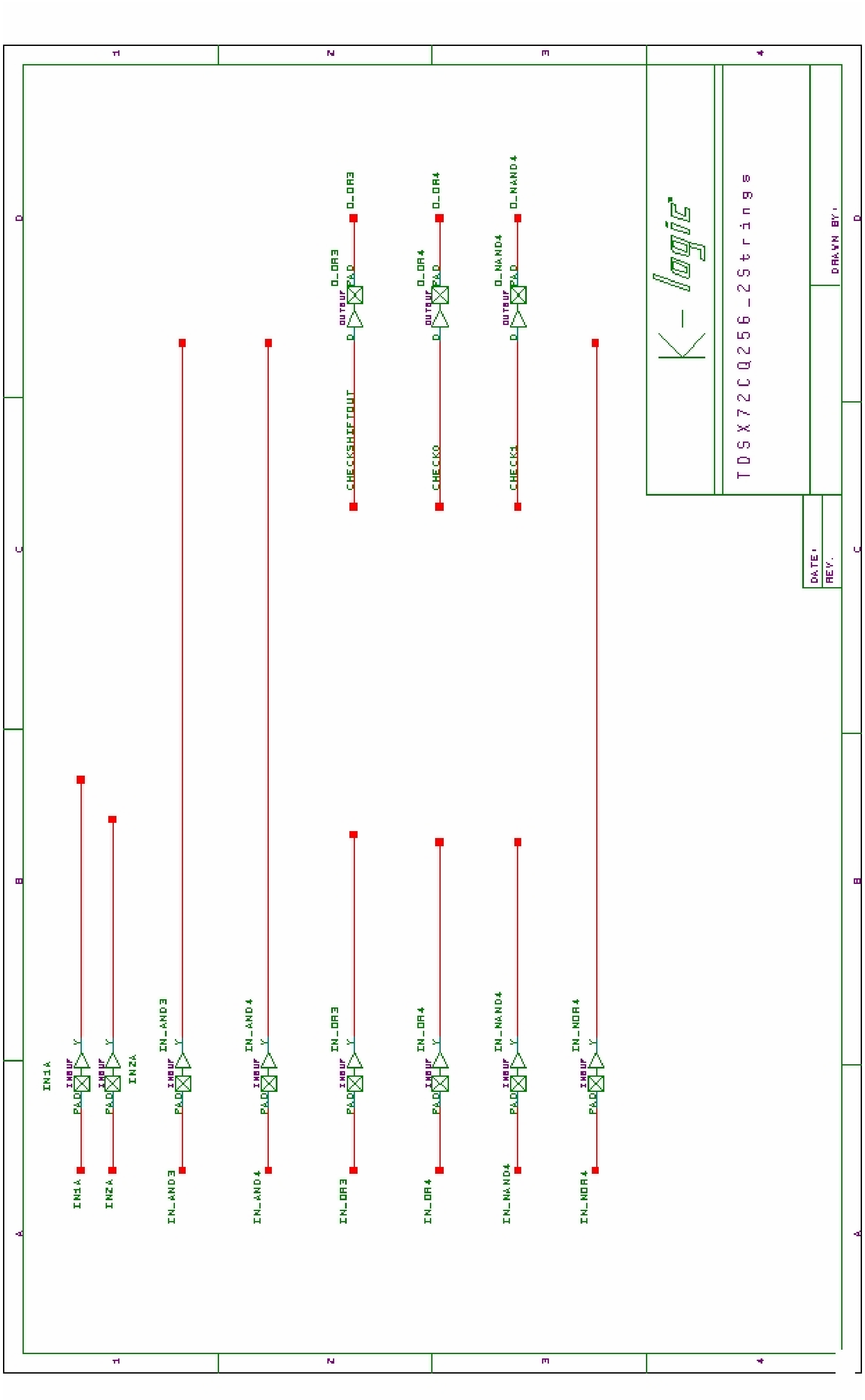
Figure 19(b) DUT 76664 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

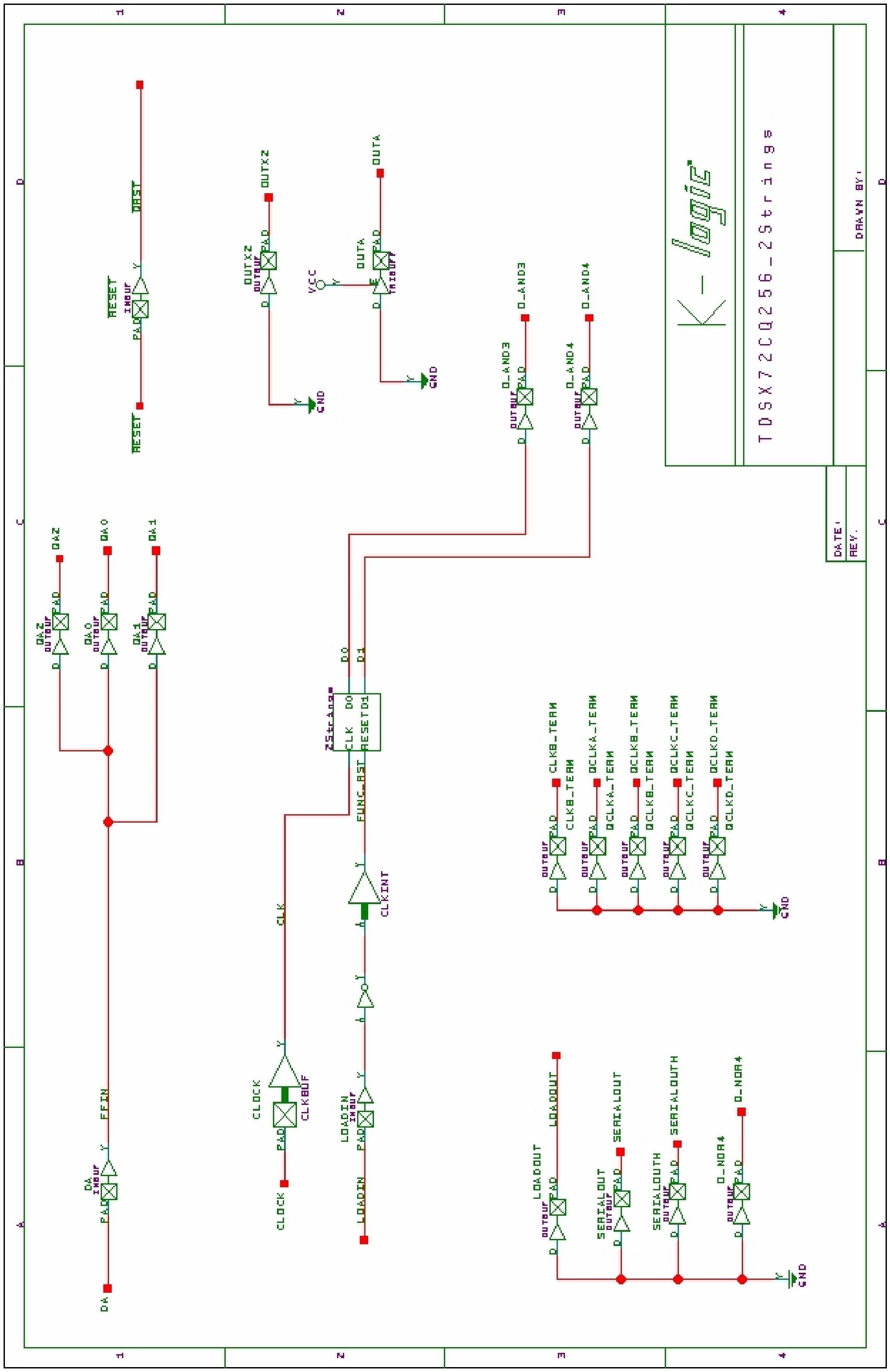
APPENDIX A DUT BIAS

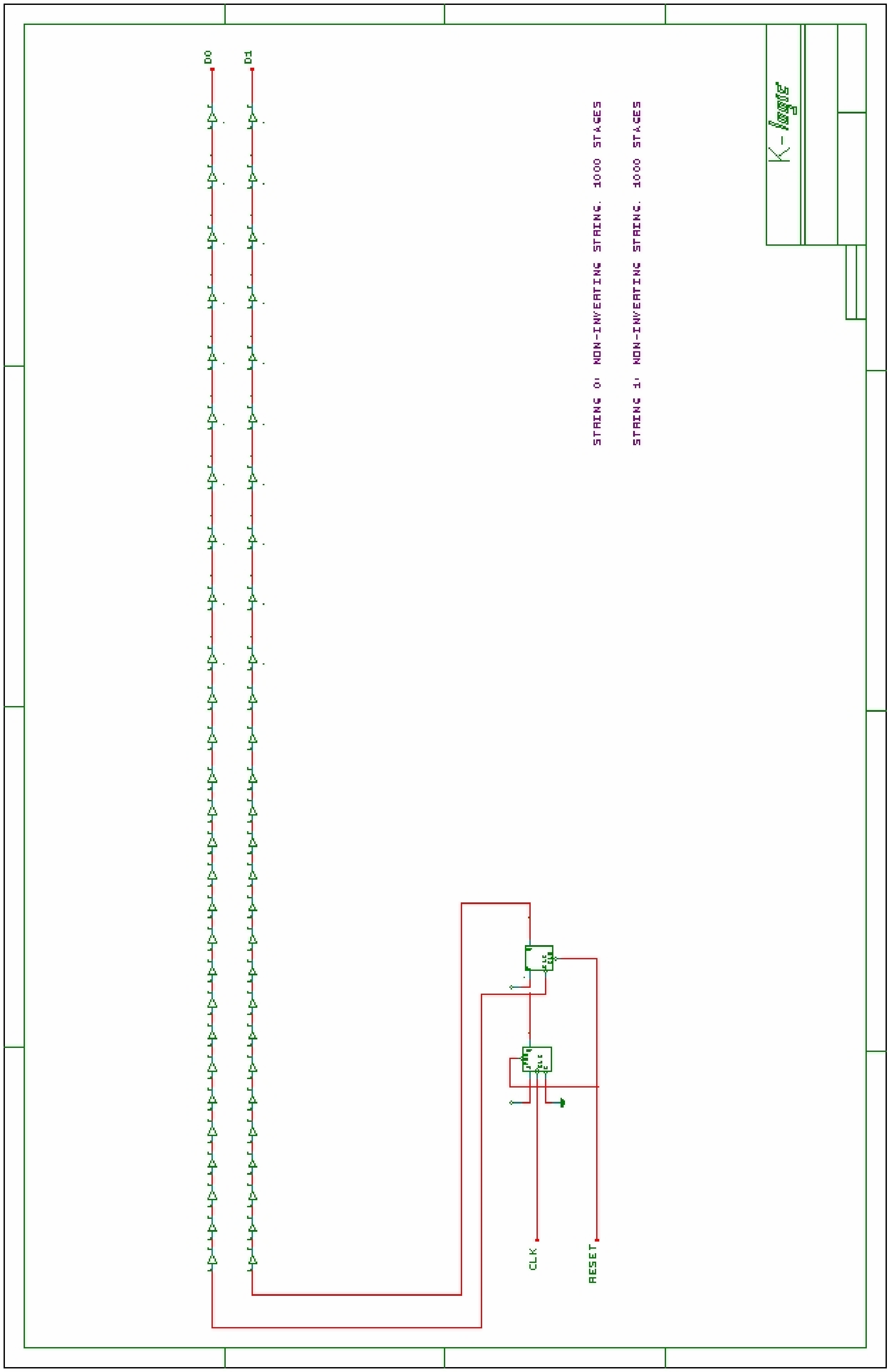


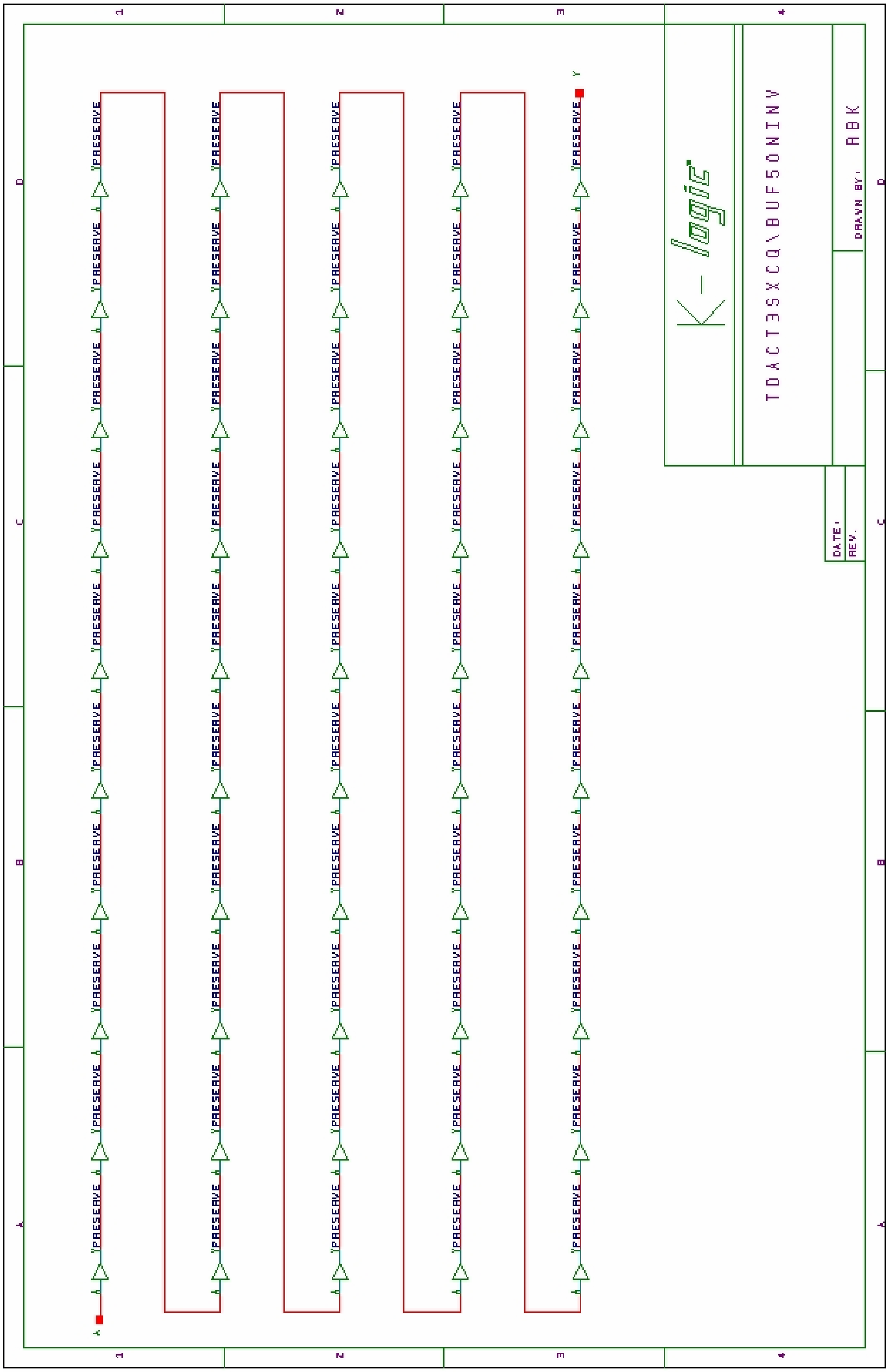

[VCCA][VCCI]
VCC
VCC
9K729CQ256
VCCI1
VCCI2
VCCI3
VCCI4
VCCI5
VCCI6
VCCI7
VCCI8
VCCI9
VCCI10
VCCI11
VCCI12
VCCA1
VCCA2
VCCA3
VCCA4
VCCA5
VCCA6
VCCA7
VCCA8
VCCA9
TDI
TMS
TRST
TCK
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND16
GND17
GND18
GND19
GND
GND
10K
10K
10K
10K

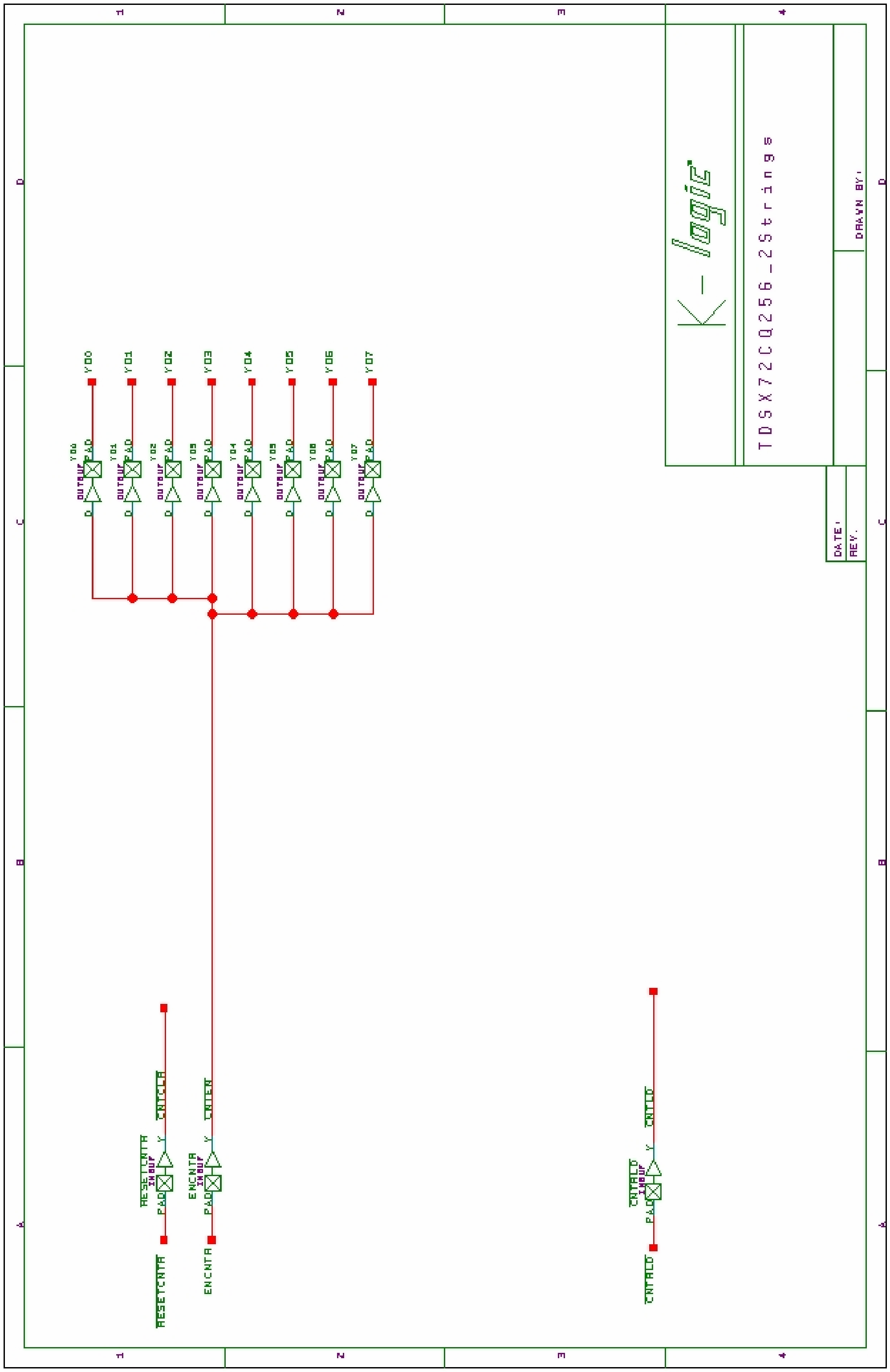
APPENDIX B DUT DESIGN SCHEMATICS

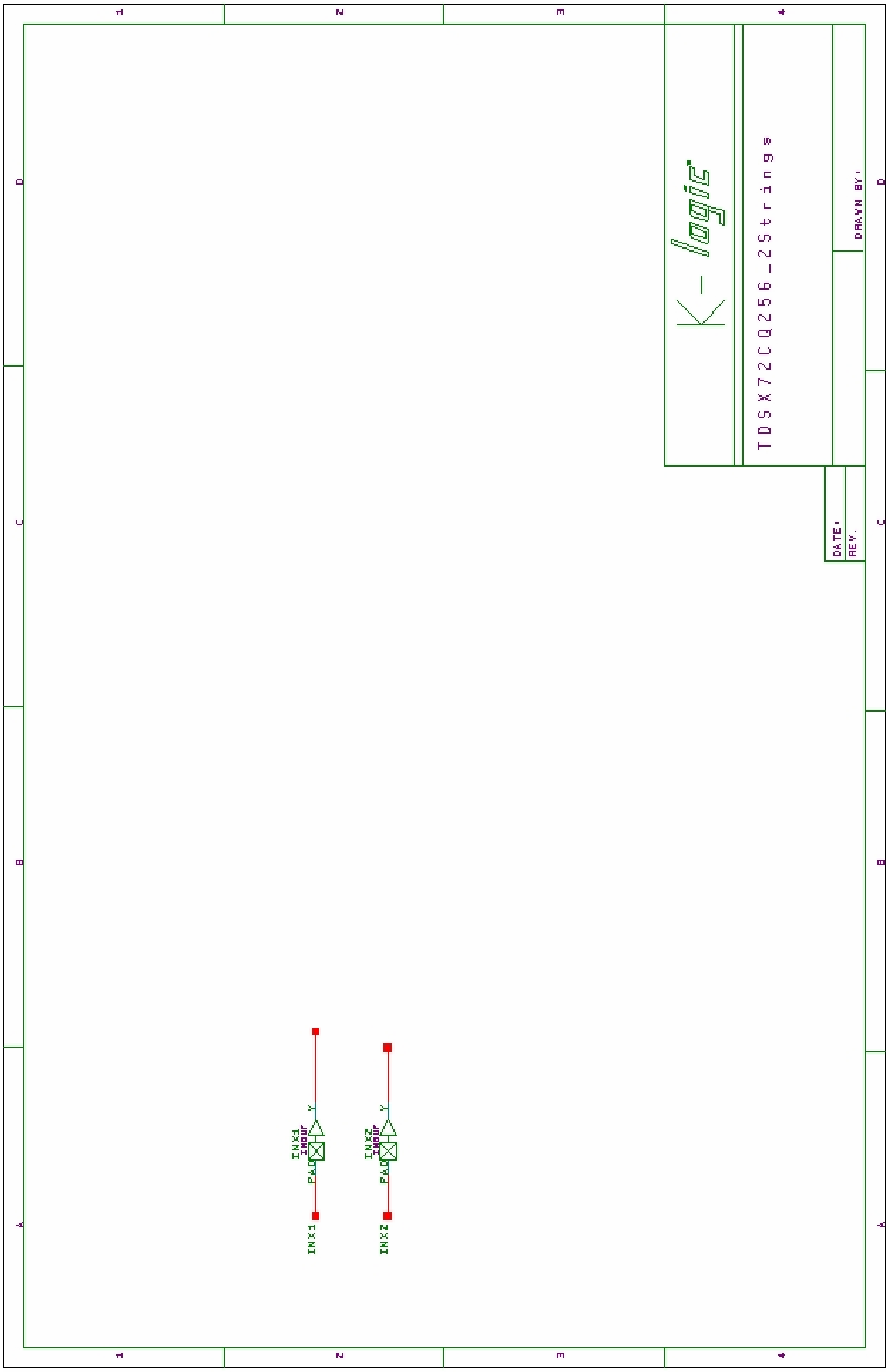


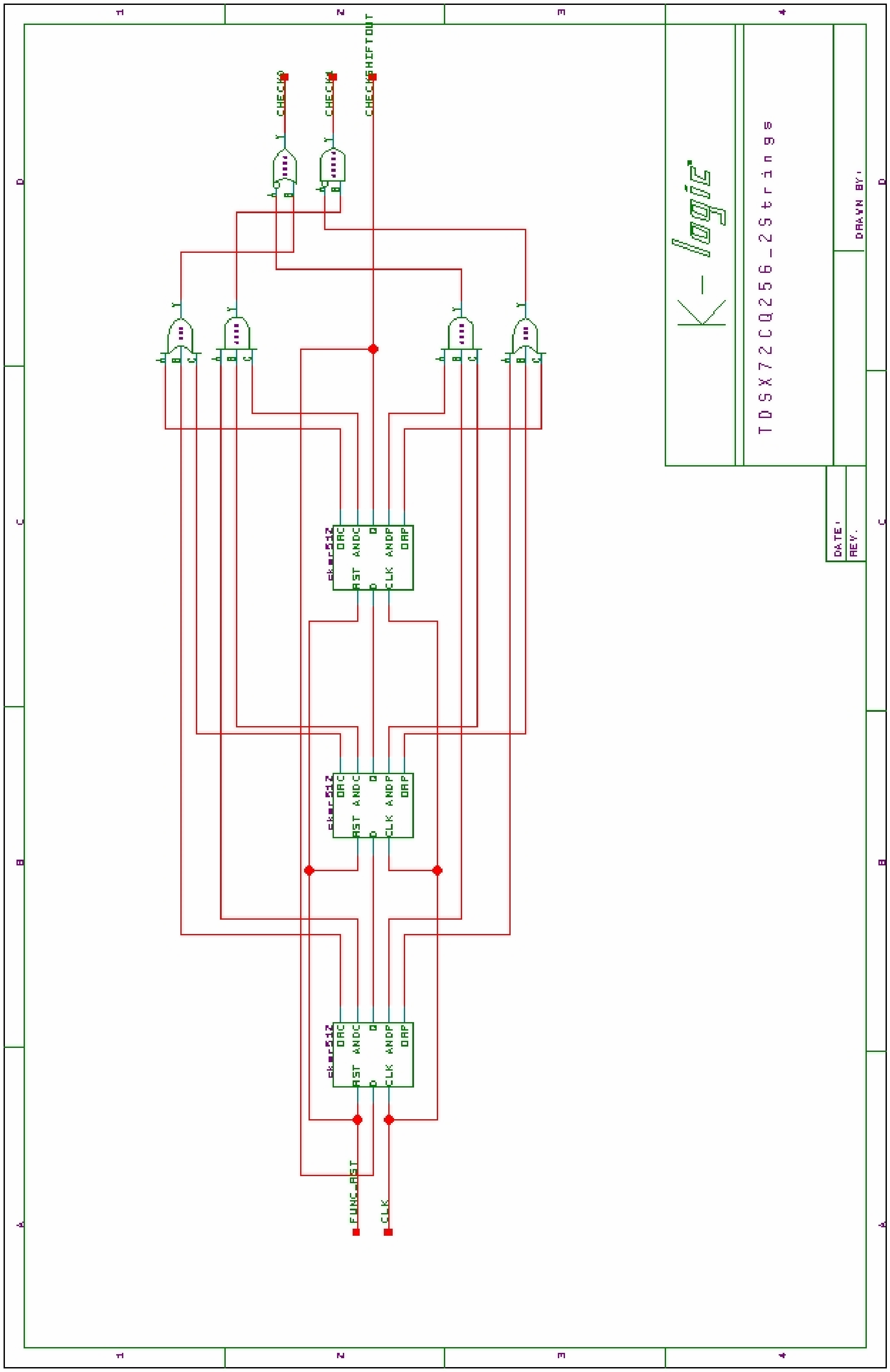

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
OUTX2
OUTA
VCC
GND
D_AND3
D_AND4
QA2
QA0
QA1
2Strings
CLK
RESET
D0
D1
FUNC_RST
CLK
CLKINT
CLOCK
CLKBUF
LOADIN
DA
FFIN
CLKB_TERM
QCLKA_TERM
QCLKB_TERM
QCLKC_TERM
QCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

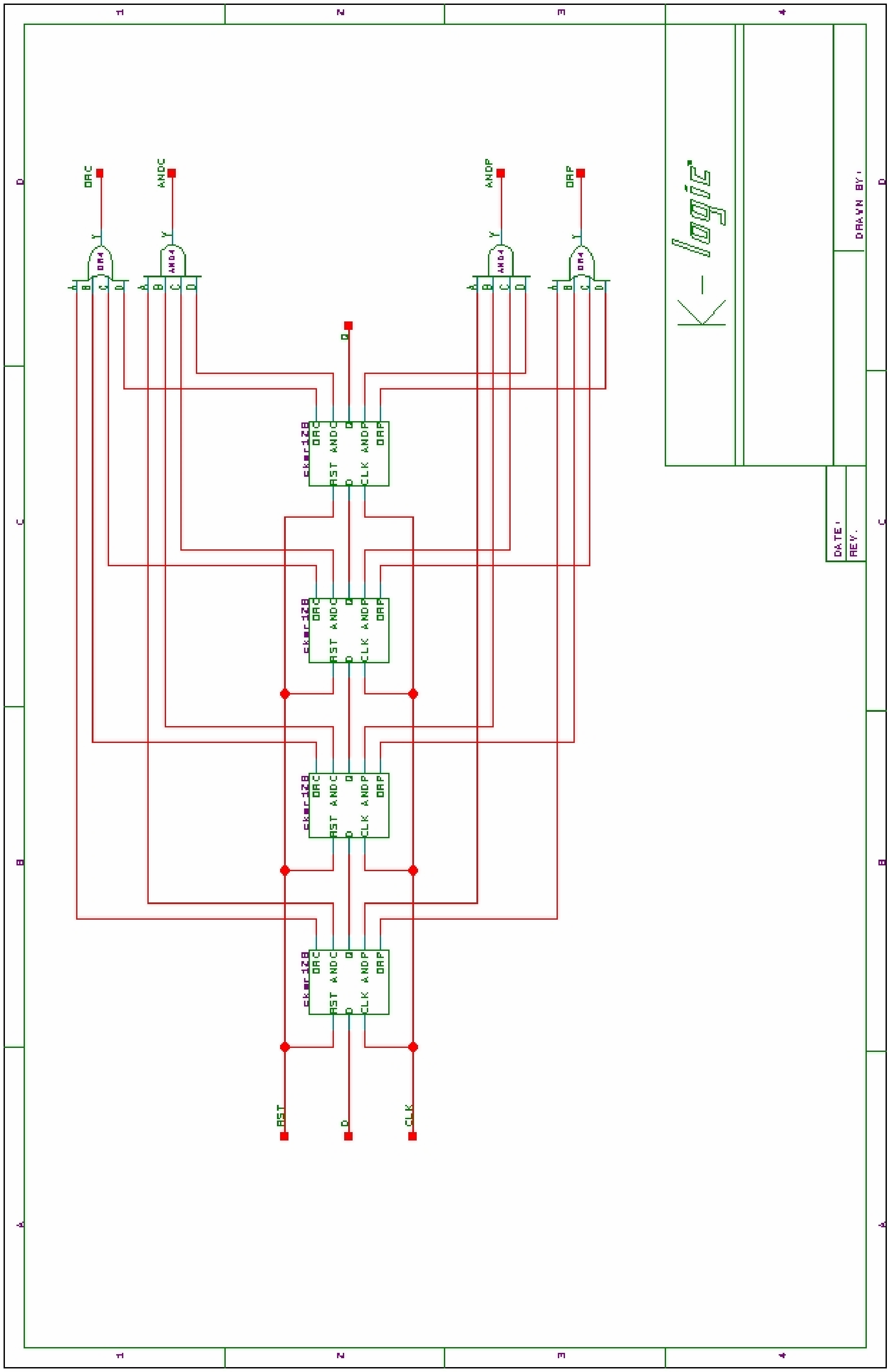

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
CLK
RESET


K-logic
TDACT3SXCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.

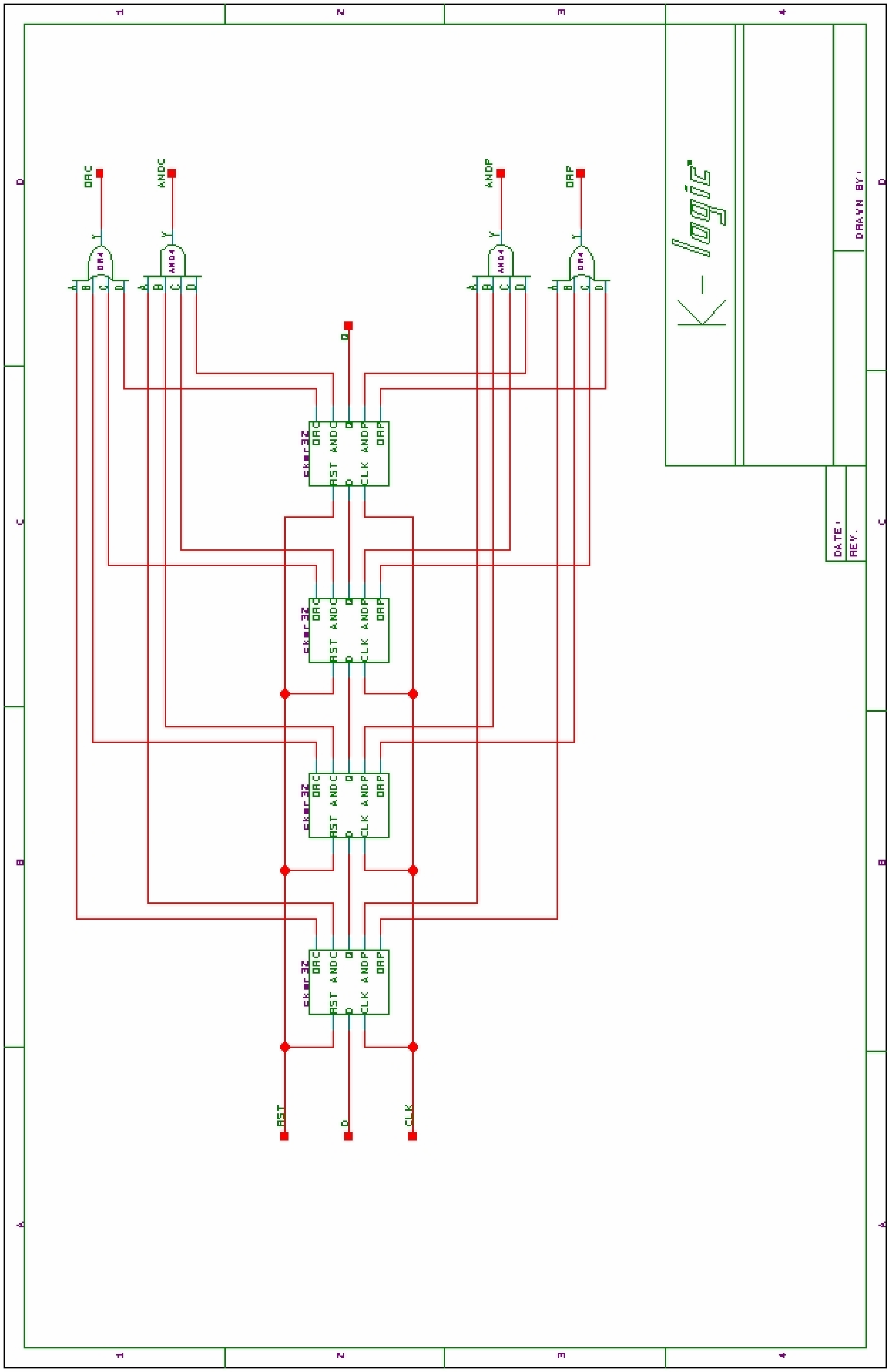

TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:
YO0
YO1
YO2
YO3
YO4
YO5
YO6
YO7
OUTBUF
PAD
INBUF
RESETCNTA
ENCNTA
CNTCLR
CNTEN
CNTALD
CNTLD

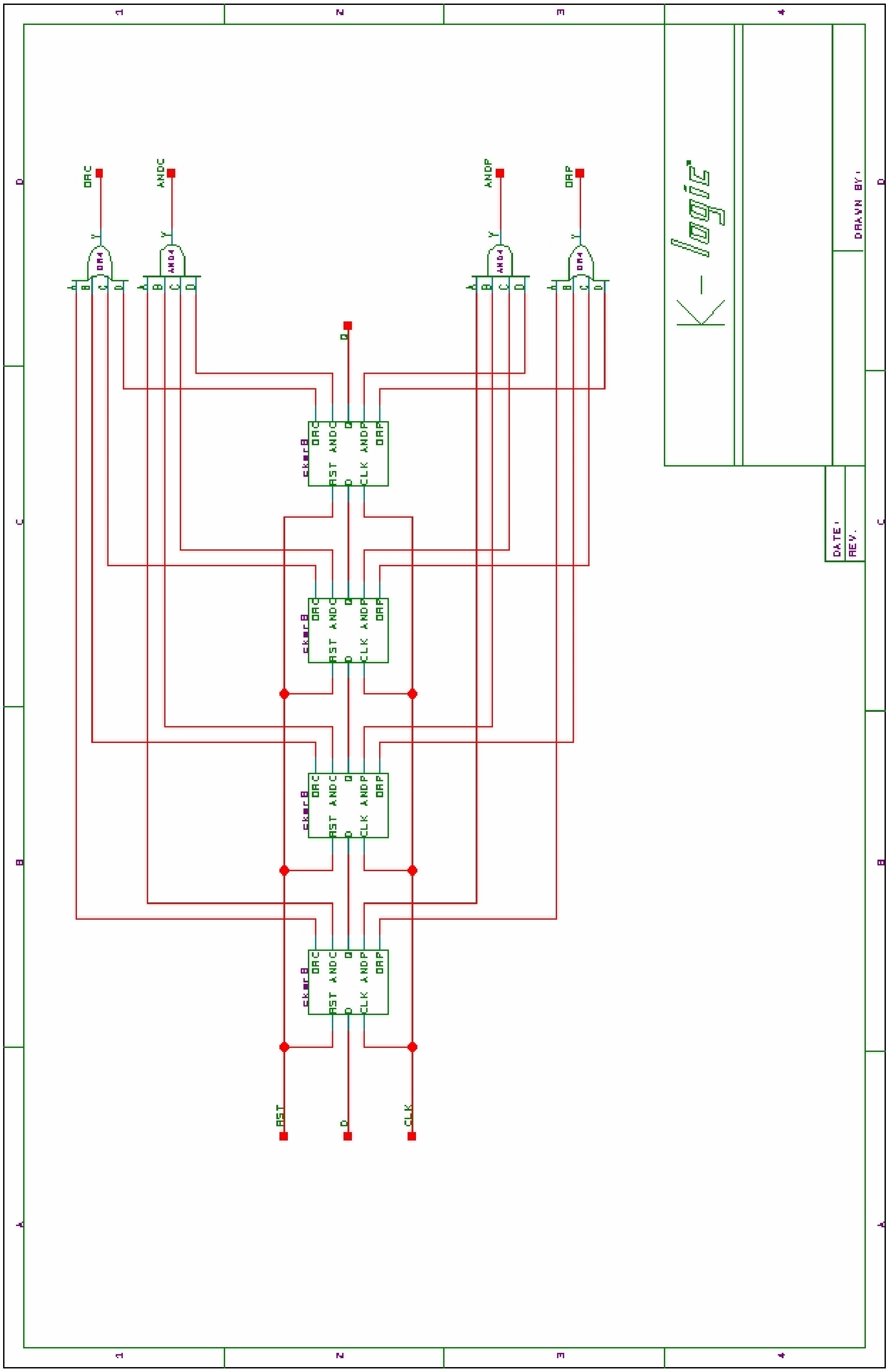

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2
INBUF
Y

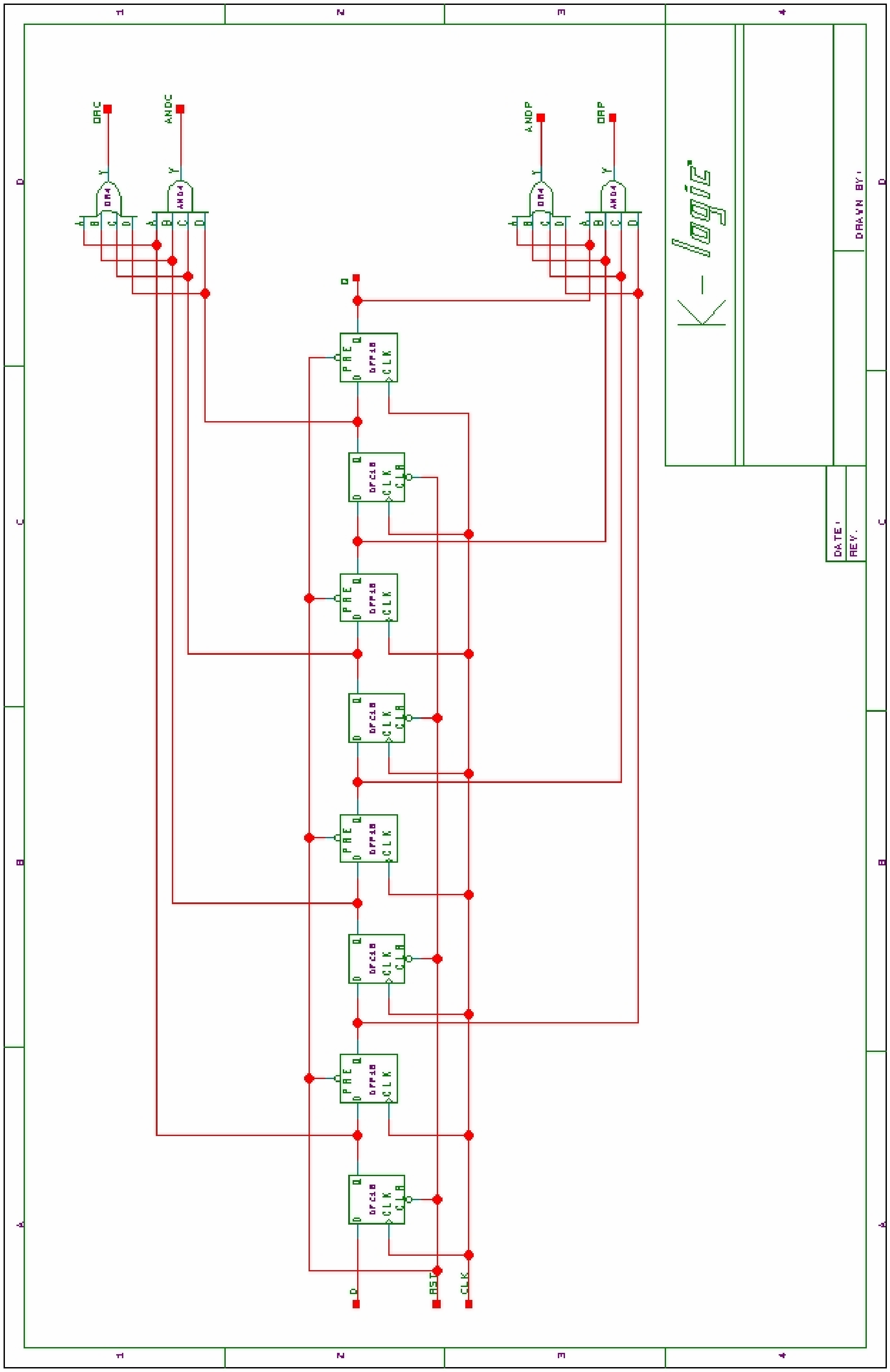

CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

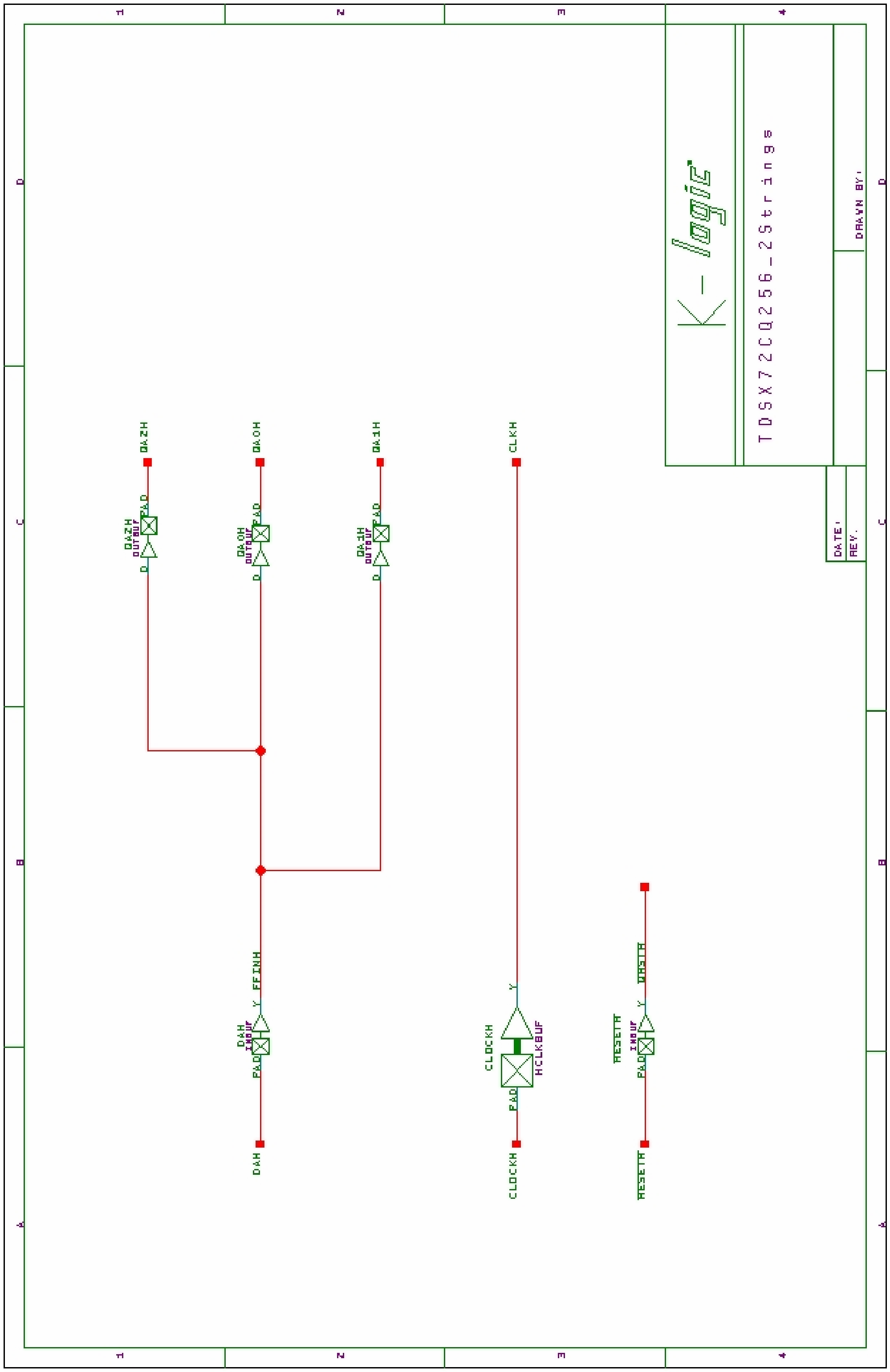


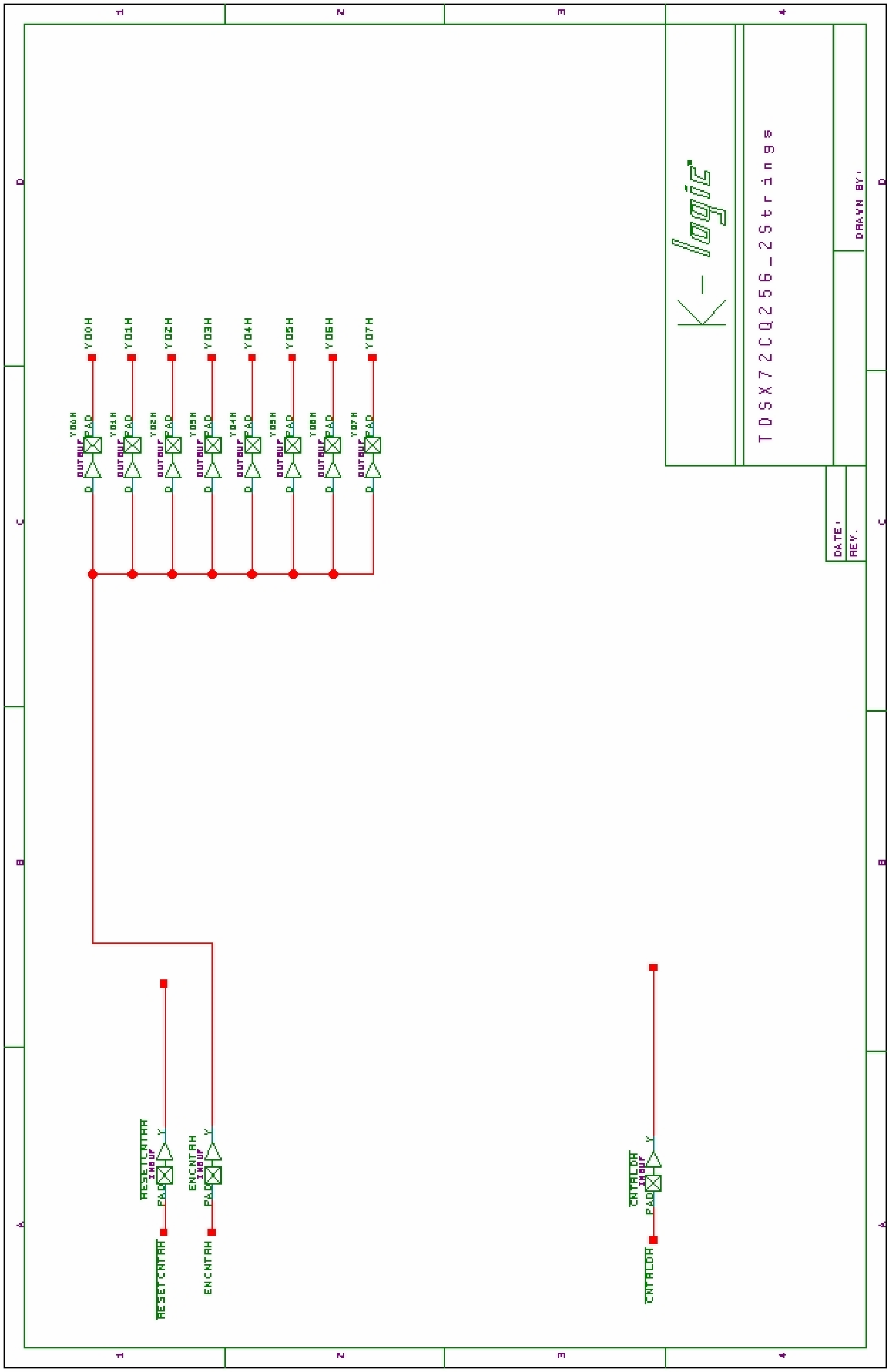
ORC
ANDC
ANDP
ORP
Q
ckmr128
RST
D
CLK
DATE:
REV.
DRAWN BY:


ORC
ANDC
ANDP
ORP
Q
ckmr32
RST
D
CLK
DRAWN BY:
DATE:
REV.

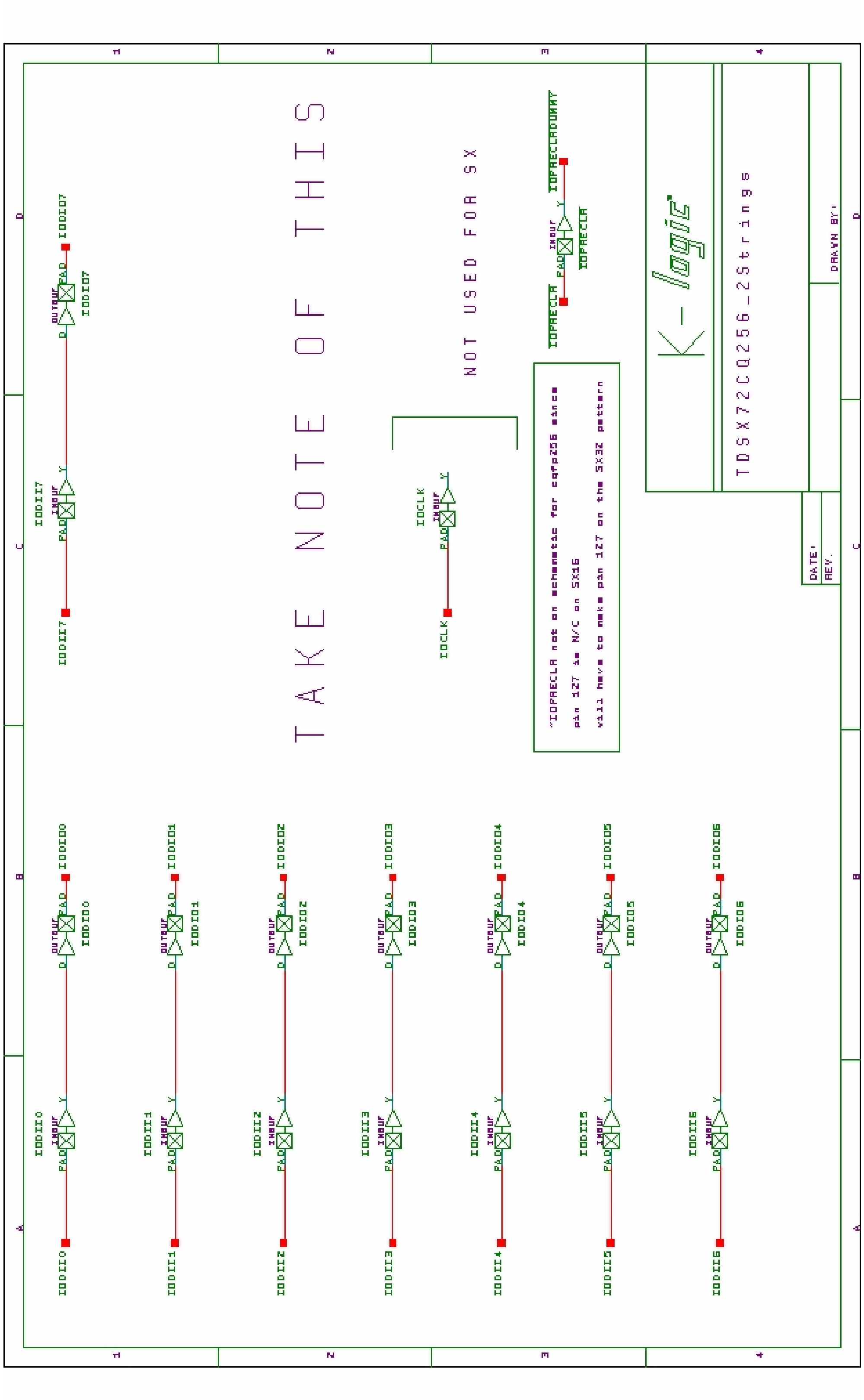

ORC
ANDC
ANDP
ORP
OR4
AND4
ckmrB
RST
D
CLK
Q
DRAWN BY:
DATE:
REV.

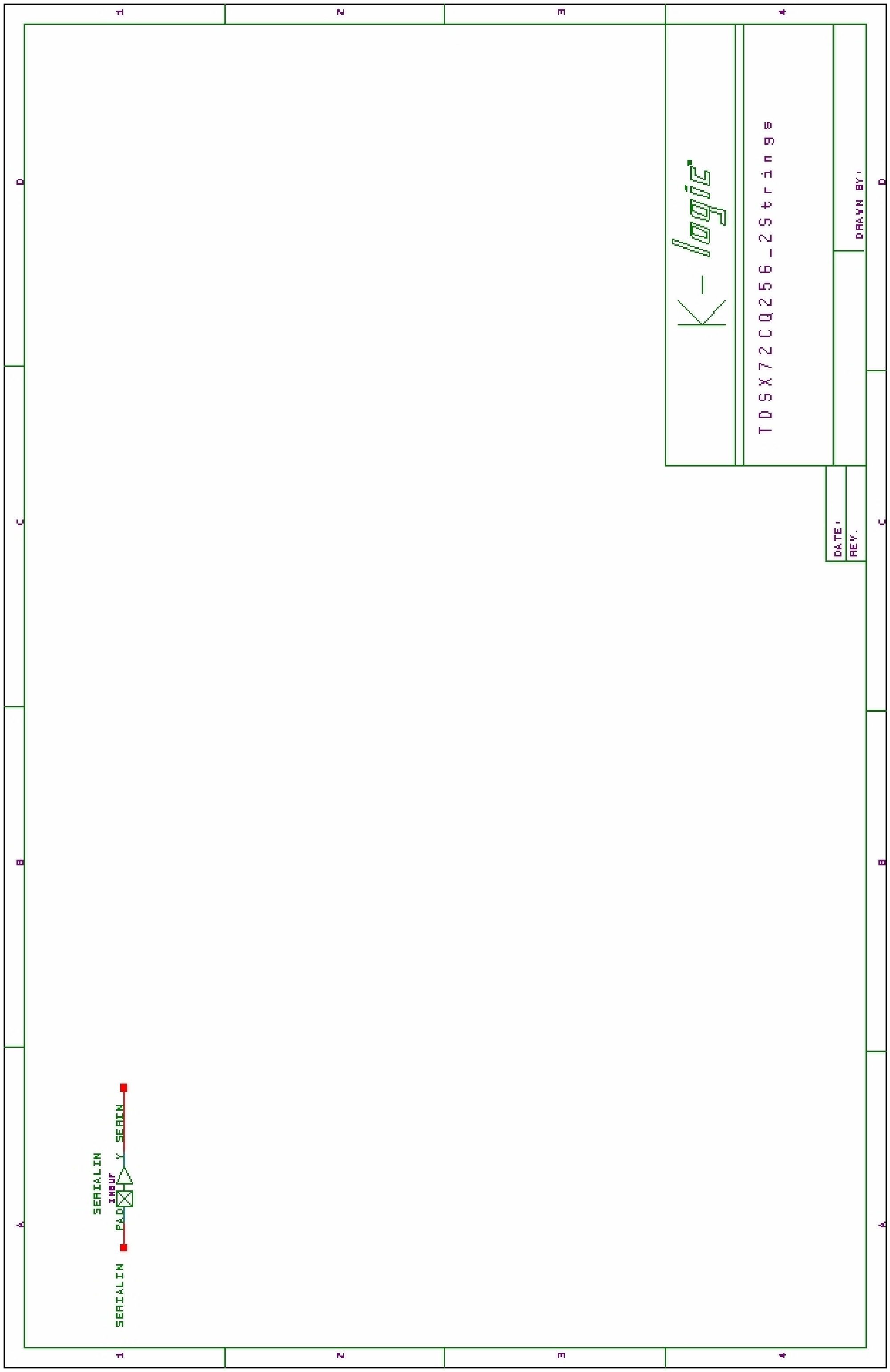

ORC
ANDC
ANDP
ORP
Q
D
RST
CLK
DATE:
REV.
DRAWN BY:

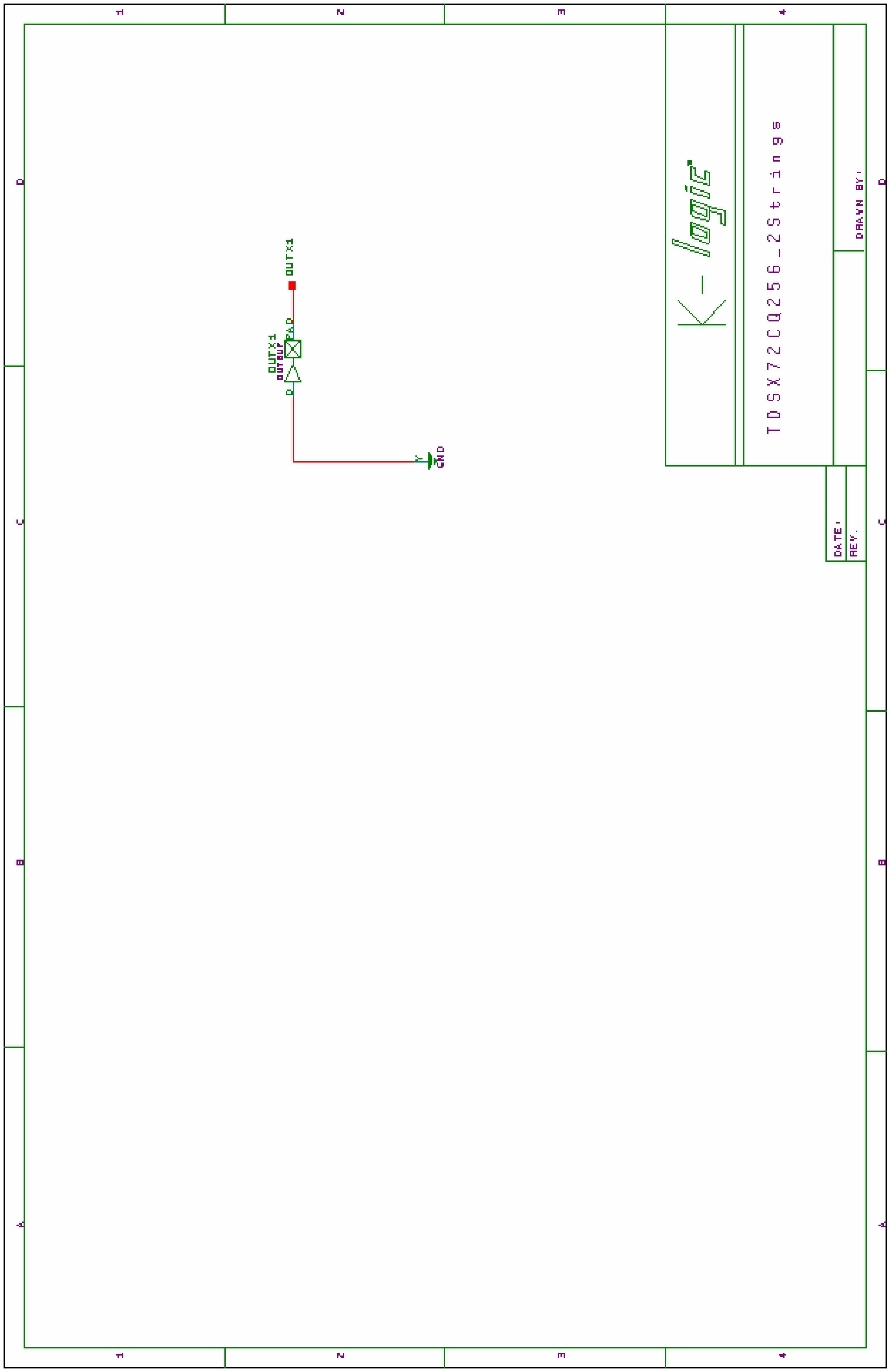

TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
QA2H
QA0H
QA1H
CLKH
OUTBUF
PAD
D
QAH
INBUF
FFINH
Y
CLOCKH
HCLKBUF
RESETH



TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
OUTBUF
PAD
INBUF
RESETCNTAH
ENCNTAH
CNTALDH


TAKE NOTE OF THIS
NOT USED FOR SX
*IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
IOPRECLR
IOPRECLRDUMMY
IOCLK
K-logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
SERIALIN
SERIALIN
INBUF
PAD
Y
SERIN



K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
OUTX1
PAD
OUTBUF
GND