Actel

TOTAL IONIZING DOSE TEST REPORT

No. 05T-RTSX72SU-D1HLJ1
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 70 krad (Si) per 25-mA spec. Post 100 krad (Si) and after 8 days room temperature annealing: average I_{CCA} = 108.8 mA; average I_{CCI} = 55.5 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) for 10% degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to the automatic-tester measurement, the bench measurement provides lower noise, better accuracy and more flexibility. The bench measurement samples pins for some measurements (e.g. threshold voltage measurement). However, since the tolerance is determined by the most degraded parameter, which is I_{CC} or propagation delay, sampling the pins for measuring non-critical parameters is appropriate.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. There are two groups: DUT 65838, 65878 and 65891 are irradiated to 60 krad; DUT 65907, 65981 and 62926 are irradiated to 100 krad. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings
Die Lot Number	D1HLJ1
Quantity Tested	6
Serial Number/Total Dose	60 krad: 65838, 65878, 65891 100 krad: 65907, 65981, 62926
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

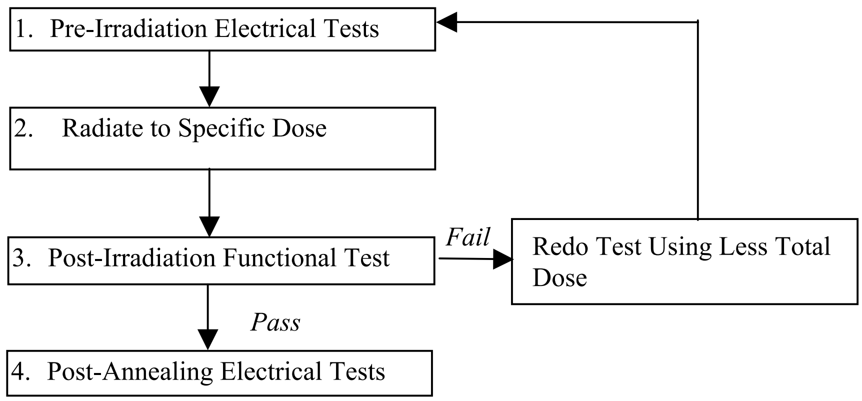


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. Both 60 krad-irradiated and 100 krad-irradiated group are annealed for approximately 8 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffer (pin DA to QA0)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (pin DA to QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (I_{CCA} and I_{CCI})

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 7 basically show the radiation-induced leakage current. The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data compares with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)		I_{CCI} (mA)	
		Post-rad	Post-ann	Post-rad	Post-ann
65838	60 krad	15.5	10	19	7.5
65878	60 krad	16.4	10.3	18.9	7.1
65891	60 krad	16.8	10.6	20.6	7.5
65907	100 krad	198	140	166	54.8
65981	100 krad	230	93	177	55
62926	100 krad	228	93.5	182	56.8

The 60 krad group shows the post-annealed I_{CC} passing the 25 mA spec. For the 100 krad group, an empirical equation is used to extract the total dose tolerance. The critical total dose ($\gamma_{critical}$) for a 10-year mission to induce I_{CC} to 25 mA is obtained from the equation:

$$I_{CCA}(\gamma_{critical}) \times 0.32 + I_{CCI}(\gamma_{critical}) \times 0.29 = 25mA$$

Where $I_{CCA}(\gamma)$ and $I_{CCI}(\gamma)$ are in-flux currents when total dose equals to γ. Using the-worst-case in-flux currents degradation, which is DUT 65981 (Figure 6), the tolerance ($\gamma_{critical}$) is obtained as approximately 70 krad (Si). This equation produces a conservative tolerance because the process of a high-dose-rate irradiation plus annealing produces an I_{CC} higher than the I_{CC} produced by a consistent low-dose-rate irradiation process.

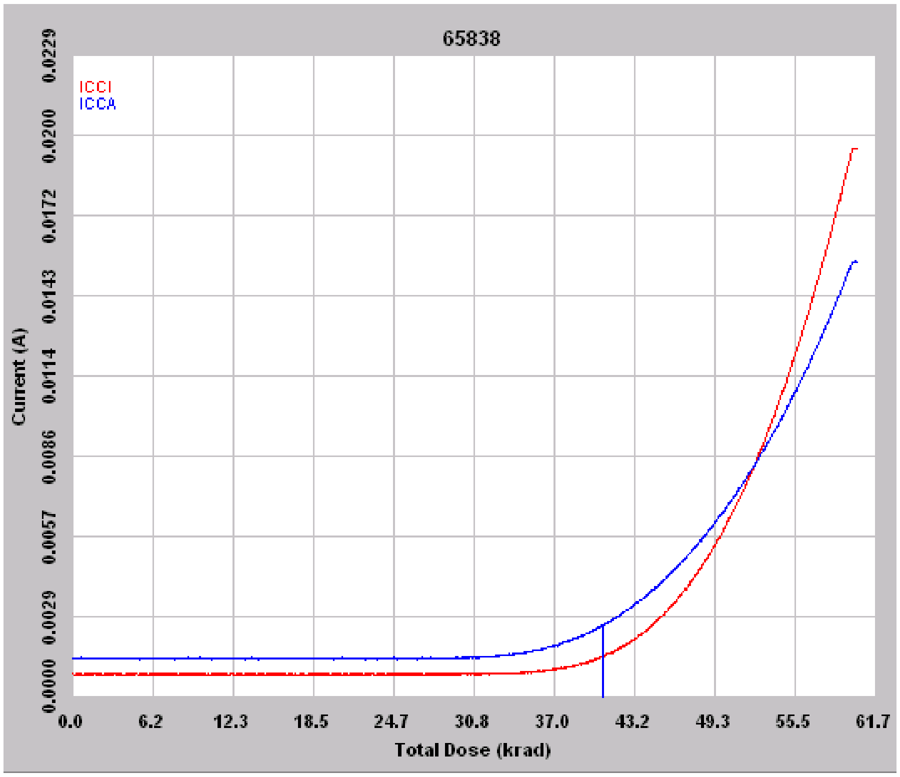


Figure 2 DUT 65838 in-flux I_{CCA} and I_{CCI}, 60 krad total dose

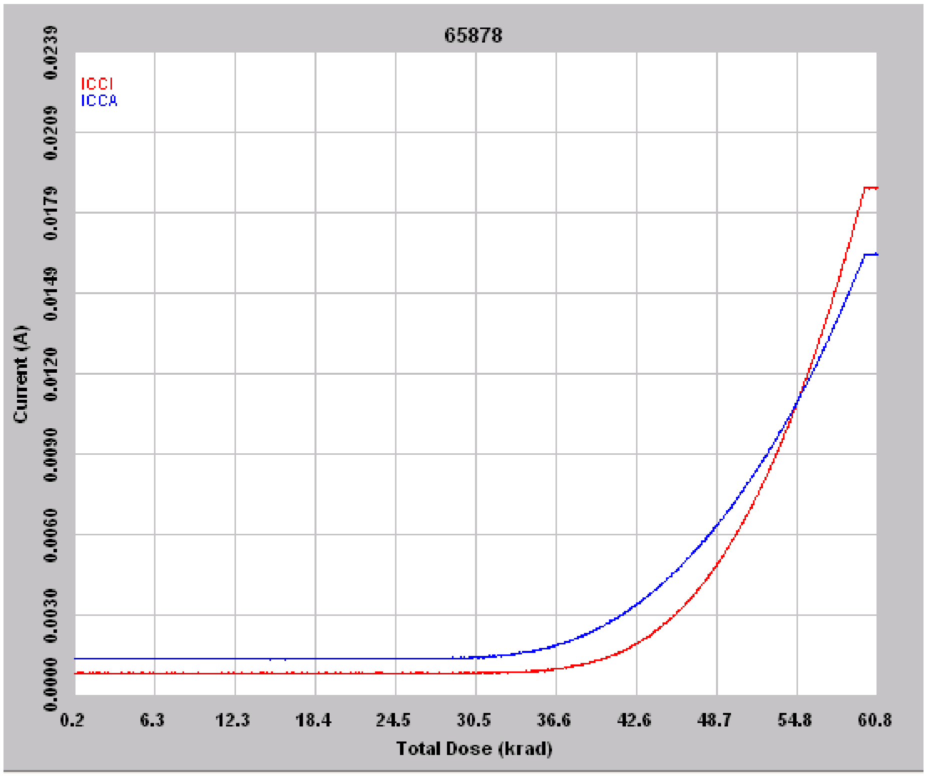


Figure 3 DUT 65878 in-flux I_{CCA} and I_{CCI}, 60 krad total dose

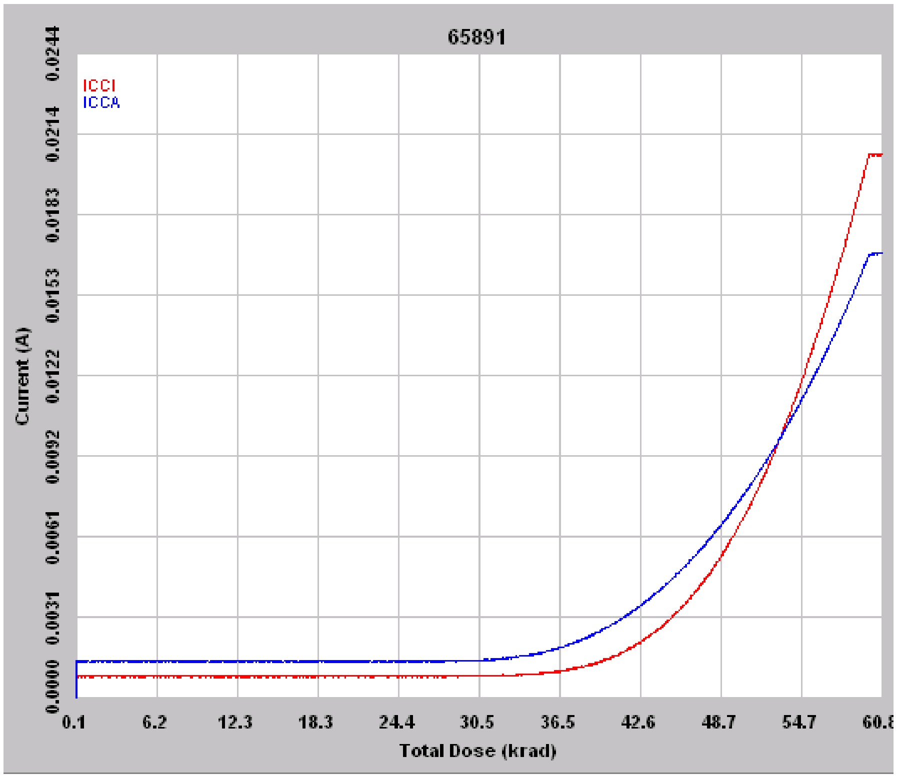


Figure 4 DUT 65891 in-flux I_{CCA} and I_{CCI}, 60 krad total dose

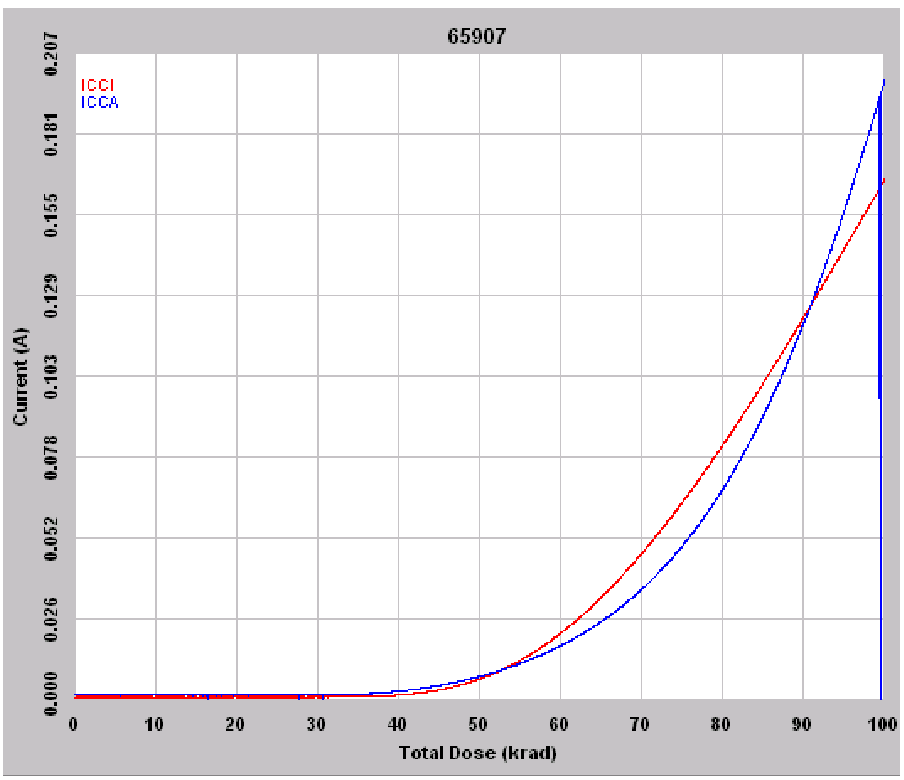


Figure 5 DUT 65907 in-flux I_{CCA} and I_{CCI}, 100 krad total dose

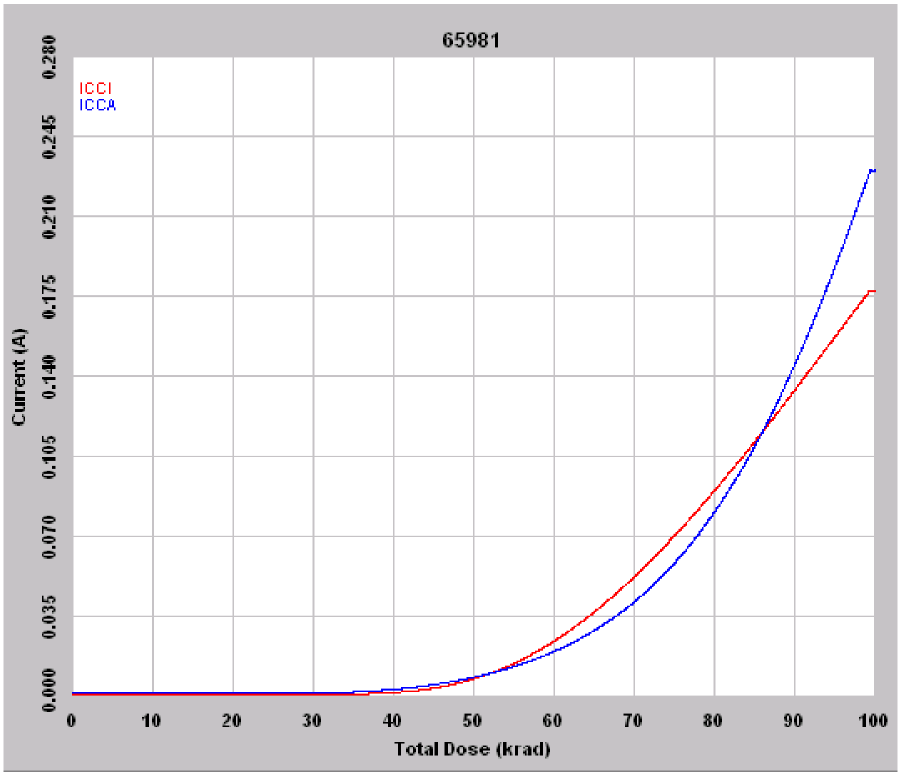


Figure 6 DUT 65981 in-flux I_{CCA} and I_{CCI}, 100 krad total dose

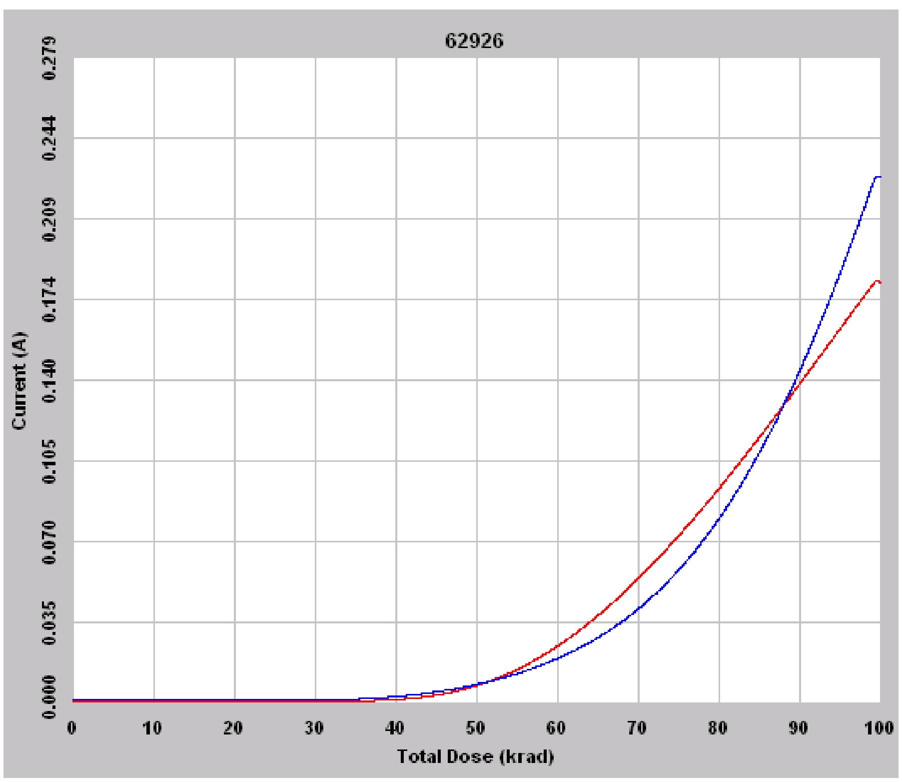


Figure 7 DUT 62926 in-flux I_{CCA} and I_{CCI}, 100 krad total dose

C. *Input Logic Threshold (V_{IL}/V_{IH})*

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds

DUT	Total Dose	Pre-Irradiation		Post-Annealing	
		V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
65838	60 krad	1.32	1.49	1.25	1.48
65878	60 krad	1.32	1.48	1.26	1.48
65891	60 krad	1.33	1.51	1.27	1.50
65907	100 krad	1.32	1.50	1.27	1.48
65981	100 krad	1.30	1.48	1.29	1.48
62926	100 krad	1.29	1.53	1.25	1.46

D. *Output-Drive Voltage (V_{OL}/V_{OH})*

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
65838	60 krad	0.009	0.009	0.103	0.103	0.171	0.172	0.432	0.434	0.888	0.892
65878	60 krad	0.009	0.009	0.103	0.103	0.171	0.172	0.432	0.433	0.888	0.889
65891	60 krad	0.009	0.009	0.104	0.105	0.174	0.175	0.439	0.440	0.901	0.905
65907	100 krad	0.009	0.009	0.103	0.106	0.172	0.176	0.435	0.443	0.892	0.909
65981	100 krad	0.009	0.009	0.103	0.105	0.172	0.175	0.434	0.440	0.892	0.904
62926	100 krad	0.009	0.009	0.104	0.105	0.173	0.175	0.436	0.440	0.897	0.904

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
65838	60 krad	4.99	4.98	4.87	4.85	4.65	4.64	4.07	4.04	2.79	2.70
65878	60 krad	4.99	4.98	4.87	4.85	4.65	4.64	4.08	4.05	2.80	2.71
65891	60 krad	4.99	4.98	4.87	4.85	4.65	4.64	4.08	4.05	2.80	2.71
65907	100 krad	4.99	4.99	4.87	4.86	4.65	4.64	4.07	4.03	2.78	2.64
65981	100 krad	4.99	4.98	4.87	4.85	4.65	4.63	4.07	4.03	2.78	2.64
62926	100 krad	4.99	4.98	4.86	4.86	4.65	4.64	4.06	4.04	2.72	2.67

E. *Propagation Delay*

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. The 60 krad group shows negative degradation, indicating that the radiation effect is negligible. In the 100 krad group, DUT 65981 has the worst degradation of 2.34%.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation	Post-Annealing	Degradation
65838	60 krad	1267.8	1252.6	-1.16%
65878	60 krad	1278.0	1271.1	-0.54%
65891	60 krad	1274.2	1270.8	-0.27%
65907	100 krad	1273.9	1297.0	1.81%
65981	100 krad	1273.1	1302.5	2.34%
62926	100 krad	1263.3	1290.4	2.15%

F. Transition Time

Figures 8 to 19 show the pre-irradiation and post-annealing transition edges. In each case, the radiation effect is not significant.

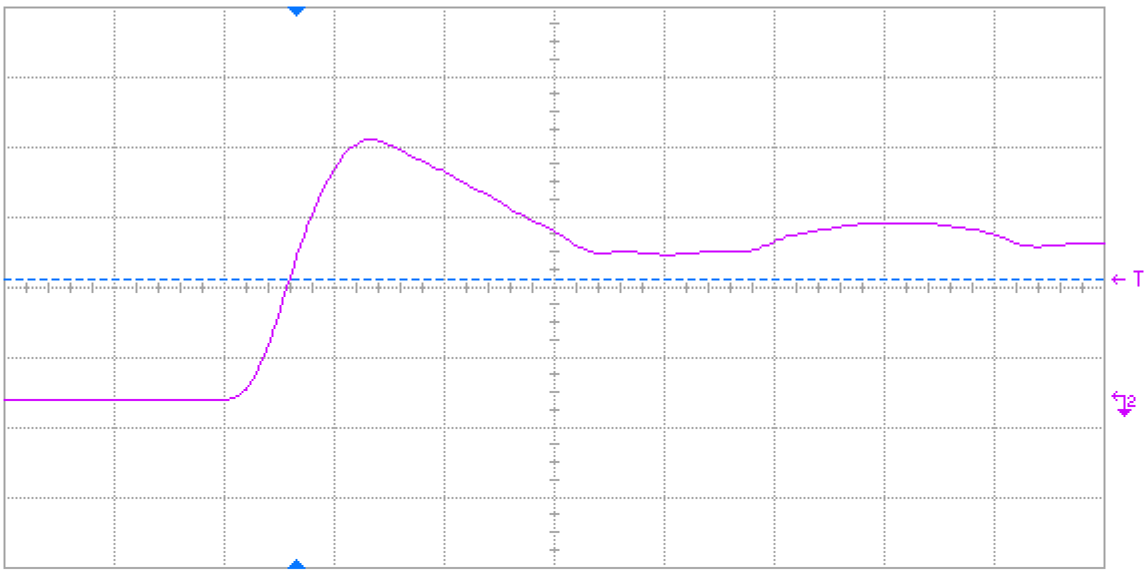


Figure 8(a) DUT 65838 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

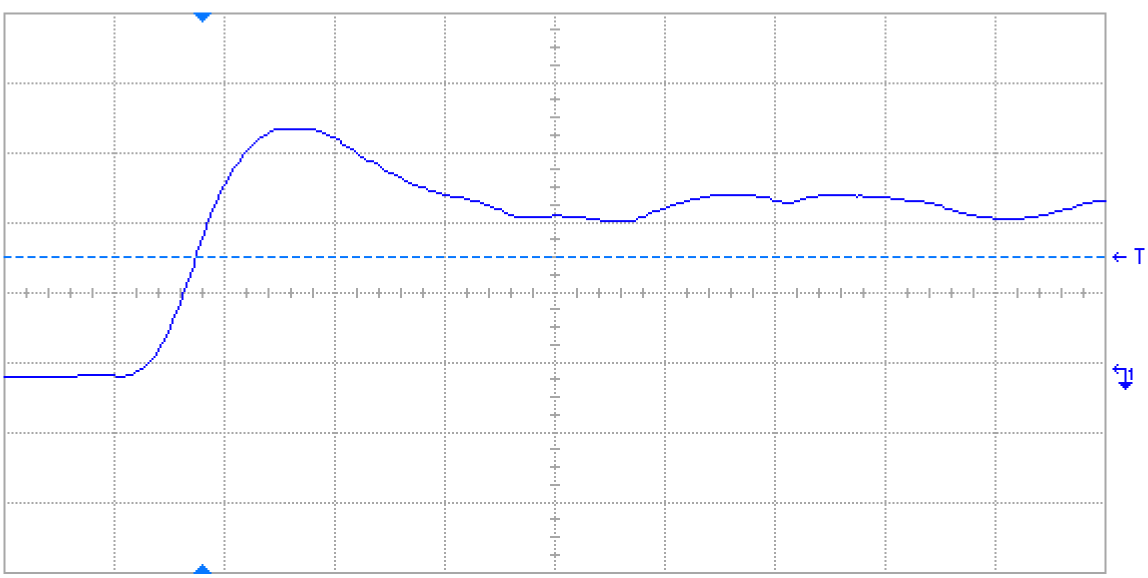


Figure 8(b) DUT 65838 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

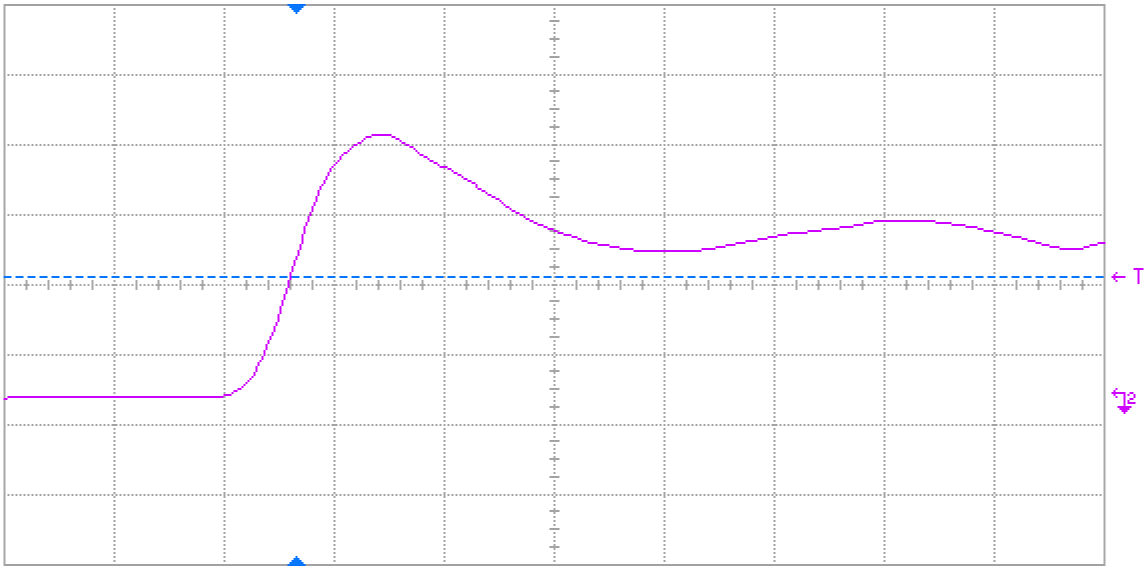


Figure 9(a) DUT 65878 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

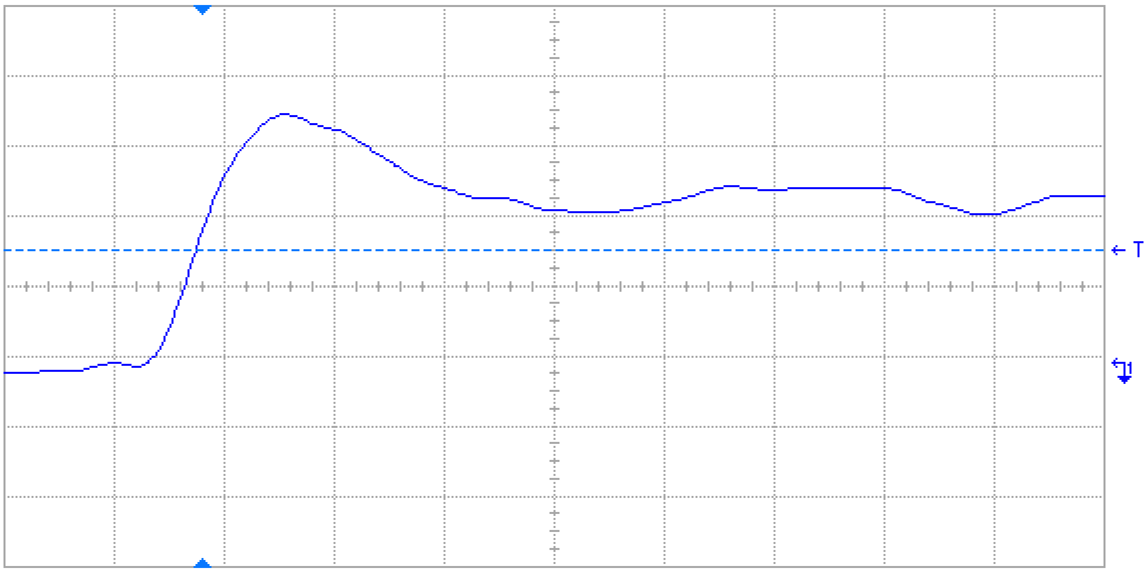


Figure 9(b) DUT 65878 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

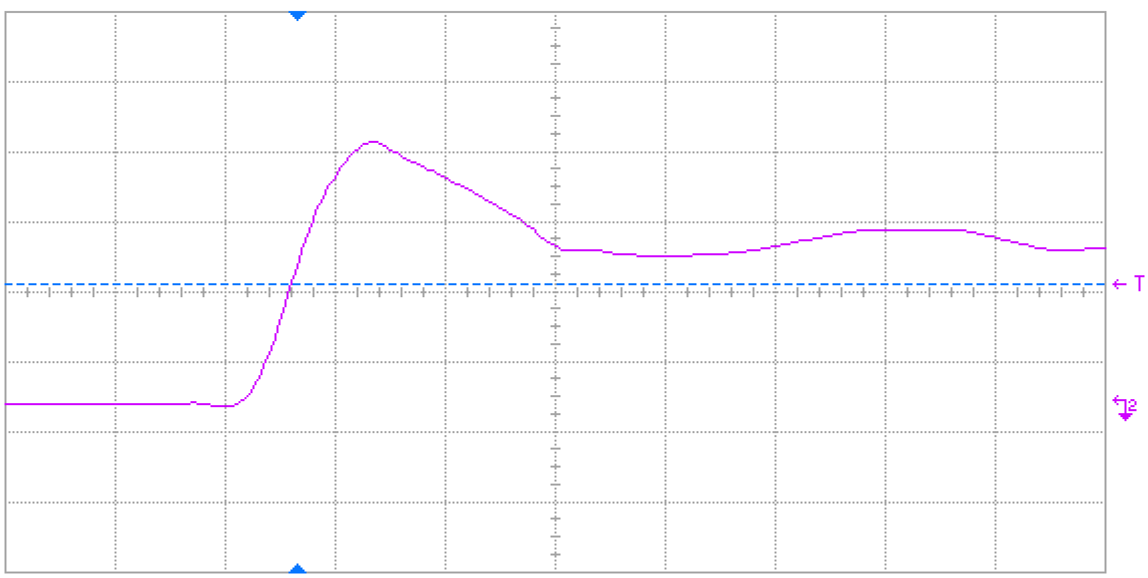


Figure 10(a) DUT 65891 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

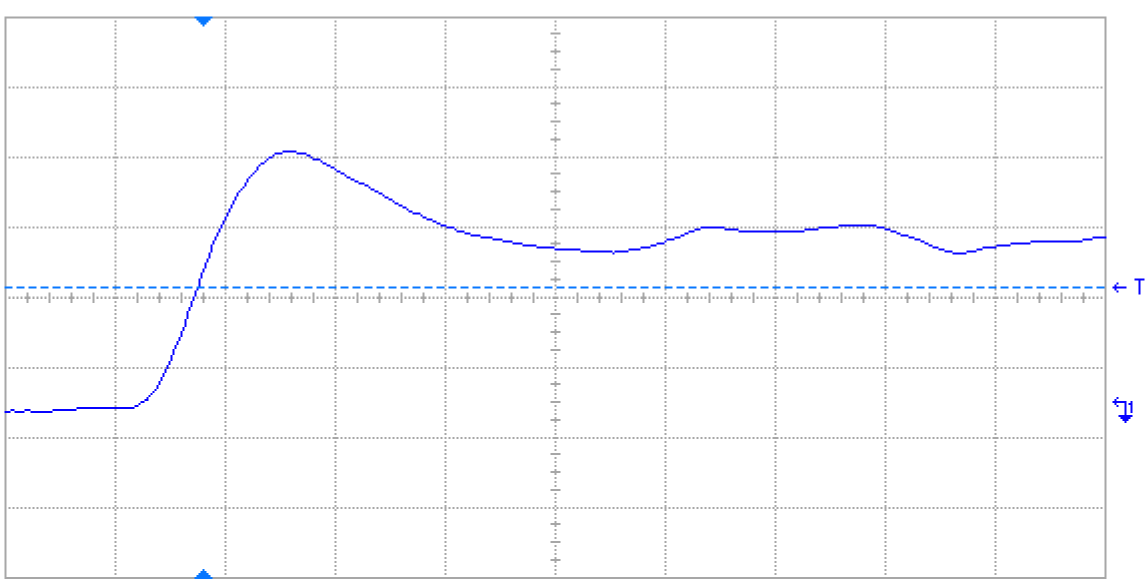


Figure 10(b) DUT 65891 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

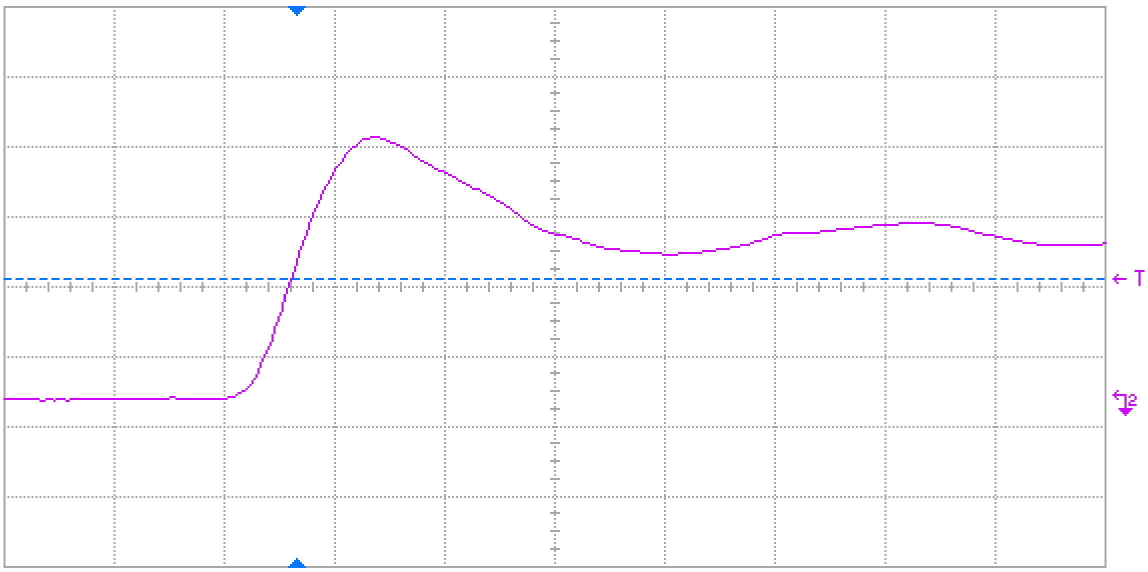


Figure 11(a) DUT 65907 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

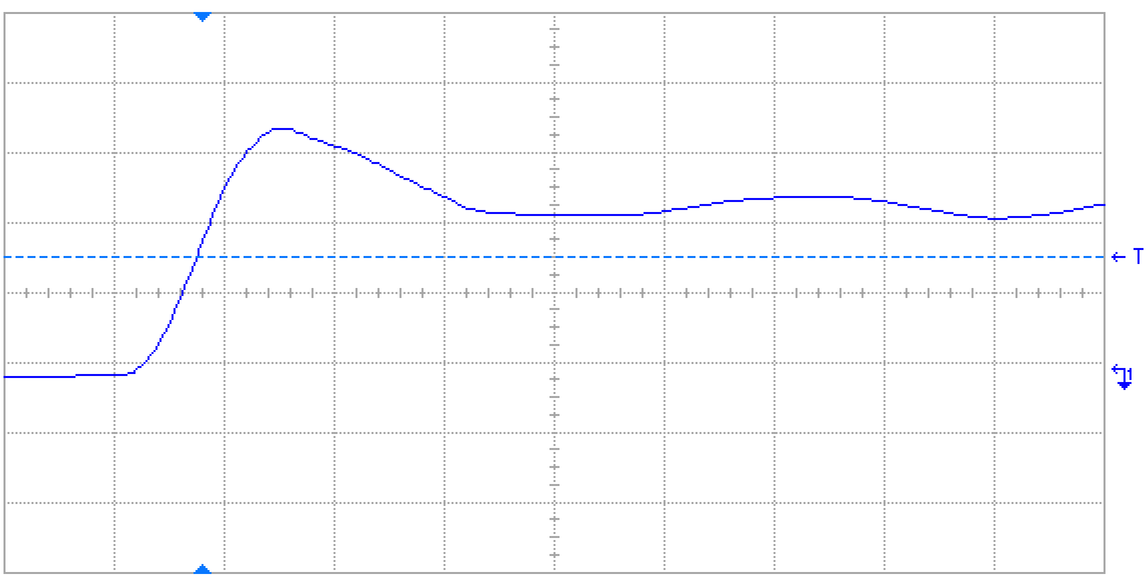


Figure 11(b) DUT 65907 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

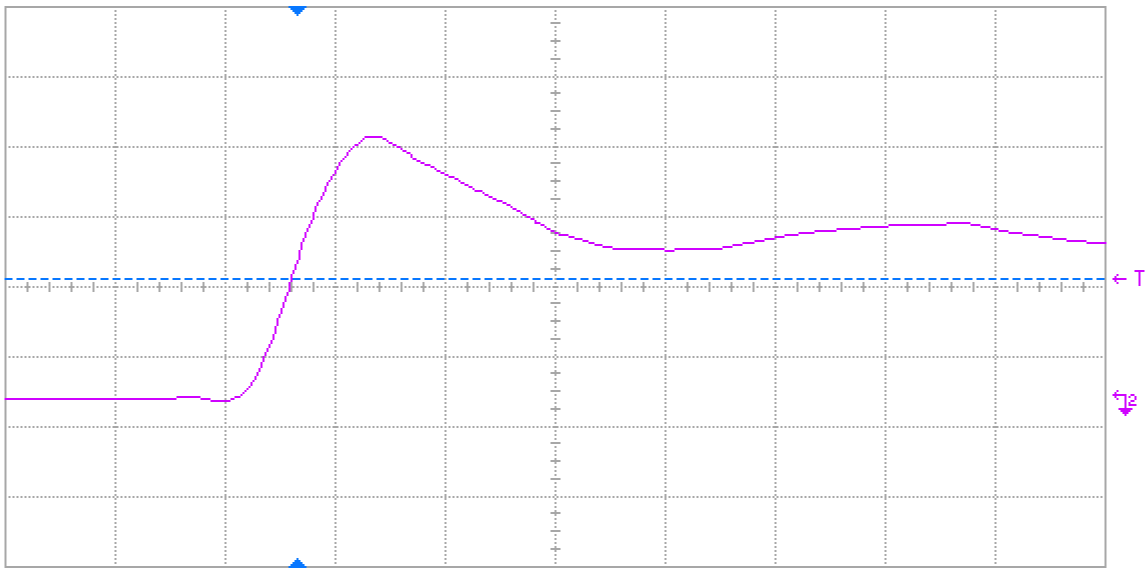


Figure 12(a) DUT 65981 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

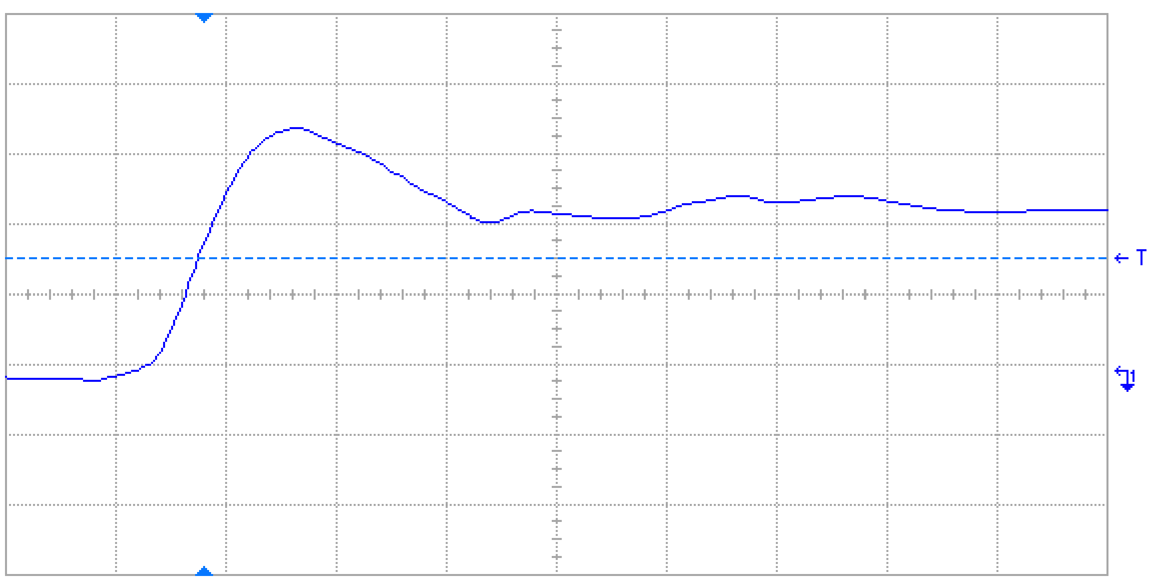


Figure 12(b) DUT 65981 post-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

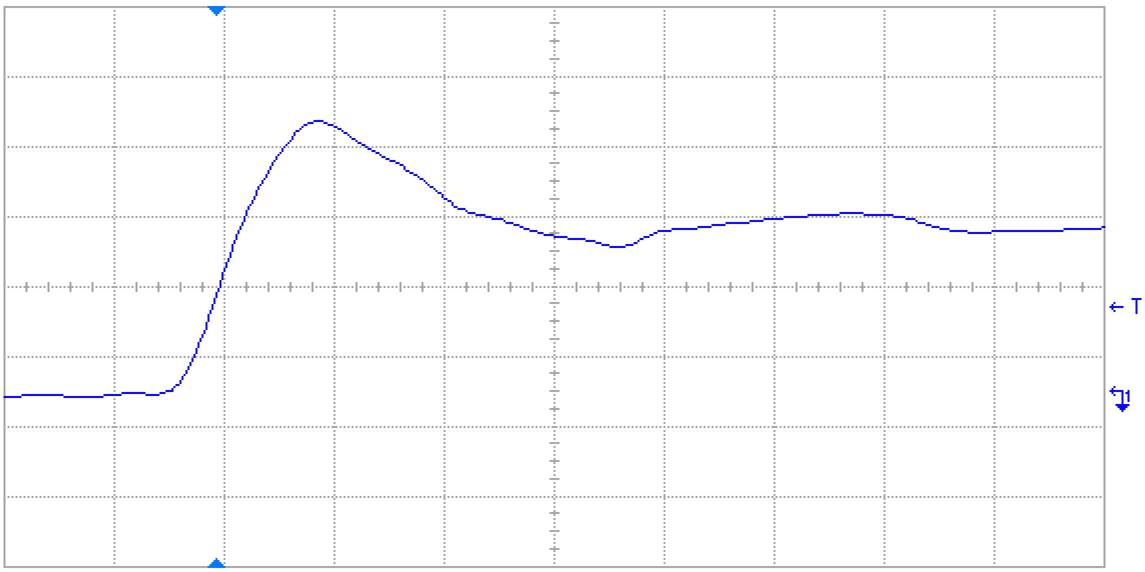


Figure 13(a) DUT 62926 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

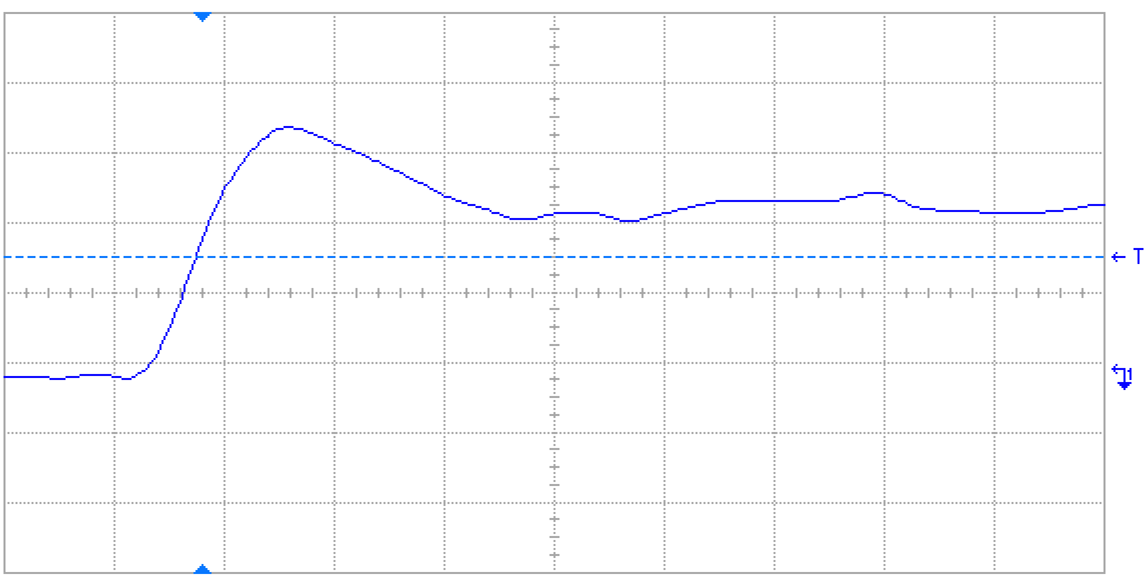


Figure 13(b) DUT 62926 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

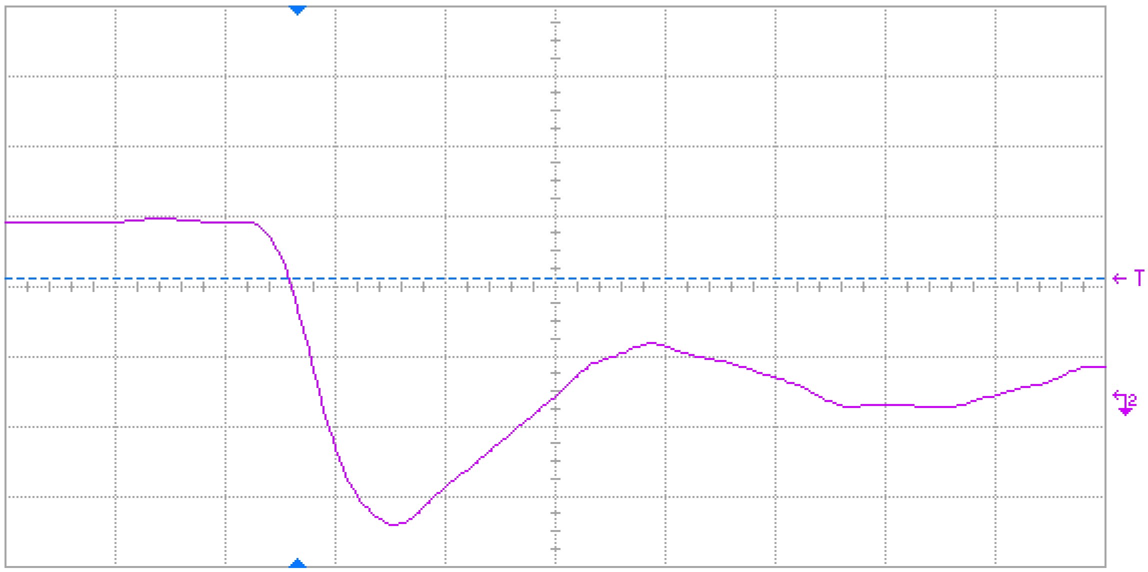


Figure 14(a) DUT 65838 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

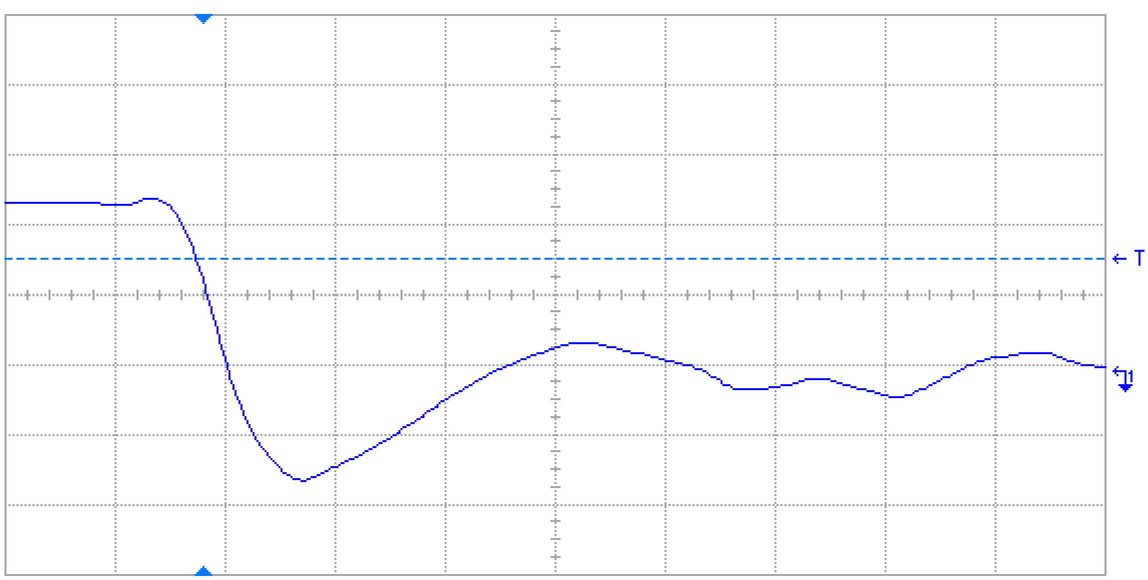


Figure 14(b) DUT 65838 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

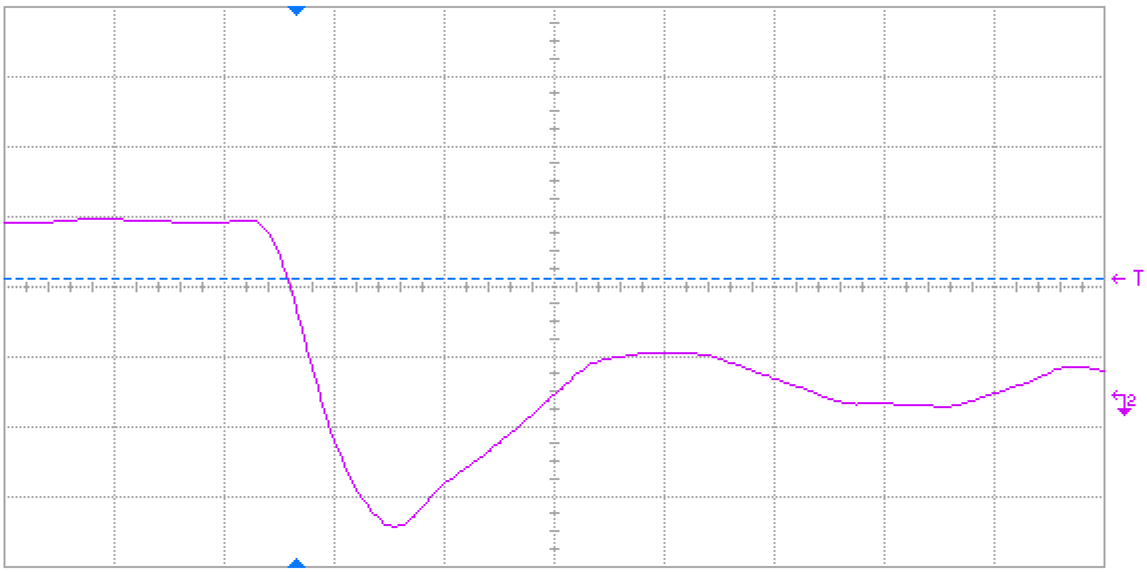


Figure 15(a) DUT 65878 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

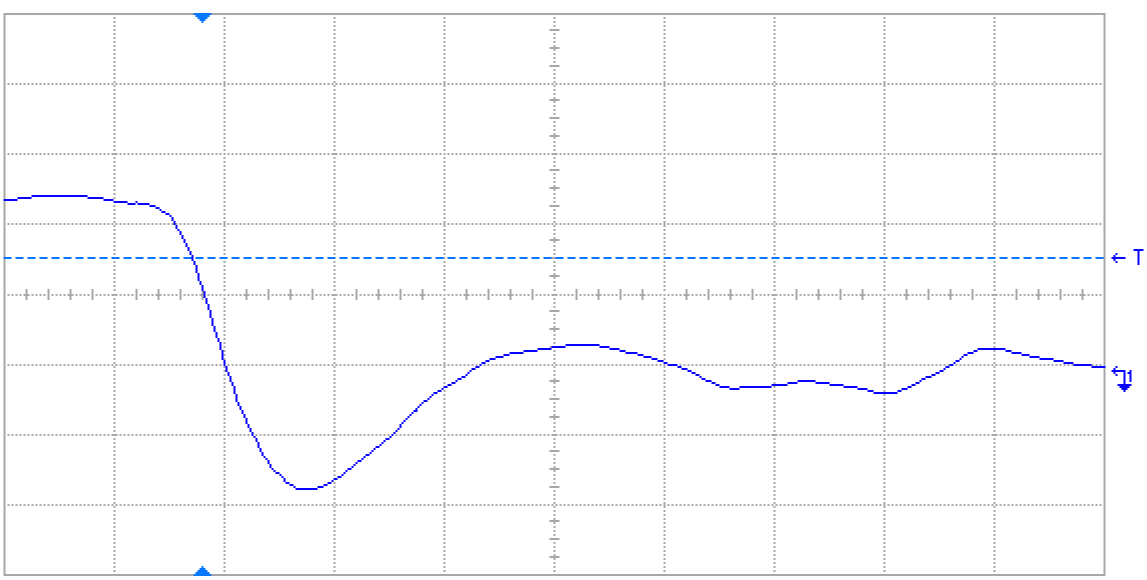


Figure 15(b) DUT 65878 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

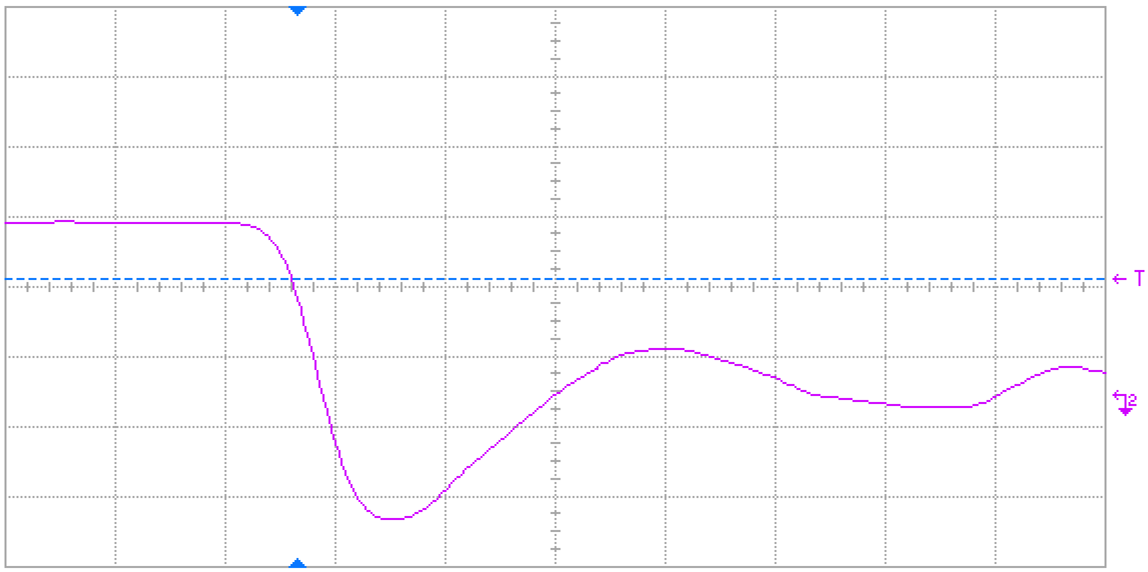


Figure 16(a) DUT 65891 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

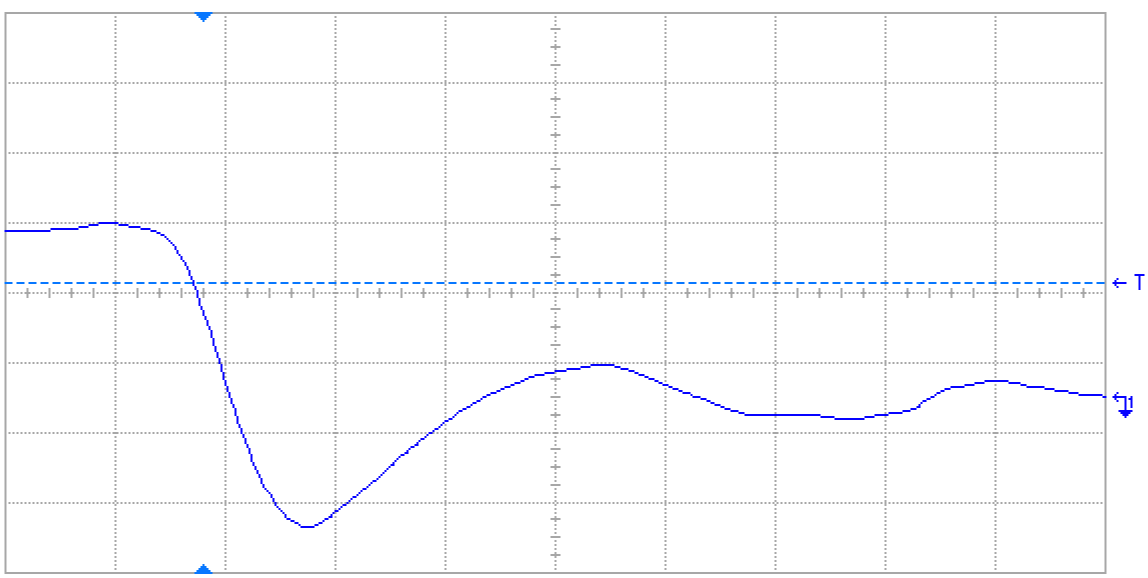


Figure 16(b) DUT 65891 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

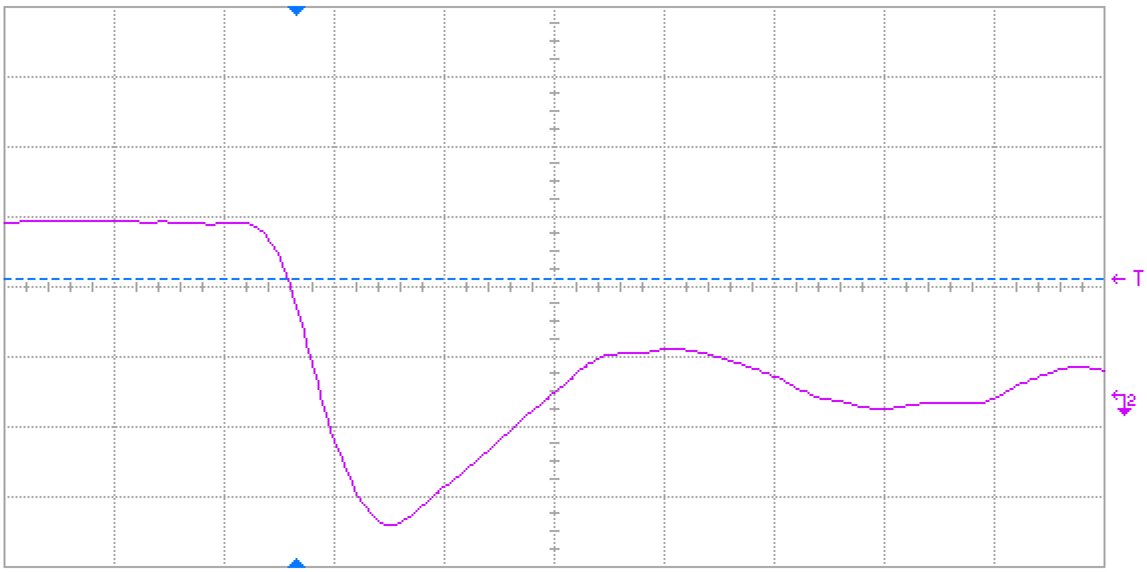


Figure 17(a) DUT 65907 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

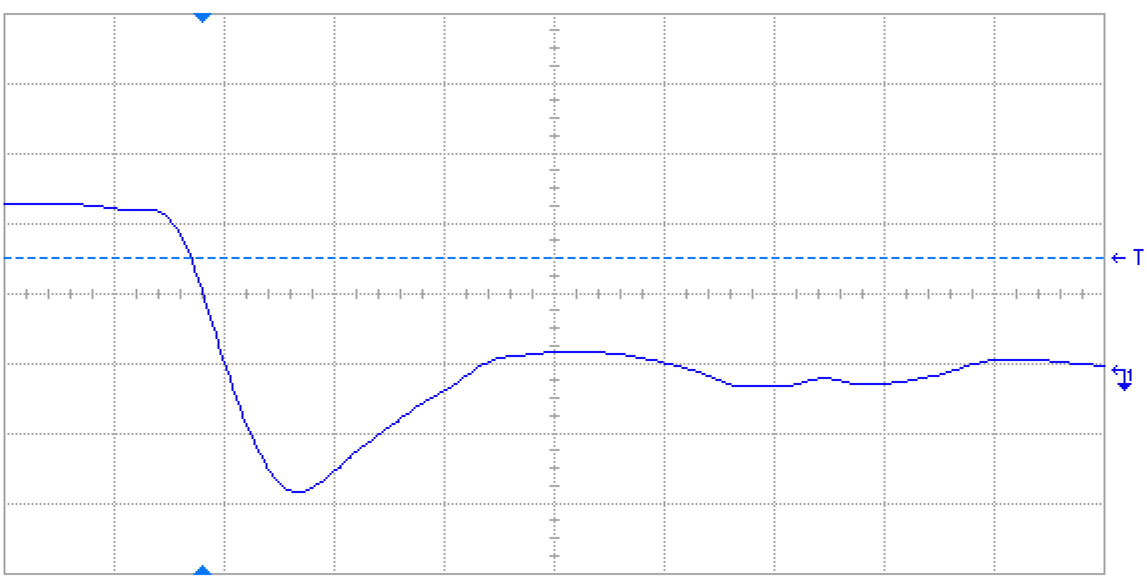


Figure 17(b) DUT 65907 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

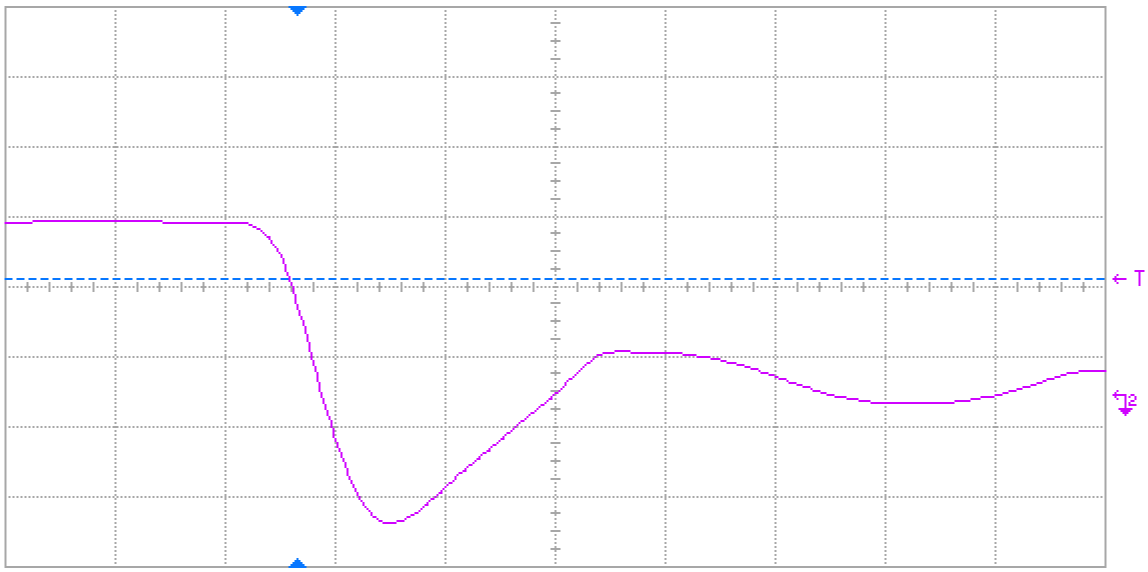


Figure 18(a) DUT 65981 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

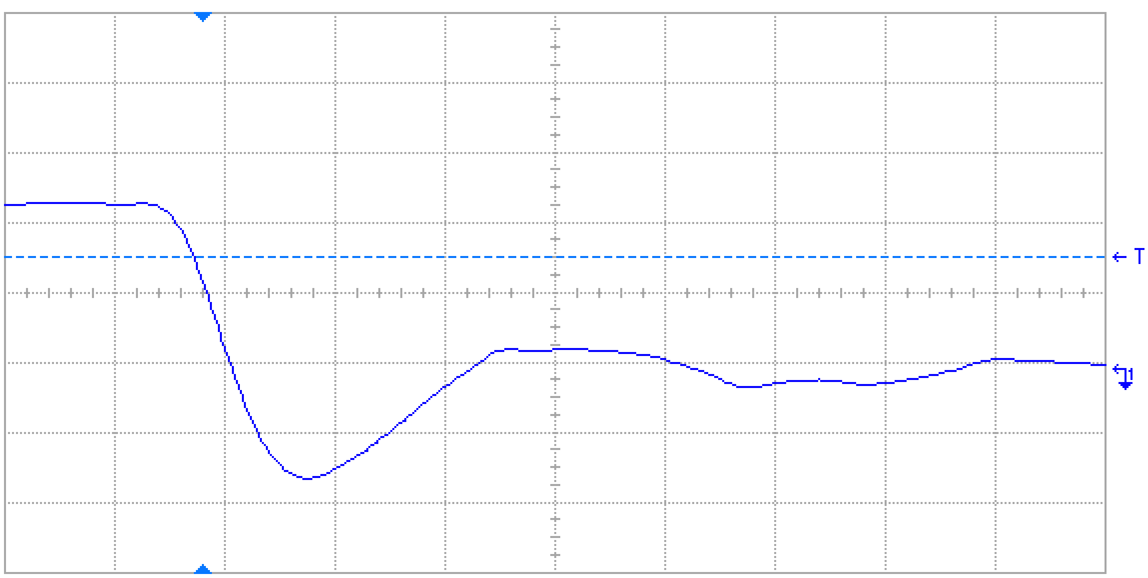


Figure 18(b) DUT 65981 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

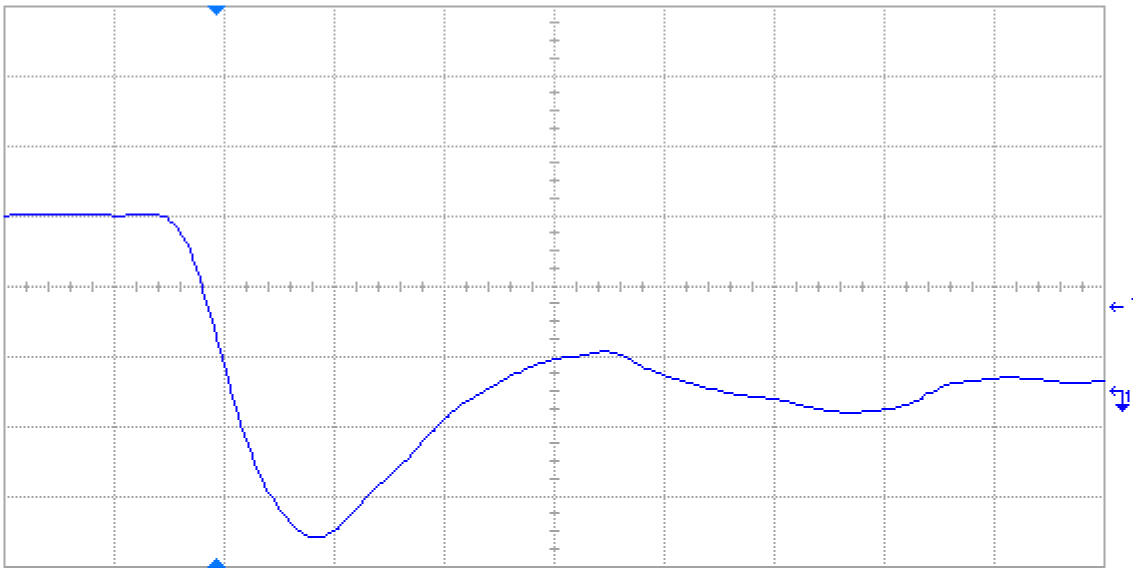


Figure 19(a) DUT 62926 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

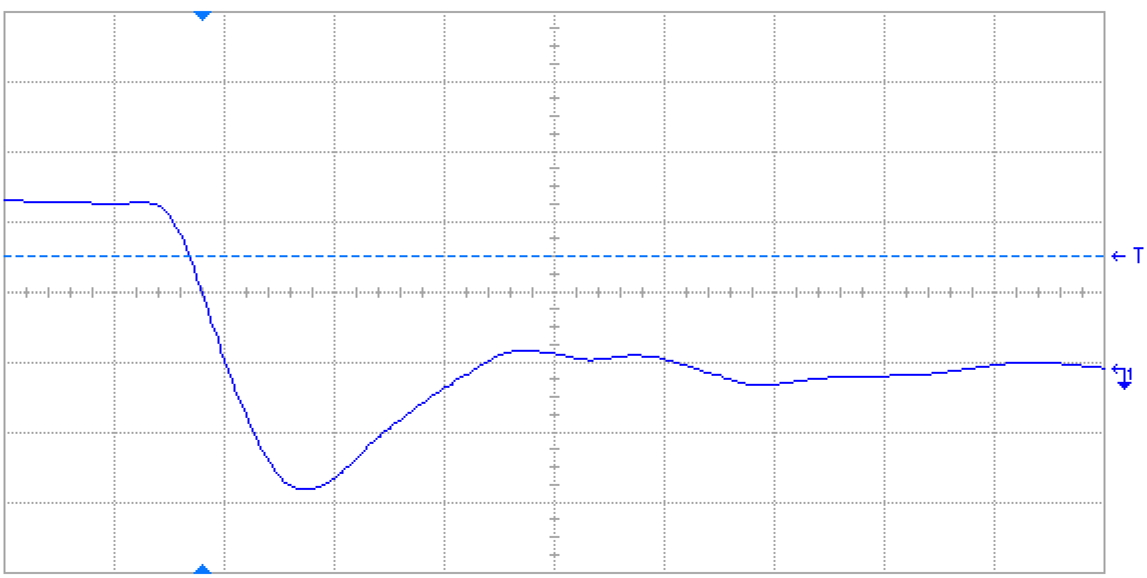
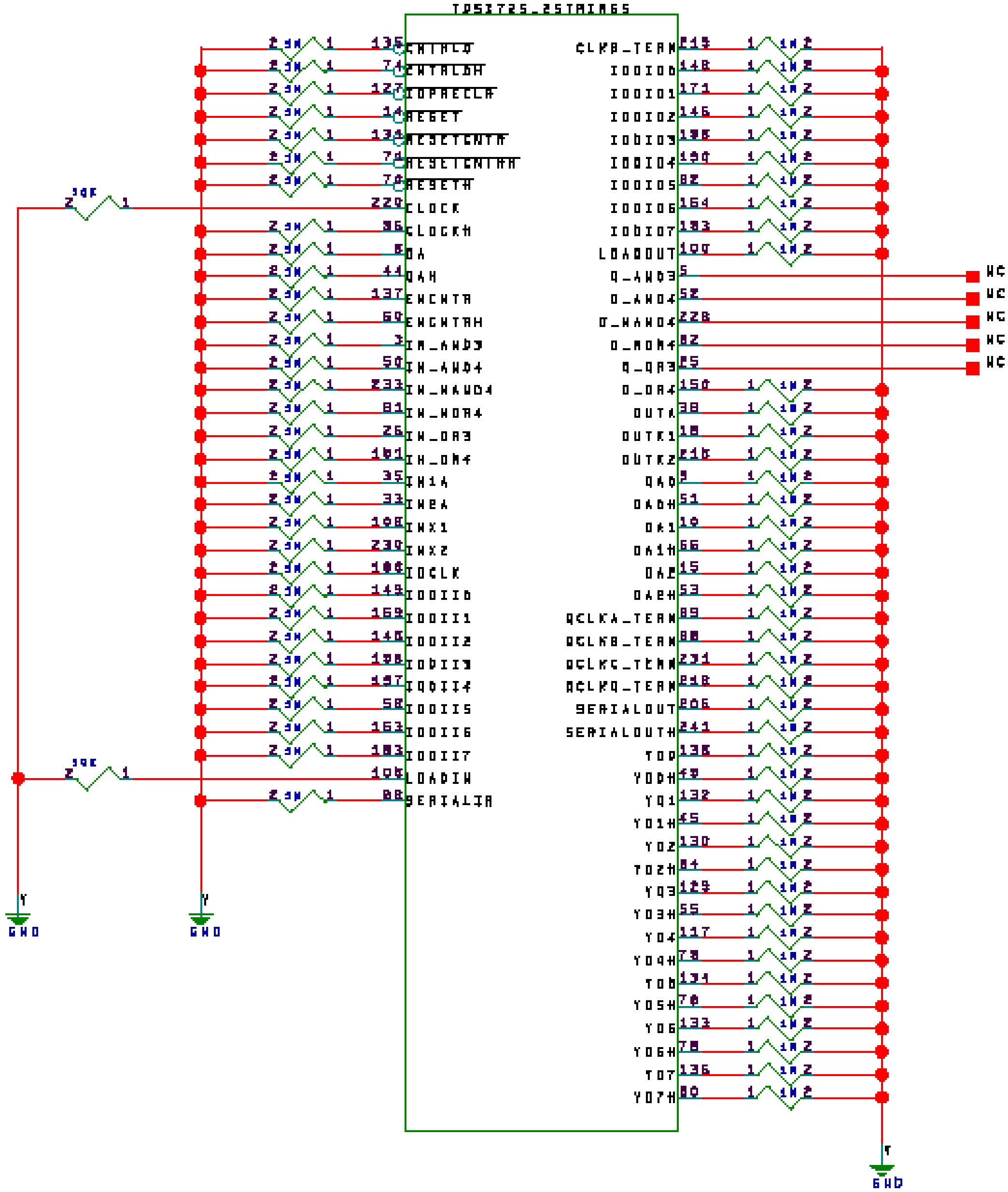
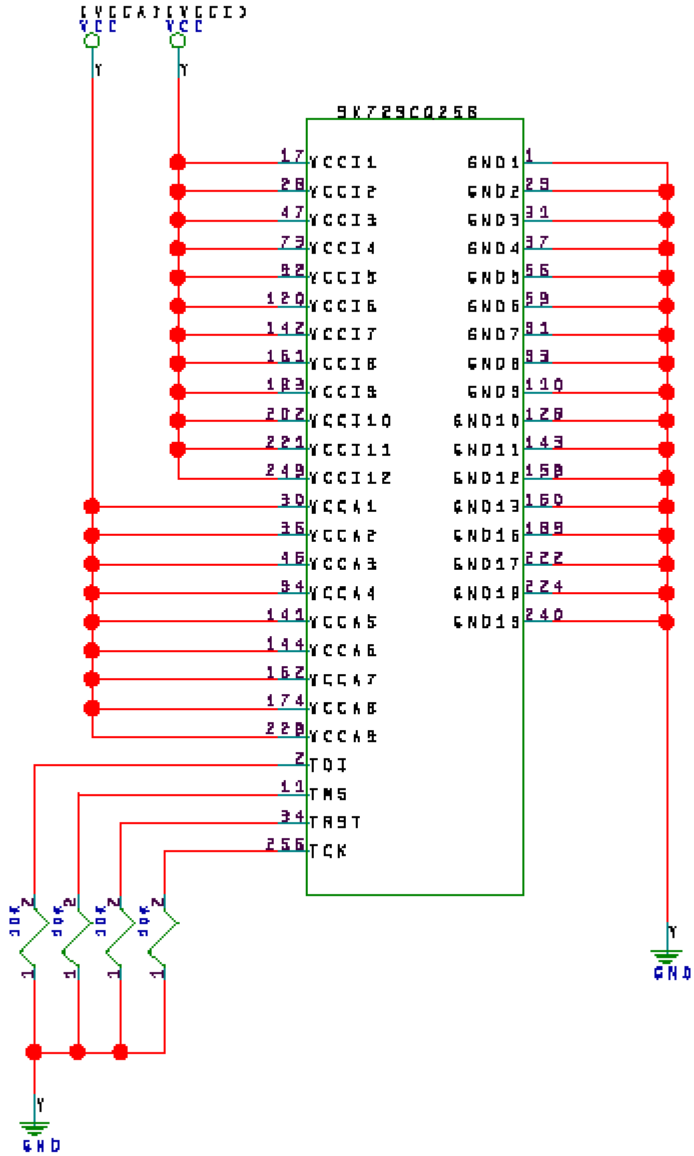


Figure 19(b) DUT 62926 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

APPENDIX A DUT BIAS





(VCCA)(VCCI)
VCC
VCC
9K729CQ256
VCCI1
VCCI2
VCCI3
VCCI4
VCCI5
VCCI6
VCCI7
VCCI8
VCCI9
VCCI10
VCCI11
VCCI12
VCCA1
VCCA2
VCCA3
VCCA4
VCCA5
VCCA6
VCCA7
VCCA8
VCCA9
TDI
TMS
TRST
TCK
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
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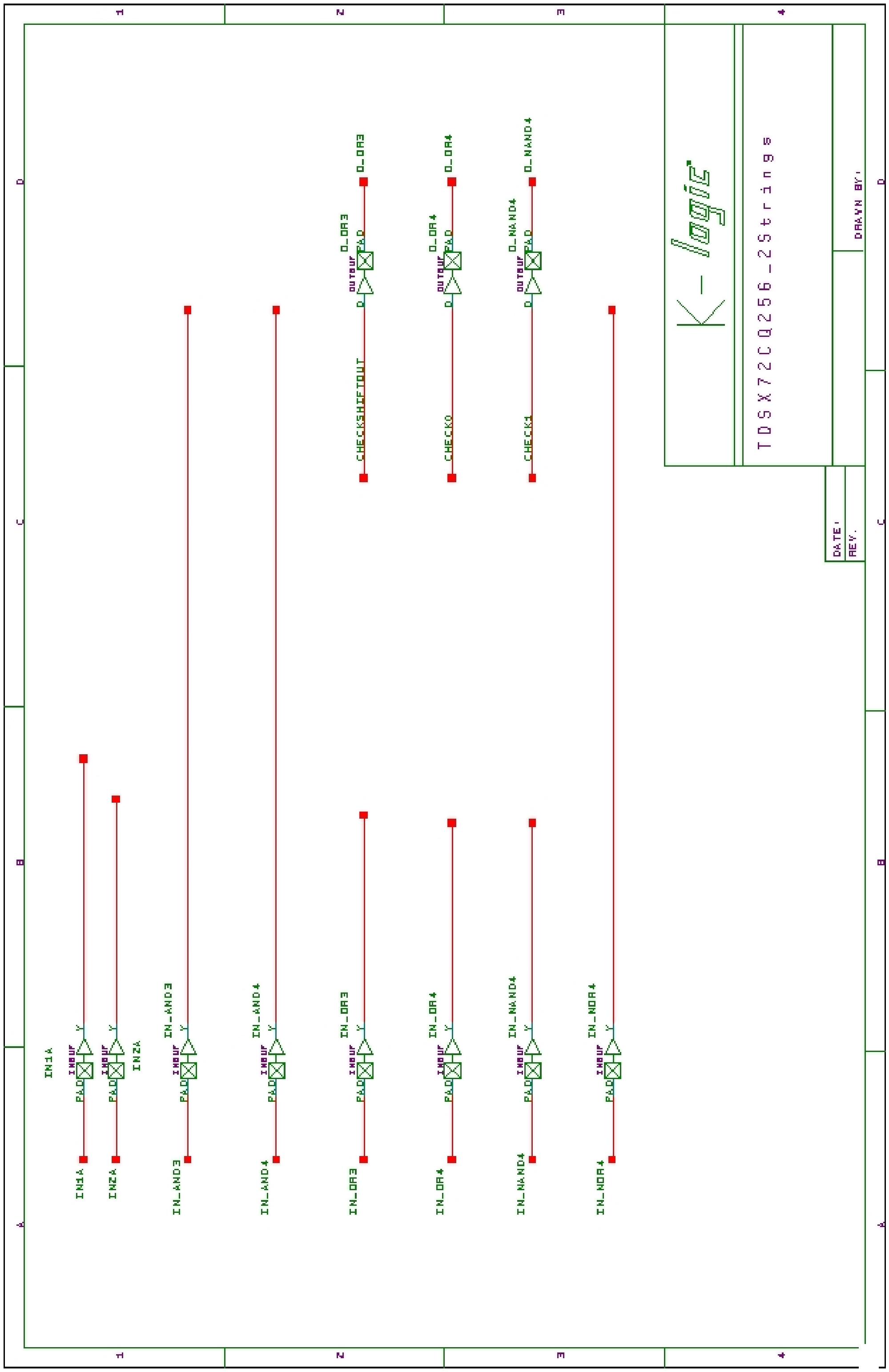
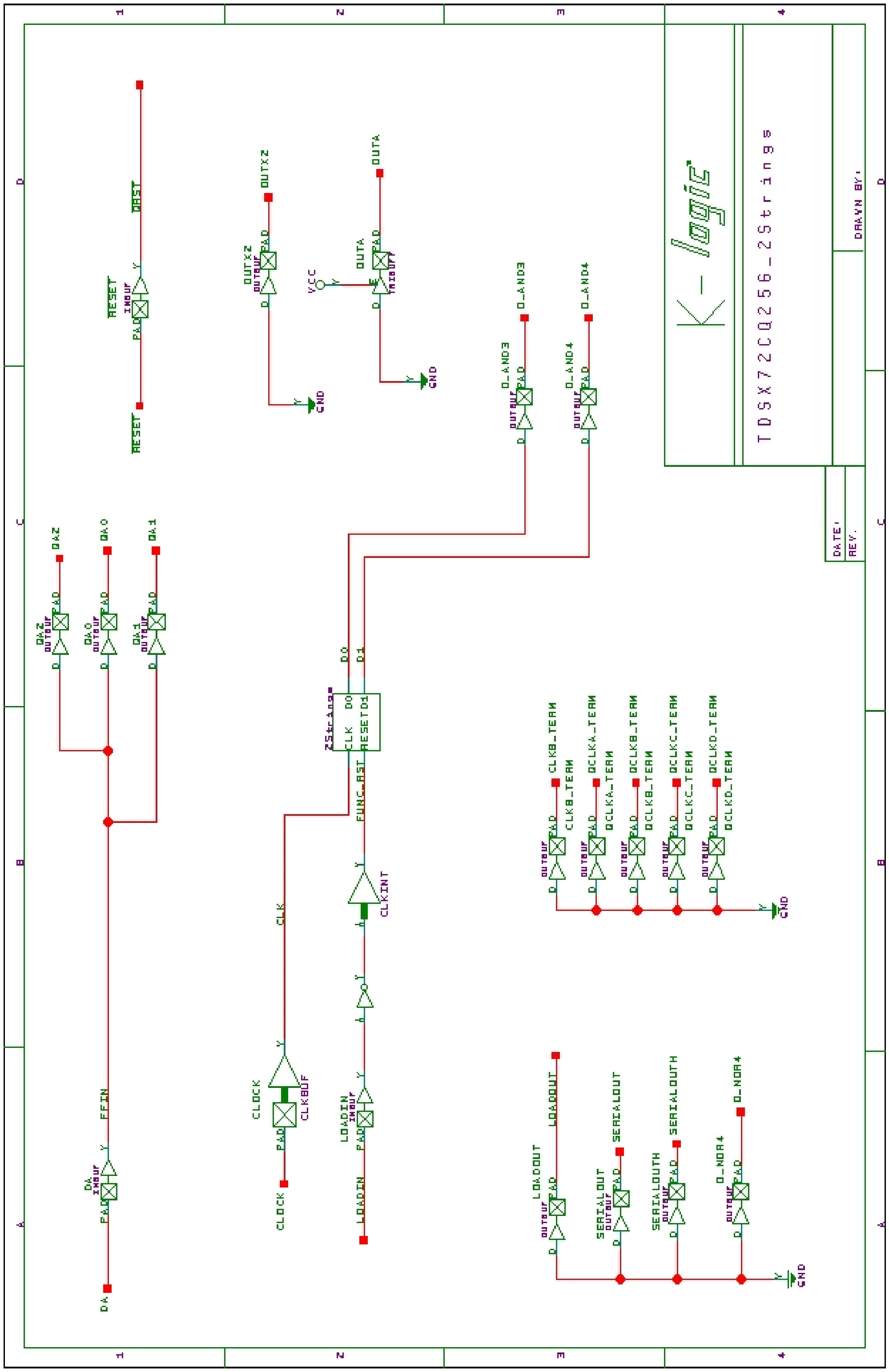
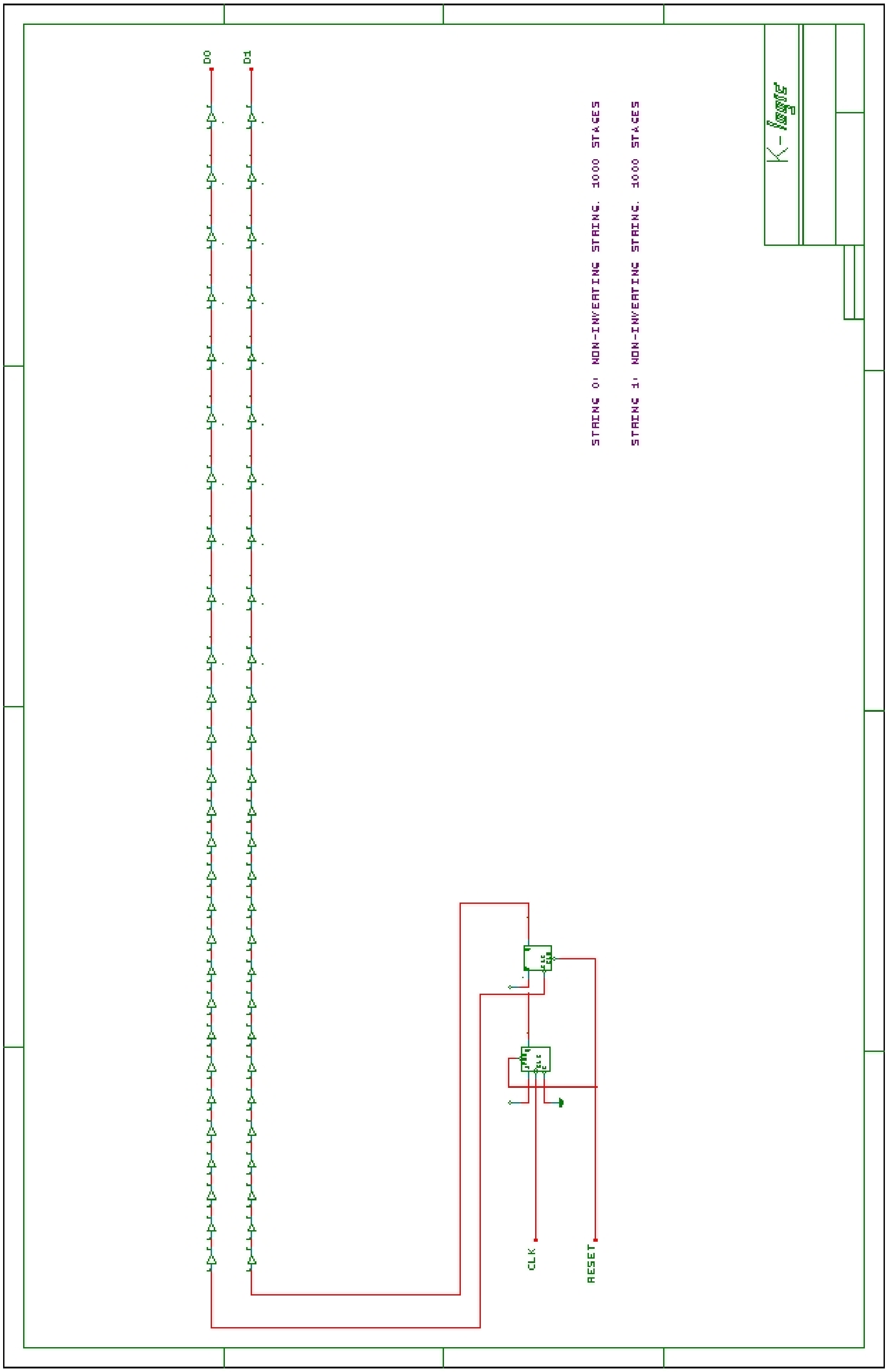
GND16
GND17
GND18
GND19
GND
GND

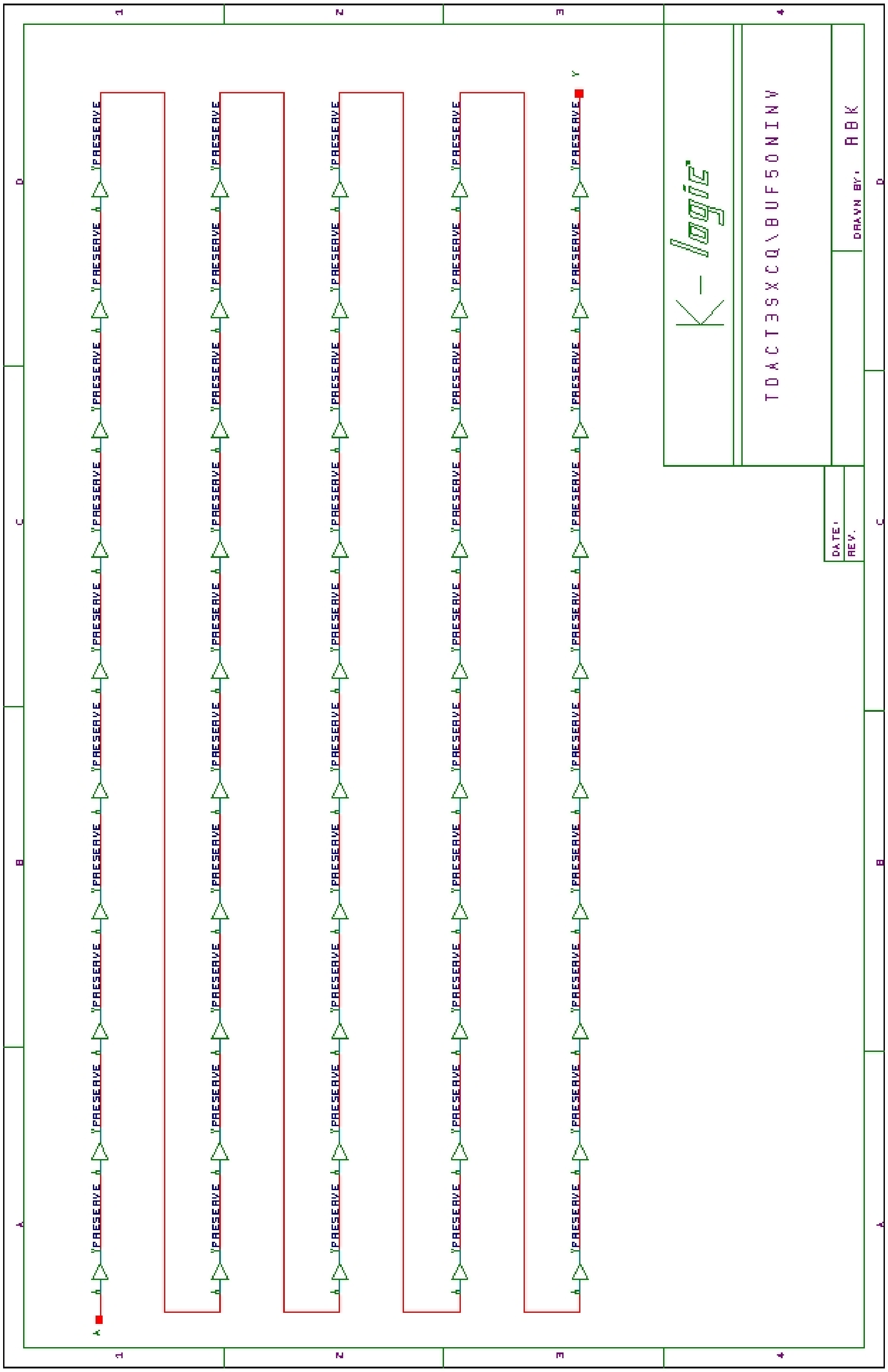
APPENDIX B DUT DESIGN SCHEMATICS



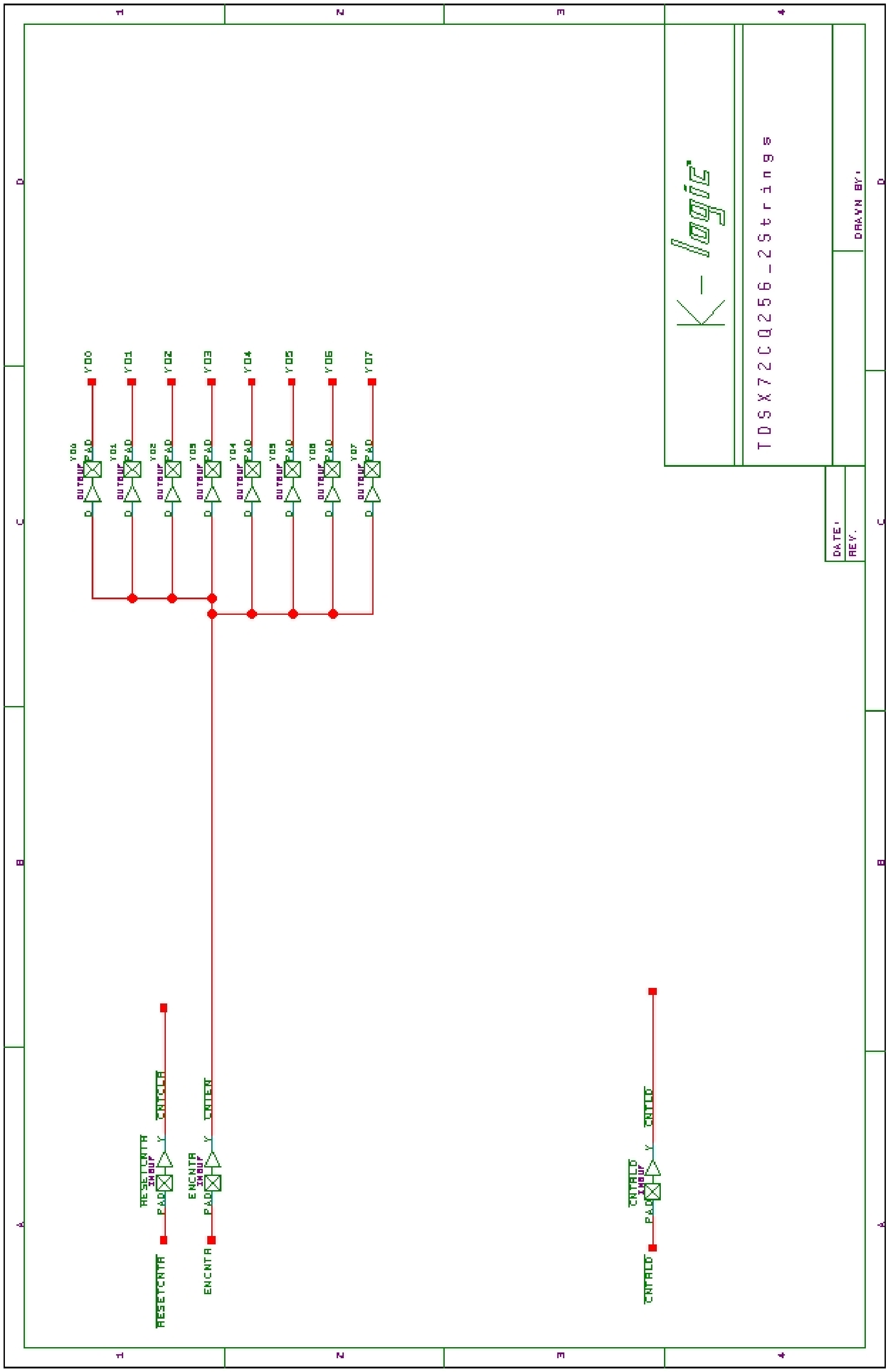


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
QRST
OUTX2
OUTA
VCC
GND
D_AND3
D_AND4
QA2
QA0
QA1
2Strings
CLK
D0
D1
RESET
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
DA
FFIN
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4
CLKB_TERM
QCLKA_TERM
QCLKB_TERM
QCLKC_TERM
QCLKD_TERM

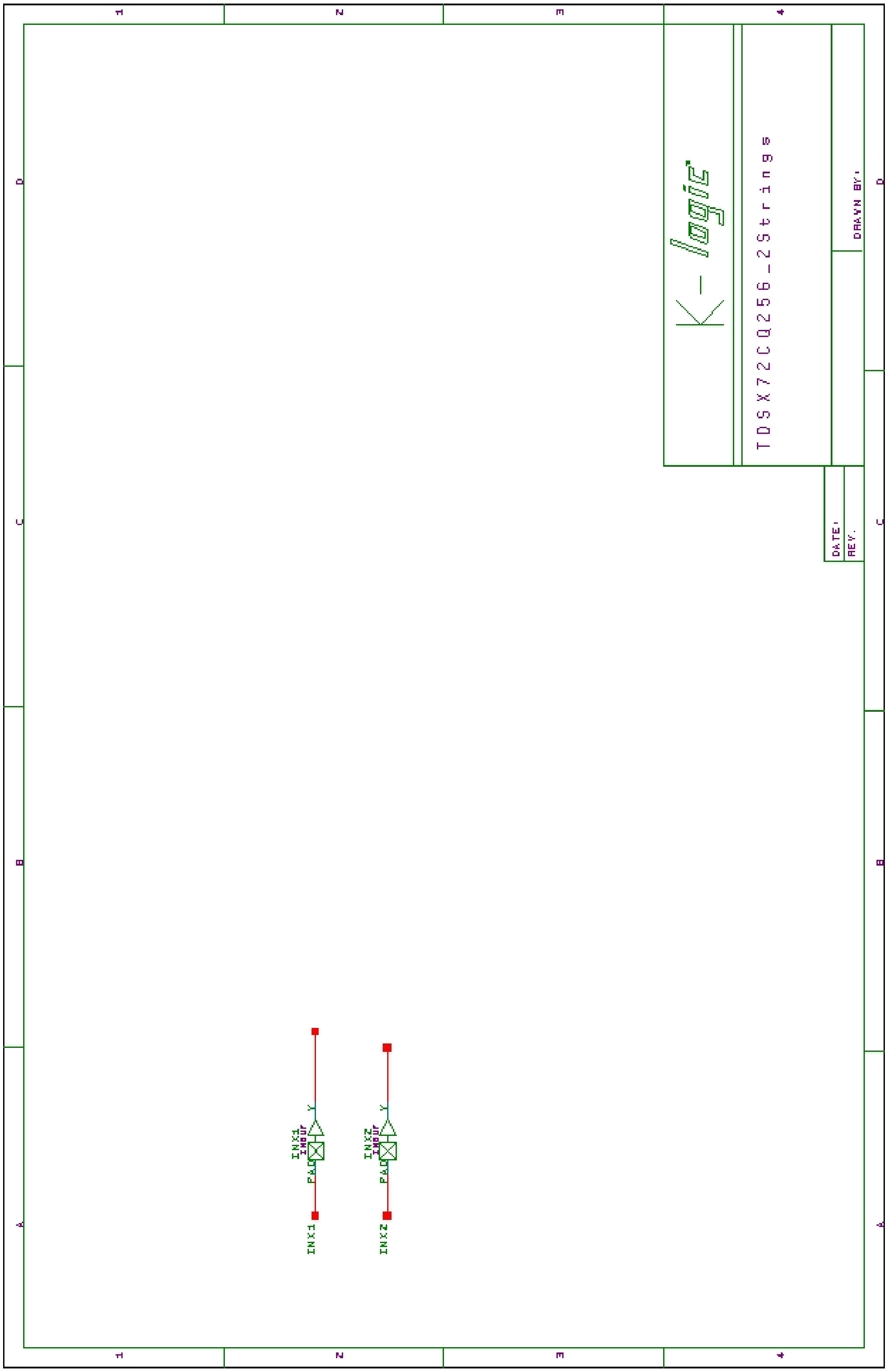

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
CLK
RESET



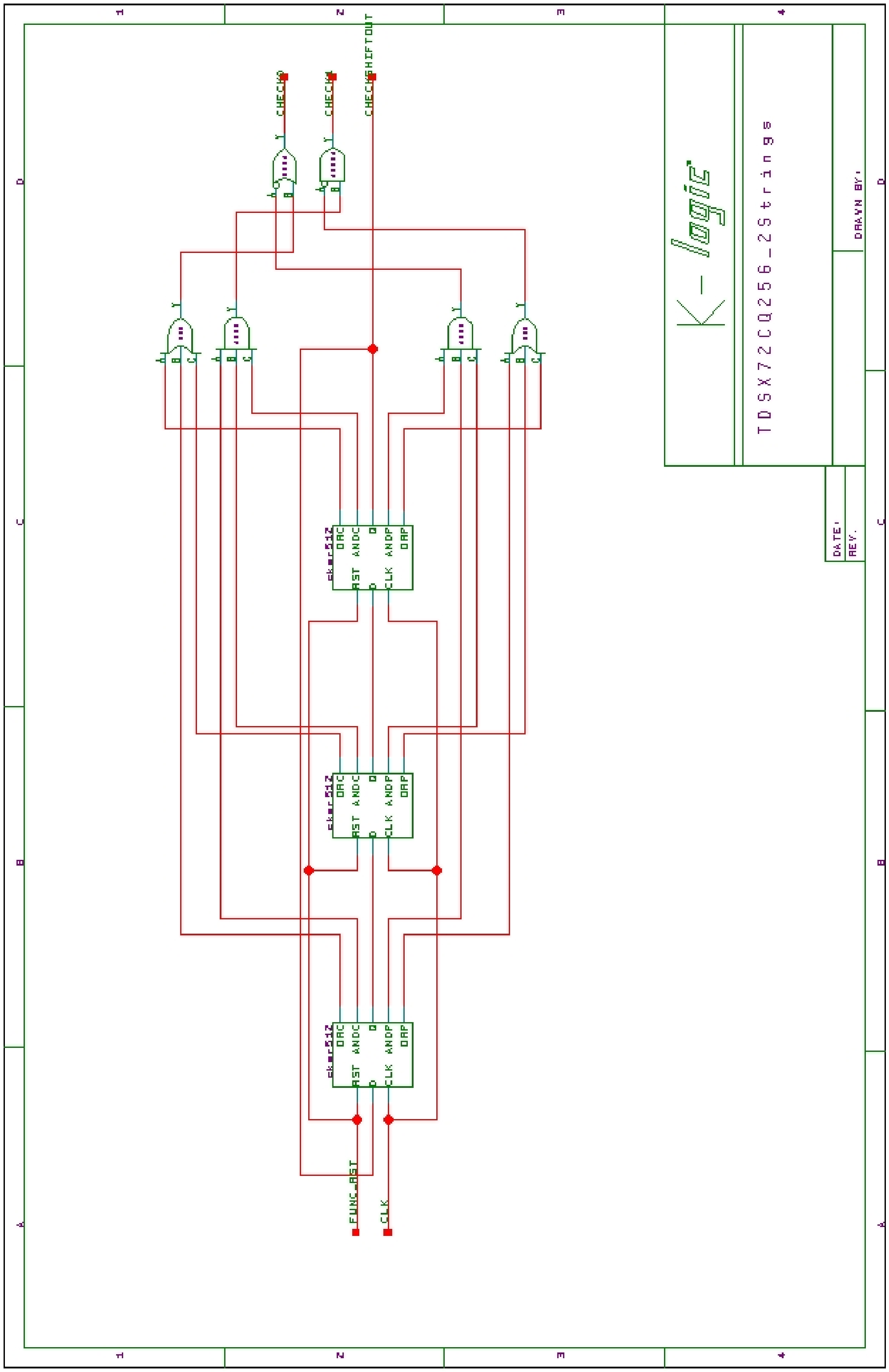
K-logic
TDACT3SXCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
PRESERVE
A
Y

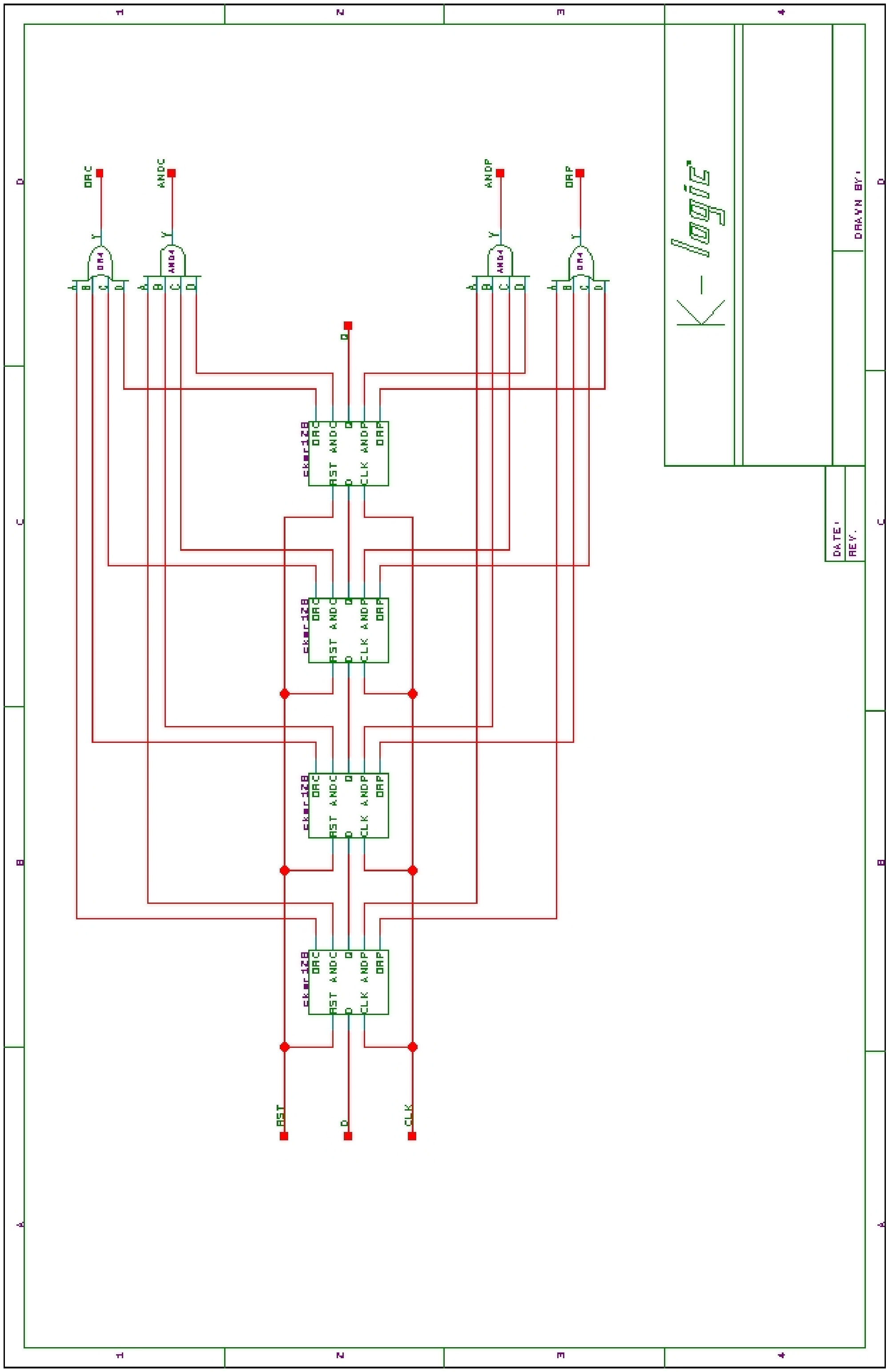


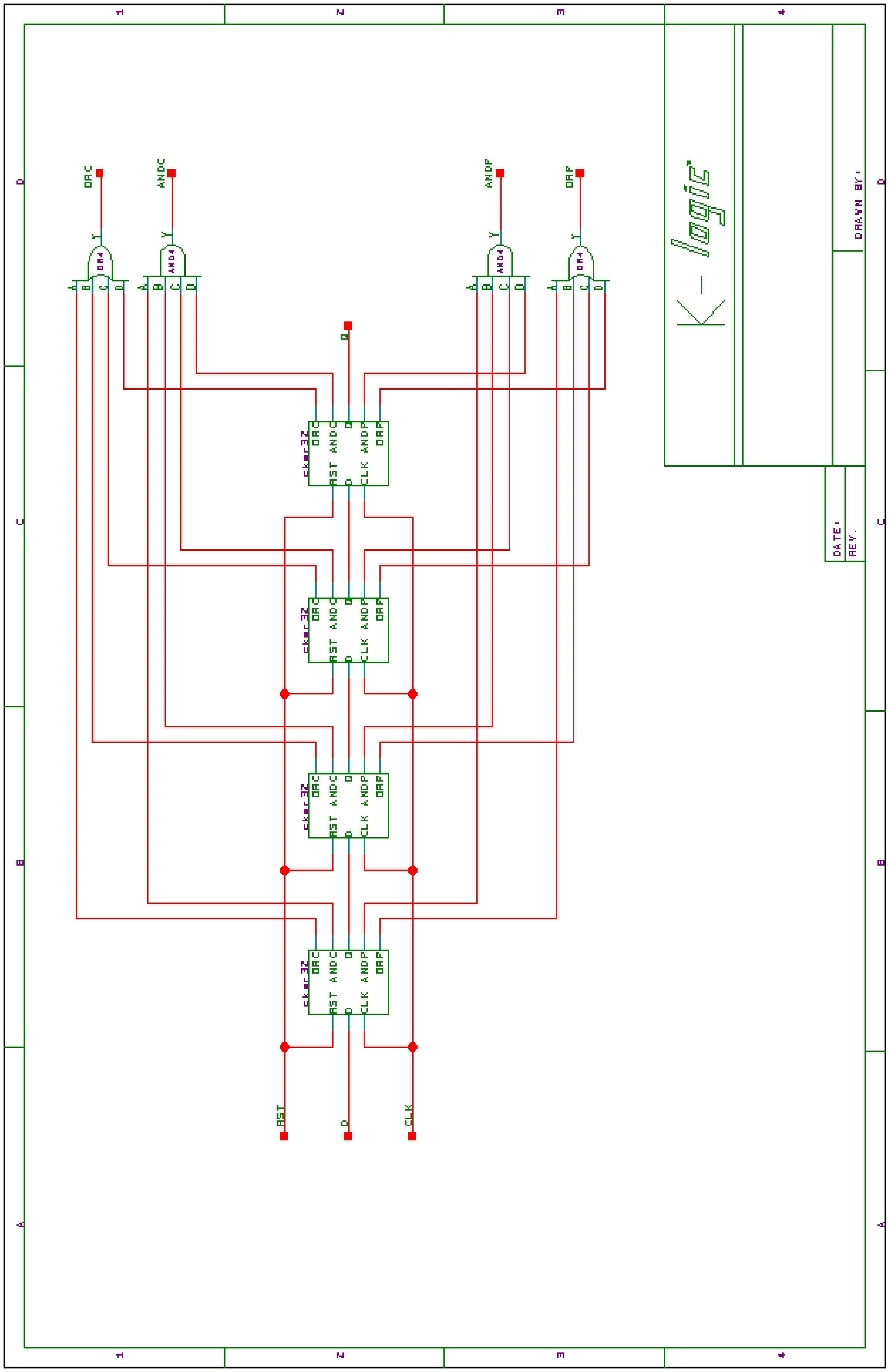
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
INBUF
RESETCNTA
ENCNTA
CNTALD

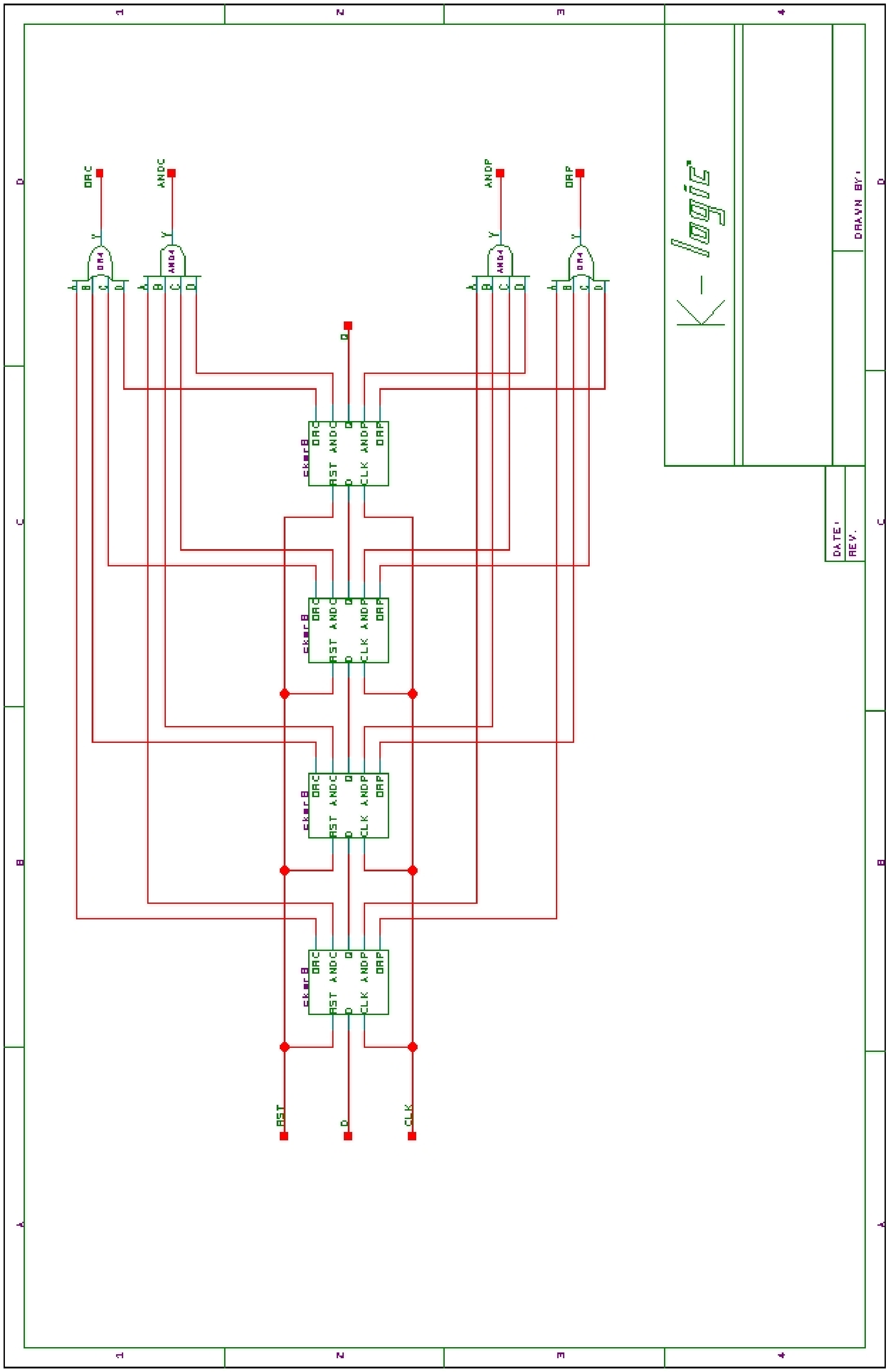


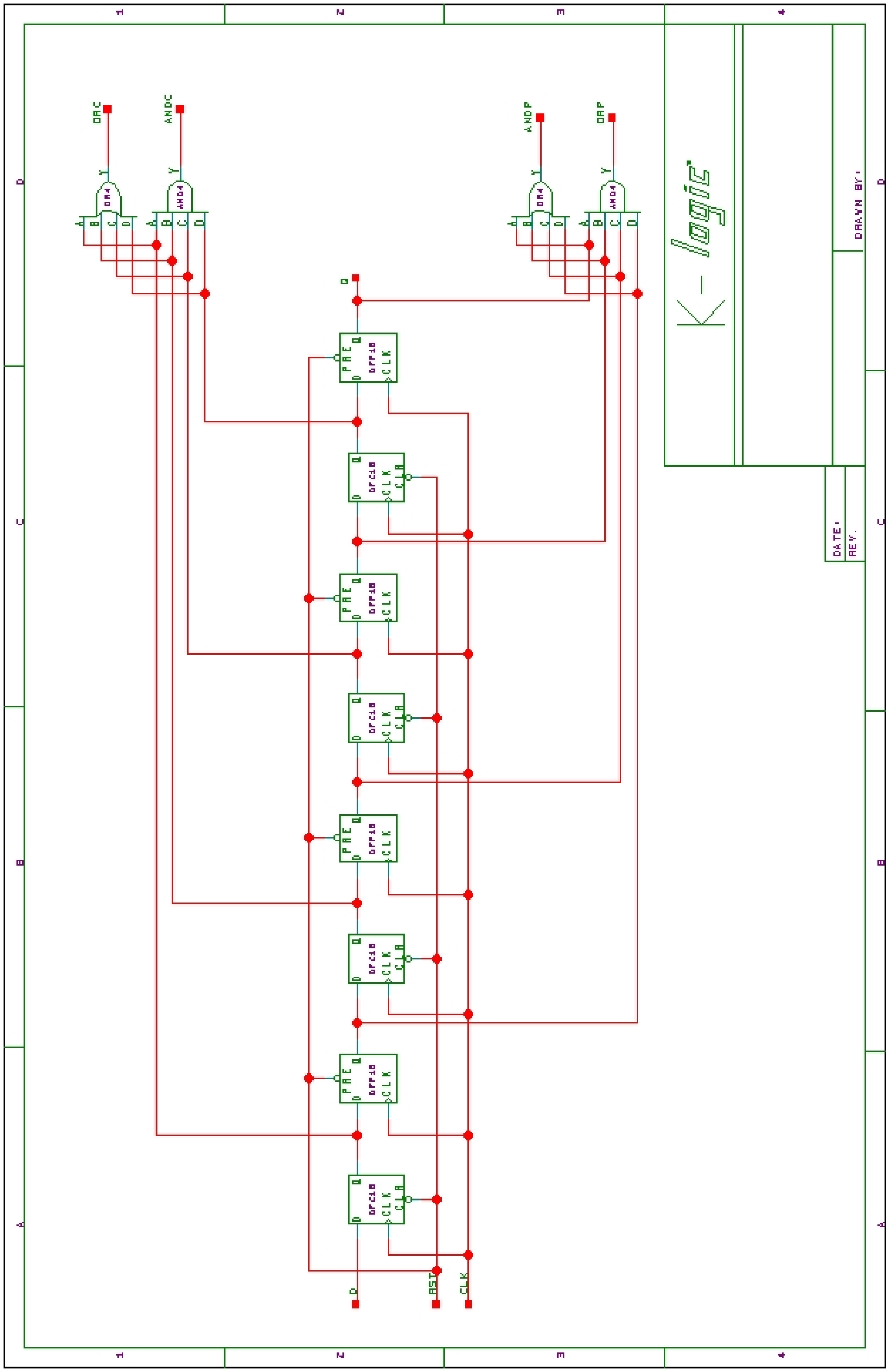
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2
INBUF
PAD
Y

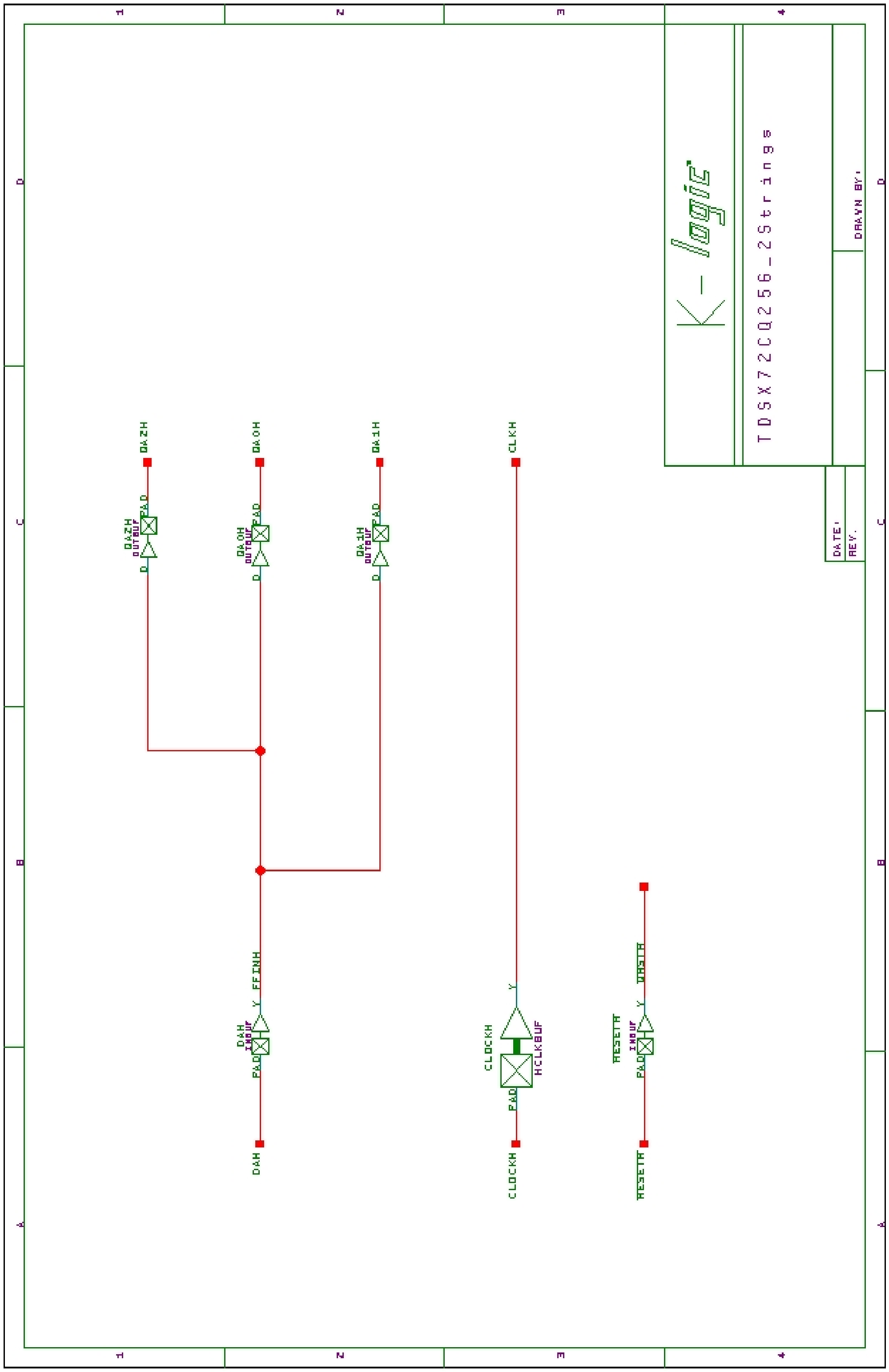

CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:

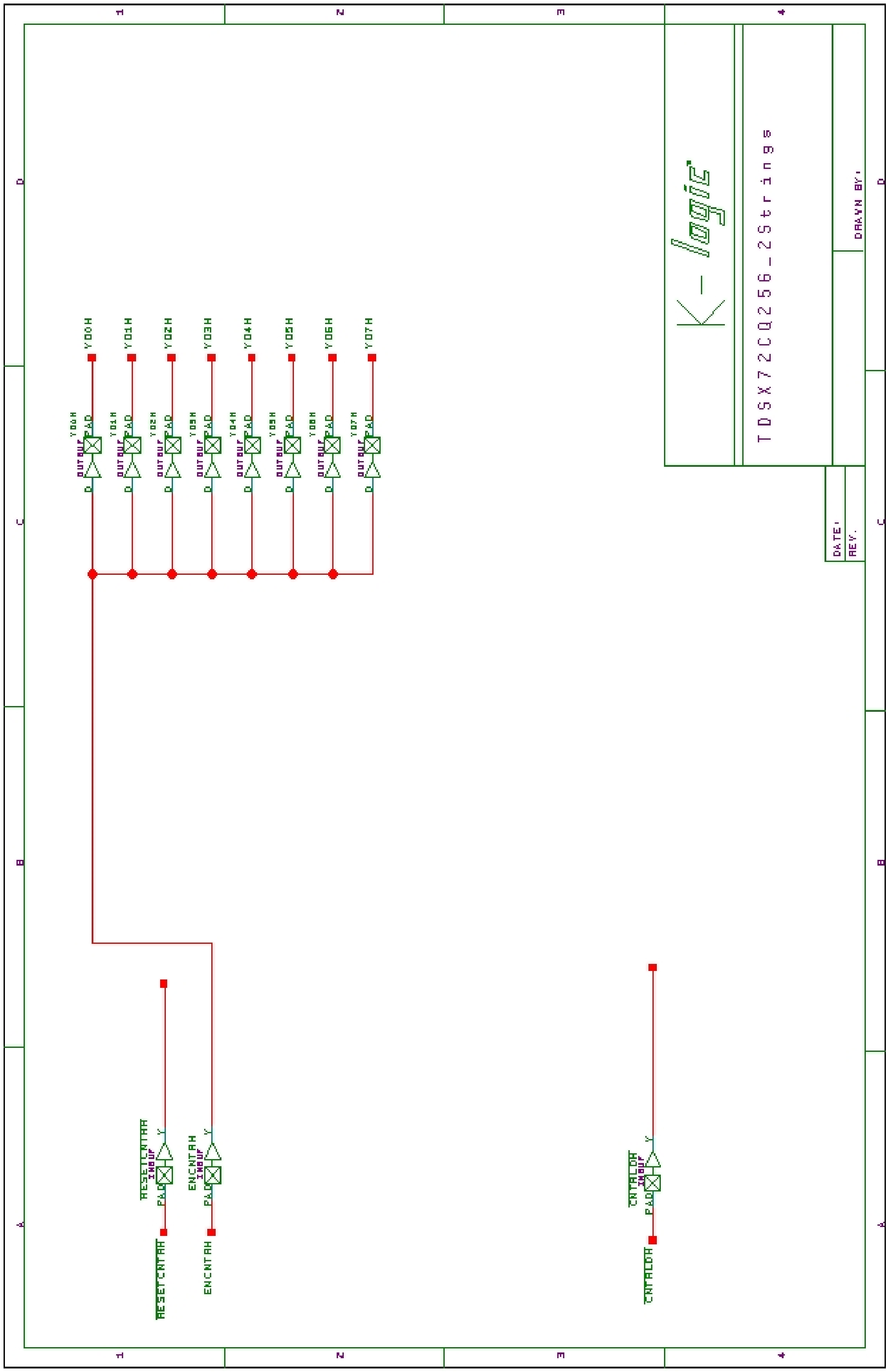

ORC
ANDC
ANDP
ORP
OR4
AND4
Y
A
B
C
D
ckmr128
RST
CLK
Q
K-logic
DRAWN BY:
DATE:
REV.

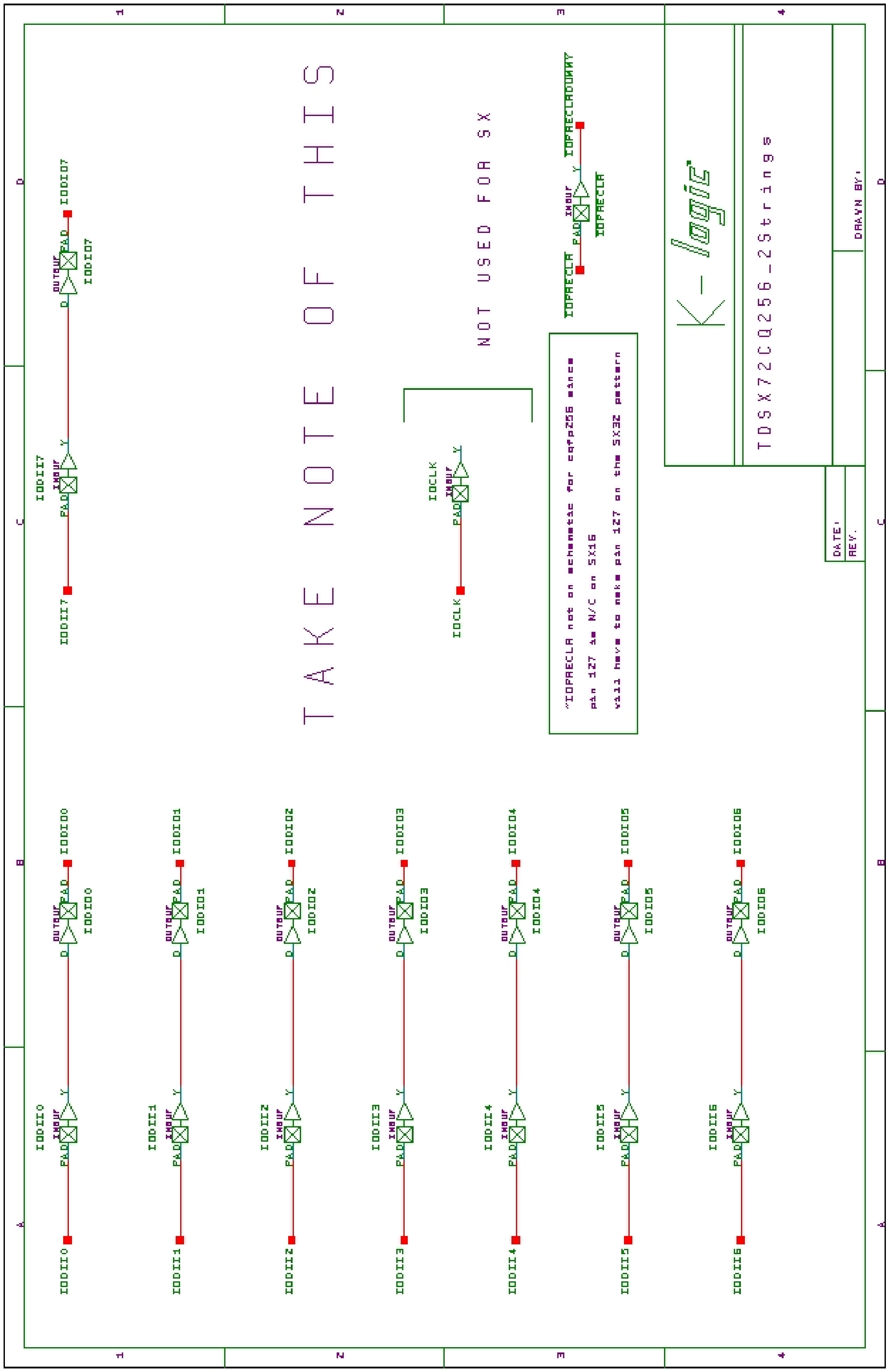

ORC
ANDC
ANDP
ORP
OR4
AND4
Q
ckmr32
RST
D
CLK
K-logic
DATE:
REV.
DRAWN BY:

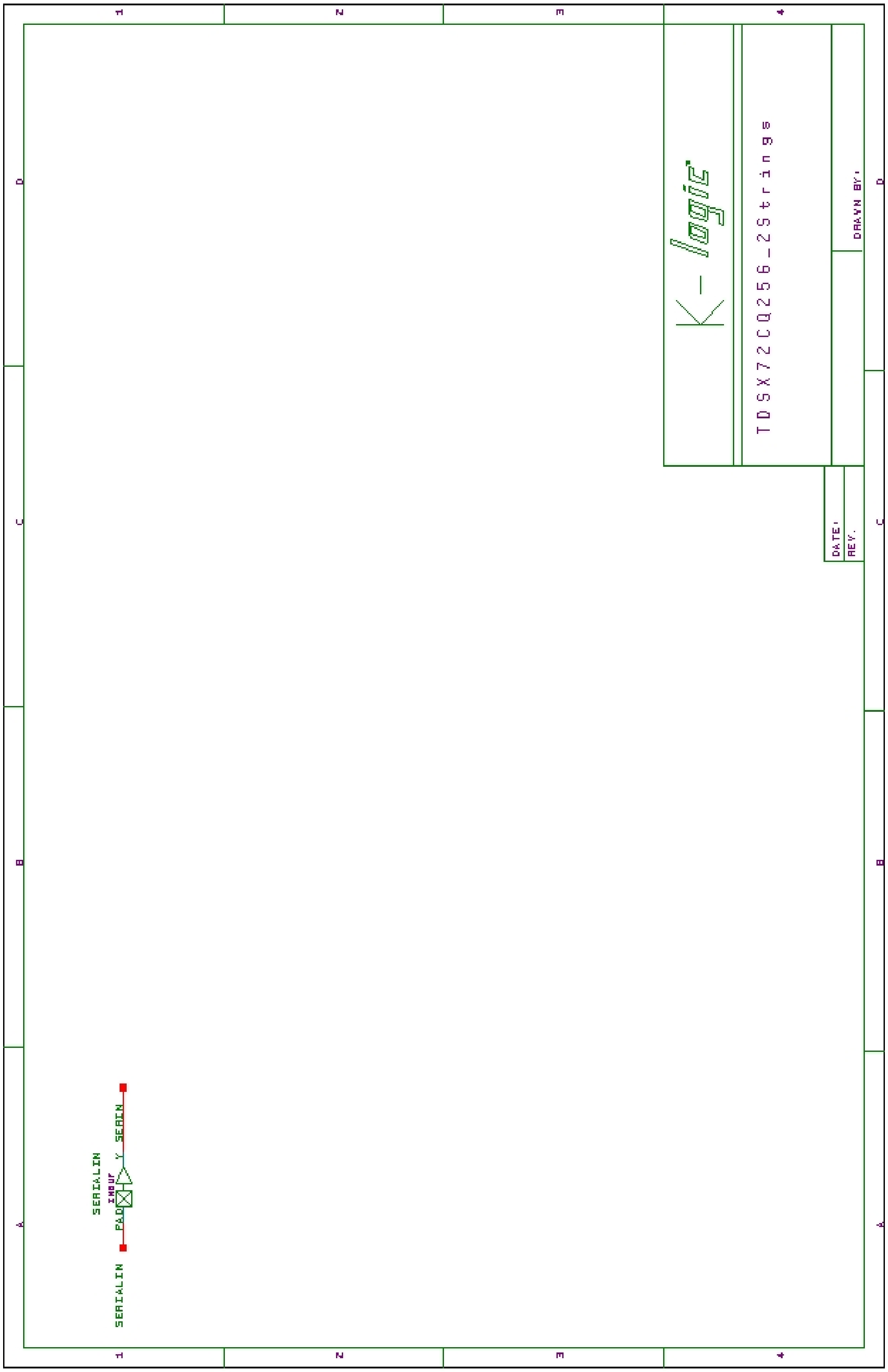

ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

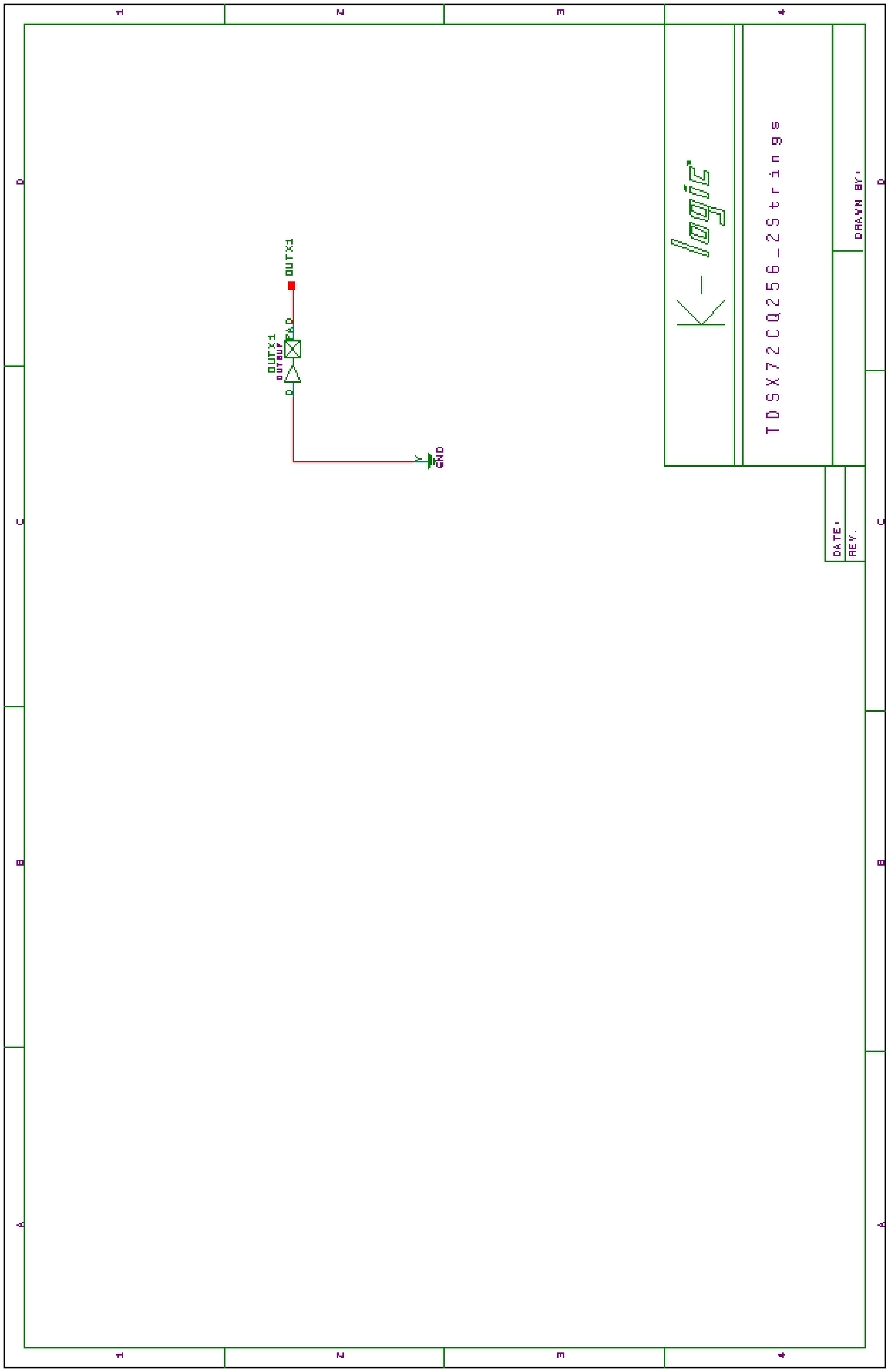

ORC
ANDC
ANDP
ORP
RST
CLK
K-logic
DRAWN BY:
DATE:
REV.


DA2H
DA0H
DA1H
CLKH
OUTBUF
PAD
D
DAH
INBUF
Y
FFINH
CLOCKH
HCLKBUF
RESETH
K-logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
OUTBUF
PAD
INBUF
RESETCNTAH
ENCNTAH
CNTALDH


TAKE NOTE OF THIS
NOT USED FOR SX
*IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
IOPRECLR
IOPRECLRDUMMY
IOCLK
IODII0
IODII1
IODII2
IODII3
IODII4
IODII5
IODII6
IODII7
IODIO0
IODIO1
IODIO2
IODIO3
IODIO4
IODIO5
IODIO6
IODIO7
INBUF
OUTBUF
PAD
K-logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
SERIALIN
PAD
IBUF
Y
SERIN


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
OUTX1
OUTBUF
PAD
GND