TOTAL IONIZING DOSE TEST REPORT

No. 04T-RT54SX32SU-D122H1
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si) after room temperature annealing
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 55 krad (Si) per 25-mA spec. Post 100 krad (Si) and after 15 days room temperature annealing: average I_{CCA} = 136.4 mA, and average I_{CCI} = 123.2 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 84 krad (Si) for 10% degradation criterion, post 100 krad degradation is 13.52%.
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to an automatic-tester measurement, the bench measurement offers lower noise, better accuracy and more flexibility. Although not every pin is sampled for some tests (e.g. threshold voltage measurement), the bench measurement is suitable to determine the total dose tolerance because either the I_{CC} or propagation delay always dominates the result.

A. Device Under Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RT54SX32SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX32CQFP256_2Strings
Die Lot Number	D122H1
Quantity Tested	5
Serial Number	49697, 49698, 49699, 49700, 49701
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

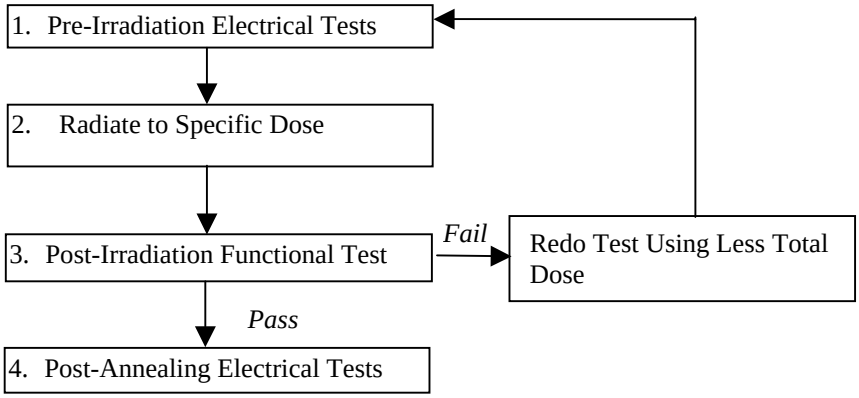


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. DUTs are biased annealed for 10 days after the 100-krad (Si) irradiation.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 616 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 512 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots of the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffer (pin DA to QA0)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (pin DA to QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. *Functionality*

Every DUT passes the pre-irradiation and post-irradiation-annealing functional tests.

B. *Power Supply Current (I_{CCA} and I_{CCI})*

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 6 basically show the radiation-induced leakage current. For every DUT, the logic array current, I_{CCA} exhibits a transition near 60 krad. This transition is due to the temporary degradation of the charge pump because the radiation-induced leakage current overloads the output of the charge pump. After the pump degrading to a certain voltage, the array logic changes to another state and logic outputs are disabled; this causes the I_{CCA} transition. However, the temporary degradation of the charge pump is only a testing artifact because the logic outputs recover after few hours of room temperature annealing.

By technicality, TM1019 doesn't allow further irradiation after disabling of the logic outputs. However, in this case, because the logic state of the DUT is still well defined, further irradiation is still valid. Every DUT was irradiated to 100 krad; after few hours of room temperature annealing, the logic outputs in every DUT were recovered.

The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data are compared with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	I_{CCA} (mA)		I_{CCI} (mA)	
	Post-rad	Post-ann	Post-rad	Post-ann
49697	332	77	256	129
49698	361	164	276	111
49699	324	172	247	102
49700	344	98	265	140
49701	335	171	261	134

An empirical equation is used to extract the tolerance for I_{CC} reaching 25-mA spec. The critical total dose ($\gamma_{critical}$) for a 10-year mission to induce I_{CC} to 25 mA is obtained from the equation:

$$I_{CCA}(\gamma_{critical}) \times 0.32 + I_{CCI}(\gamma_{critical}) \times 0.29 = 25mA$$

Where $I_{CCA}(\gamma)$ and $I_{CCI}(\gamma)$ are in-flux currents extracted from the raw data. Using the worst-case degradation, which belongs to DUT 49698 (Figure 6), the tolerance ($\gamma_{critical}$) is obtained as approximately 55 krad (Si). Since the total-dose-induced leakage current distributes uniformly across the whole chip and causes no other impact except the background DC current, this derived tolerance is very conservative.

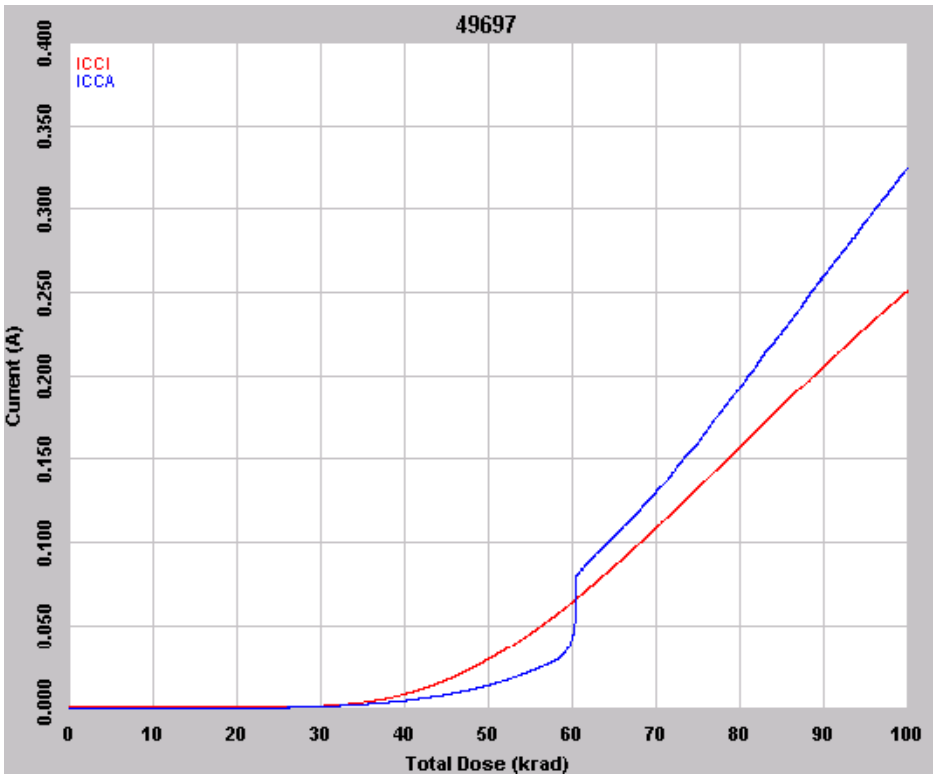


Figure 2 In flux I_{CCA} and I_{CCI} of DUT 49697, I_{CCA} shows a transition near 60 krad that indicates the temporary disabling of the outputs.

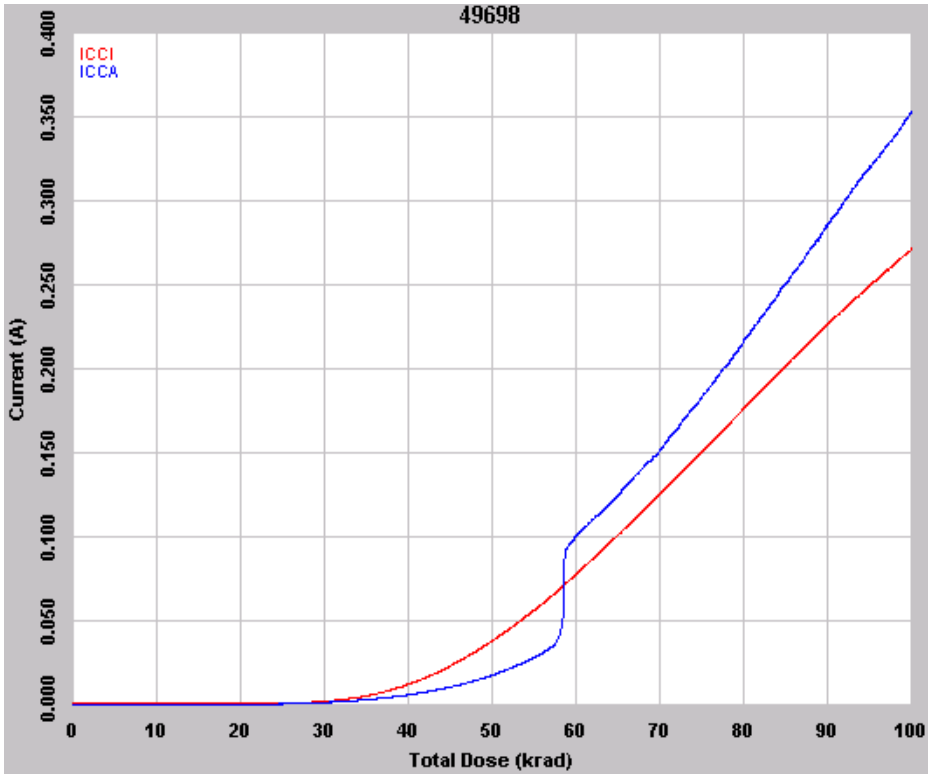


Figure 3 In flux I_{CCA} and I_{CCI} of DUT 49698, I_{CCA} shows a transition near 58 krad that indicates the temporary disabling of the outputs.

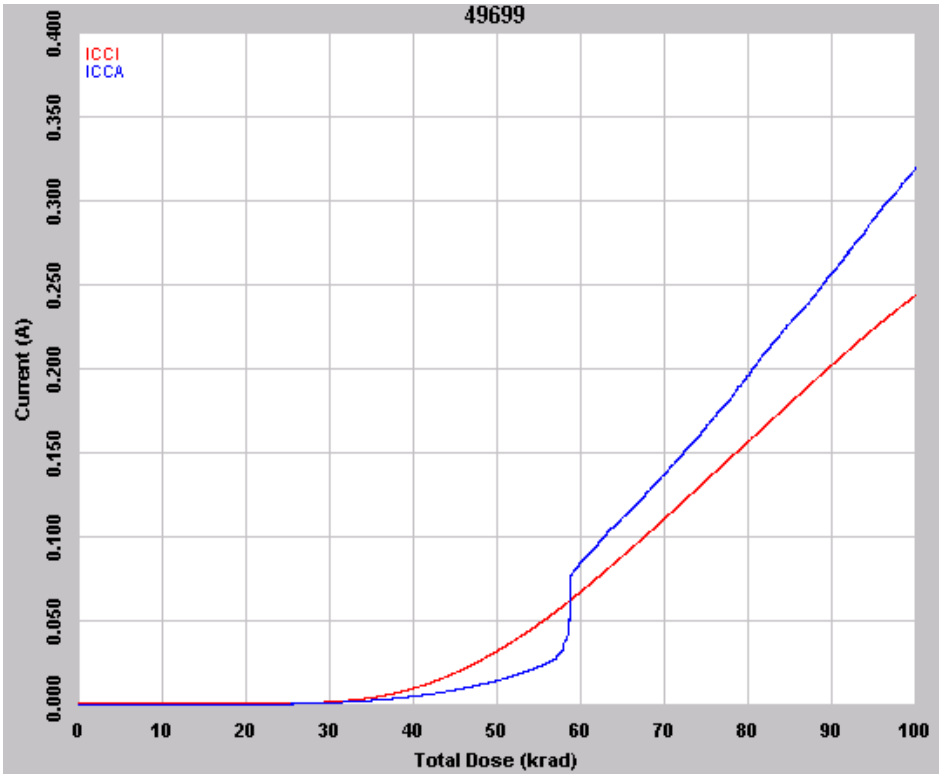


Figure 4 In flux I_{CCA} and I_{CCI} of DUT 49699, I_{CCA} shows a transition near 58.5 krad that indicates the temporary disabling of the outputs.

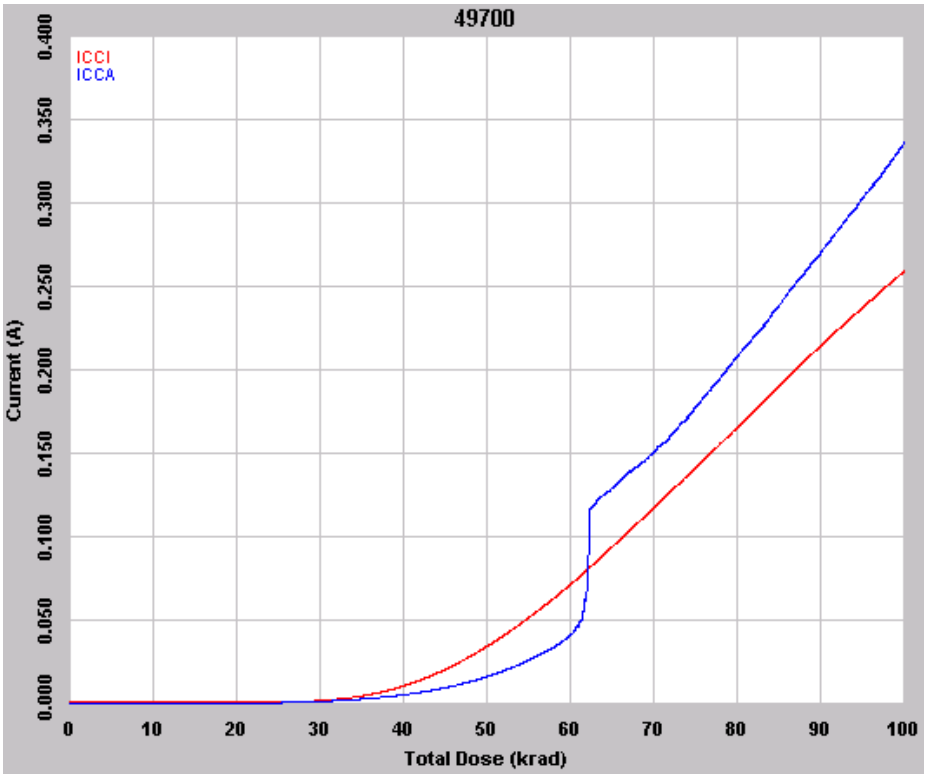


Figure 5 In flux I_{CCA} and I_{CCI} of DUT 49700, I_{CCA} shows a transition near 62 krad that indicates the temporary disabling of the outputs.

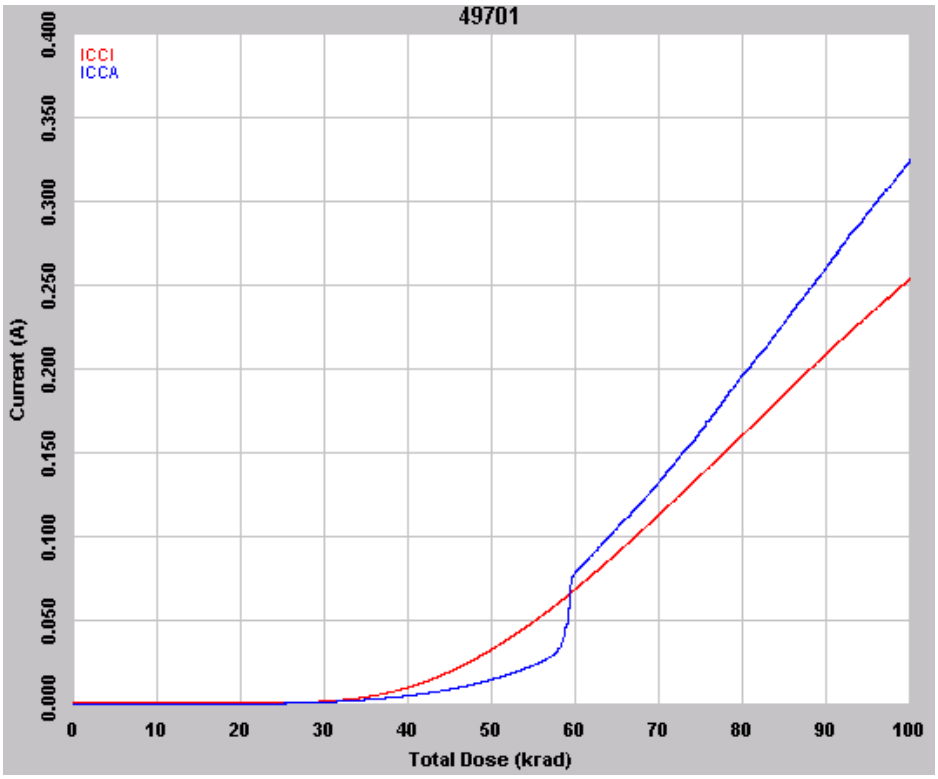


Figure 6 In flux I_{CCA} and I_{CCI} of DUT 49701, I_{CCA} shows a transition near 58 krad that indicates the temporary disabling of the outputs.

C. *Input Logic Threshold (V_{IL}/V_{IH})*

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits. Although DUT 49698 and 49701 have shifted more than 1 V after 100-krad irradiation and annealing, but it doesn't deteriorate the functionality of the devices. Since both DUTs have shifted to the center of V_{CCI}, the noise margin actually increased after irradiation and annealing. The thresholds of more than one pin were measured to verify that the shift is not due to artifact such as ESD during handling. Further annealing is in progress to investigate if this is a dose-rate effect.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds

DUT	Pre-Irradiation		Post-Annealing	
	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
49697	1.25	1.48	1.26	1.53
49698	1.24	1.48	2.29	2.52
49699	1.25	1.47	1.25	1.47
49700	1.25	1.49	1.23	1.51
49701	1.25	1.47	2.32	2.55

D. *Output-Drive Voltage (V_{OL}/V_{OH})*

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
49697	0.009	0.010	0.103	0.109	0.172	0.182	0.434	0.458	0.894	0.943
49698	0.009	0.010	0.102	0.108	0.169	0.179	0.428	0.451	0.881	0.930
49699	0.009	0.009	0.102	0.106	0.170	0.176	0.429	0.443	0.883	0.911
49700	0.009	0.009	0.103	0.104	0.171	0.174	0.432	0.439	0.891	0.906
49701	0.009	0.010	0.103	0.107	0.171	0.177	0.432	0.447	0.890	0.922

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
49697	4.98	4.98	4.87	4.85	4.66	4.64	4.12	4.06	2.97	2.78
49698	4.98	4.98	4.87	4.86	4.66	4.64	4.12	4.04	2.96	2.48
49699	4.98	4.98	4.87	4.86	4.66	4.65	4.12	4.07	2.97	2.78
49700	4.98	4.99	4.86	4.87	4.66	4.66	4.11	4.09	2.93	2.84
49701	4.98	4.99	4.87	4.87	4.67	4.65	4.13	4.07	2.98	2.80

E. *Propagation Delay*

Table 7 lists the pre-irradiation and post-annealing propagation delays and the radiation-induced degradations in percentage. To extract the 10% degradation tolerance, a piece-wise linear approximation based on empirical curve fitting is used. The piece-wise linear curve has two regions, region 1 from 0 krad(Si) to 40 krad(Si) has 0% degradation, and region 2 from 40 krad(Si) to 100 krad(Si) has a slope defined in the equation,

$$Slope = \frac{TPD(Max\ Dose) - TPD(Initial)}{Maximum\ Dose - 40krad}$$

TPD is the propagation delay in percentage. To be conservative, TPD(Max Dose = 100 krad) uses the worst degradation of 13.52% in DUT 49701. The tolerance is obtained as 84 krad, which corresponds to 10% degradation on the linear curve in region 2.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Pre-Irradiation	Post-Annealing	Degradation
49697	566.95	630.29	11.22%
49698	570.02	637.70	11.94%
49699	560.97	613.50	9.42%
49700	568.93	636.36	11.90%
49701	571.46	648.33	13.52%

F. Transition Time

Figures 7 to 16 show the post-annealing transition rising and falling edges. These waveforms show no observable radiation induced degradations.

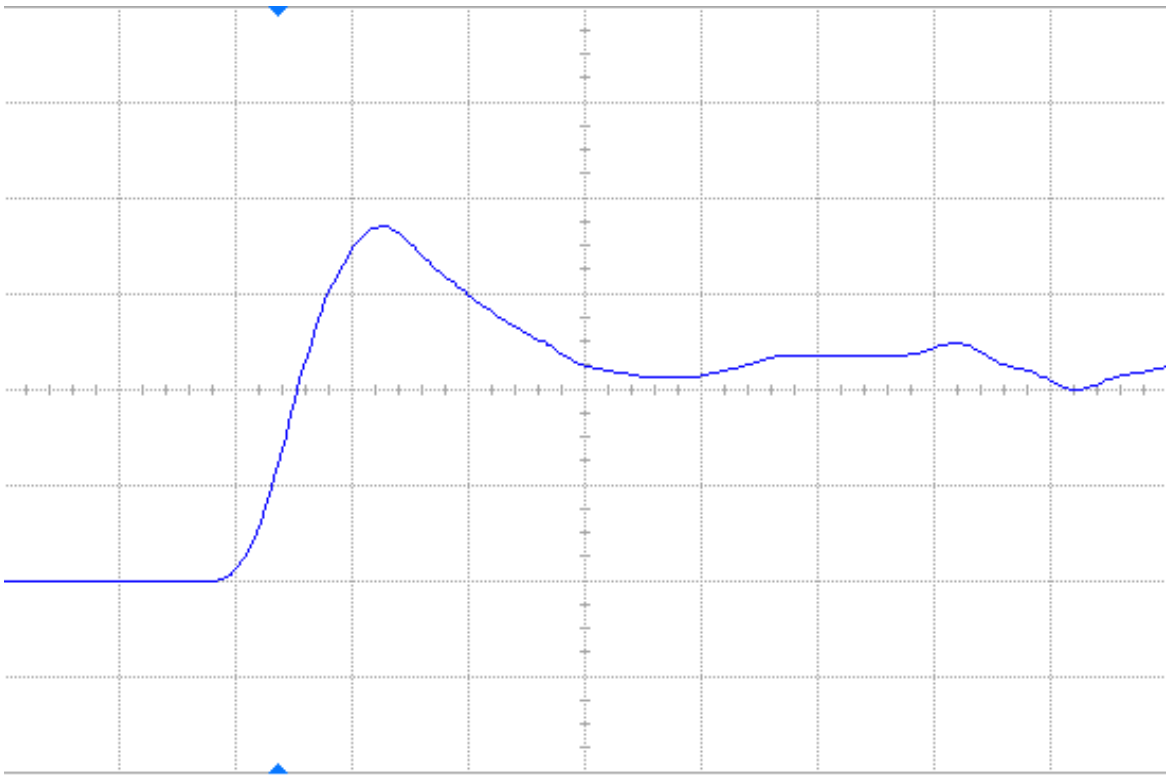


Figure 7 Post-annealing rising edge of DUT 49697, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

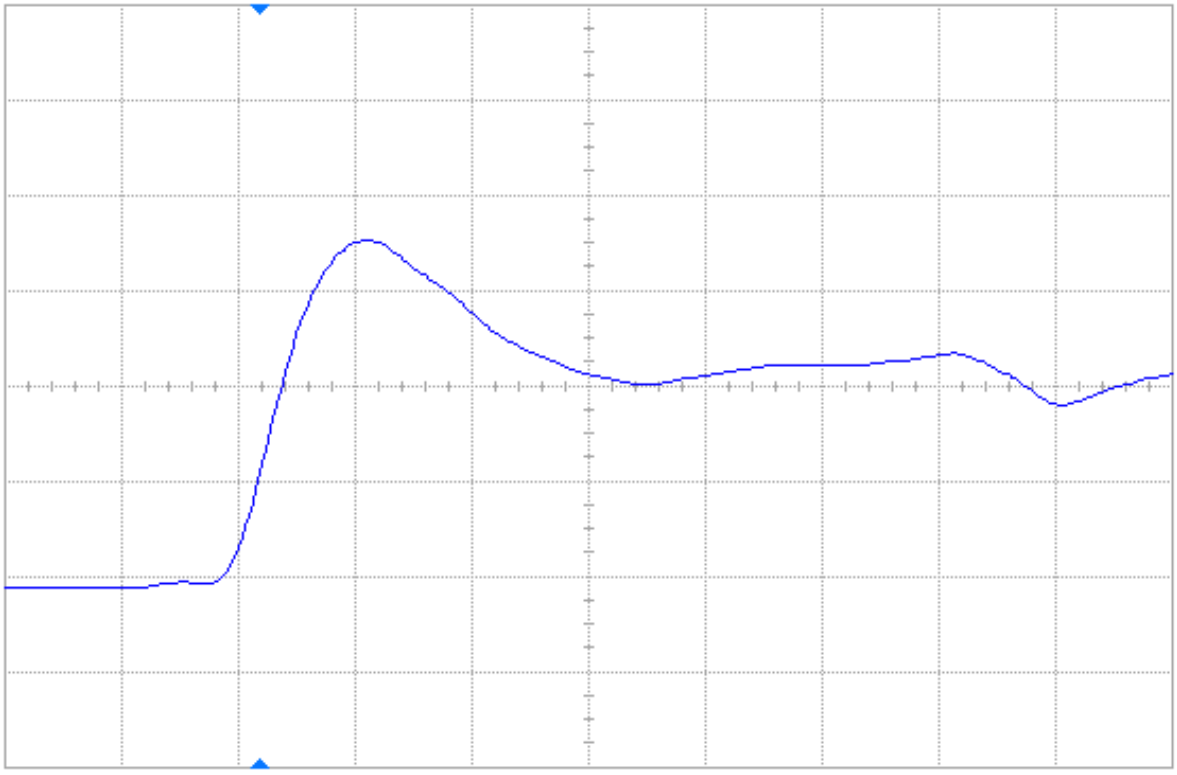


Figure 8 Post-annealing rising edge of DUT 49698, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

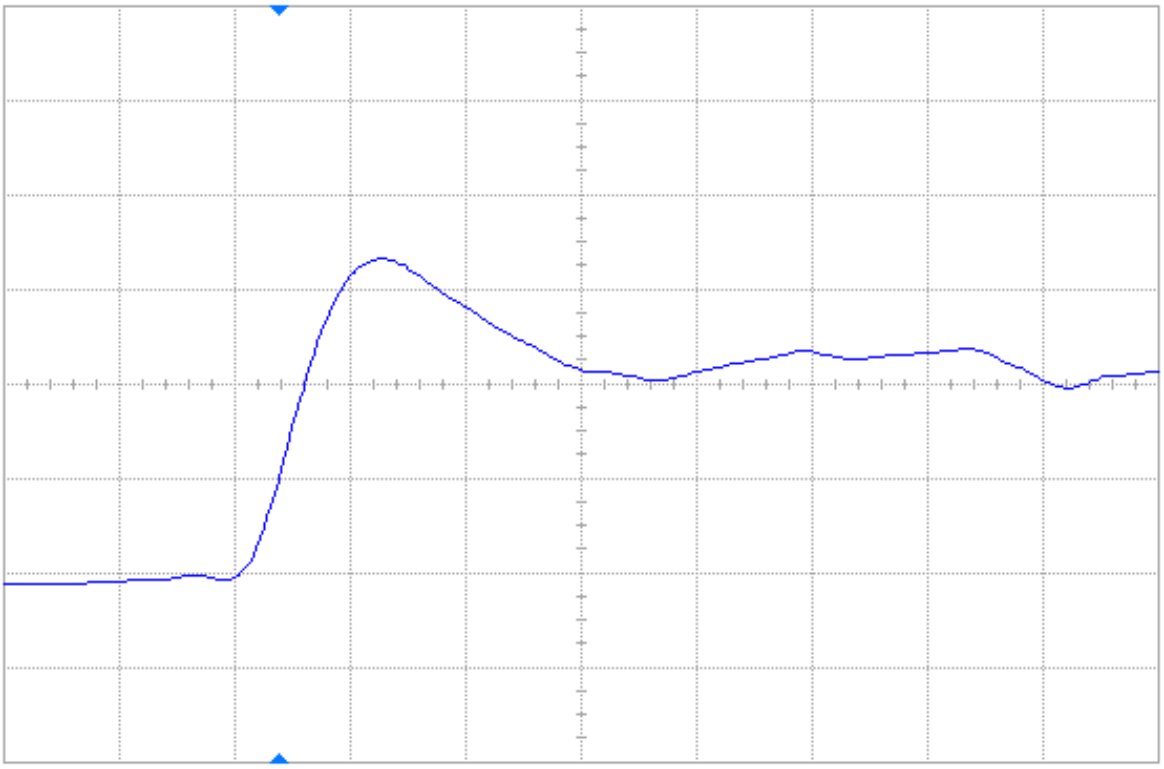


Figure 9 Post-annealing rising edge of DUT 49699, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

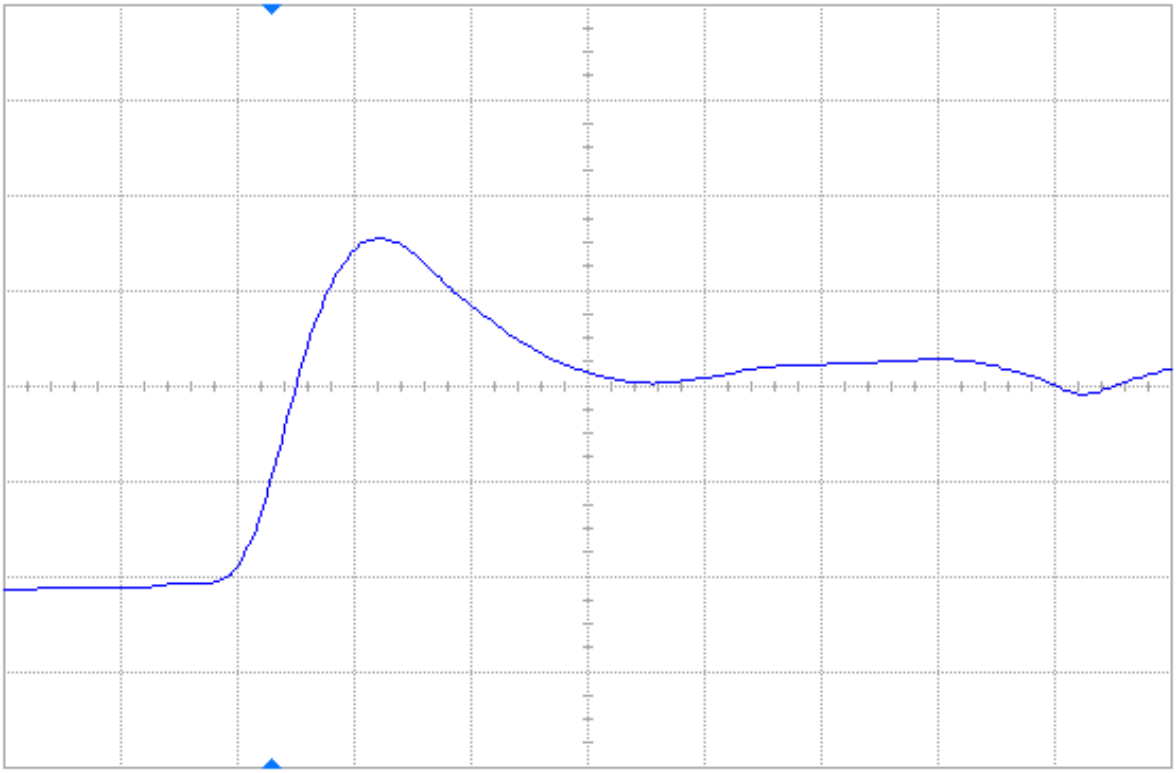


Figure 10 Post-annealing rising edge of DUT 49700, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

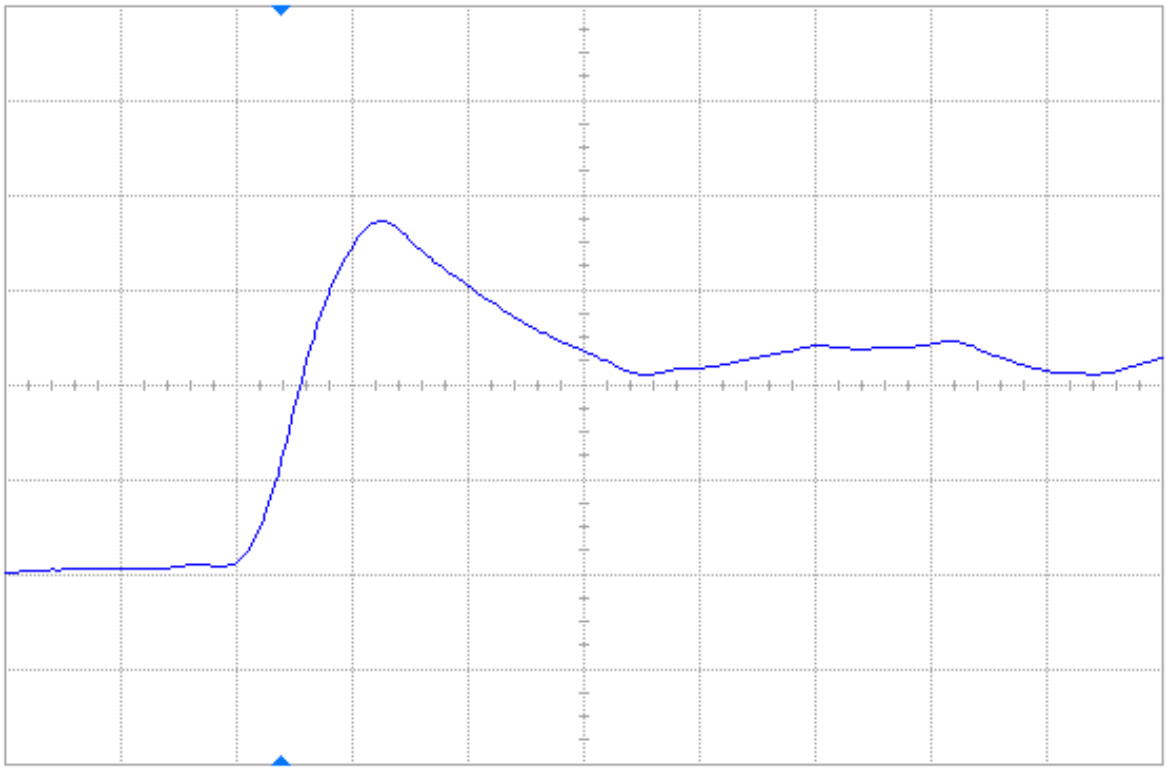


Figure 11 Post-annealing rising edge of DUT 49701, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

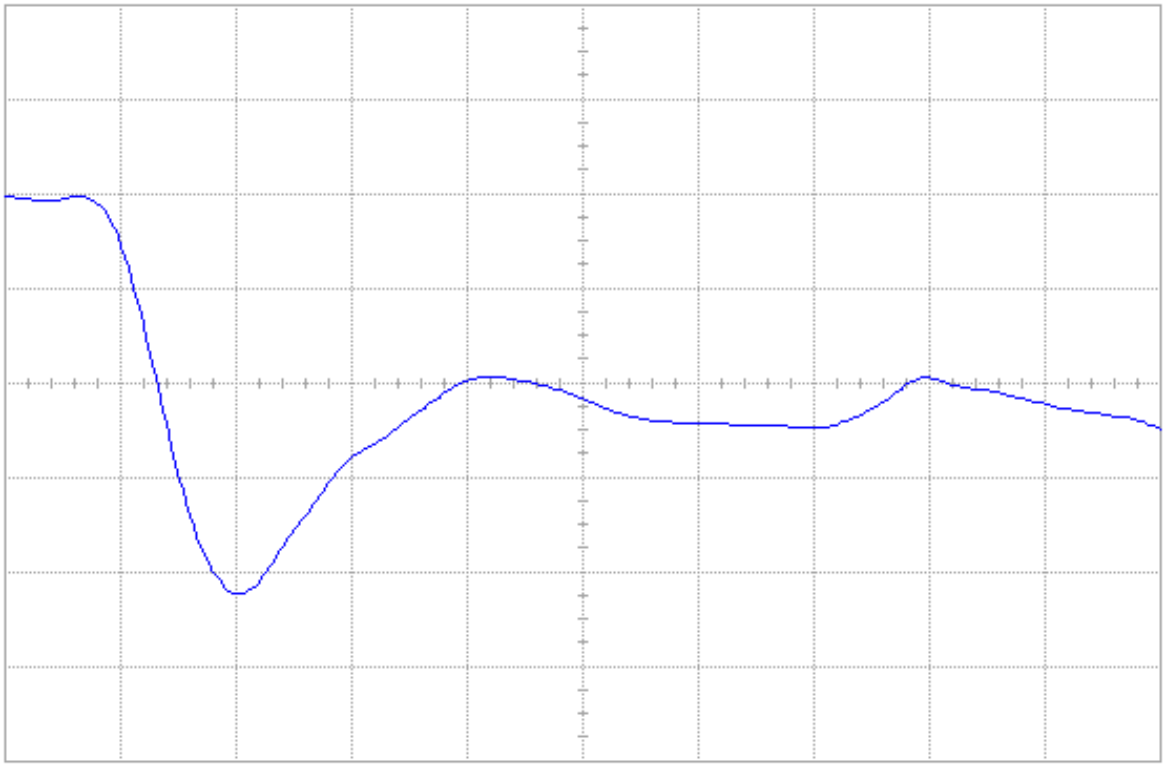


Figure 12 Post-annealing falling edge of DUT 49697, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

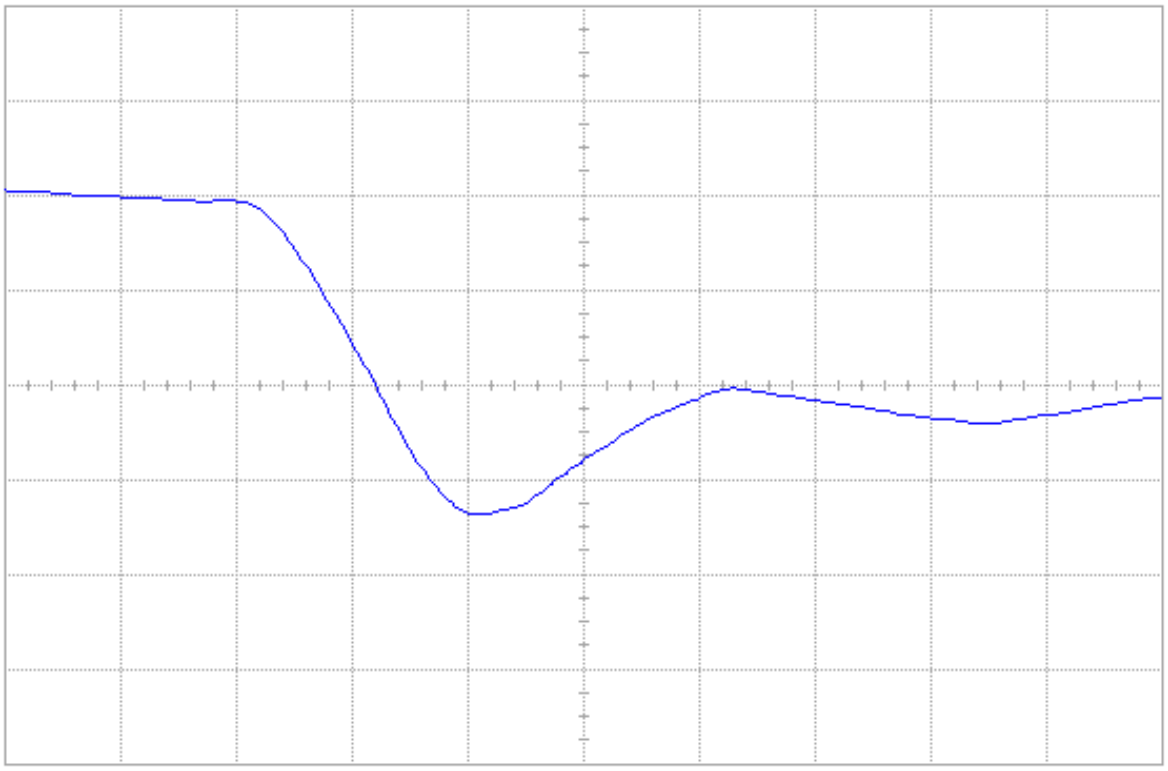


Figure 13 Post-annealing falling edge of DUT 49698, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

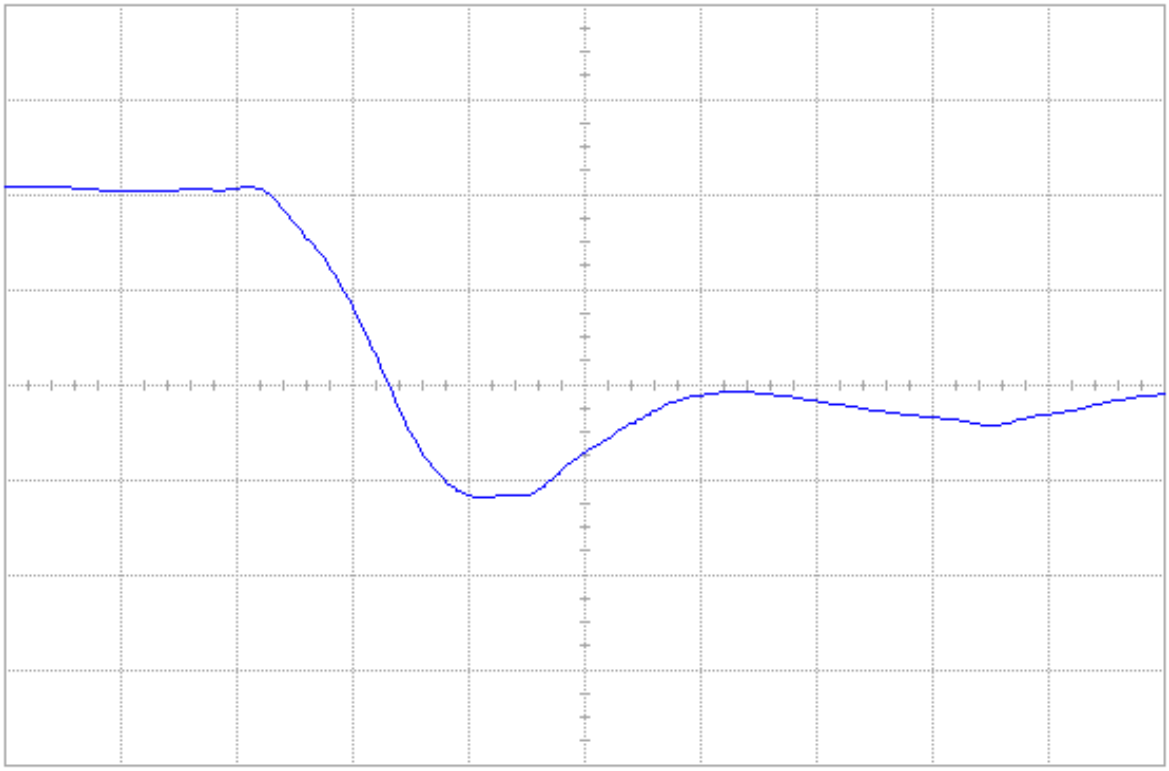


Figure 14 Post-annealing falling edge of DUT 49699, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

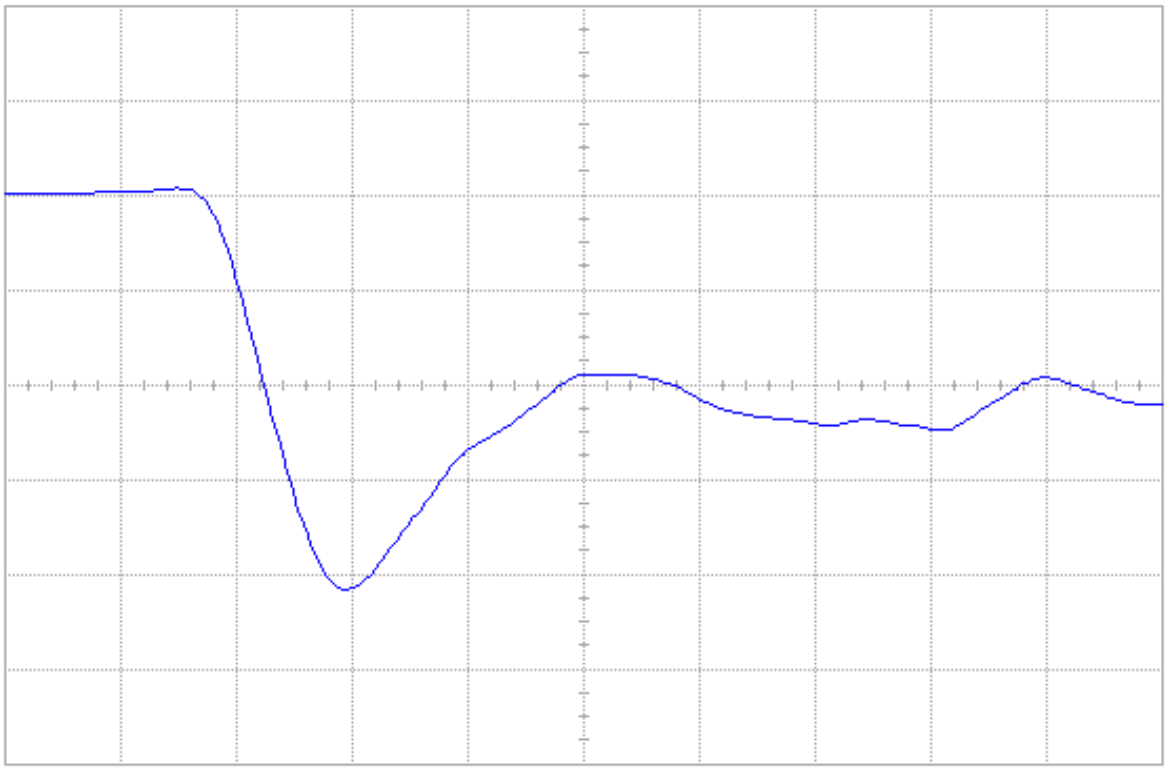


Figure 14 Post-annealing falling edge of DUT 49700, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

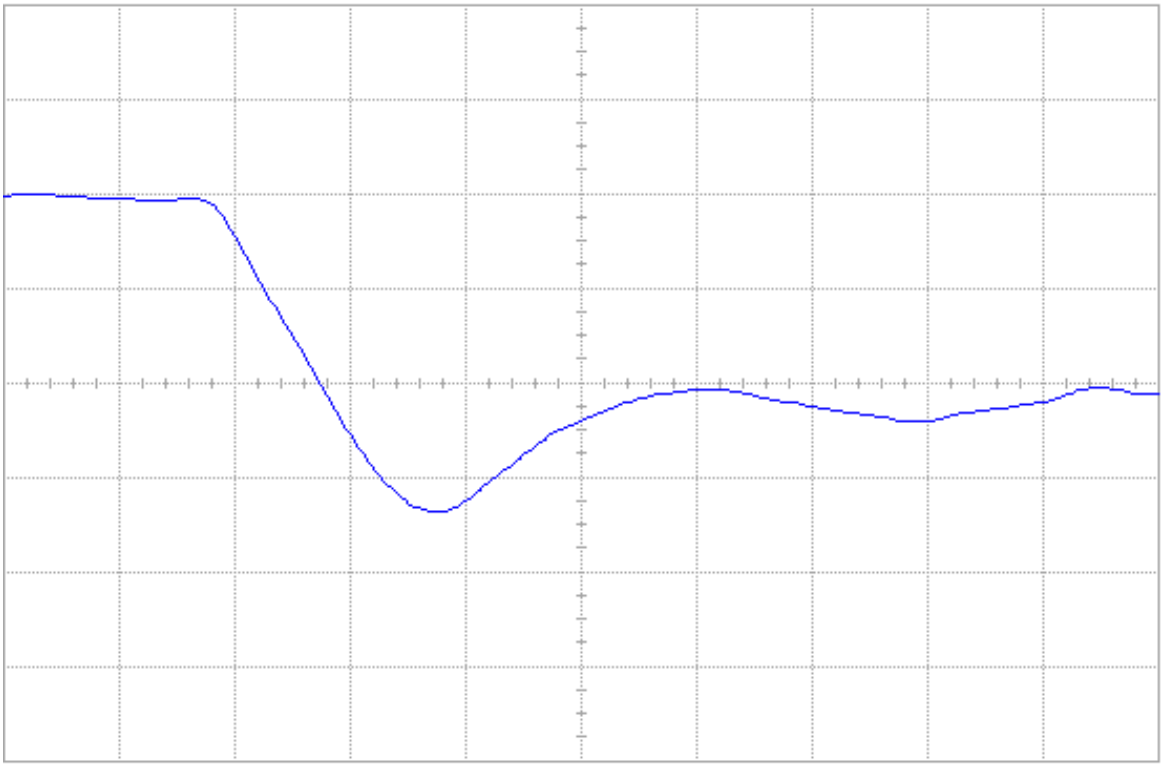
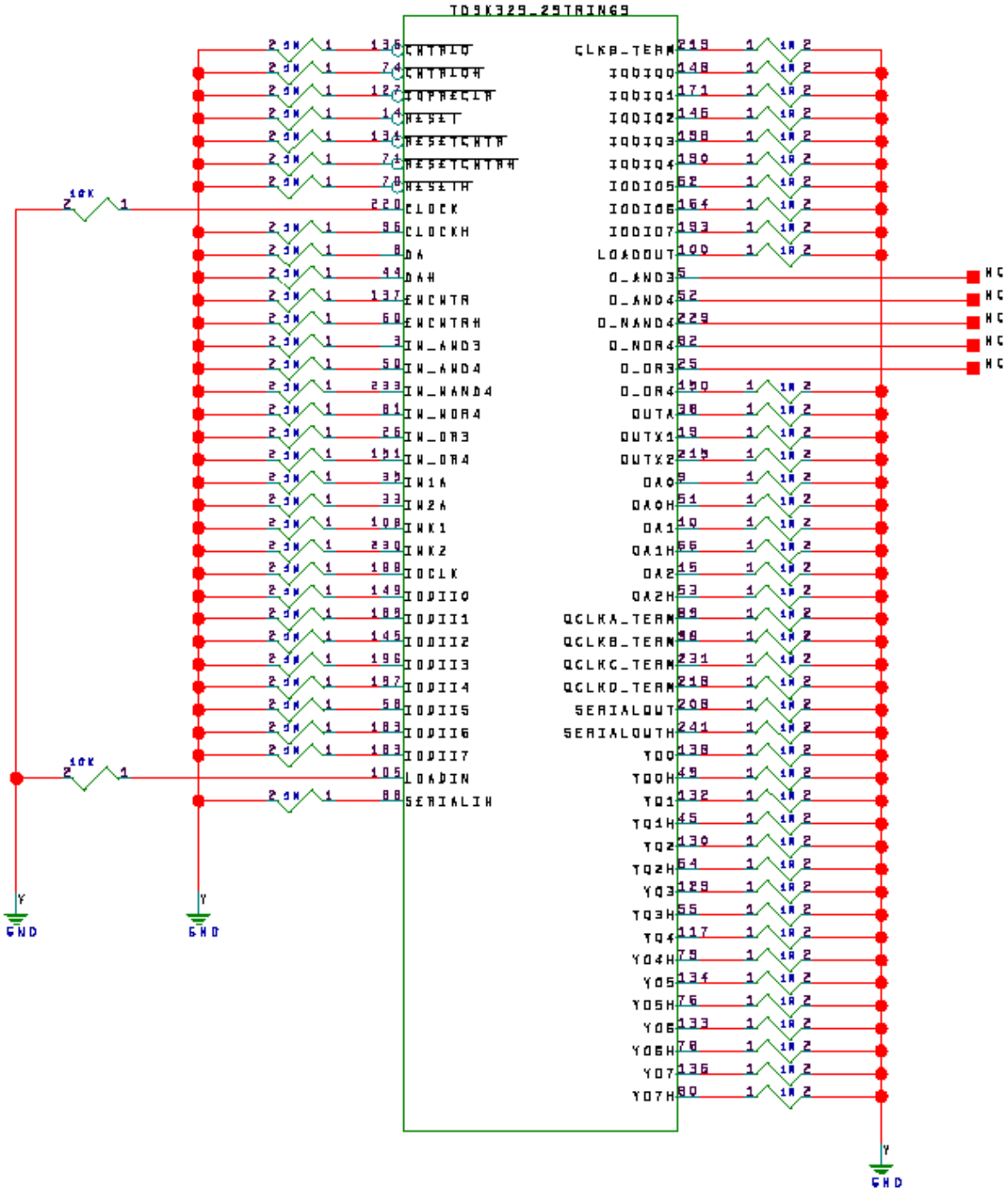
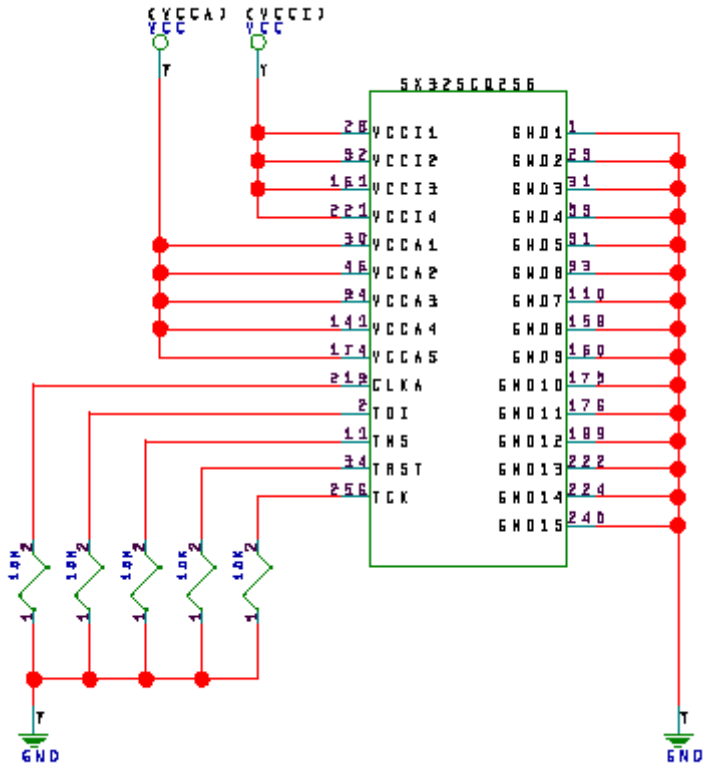


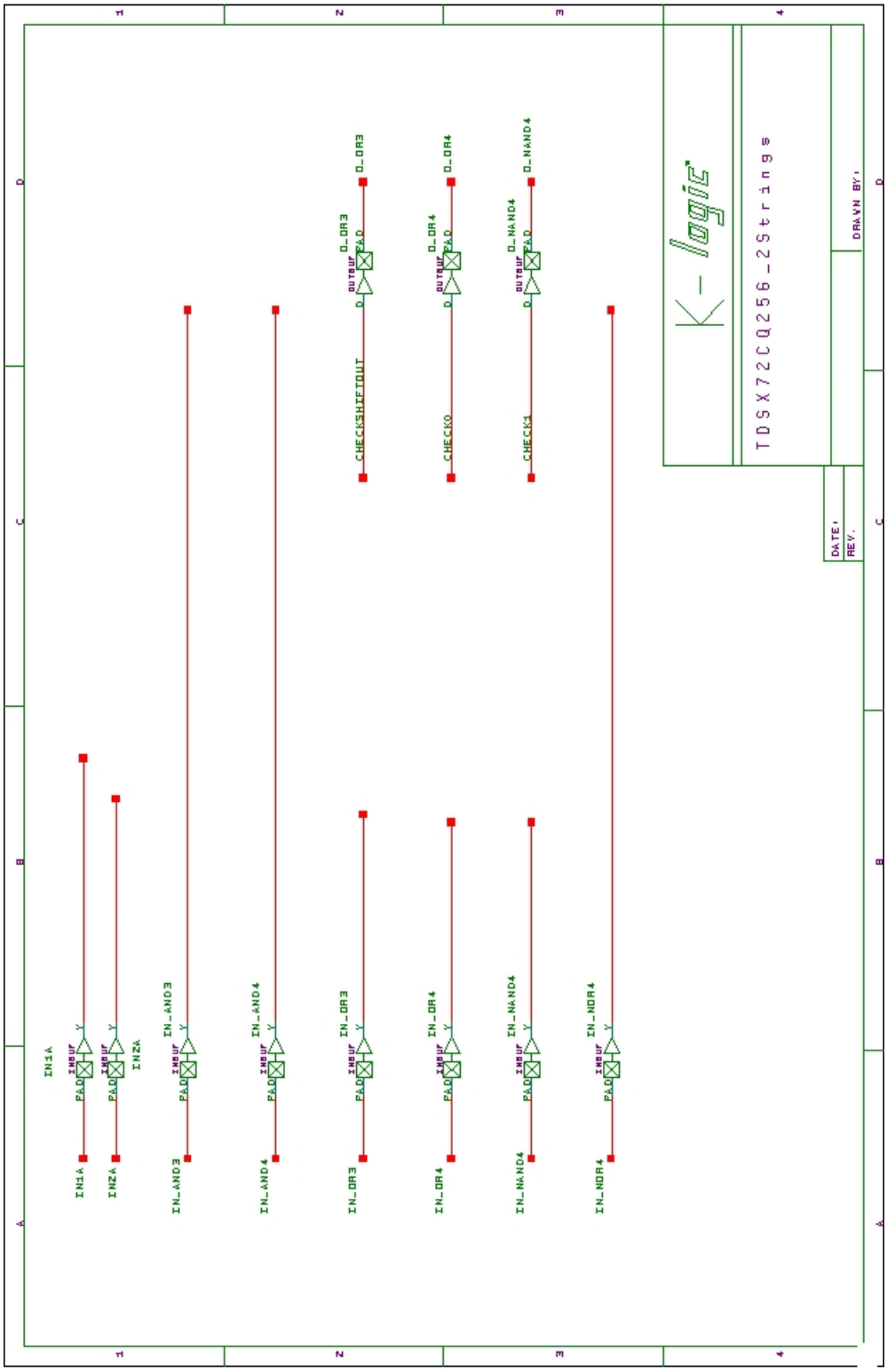
Figure 15 Post-annealing falling edge of DUT 49701, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

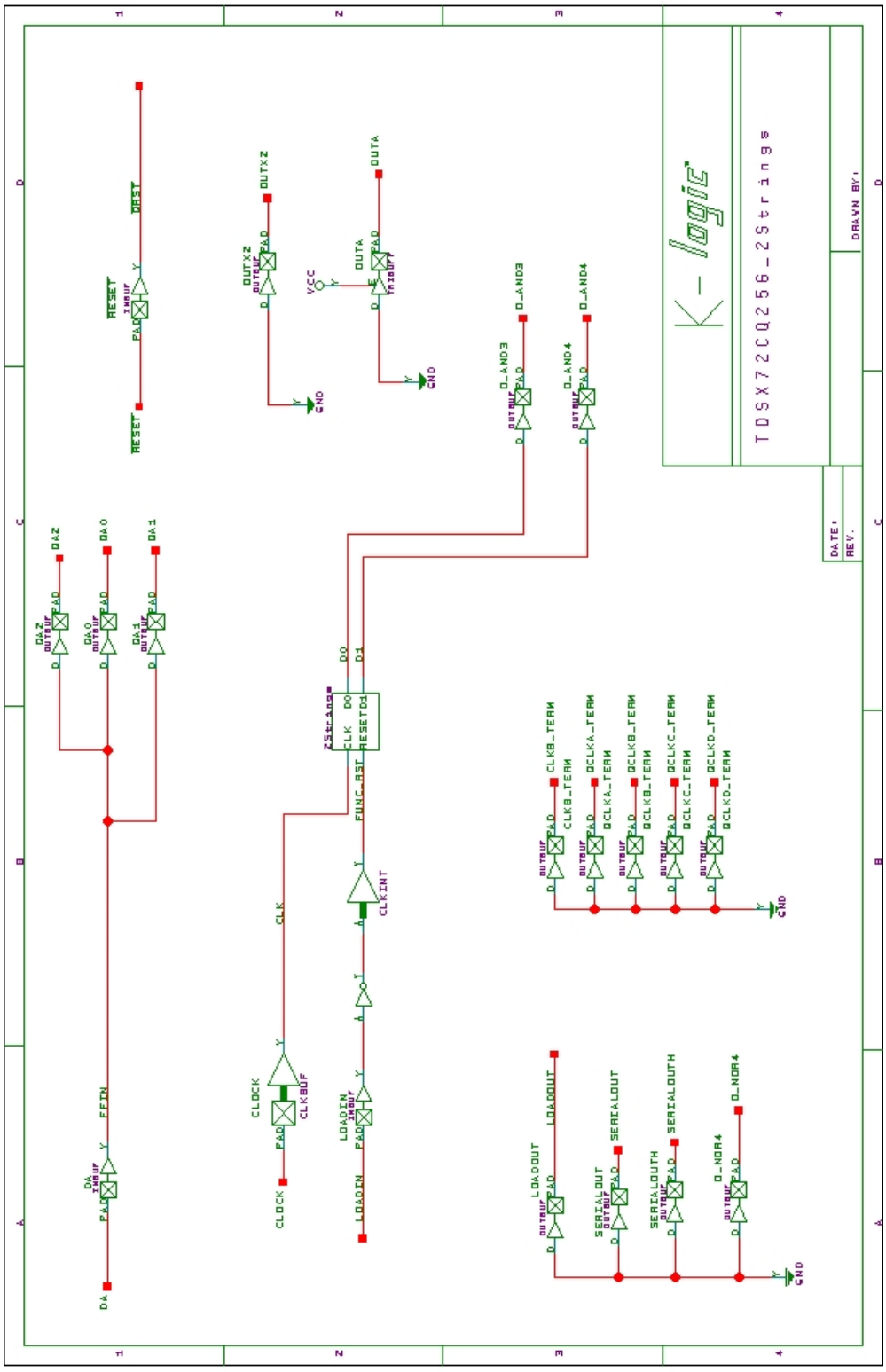
Appendix A DUT Bias

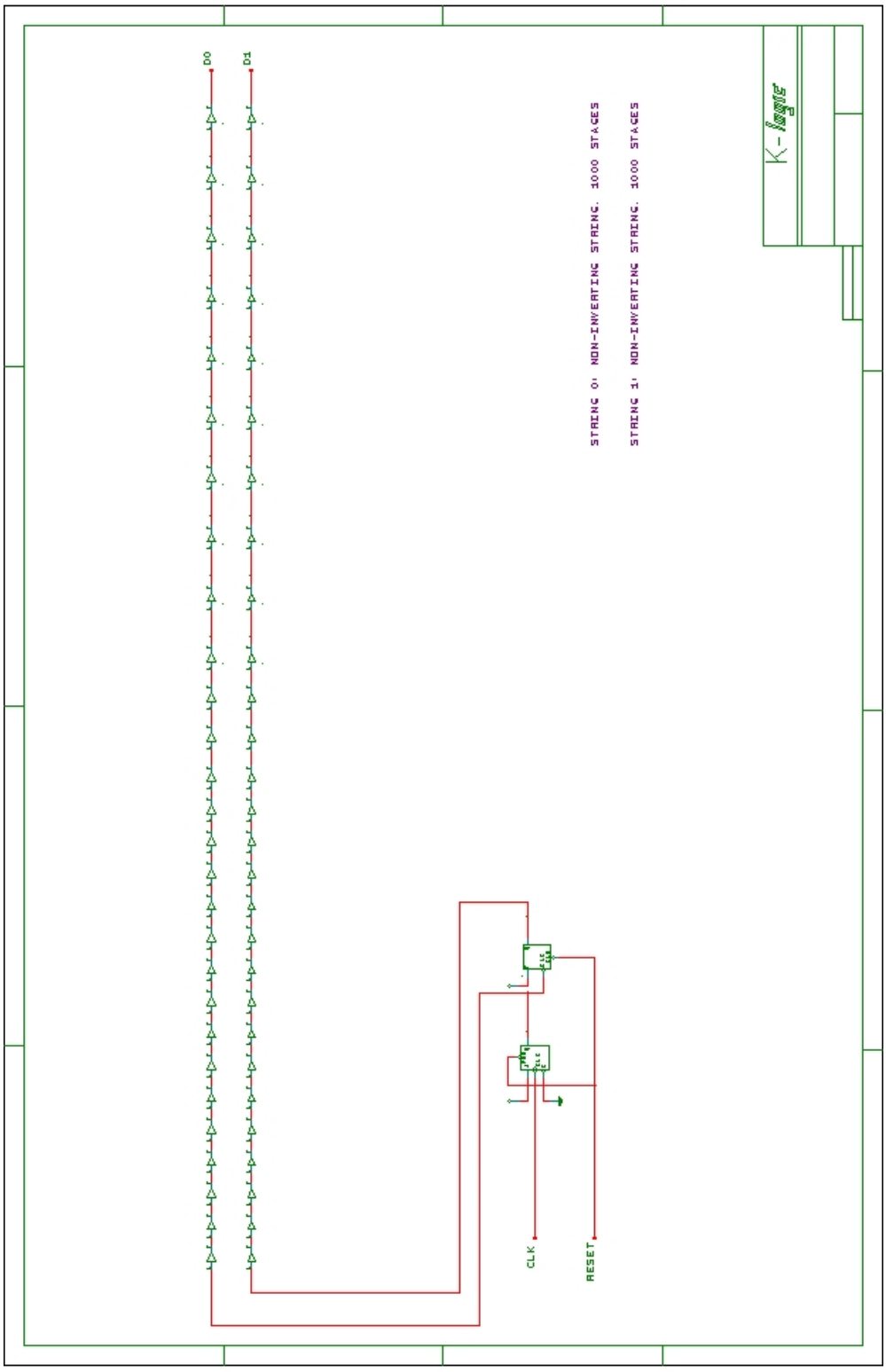


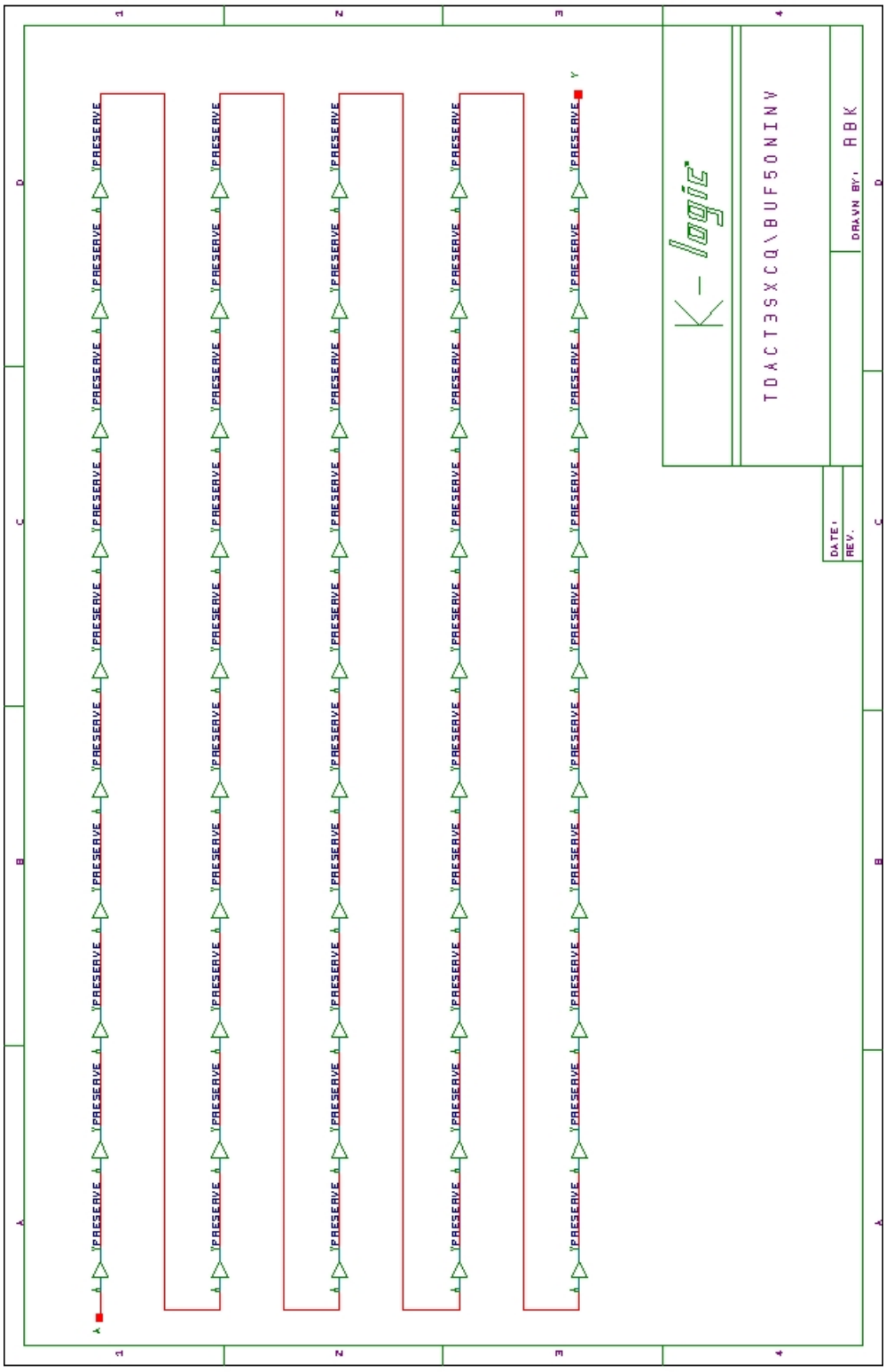

(VCCA)
VCC
(VCCI)
VCC
5X325CQ256
VCCI1
VCCI2
VCCI3
VCCI4
VCCA1
VCCA2
VCCA3
VCCA4
VCCA5
CLKA
TDI
TMS
TRST
TCK
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
10K
10K
10K
10K
10K
GND
GND

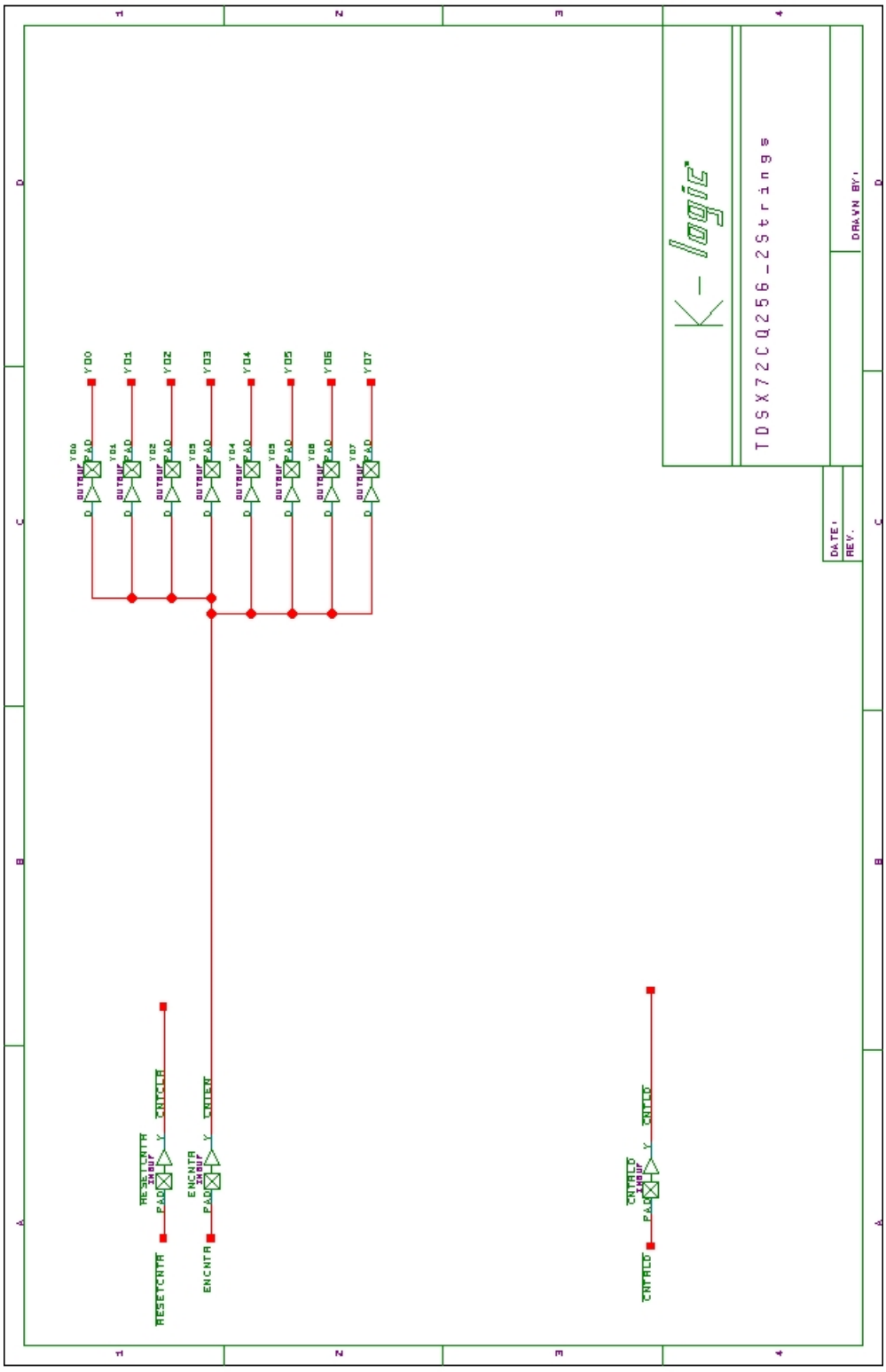
APPENDIX B DUT DESIGN SCHEMATICS (TDSX32CQ256_2STRINGS is the same as TDSX72CQ256_2STRINGS except the sizes of buffer strings and shift registers)




K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
RST
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
ZStrings
CLK
D0
D1
RESET01
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
CLKB_TERM
DCLKA_TERM
DCLKB_TERM
DCLKC_TERM
DCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4


D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
CLK
RESET


K- logic
TDACT35XCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
Y
PRESERVE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TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
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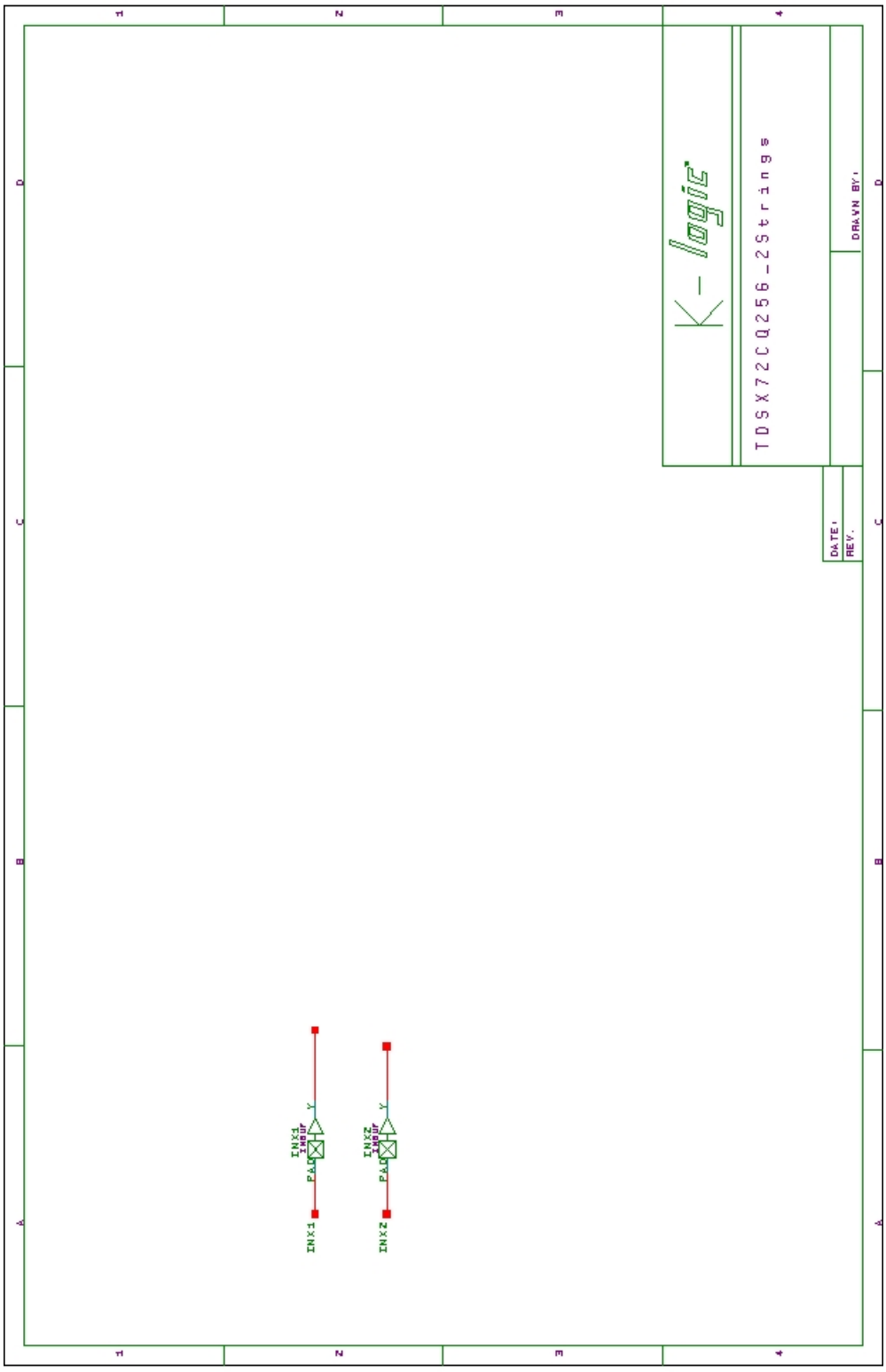
PAD
RESETCNTR
ENCNTR
CNTRLD
CNTLD
CNTCLK
CNTENT


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
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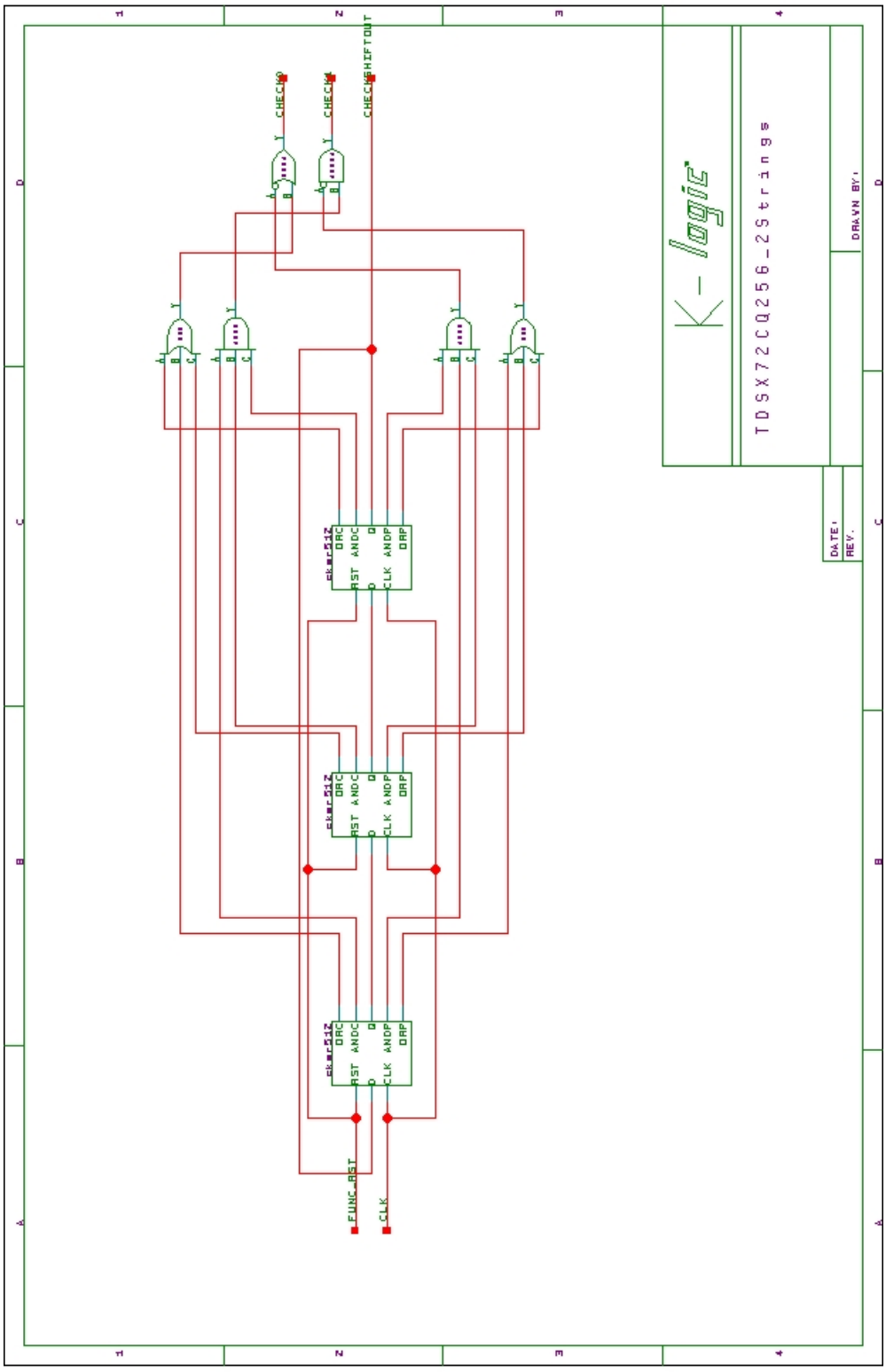
INX2
Y
A
B
C
D
1
2
3
4


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
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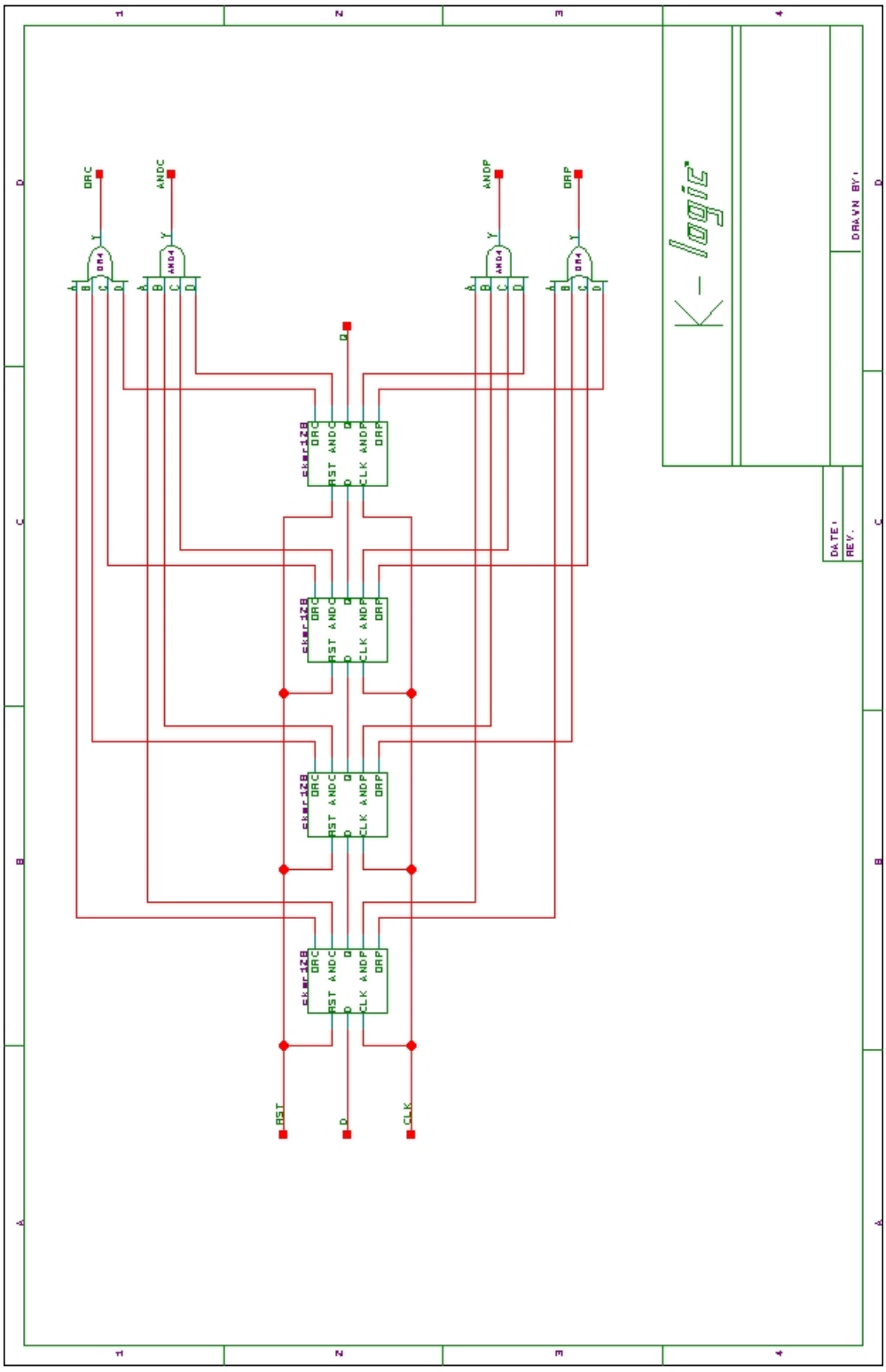
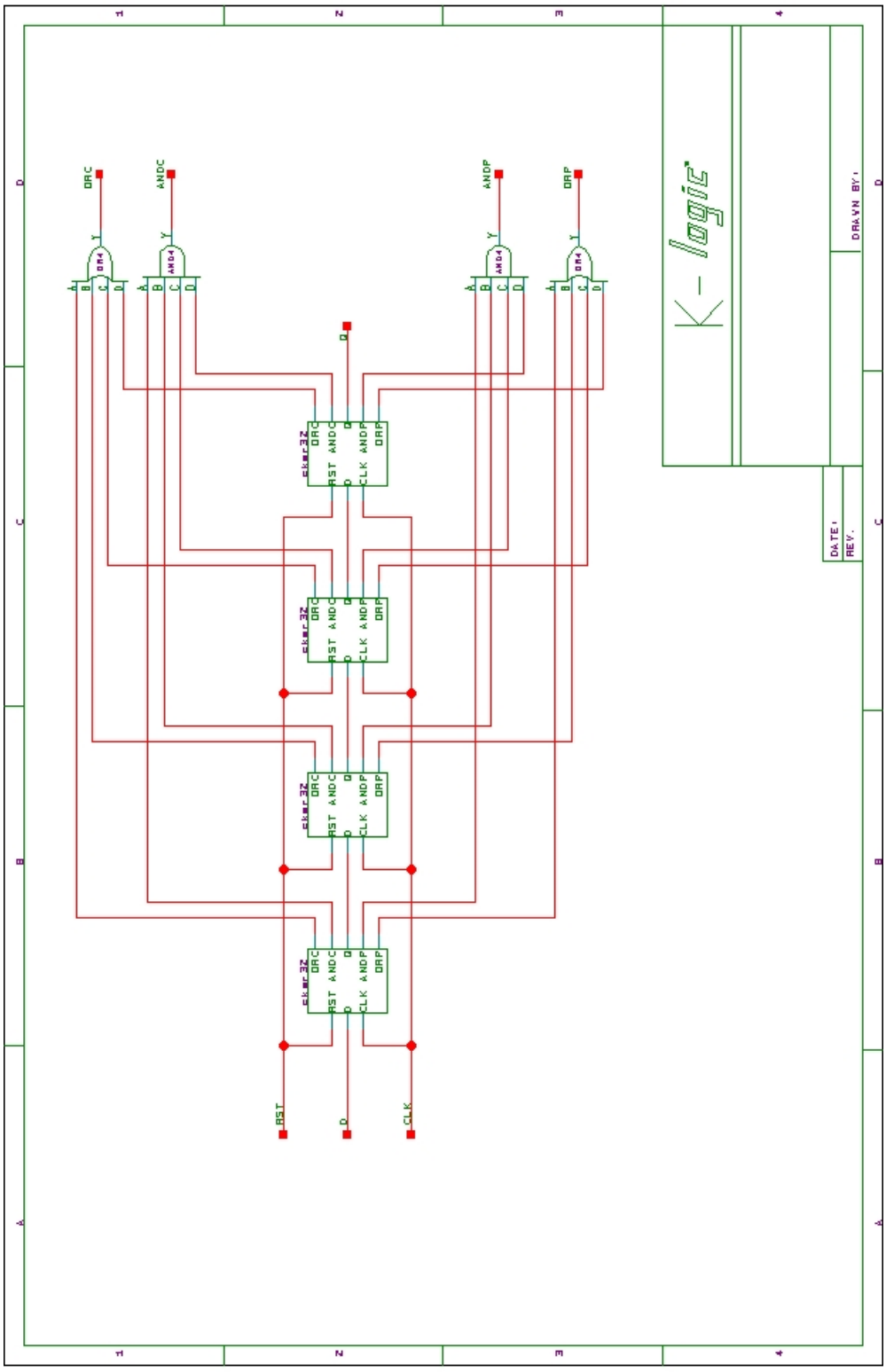
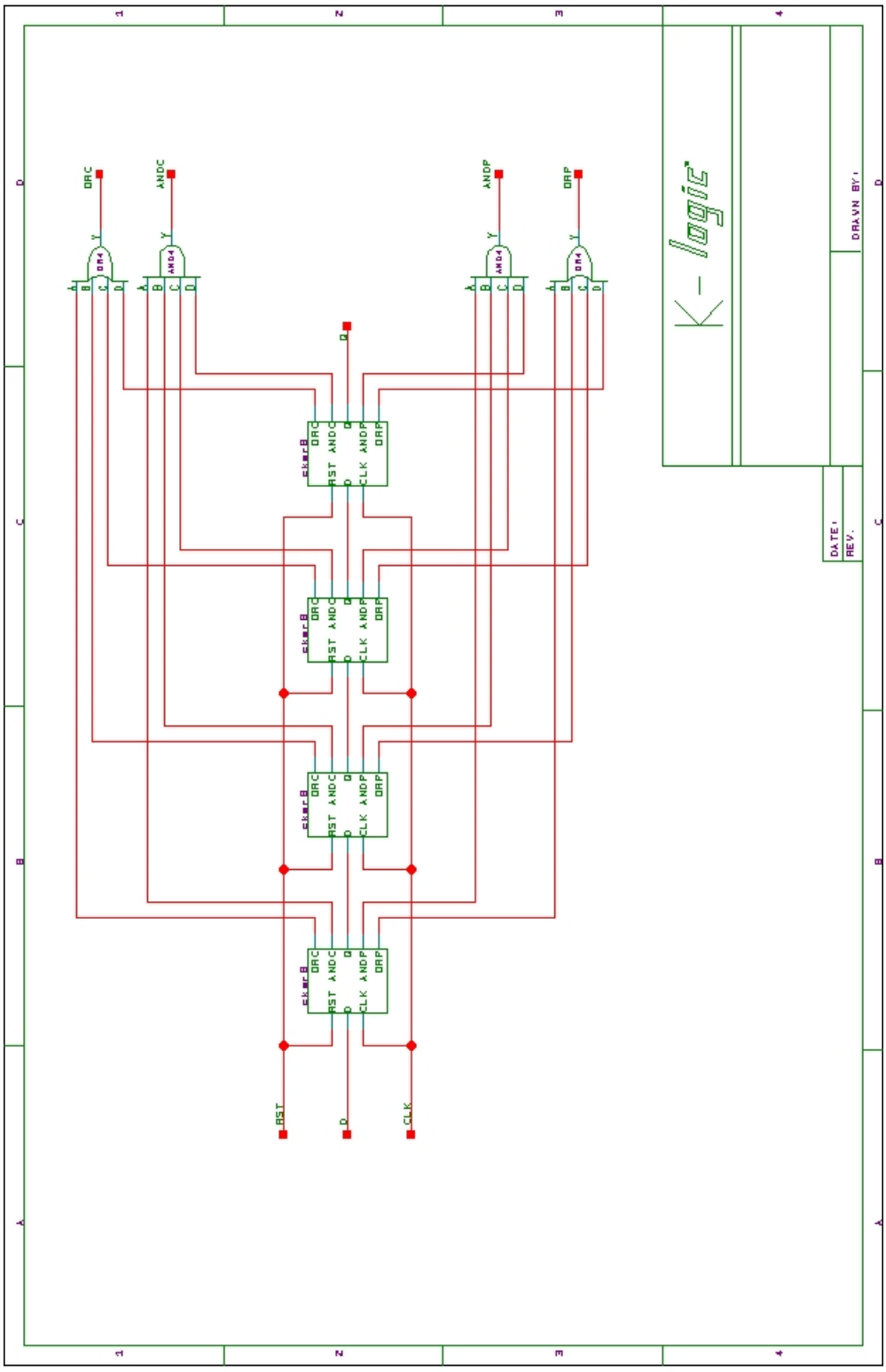
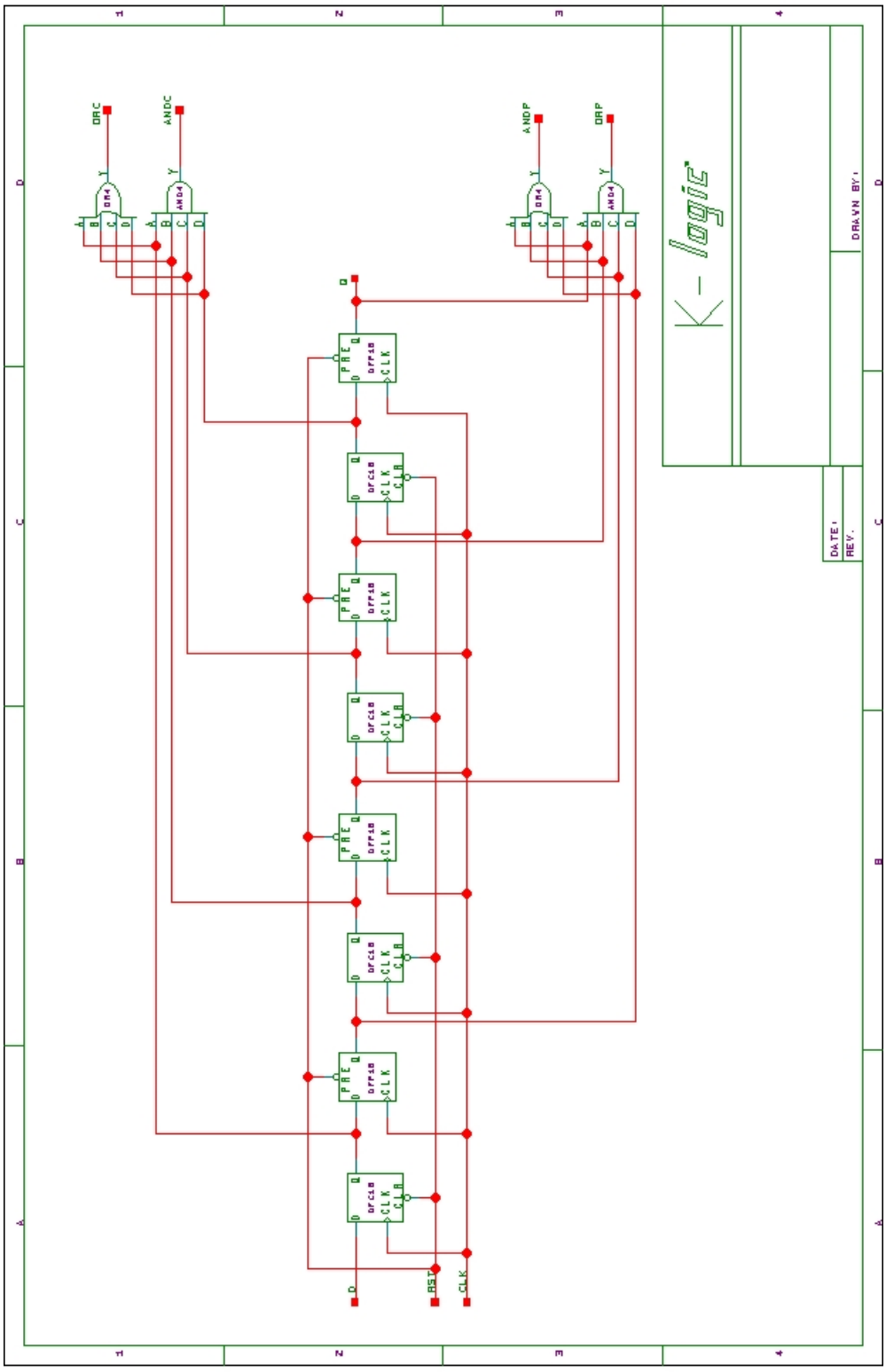
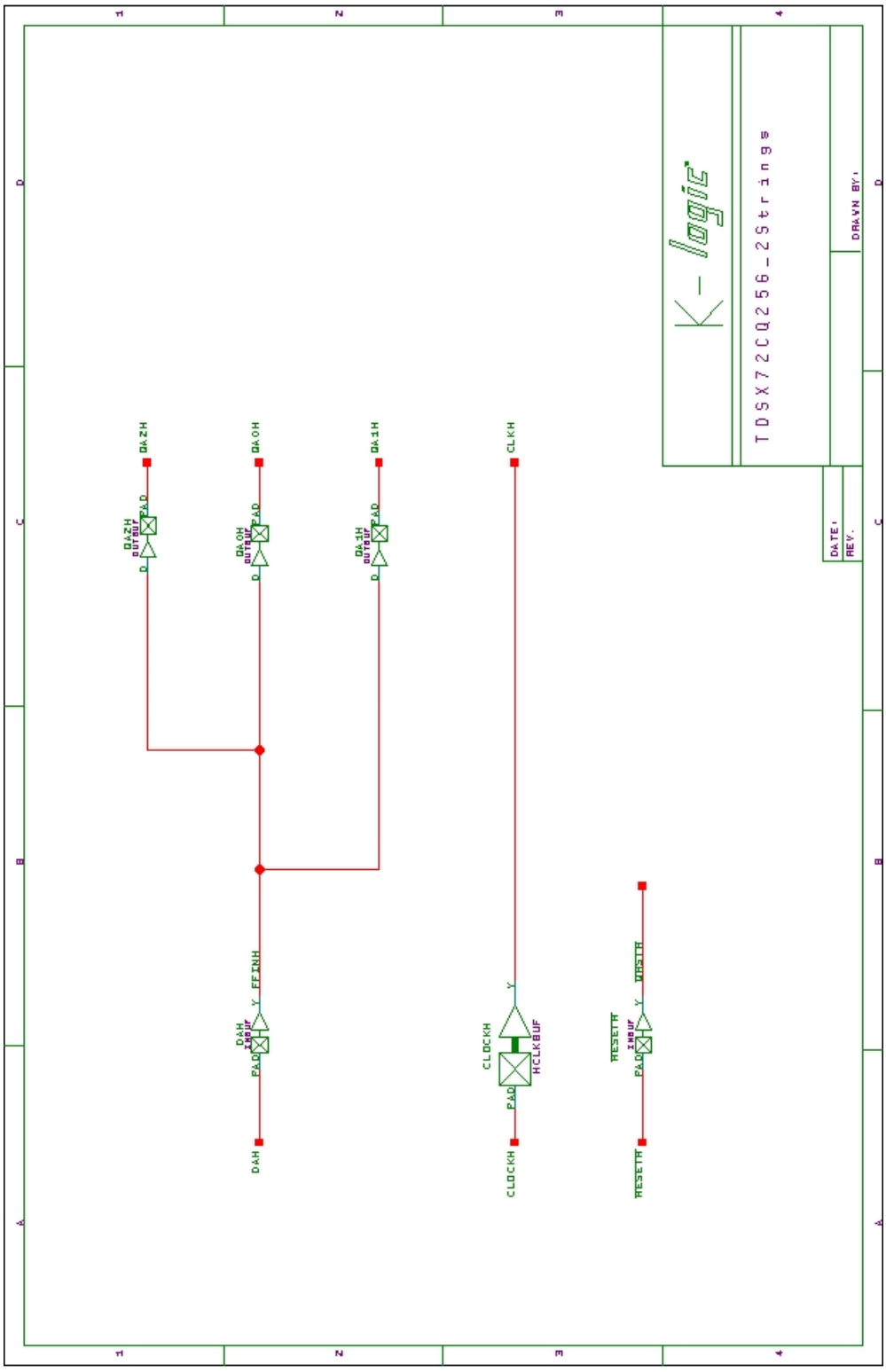
REV.
CHECKSHIFTOUT
CHECK0
CHECK1
FUNC_RST
CLK

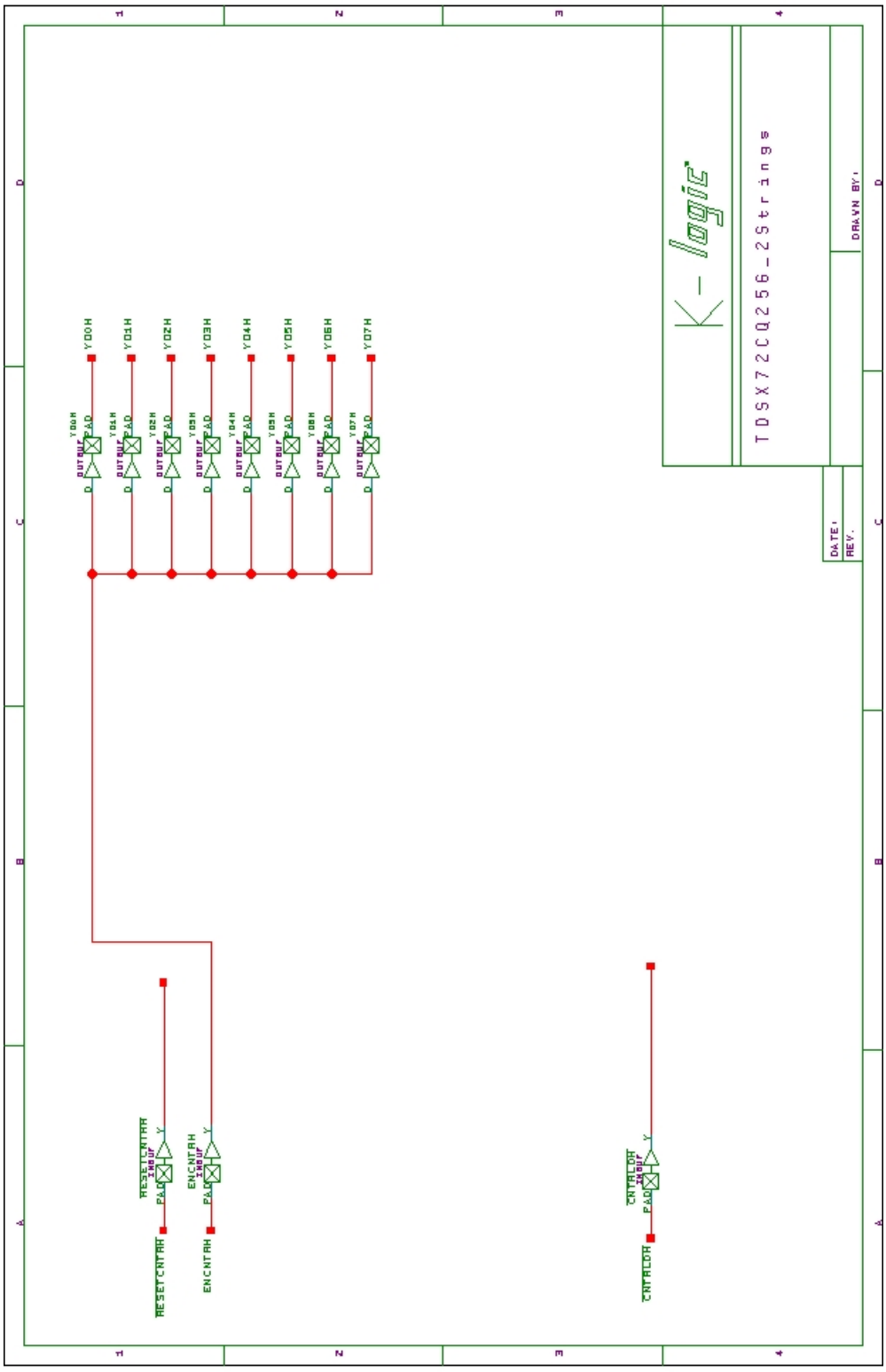

DRC
ANDC
ANDP
DRP
K - logic
DRAWN BY:
DATE:
REV.
RST
D
CLK

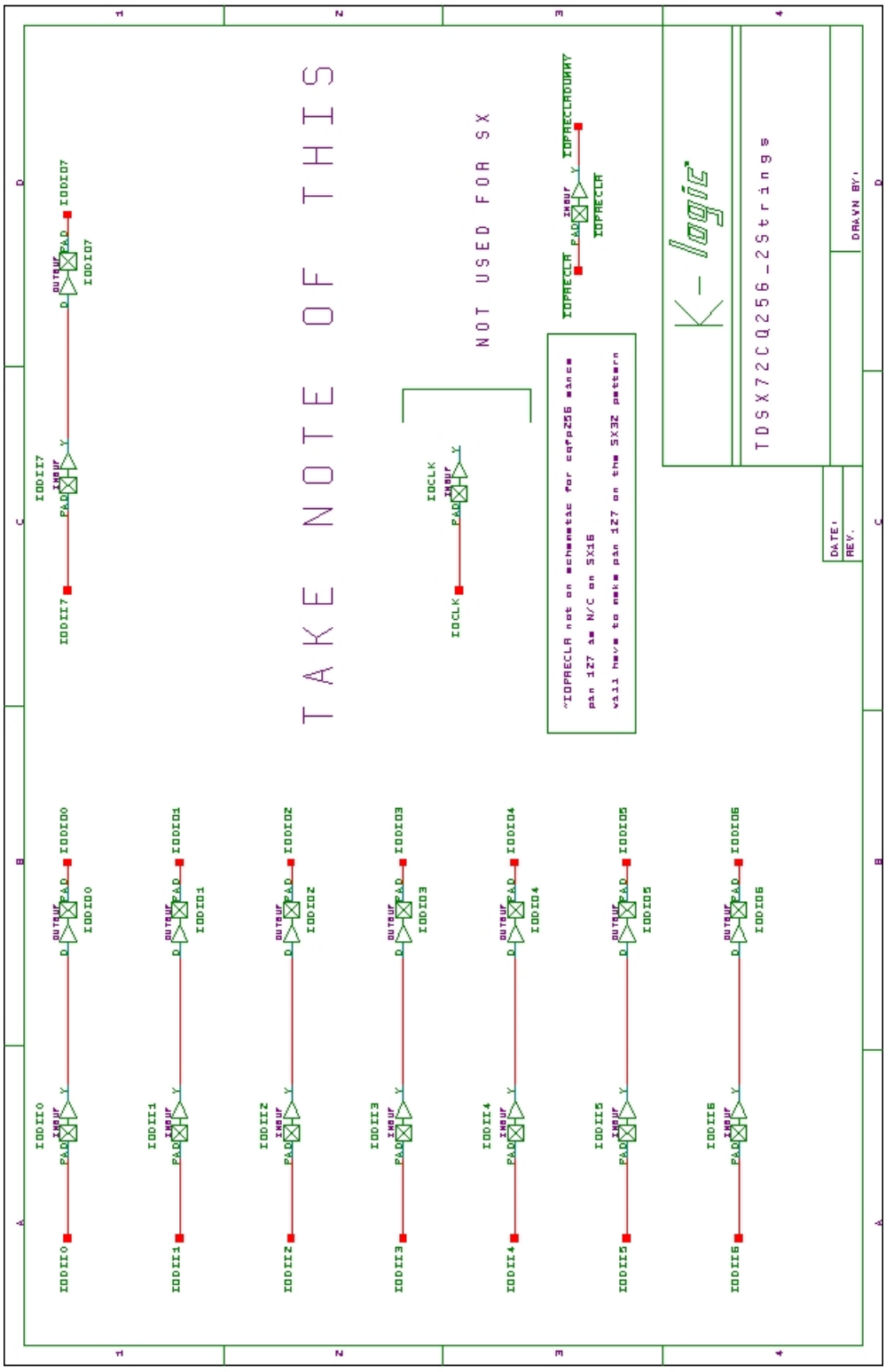

DRC
ANDC
ANDP
DRP
AND4
OR4
RST
D
CLK
K- logic
DRAWN BY:
DATE:
REV.

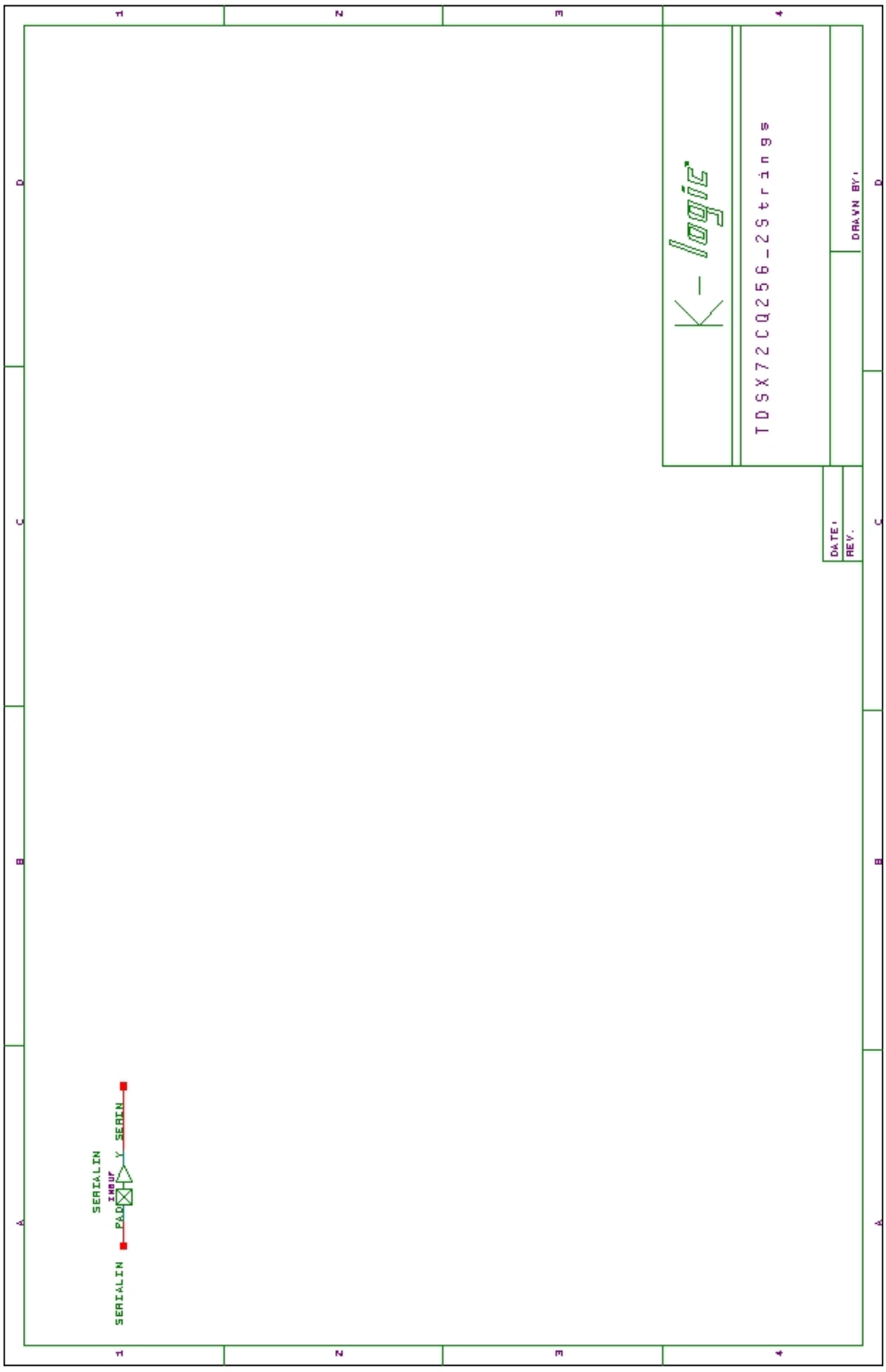

DRC
ANDC
ANDP
DRP
AND4
DR4
Y
A
B
C
D
Q
Ckrc8
RST
CLK
RST
D
CLK
K- logic
DRAWN BY:
DATE:
REV.

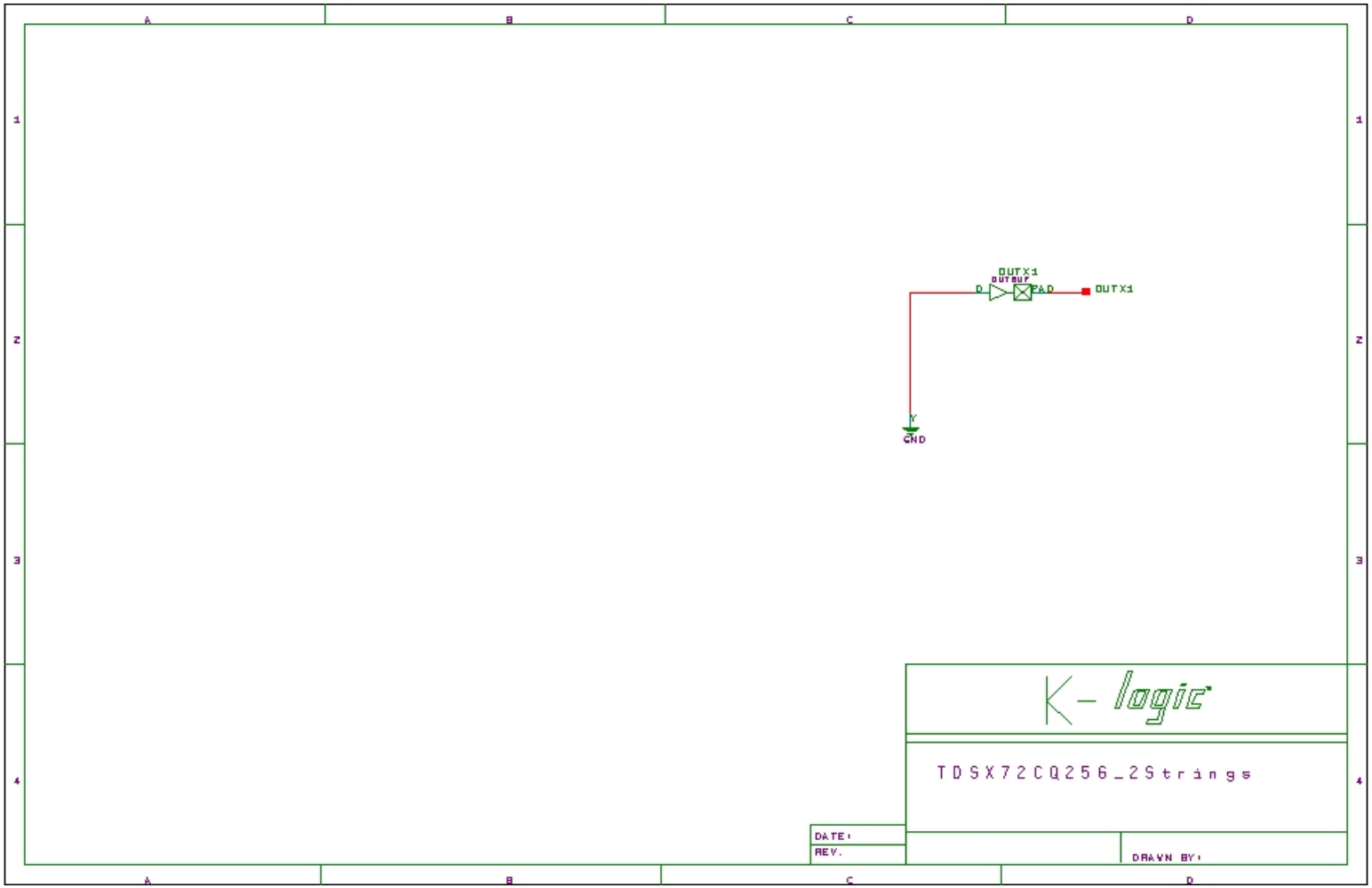

K- logic
DRAWN BY:
DATE:
REV.
DRC
ANDC
ANDF
DRF
D
RST
CLK


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DA2H OUTBUF
DA0H OUTBUF
DA1H OUTBUF
PAD
D
DAH INBUF
Y FFINH
PAD
DAH
CLOCKH HCLKBUF
Y
PAD
CLOCKH
RESETH INBUF
Y RRSTH
PAD
RESETH


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
YD0H
YD1H
YD2H
YD3H
YD4H
YD5H
YD6H
YD7H
OUTBUF
PAD
RESETCNTAH
ENCNTAH
CNTALOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.
IOCLK
IOPRECLR
IOPRECLRQUINARY
*IOPRECLR not on schematic for csfp256 mance
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
SERIALIN
SERIALIN
SERIN


A
B
C
D
1
2
3
4
OUTX1
OUTBUF
D
PAD
OUTX1
Y
GND
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY: