TOTAL IONIZING DOSE TEST REPORT

No. 03T-RT54SX72S-T25KS008

September 17, 2003

J.J. Wang
(650) 318-4576
jih-jong.wang@actel.com

I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad(Si)
2. I_{CC}	Passed 75 krad(Si) for 25 mA spec, I_{CC} averaging 65.5 mA after 100 krad(Si) and room temp annealing
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad(Si)
4. Output Drives (V_{OL}/V_{OH})	Passed 100 krad(Si)
5. Propagation Delays	Passed 100 krad(Si) for 10% degradation criterion
6. Transition Time	Passed 100 krad(Si)

II. Total Ionizing Dose (TID) Testing

A. Device Under Test (DUT) and Irradiation

Table 1 lists the DUT information and irradiation conditions.

Table 1. DUT information and irradiation conditions

Part Number	RT54SX72S
Package	CQFP256
Foundry	Matsushita Electronics Corporation
Technology	0.25 μm CMOS
DUT Design	TDSX72CQFP256_2Strings
Die Lot Number	T25KS008
Quantity Tested	5
Serial Number	22245, 22253, 22255, 22272, 22275
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad(Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

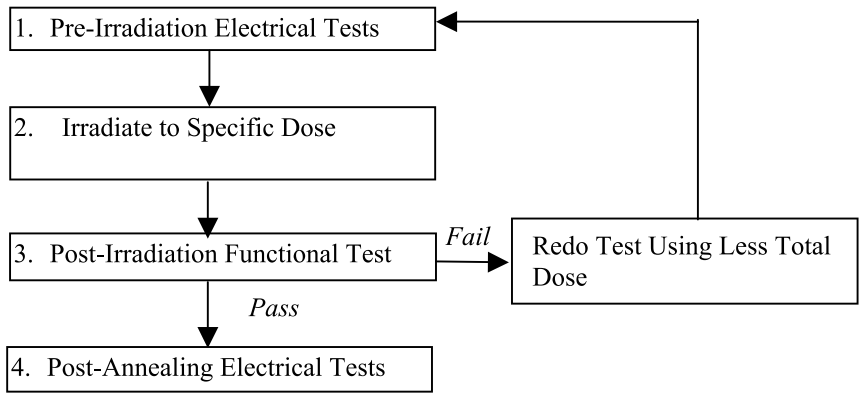


Fig 1 Parametric test flow chart

The parametric tests follow the military standard test method 1019.5. Fig 1 shows the testing flow. The time dependent effect (TDE) of this product was previously evaluated by comparing the results of a high dose rate (1 krad(Si)/min) against the results of a low dose rate (1 krad(Si)/hr). No adverse TDE was observed. Therefore the accelerated aging test (rebound test) is omitted. Room temperature annealing were performed for approximately one month after 100 krad(Si) of irradiation. DUTs were static biased during annealing.

C. Electrical Parameter Measurements

A high utilization design (TDSX72CQ256_2Strings) to address total dose effects in typical space applications is used. The circuit schematics are shown in appendix A.

Table 2 lists the electrical parameters measured. The functionality is measured pre-irradiation, post-irradiation, and post-annealing on the output pin (O_AND3 or O_AND4) of the two combinational buffer-strings and on the output pins (O_OR4 and O_NAND4) of the shift register. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively.

The input logic thresholds (V_{TIL}/V_{IH}) and output drives (V_{OL}/V_{OH}) are measured pre-irradiation and post-annealing on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured pre-irradiation and post-annealing on the O_AND4 output of one of the buffer strings. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the O_AND4. The transient times (rise and fall times) are measured post-annealing on the O_AND4.

Each unused input is grounded with an 1 M ohm resistor during irradiation and an 1.2K ohm resistor during annealing.

Table 2. Logic design for parametric tests

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffer (pin DA to QA0)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (pin DA to QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Time	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passed the gross functional test at pre-irradiation, post-irradiation, and post-annealing.

B. I_{CC}

Figs 2-6 show the in-flux I_{CC} plots. Table 3 lists the post-annealing I_{CC}.

Table 3. Post-annealing I_{CC}

DUT	I_{CCA} (mA)	I_{CCI} (mA)
22245	49.5	17.7
22253	33.4	4.9
22255	68.3	9
22272	55	18
22275	65	6.9

An empirical equation is used to extract the total dose tolerance after a 10 years annealing. The critical total dose ($\gamma_{critical}$) for a 10-year mission to induce I_{CC} to 25 mA can be obtained by the equation:

$$I_{CCA}(\gamma_{critical}) \times 0.32 + I_{CCI}(\gamma_{critical}) \times 0.29 = 25mA$$

Where $I_{CCA}(\gamma)$ and $I_{CCI}(\gamma)$ are read from the raw data of the worst case, i.e. DUT 22272 (Fig 5). The tolerance ($\gamma_{critical}$) is obtained as approximately 75 krad(Si). This extracted tolerance is very conservative. Experiments have shown that a DUT irradiated at high dose rate and then annealed for the duration to match the total mission time results a significantly higher I_{CC} than that of a DUT, manufactured by the same technology, irradiated at a low, uniform dose rate throughout the total mission time.

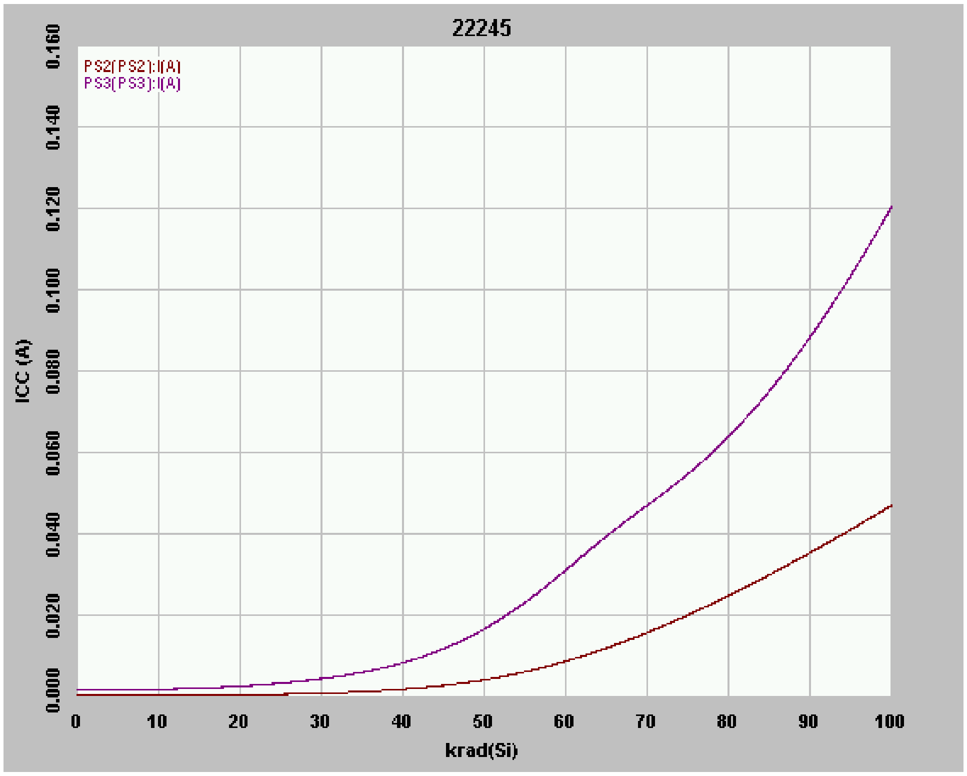


Fig 2 In-flux I_{CC} of DUT 22245, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

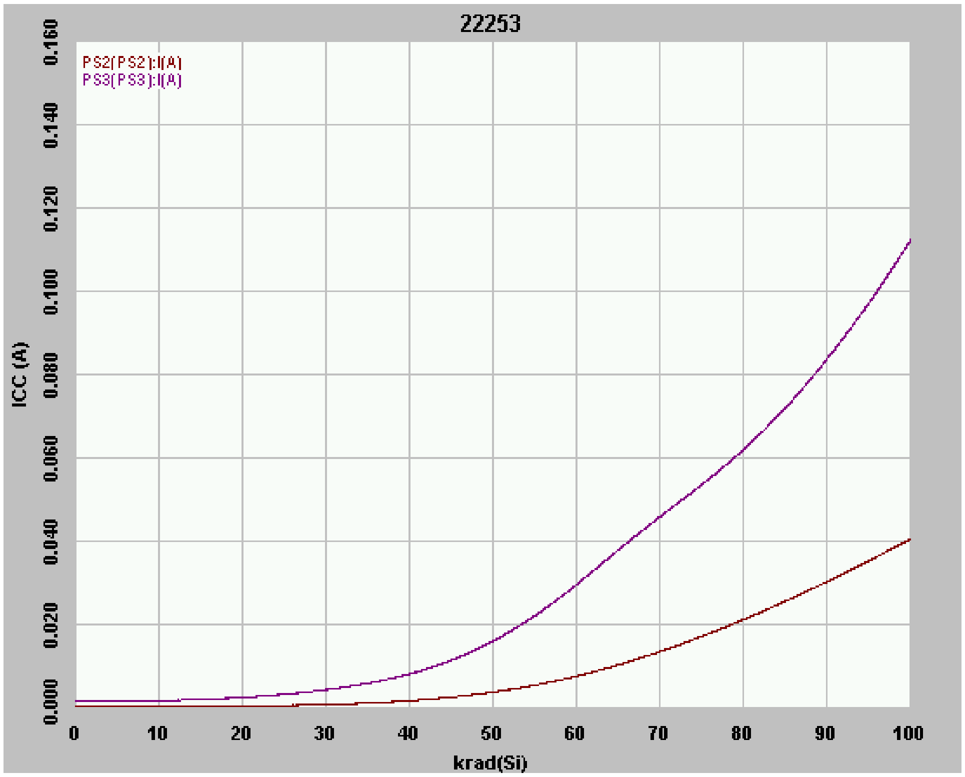


Fig 3 In-flux I_{CC} of DUT 22253, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

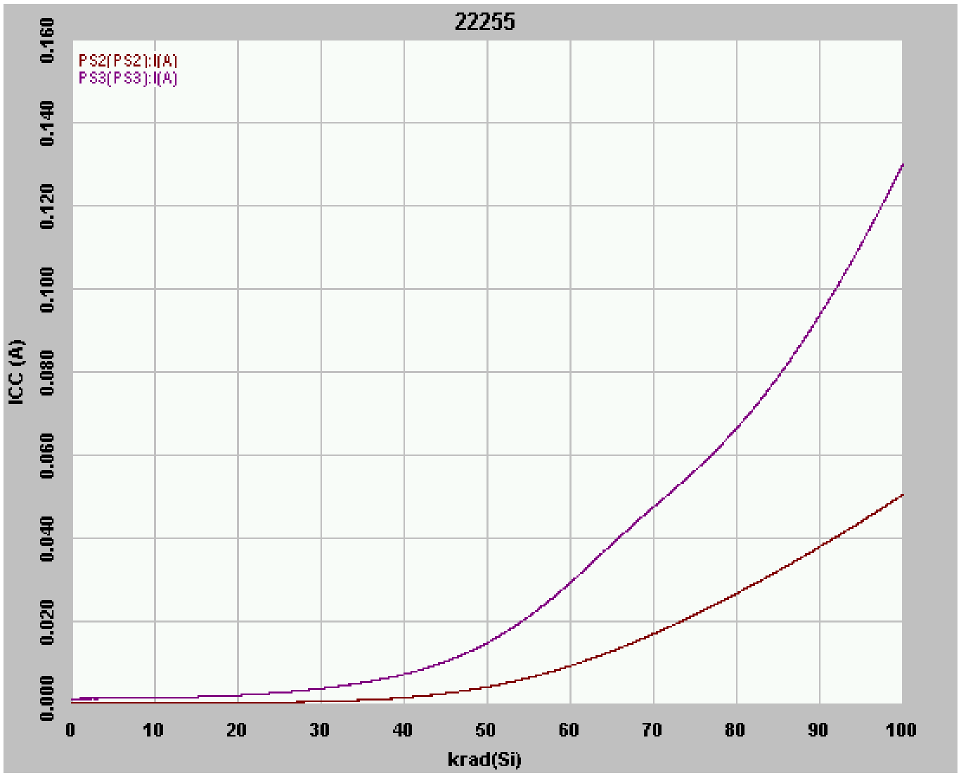


Fig 4 In-flux I_{CC} of DUT 22255, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

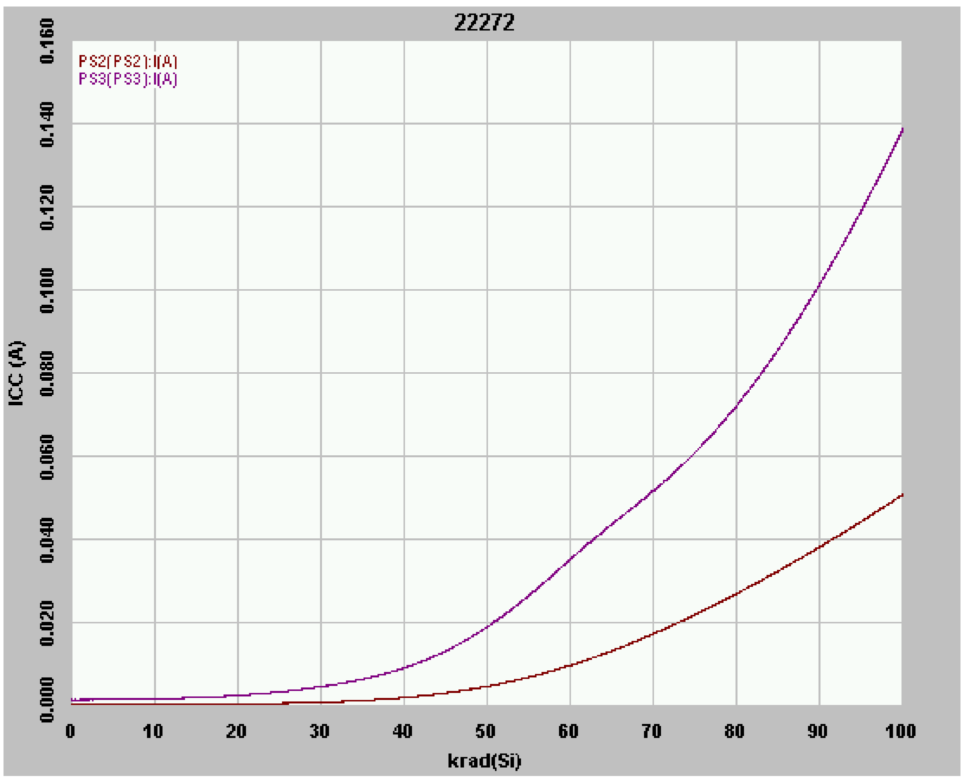


Fig 5 In-flux I_{CC} of DUT 22272, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

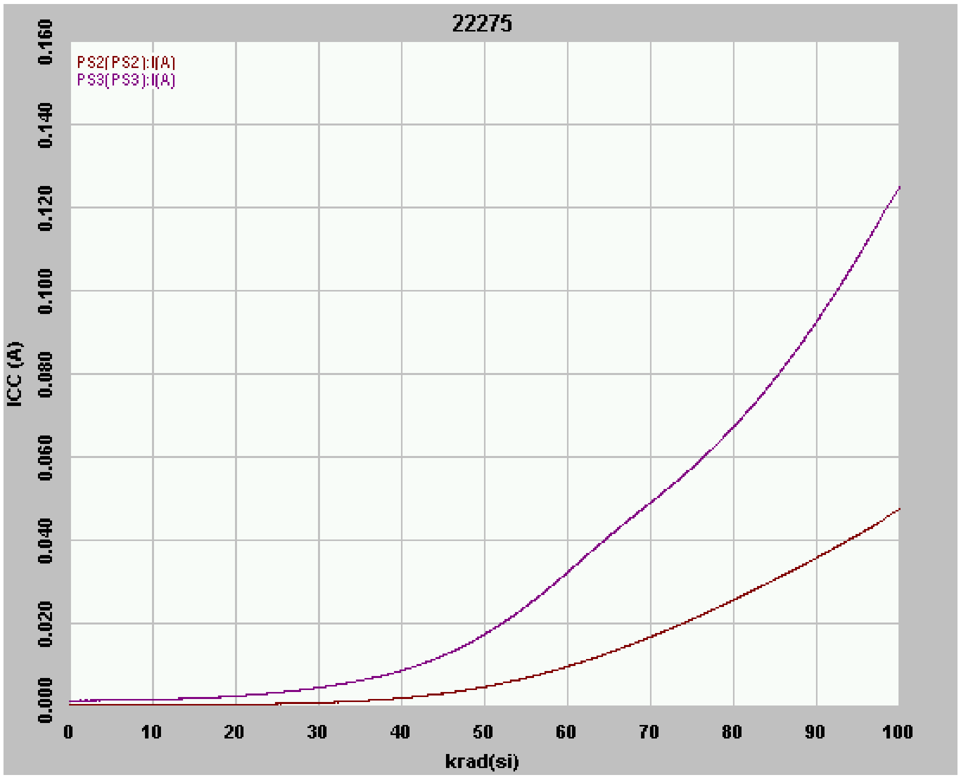


Fig 6 In-flux I_{CC} of DUT 22275, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

C. *Input Logic Threshold (V_{IL}/V_{IH})*

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4 Pre-irradiation and post-annealing input logic threshold in volts

DUT	Pre-Irradiation		Post-Annealing	
	V_{IL}	V_{IH}	V_{IL}	V_{IH}
22245	1.25	1.48	1.32	1.42
22253	1.38	1.43	1.33	1.42
22255	1.41	1.45	1.32	1.42
22272	1.40	1.45	1.31	1.41
22275	1.41	1.45	1.32	1.41

D. *Output Characteristics (V_{OL}/V_{OH})*

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in table 5 and 6. The post-annealing data are within the spec limits, and 100 krad(Si) radiation has little effect on these parameters.

Table 5 Pre-irradiation and post-annealing V_{OL} (in volts) at various sinking current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
22245	0.009	0.010	0.100	0.110	0.170	0.180	0.430	0.430	0.880	0.890
22253	0.010	0.010	0.120	0.120	0.200	0.200	0.490	0.490	1.000	1.000
22255	0.009	0.020	0.100	0.110	0.170	0.180	0.430	0.430	0.880	0.880
22272	0.009	0.010	0.100	0.110	0.170	0.180	0.430	0.430	0.880	0.890
22275	0.009	0.010	0.100	0.110	0.170	0.170	0.430	0.430	0.880	0.880

Table 6 Pre-irradiation and post-annealing V_{OH} (in volts) at various sourcing current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
22245	4.990	4.980	4.870	4.860	4.670	4.660	4.130	4.120	3.050	3.020
22253	4.990	4.980	4.860	4.860	4.640	4.640	4.060	4.050	2.910	2.890
22255	4.990	4.980	4.870	4.860	4.660	4.650	4.120	4.100	3.020	2.970
22272	4.990	4.980	4.870	4.860	4.660	4.660	4.120	4.100	3.020	2.980
22275	4.990	4.980	4.870	4.860	4.660	4.650	4.120	4.100	3.020	2.960

E. Propagation Delays

Tables 7 and 8 list the pre-irradiation and post-annealing propagation delays, and radiation-induced degradations. The radiation-induced degradations are less than 5%.

Table 7 Low to high delays (in nanoseconds)

DUT	Pre-Irradiation	Post-Anneal	Degradation (%)
22245	1233.6	1287.4	4.36
22253	1238.8	1243.5	0.38
22255	1235.9	1262.4	2.14
22272	1245.9	1300.5	4.38
22275	1236.6	1266.7	2.43

Table 8 High to low delays (in nanoseconds)

DUT	Pre-Irradiation	Post-Anneal	Degradation (%)
22245	1085.9	1133.1	4.35
22253	1077.0	1083.7	0.62
22255	1091.6	1114.0	2.05
22272	1080.8	1125.4	4.13
22275	1093.7	1116.1	2.05

F. Transition Time

The post-annealing rising and falling edges are plotted in Figs 8-12. In every case, the transition time is approximately 2 nanoseconds.

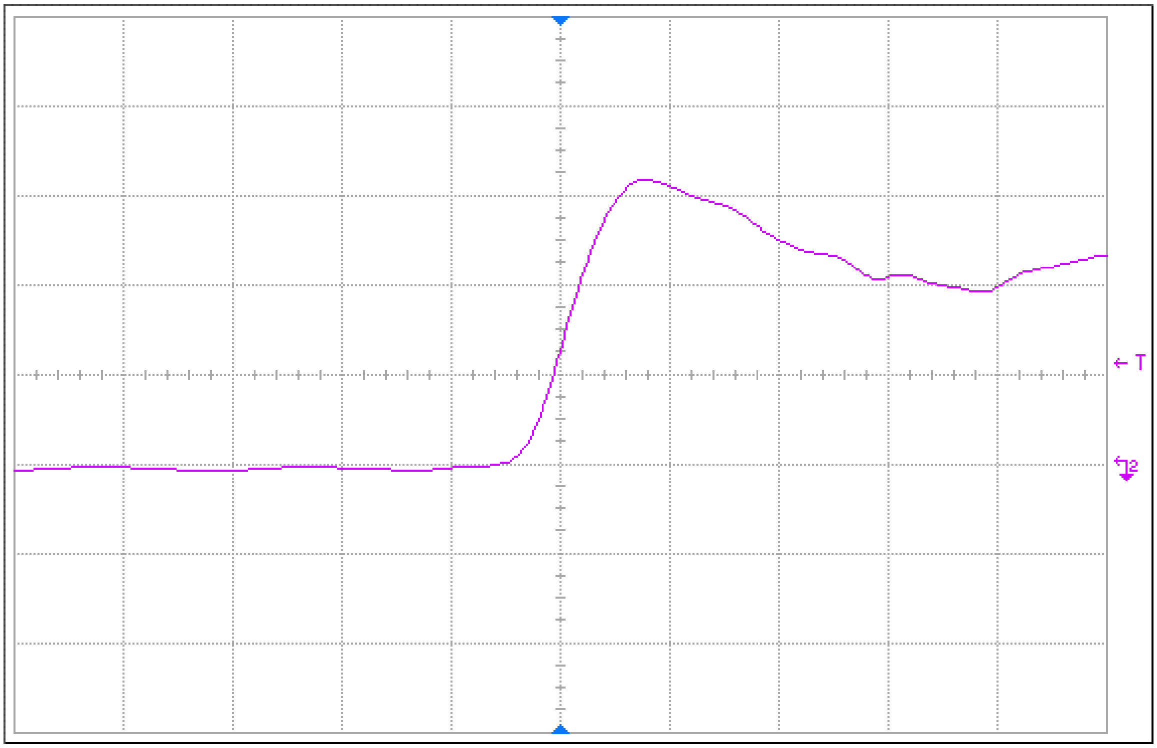


Fig 8(a) Post-annealing rising edge of DUT 22245, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

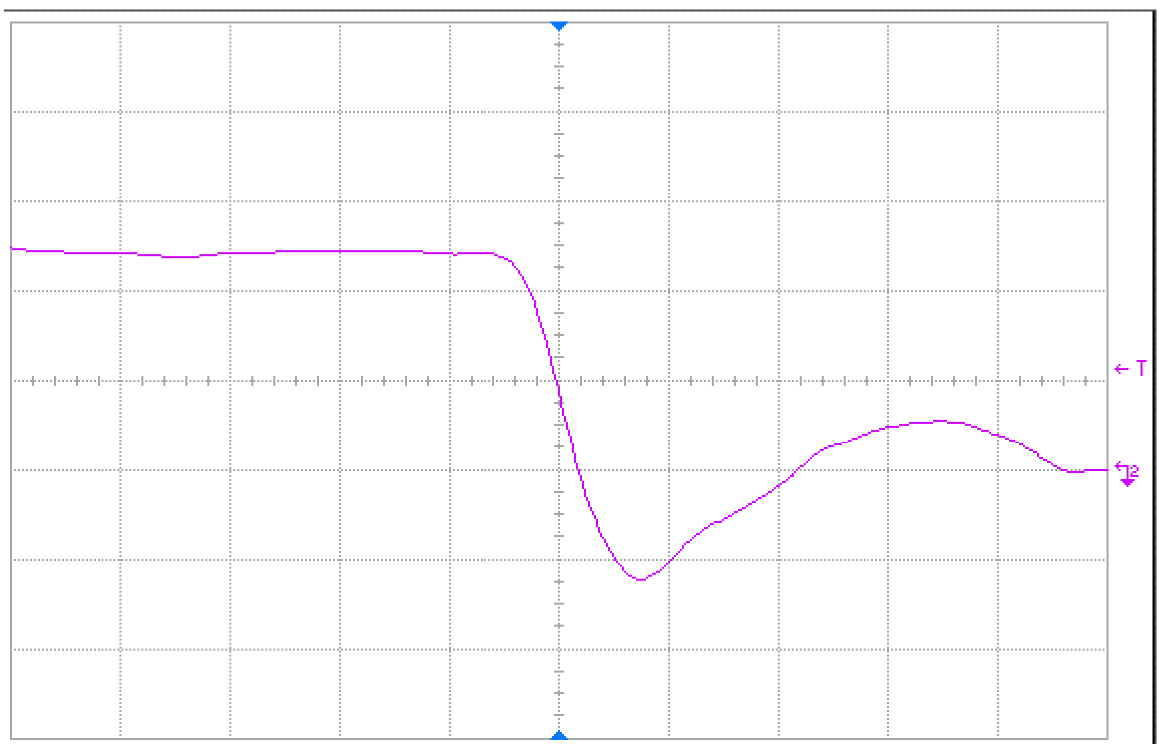


Fig 8(b) Post-annealing falling edge of DUT 22245, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

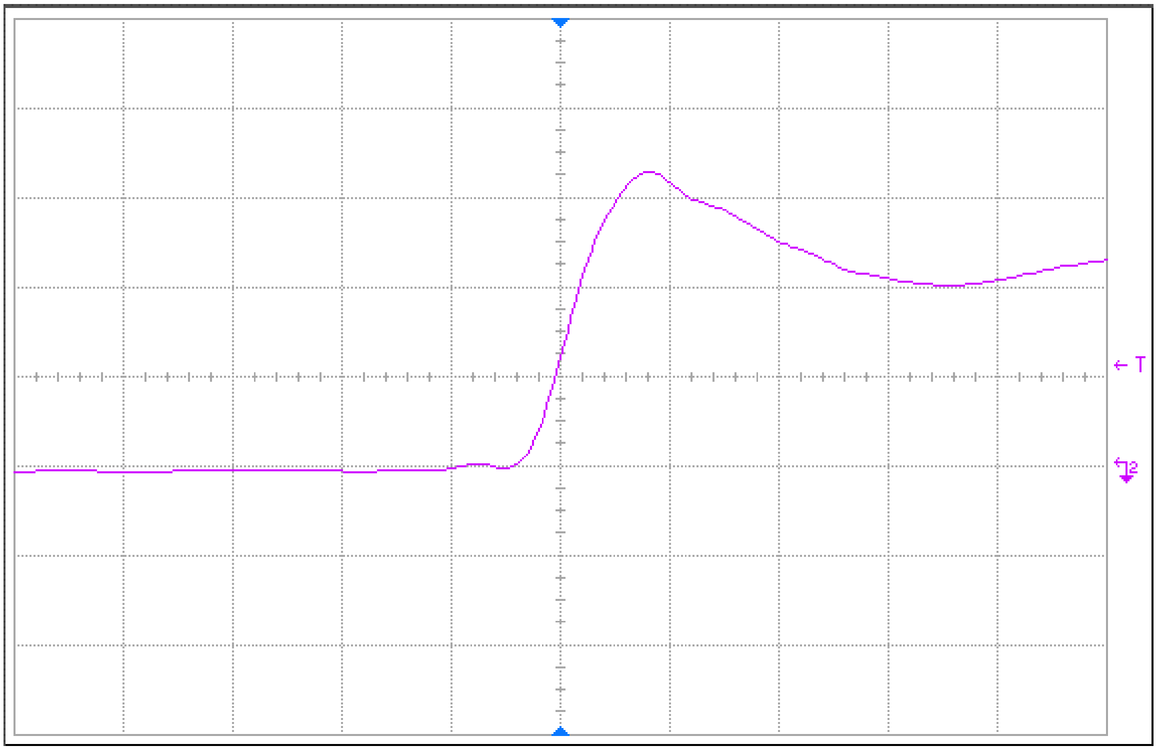


Fig 9(a) Post-annealing rising edge of DUT 22253, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

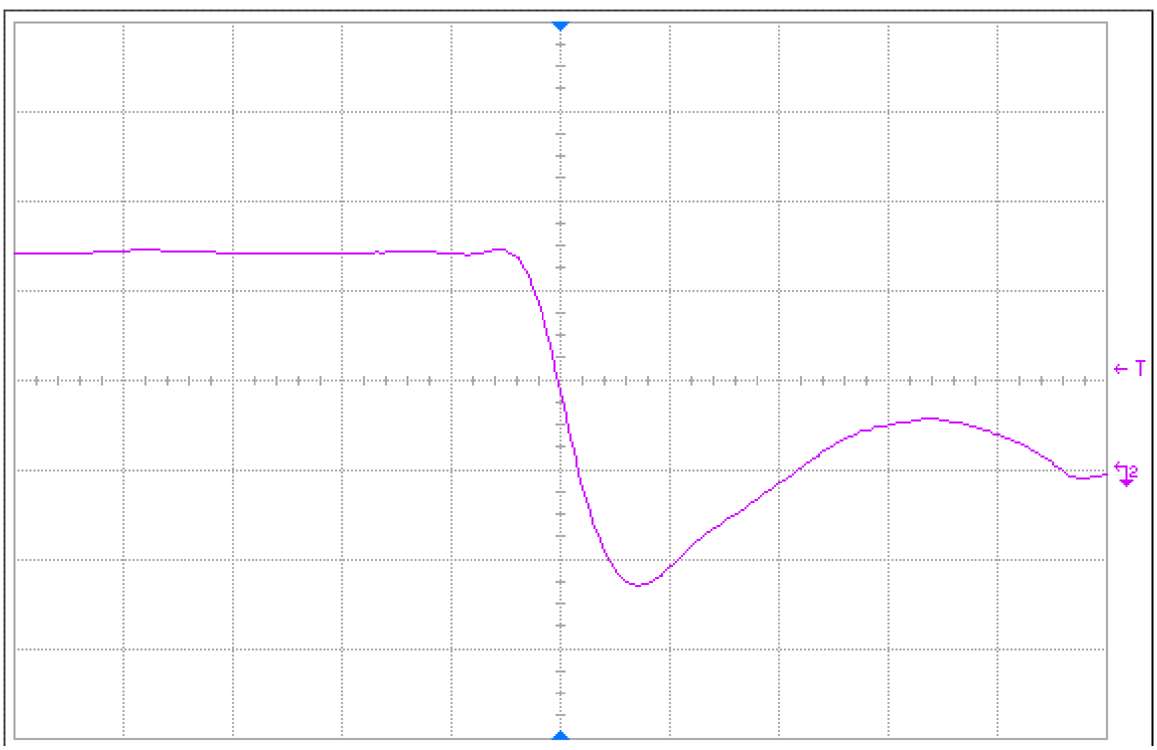


Fig 9(b) Post-annealing falling edge of DUT 22253, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

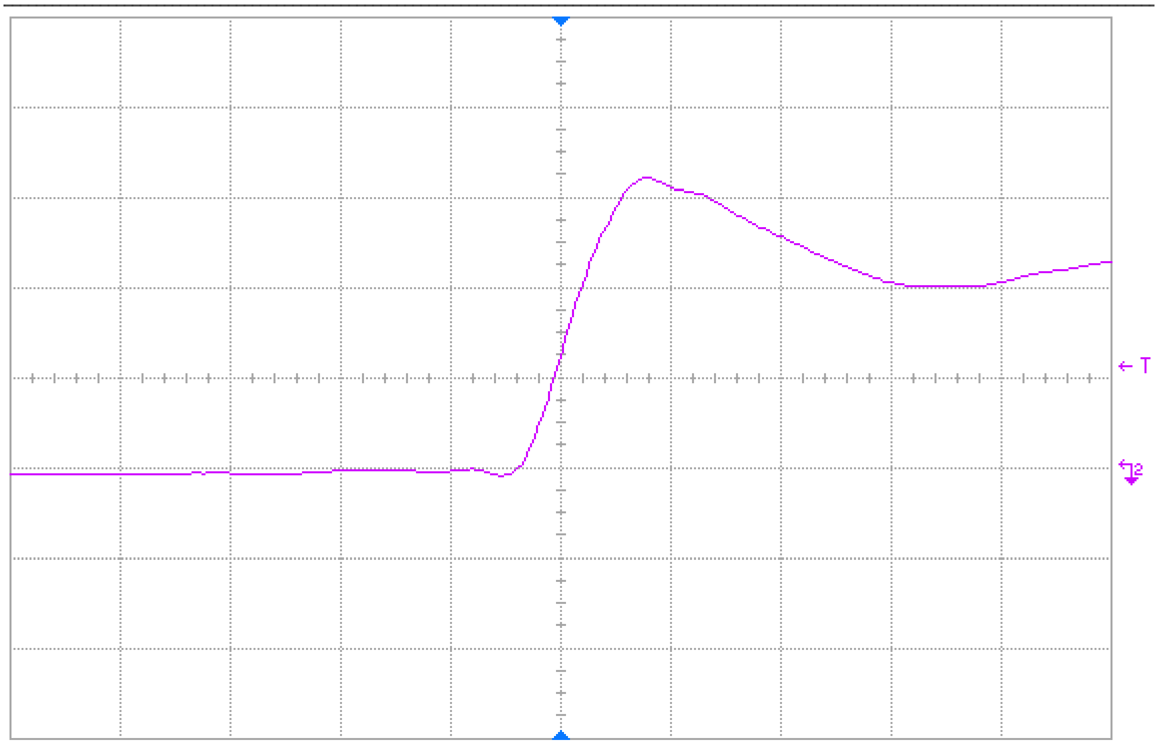


Fig 10(a) Post-annealing rising edge of DUT 22255, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

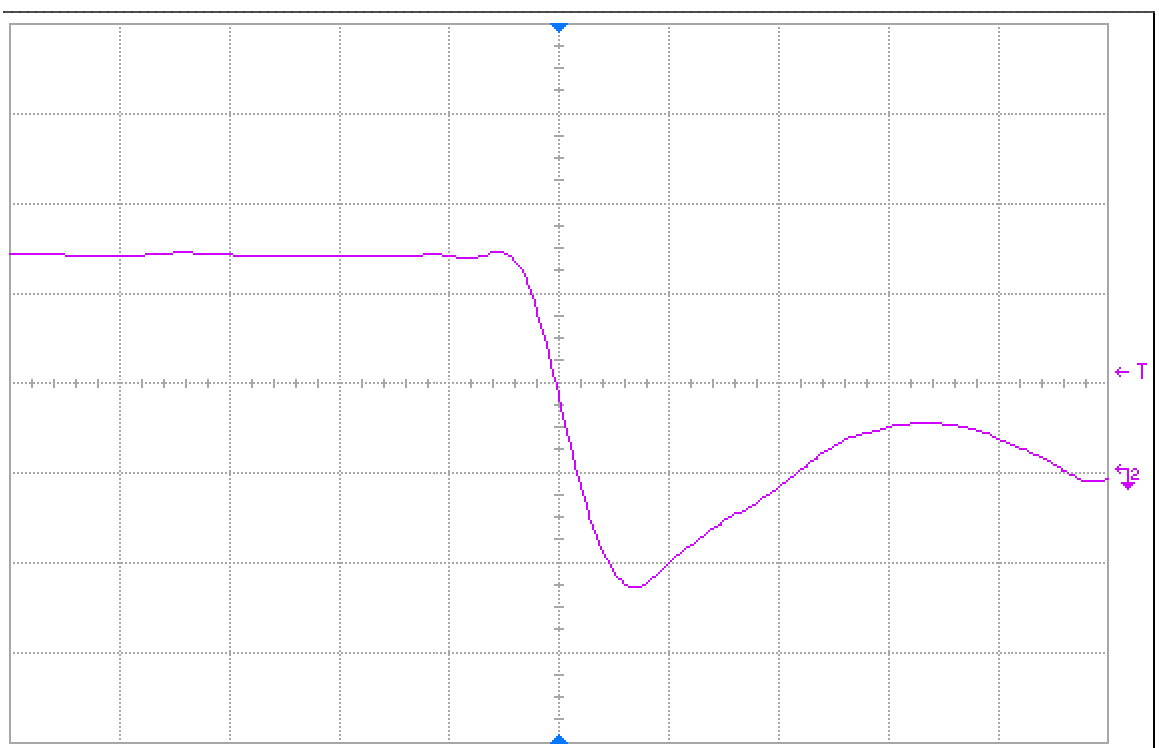


Fig 10(b) Post-annealing falling edge of DUT 22255, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

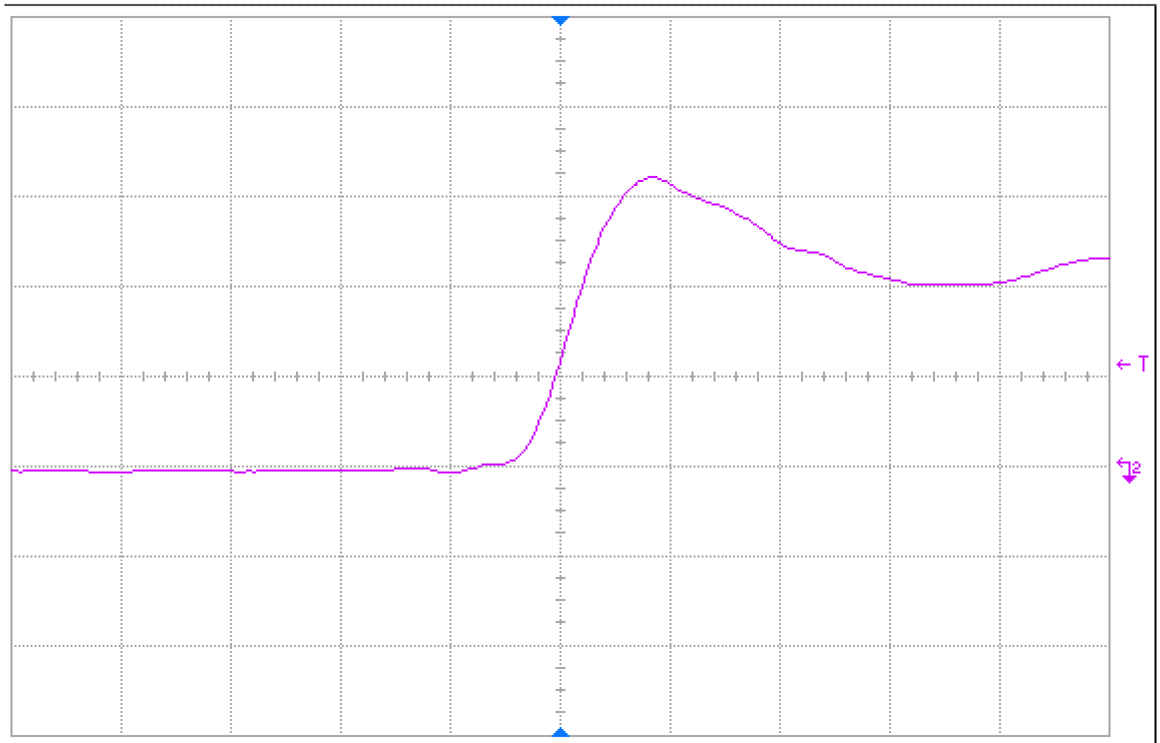


Fig 11(a)   Post-annealing rising edge of DUT 22272, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

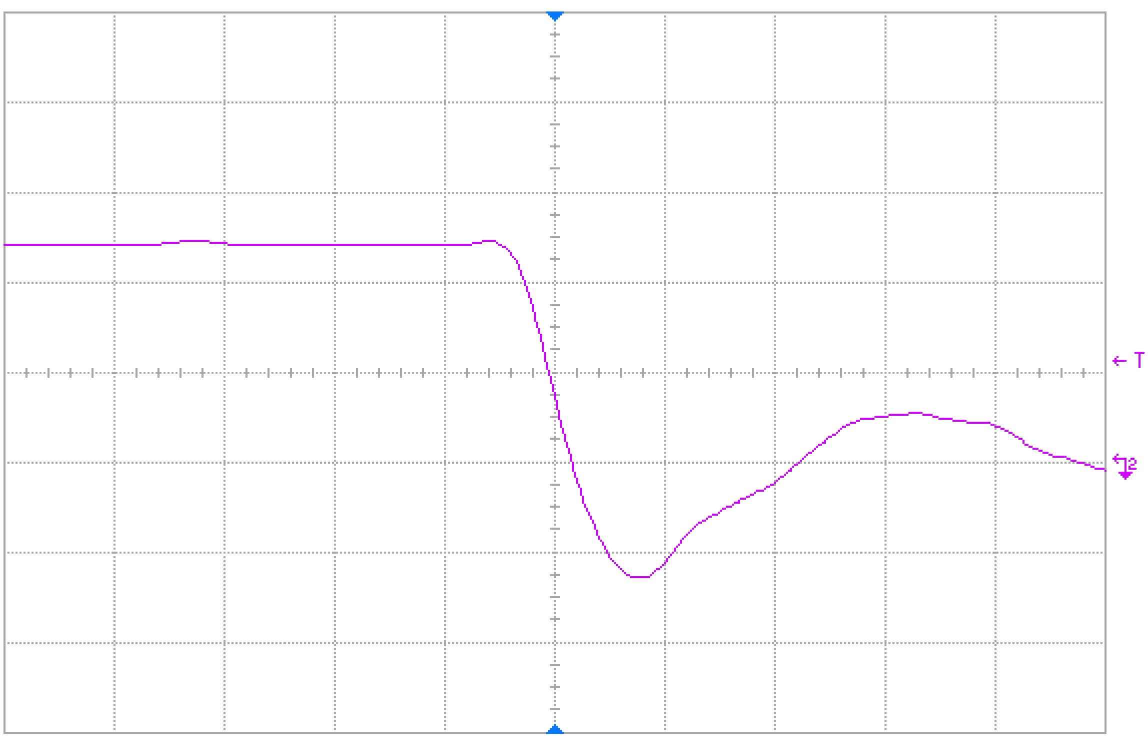


Fig 11(b)   Post-annealing falling edge of DUT 22272, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

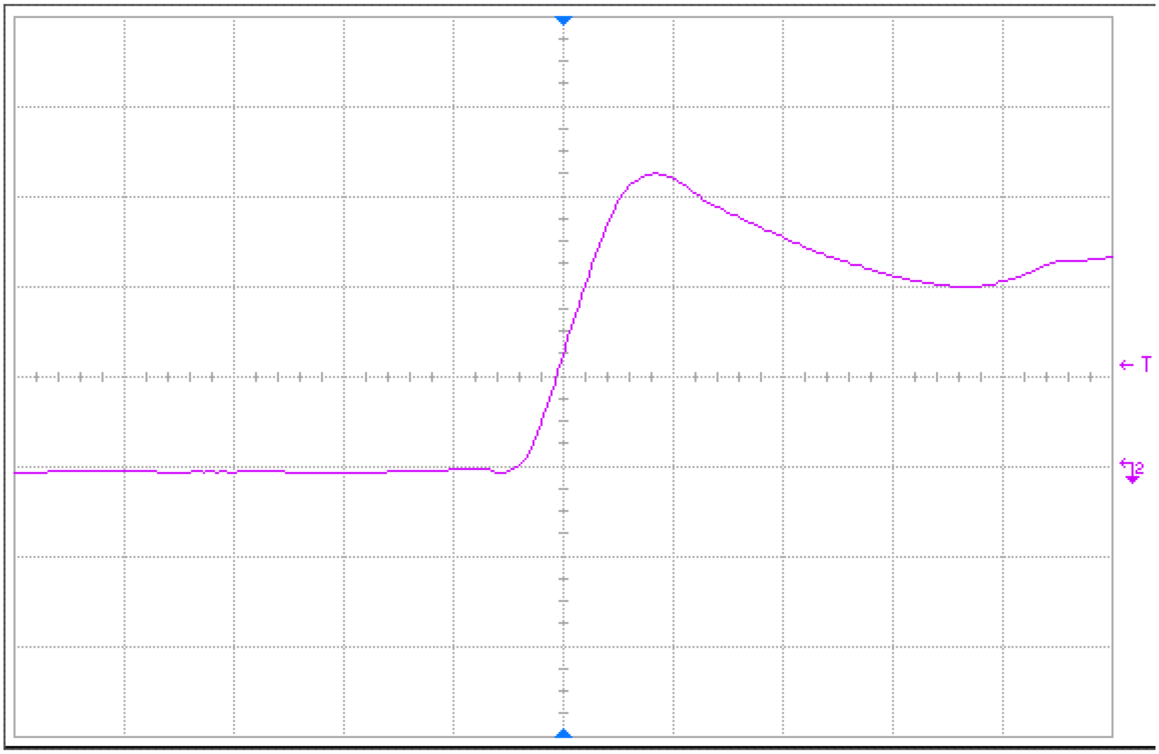


Fig 12(a) Post-annealing rising edge of DUT 22275, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

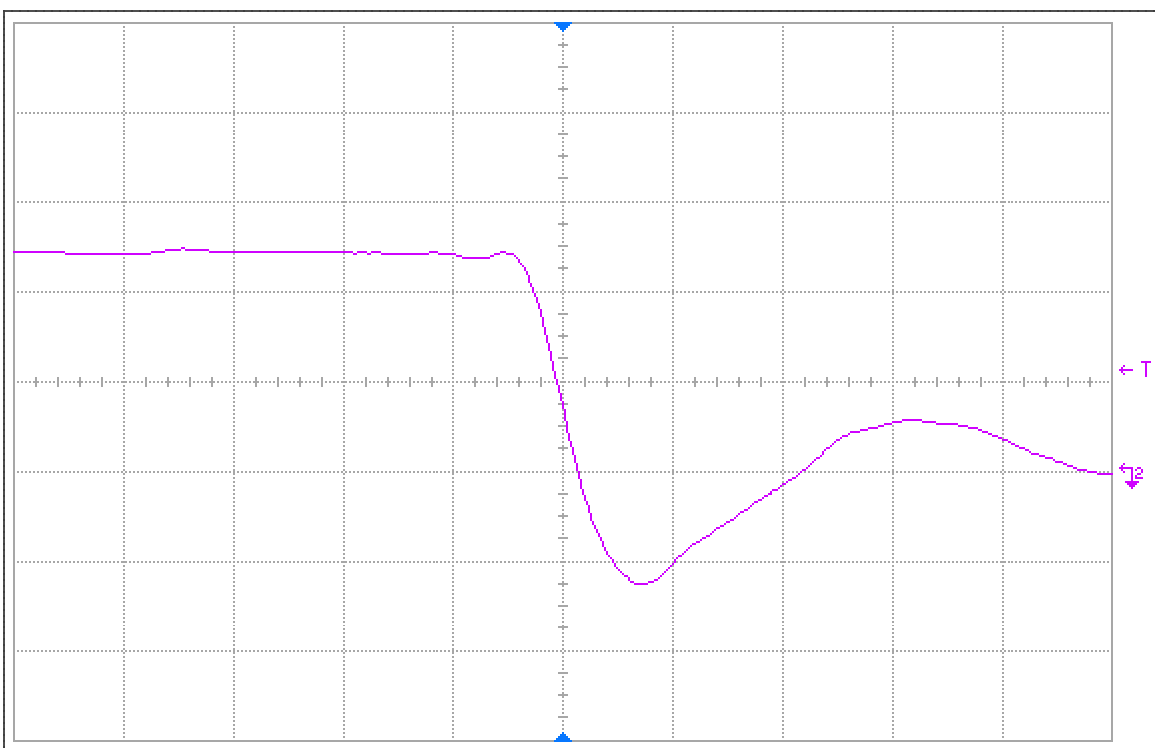
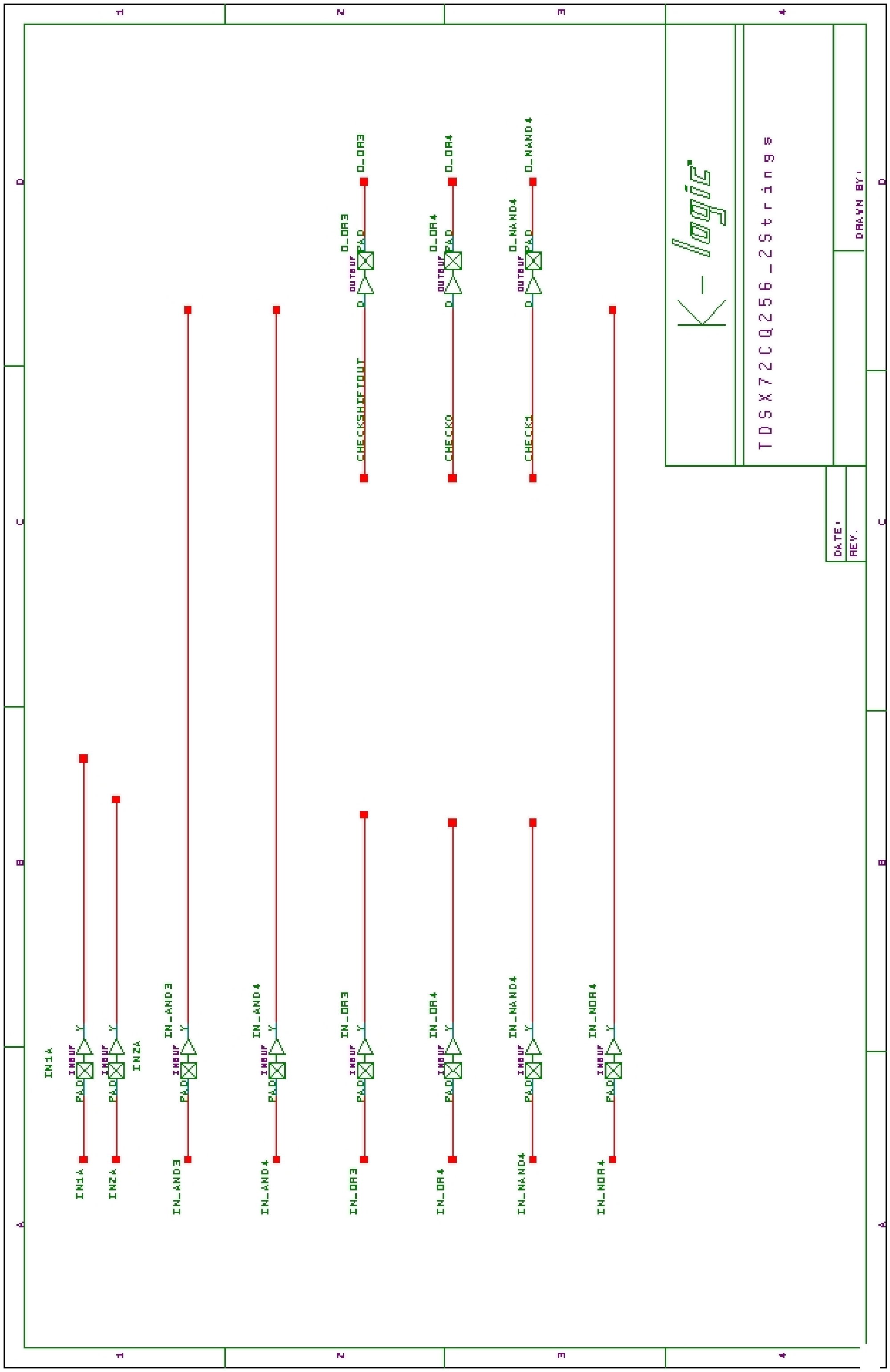
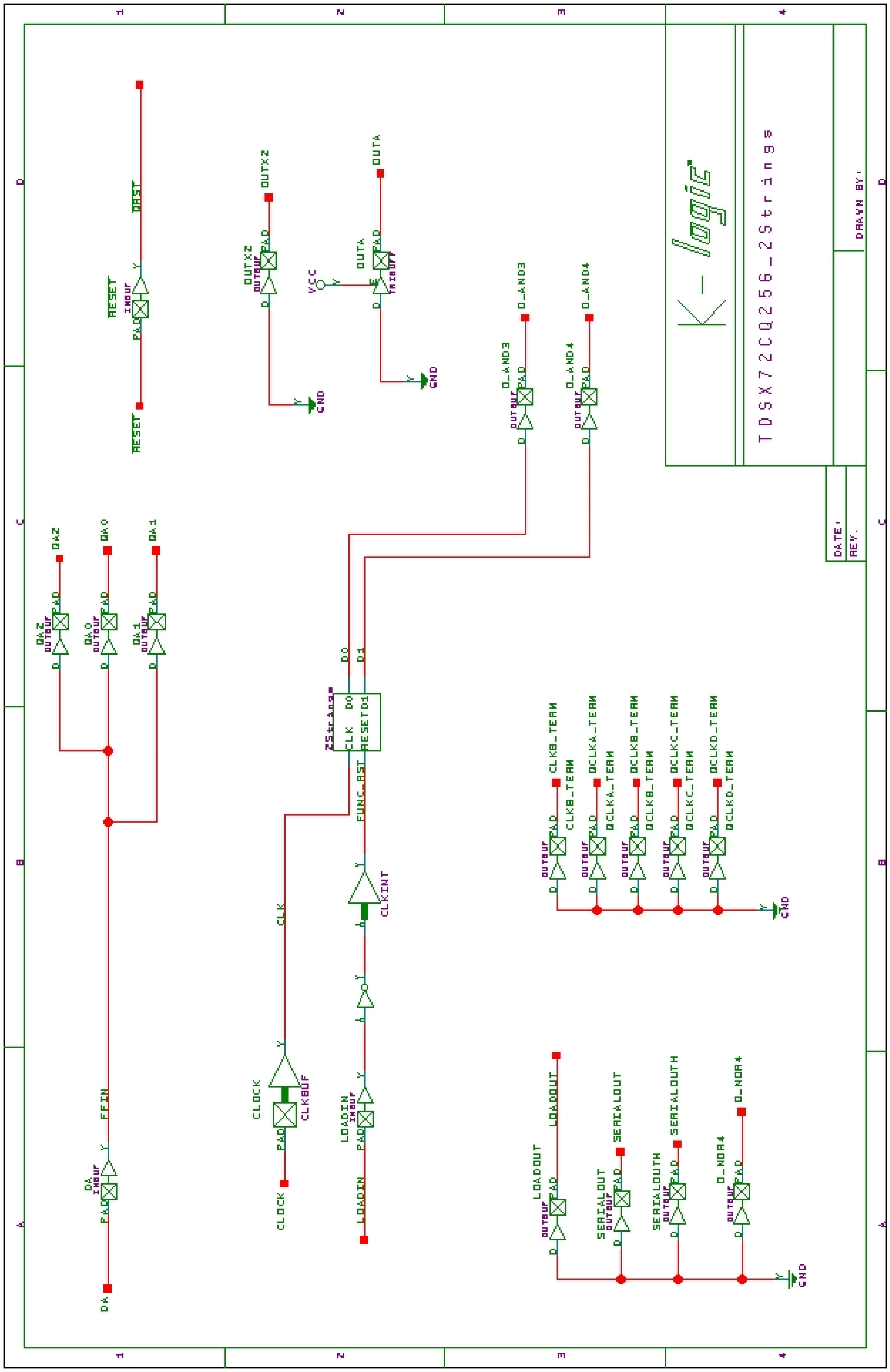
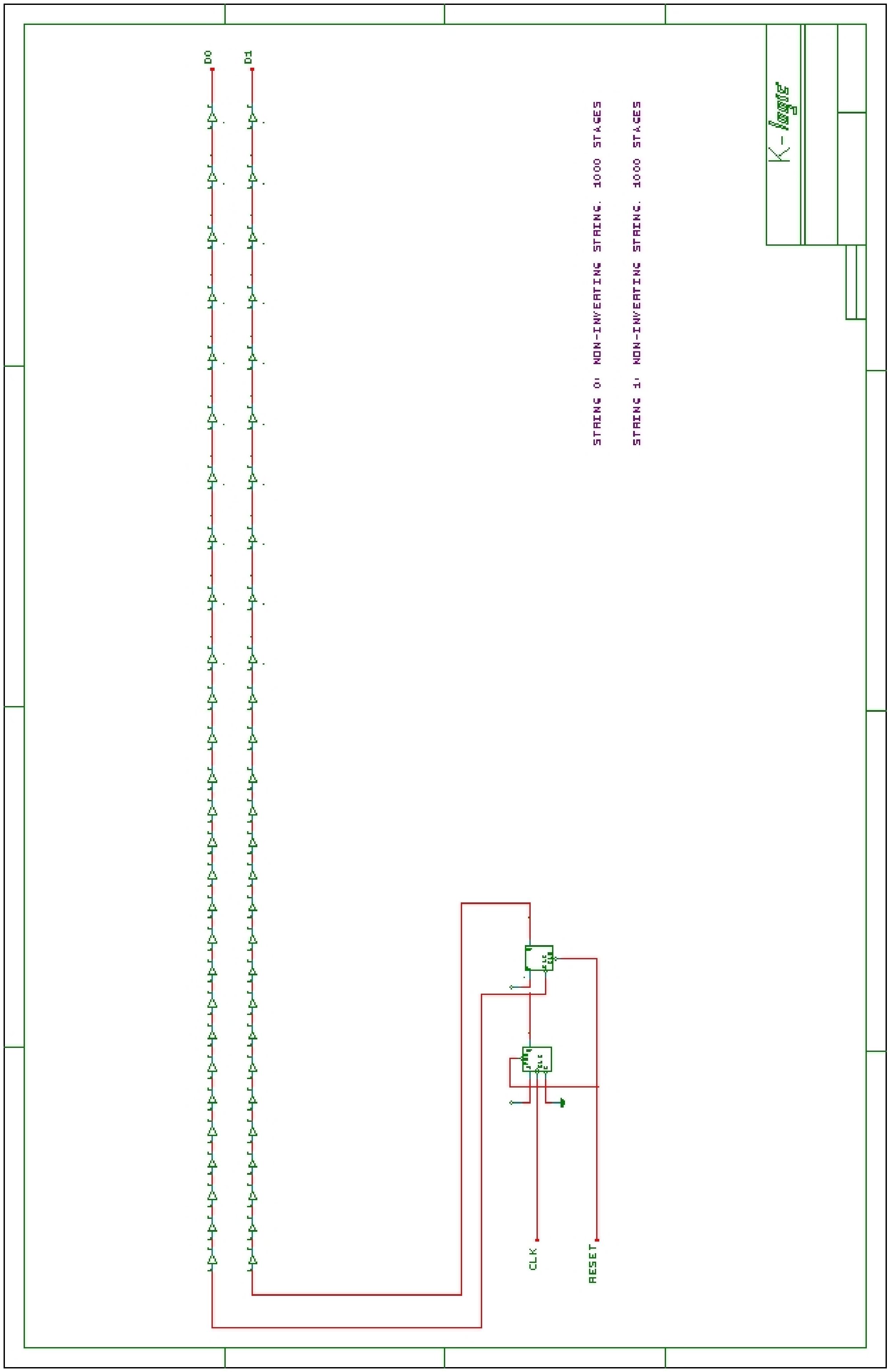


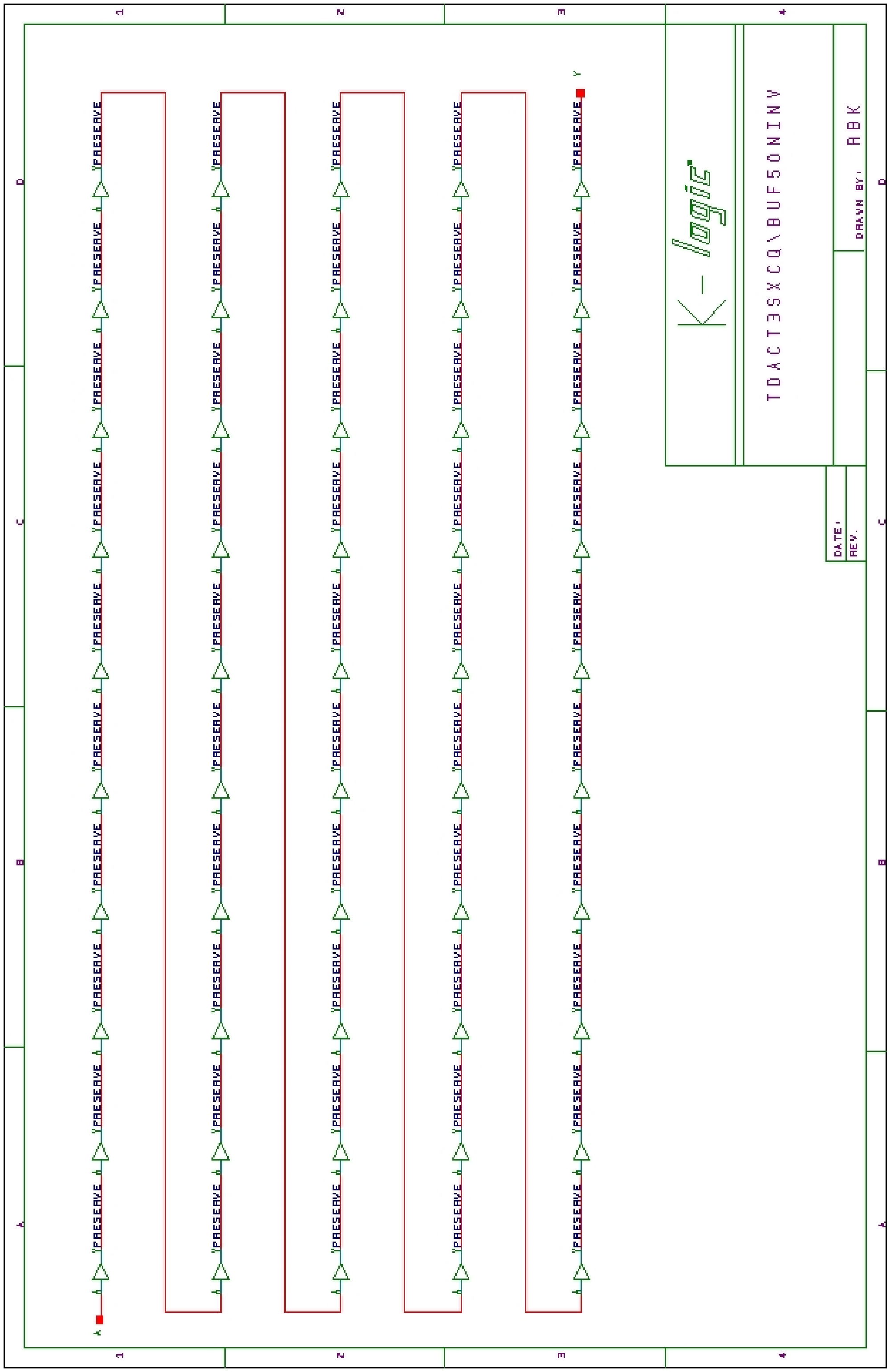
Fig 12(b) Post-annealing falling edge of DUT 22275, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

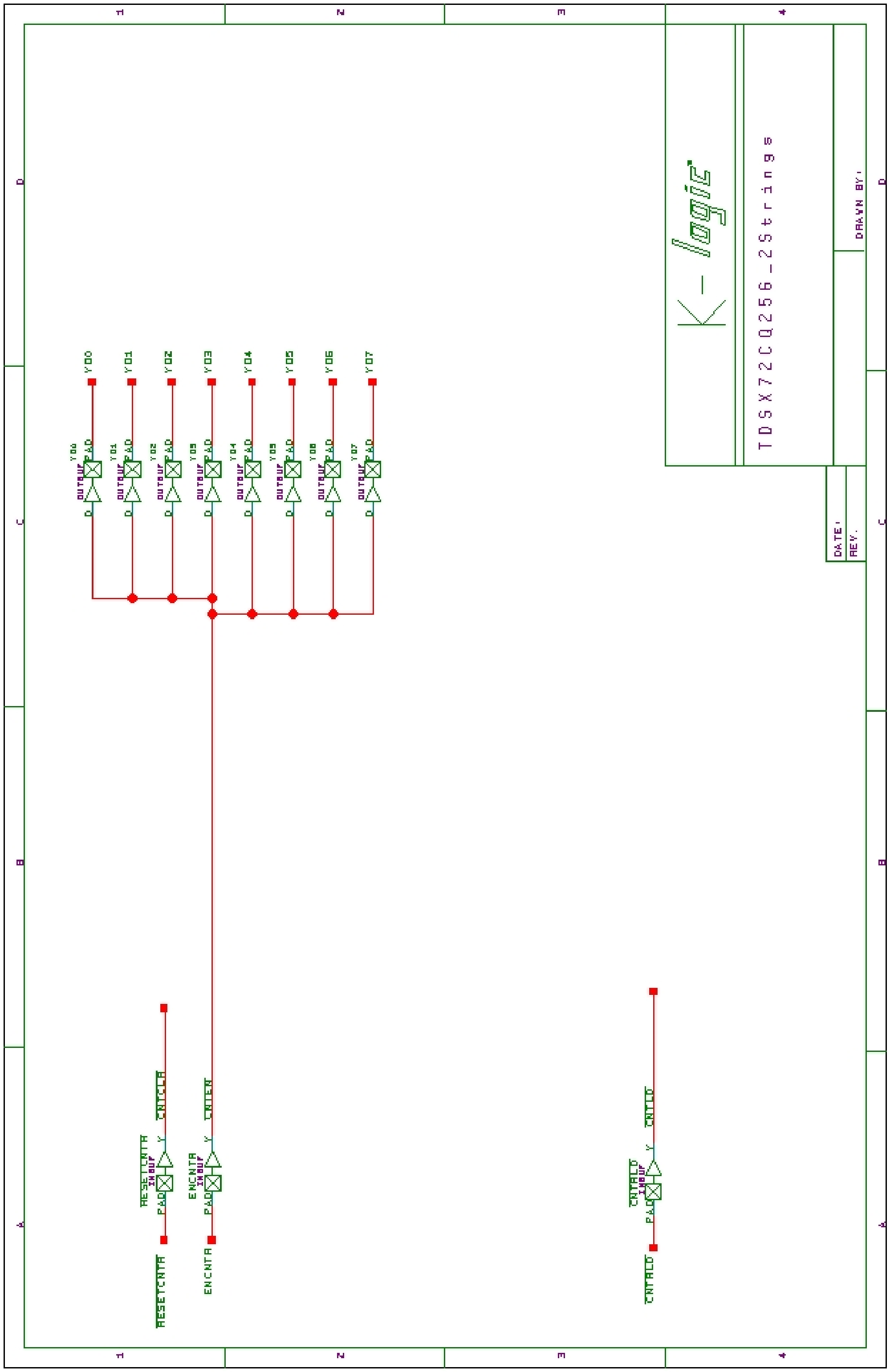
APPENDIX A DUT DESIGN SCHEMATICS



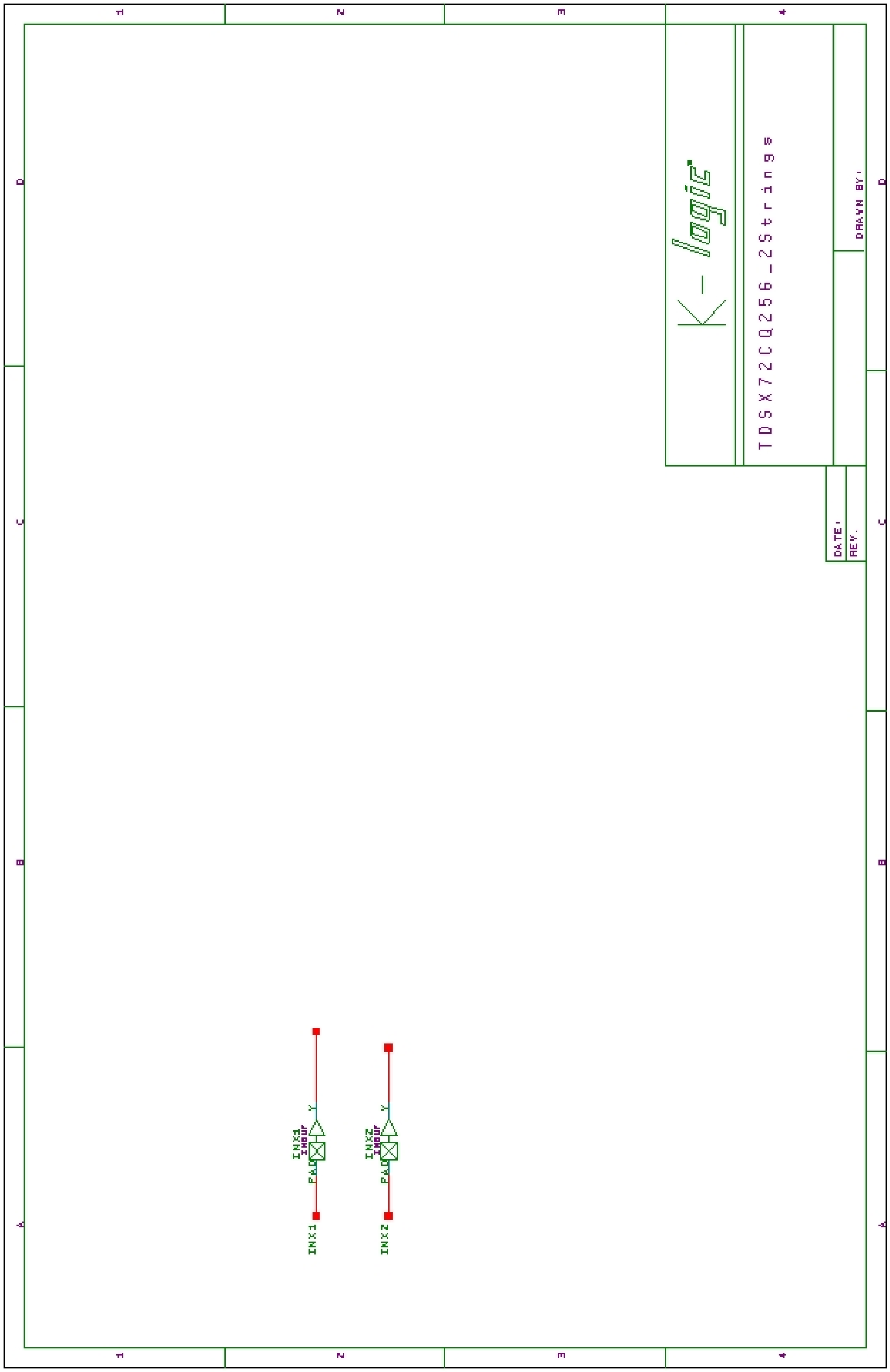

TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
QRST
OUTX2
OUTA
VCC
GND
QA2
QA0
QA1
D_AND3
D_AND4
2Strings
CLK
RESET
D0
D1
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
INBUF
OUTBUF
DA
FFIN
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4
CLKB_TERM
QCLKA_TERM
QCLKB_TERM
QCLKC_TERM
QCLKD_TERM

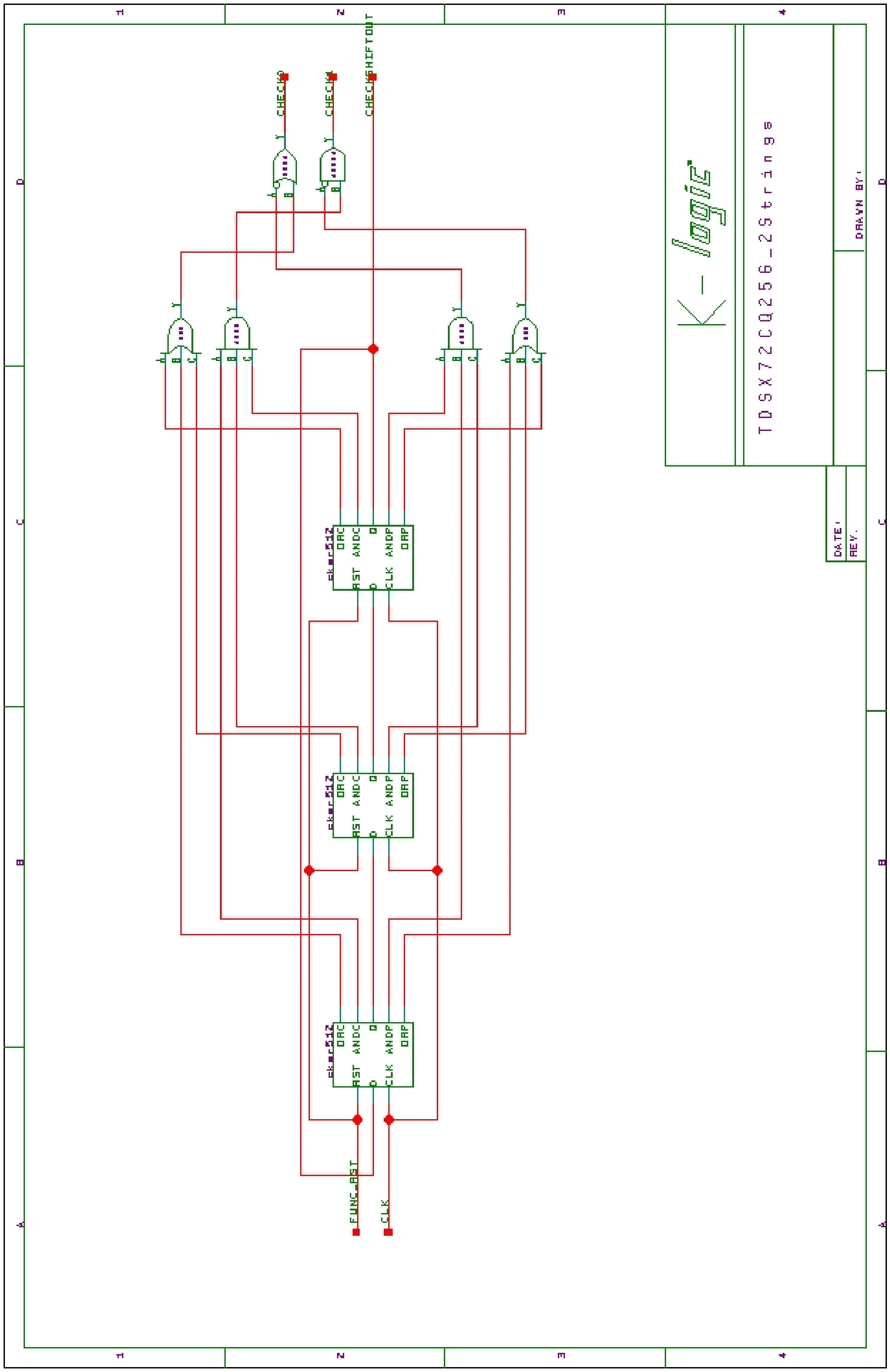

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
CLK
RESET

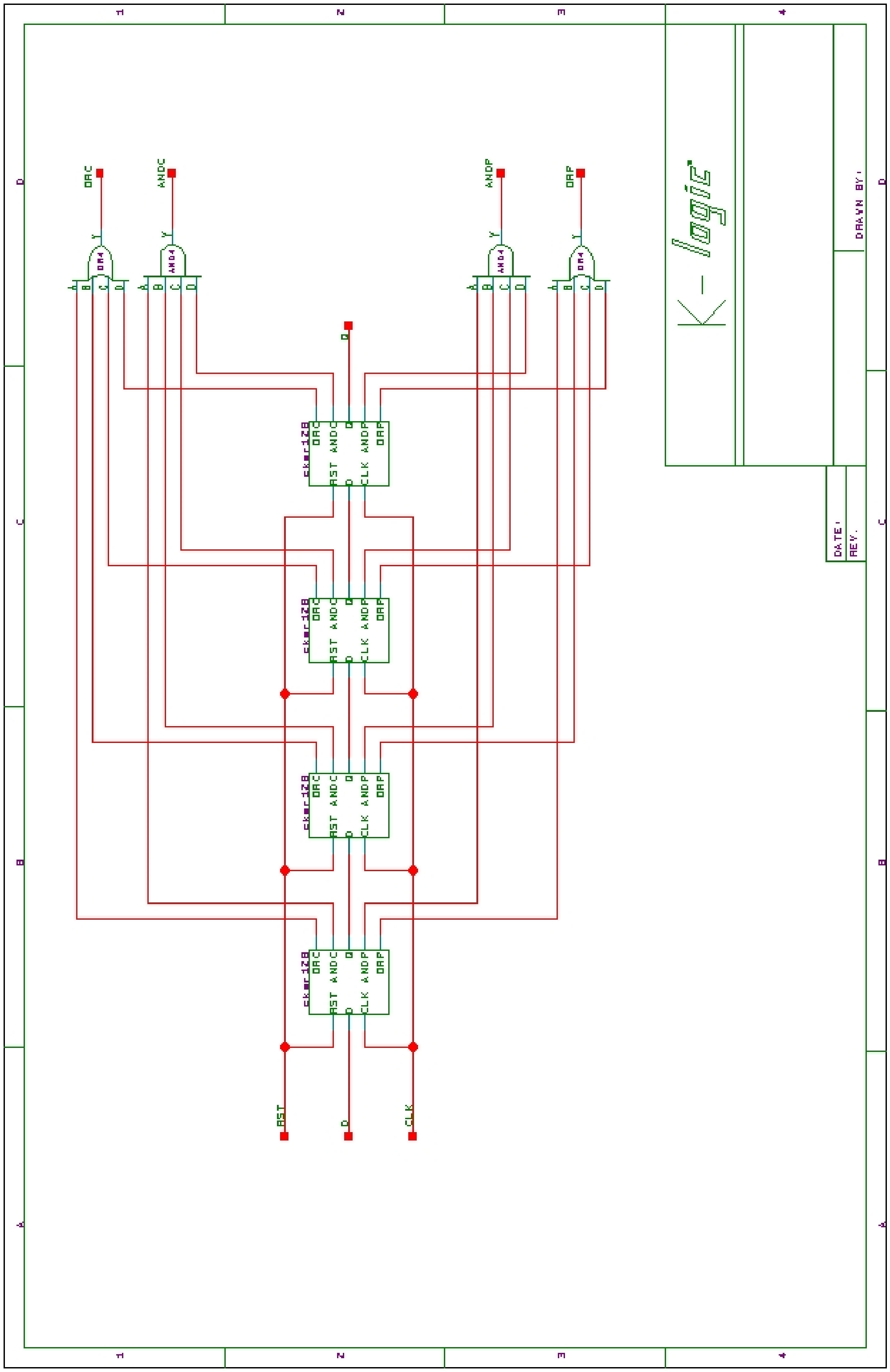

K-logic
TDACT3SXCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
A
Y
PRESERVE

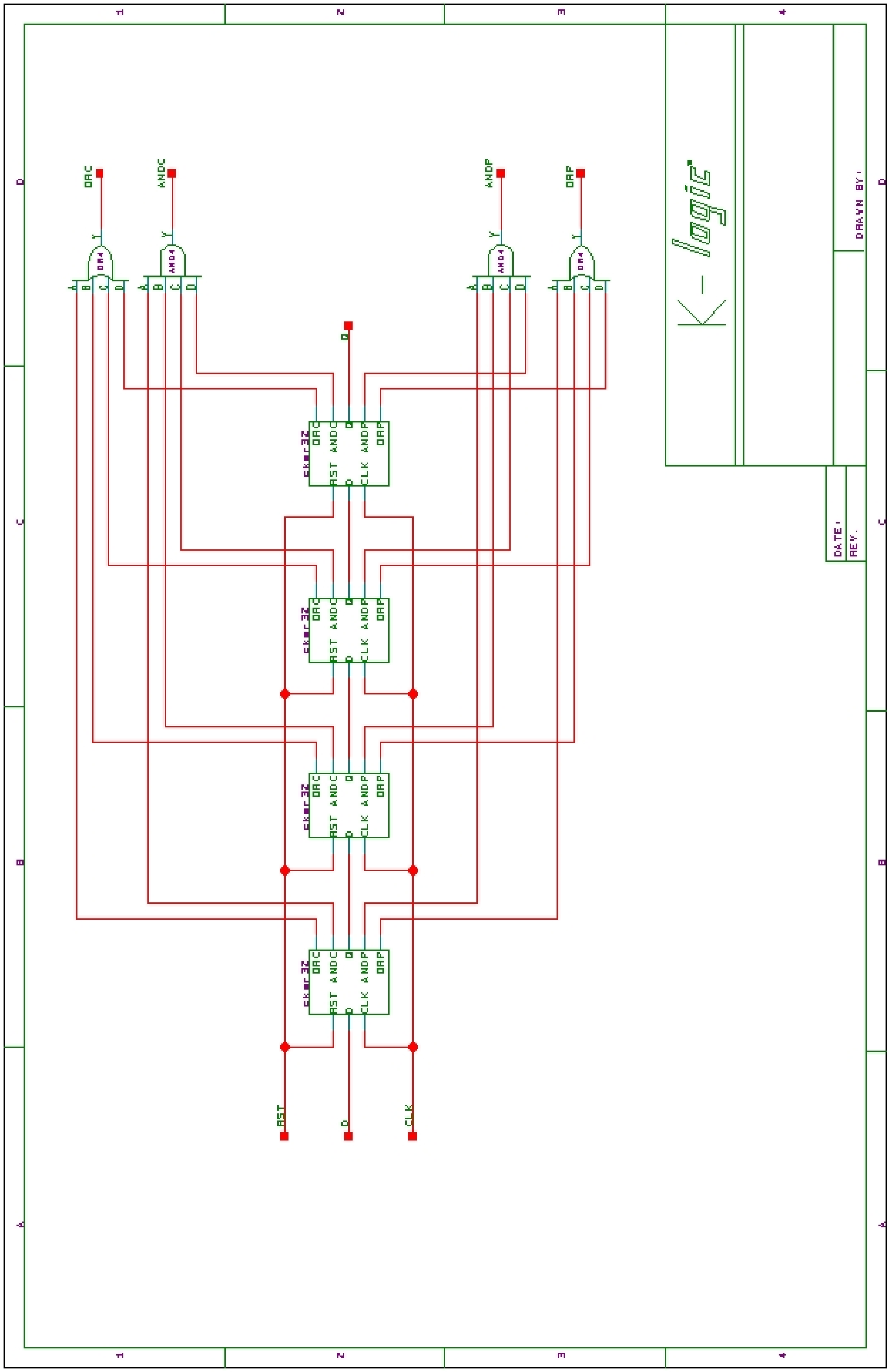


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
RESETCNTA
CNTCLR
ENCNTA
CNTEN
INBUF
CNTALD
CNTLD

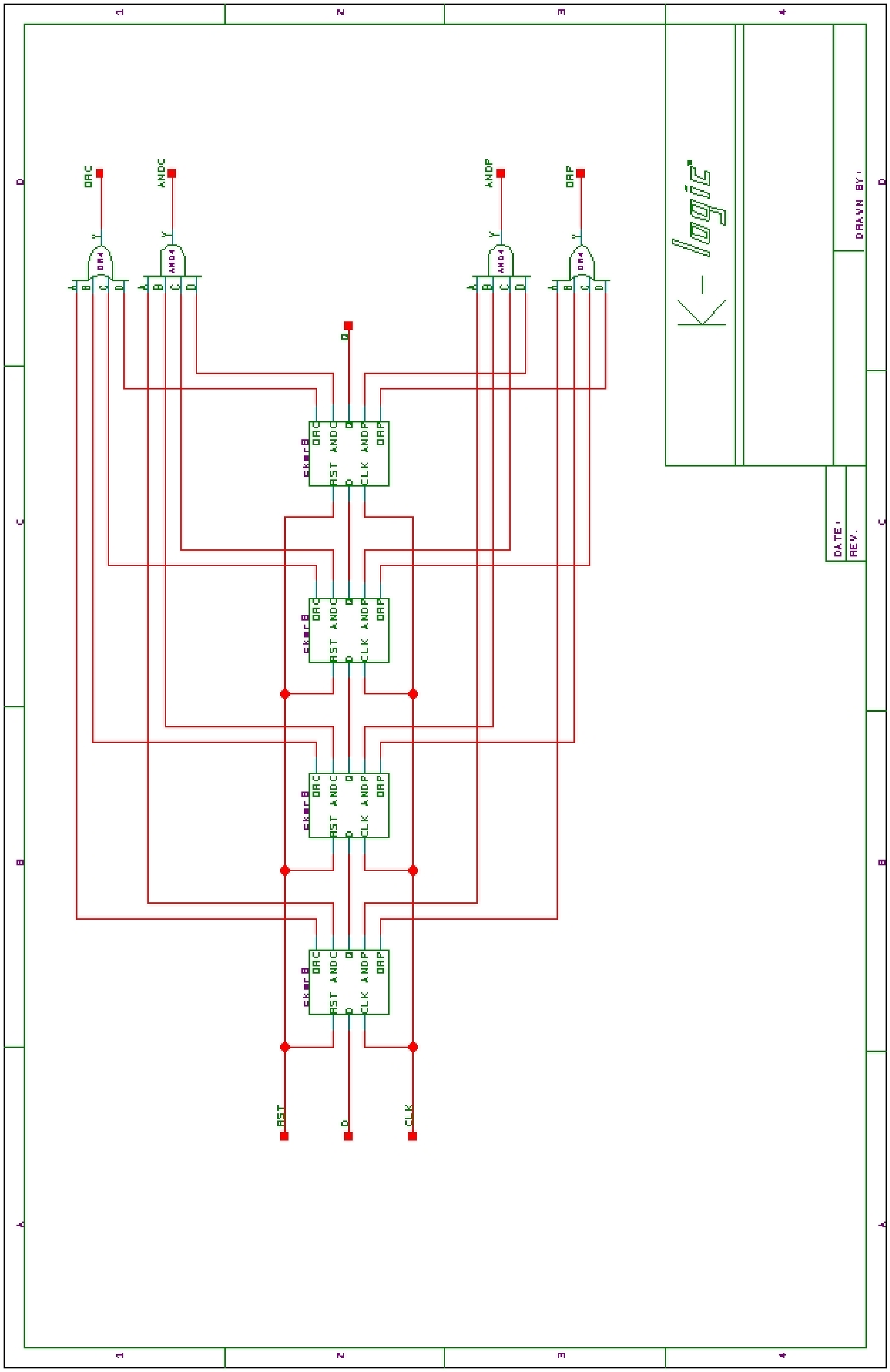

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2
INBUF
Y

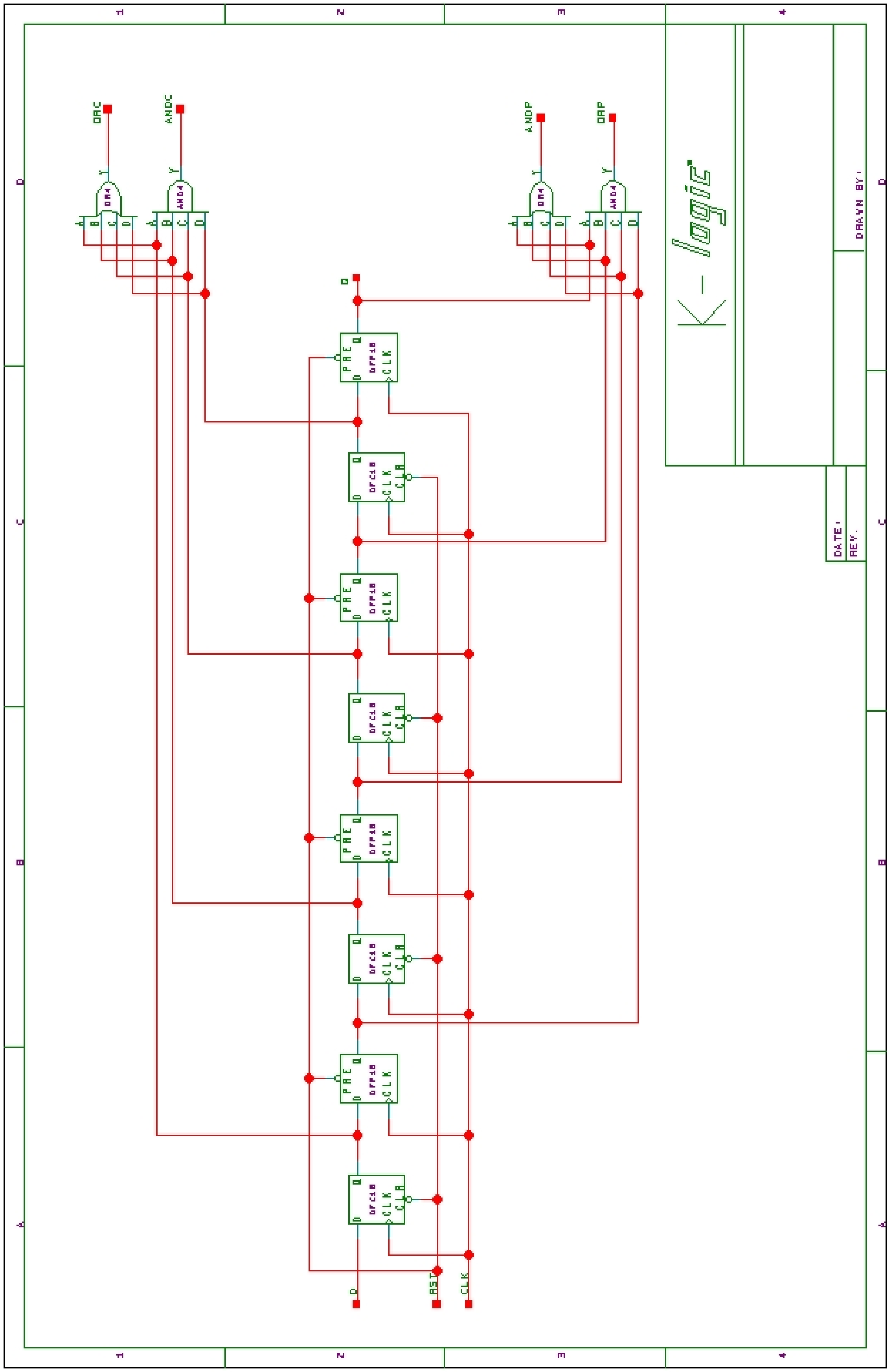

CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:

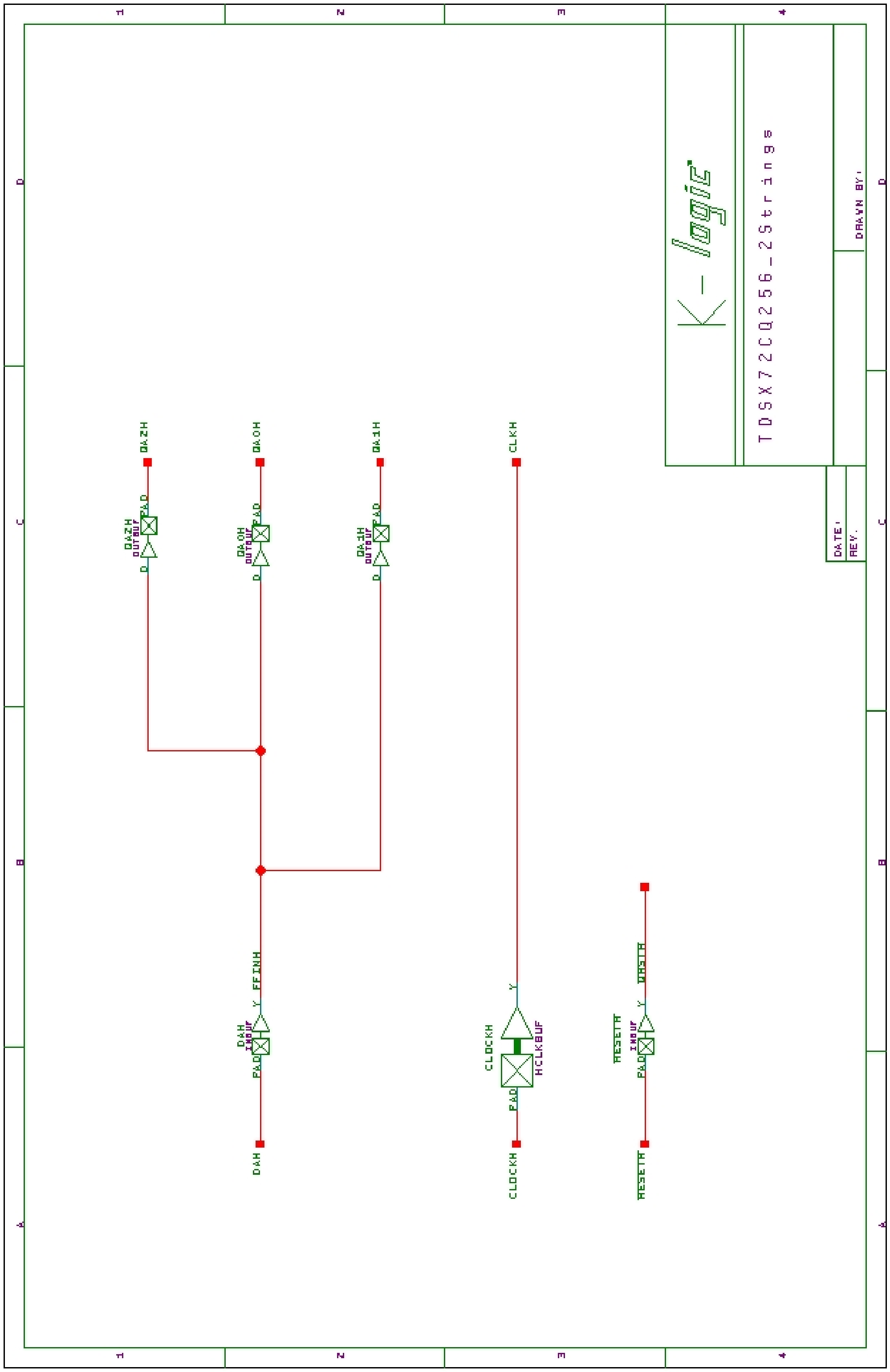

ORC
ANDC
ANDP
ORP
Q
ckmr128
RST
D
CLK
K-logic
DATE:
REV.
DRAWN BY:



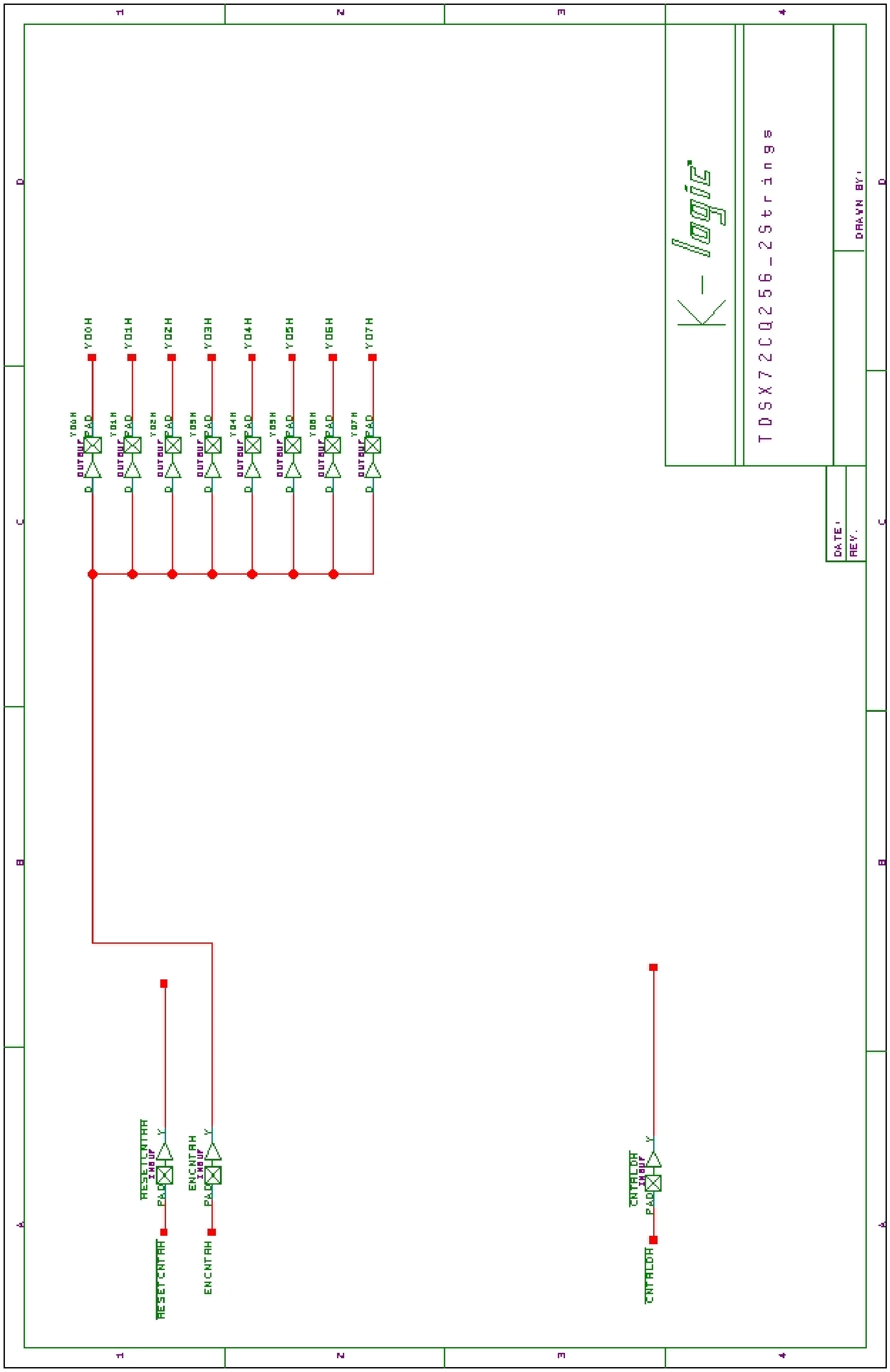
ORC
ANDC
ANDP
ORP
OR4
AND4
ckmr32
RST
D
CLK
Q
K-logic
DRAWN BY:
DATE:
REV.


ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
ckmrB
DATE:
REV.
DRAWN BY:

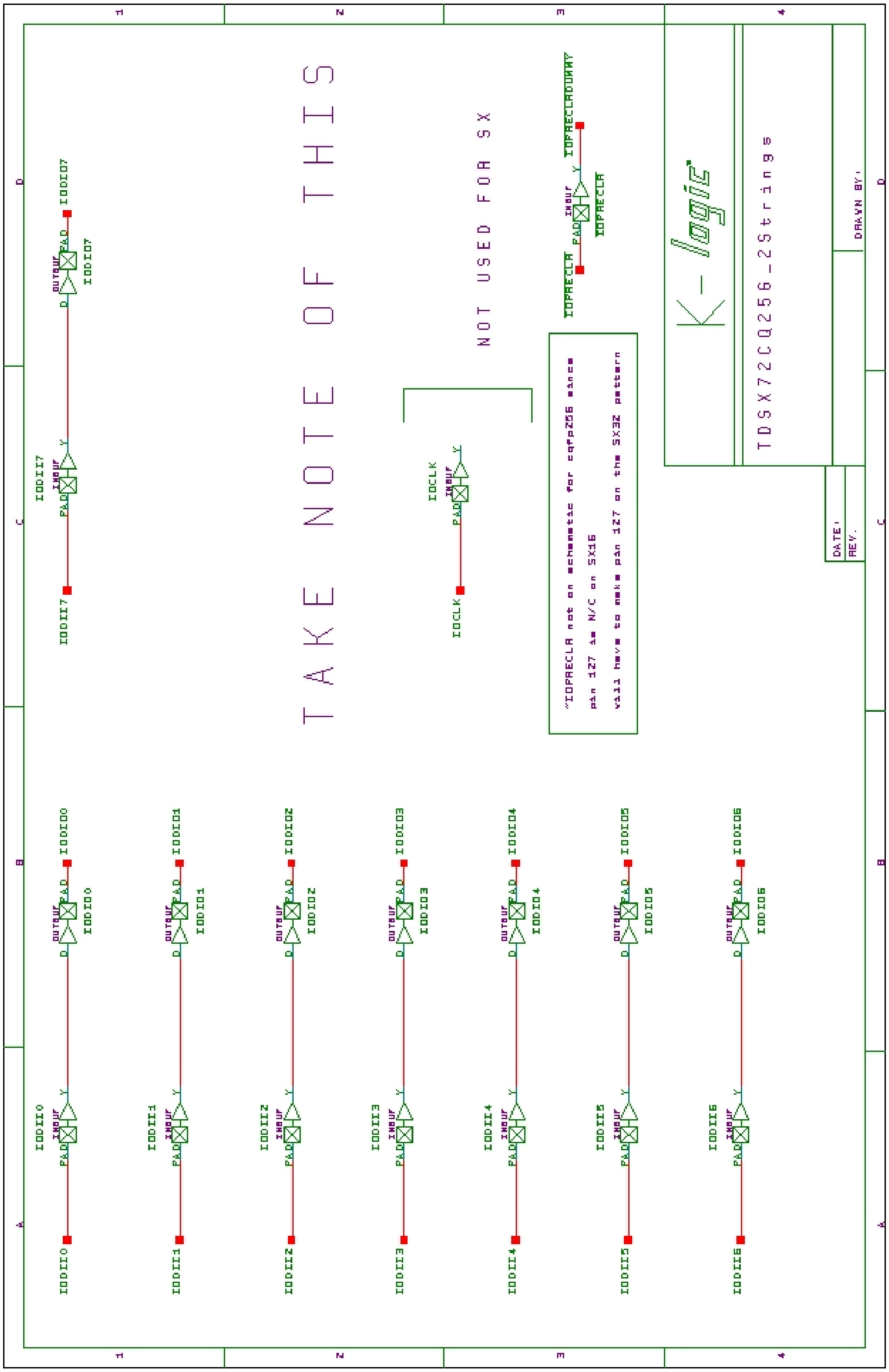

ORC
ANDC
ANDP
ORP
OR4
AND4
DFF1B
DFC1B
Q
D
RST
CLK
DATE:
REV.
DRAWN BY:



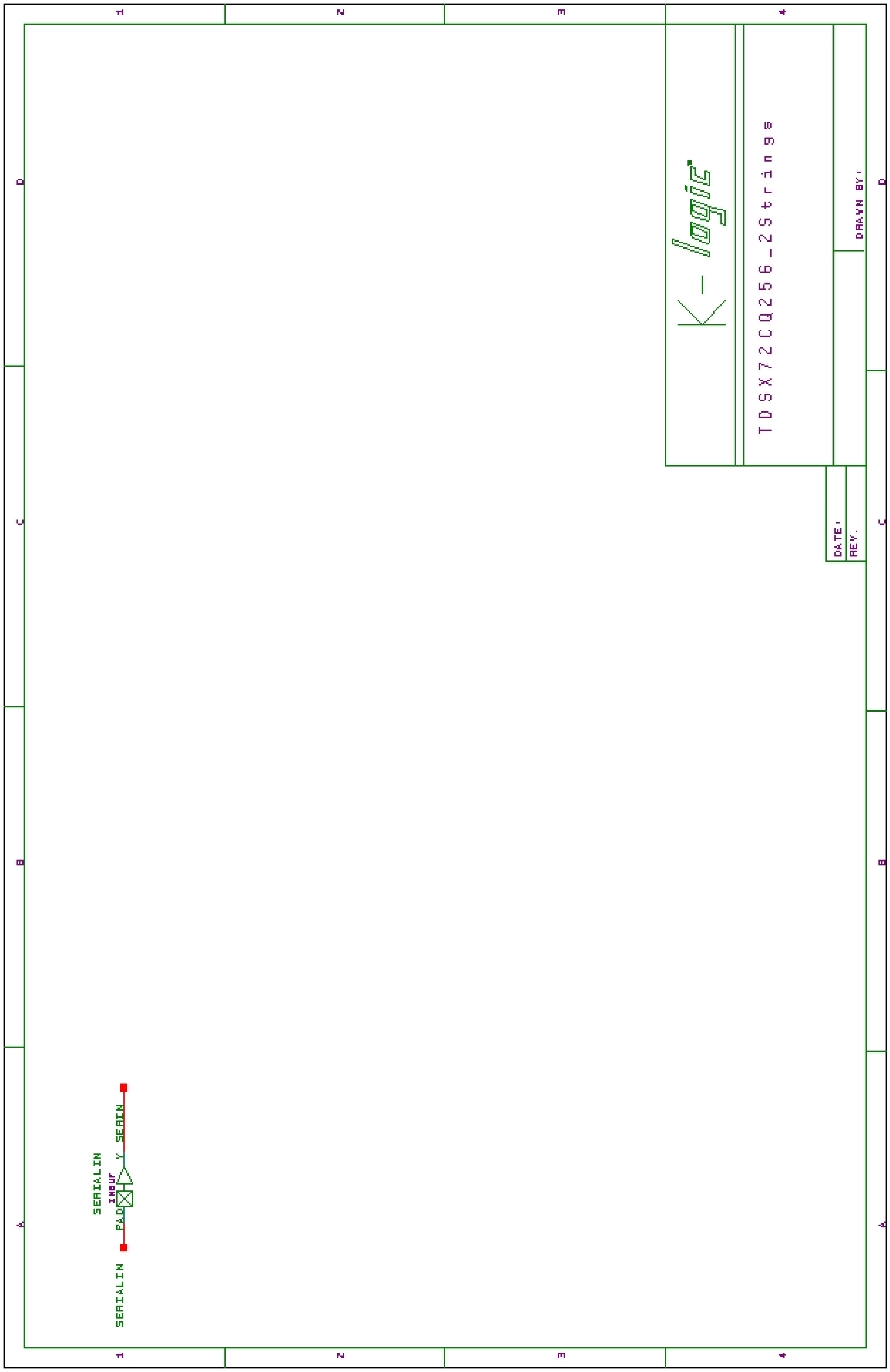
QA2H
QA0H
QA1H
CLKH
OUTBUF
PAD
INBUF
HCLKBUF
DAH
CLOCKH
RESETH
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

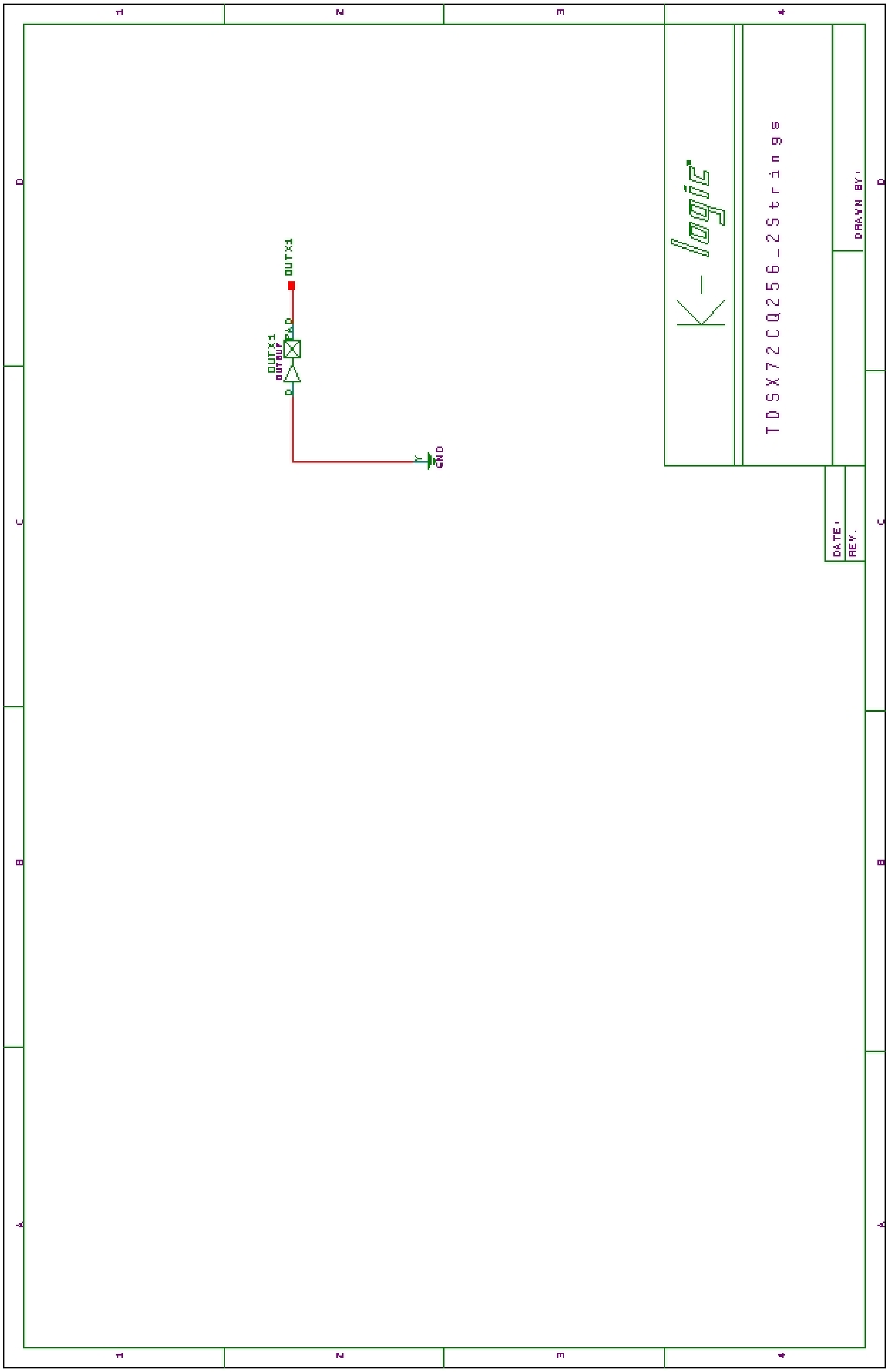


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
OUTBUF
PAD
INBUF
RESETCNTAH
ENCNTAH
CNTALDH



TAKE NOTE OF THIS
NOT USED FOR SX
IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
K-logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
SERIALIN
SERIALIN
IBUF
PAD
Y
SERIN


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
OUTX1
OUTBUF
PAD
GND