TOTAL IONIZING DOSE TEST REPORT

No. 03T-RT54SX32S-T25JS004
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad(Si)
2. I_{CC}	Passed 73 krad(Si), total I_{CC} averaged 85 mA after 100 krad(Si) and 2 weeks room temperature annealing
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad(Si)
4. Output Drives (V_{OL}/V_{OH})	Passed 100 krad(Si)
5. Propagation Delays	Passed 100 krad(Si)
6. Transition Time	Passed 100 krad(Si)

II. TOTAL IONIZING DOSE (TID) TESTING

A. Device Under Test (DUT) and Irradiation

Table 1 lists the DUT information and irradiation conditions.

Table 1. DUT information and irradiation conditions

Part Number	RT54SX32S
Package	CQFP256
Foundry	Matsushita Electronics Corporation
Technology	0.25 μm CMOS
DUT Design	TDSX32CQFP256_2Strings
Die Lot Number	T25JS004
Quantity Tested	5
Serial Number	13093, 13094, 13097, 13100, 13109
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad(Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	5.0 V/2.5 V

B. Test Method

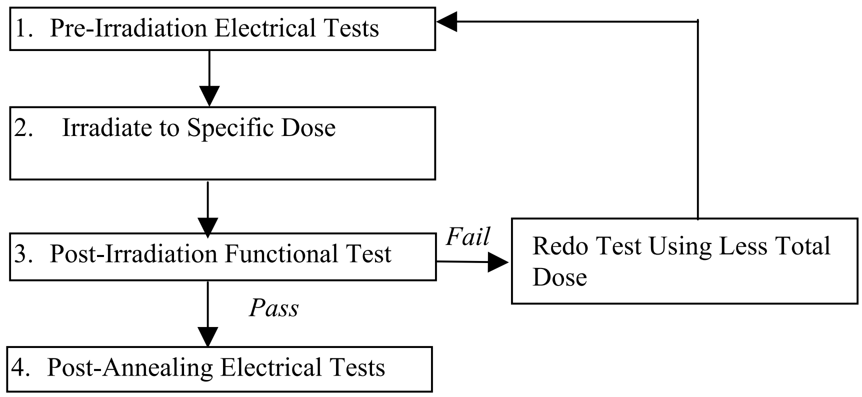


Fig 1 Parametric test flow chart

The parametric tests follow the military standard test method 1019.5. Fig 1 shows the testing flow. The time dependent effect (TDE) of this product was previously evaluated by comparing the results of a high dose rate (1 krad(Si)/min) against the results of a low dose rate (1 krad(Si)/hr). No adverse TDE was observed. Therefore the accelerated aging test (rebound test) is omitted in this report.

C. Electrical Parameter Measurements

A high utilization design (TDSX32CQ256_2Strings) to address total dose effects in typical space applications is used. The circuit schematics are shown in appendix A.

Table 2 lists the electrical parameters measured. The functionality is measured pre-irradiation, post-irradiation, and post-annealing on the output pin (O_AND3 or O_AND4) of the two combinatorial buffer-strings and on the output pins (O_OR4 and O_NAND4) of the shift register. The in-flux I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. During annealing, the I_{CC} of one DUT (S/N number 13097) is monitored independently. The other four DUT are grouped on a burn-in board and their total I_{CC} is monitored.

The input logic thresholds (V_{TIL}/V_{IH}) and output drives (V_{OL}/V_{OH}) are measured pre-irradiation and post-annealing on a combinatorial net, the input pin DA to the output pin QA0. The propagation delays are measured pre-irradiation and post-annealing on the buffer strings in three stages. Each stage has 60, 320, or 560 buffers. The delay is defined as from the input CLOCK to the output. The transient time is measured pre-irradiation and post-annealing on O_AND4. The buffer string is controlled by clocked flip-flops during the propagation delay and transient measurements.

Unused inputs are grounded with an 1 M ohm resistor during irradiation and an 1.2K ohm resistor during annealing.

Table 2. Logic design for parametric tests

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	TTL compatible input buffer (pin DA to QA0)
4. Output Drive (V_{OL}/V_{OH})	TTL compatible output buffer (pin QA0)
5. Propagation Delay	String of buffers (pin LOADIN to Y60, Y320, or O_AND4)
6. Transition Time	D flip-flop output (O_AND4)

III. TEST RESULTS

A. Functionality

Every DUT passed the gross functional test at pre-irradiation, post-irradiation, and post-annealing.

B. I_{CC}

Figs 2-5 show the in-flux I_{CC} of DUT 13093, 13094, 13097 and 13109. DUT 13100 did not have in-flux I_{CC} plot because of an operation error. For the same accumulative total dose, I_{CC} at the present dose rate of 1 krad(Si)/min is significant higher than the previous results tested at lower dose rate of 1 krad(Si)/hr (see for example report No. 02T-RT54SX32S-T25JS001). At 100 krad(Si) total dose, I_{CC} (I_{CCA} and I_{CCI}) for high dose rate is averaging 188 mA, while I_{CC} for low dose rate is 70 mA.

The room temperature biased annealing was performed on every DUT. After 2 weeks, the average I_{CC} dropped to 85 mA. However, the I_{CC} spec is 25 mA. The radiation tolerance for this spec has to be extracted from the annealing characteristic. Fig 6 shows the annealing characteristic of DUT 13097. The current is normalized with the peak current at 100 krad(Si). The log-log plot shows a straight line after the short initial stage. Extending the curve to 10 years mission time, the annealing factor is obtained as 0.32 for I_{CCA} and 0.29 for I_{CCI}. Assume that annealing factors are dependent on the product and bias voltage but relatively independent of the total dose in the range of interest, the critical total dose ($\gamma_{critical}$) at the 10-year mission dose rate to induce I_{CC} to 25 mA can be obtained by the equation,

$$I_{CCA}(\gamma_{critical}) \times 0.32 + I_{CCI}(\gamma_{critical}) \times 0.29 = 25mA$$

Where $I_{CCA}(\gamma)$ and $I_{CCI}(\gamma)$ are displayed in Fig 4. The tolerance is thus obtained as approximately 73 krad(Si).

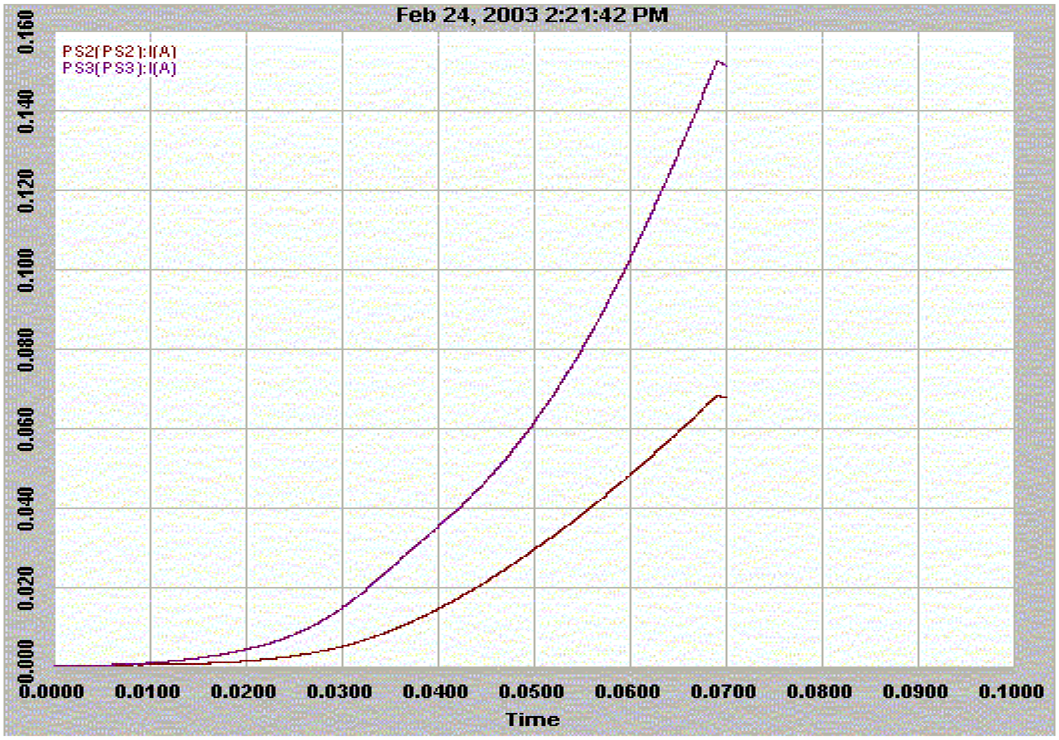


Fig 2 In-flux I_{CC} of DUT 13093, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}. The current unit is amps and the time unit is days, 0.01 day is equivalent to 14.4 krad(Si). I_{CC} reaches the peak at 100 krad(Si), irradiation stops after 100 krad(Si) and I_{CC} drops due to annealing effect.

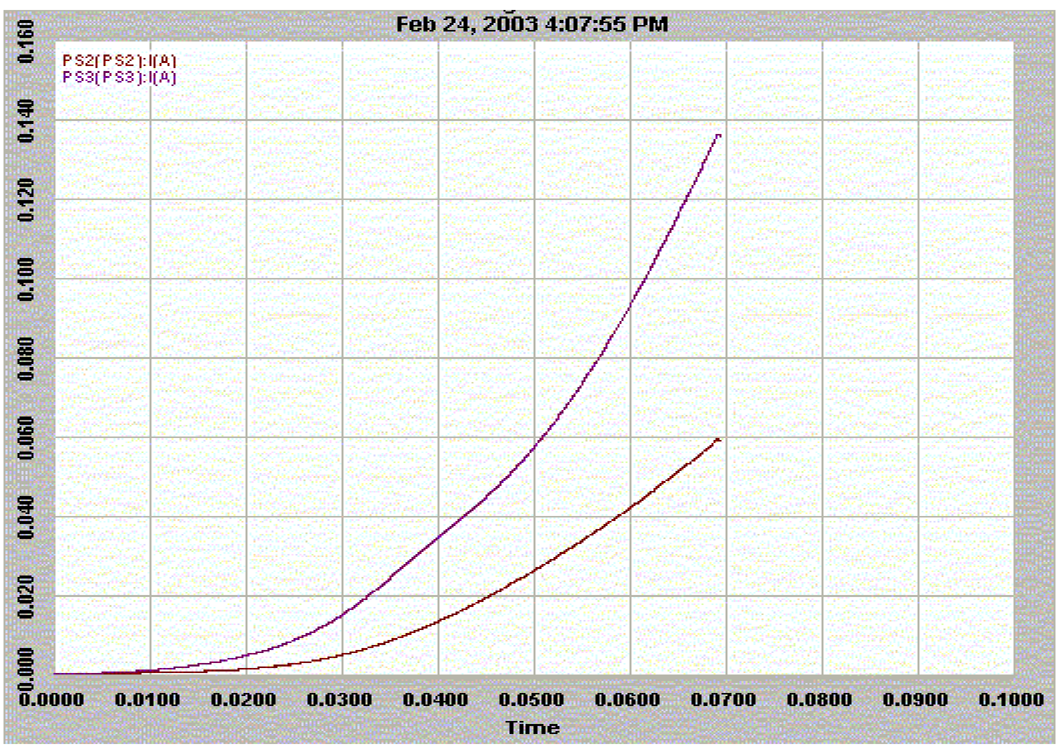


Fig 3 In-flux I_{CC} of DUT 13094, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}. The current unit is amps and the time unit is days, 0.01 day is equivalent to 14.4 krad(Si). I_{CC} reaches the peak at 100 krad(Si), irradiation stops after 100 krad(Si) and I_{CC} drops due to annealing effect.

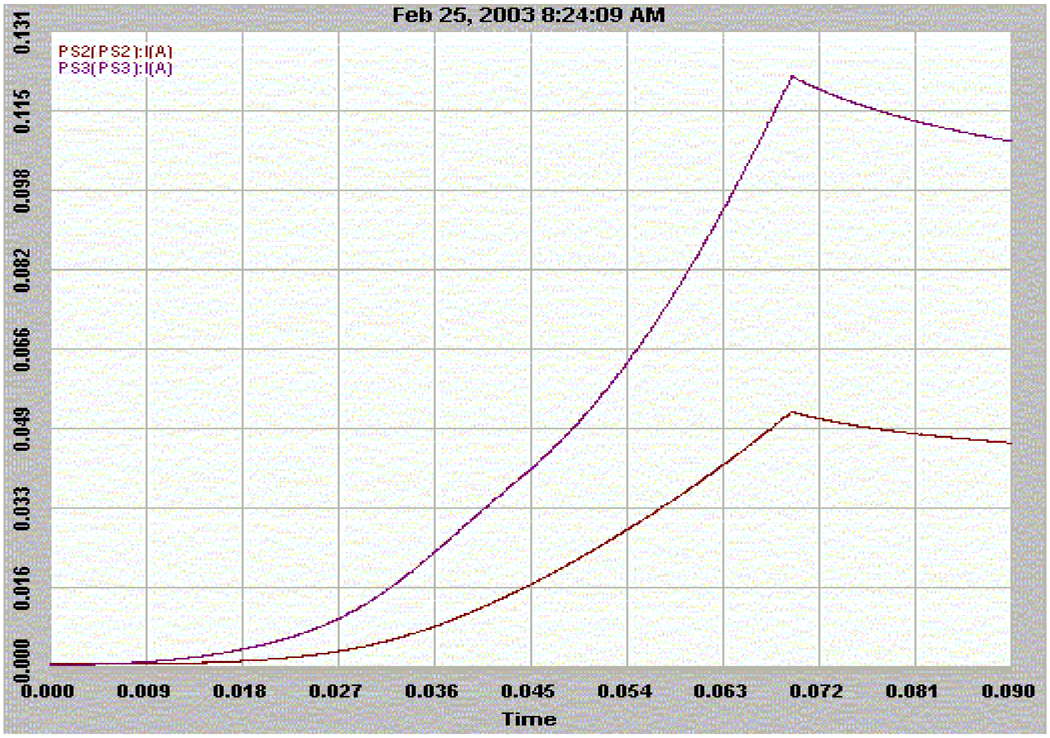


Fig 4 In-flux I_{CC} of DUT 13097, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}. The current unit is amps and the time unit is days, 0.01 day is equivalent to 14.4 krad(Si). I_{CC} reaches the peak at 100 krad(Si), irradiation stops after 100 krad(Si) and I_{CC} drops due to annealing effect.

Fig 5 In-flux I_{CC} of DUT 13109, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}. The current unit is amps and the time unit is days, 0.01 day is equivalent to 14.4 krad(Si). I_{CC} reaches the peak at 100 krad(Si), irradiation stops after 100 krad(Si) and I_{CC} drops due to annealing effect.

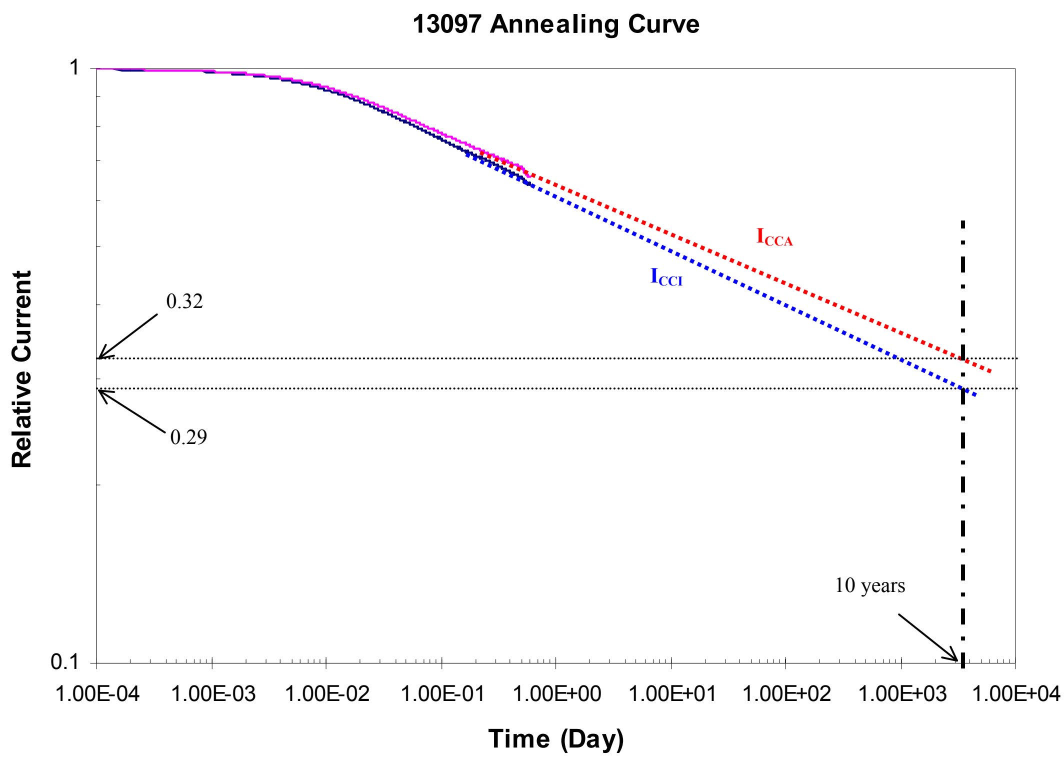


Fig 6 I_{CC} annealing curve, the dotted lines are extrapolations for the 10 years flight mission.

C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4 lists the pre-irradiation and post-annealing input logic threshold for each DUT. These parameters are well within the spec limit after 100 krad(Si) irradiation.

Table 4 Pre-irradiation and post-annealing input logic threshold in voltages

DUT	Pre-Irradiation		Post-Annealing	
	V_{IL}	V_{IH}	V_{IL}	V_{IH}
13093	1.43	1.53	1.26	1.52
13094	1.42	1.56	1.28	1.51
13097	1.44	1.57	1.26	1.52
13100	1.39	1.53	1.26	1.50
13109	1.43	1.51	1.27	1.50

D. Output Characteristics (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in table 5 and 6. 100 krad(Si) radiation has a negligible effect on these parameters.

Table 5 Pre-irradiation and post-annealing V_{OL} (in voltages) at various sinking current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
13093	0.01	0.01	0.1	0.1	0.17	0.17	0.43	0.43	0.89	0.88
13094	0.01	0.01	0.1	0.1	0.17	0.17	0.43	0.44	0.90	0.90
13097	0.01	0.01	0.1	0.1	0.17	0.17	0.43	0.43	0.90	0.90
13100	0.01	0.01	0.1	0.1	0.17	0.17	0.43	0.43	0.88	0.88
13109	0.01	0.01	0.1	0.1	0.17	0.17	0.44	0.44	0.90	0.90

Table 6 Pre-irradiation and post-annealing V_{OH} (in voltages) at various sourcing current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
13093	4.98	4.98	4.87	4.86	4.66	4.66	4.11	4.10	2.99	2.97
13094	4.98	4.98	4.86	4.86	4.65	4.65	4.10	4.08	2.97	2.92
13097	4.98	4.98	4.86	4.86	4.65	4.64	4.10	4.07	2.95	2.89
13100	4.99	4.98	4.86	4.86	4.65	4.64	4.10	4.08	2.99	2.93
13109	4.98	4.98	4.86	4.86	4.65	4.65	4.10	4.08	2.96	2.93

E. Propagation Delays

Table 7 lists the pre-irradiation and post-annealing propagation delays and radiation-induced degradations. The larger than usual degradation is due to the high dose rate used in this test. However, the degradation is less for shorter buffer strings. In practical designs with buffer strings less than 60 stages, the propagation delay should be well below 10% in low dose rate environment.

Table 7 Propagation delays in nanoseconds

DUT	60 buffers stage			320 buffers stage			560 buffers stage		
	Pre-Irra	Post-Ann	Degrad	Pre-Irra	Post-Ann	Degrad	Pre-Irra	Post-Ann	Degrad
13093	53.79	57.3	6.53%	244.65	262.35	7.23%	415.86	444.6	6.91%
13094	54.5	58.875	8.03%	248.03	269.24	8.55%	420.77	459.07	9.10%
13097	54.785	60.44	10.32%	250.29	277.961	11.06%	426.87	501.025	17.37%
13100	53.585	56.875	6.14%	244.3	260.43	6.60%	415.68	452.27	8.80%
13109	54.535	60.12	10.24%	249.06	273.265	9.72%	424.49	471.46	11.07%

F. Transition Time

The pre-irradiation and post-annealing rising, and falling edges are plotted in Figs 7-16. The voltage scale in these plots is 2 V/div, and the time scale is 2 ns/div. The radiation-induced degradation is not very obvious in every case. The transition time is within few nanoseconds in every case.

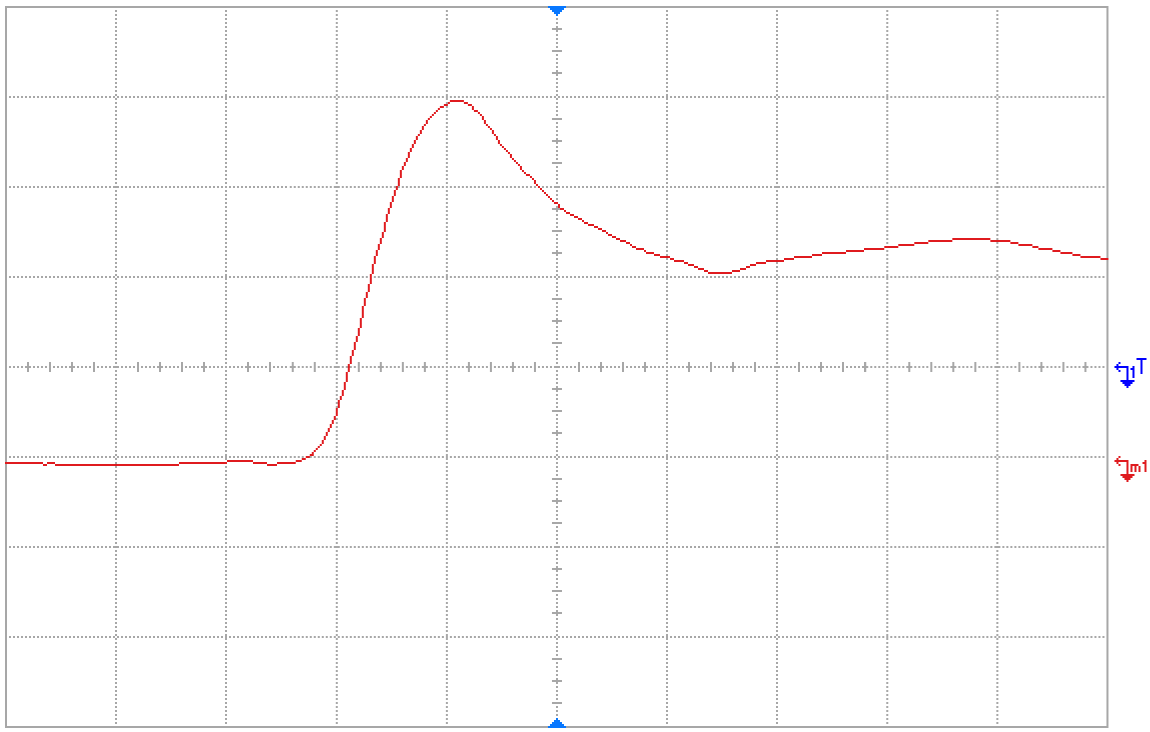


Fig 7(a) Pre-irradiation rising edge of DUT 13093

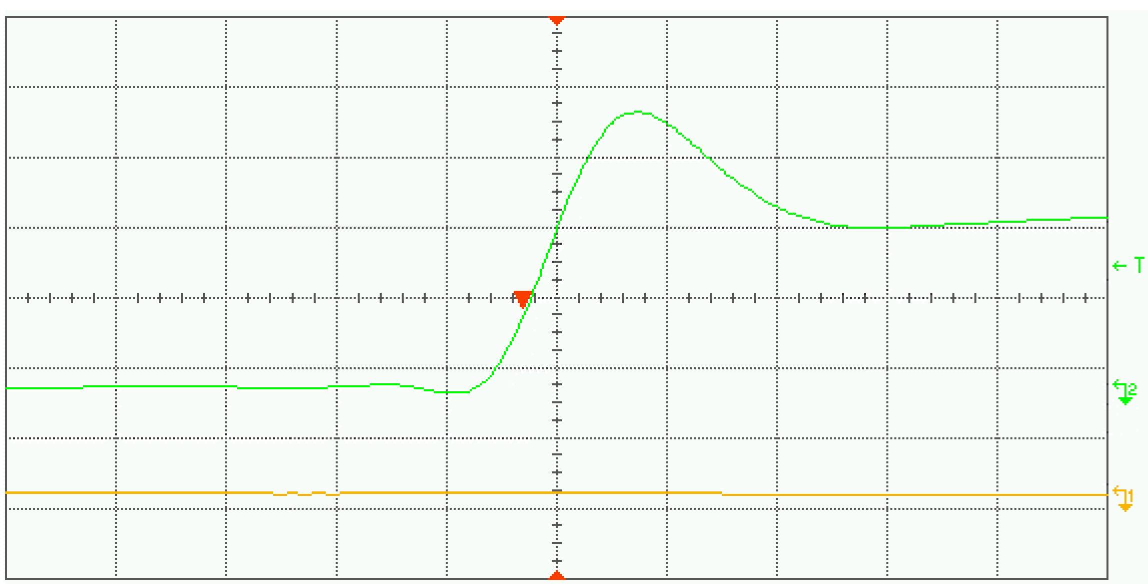


Fig 7(b) Post-annealing rising edge of DUT 13093

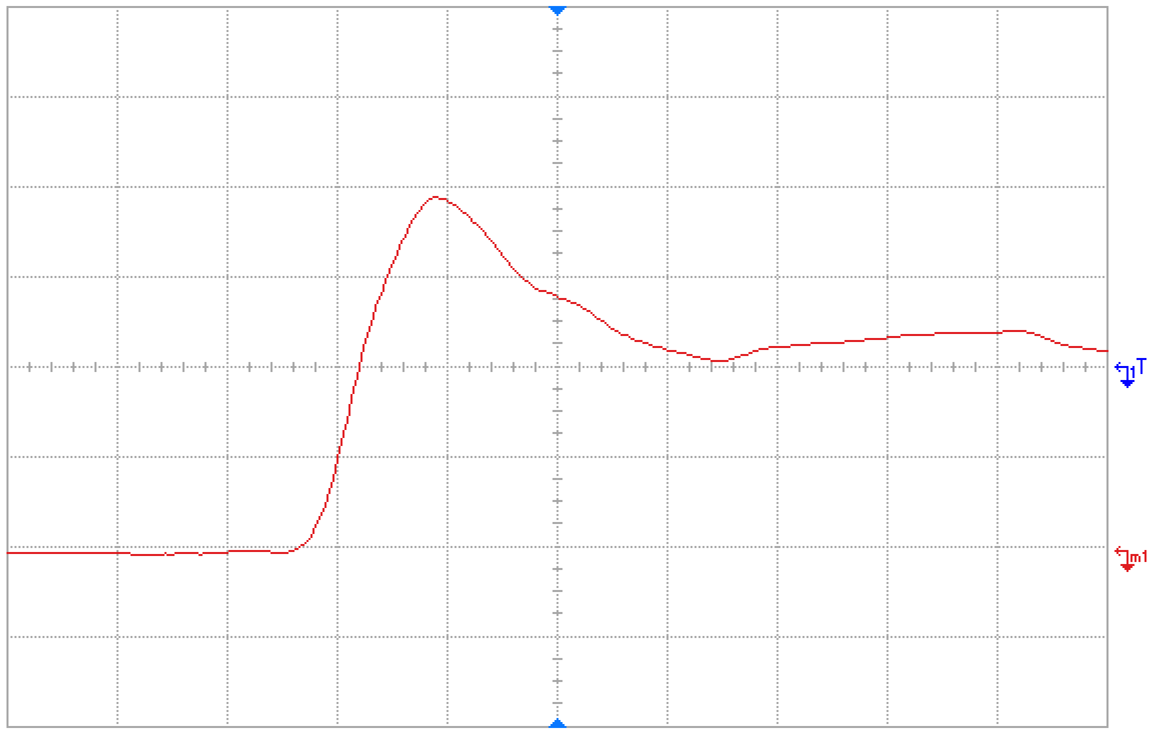


Fig 8(a) Pre-irradiation rising edge of DUT 13094

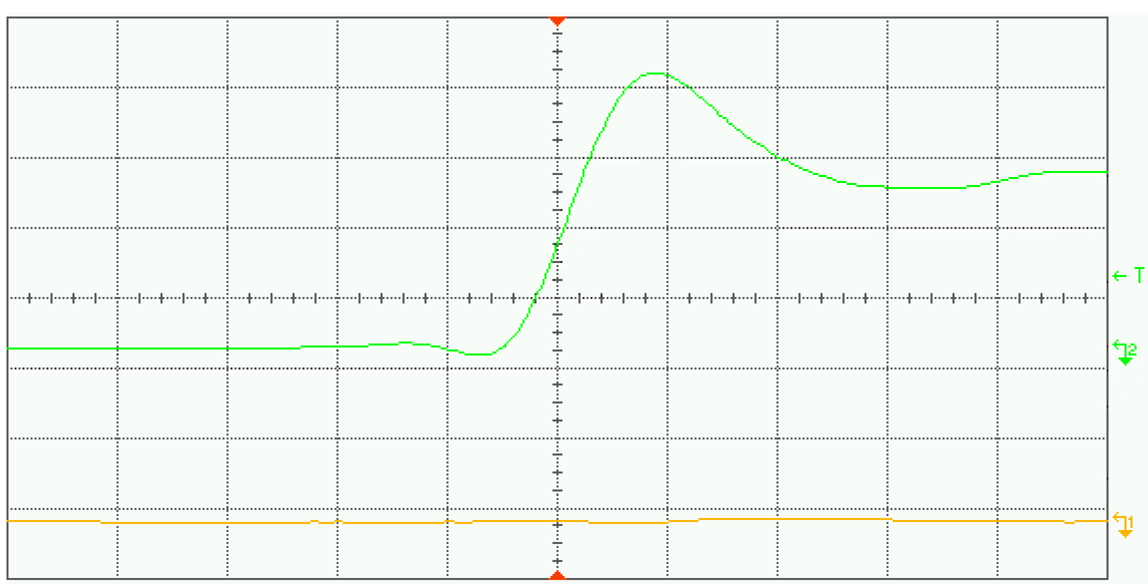


Fig 8(b) Post-annealing rising edge of DUT 13094

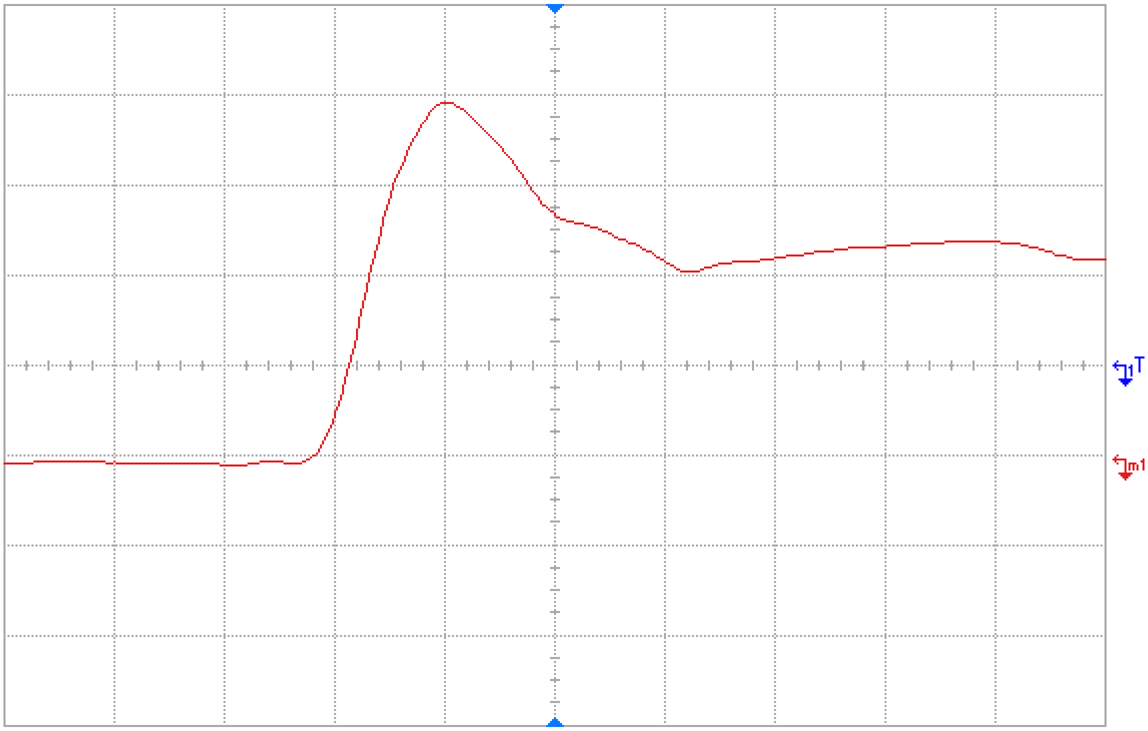


Fig 9(a) Pre-irradiation rising edge of DUT 13097

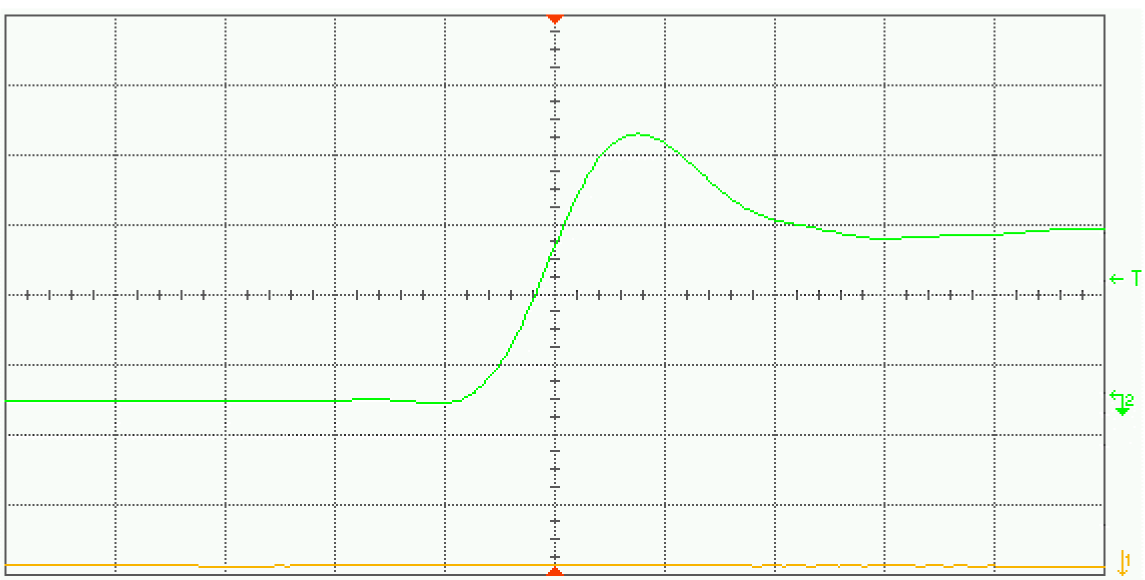


Fig 9(b) Post-annealing rising edge of DUT 13097

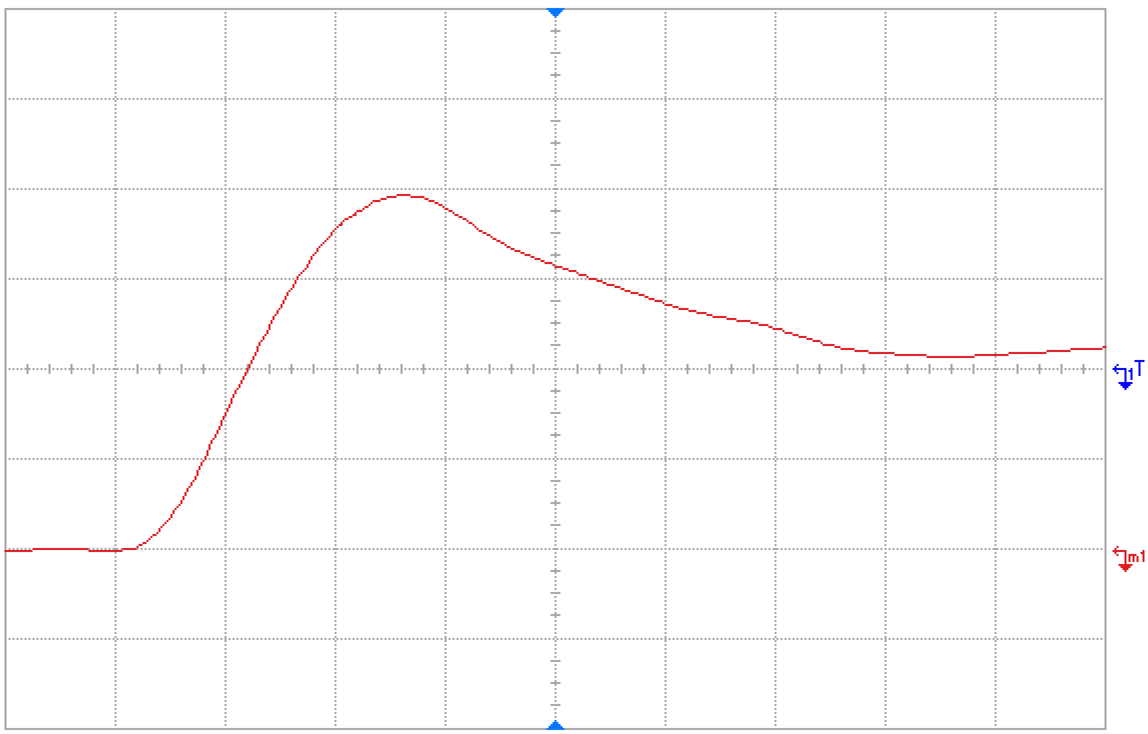


Fig 10(a) Pre-irradiation rising edge of DUT 13100, notice that the time scale is 1 ns/div, which is different from 2 ns/div used in Fig 10(b).

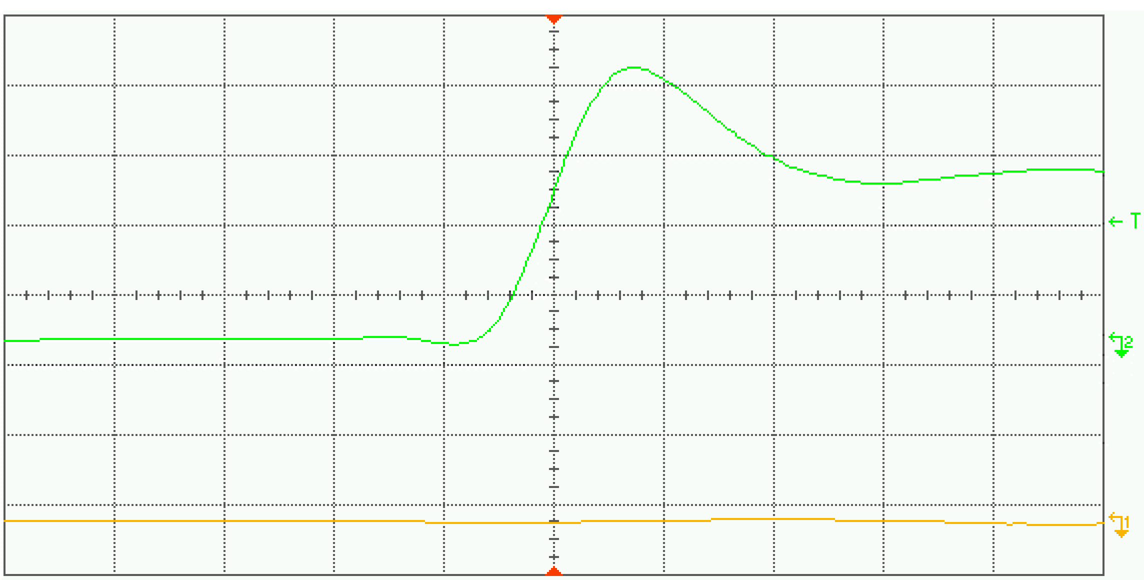


Fig 10(b) Post-annealing rising edge of DUT 13100

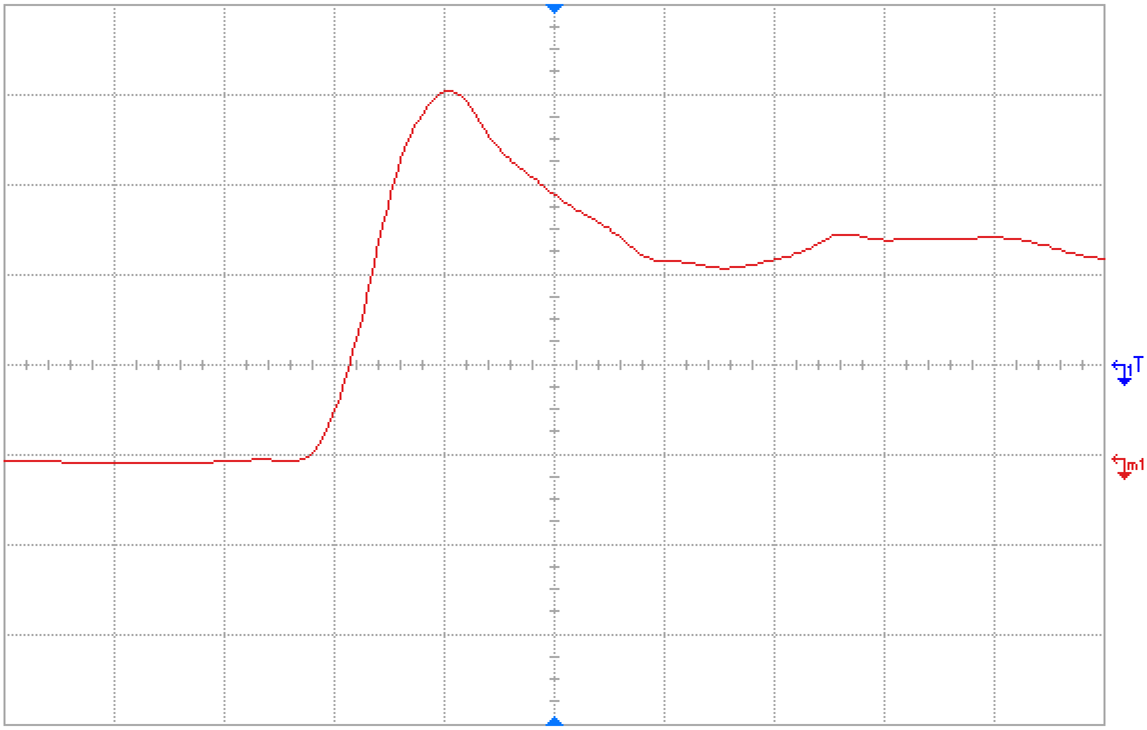


Fig 11(a) Pre-irradiation rising edge of DUT 13109

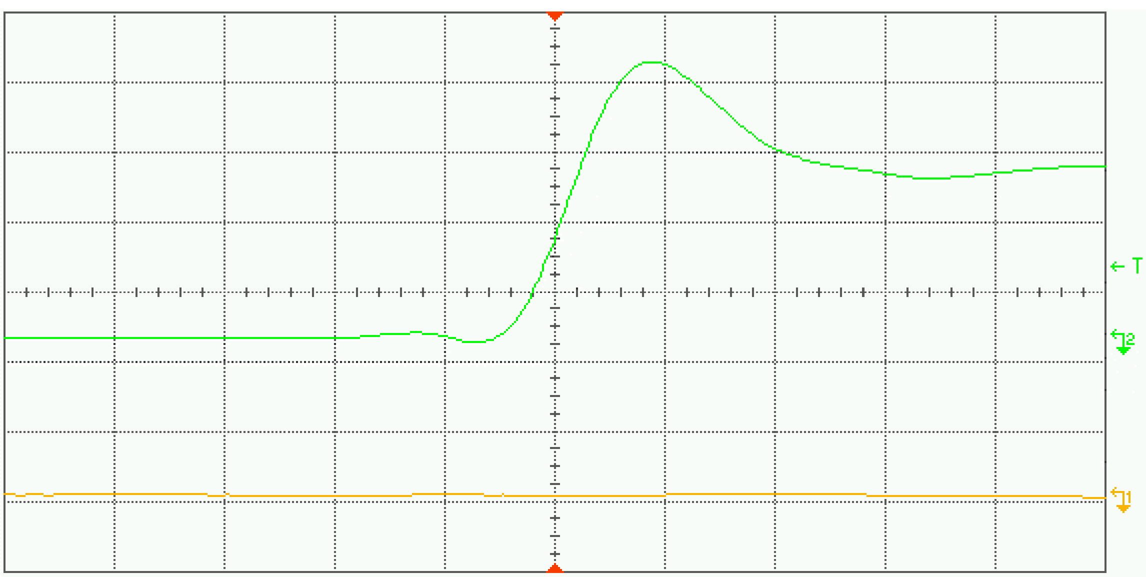


Fig 11(b) Post-annealing rising edge of DUT 13109

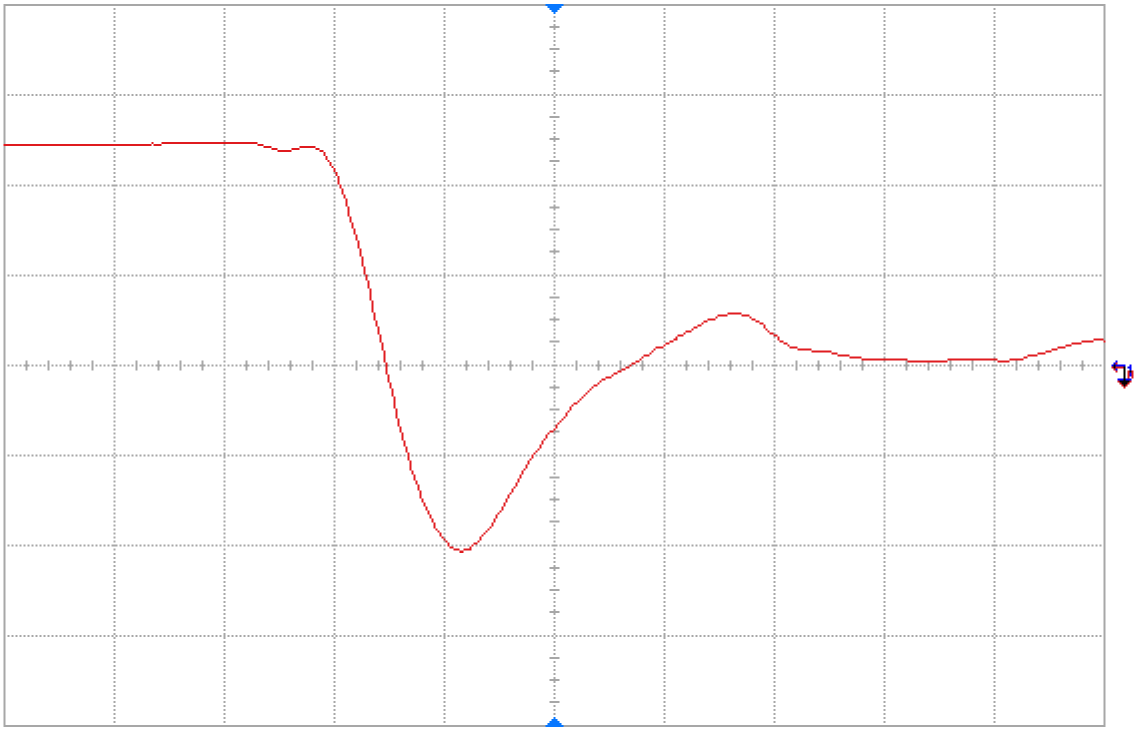


Fig 12(a) Pre-irradiation falling edge of DUT 13093

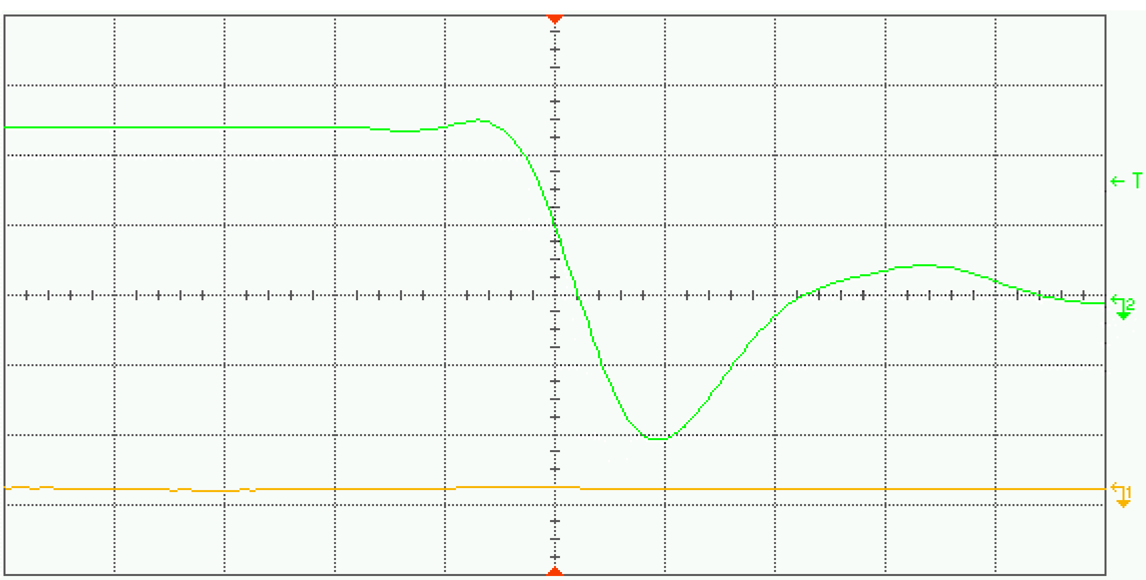


Fig 12(b) Post-annealing falling edge of DUT 13093

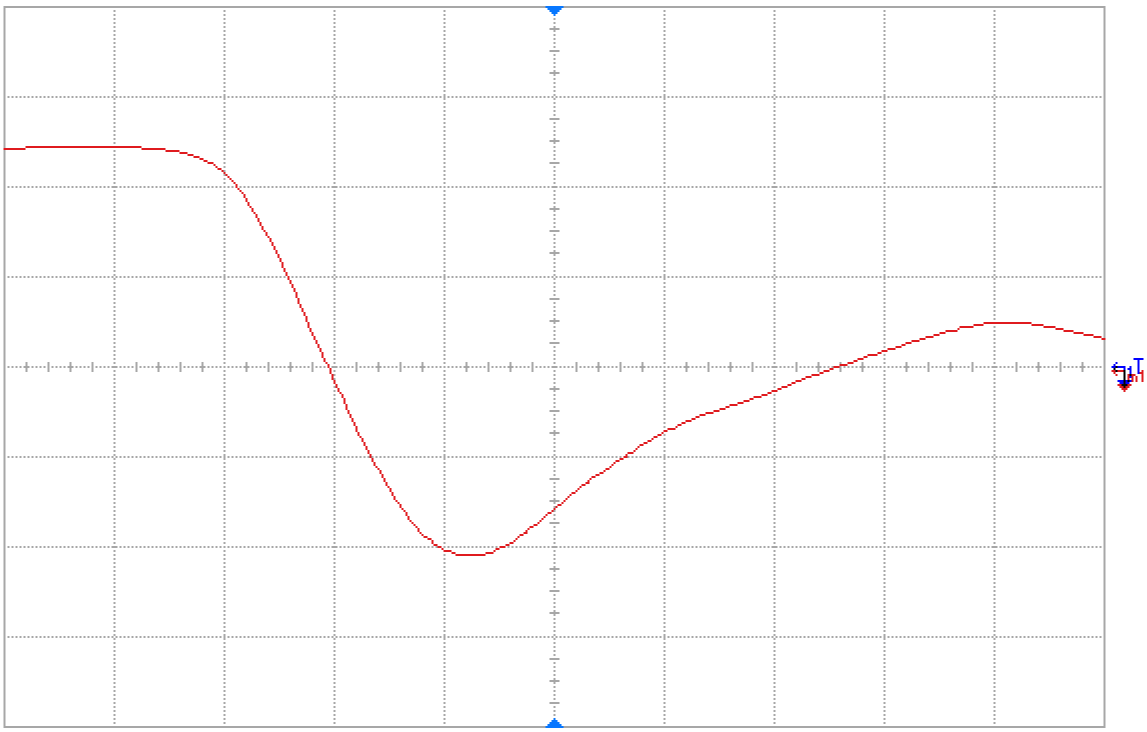


Fig 13(a) Pre-irradiation falling edge of DUT 13094, notice that the time scale is 1 ns/div, which is different from 2 ns/div used in Fig 13(b).

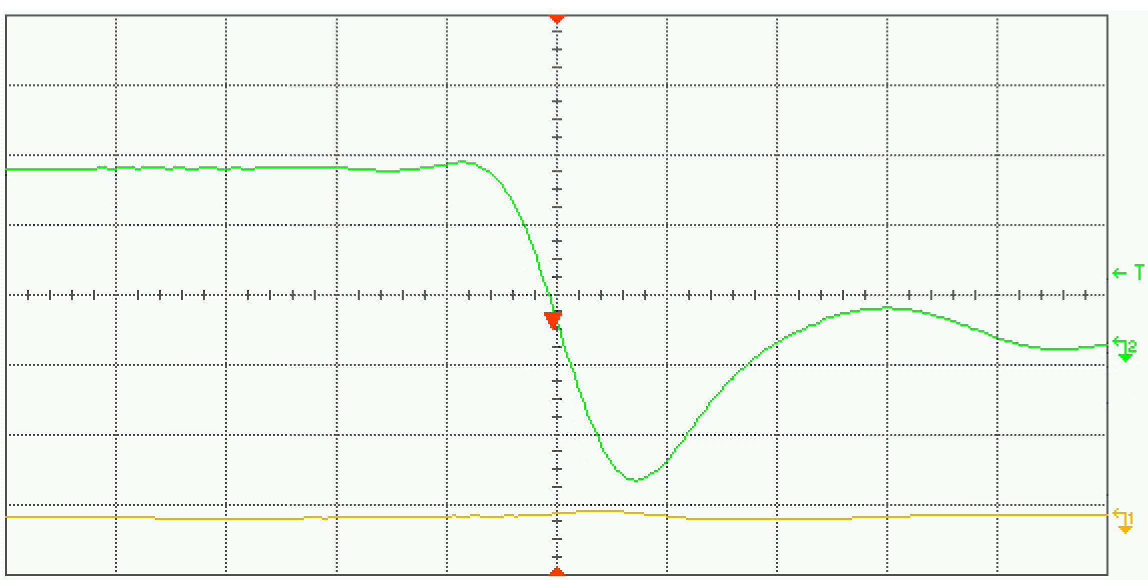


Fig 13(b) Post-annealing falling edge of DUT 13094

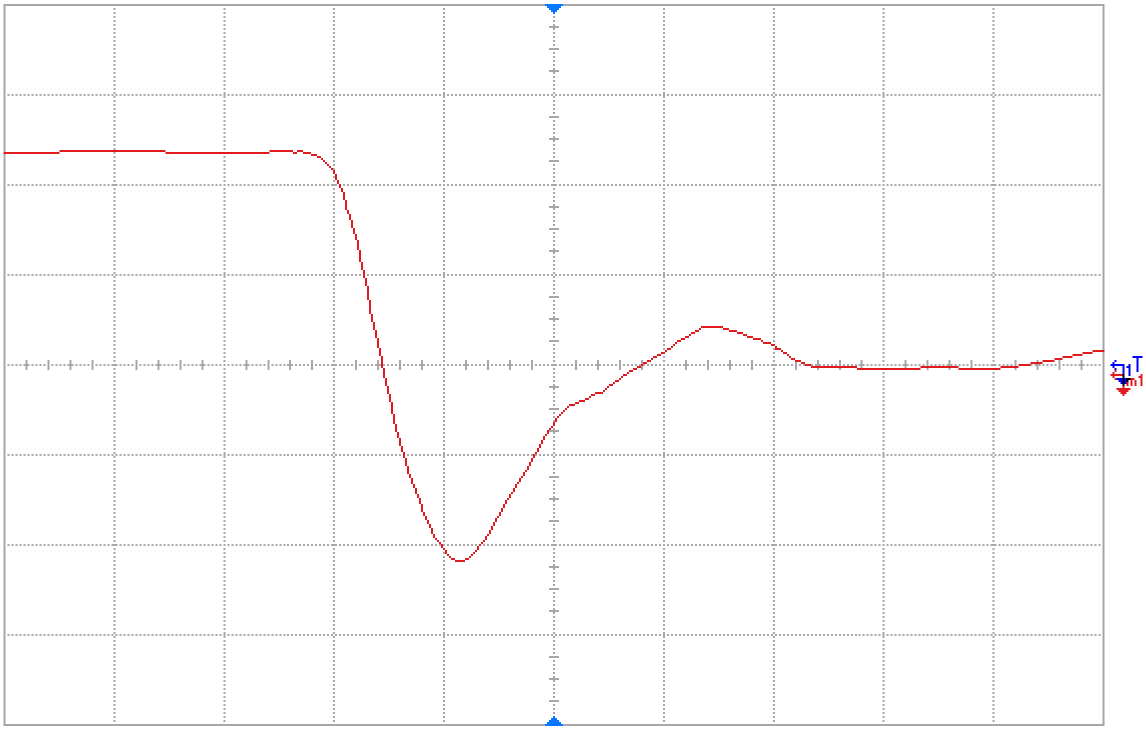


Fig 14(a) Pre-irradiation falling edge of DUT 13097

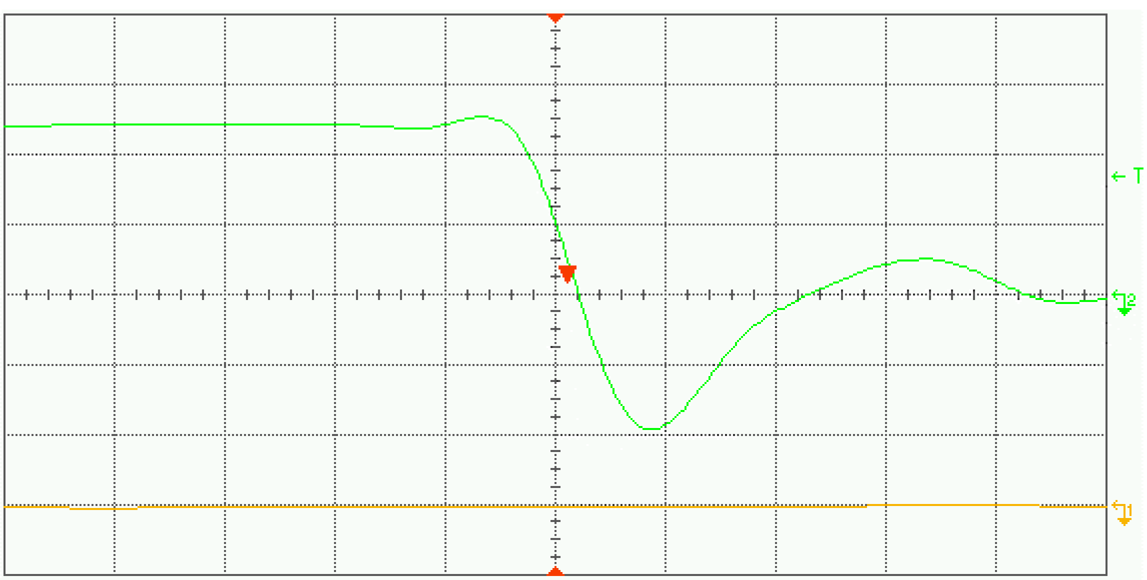


Fig 14(b) Post-annealing falling edge of DUT 13097

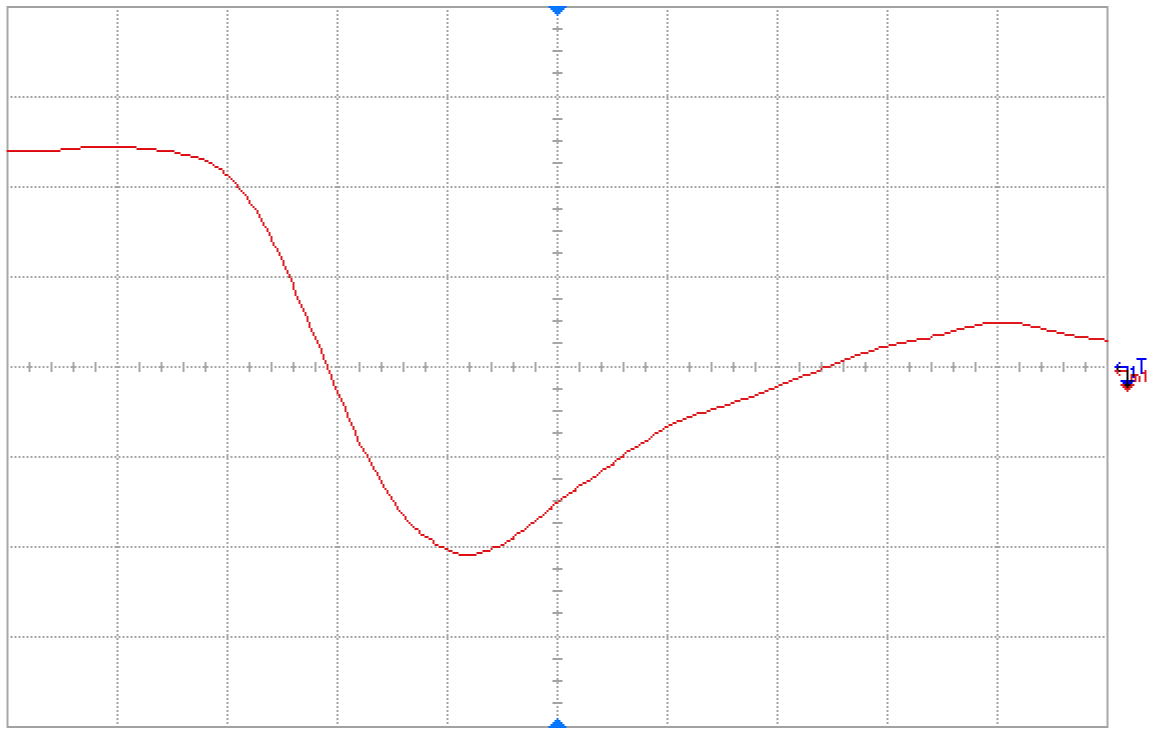


Fig 15(a) Pre-irradiation falling edge of DUT 13100, notice that the time scale is 1 ns/div, which is different from 2 ns/div used in Fig 15(b).

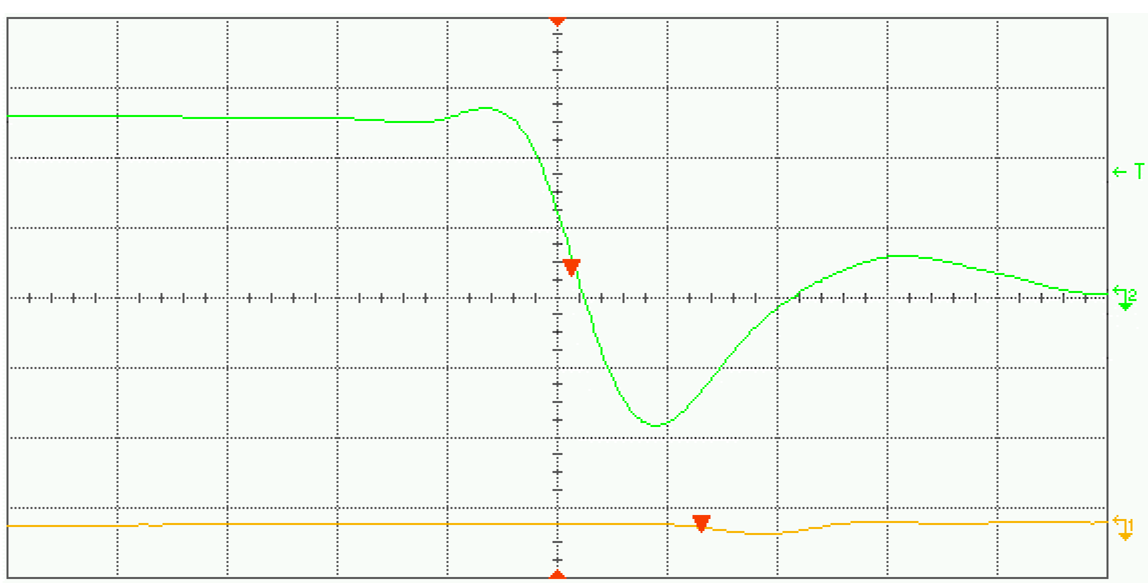


Fig 15(b) Post-annealing falling edge of DUT 13100

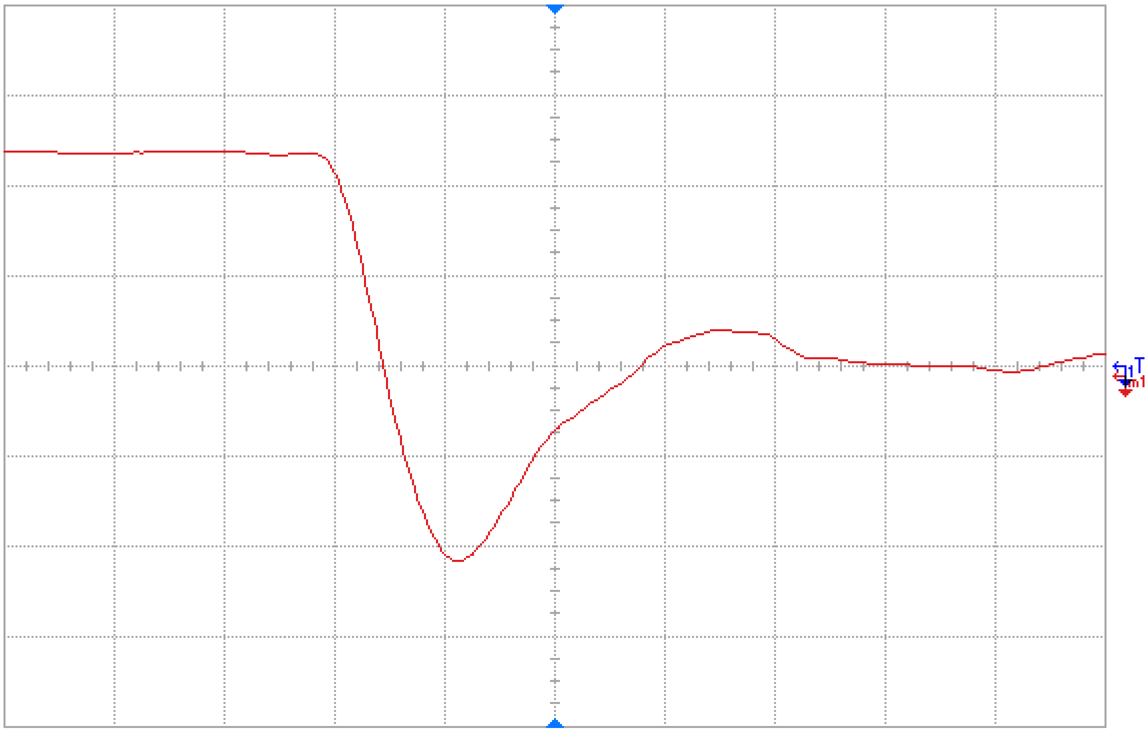


Fig 16(a) Pre-irradiation falling edge of DUT 13109

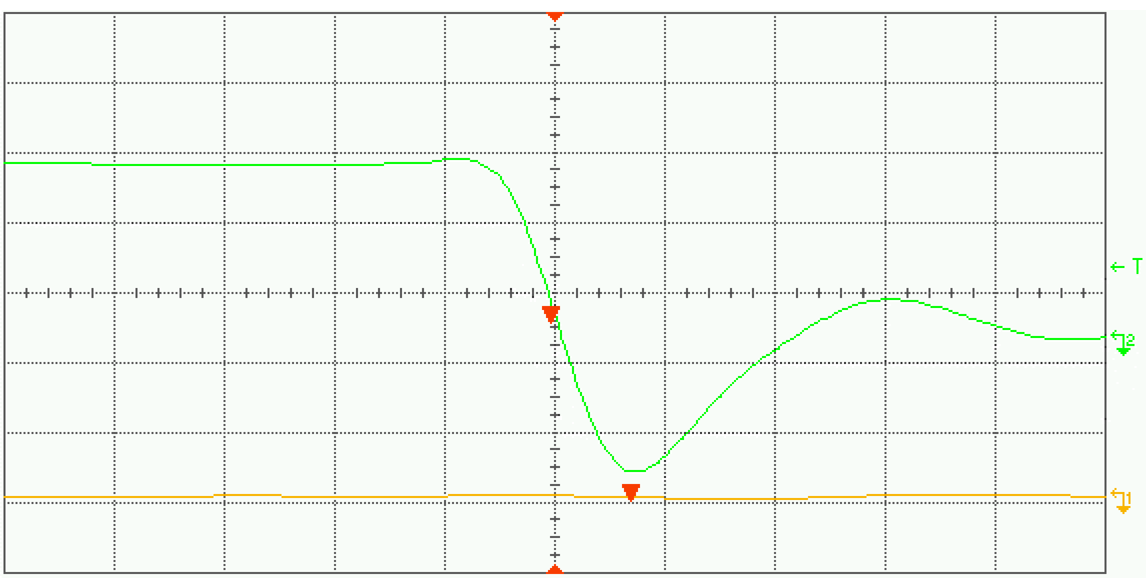
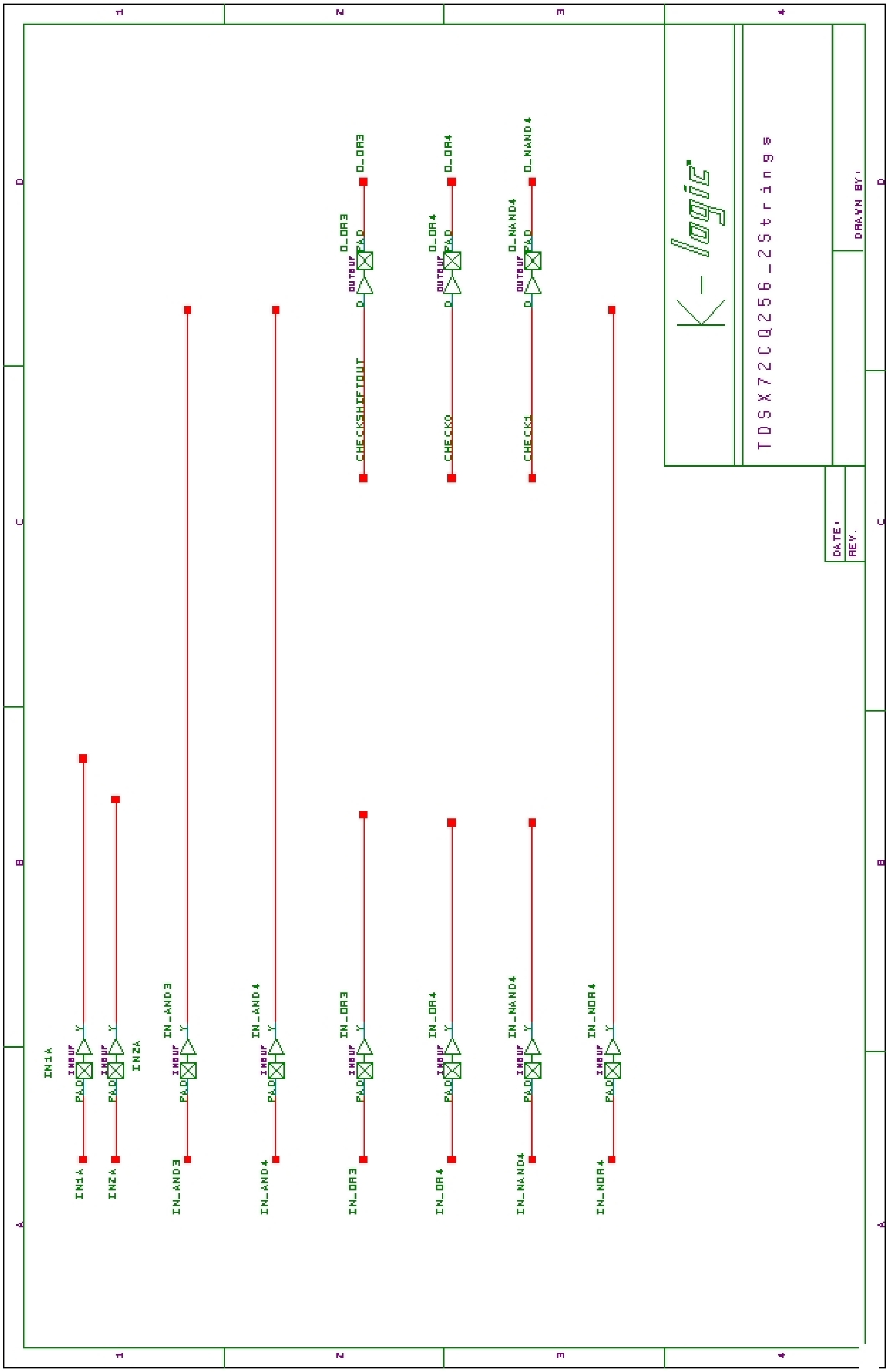
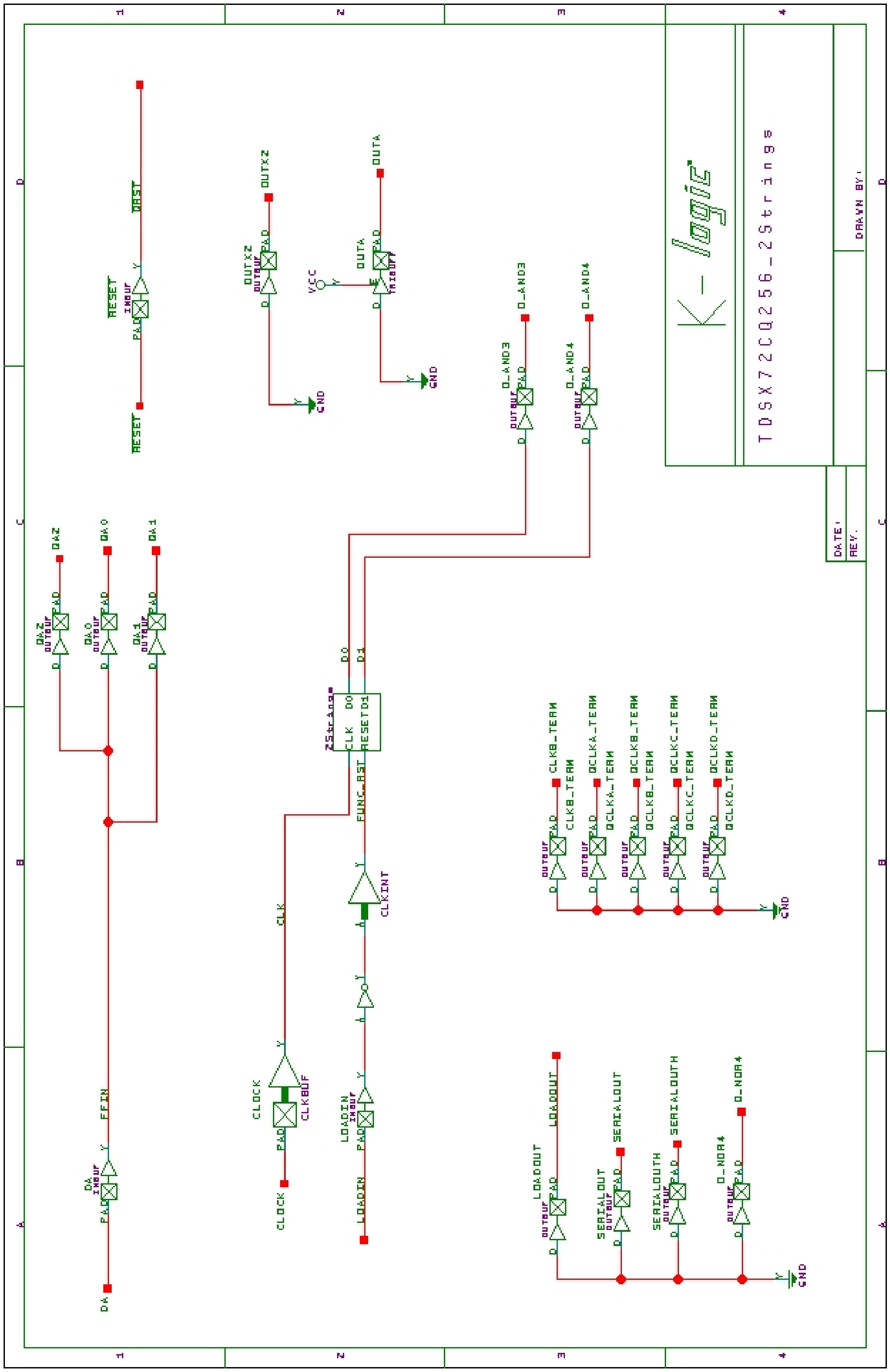


Fig 16(b) Post-annealing falling edge of DUT 13109

APPENDIX A DUT DESIGN SCHEMATICS




TDSX72CQ256_2Strings
DRAWN BY:
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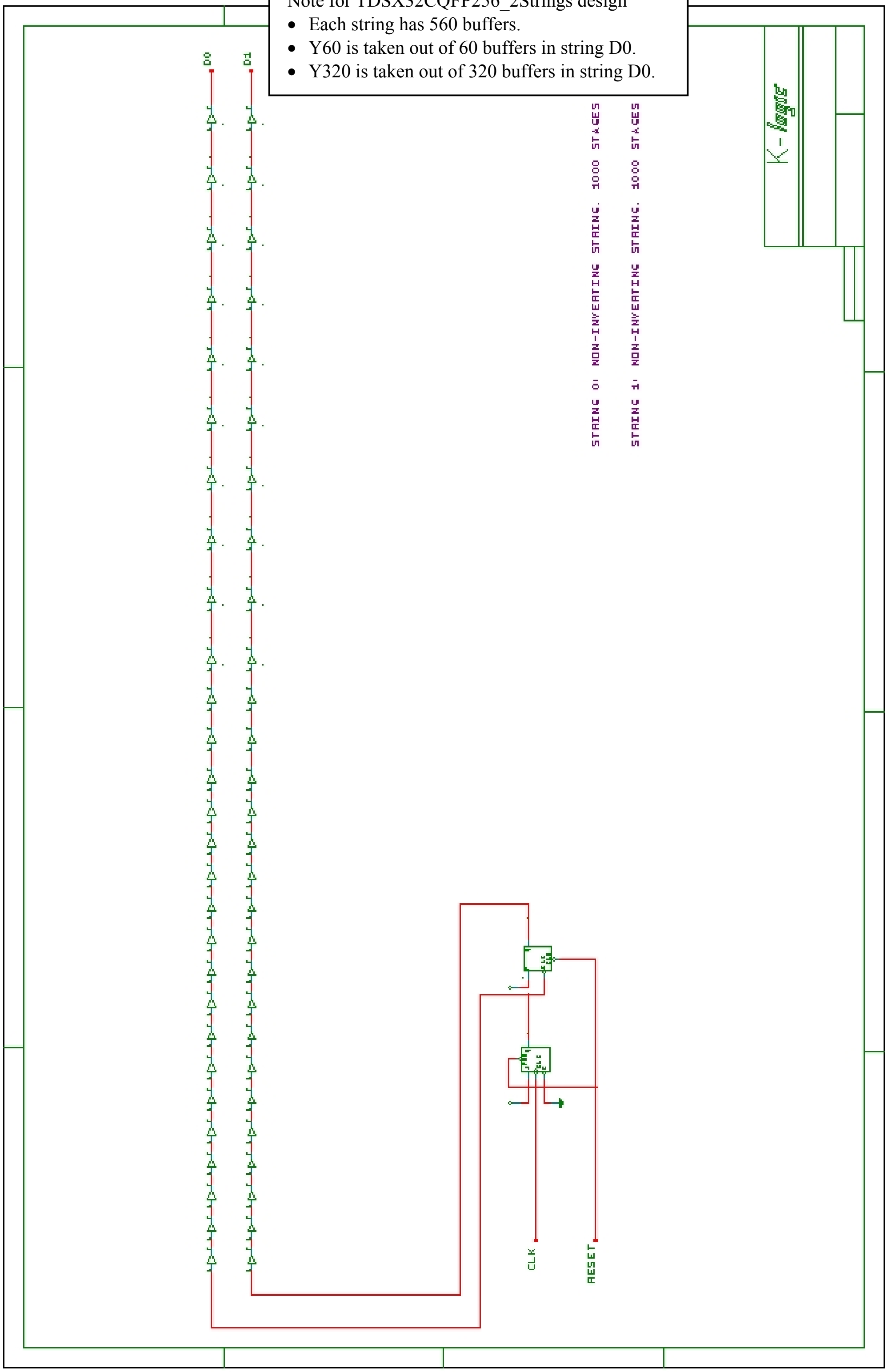
RESET
QRST
OUTX2
OUTA
VCC
GND
D_AND3
D_AND4
QA2
QA0
QA1
2Strings
CLK
RESET
D0
D1
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
INBUF
OUTBUF
TRIBUF
PAD
FFIN
DA
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4
CLKB_TERM
QCLKA_TERM
QCLKB_TERM
QCLKC_TERM
QCLKD_TERM

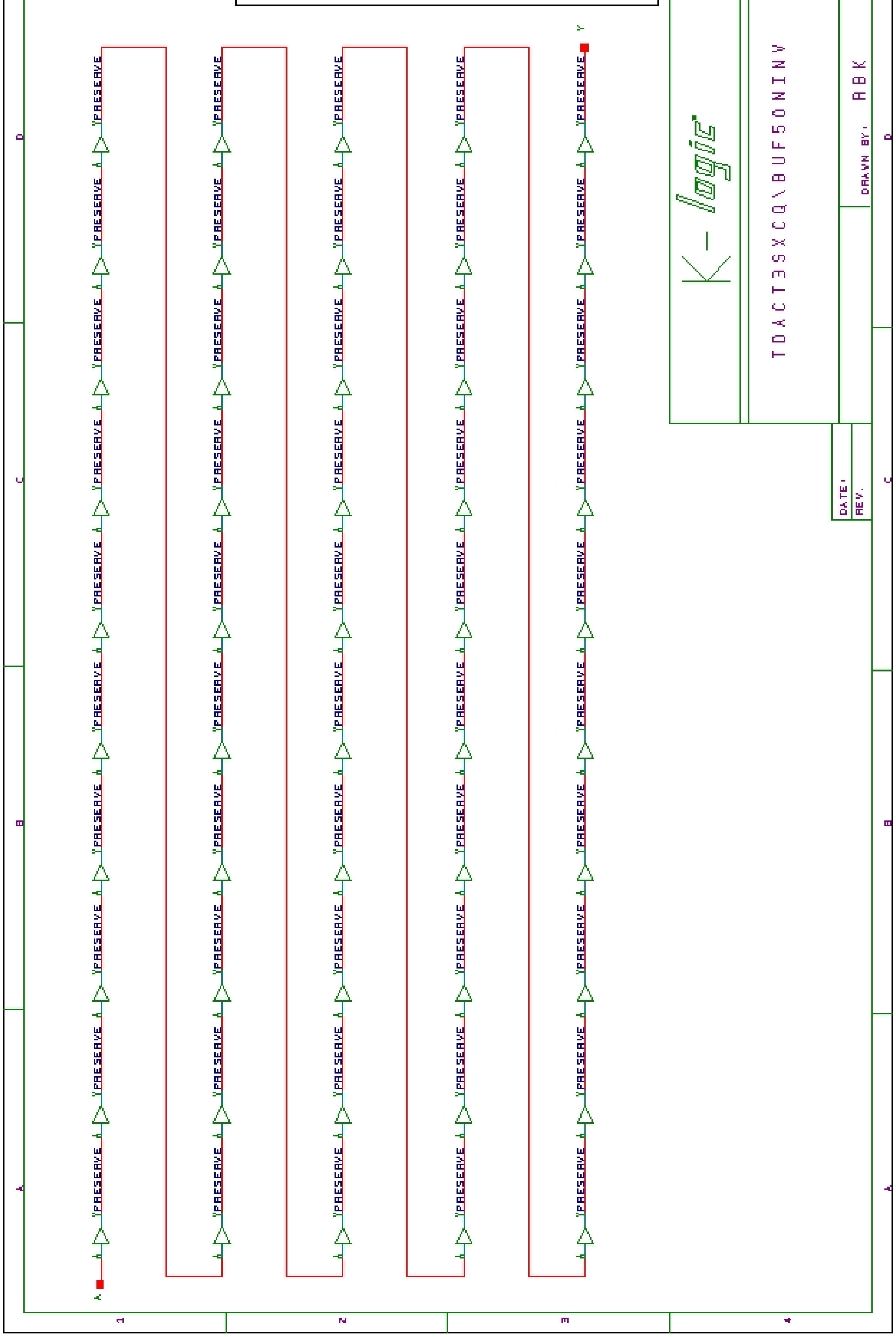
Note for TDSX32CQFP256_2Strings design

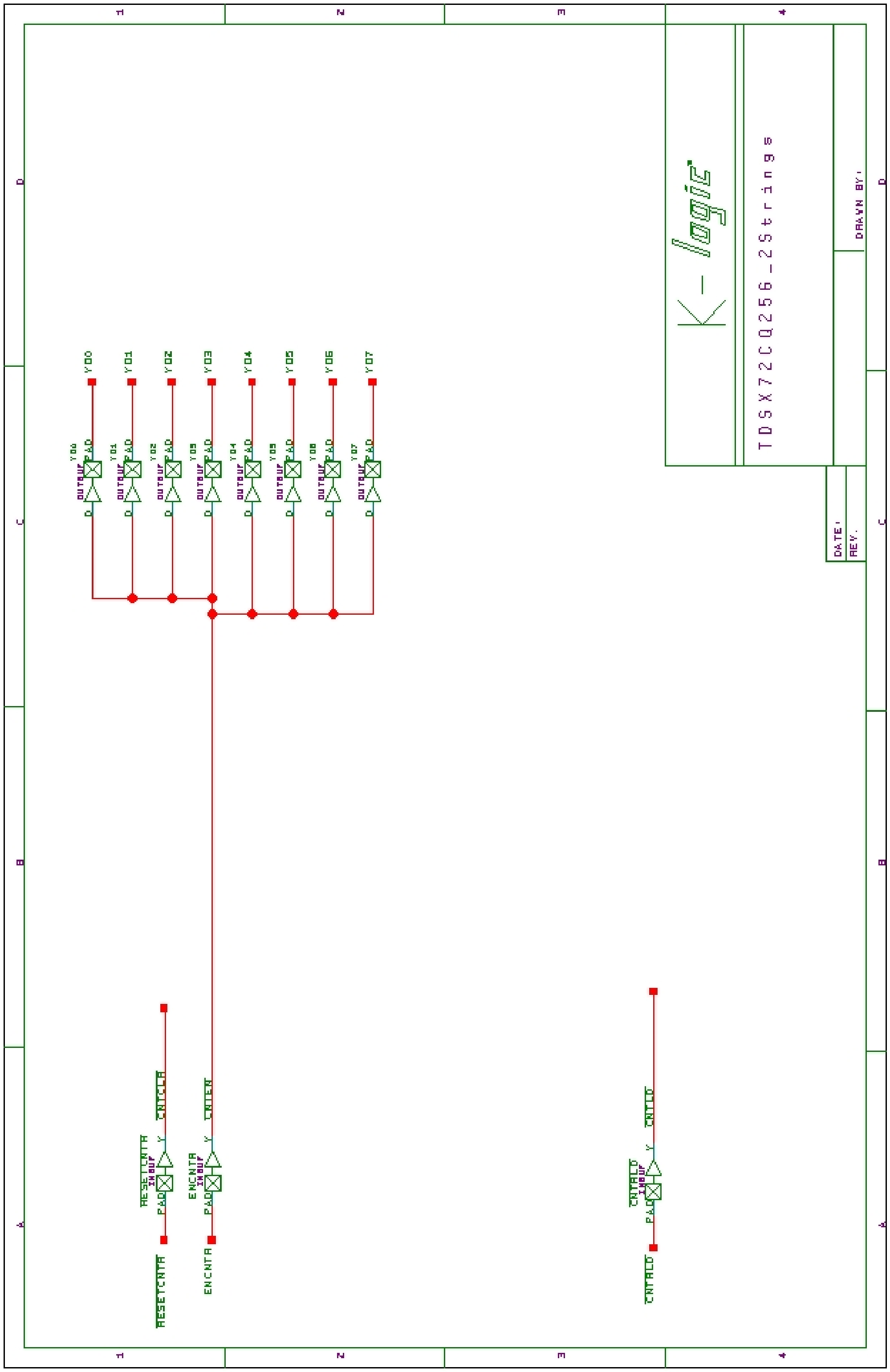
- Each string has 560 buffers.
- Y60 is taken out of 60 buffers in string D0.
- Y320 is taken out of 320 buffers in string D0.



Note for TDSX32CQFP256_2Strings design

- There are only 20 buffers in this page.





K-logic
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Y02
Y03
Y04
Y05
Y06
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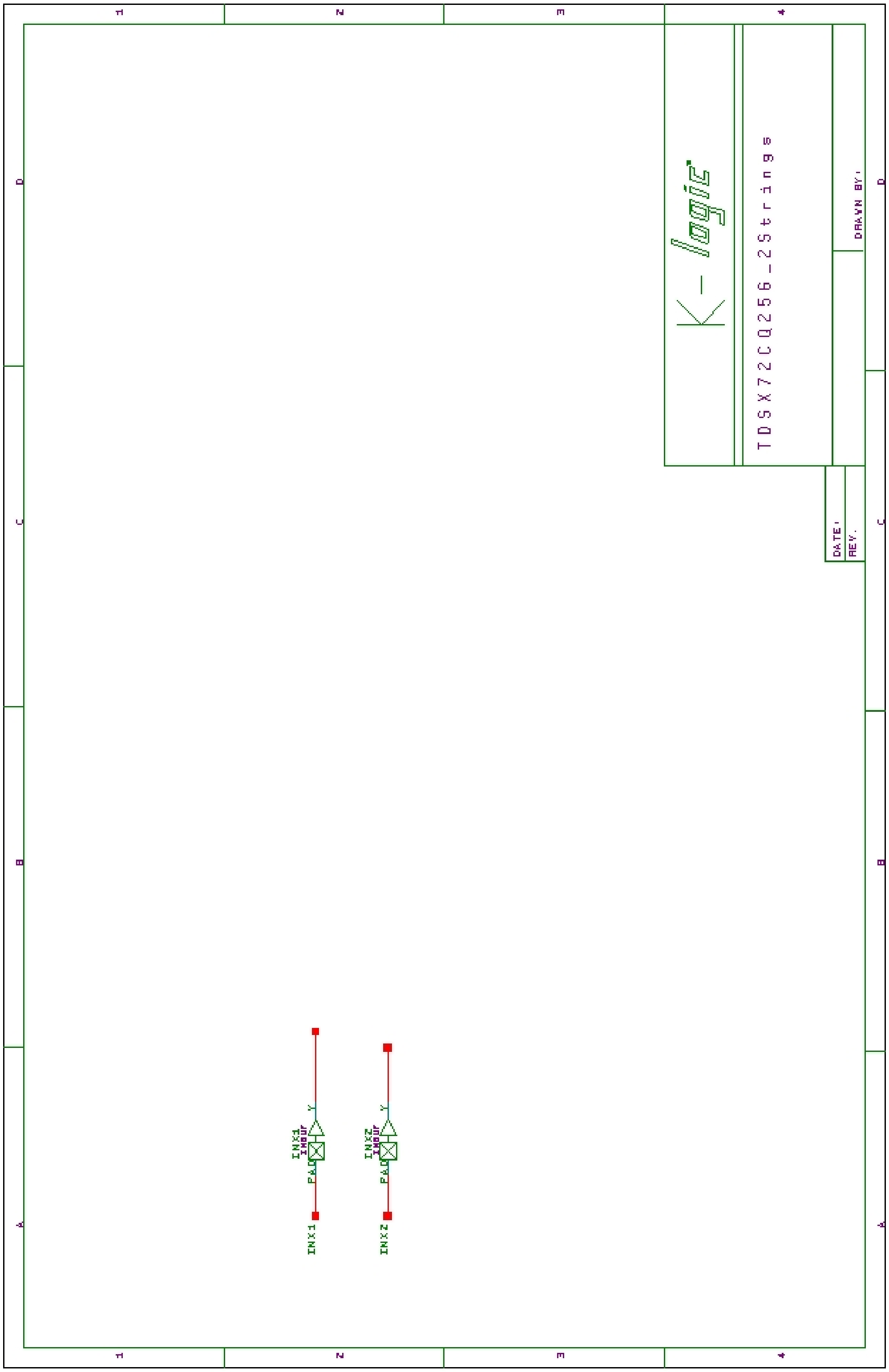
CNTCLR
CNTEN
CNTALD
CNTLD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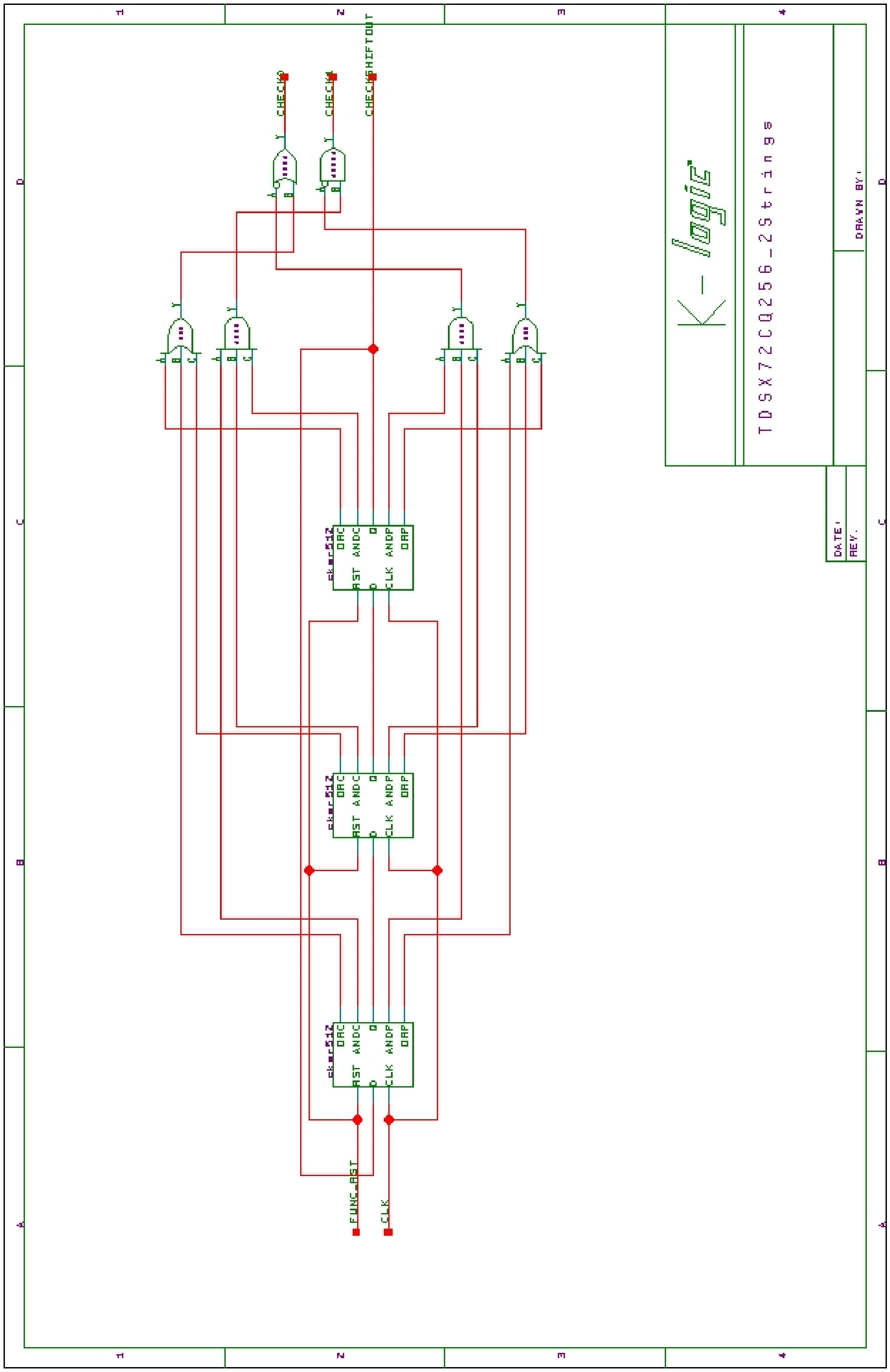
INX2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DRAWN BY:
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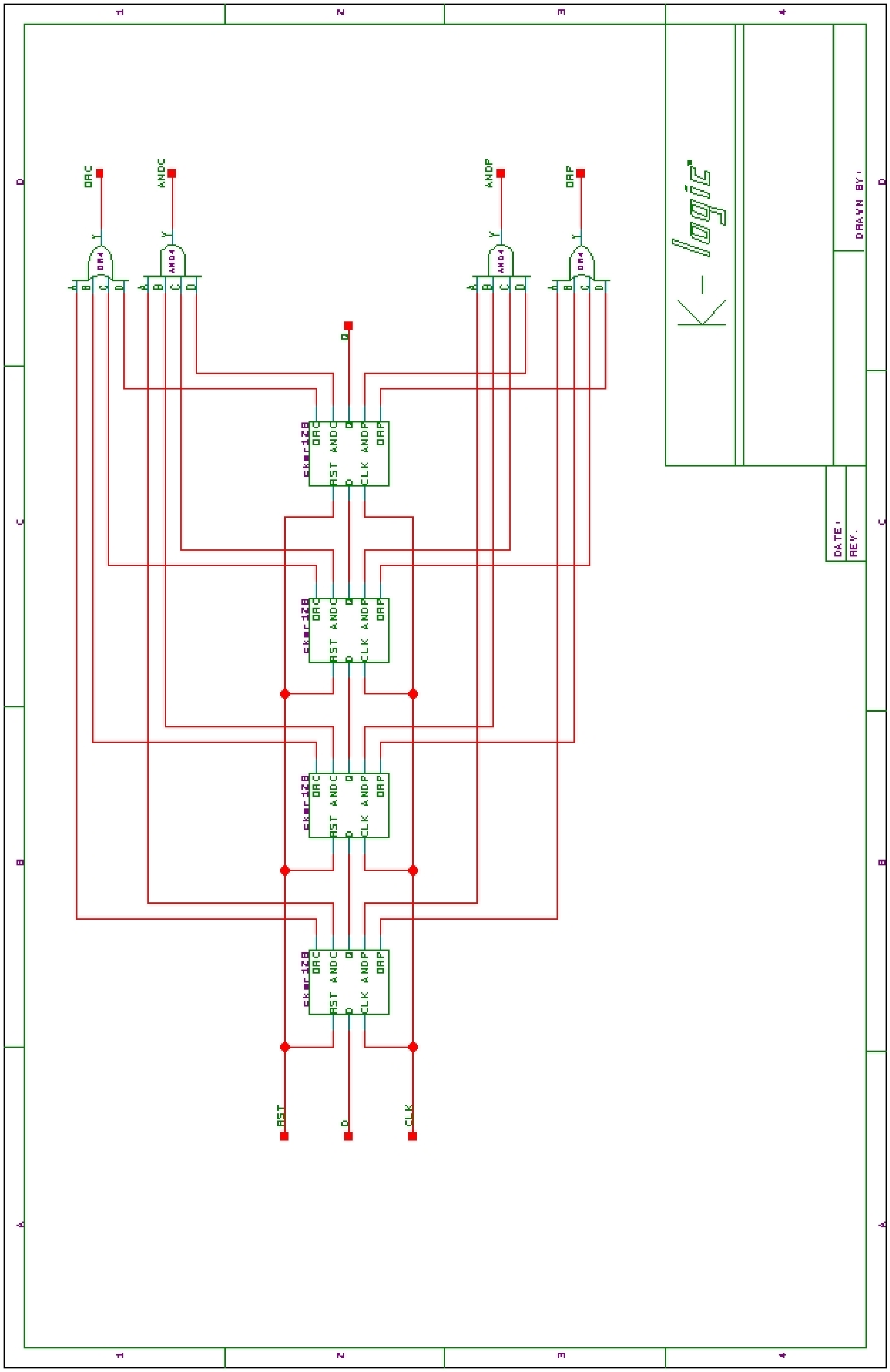
REV.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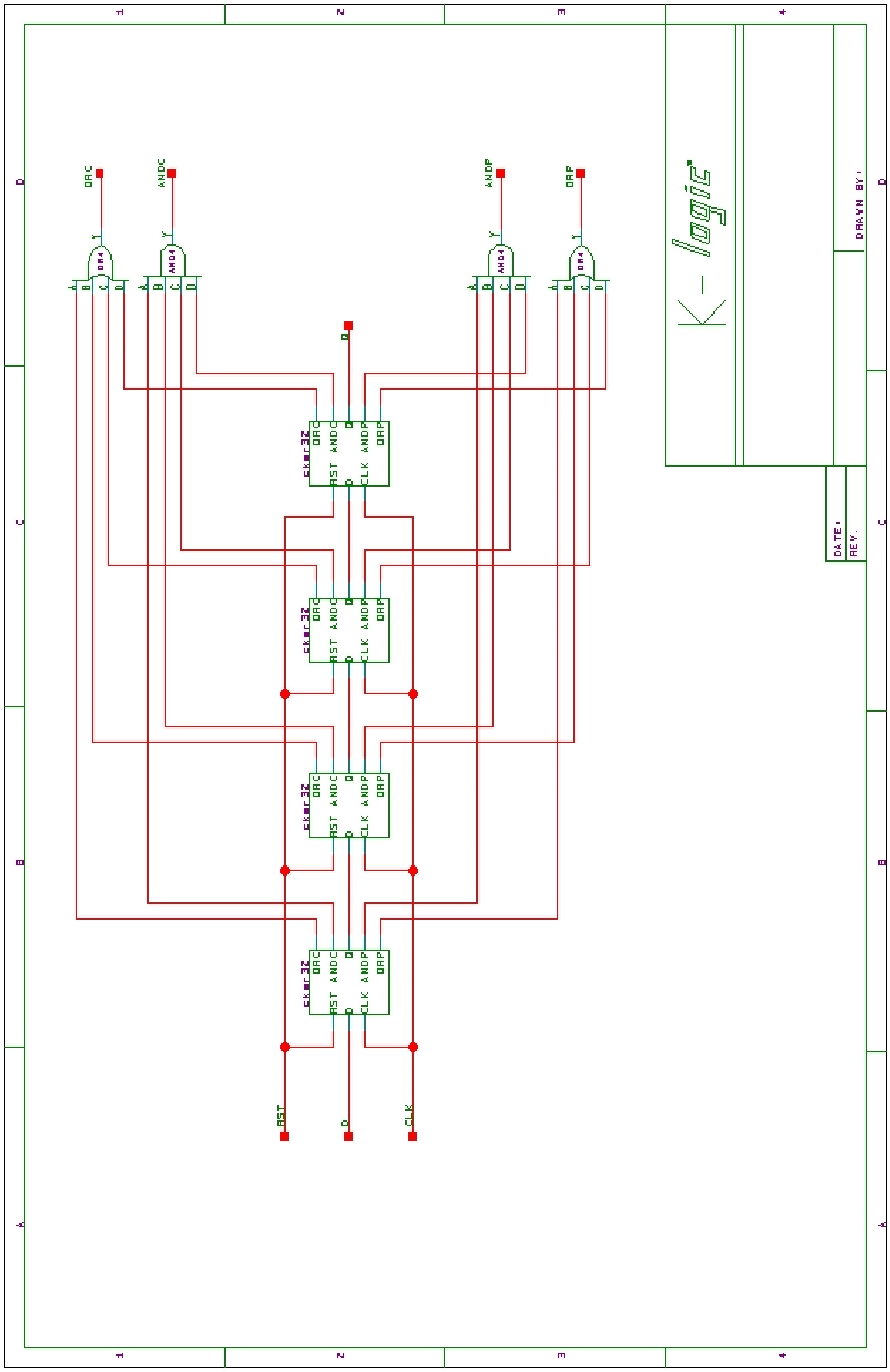
ANDP
ORP
Q
ckmr128
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.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RST
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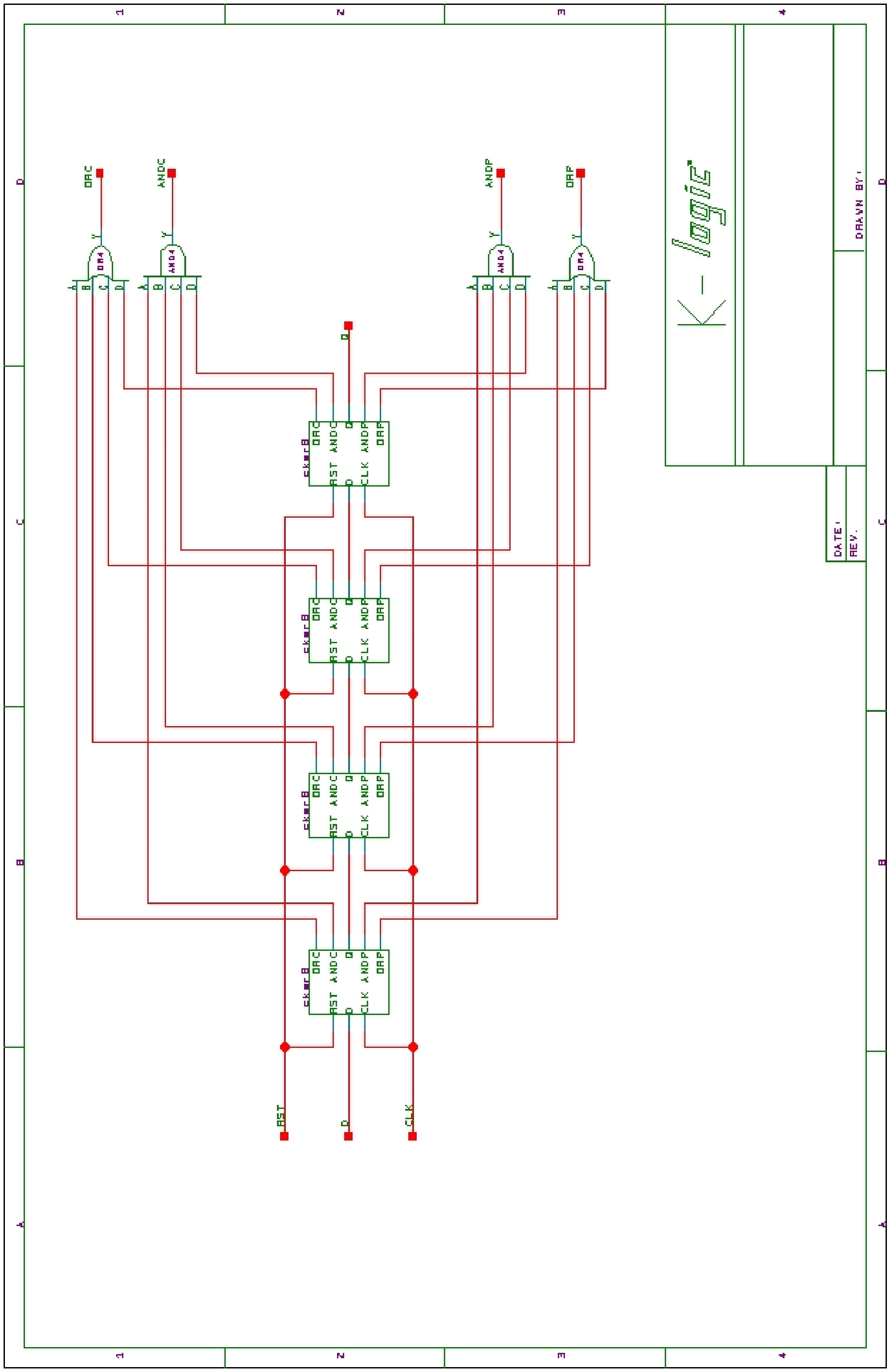
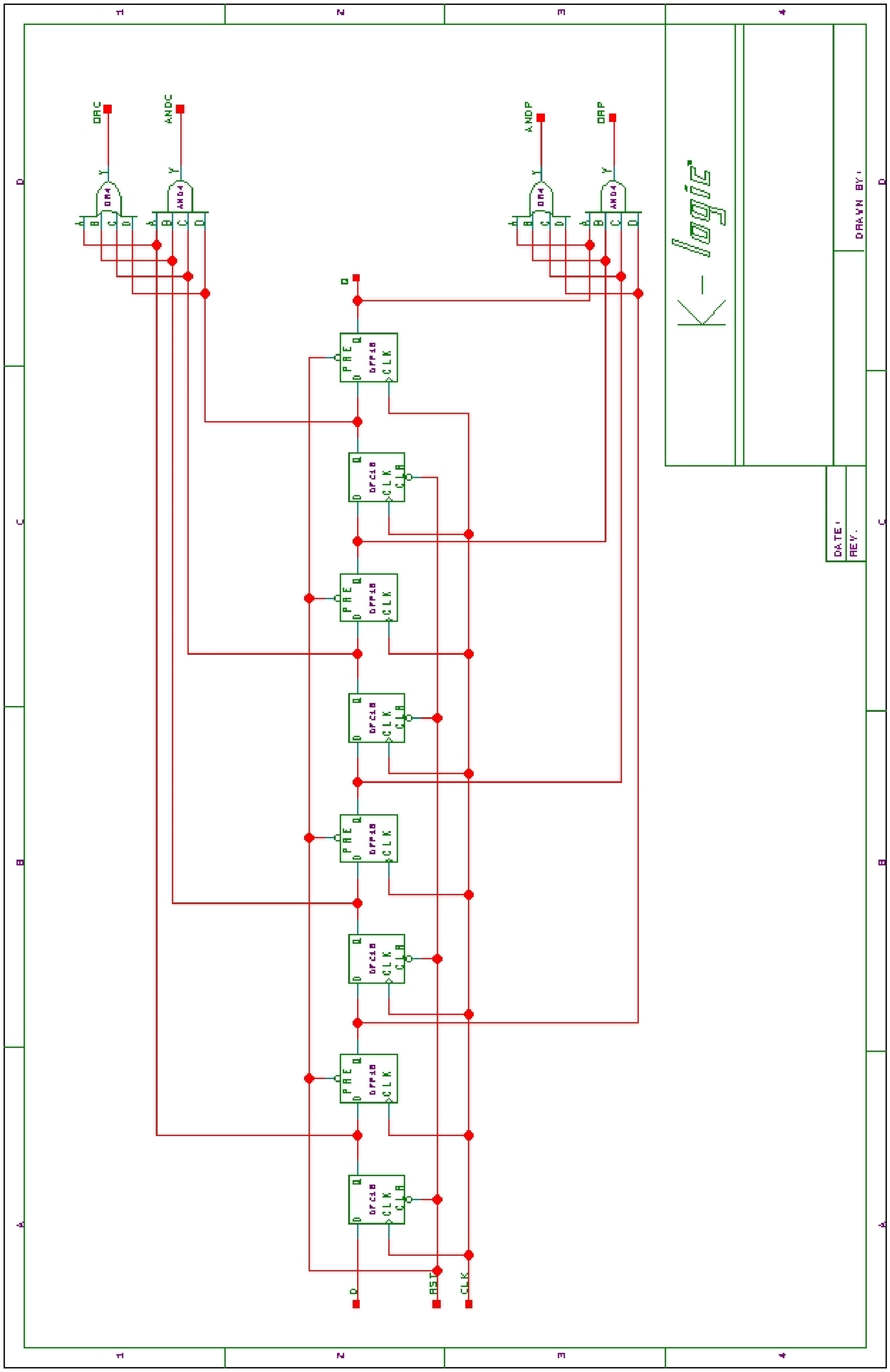
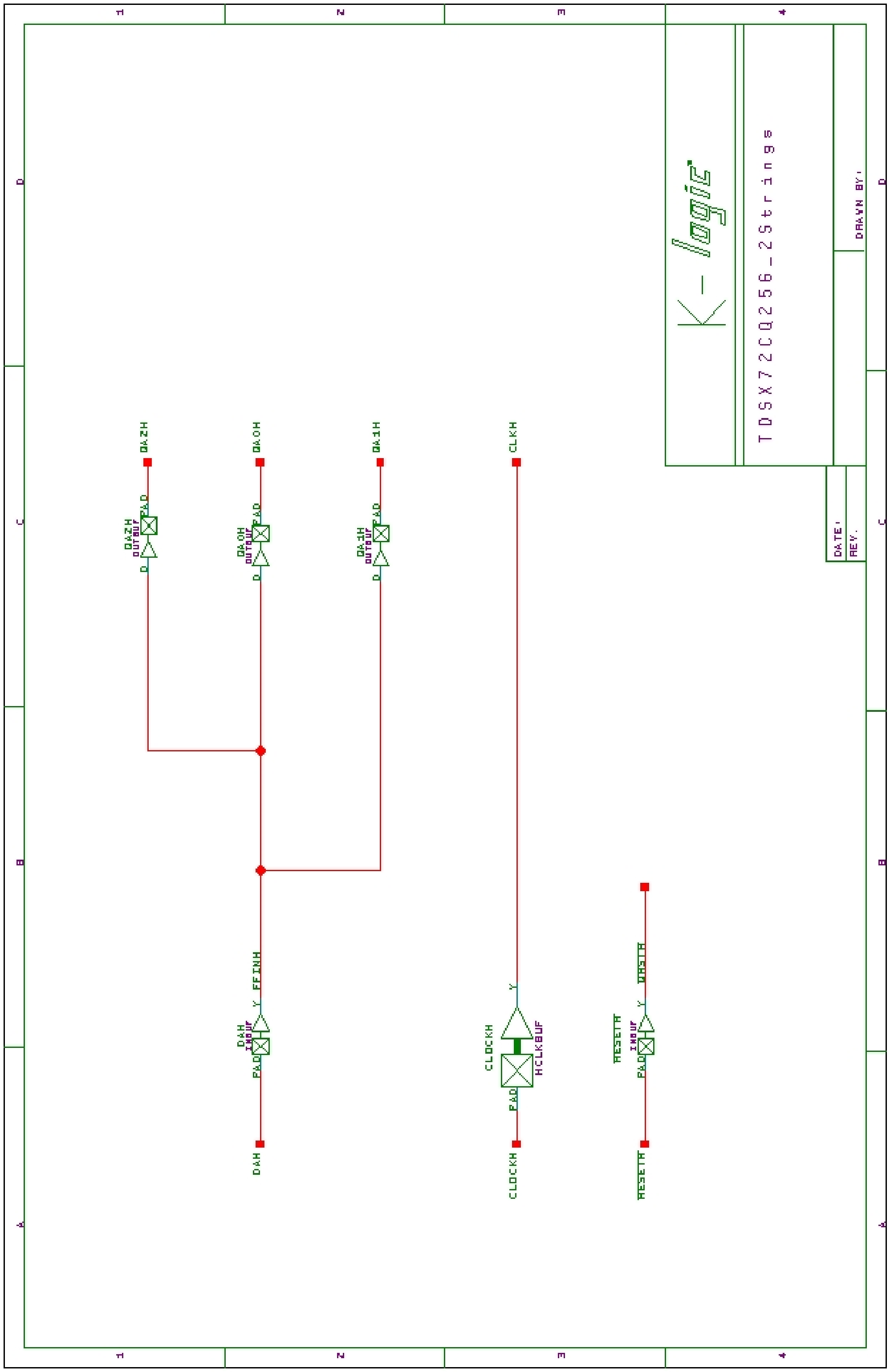
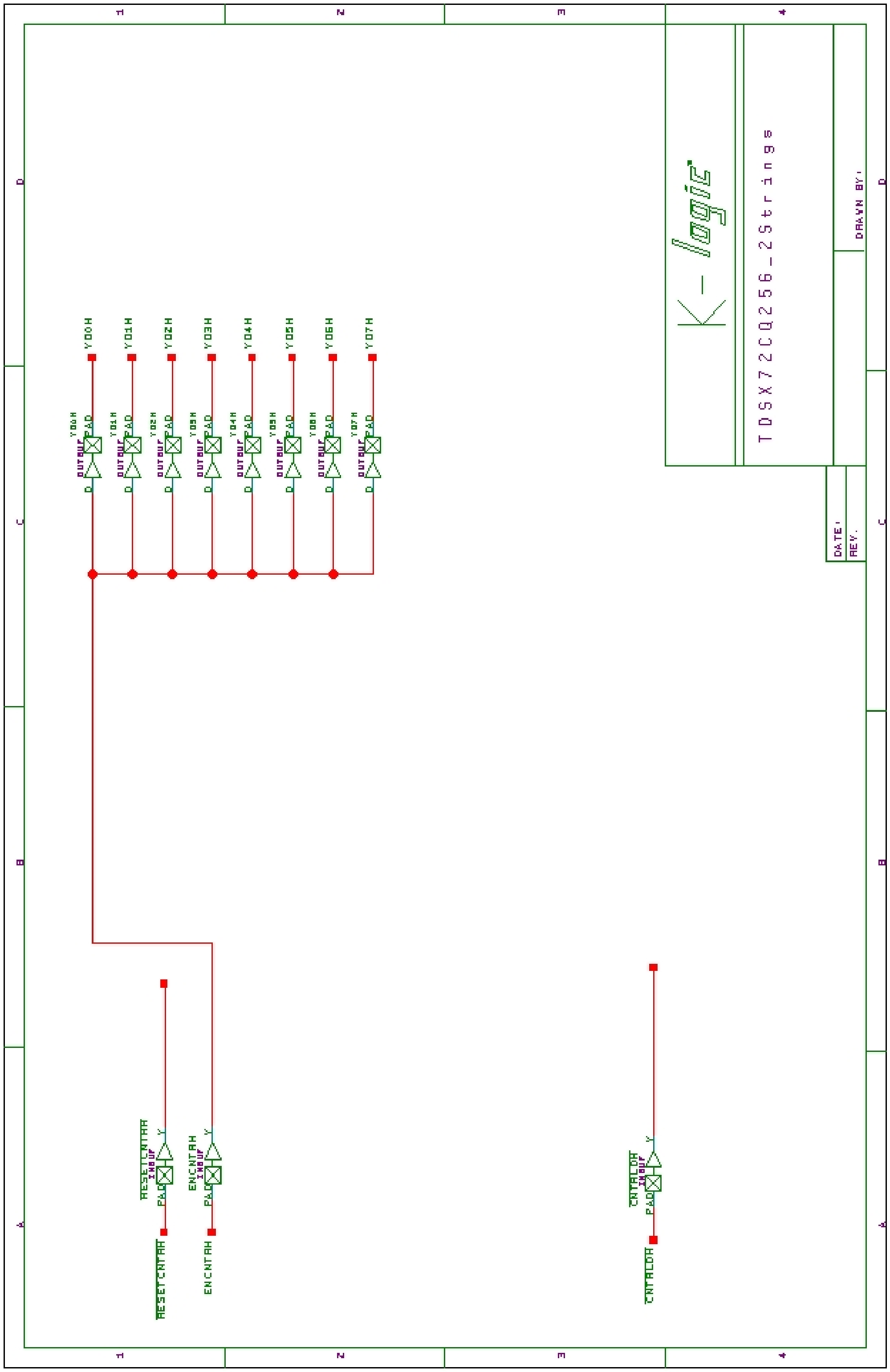
DRAWN BY:
DATE:
REV.

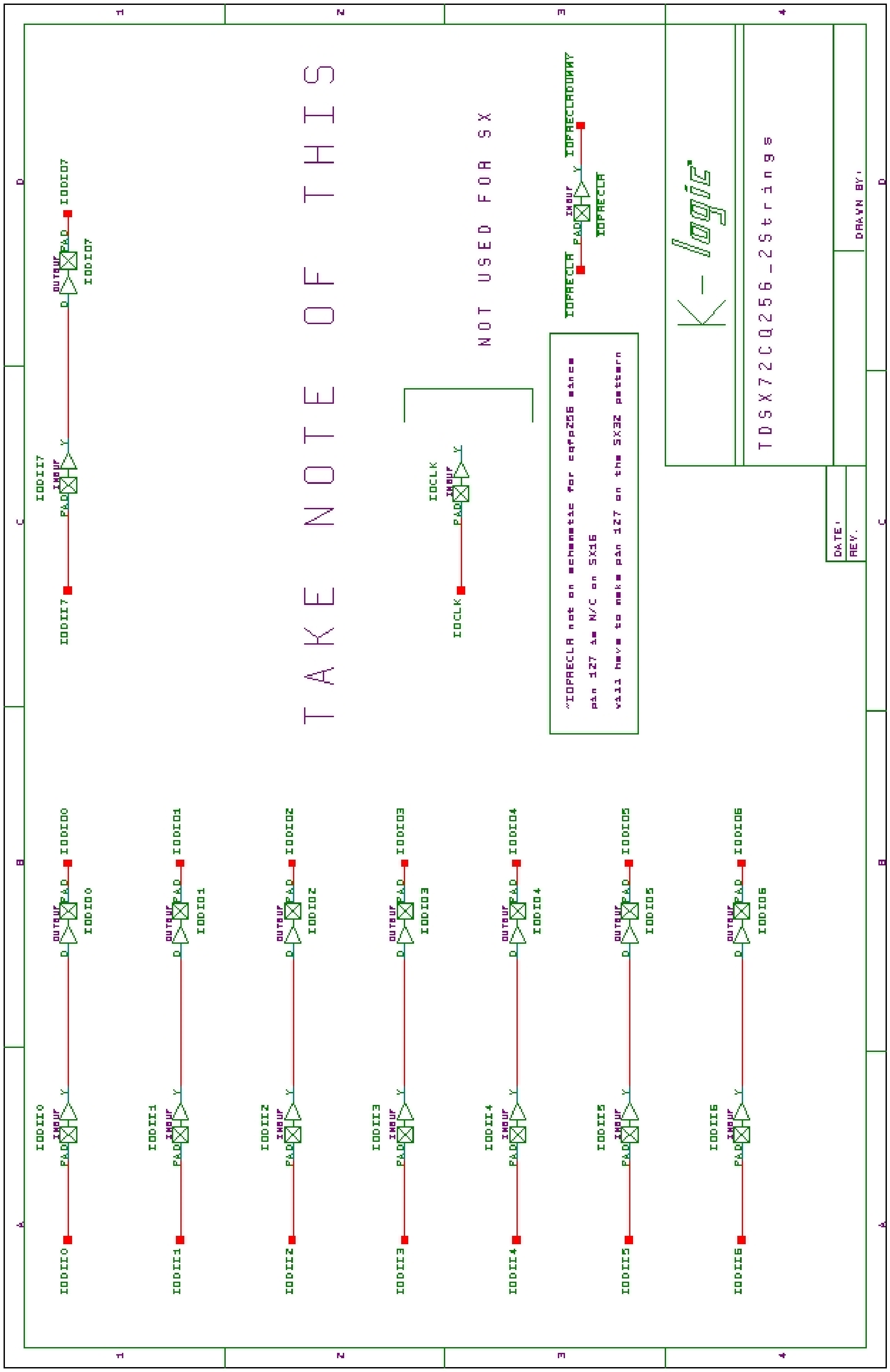

ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
K – logic
DRAWN BY:
DATE:
REV.


ORC
ANDC
ANDP
ORP
Q
D
RST
CLK
DFF1B
DFC1B
K-logic
DRAWN BY:
DATE:
REV.

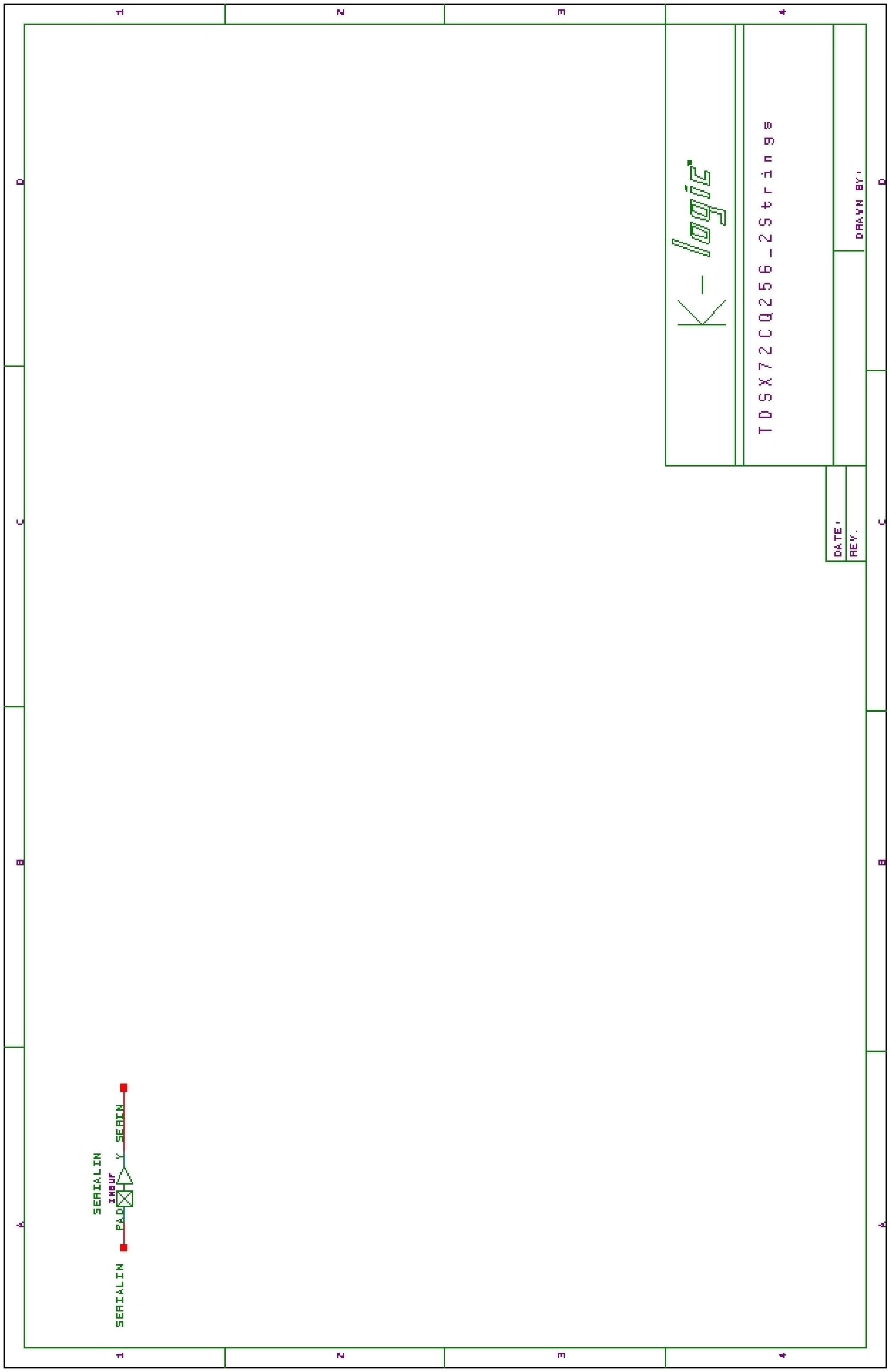


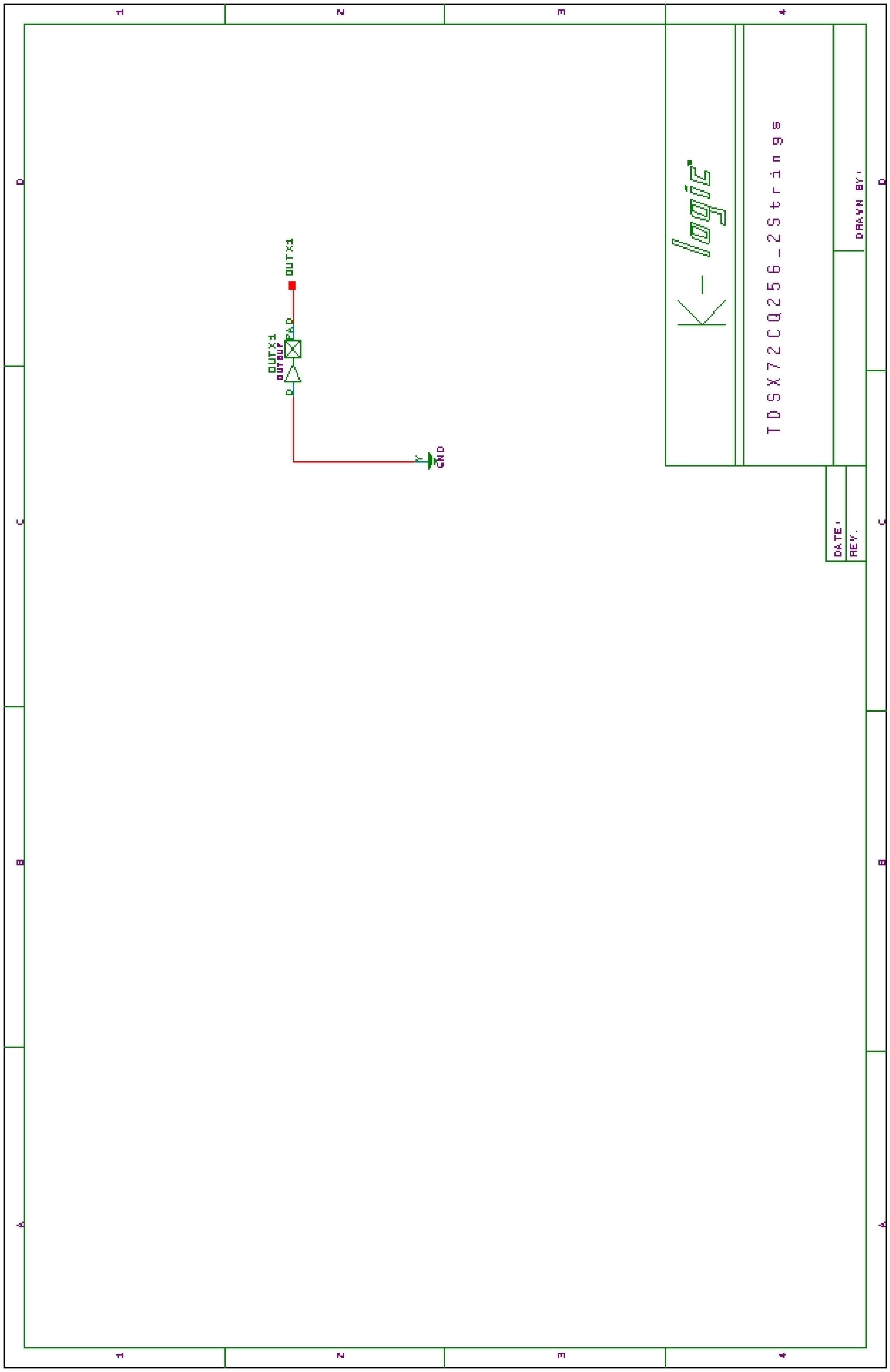
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:
DA2H
DA0H
DA1H
CLKH
DAH
FFINH
CLOCKH
HCLKBUF
RESETH
OUTBUF
INBUF
PAD


Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
OUTBUF
PAD
D
INBUF
Y
RESETCNTAH
ENCNTAH
CNTALDH
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.



TAKE NOTE OF THIS
NOT USED FOR SX
"IOPRECLA not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
IOPRECLA
IOPRECLADUMMY
IOCLK
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
SERIALIN
SERIALIN
INBUF
PAD
Y
SERIN


OUTX1
PAD
OUTX1
OUTBUF
D
GND
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.