Actel's ProASIC Family: The non-volatile, reprogrammable gate array

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Profile
The world's leading supplier of antifuse based FPGAs, Actel, is dedicated to becoming the field programmable gate array provider of choice.

The company's FPGAs are used by manufacturers of communications, computer, consumer, industrial control, military/aerospace, and other electronic systems to bring complex, high-density digital designs to market rapidly. Actel has recently introduced the industry's first family of reprogrammable FPGAs based on Flash technology, and is readying a new line of reprogrammable SRAM-based FPGAs.

Non-Volatile Reprogrammable FLASH Technology
- Live at Power-Up
- No Configuration Boot Device Required
- Retains Configuration During Power-Up/Down

Low Power Consumption
- Small Efficient Logic Cells
- Segmented Hierarchical Routing Structure
- Low-Power Impedence Flash Switches
- Improved System Reliability
- Eliminate External Fans and Heat Sinks

High Capacity
- 98,000 to 1.1 Million System Gates
- 30–50% smaller than equivalent sized FPGAs
- 14K to 138K Bits of Two-Port SRAM

Secure Programming
- Security Bit Prevents Read Back of Device Configuration Data

ProASIC Product Profile

	A500K050	A500K130	A500K180	A500K270	A500K350	A500K440	A500K510
Maximum System Gates	98,000	287,000	369,000	473,000	638,000	956,000	1,100,000
Typical Gates	43,000	105,000	150,000	215,000	280,000	350,000	410,000
Maximum Flip-Flops	5,376	12,800	18,432	26,880	34,816	43,776	51,200
Embedded RAM Bits	14K	46K	55K	65K	74K	124K	138K
Embedded RAM Blocks (256 X 9)	6	20	24	28	32	54	60
Logic Tiles	5,376	12,800	18,432	26,880	34,816	43,776	51,200
Maximum User I/Os	210	312	368	446	496	570	623
JTAG	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package (by Pin Count) PQFP PBGA FBGA	208 272	208 272, 456	208 456, 580	208 456, 580	580	580	580

Company Information

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A500K130 die
(actual size)

ProASIC devices work equally well in ASIC and FPGA design environments, allowing designers to leverage their existing design tools.

Actel's ProASIC 500K devices are supported by ASICmaster™ and MEMORYmaster™ software, as well as third party CAE tools, offering designers an open design environment.

ProASIC Design Methodology FAQ's

- **What special settings are needed for the export of VHDL netlists and forward constraints (SDF) for ASICmaster from Synopsys Design Compiler?**

  Actel recommends the following settings:

```
define_name_rules NO_SLASH -restricted
    "/" -replacement_char "_"
default_name_rules = NO_SLASH
vhdlout_bit_type = std_logic;
vhdlout_bit_vector_type =
    std_logic_vector;
bus_naming_style = "%s_%d"
bus_dimension_separator_style = "_"
```

  Before writing out the netlist or the constraints file, use the following command to make sure that these rules are applied everywhere in the design:

```
change_names -hierarchy
```

- **How do you minimize runtime with a design that contains multiple instantiations of one block?**

  The block instantiated multiple times should be placed and routed separately. The *last_placement.gcf* file of the result is then used to create a macro placement for this block. Refer to the *ASICmaster User's Guide* for details on macro syntax and macro placement.

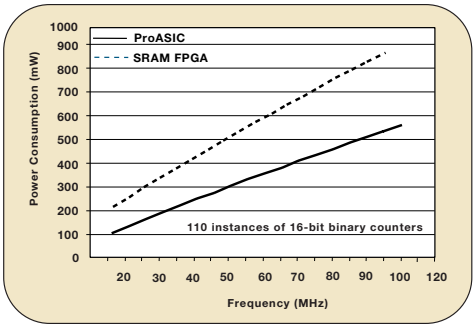

Figure 1: ProASIC Power Consumption

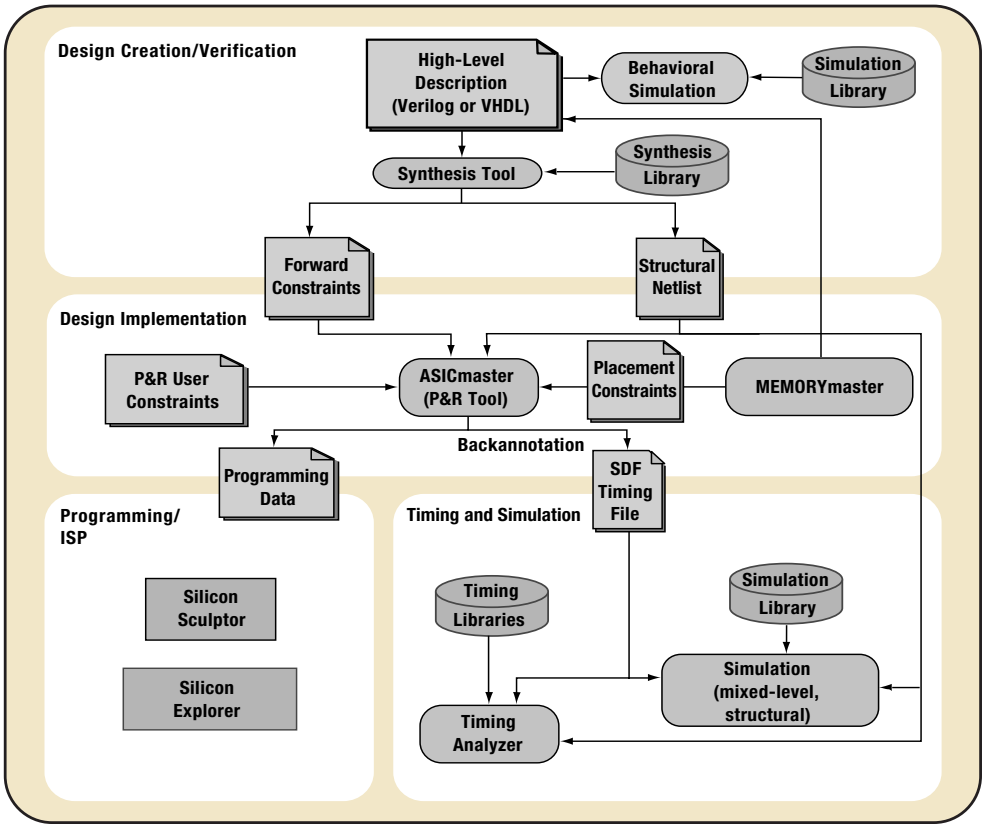

Figure 2: ASICmaster Design Flow

- **How do you force a net on the global network?**

  There are two ways to force a net onto one of the four global networks with in ASICmaster:

  1. Assign the signal a global pad location.

```
set_io clock <global_pad_location>;
```

  2. Use the set_global constraint:

```
set_global clock1;
```

  Both constraints have to be submitted to ASICmaster in a constraints file.

- **How can an input signal, which was assigned to a global pad location, be placed on a normal routing resource without wasting the global network?**

  To place an input signal assigned to a global pad location onto a normal routing resource and to use the global net for an internal signal use the GLIB buffer. This buffer connects the pad with a normal routing resource while connecting a second internal signal with the global network.

- **How do you limit fanout in a design?**

  During checking phase, ASICmaster deletes all buffers and inverters restricting fanout by default. This is done to limit routing congestion by the insert buffer tree. In some cases, the congestion of a design is low and timing can be improved by leaving the buffers in the netlist. In such a case the default deletion can be overwritten with the `set_max_fanout` constraint. This constraint has to be delivered to ASICmaster in a constraints file with the following syntax:

```
set_max_fanout 16;
```

  This will result in the deletion of all the buffers, which are driving less than 16 input pins.