Actel®

Active-HDL™

Complete FPGA Verification Environment

ALDEC, INC

DO-254 COMPLIANCE SOLUTION

Aldec provides a complete software/hardware solution for verification and validation of airborne systems to meet airborne system safety requirements as specified by the DO-254 objectives.

Verification Methodology

The verification proposal of each design consists of four stages of verification: RTL and timing simulation, co-simulation of the design in hardware with the software testbench, and design prototyping in hardware at high speed. According to DO-254, simulation is an important design analysis tool, both for design operation visualization and high-level functional verification.

A multi-stage solution, such as that from Aldec and Actel, can allow hardware design verification of each phase of the design creation and implementation. Designers are able to use the same testbench and a set of golden vectors for validation of RTL code both in the software simulator and in the hardware.

Testing Compliance

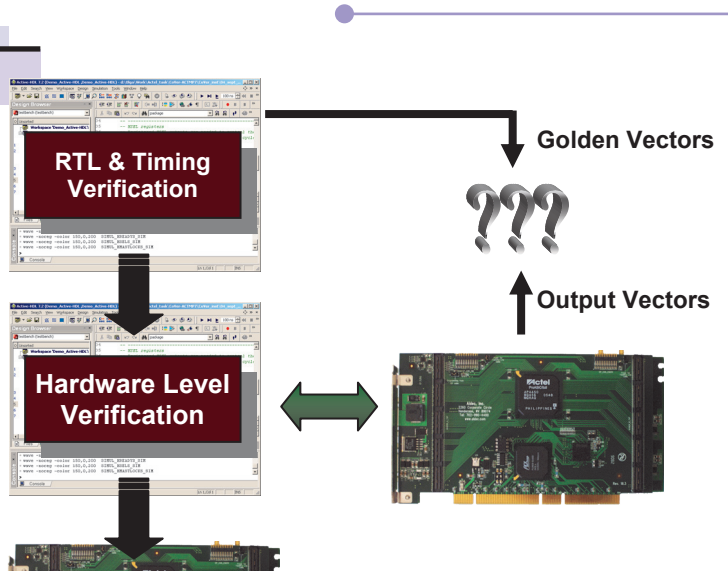
Simulation results from RTL and gate level simulation are saved in a waveform file and compared against the results of the design verification from the hardware. Assuming all results are the same, compliance between the HDL model and physical hardware will be achieved.

Hardware in the Loop

Simulation in hardware is used to achieve two major goals: functional design verification in real hardware and running more test cases against the design in the hardware with high simulation performance.

Aldec's compliance solution automatically implements an RTL design into the hardware (FPGA board) and reuses the same set of testbenches as in RTL simulation. By comparing signal waveform files from hardware and RTL simulation, functional verification of the design logic in the hardware is proved.

High speed design prototyping is an important stage of the design verification. Aldec's software assists in building a prototype model by retargeting the design from Actel's antifuse to flash architecture.



Benefits:

- Rapid design validation in hardware using RTL testbench and waveform output file
- Automatic setup of the design to hardware
- Automatic architecture retargeting for design prototyping
- Complete solution for hardware design verification

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