Axcelerator Evaluation Platform

The Axcelerator evaluation platform has been designed to demonstrate the unique capabilities of Actel's new Axcelerator family of FPGAs. It provides the designers an easy to use hardware platform to evaluate and test various Axcelerator features such as the PLL, LVDS I/Os, Block RAMs, etc. The modularity of the platform allows the designer to build systems to their own special requirements, providing them with a vehicle to test their FPGA design.

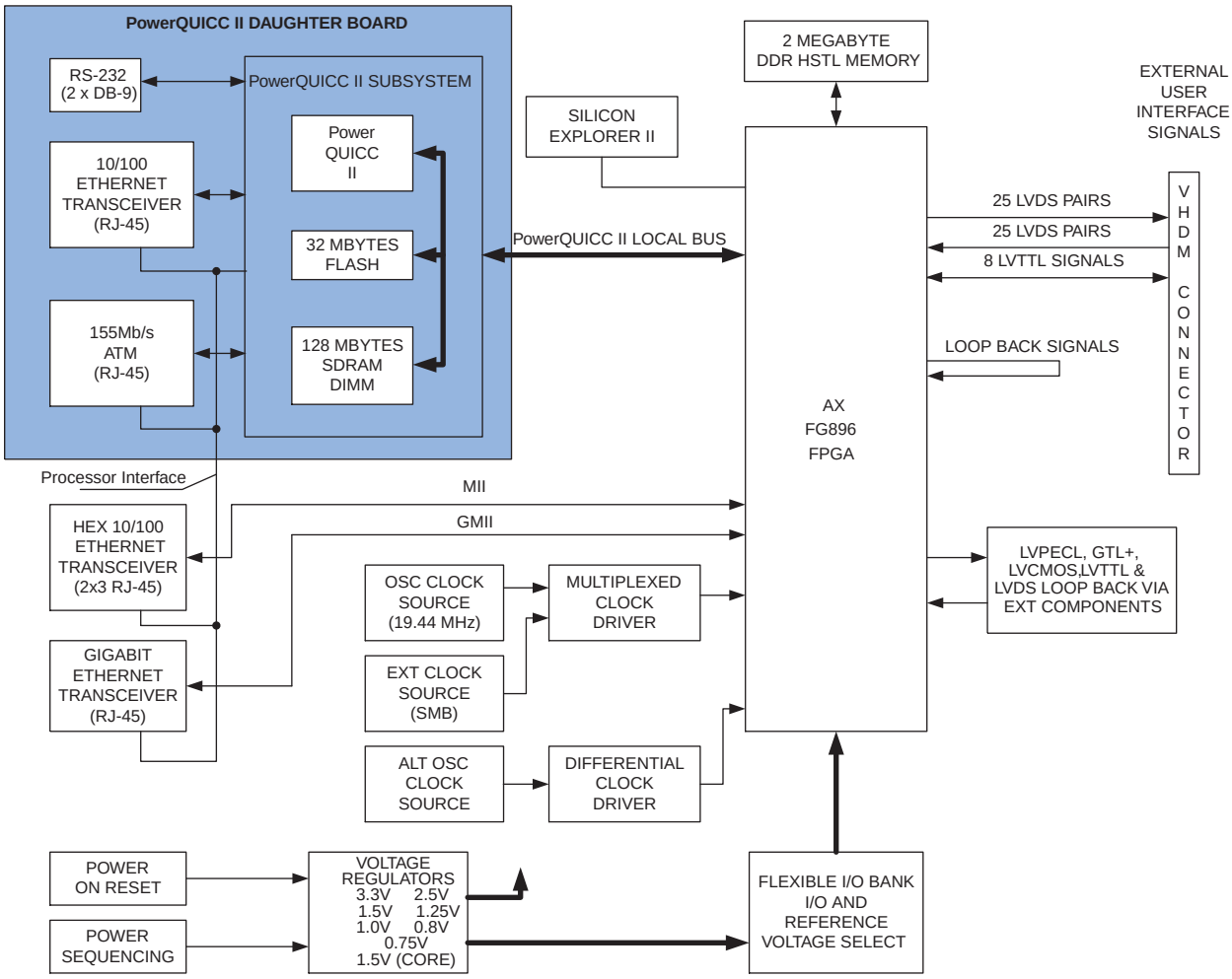

Figure 1 • *Demo Board Block Diagram*

Features

Mother Board

- LXT9763 Hex Ethernet Transceiver
- LXT1000 Gigabit Ethernet Transceiver
- VHDM High Speed Connector
- HSTL DDR Memory
- FG896 FPGA Socket

Daughter Board

- PowerQUICC II Microprocessor
- 32 MB Flash Memory
- 128 MB SDRAM
- LXT971 Ethernet Transceiver
- PM5350 155 MB/S ATM
- RS232

Basic Building Blocks

The evaluation platform is separated into two pieces: a mother board and a daughter board. The mother board contains the Axcelerator FPGA (socketed), clocks, voltage selector for I/O bank V_{REF}s, daughter board connectors, and a Silicon Explorer II connector.

The daughter board contains a PowerQUICC II Microprocessor, 32MB of Flash Memory, 128MB of SDRAM, and is connected to the mother board through the mezzanine connectors.

Communication System Development

The Axcelerator demo board provides a complete hardware environment for developing and testing communication system FPGA design. The Hex Ethernet and the Gigabit Ethernet transceivers allow the FPGA to communicate with other Ethernet devices, giving a designer the ability to monitor traffic between the FPGA and other devices in the system.

Loop-Back Board

A loop-back board is provided with each Axcelerator demo board. This loop-back board connects to the VHDM connector of the Axcelerator demo board. It allows outputs from the Axcelerator device to be brought back to inputs of the Axcelerator device (Figure 2).

Mini Backplane

An optional mini backplane, which allows two Axcelerator demo board to be connected together, is also available from Actel. This mini backplane allows the two Axcelerator devices to communicate with each other, giving the designer the ability to simulate/test two communication systems and their communication with each other (Figure 3).

Silicon Explorer II Header

A Silicon Explorer II header is used to further enhance the development process by allowing the designer to use the Silicon Explorer II to perform real time probing without having to recompile and reprogram.

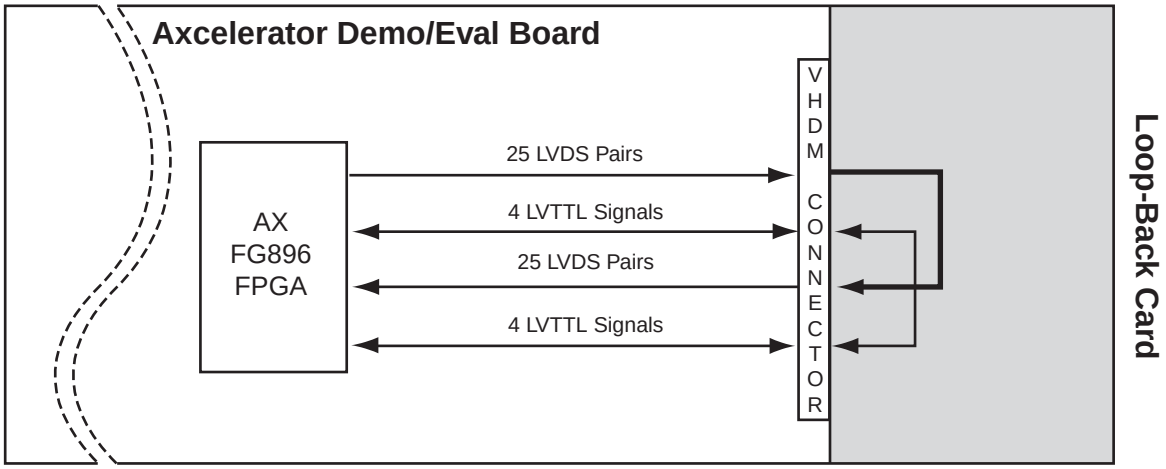

Figure 2 • *System Block Diagram (1 Card)*

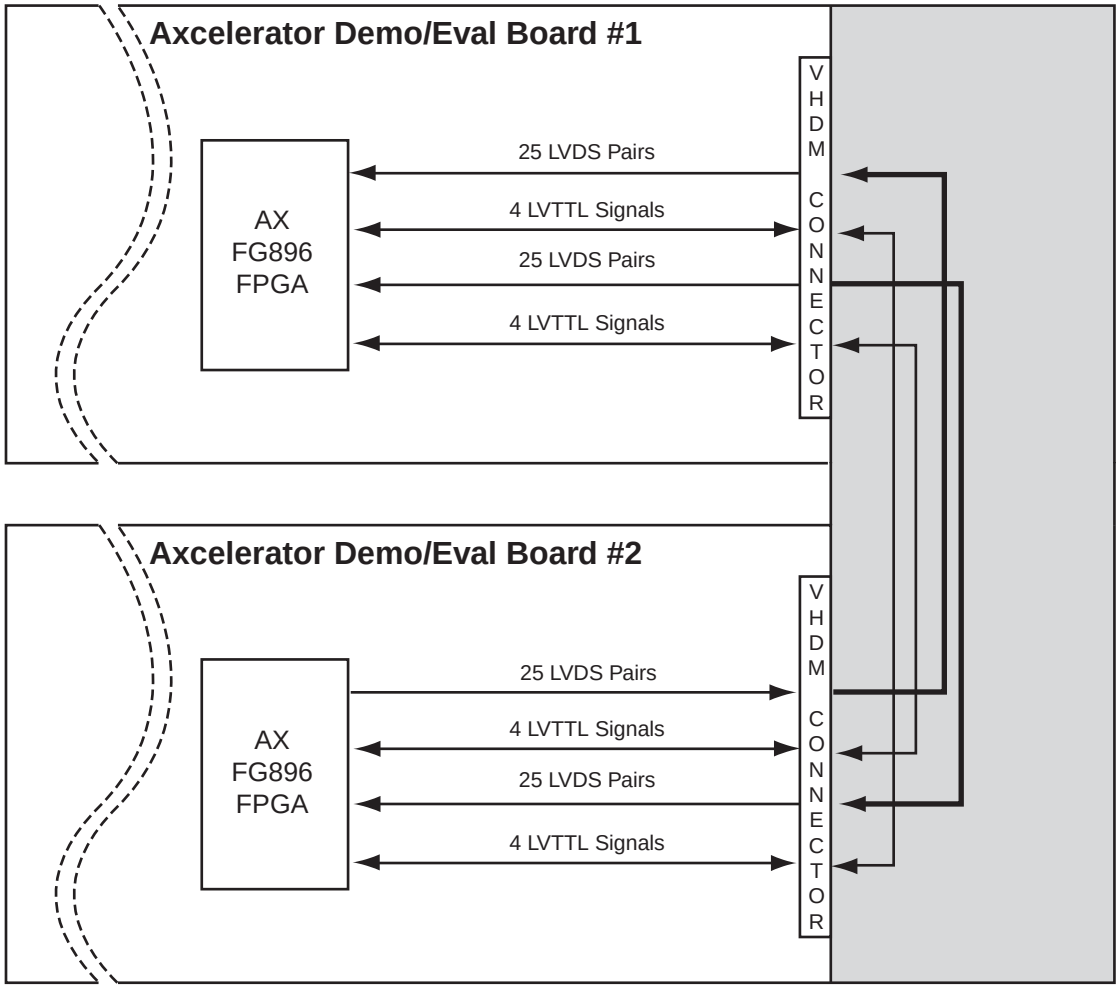

Figure 3 • *System Block Diagram (2 Card)*

Demonstration Application

One of the key features of this board is to demonstrate the wide range of I/O standards that the Axcelerator FPGA supports. The Axcelerator FPGA is configured to transmit and/or receive using the following I/O standards: LVTTL-3.3V, LVCMOS-2.5V/1.8V/1.5V, GTL+, HSTL Class I, LVDS, LVPECL, SSTL2 Class I, SSTL2 Class II.

Application Software

The application software consists of two parts: a PC Window-based client application and an embedded server running on the PowerQUICC II processor. The application software allows the user to control the PowerQUICC II 10/100 Ethernet and ATM interface, the Hex 10/100 Ethernet interface on the main board, and other Gigabit Ethernet devices via MDIO. The application also allows the user to run diagnostic tests, Double Data Rate (DDR) memory test, LVDS loop-back, Ethernet Interfacing, as well as read and modify memory mapped FPGA status and user registers.

All of these functions are selected and controlled through the Graphical User Interface and all results are displayed for easy debugging. Communication from the PC to the Axcelerator demo board is done via the 10/100 Ethernet Interface.

Kit Contains

- Mother Board
- PowerQuicc II Daughter Board
- Loop-back Board
- Power Supply
- RS232 Cable
- CD – User Guide, Demo Design Files, Board Schematic, Application Software
- CAT-5 Cable(s)

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