Antifuse Macro Library Guide

for Software v9.0SP1

Actel®

Actel Corporation, Mountain View, CA 94043

Part Number: 5029009-25

Release: July 2010

Trademarks

Table of Contents

Introduction

Lists

Introduction

This guide includes macros for all Actel antifuse devices. For flash devices, see the *Fusion, IGLOO and ProASIC3 Macro Library Guide*.

Definitions

Macros

The Macro library consists of logic elements constructed of one or more ACT family modules. Modules may be of type sequential or combinatorial. The relative placement of two module-macros is predefined. The timing characteristics are a function of the fanout on the output of the macro.

SmartGen Cores

SmartGen cores are described in Actel's publication *SmartGen Cores Reference Guide*.

How to Use this Guide

Family Inclusion Indicator

In the titlebar of each macro is a list indicating whether the cell is a member of the ACT 1, ACT 2, 3200DX, ACT 3, MX, SX, SX-A, eX, or Axcelerator library.

Guidelines

1. All input pin loading is assumed to be a single load except macros that are built using two combinational modules or one sequential and one combinatorial module. These macros are assumed to have a load of two on some of their input pins.

2. All macros have output pin loading of zero except for the sequential macros that are built using two combinational modules only. These macros have an output pin loading of one.

3. All macros have logic levels equal to one except cells with pin delays of two. A "2" is added to the corresponding symbol in the macro section of this manual.

Truth Table Nomenclature

Truth tables are arranged with *Inputs* before *Outputs*. The following symbol definitions apply.

↑	denotes rising edge clock
↓	denotes falling edge clock
X	in an input column denotes a 'don't care' or logic simulation state 'unknown'
!Q	denotes Q not

Pin Delay Annotation

Two-module combinatorial macros contain extra delay on some or all of the pins. If a macro symbol in this guide displays a "2" on a pin, then two levels of logic delay exist on the input to output path.

Note: Many two-level logic functions in one family are implemented in a single module in another family, hence the "2" may apply to specific families only.

Restrictions

Special I/Os

Some I/O pins are able to connect to global control signals such as clock or clear. These I/O pins may be used as "normal" data input/output buffers or they may be used as "special" pins. The following constraints apply to I/O pins used as "special" pins.

All ACT 2, 3200DX, ACT 3, MX, SX, SX-A, and eX register cells may be clocked by either of the two global clock networks by connecting their CLK input to the output of a CLKBUF, CLKBIBUF, or CLKINT macro.

All ACT 2, 3200DX, ACT 3, MX, SX, SX-A, and eX register cells may be globally preset, reset or enabled by connecting the PRE, CLR, or E input to the output of a CLKBUF, CLKBIBUF, CLKINT macro.

All ACT 2, 3200DX, ACT 3, MX, SX, SX-A and eX I/O three-state buffers may be globally enabled by connecting their E input to the output of a CLKBUF, CLKBIBUF, OR CLKINT macro.

All ACT 3, SX, SX-A and eX register cells composed of sequential modules may be clocked by high speed clock buffer network by connecting their CLK input to the output of a HCLKBUF macro.

ACT 3 registered I/O macros may only be clocked by the IOCLKBUF macro.

ACT 3 registered I/O macros may *only* be asynchronously set or preset by the IOPCL macro.

Advanced Application Notes

For Advanced Application notes, please go to the Actel website at http://www.actel.com.

HDL Instantiation of Macros

Refer to the *HDL Coding Style Guide* for information on instantiating macros.

Migration Between Families

Actel provides the capability of migrating a netlist created for one family to another family in some cases. Macros listed in this manual as being available in the old family will not be shown as available in the new family when the new macro is inefficient or when the function can be better implemented with different macros, however, the macro may be available in the new family. Such macros are not recommended for new designs.

In all cases, if an HDL description is available, it is best to resynthesize, targeting the new family.

If an HDL description is not available, it is still generally best to do gate level retargeting to the new family.

If neither of the above is done, a netlist created for one family may be used in another family as follows: No special procedures are needed to use the netlist in Designer, but a migration library must be enabled in CAE environments as explained in individual CAE Interface Guides.

	Target Family					
Original Family	ACT 1/MX	ACT 2/ 3200DX/MX	ACT 3	SX	SX-A	eX
ACT 1 or MX	X	YES	YES	NO	NO	NO
ACT 2, 1200XL, 3200DX, MX	NO	X	YES**	YES**	YES**	YES**
ACT 3	NO	NO	X	YES*	YES*	YES*
SX	NO	NO	NO	X	YES	YES
SX-A	NO	NO	NO	YES**	X	YES
eX	NO	NO	NO	YES	YES	X

* Except registered I/O, IOCLK, and IOPCL

** Except QCLK and RAM

List of Combinational Macros

List of Sequential Macros

List of CC Macros

List of RAM Macros

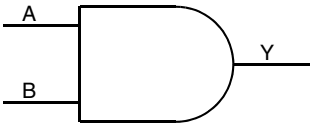
List of Input/Output Macros

Alphabetical List of Macros

Combinational/Sequential Macros

AND2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input AND

Truth Table

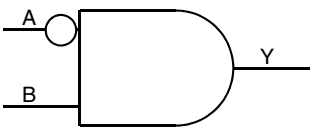
A	B	Y
X	0	0
0	X	0
1	1	1

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

AND2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input AND with active low A Input

Truth Table

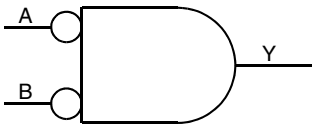
A	B	Y
X	0	0
0	1	1
1	X	0

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

AND2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input AND with active low Inputs

Truth Table

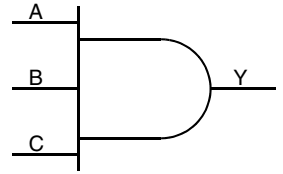
A	B	Y
0	0	1
X	1	0
1	X	0

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

AND3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND

Truth Table

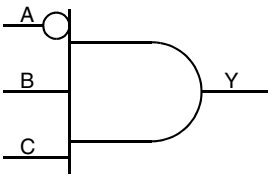
A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

Input	Output
A, B,C	Y

Family	Modules	
	Seq	Comb
All		1

AND3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND with active low A-Input

Truth Table

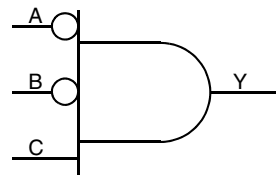
A	B	C	Y
X	X	0	0
X	0	X	0
0	1	1	1
1	X	X	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

AND3B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND with active low A- and B-Inputs

Truth Table

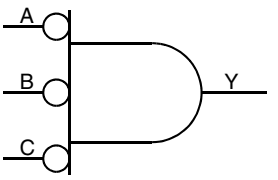
A	B	C	Y
X	X	0	0
0	0	1	1
X	1	X	0
1	X	X	0

Input	Output
A, B,C	Y

Family	Modules	
	Seq	Comb
All		1

AND3C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND with active low Inputs

Truth Table

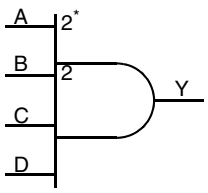
A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

AND4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

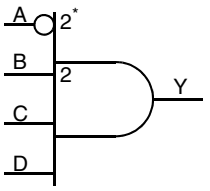
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays, only for ACT 1 and MX.

AND4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND with active low A-Input

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	1	1	1	1
1	X	X	X	0

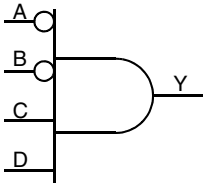
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
MX/ACT1		2
Others		1

* A 2 on the symbol implies 2 logic module delays, only for ACT 1 and MX.

AND4B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND with active low A- and B-Inputs

Truth Table

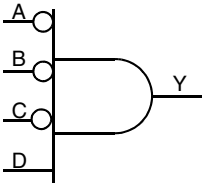
A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	1	1	1
X	1	X	X	0
1	X	X	X	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

AND4C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND with active low A-, B-, and C-Inputs

Truth Table

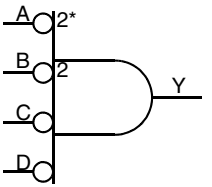
A	B	C	D	Y
X	X	X	0	0
0	0	0	1	1
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

AND4D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND with active low Inputs

Truth Table

A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

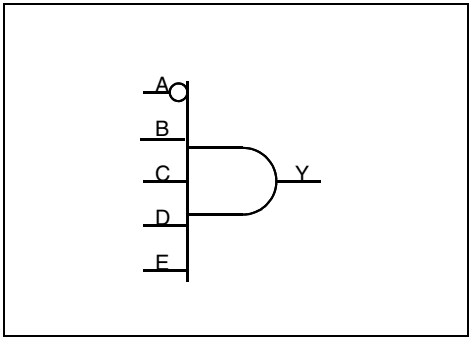
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
SX, SX-A, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays, except SX, SX-A, and eX.

AND5A

SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input AND with active low A input

Truth Table

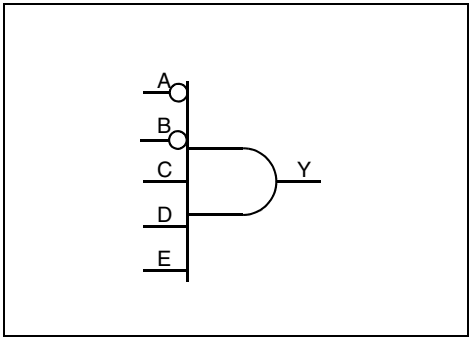
A	B	C	D	E	Y
0	1	1	1	1	1
1	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
All listed		1

AND5B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input AND with active low A-, and B-Inputs

Truth Table

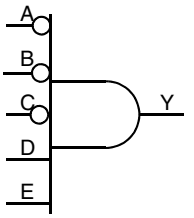
A	B	C	D	E	Y
X	X	X	X	0	0
X	X	X	0	X	0
X	X	0	X	X	0
0	0	1	1	1	1
X	1	X	X	X	0
1	X	X	X	X	0

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
All		1

AND5C

SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input AND with active low A-, B- and C-Inputs

Truth Table

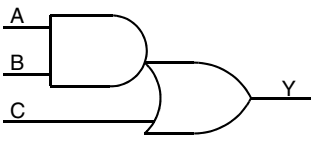
A	B	C	D	E	Y
0	0	0	1	1	1
1	X	X	X	X	0
X	1	X	X	X	0
X	X	1	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
SX, SX-A, eX, Axcelerator		1

A01

ACT1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR

Truth Table

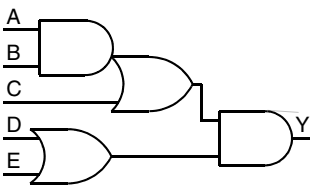
A	B	C	Y
X	0	0	0
X	X	1	1
0	X	0	0
1	1	X	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

AO10

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input AND-OR-AND

Truth Table

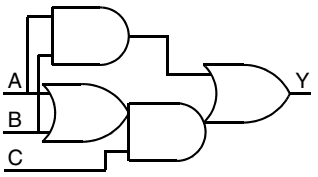
A	B	C	D	E	Y
X	X	X	0	0	0
X	0	0	X	X	0
X	X	1	X	1	1
X	X	1	1	X	1
0	X	0	X	X	0
1	1	X	X	1	1
1	1	X	1	X	1

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
All except ACT1 and MX		1

AO11

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR

Truth Table

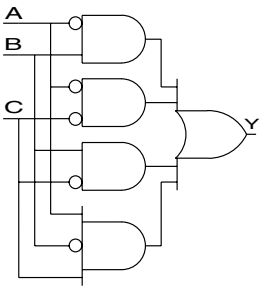
A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All except ACT1 and MX		1

AO12

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function

3-Input AND-OR

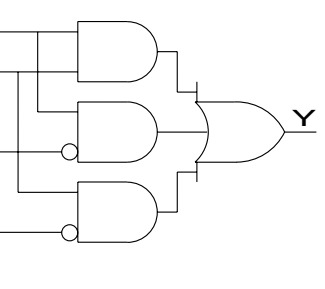
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

AO13

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function

3-Input AND-OR

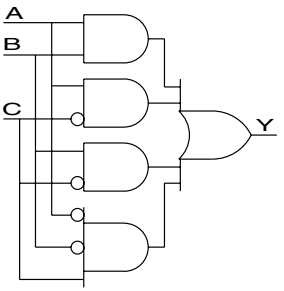
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

AO14

SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR

Truth Table

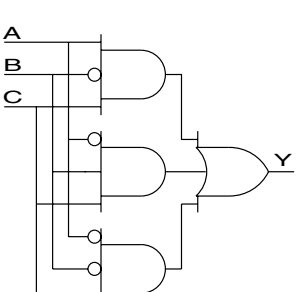
A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AO15

SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR

Truth Table

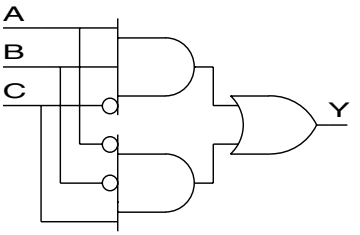
A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AO16

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function

3-Input AND-OR

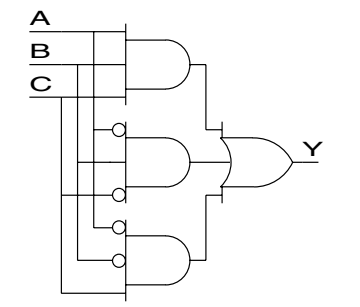
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

AO17

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function

3-Input AND-OR

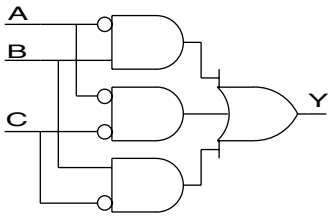
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

AO18

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function

3-Input AND-OR

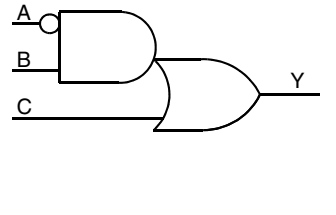
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

AO1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function

3-Input AND-OR with active low A-Input

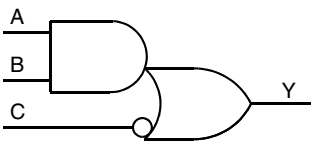
Truth Table

A	B	C	Y
X	0	0	0
X	X	1	1
0	1	X	1
1	X	0	0

Family	Modules	
	Seq	Comb
All listed		1

AO1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR with active low C-Input

Truth Table

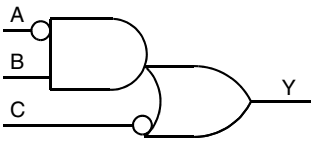
A	B	C	Y
X	X	0	1
X	0	1	0
0	X	1	0
1	1	X	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

AO1C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR with active low A- and C-Inputs

Truth Table

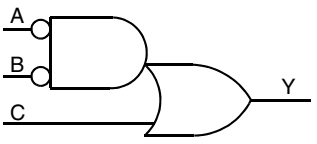
A	B	C	Y
X	X	0	1
X	0	1	0
0	1	X	1
1	X	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

AO1D

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR with active low A- and B-Inputs

Truth Table

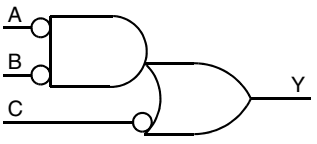
A	B	C	Y
0	0	X	1
X	1	0	0
X	X	1	1
1	X	0	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO1E

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR with active low Inputs

Truth Table

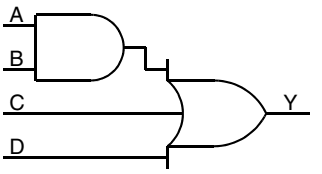
A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR

Truth Table

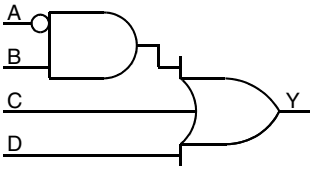
A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	X	0	0	0
1	1	X	X	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ALL		1

AO2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR with active low A-Input

Truth Table

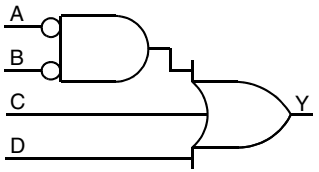
A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	1	X	X	1
1	X	0	0	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ALL		1

AO2B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR with active low A and B-Inputs

Truth Table

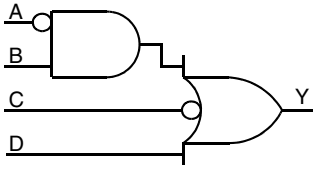
A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO2C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR with active low A- and C-Inputs

Truth Table

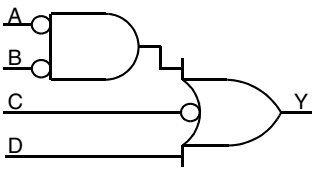
A	B	C	D	Y
1	X	1	0	0
X	0	1	0	0
0	1	X	X	1
X	X	0	X	1
X	X	X	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO2D

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR with active low A-, B- and C-Inputs

Truth Table

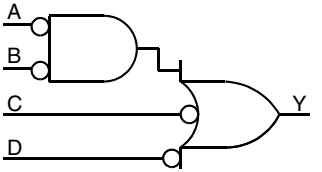
A	B	C	D	Y
X	X	0	X	1
0	0	X	X	1
X	1	1	0	0
X	X	X	1	1
1	X	1	0	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO2E

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR with active low Inputs

Truth Table

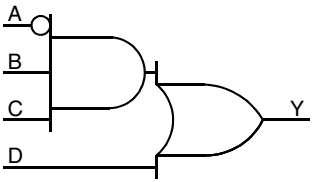
A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR with active low A Input

Truth Table

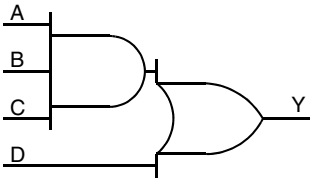
A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	1	1	X	1
1	X	X	0	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ALL		1

AO3A

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR

Truth Table

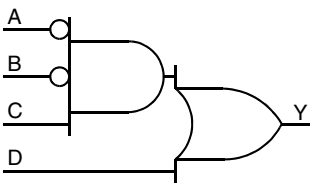
A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	X	X	0	0
1	1	1	X	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO3B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4 Input AND-OR with active low A-, B- Inputs

Truth Table

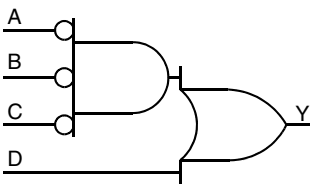
A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
0	0	1	X	1
X	1	X	0	0
1	X	X	0	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO3C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR with active low A-, B-, C- Inputs

Truth Table

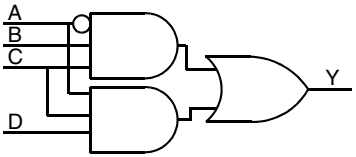
A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR

Truth Table

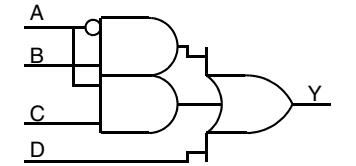
A	B	C	D	Y
X	X	0	X	0
X	0	X	0	0
0	0	X	X	0
0	1	1	X	1
1	X	1	1	1
1	X	X	0	0
X	1	1	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ALL		1

AO5A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR

Truth Table

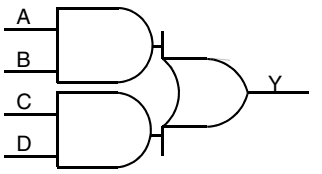
A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
0	0	X	0	0
0	1	X	X	1
1	X	1	X	1
1	X	0	0	0
X	1	1	X	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ALL		1

AO6

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C, D	Y

Function

2-wide 4-Inputs AND-OR

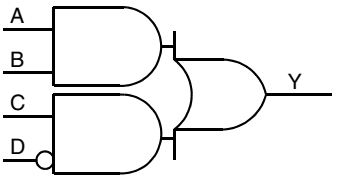
Truth Table

A	B	C	D	Y
X	0	X	0	0
X	0	0	X	0
X	X	1	1	1
0	X	X	0	0
0	X	0	X	0
1	1	X	X	1

Family	Modules	
	Seq	Comb
All listed above		1

AO6A

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C, D	Y

Function

2-wide 4-Inputs AND-OR with active low D-Input

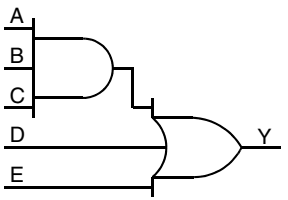
Truth Table

A	B	C	D	Y
X	0	0	X	0
X	X	1	0	1
X	0	X	1	0
0	X	0	X	0
0	X	X	1	0
1	1	X	X	1

Family	Modules	
	Seq	Comb
All listed above		1

AO7

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input AND-OR

Truth Table

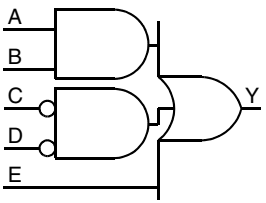
A	B	C	D	E	Y
X	X	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	0	X	0	0	0
0	X	X	0	0	0
1	1	1	X	X	1

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO8

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input AND-OR with active low C- and D-Inputs

Truth Table

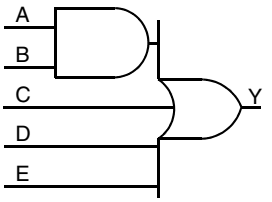
A	B	C	D	E	Y
X	X	0	0	X	1
X	0	X	1	0	0
X	X	X	X	1	1
X	0	1	X	0	0
0	X	X	1	0	0
0	X	1	X	0	0
1	1	X	X	X	1

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
All listed above		1

AO9

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input AND-OR

Truth Table

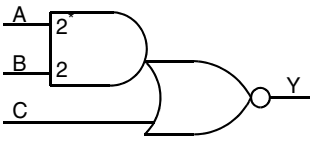
A	B	C	D	E	Y
X	0	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1
0	X	0	0	0	0
1	1	X	X	X	1

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
All listed above		1

AOI1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR-INVERT

Truth Table

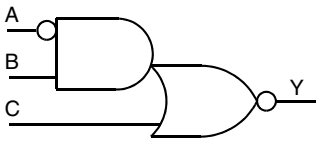
A	B	C	Y
X	0	0	1
X	X	1	0
0	X	0	1
1	1	X	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others		1

AOI1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR-INVERT with active low A-Input

Truth Table

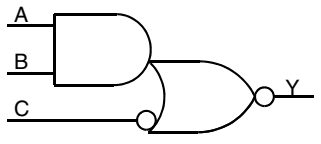
A	B	C	Y
X	0	0	1
X	X	1	0
0	1	X	0
1	X	0	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
ALL		1

AOI1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR-INVERT with active low C-Input

Truth Table

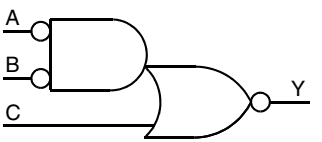
A	B	C	Y
X	X	0	0
X	0	1	1
0	X	1	1
1	1	X	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
ALL		1

AOI1C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3 Input AND-OR-INVERT with active low A- and B-Inputs

Truth Table

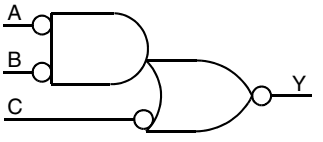
A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed above		1

AOI1D

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR-INVERT with active low Inputs

Truth Table

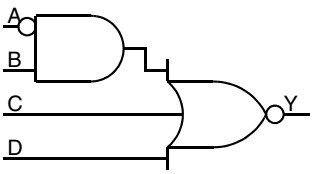
A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AOI2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR-INVERT with active low A-Input

Truth Table

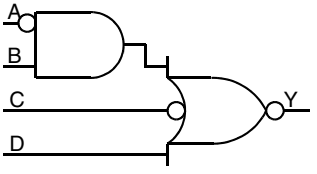
A	B	C	D	Y
X	0	0	0	1
X	X	X	1	0
X	X	1	X	0
0	1	X	X	0
1	X	0	0	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ALL		1

AOI2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR-INVERT with active low A- and C-Inputs

Truth Table

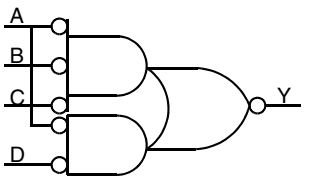
A	B	C	D	Y
X	X	0	X	0
X	0	1	0	1
X	X	X	1	0
0	1	X	X	0
1	X	1	0	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ALL		1

AOI3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input AND-OR-INVERT with active low Inputs

Truth Table

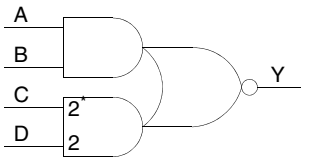
A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ALL		1

AOI4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-wide 4-Inputs AND-OR-INVERT

Truth Table

A	B	C	D	Y
X	0	X	0	1
X	0	0	X	1
X	X	1	1	0
0	X	X	0	1
0	X	0	X	1
1	1	X	X	0

Input	Output
A, B, C, D	Y

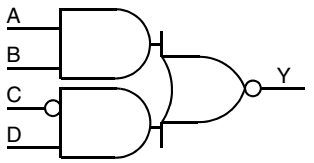
1

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays for all families except SX, SX-A, SX-S, and eX.

AOI4A

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-wide 4-Inputs AND-OR-INVERT with active low C-Input

Truth Table

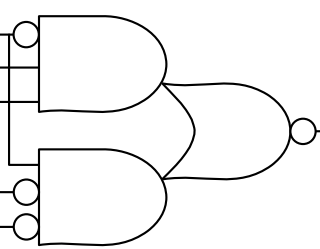
A	B	C	D	Y
X	0	X	0	1
X	X	0	1	0
X	0	1	X	1
0	X	X	0	1
0	X	1	X	1
1	1	X	X	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed		1

AOI5

SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-OR-INVERT

Truth Table

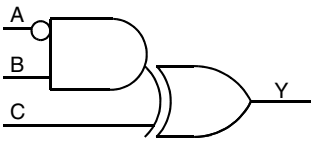
A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AX1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-XOR with active low A-Input

Truth Table

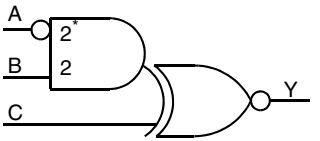
A	B	C	Y
X	0	0	0
X	0	1	1
0	1	0	1
0	1	1	0
1	X	0	0
1	X	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AX1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-XOR-INVERT with active low A-Input

Truth Table

A	B	C	Y
X	0	0	1
X	0	1	0
0	1	0	0
0	1	1	1
1	X	0	1
1	X	1	0

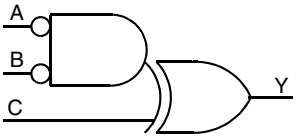
Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
ACT 1,MX,SX, SX-A, SX-S, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays for all families except ACT 1, MX, SX, SX-A, SX-S and eX.

AX1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-XOR with active low A- and B-Inputs

Truth Table

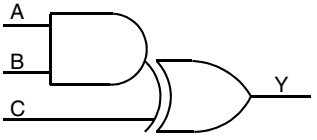
A	B	C	Y
0	0	0	1
0	0	1	0
X	1	0	0
X	1	1	1
1	X	0	0
1	X	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

AX1C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input AND-XOR

Truth Table

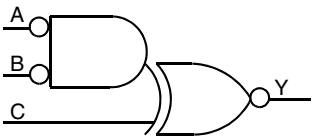
A	B	C	Y
X	0	0	0
X	0	1	1
0	X	0	0
0	X	1	1
1	1	0	1
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AX1D

SX, SX-A, SX-S, eX, Axcelerator



Function
3-Input AND-XNOR

Truth Table

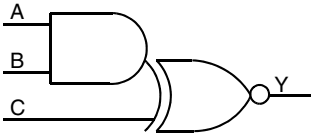
A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AX1E

SX, SX-A, SX-S, eX, Axcelerator



Function
3-Input AND-XNOR

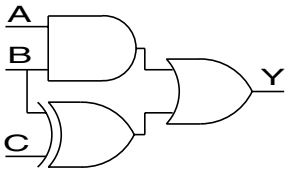
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AXO1



Function

3-Input Combinatorial Gate

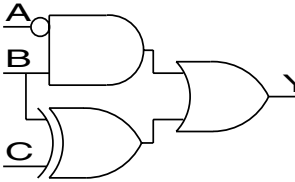
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AXO2



Function

3-Input Combinatorial Gate

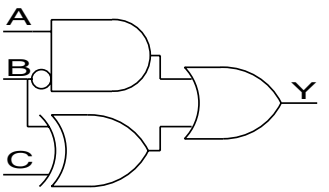
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AXO3



Input	Output
A, B, C	Y

Function

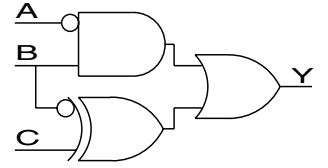
3-Input Combinatorial Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

AXO5



Input	Output
A, B, C	Y

Function

3-Input Combinatorial Gate

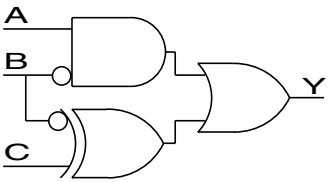
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

AXO6

SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input Combinatorial Gate

Truth Table

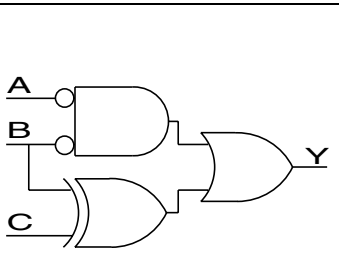
A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AXO7

SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input Combinatorial Gate

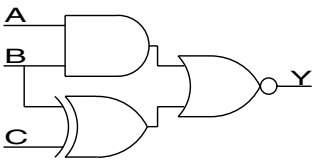
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AXOI1



Function

3-Input Combinatorial Gate

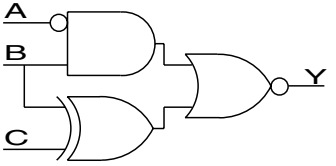
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AXOI2



Function

3-Input Combinatorial Gate

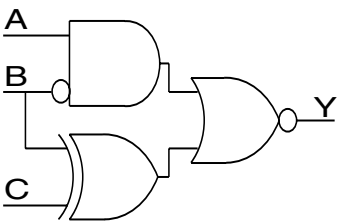
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AXOI3



Function

3-Input Combinatorial Gate

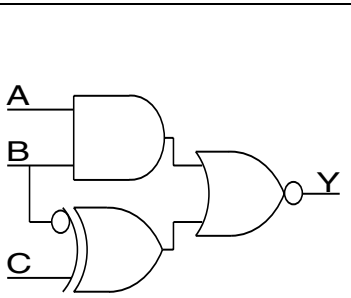
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AXOI4



Function

3-Input Combinatorial Gate

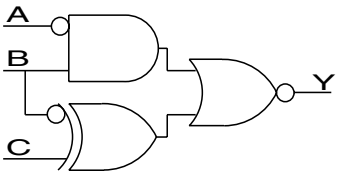
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AXOI5



Function

3-Input Combinatorial Gate

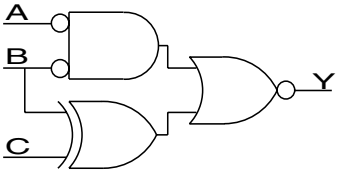
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

AXOI7



Function

3-Input Combinatorial Gate

Truth Table

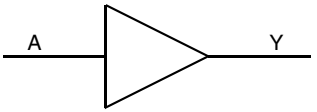
A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All listed		1

BUFA

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A	Y

Function

Buffer, with active low Input and Output

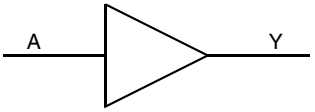
Truth Table

A	Y
0	0
1	1

Family	Modules	
	Seq	Comb
All		1

BUFF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A	Y

Function

Buffer

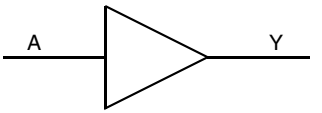
Truth Table

A	Y
0	0
1	1

Family	Modules	
	Seq	Comb
All		1

BUFD

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Buffer
NOTE: The Combiner will not remove this macro

Truth Table

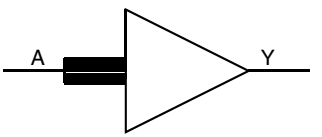
A	Y
0	0
1	1

Input	Output
A	Y

Family	Modules	
	Seq	Comb
All		1

CLKINT

ACT 2, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Internal Clock Interface

Truth Table

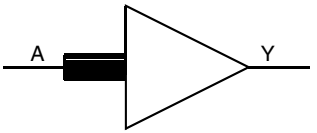
A	Y
0	0
1	1

Input	Output
A	Y

NOTE: CLKINT does not use any modules.
For more information on the Global Clock Network, refer to the latest Actel datasheet.

HCLKINT

Axcelerator



Function

Internal Clock Interface

Truth Table

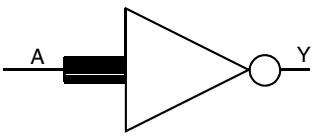
A	Y
0	0
1	1

Input	Output
A	Y

NOTE: CLKINT does not use any modules.
For more information on the Global Clock Network, refer to the latest Actel datasheet.

CLKINTI

SX, SX-A, SX-S, eX



Function

Inverting Internal Clock Interface

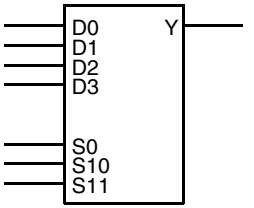
Truth Table

A	Y
0	1
1	0

Input	Output
A	Y

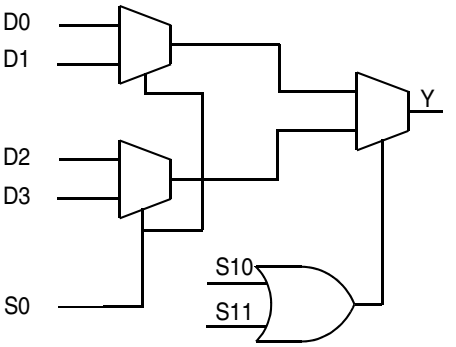
NOTE: CLKINTI does not use any modules.

For more information on the Global Clock Network, refer to Actel's Databook.



Function

Full Combinational Module

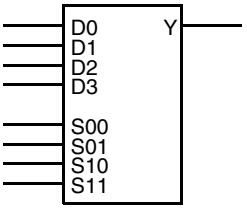


Input	Output
D0, D1, D2, D3, S0, S10, S11	y

Truth Table

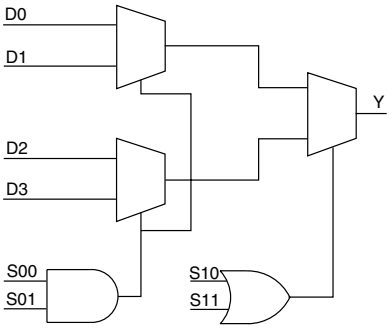
S11	S10	S0	Y
0	0	0	D0
0	0	1	D1
X	1	0	D2
1	X	0	D2
X	1	1	D3
1	X	1	D3

Family	Modules	
	Seq	Comb
All listed		1



Function

Full Combinational Module



Input	Output
D0, D1, D2, D3, S00, S01, S10, S11	y

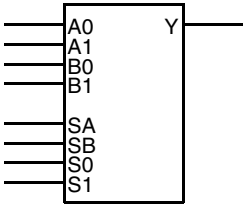
Truth Table

S11	S10	S01	S00	Y
0	0	X	0	D0
0	0	0	X	D0
0	0	1	1	D1
X	1	X	0	D2
X	1	0	X	D2
1	X	X	0	D2
1	X	0	X	D2
X	1	1	1	D3
1	X	1	1	D3

Family	Modules	
	Seq	Comb
All listed		1

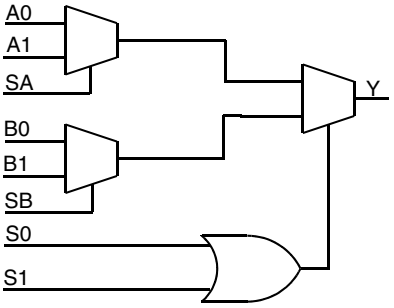
CM8A

ACT 1, MX



Function

Full Combinational Module

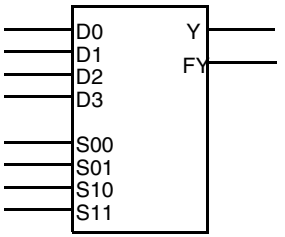


Input	Output
A0, A1, B0, B1, SA, SB, S0, S1	Y

Truth Table

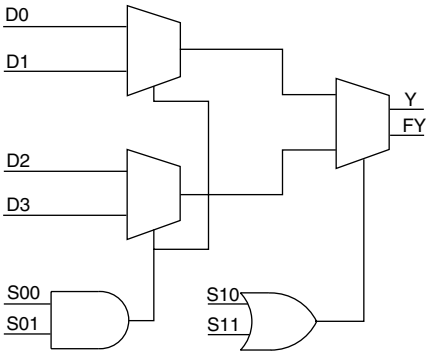
S0	S1	SA	SB	Y
0	0	0	X	A0
0	0	1	X	A1
1	X	X	0	B0
X	1	X	0	B0
1	X	X	1	B1
X	1	X	1	B1

Family	Modules	
	Seq	Comb
ACT 1, MX		1



Function

Full Combinational Module with fast output



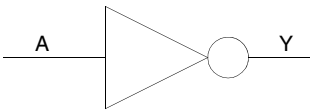
Input	Output
D0, D1, D2, D3, S00, S01, S10, S11	Y, FY

Truth Table

S11	S10	S01	S00	Y	FY
0	0	X	0	D0	D0
0	0	0	X	D0	D0
0	0	1	1	D1	D1
X	1	X	0	D2	D2
X	1	0	X	D2	D2
1	X	X	0	D2	D2
1	X	0	X	D2	D2
X	1	1	1	D3	D3
1	X	1	1	D3	D3

Family	Modules	
	Seq	Comb
All listed		1

CM8INV



Function

Inverter with active low output

Truth Table

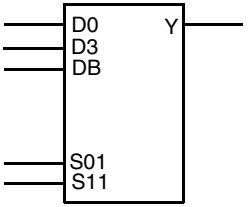
A	Y
0	1
1	0

Input	Output
A	Y

Family	Modules	
	Seq	Comb
All listed		0

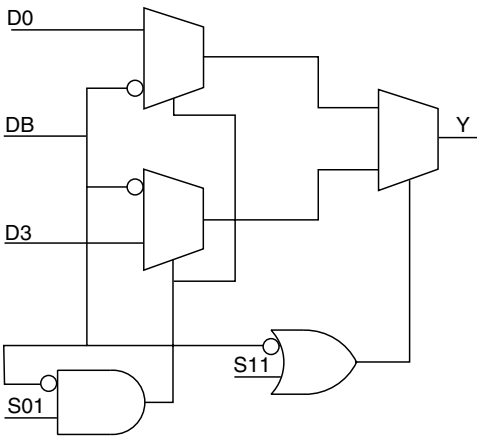
NOTE: This macro can drive any number of CM8 pins and will be absorbed into that module.

CMA9



Function

Full Combinational Module

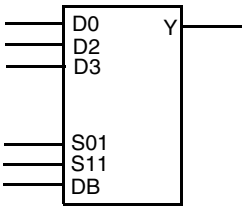


Input	Output
D0, D3. DB, S01, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

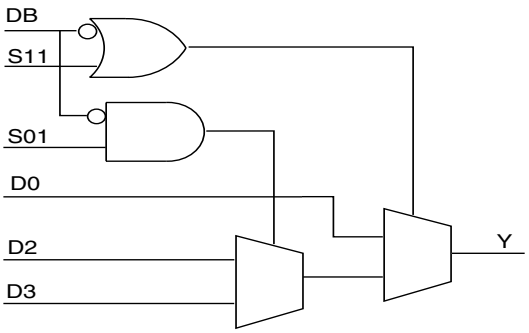
CMAF

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

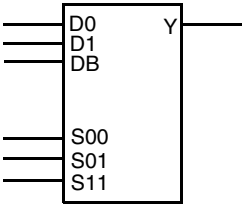


Input	Output
D0, D2, D3, DB, S01, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

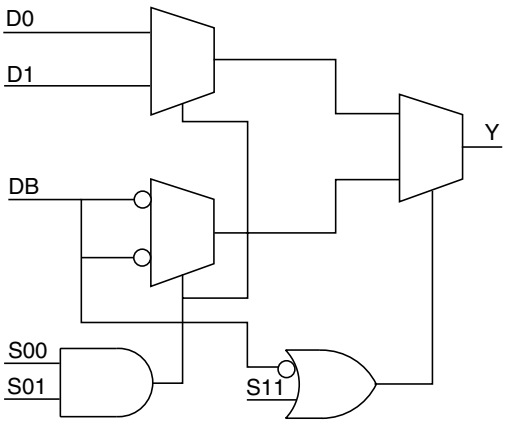
CMB3

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

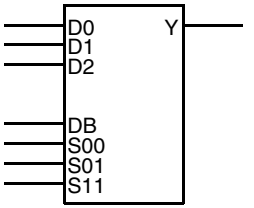


Input	Output
D0, D1, DB, S00, S01, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

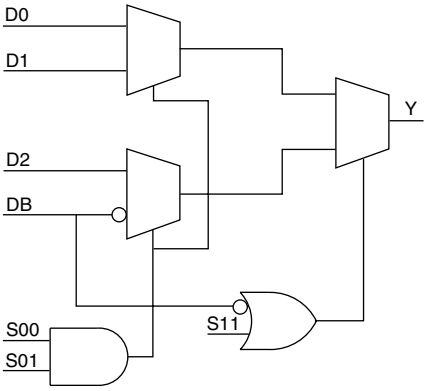
CMB7

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

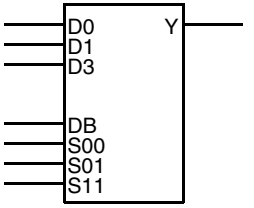


Input	Output
D0, D1, D2, DB, S00, S01, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

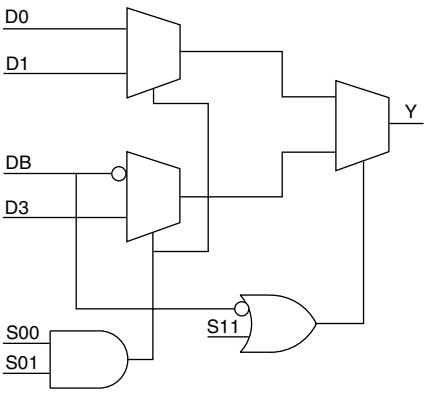
CMBB

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

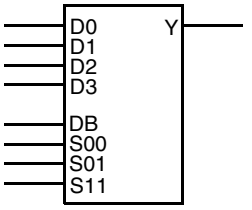


Input	Output
D0, D1, D3, DB, S00, S01, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

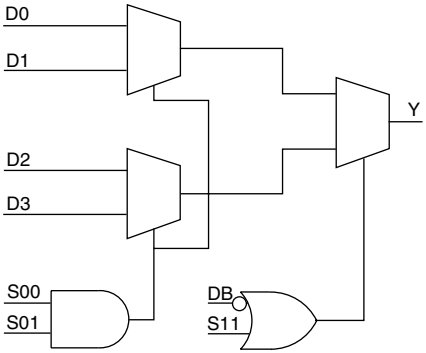
CMBF

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

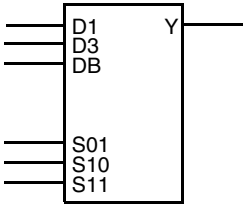


Input	Output
D0, D1, D2, D3, DB, S00, S01, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

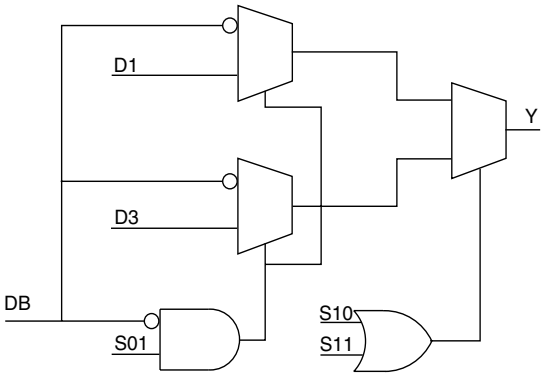
CMEA

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

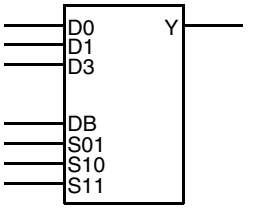


Input	Output
D1, D3, DB, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

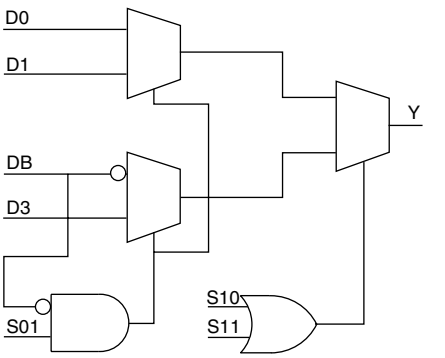
CMEB

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

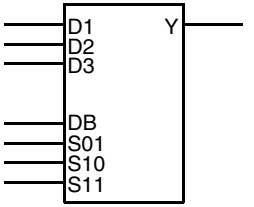


Input	Output
D0, D1, D3, DB, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

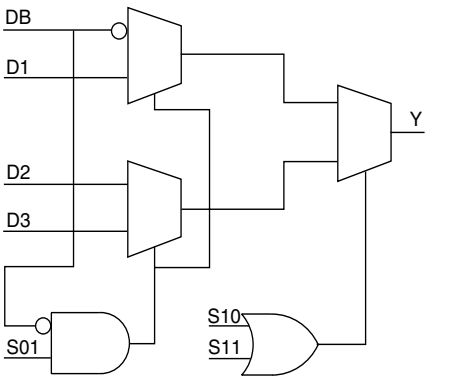
CMEE

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

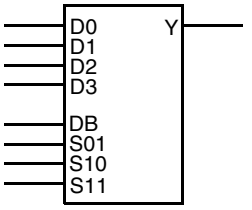


Input	Output
D1, D2, D3, DB, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

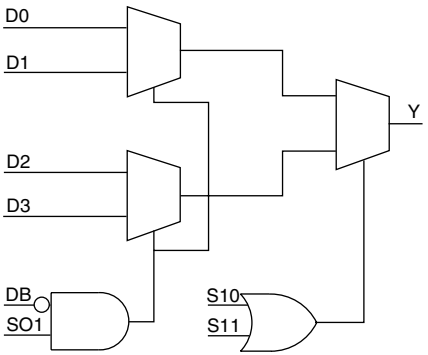
CMEF

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

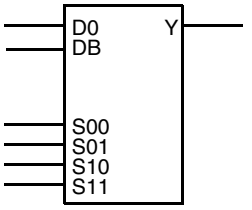


Input	Output
D0, D1, D2, D3, DB, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

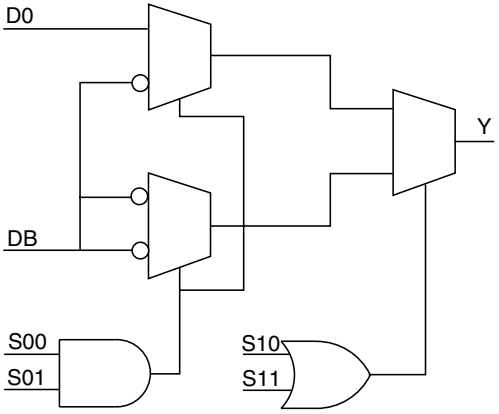
CMF1

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

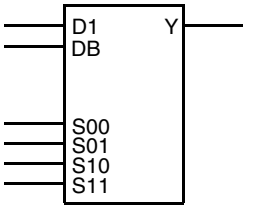


Input	Output
D0, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

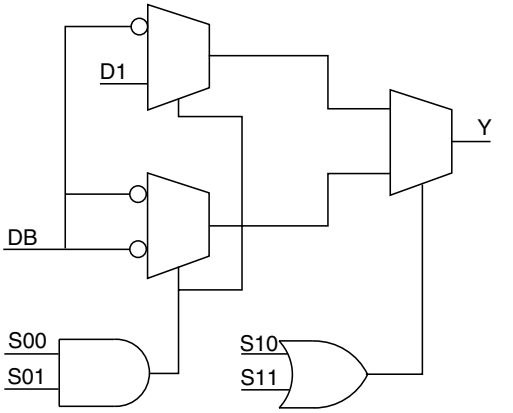
CMF2

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

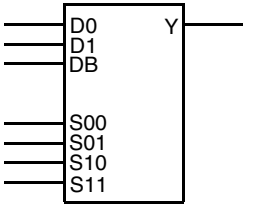


Input	Output
D1, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

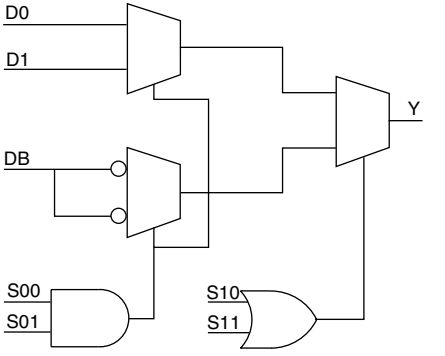
CMF3

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

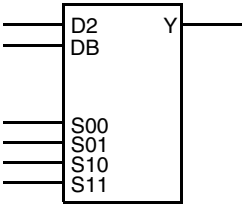


Input	Output
D0, D1, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

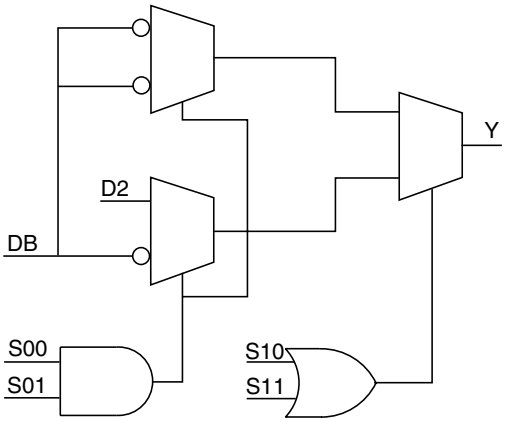
CMF4

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

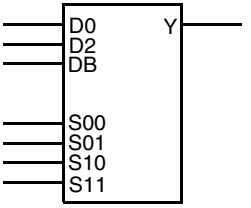


Input	Output
D2, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

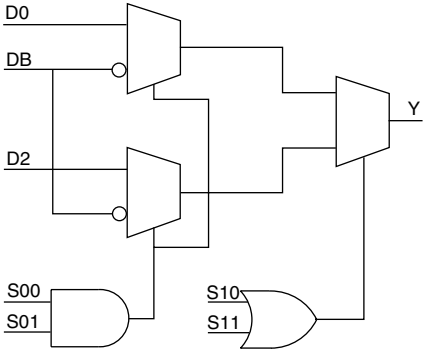
CMF5

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

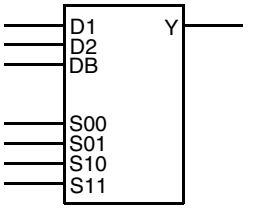


Input	Output
D0, D2, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

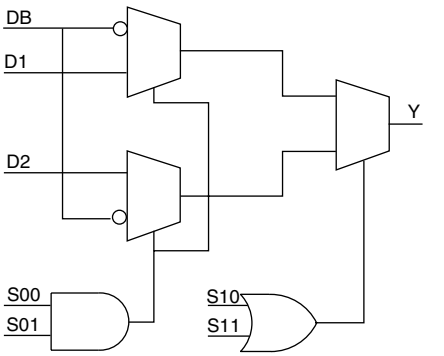
CMF6

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

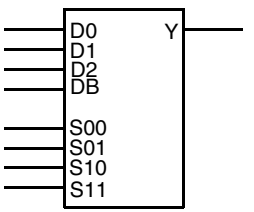


Input	Output
D1, D2, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

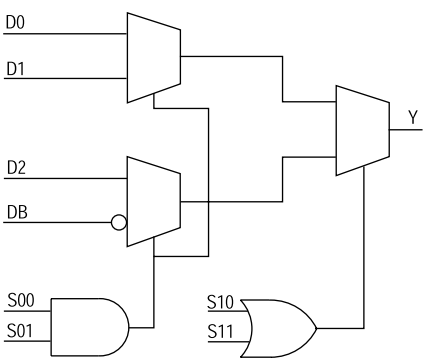
CMF7

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

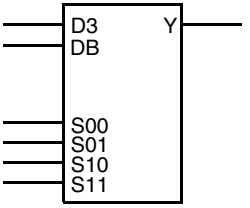


Input	Output
D0, D1, D2, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

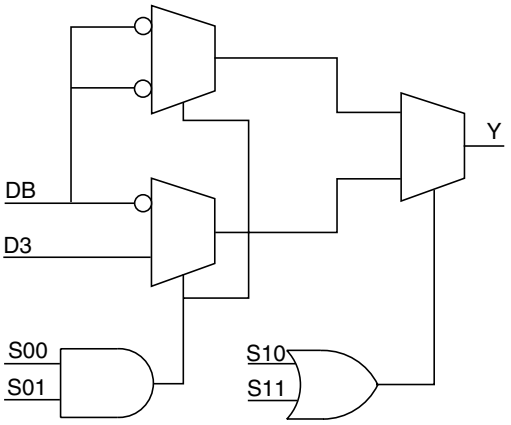
CMF8

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

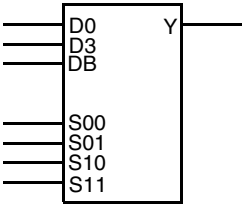


Input	Output
D3, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

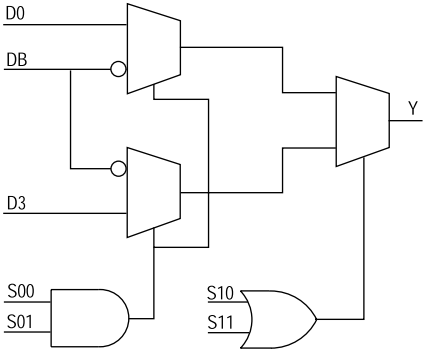
CMF9

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

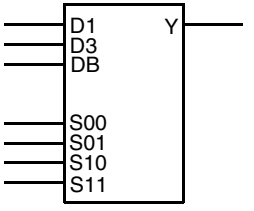


Input	Output
D0, D3, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

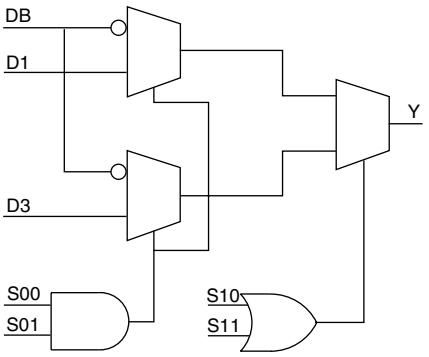
CMFA

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

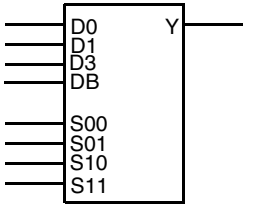


Input	Output
D1, D3, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

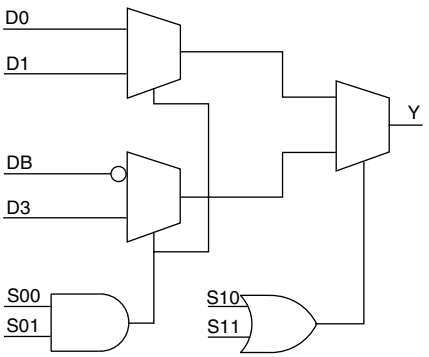
CMFB

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

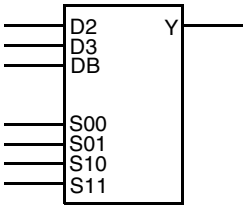


Input	Output
D0, D1, D3, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

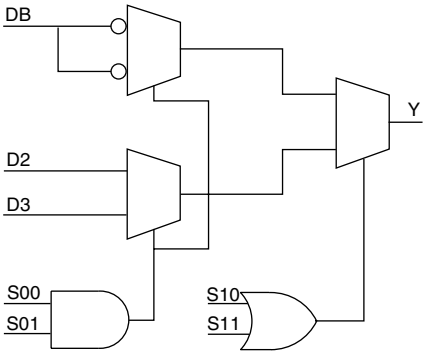
CMFC

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

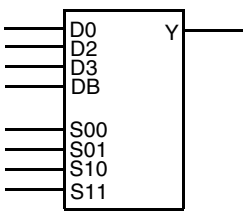


Input	Output
D2, D3, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

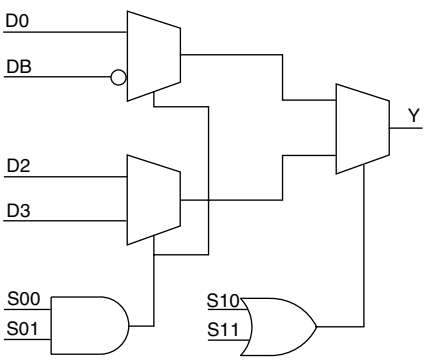
CMFD

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

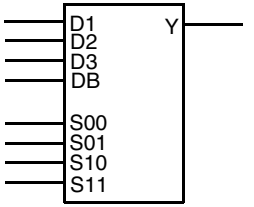


Input	Output
D0, DB, D2, D3, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

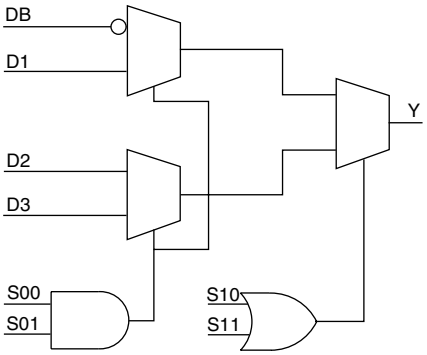
CMFE

SX, SX-A, SX-S, eX, Axcelerator



Function

Full Combinational Module

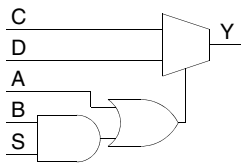


Input	Output
D1, D2, D3, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
All listed		1

CS1

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Carry Select for Implementing High Speed Adders

Truth Table

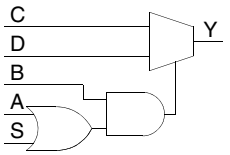
A	S	B	C	D	Y
X	X	X	0	0	0
0	X	0	0	X	0
0	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	X	X	1	1
1	X	X	X	0	0
X	X	X	1	1	1

Input	Output
A, S, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed		1

CS2

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, S, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed		1

Function

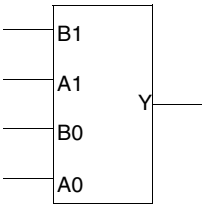
Carry Select for Implementing High Speed Adders

Truth Table

A	S	B	C	D	Y
X	X	X	0	0	0
X	X	0	0	X	0
X	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	1	X	1	1
1	X	1	X	0	0
X	X	X	1	1	1

CY2A

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A1, B1, A0, B0	Y

Family	Modules	
	Seq	Comb
All listed		1

Function

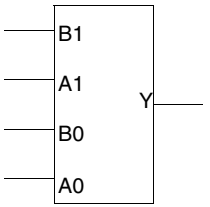
Carry Generator

Truth Table

A1	B1	A0	B0	Y
X	0	X	0	0
X	0	0	X	0
0	0	X	X	0
0	X	X	0	0
0	X	0	X	0
X	1	1	1	1
1	X	1	1	1
1	1	X	X	1

CY2B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Carry Generator

Truth Table

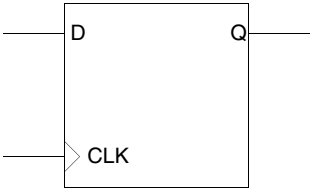
A1	B1	A0	B0	Y
X	0	0	0	0
0	0	X	X	0
0	X	0	0	0
X	1	X	1	1
X	1	1	X	1
1	X	X	1	1
1	X	1	X	1
1	1	X	X	1

Input	Output
A1, B1, A0, B0	Y

Family	Modules	
	Seq	Comb
All listed		1

DF1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop

Truth Table

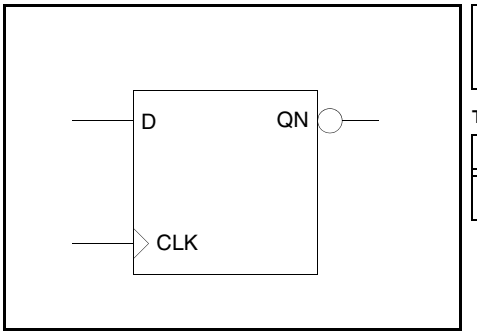
CLK	Q_{n+1}
↑	D

Input	Output
D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

DF1A

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active low Output

Truth Table

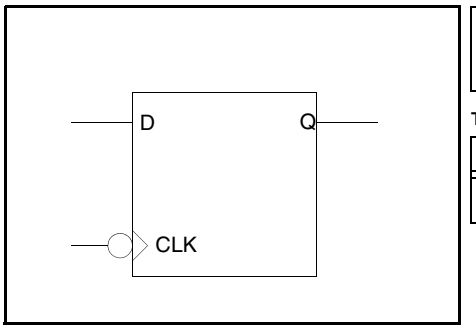
CLK	QN_{n+1}
↑	!D

Input	Output
D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DF1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Clock

Truth Table

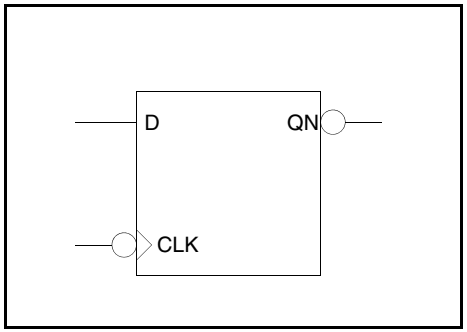
CLK	Q_{n+1}
↓	D

Input	Output
D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DF1C

ACT 1, MX,ACT2/1200XL, ACT3, 3200DX, MX



Function

D-Type Flip-Flop with active low Clock and Output

Truth Table

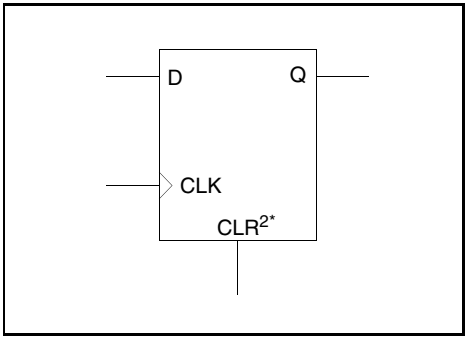
CLK	QN_{n+1}
↓	!D

Input	Output
D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFC1

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active high Clear

Truth Table

CLR	CLK	Q_{n+1}
1	X	0
0	↑	D

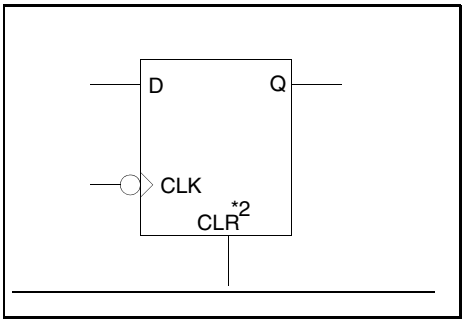
Input	Output
CLR, D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and MX.

DFC1A

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active high Clear and active low Clock

Truth Table

CLR	CLK	Q_{n+1}
1	X	0
0	↓	D

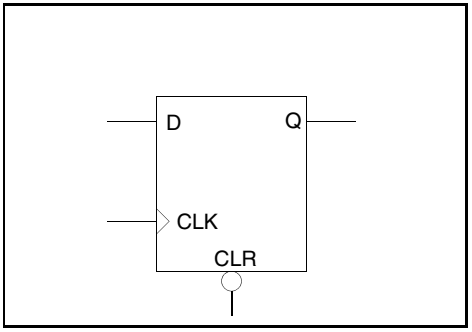
Input	Output
CLR, D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and MX.

DFC1B

ACT 1, ACT 2, ACT 3, 3200DX, MX SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Clear

Truth Table

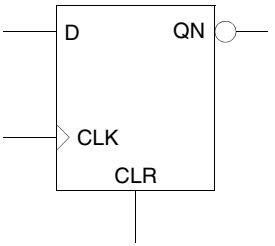
CLR	CLK	Q_{n+1}
0	X	0
1	↑	D

Input	Output
CLR, D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

DFC1C

ACT 1, MX



Function

D-Type Flip-Flop with active high Clear and Clock

Truth Table

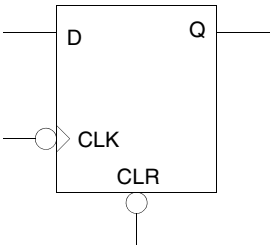
CLR	CLK	QN_{n+1}
1	X	1
0	↑	!D

Input	Output
CLR, D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1; MX		2

DFC1D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Clear and Clock

Truth Table

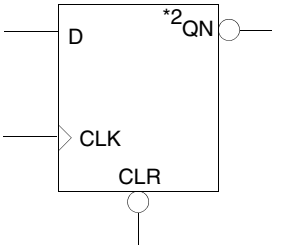
CLR	CLK	Q_{n+1}
0	X	0
1	↓	D

Input	Output
CLR, D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

DFC1E

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active low Clear and Output

Truth Table

CLR	CLK	QN_{n+1}
0	X	1
1	↑	!D

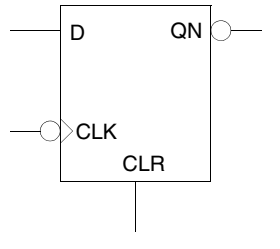
Input	Output
CLR, D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT1 and MX.

DFC1F

ACT 1, MX



Function

D-Type Flip-Flop with active high Clear, active low Clock and Output

Truth Table

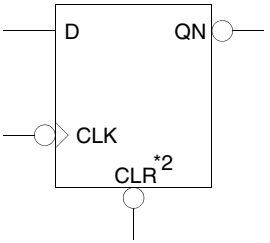
CLR	CLK	QN_{n+1}
1	X	1
0	↓	!D

Input	Output
CLR, D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1, MX		2

DFC1G

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active low Clear, Clock and Output

Truth Table

CLR	CLK	Q_{n+1}
0	X	1
1	↓	!D

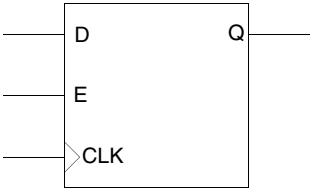
Input	Output
CLR, D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT1 and MX.

DFE

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active high Enable

Truth Table

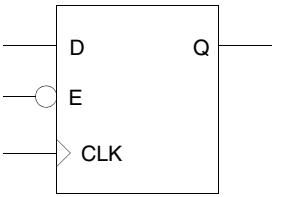
E	CLK	Q_{n+1}
0	X	Q
1	↑	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

DFE1B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Enable

Truth Table

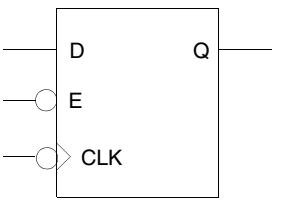
E	CLK	Q_{n+1}
1	X	Q
0	↑	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

DFE1C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Enable and Clock

Truth Table

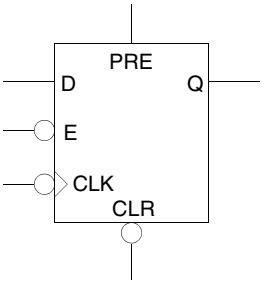
E	CLK	Q_{n+1}
1	X	Q
0	↓	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

DFE2D

ACT 1, MX



Function

D-Type Flip-Flop with active high Preset, active low Enable, Clear, and Clock

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↓	D
0	1	X	X	*

Input
CLR, D, E, PRE, CLK

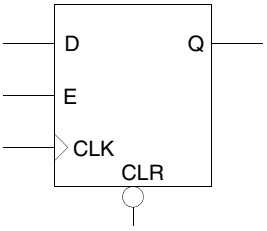
Output
Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFE3A

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop, with Enable and active low Clear

Truth Table

CLR	E	CLK	Q_{n+1}
0	X	X	0
1	0	X	Q
1	1	↑	D

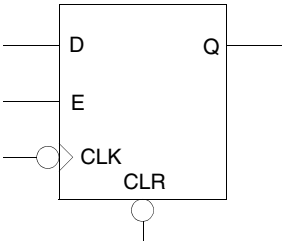
Input
CLR, D, E, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

DFE3B

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with Enable and active low Clear and Clock

Truth Table

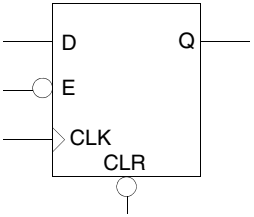
CLR	E	CLK	Q_{n+1}
0	X	X	0
1	0	X	Q
1	1	↓	D

Input	Output
CLR, D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFE3C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with Active Low Enable and Clear

Truth Table

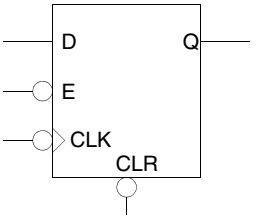
CLR	E	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	D

Input	Output
CLR, D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

DFE3D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Enable, Clear and Clock

Truth Table

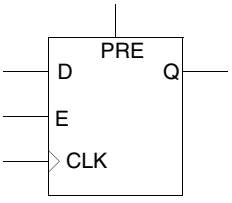
CLR	E	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↓	D

Input	Output
CLR, D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFE4

ACT 1, MX



Function

D-Type Flip-Flop with active high Enable and Preset

Truth Table

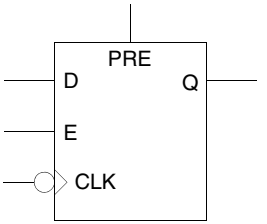
PRE	E	CLK	Q_{n+1}
1	X	X	1
0	0	X	Q
0	1	↑	D

Input	Output
D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

DFE4A

ACT 1, MX



Function

D-Type Flip-Flop with active high Enable and Preset, and active low Clock

Truth Table

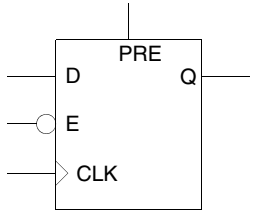
PRE	E	CLK	Q_{n+1}
1	X	X	1
0	0	X	Q
0	1	↓	D

Input	Output
D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

DFE4B

ACT 1, MX



Function

D-Type Flip-Flop with active low Enable, and active high Preset

Truth Table

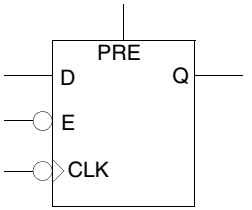
PRE	E	CLK	Q_{n+1}
1	X	X	1
0	1	X	Q
0	0	↑	D

Input	Output
D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

DFE4C

ACT 1, MX



Function

D-Type Flip-Flop with active low Enable and Clock, and active high Preset

Truth Table

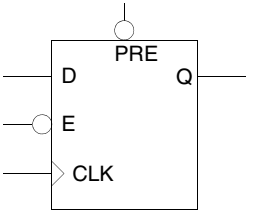
PRE	E	CLK	Q_{n+1}
1	X	X	1
0	1	X	Q
0	0	↓	D

Input	Output
D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

DFE4F

SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Enable and Preset

Truth Table

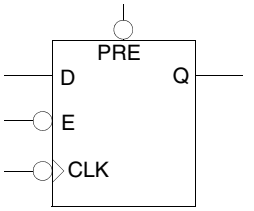
PRE	E	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	D

Input	Output
D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFE4G

SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Enable, Clock, and Preset

Truth Table

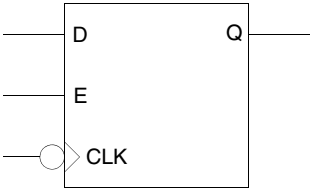
PRE	E	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↓	D

Input	Output
D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFEA

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop, with Enable, and active low Clock

Truth Table

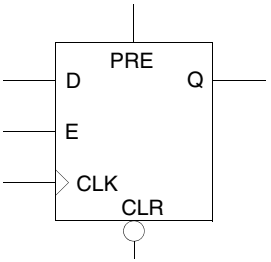
E	CLK	Q_{n+1}
0	X	Q
1	↓	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

DFEB

ACT 1, MX



Function

D-Type Flip-Flop with Enable, Preset, and active low Clear

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↑	D
0	1	X	X	*

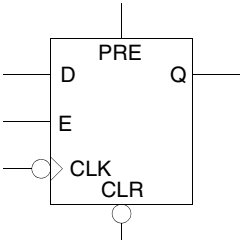
Input	Output
CLR, D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

*Your design should not allow both PRE and CLR to be asserted at the same time.

DFEC

ACT 1, MX



Function

D-Type Flip-Flop with Enable, Preset, and active low Clear and Clock

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↓	D
0	1	X	X	*

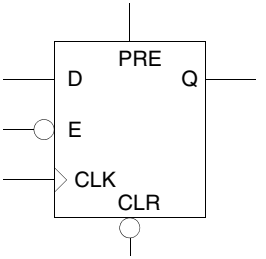
Input	Output
CLR, D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFED

ACT 1, MX



Function

D-Type Flip-Flop with active low Enable and Clear, and active high Preset

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↑	D
0	1	X	X	*

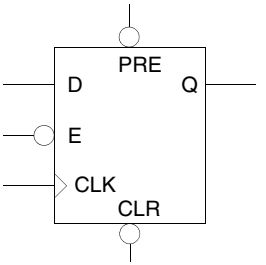
Input	Output
CLR, D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFEG

SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Enable, Preset, and Clear

Truth Table

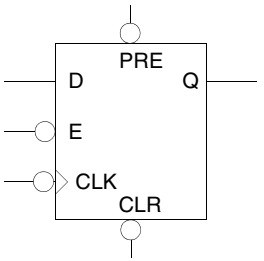
CLR	PRE	E	CLK	Q_{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	1	X	Q
1	1	0	↑	D

Input	Output
CLR, D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFEH

SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Enable, Clear, Preset, and Clock

Truth Table

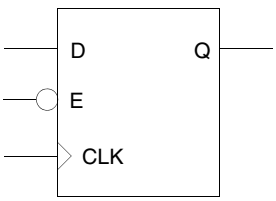
CLR	PRE	E	CLK	Q_{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	1	X	Q
1	1	0	↓	D

Input	Output
CLR, D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
All listed	1	

IODFE

ACT 3



Function

D-Type Flip-Flop with active low Enable

Truth Table

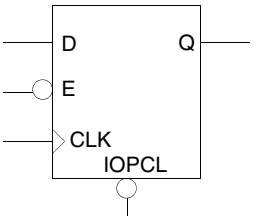
E	CLK	Q_{n+1}
1	X	Q
0	↑	D

Input	Output
D, E, CLK	Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
WARNING: Using the IODFE macro will disable the IOPCLBUF clock network.
NOTE 2: Uses an I/O module.

IODFEC

ACT 3



Function

D-Type Flip-Flop with active low Enable and Clear

Truth Table

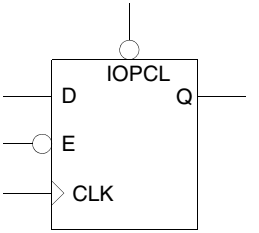
IOPCL	E	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	D

Input	Output
IOPCL, D, E, CLK	Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
NOTE 2: Uses an I/O module.
NOTE 3: The IOPCL pin must be driven by the IOPCLBUF macro.

IODFEP

ACT 3



Function

D-Type Flip-Flop with active low Enable and Preset

Truth Table

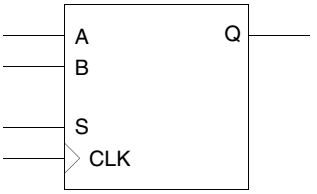
IOPCL	E	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	D

Input	Output
IOPCL, D, E, CLK	Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
NOTE 2: The IOPCL pin must be driven by the IOPCLBUF macro.
NOTE 3: Uses an I/O module.

DFM

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX, Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data

Truth Table

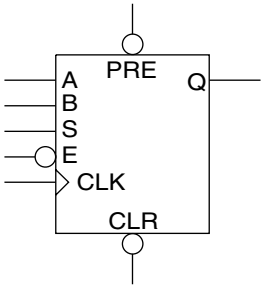
S	CLK	Q_{n+1}
0	↑	A
1	↑	B

Input	Output
A, B, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFMEG

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Enable, Preset, and Clear

Truth Table

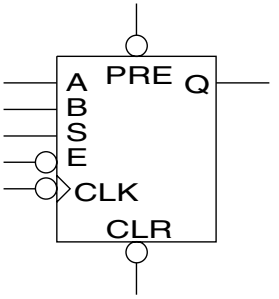
CLR	PRE	E	S	CLK	Q_{n+1}
0	X	X	X	X	0
1	0	X	X	X	1
1	1	1	X	X	Q
1	1	0	0	↑	A
1	1	0	1	↑	B

Input	Output
CLK, A, B, S, E, PRE, CLR	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFMEH

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable, Preset, and Clear

Truth Table

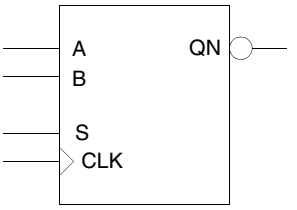
CLR	PRE	E	S	CLK	Q_{n+1}
0	X	X	X	X	0
1	0	X	X	X	1
1	1	1	X	X	Q
1	1	0	0	↓	A
1	1	0	1	↓	B

Input	Output
CLK, A, B, S, E, PRE, CLR	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFM1B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

Truth Table

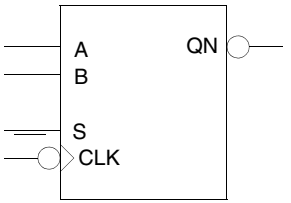
S	CLK	QN_{n+1}
0	↑	!A
1	↑	!B

Input	Output
A, B, S, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFM1C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock and Output

Truth Table

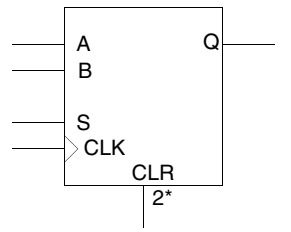
S	CLK	QN_{n+1}
0	↓	!A
1	↓	!B

Input	Output
A, B, S, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFM3

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active high Clear

Truth Table

CLR	S	CLK	Q_{n+1}
1	x	x	0
0	1	↑	B
0	0	↑	A

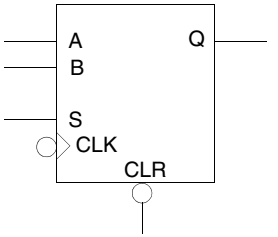
Input	Output
A, B, CLR, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT 1 and MX.

DFM3B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX, Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear and Clock

Truth Table

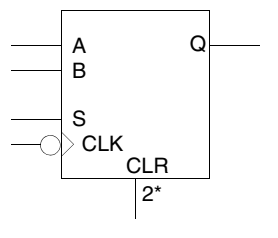
CLR	S	CLK	Q_{n+1}
0	X	X	0
1	0	↓	A
1	1	↓	B

Input	Output
A, B, CLR, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFM3E

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock

Truth Table

CLR	S	CLK	Q_{n+1}
1	X	X	0
0	0	↓	A
0	1	↓	B

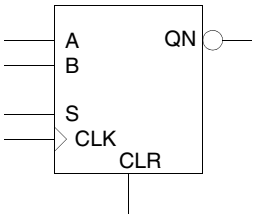
Input	Output
A, B, CLR, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT 1 and MX.

DFM3F

ACT 1, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Output

Truth Table

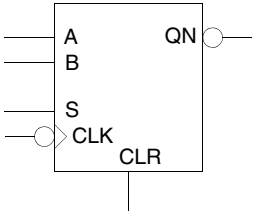
CLR	S	CLK	QN_{n+1}
1	X	X	1
0	0	↑	!A
0	1	↑	!B

Input	Output
A, B, CLR, S, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2

DFM3G

ACT 1, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock and Output

Truth Table

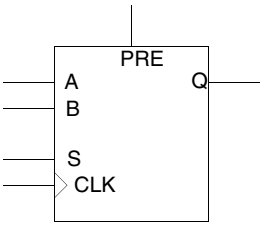
CLR	S	CLK	QN_{n+1}
1	X	X	1
0	0	↓	!A
0	1	↓	!B

Input	Output
A, B, CLR, S, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2

DFM4

ACT 1, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active high Preset

Truth Table

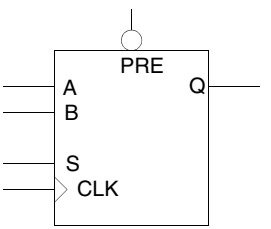
PRE	S	CLK	Q_{n+1}
1	X	X	1
0	0	↑	A
0	1	↑	B

Input	Output
A, B, PRE, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

DFM4A

ACT 1, MX, Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset

Truth Table

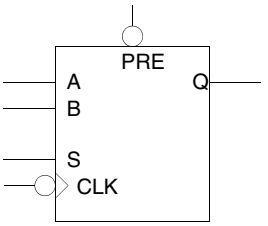
PRE	S	CLK	Q_{n+1}
0	X	X	1
1	0	↑	A
1	1	↑	B

Input	Output
A, B, PRE, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

DFM4B

ACT 1, MX, Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Clock

Truth Table

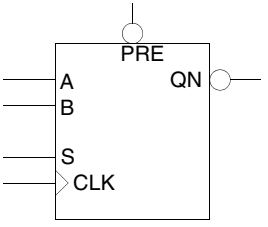
PRE	S	CLK	Q_{n+1}
0	X	X	1
1	0	↓	A
1	1	↓	B

Input	Output
A, B, PRE, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

DFM4C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Output

Truth Table

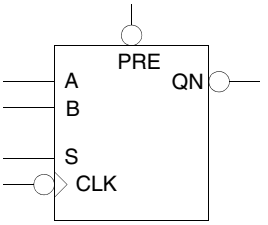
PRE	S	CLK	QN_{n+1}
0	X	X	0
1	0	↑	!A
1	1	↑	!B

Input	Output
A, B, PRE, S, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFM4D

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset, Clock and Output

Truth Table

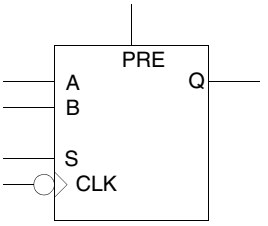
PRE	S	CLK	QN_{n+1}
0	X	X	0
1	0	↓	!A
1	1	↓	!B

Input	Output
A, B, PRE, S, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFM4E

ACT 1, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clock

Truth Table

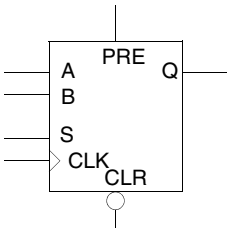
PRE	S	CLK	Q_{n+1}
1	X	X	1
0	0	↓	A
0	1	↓	B

Input	Output
A, B, PRE, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

DFM5A

ACT 1, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear

Truth Table

CLR	PRE	S	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	↑	A
1	0	1	↑	B
0	1	X	X	*

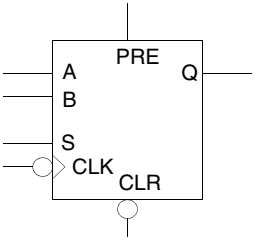
Input	Output
A, B, CLR, PRE, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFM5B

ACT 1, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear and Clock

Truth Table

CLR	PRE	S	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	↓	A
1	0	1	↓	B
0	1	X	X	*

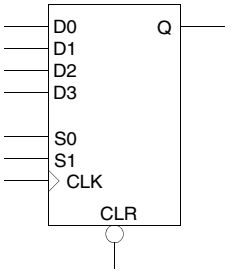
Input	Output
A, B, CLR, PRE, S, CLK	Q

Family	Modules	
	Seq	Comb
All listed		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFM6A

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table

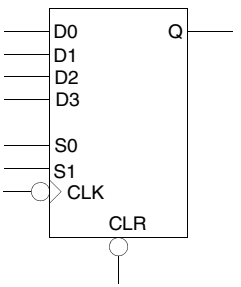
CLR	S1	S0	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	↑	D0
1	0	1	↑	D1
1	1	0	↑	D2
1	1	1	↑	D3

Input	Output
D0, D1, D2, D3, S0, S1, CLK, CLR	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFM6B

ACT 2, ACT 3, 3200DX, MX



Function

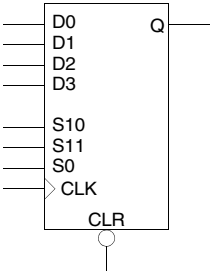
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and Clock

Truth Table

CLR	S1	S0	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	↓	D0
1	0	1	↓	D1
1	1	0	↓	D2
1	1	1	↓	D3

Input	Output
D0, D,1 D2, D3 S0, S1, CLK, CLR	Q

Family	Modules	
	Seq	Comb
All listed	1	



Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table

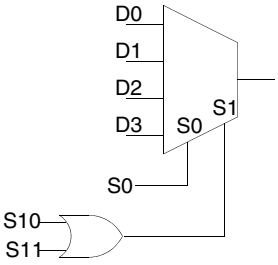
CLR	S11	S10	S0	CLK	Q_{n+1}
0	X	X	X	X	0
1	0	0	0	↑	D0
1	0	0	1	↑	D1
1	1	X	0	↑	D2
1	X	1	0	↑	D2
1	1	X	1	↑	D3
1	X	1	1	↑	D3

Input	Output
D0, D1, D2, D3, S0, S10, S11, CLK, CLR	Q

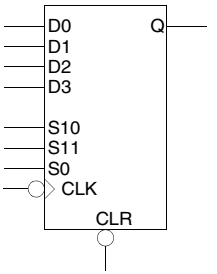
Family	Modules	
	Seq	Comb
All listed	1	

NOTE 1: The DFM7A macro represents the full ACT 2, 3200DX and MX S-module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DFM7B



Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

Truth Table

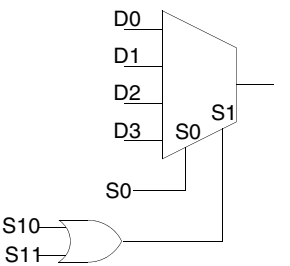
CLR	S11	S10	S0	CLK	Q_{n+1}
0	X	X	X	X	0
1	0	0	0	↓	D0
1	0	0	1	↓	D1
1	1	X	0	↓	D2
1	X	1	0	↓	D2
1	1	X	1	↓	D3
1	X	1	1	↓	D3

Input	Output
D0, D1, D2, D3, S0, S10, S11, CLK, CLR	Q

Family	Modules	
	Seq	Comb
All listed	1	

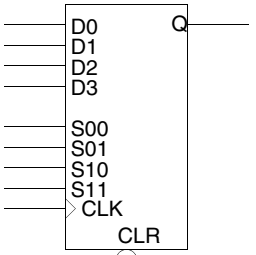
NOTE 1: The DFM7B macro represents the full ACT 2, 3200DX and MX S-module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DFM8A

ACT 3



Input	Output
D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR	Q

Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

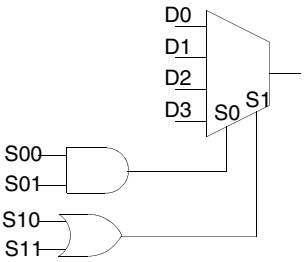
Truth Table

CLR	S11	S10	S01	S00	CLK	Q_{n+1}
0	X	X	X	X	X	0
1	0	0	0	X	↑	D0
1	0	0	X	0	↑	D0
1	0	0	1	1	↑	D1
1	1	X	0	X	↑	D2
1	X	1	0	X	↑	D2
1	1	X	X	0	↑	D2
1	X	1	X	0	↑	D2
1	1	X	1	1	↑	D3
1	X	1	1	1	↑	D3

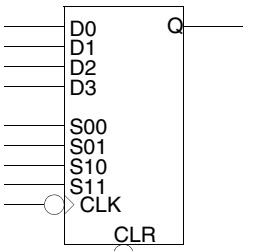
Family	Modules	
	Seq	Comb
ACT3	1	

NOTE 1: The DFM8A macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DFM8B



Input	Output
D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR	Q

Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

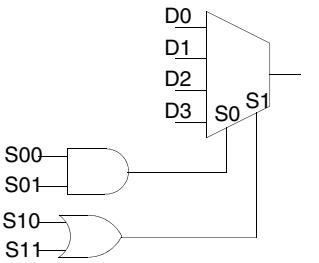
Truth Table

CLR	S11	S10	S01	S00	CLK	Q_{n+1}
0	X	X	X	X	X	0
1	0	0	0	X	↓	D0
1	0	0	X	0	↓	D0
1	0	0	1	1	↓	D1
1	1	X	0	X	↓	D2
1	X	1	0	X	↓	D2
1	1	X	X	0	↓	D2
1	X	1	X	0	↓	D2
1	1	X	1	1	↓	D3
1	X	1	1	1	↓	D3

Family	Modules	
	Seq	Comb
ACT3	1	

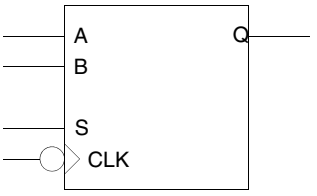
NOTE 1: The DFM8B macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DFMA

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

Truth Table

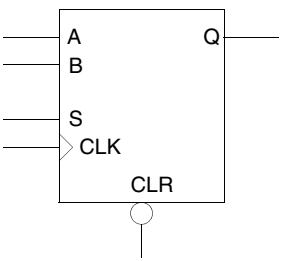
S	CLK	Q_{n+1}
0	↓	A
1	↓	B

Input	Output
A, B, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFMB

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear

Truth Table

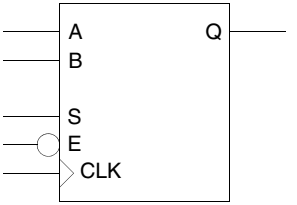
CLR	S	CLK	Q_{n+1}
0	X	X	0
1	0	↑	A
1	1	↑	B

Input	Output
A, B, CLR, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFME1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

2-bit D-Type Flip-Flop with Multiplexed Data, and active low Enable

Truth Table

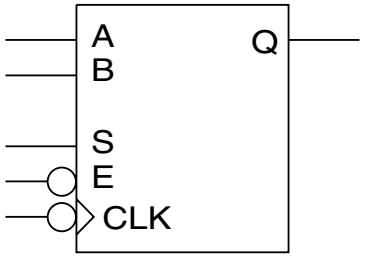
E	S	CLK	Q_{n+1}
1	X	X	Q
0	0	↑	A
0	1	↑	B

Input	Output
A, B, S, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFME1B

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable

Truth Table

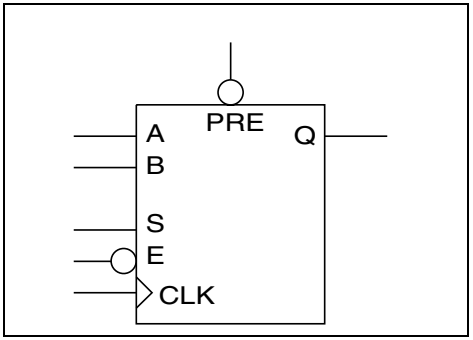
E	S	CLK	Q_{n+1}
1	X	X	Q
0	0	↓	A
0	1	↓	B

Input	Output
CLK, A, B, S, E,	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFME2A

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Enable and Preset

Truth Table

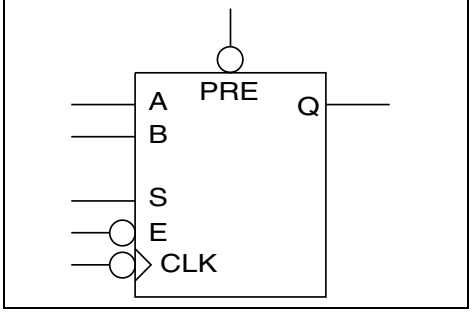
PRE	E	S	CLK	Q_{n+1}
0	X	X	X	1
1	1	X	X	Q
1	0	0	↑	A
1	0	1	↑	B

Input	Output
CLK, A, B, S, E, PRE	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFME2B

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable and Preset

Truth Table

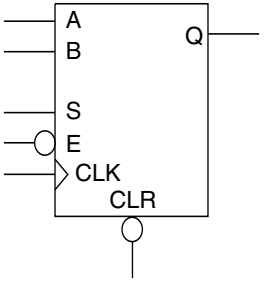
PRE	E	S	CLK	Q_{n+1}
0	X	X	X	1
1	1	X	X	Q
1	0	0	↓	A
1	0	1	↓	B

Input	Output
CLK, A, B, S, E, PRE	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFME3A

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Enable and Clear

Truth Table

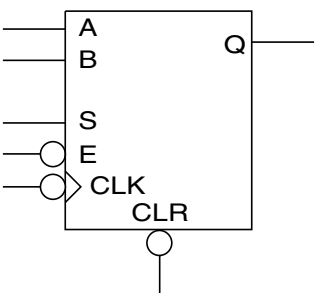
CLR	E	S	CLK	Q_{n+1}
0	X	X	X	0
1	1	X	X	Q
1	0	0	↑	A
1	0	1	↑	B

Input	Output
CLK, A, B, S, E, CLR	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFME3B

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable and Clear

Truth Table

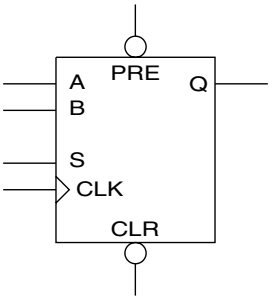
CLR	E	S	CLK	Q_{n+1}
0	X	X	X	0
1	1	X	X	Q
1	0	0	↓	A
1	0	1	↓	B

Input	Output
CLK, A, B, S, E, CLR	Q

Family	Modules	
	Seq	Comb
All listed	1	

DFMPCA

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Preset and Clear

Input
CLK, A, B, S, E, PRE, CLR

Output
Q

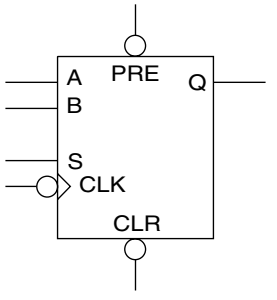
Truth Table

CLR	PRE	S	CLK	Q_{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	0	↑	A
1	1	1	↑	B

Family	Modules	
	Seq	Comb
All listed	1	

DFMPCB

Axcelerator



Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Preset and Clear

Input
CLK, A, B, S, E, PRE, CLR

Output
Q

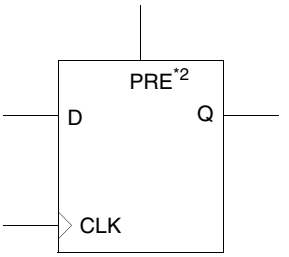
Truth Table

CLR	PRE	S	CLK	Q_{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	0	↓	A
1	1	1	↓	B

Family	Modules	
	Seq	Comb
All listed	1	

DFP1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active high Preset

Truth Table

PRE	CLK	Q_{n+1}
1	X	1
0	↑	D

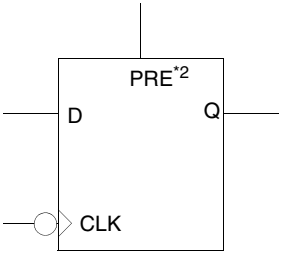
Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX, Axcelerator	1	1
Others		2

* A 2 on the symbol implies 2 logic module delays only for SX, SX-A, SX-S, eX, and Axcelerator.

DFP1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active high Preset, and active low Clock

Truth Table

PRE	CLK	Q_{n+1}
1	X	1
0	↓	D

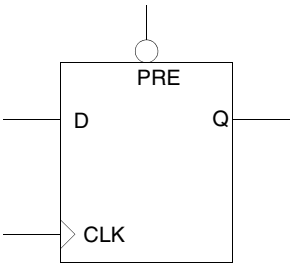
Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
SX, SX-A, eX, Axcelerator	1	1
Others		2

* A 2 on the symbol implies 2 logic module delays only for SX, SX-A, SX-S, eX, and Axcelerator.

DFP1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Preset

Truth Table

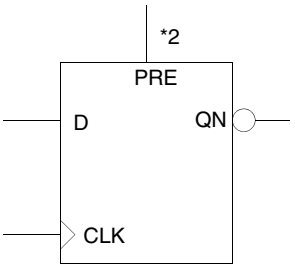
PRE	CLK	Q_{n+1}
0	X	1
1	↑	D

Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX, Axcelerator	1	
Others		2

DFP1C

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active high Preset, and active low Output

Truth Table

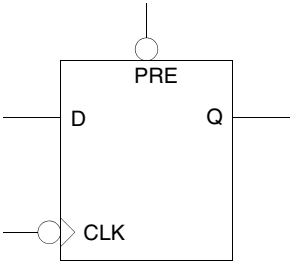
PRE	CLK	QN_{n+1}
1	X	0
0	↑	!D

Input	Output
D, PRE, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	1

DFP1D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Preset and Clock

Truth Table

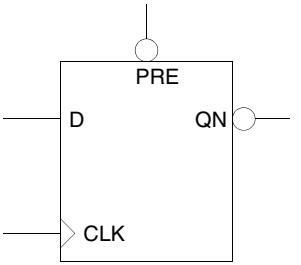
PRE	CLK	Q_{n+1}
0	X	1
1	↓	D

Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX, and Axcelerator	1	
Others		2

DFP1E

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active low Preset and Output

Truth Table

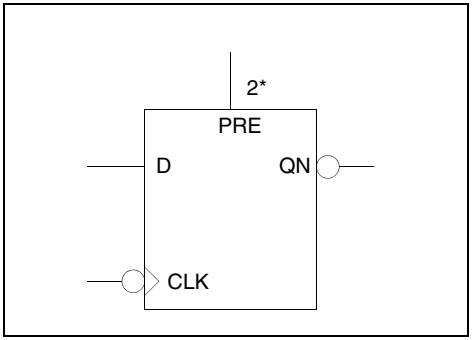
PRE	CLK	QN_{n+1}
0	X	0
1	↑	!D

Input	Output
D, PRE, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFP1F

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active high Preset, and active low Clock and Output

Truth Table

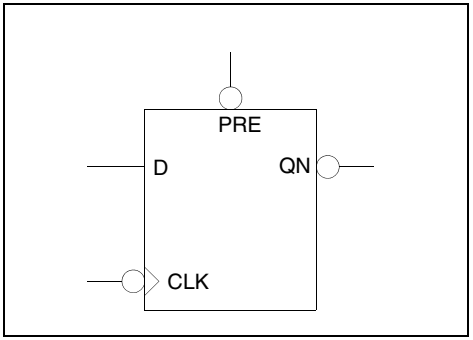
PRE	CLK	QN_{n+1}
1	X	0
0	↓	!D

Input	Output
D, PRE, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	1

DFP1G

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active low Preset, Clock and Output

Truth Table

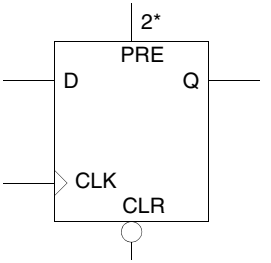
PRE	CLK	QN_{n+1}
0	X	0
1	↓	!D

Input	Output
D, PRE, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

DFPC

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
CLR, D, PRE, CLK	Q

Function

D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	↑	D
0	1	X	**

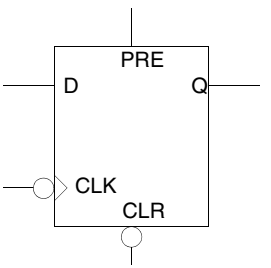
Family	Modules	
	Seq	Comb
Others	1	1
ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX, SX, SX-A, SX-S		2

* A 2 on the symbol implies 2 logic module delays only for SX, SX-A, SX-S, and eX.

** In ACT 1/MX, your design should not allow both PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DFPCA

ACT 1, ACT 2, ACT 3, 3200DX, MX



Input	Output
CLR, D, PRE, CLK	Q

Function

D-Type Flip-Flop with active high Preset, active low Clear and Clock

Truth Table

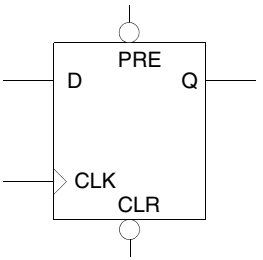
CLR	PRE	CLK	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	*

Family	Modules	
	Seq	Comb
All		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFPCB

SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop, with active low Clear, and Preset

Truth Table

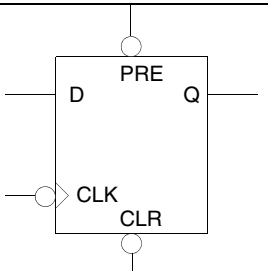
CLR	PRE	CLK	Q_{n+1}
0	X	X	0
1	0	X	1
1	1	↑	D

Input	Output
CLR, D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX, Axcelerator	1	

DFPCC

SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Preset, Clear and Clock

Truth Table

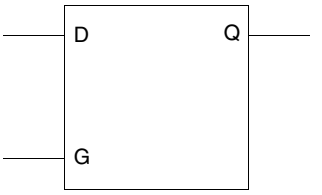
CLR	PRE	CLK	Q_{n+1}
0	X	X	0
1	0	X	1
1	1	↓	D

Input	Output
CLR, D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
All listed	1	

DL1

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch

Truth Table

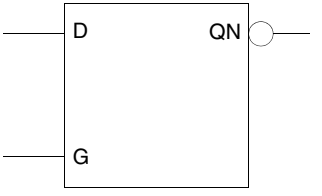
G	Q_{n+1}
0	Q
1	D

Input	Output
D, G	Q

Family	Modules	
	Seq	Comb
ACT 1, MX, SX, SX-A, SX-S, eX		1
Others	1	

DL1A

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



Function

Data Latch with active low Output

Truth Table

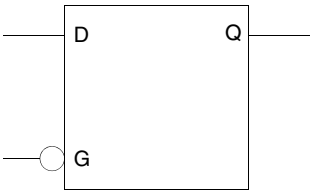
G	QN_{n+1}
0	QN
1	!D

Input	Output
D, G	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DL1B

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active low Clock

Truth Table

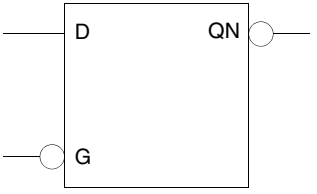
G	Q_{n+1}
1	Q
0	D

Input	Output
D, G	Q

Family	Modules	
	Seq	Comb
ACT 1, MX, SX, SX-A, SX-S, eX		1
Others	1	

DL1C

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



Function

Data Latch, with active low Clock and Output

Truth Table

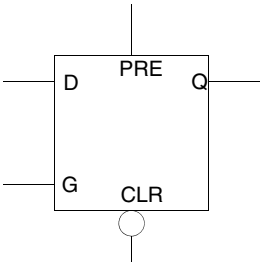
G	QN_{n+1}
1	QN
0	!D

Input	Output
D, G	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DL2A

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active low Clear and active high Preset

Truth Table

CLR	PRE	G	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	0	Q
1	0	1	D
0	1	X	*

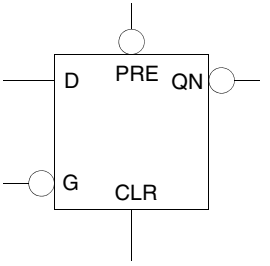
Input	Output
CLR, D, G, PRE	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

*In ACT 1 and MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DL2B

ACT 1, ACT 2, ACT3, 3200DX, MX



Function

Data Latch with active high Clear and active low Preset, Clock, and Output

Truth Table

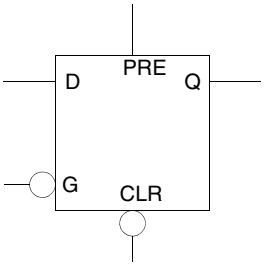
CLR	PRE	G	QN_{n+1}
1	1	X	1
0	0	X	0
0	1	1	QN
0	1	0	!D
1	0	X	*

Input	Output
CLR, D, G, PRE	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

*In ACT 1 and MX, your design should not allow PRE and CLR to be asserted at the same time.
In other families, CLR has priority over PRE.

DL2C



Function

Data Latch with active low Clear, active high Preset, and active low Clock

Truth Table

CLR	PRE	G	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	1	Q
1	0	0	D
0	1	X	*

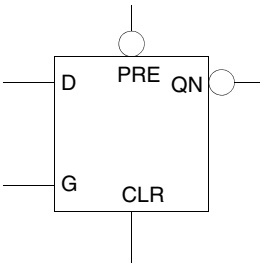
Input	Output
CLR, D, G, PRE	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

*In ACT 1 and MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DL2D

ACT 1, ACT 2, ACT3, 3200DX, MX



Function

Data Latch with active high Clear and active low Preset and Output

Truth Table

CLR	PRE	G	QN_{n+1}
1	1	X	1
0	0	X	0
0	1	0	QN
0	1	1	!D
1	0	X	*

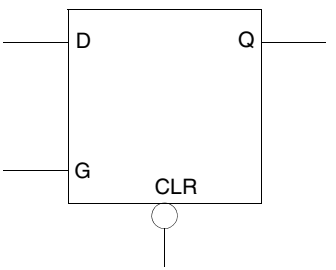
Input	Output
CLR, D, G, PRE	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

*In ACT 1 and MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DLC

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active low Clear

Truth Table

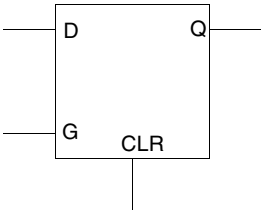
CLR	G	Q_{n+1}
0	X	0
1	0	Q
1	1	D

Input	Output
CLR, D, G	Q

Family	Modules	
	Seq	Comb
ACT 1, MX, SX, SX-A, SX-S, eX		1
Others	1	

DLC1

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active high Clear

Truth Table

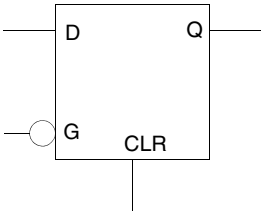
CLR	G	Q_{n+1}
1	X	0
0	0	Q
0	1	D

Input	Output
CLR, D, G	Q

Family	Modules	
	Seq	Comb
All		1

DLC1A

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active high Clear and active low Clock

Truth Table

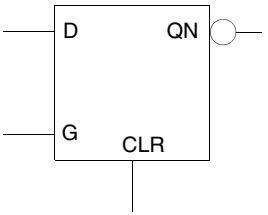
CLR	G	Q_{n+1}
1	X	0
0	1	Q
0	0	D

Input	Output
CLR, D, G	Q

Family	Modules	
	Seq	Comb
All		1

DLC1F

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



Function

Data Latch with active high Clear and active low Output

Truth Table

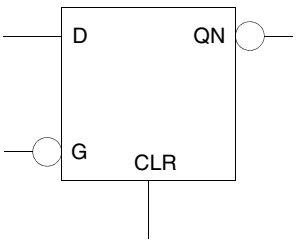
CLR	G	QN_{n+1}
1	X	1
0	0	QN
0	1	!D

Input	Output
CLR, D, G	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

DLC1G

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



Function

Data Latch with active high Clear and active low Clock and Output

Truth Table

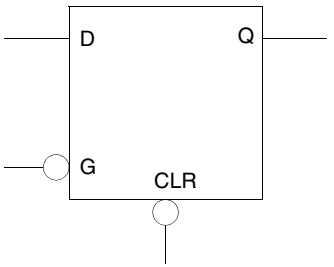
CLR	G	QN_{n+1}
1	X	1
0	1	QN
0	0	!D

Input	Output
CLR, D, G	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

DLCA

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active low Clear and Clock

Truth Table

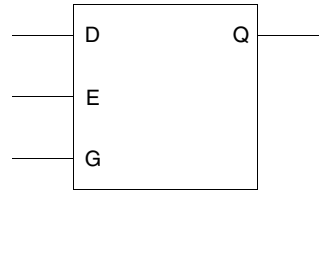
CLR	G	Q_{n+1}
0	X	0
1	1	Q
1	0	D

Input	Output
CLR, D, G	Q

Family	Modules	
	Seq	Comb
Others		1
ACT 2, 1200XL, ACT 3, 3200DX, MX	1	

DLE

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



Function

Data Latch with active high Enable

Truth Table

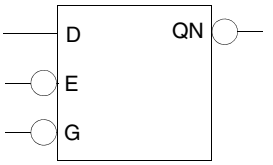
E	G	Q_{n+1}
0	X	Q
X	0	Q
1	1	D

Input	Output
D, E, G	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DLE1D

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



Function

Data Latch with active low Enable and Clock and active low Output

Truth Table

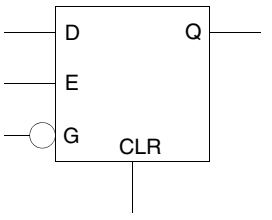
E	G	QN_{n+1}
1	X	QN
X	1	QN
0	0	!D

Input	Output
D, E, G	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DLE2A

ACT 1, MX



Function

Data Latch with active high Enable and Clear, and active low Clock

Truth Table

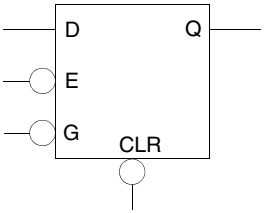
CLR	E	G	Q_{n+1}
1	X	X	0
0	0	X	Q
0	X	1	Q
0	1	0	D

Input	Output
CLR, D, E, G	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1

DLE2B

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



Function

Data Latch with active low Enable, Clear, and Clock

Truth Table

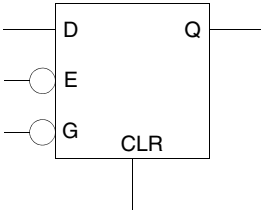
CLR	E	G	Q_{n+1}
0	X	X	0
1	1	X	Q
1	X	1	Q
1	0	0	D

Input	Output
CLR, D, E, G	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DLE2C

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active low Enable and Clock, and active high Clear

Truth Table

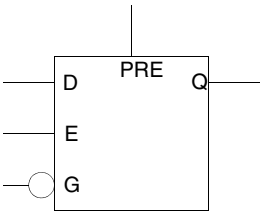
CLR	E	G	Q_{n+1}
1	X	X	0
0	1	X	Q
0	X	1	Q
0	0	0	D

Input	Output
CLR, D, E, G	Q

Family	Modules	
	Seq	Comb
All		1

DLE3A

ACT 1, MX



Function

Data Latch with active high Enable and Preset, and active low Clock

Truth Table

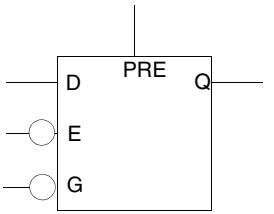
PRE	E	G	Q_{n+1}
1	X	X	1
0	0	X	Q
0	1	0	D
0	X	1	Q

Input	Output
D, E, G, PRE	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1

DLE3B

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active low Enable and Clock, and active high Preset

Truth Table

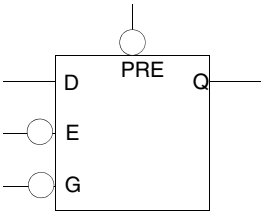
PRE	E	G	Q_{n+1}
1	X	X	1
0	1	X	Q
0	X	1	Q
0	0	0	D

Input	Output
D, E, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

DLE3C

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active low Enable, Preset, and Clock

Truth Table

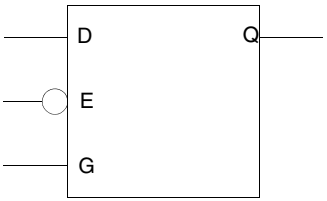
PRE	E	G	Q_{n+1}
0	X	X	1
1	1	X	Q
1	X	1	Q
1	0	0	D

Input	Output
D, E, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

DLEA

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



Function

Data Latch with active low Enable and active high Clock

Truth Table

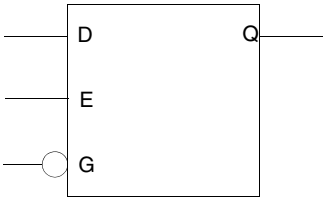
E	G	Q_{n+1}
1	X	Q
X	0	Q
0	1	D

Input	Output
D, E, G	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DLEB

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

Data Latch with active high Enable, and active low Clock

Truth Table

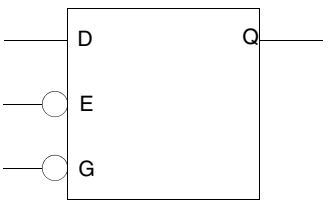
E	G	Q_{n+1}
0	X	Q
X	1	Q
1	0	D

Input	Output
D, E, G	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DLEC

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

Data Latch with active low Enable and Clock

Truth Table

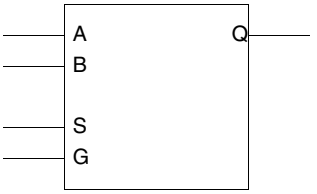
E	G	Q_{n+1}
1	X	Q
X	1	Q
0	0	D

Input	Output
D, E, G	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DLM

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

Data Latch with 2-input Multiplexed Data

Truth Table

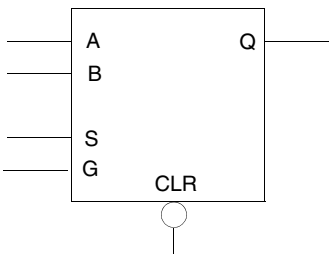
S	G	Q_{n+1}
X	0	Q
0	1	A
1	1	B

Input	Output
A, B, S, G	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DLM2

ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

Data Latch with 2-input Multiplexed Data and Active-Low Clear

Truth Table

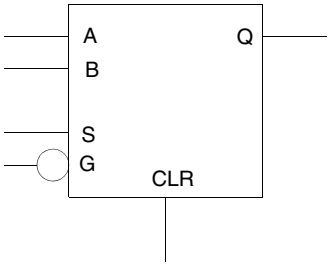
CLR	S	G	Q_{n+1}
0	X	X	0
1	X	0	Q
1	0	1	A
1	1	1	B

Input	Output
A, B, S, G, CLR	Q

Family	Modules	
	Seq	Comb
All listed	1	

DLM2A

ACT 1, MX



Function

Data Latch with 2-input Multiplexed Data and Clear, and Active-Low Clock

Truth Table

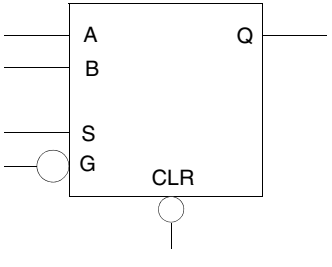
CLR	S	G	Q_{n+1}
1	X	X	0
0	X	1	Q
0	0	0	A
0	1	0	B

Input	Output
A, B, CLR, S, G	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1

DLM2B

ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

Data Latch with 2-input Multiplexed Data and Active-Low Clock and Clear

Truth Table

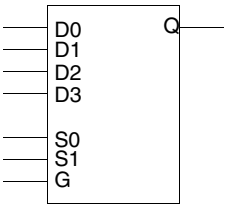
CLR	S	G	Q_{n+1}
0	X	X	0
1	X	1	Q
1	0	0	A
1	1	0	B

Input	Output
A, B, CLR, S, G	Q

Family	Modules	
	Seq	Comb
All listed	1	

DLM3

ACT 2, ACT 3, 3200DX, MX, Axcelerator



Input	Output
D0, D1, D2, D3, S0, S1, G	Q

Function

Data Latch with 4-input Multiplexed Data

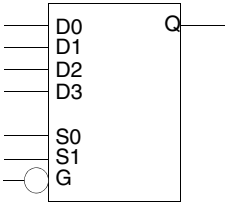
Truth Table

S1	S0	G	Q_{n+1}
X	X	0	Q
0	0	1	D0
0	1	1	D1
1	0	1	D2
1	1	1	D3

Family	Modules	
	Seq	Comb
All listed	1	

DLM3A

ACT 2, ACT 3, 3200DX, MX, Axcelerator



Input	Output
D0, D1, D2, D3, S0, S1, G	Q

Function

Data Latch with 4-input Multiplexed Data, and active low Clock

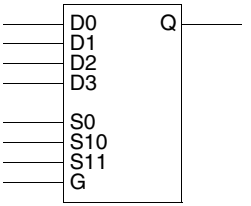
Truth Table

S1	S0	G	Q_{n+1}
X	X	1	Q
0	0	0	D0
0	1	0	D1
1	0	0	D2
1	1	0	D3

Family	Modules	
	Seq	Comb
All listed	1	

DLM4

ACT 2, ACT 3, 3200DX, MX, Axcelerator



Input	Output
D0, D1, D2, D3, S0, S10, S11, G	Q

Function

Data Latch with 4-input Multiplexed Data

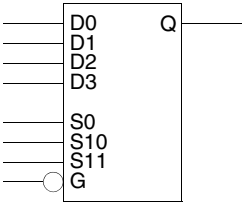
Truth Table

S10	S11	S0	G	Q_{n+1}
X	X	X	0	Q
0	0	0	1	D0
0	0	1	1	D1
X	1	0	1	D2
1	X	0	1	D2
X	1	1	1	D3
1	X	1	1	D3

Family	Modules	
	Seq	Comb
All listed	1	

DLM4A

ACT 2, ACT 3, 3200DX, MX, Axcelerator



Input	Output
D0, D1, D2, D3, S0, S10, S11, G	Q

Function

Data Latch with 4-input Multiplexed Data and active low Clock

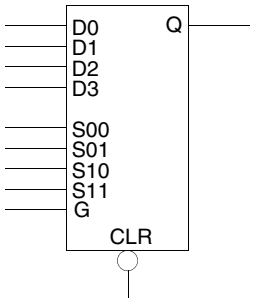
Truth Table

S10	S11	S0	G	Q_{n+1}
X	X	X	1	Q
0	0	0	0	D0
0	0	1	0	D1
X	1	0	0	D2
1	X	0	0	D2
X	1	1	0	D3
1	X	1	0	D3

Family	Modules	
	Seq	Comb
All listed	1	

DLM8A

ACT 3



Input	Output
D0, D1, D2, D3, S00, S01, S10, S11, G, CLR	Q

Function

D-Type Latch with 4-input Multiplexed Data and active low Clear

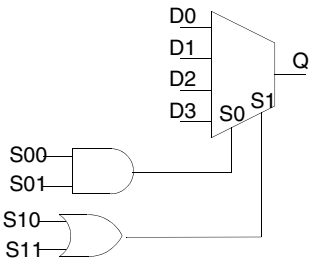
Truth Table

CLR	S11	S10	S01	S00	G	Q_{n+1}
0	X	X	X	X	X	0
1	X	X	X	X	0	Q
1	0	0	0	X	1	D0
1	0	0	X	0	1	D0
1	0	0	1	1	1	D1
1	1	X	0	X	1	D2
1	X	1	0	X	1	D2
1	1	X	X	0	1	D2
1	X	1	X	0	1	D2
1	1	X	1	1	1	D3
1	X	1	1	1	1	D3

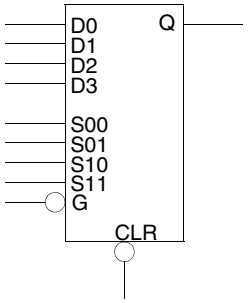
Family	Modules	
	Seq	Comb
ACT 3	1	

NOTE 1: The DLM8A macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DLM8B



Input	Output
D0, D1, D2, D3, S00, S01, S10, S11, G, CLR	Q

Function

D-Type Latch with 4-input Multiplexed Data and active low Clear and Clock

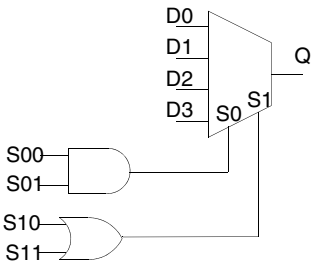
Truth Table

CLR	S11	S10	S01	S00	G	Q_{n+1}
0	X	X	X	X	X	0
1	X	X	X	X	1	Q
1	0	0	0	X	0	D0
1	0	0	X	0	0	D0
1	0	0	1	1	0	D1
1	1	X	0	X	0	D2
1	X	1	0	X	0	D2
1	1	X	X	0	0	D2
1	X	1	X	0	0	D2
1	1	X	1	1	0	D3
1	X	1	1	1	0	D3

Family	Modules	
	Seq	Comb
ACT 3	1	

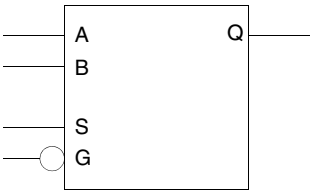
NOTE 1: The DLM8B macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DLMA

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

Data Latch with 2-input Multiplexed Data and active low Clock

Truth Table

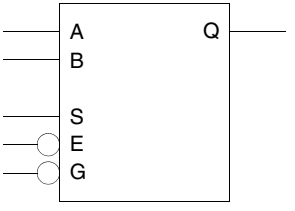
S	G	Q_{n+1}
X	1	Q
0	0	A
1	0	B

Input	Output
A, B, G, S	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DLME1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

2-bit Data Latch with Multiplexed Data and Enable and active low Clock and Enable

Truth Table

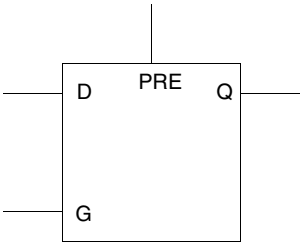
E	S	G	Q_{n+1}
1	X	X	Q
X	X	1	Q
0	0	0	A
0	1	0	B

Input	Output
A, B, E, G, S	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DLP1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active high Preset and Clock

Truth Table

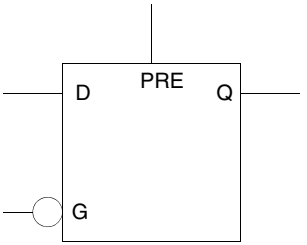
PRE	G	Q_{n+1}
1	X	1
0	0	Q
0	1	D

Input	Output
D, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

DLP1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active high Preset and active low Clock

Truth Table

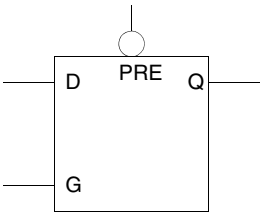
PRE	G	Q_{n+1}
1	X	1
0	1	Q
0	0	D

Input	Output
D, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

DLP1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active low Preset and active high Clock

Truth Table

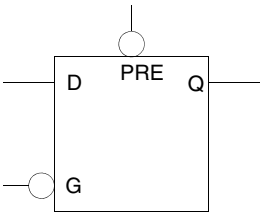
PRE	G	Q_{n+1}
0	X	1
1	0	Q
1	1	D

Input	Output
D, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

DLP1C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Data Latch with active low Preset and Clock

Truth Table

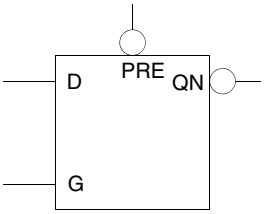
PRE	G	Q_{n+1}
0	X	1
1	1	Q
1	0	D

Input	Output
D, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

DLP1D

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

Data Latch with active low Preset and Output, and active high Clock

Truth Table

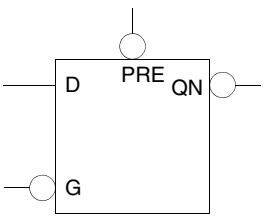
PRE	G	QN_{n+1}
0	X	0
1	0	QN
1	1	!D

Input	Output
D, G, PRE	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DLP1E

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



Function

Data Latch with active low Preset, Clock, and Output

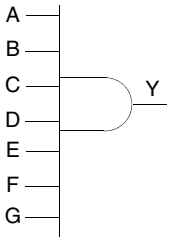
Truth Table

PRE	G	Q_{n+1}
0	X	0
1	0	!D
1	1	QN

Input	Output
D, G, PRE	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

DXAND7



Function

Seven-input AND Gate

Truth Table

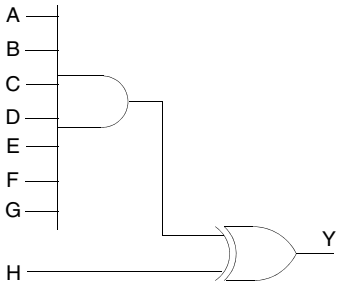
A through G	Y
All inputs = 1	1
Any input = 0	0

Input	Output
A, B, C, D, E, F, G	Y

Family	Modules	
	Seq	DX
3200DX/ MX		1

DXAX7

3200DX, MX



Function

Eight-input AND/Exclusive-OR Gate

Truth Table

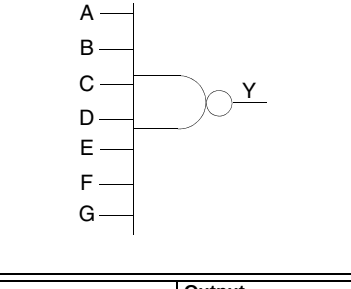
A through G	H	Y
Any input = 0	0	0
Any input = 0	1	1
All inputs = 1	0	1
All inputs = 1	1	0

Input	Output
A, B, C, D, E, F, G, H	Y

Family	Modules	
	Seq	DX
3200DX/ MX		1

DXNAND7

3200DX, MX



Function

Seven-input NAND Gate

Truth Table

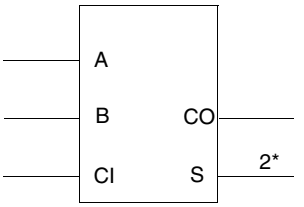
A through G	Y
All inputs = 1	0
Any input = 0	1

Input	Output
A, B, C, D, E, F, G	Y

Family	Modules	
	Seq	DX
3200DX/ MX		1

FA1

ACT 1, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

1 bit adder with active high I/Os

Truth Table

A	B	CI	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

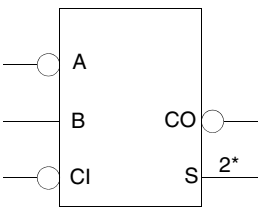
Input	Output
A, B, CI	CO, S

Family	Modules	
	Seq	Comb
ACT 1/ MX		3
SX, SX-A, SX-S, eX		2

* A 2 on the symbol implies 2 logic module delays only in ACT 1 and MX.

FA1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

1-bit Adder, with active low Carry In and Carry Out, and active low A-Input

Truth Table

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0

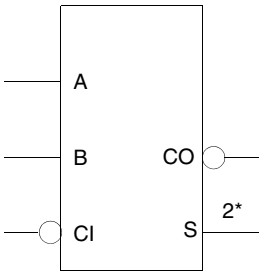
Input	Output
A, B, CI	CO, S

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families except SX and SXA.

FA1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

1-bit Adder with active low Carry In and Carry Out

Truth Table

A	B	CI	CO	S
0	0	0	1	1
0	0	1	1	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1

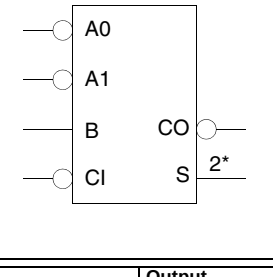
Input	Output
A, B, CI	CO, S

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families except SX and SXA.

FA2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

1-bit Adder, with active low Carry In and Carry Out, and active low A0 and A1 Inputs, used in multipliers

Truth Table [1]

A0	A1	B	CI	CO	S
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	1	1	1
1	1	0	0	1	1

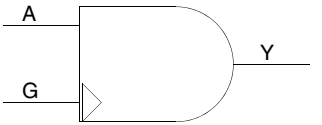
Input	Output
A0, A1, B, CI	CO, S

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families.

GAND2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input AND Clock Net

Truth Table

A	G	Y
X	0	0
0	X	0
1	1	1

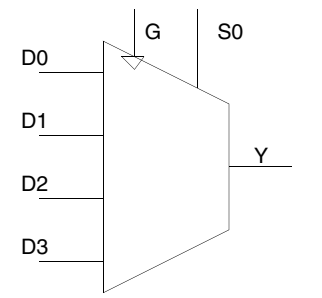
Input	Output
A, G	Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a routed clock (RCLK) or hardwired clock (HCLK) if supported by your device. See your device datasheet for more info.

GMX4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-to-1 Mux Clock Net

Truth Table

G	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

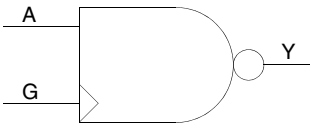
Input	Output
D0, D1, D2, D3, S0, G	Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a routed clock (RCLK) or hardwired clock (HCLK) if supported by your device. See your device datasheet for more info.

GNAND2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input NAND Clock Net

Truth Table

A	G	Y
X	0	1
0	X	1
1	1	0

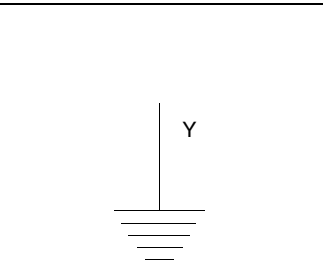
Input	Output
A, G	Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a routed clock (RCLK) or hardwired clock (HCLK) if supported by your device. See your device datasheet for more info.

GND

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

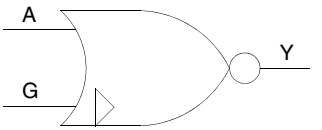
Ground

Input	Output
	Y

NOTE: Ground does not use any modules.

GNOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input NOR Clock Net

Truth Table

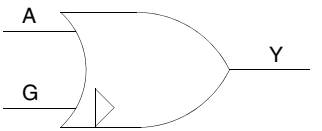
A	G	Y
0	0	1
X	1	0
1	X	0

Input	Output
A, G	Y

Family	Modules	
	Seq	Comb
All		1

GOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input OR Clock Net

Truth Table

A	G	Y
0	0	0
X	1	1
1	X	1

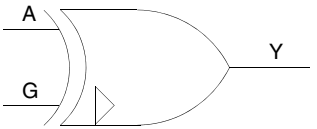
Input	Output
A, G	Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a routed clock (RCLK) if supported by your device. See your device datasheet for more information.

GXOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input XOR Clock Net

Truth Table

A	G	Y
0	0	0
0	1	1
1	0	1
1	1	0

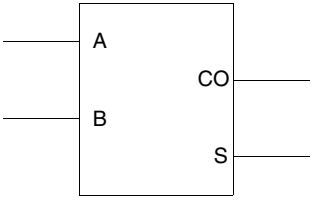
Input	Output
A, G	Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a routed clock (RCLK) if supported by your device. See your device datasheet for more information.

HA1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Half Adder

Truth Table

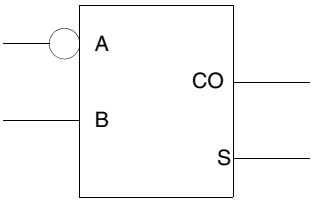
A	B	CO	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Input	Output
A, B	CO, S

Family	Modules	
	Seq	Comb
All		2

HA1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Half-Adder with active low A-Input

Truth Table

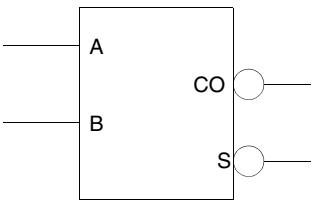
A	B	CO	S
0	0	0	1
0	1	1	0
1	0	0	0
1	1	0	1

Input	Output
A, B	CO, S

Family	Modules	
	Seq	Comb
All		2

HA1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Half-Adder with active low Carry Out and Sum

Truth Table

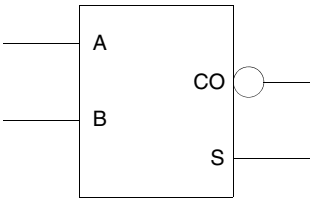
A	B	CO	S
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	1

Input	Output
A, B	CO, S

Family	Modules	
	Seq	Comb
All		2

HA1C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Half-Adder with active low Carry Out

Truth Table

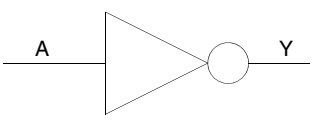
A	B	CO	S
0	0	1	0
0	1	1	1
1	0	1	1
1	1	0	0

Input	Output
A, B	CO, S

Family	Modules	
	Seq	Comb
All		2

INV

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Inverter with active low Output

Truth Table

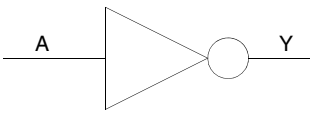
A	Y
0	1
1	0

Input	Output
A	Y

Family	Modules	
	Seq	Comb
All		1

INVD

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Inverter with active low Output
NOTE: The Combiner will not remove this macro

Truth Table

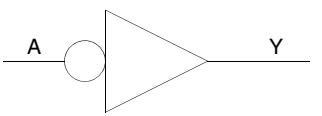
A	Y
0	1
1	0

Input	Output
A	Y

Family	Modules	
	Seq	Comb
All		1

INVA

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

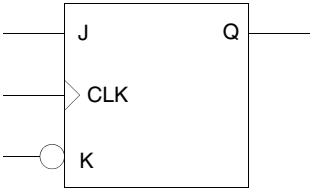
Inverter with active low Input

Truth Table

A	Y
0	1
1	0

Input	Output
A	Y

Family	Modules	
	Seq	Comb
All		1



Function

JK Flip-Flop with active low K-Input

Truth Table

J	K	CLK	Q_{n+1}
0	0	↑	0
0	1	↑	Q
1	0	↑	!Q
1	1	↑	1

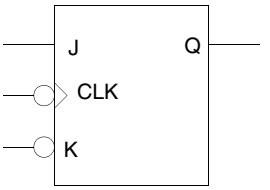
Input
J, K, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
SX, SX-A, SX-S, eX	1	1
Others	1	

JKF1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

JK Flip-Flop with active low Clock and K-Input

Truth Table

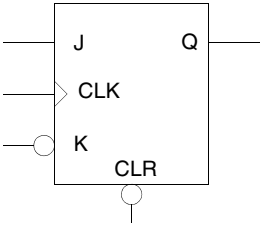
J	K	CLK	Q_{n+1}
0	0	↓	0
0	1	↓	Q
1	0	↓	!Q
1	1	↓	1

Input	Output
J, K, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
SX, SX-A, SX-S, eX	1	1
Others	1	

JKF2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

JK Flip-Flop with active low Clear and K-Input

Truth Table

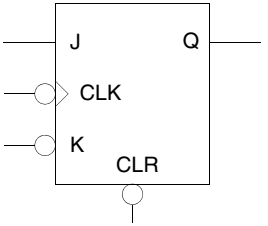
CLR	J	K	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	↑	0
1	0	1	↑	Q
1	1	0	↑	!Q
1	1	1	↑	1

Input	Output
CLR, J, K, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
SX, SX-A, SX-S, eX	1	1
Others	1	

JKF2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
CLR, J, K, CLK	Q

Function

JK Flip-Flop with active low Clear, Clock, and K-Input

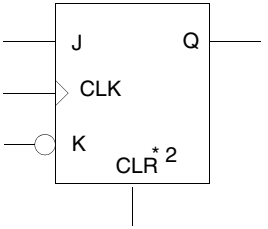
Truth Table

CLR	J	K	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	↓	0
1	0	1	↓	Q
1	1	0	↓	!Q
1	1	1	↓	1

Family	Modules	
	Seq	Comb
ACT 1/MX		2
SX, SX-A, SX-S, eX	1	1
Others	1	

JKF2C

ACT 1, ACT 2, ACT 3, 3200DX, MX



Input	Output
CLR, J, K, CLK	Q

Function

JK Flip-Flop with active high Clear and active low K-Input

Truth Table

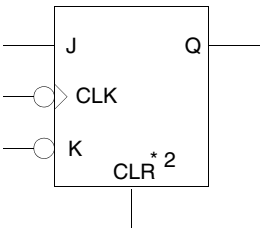
CLR	J	K	CLK	Q_{n+1}
1	X	X	X	0
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	!Q
0	1	1	↑	1

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	1

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and MX.

JKF2D

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

JK Flip-Flop with active high Clear and active low Clock and K-Input

Truth Table

CLR	J	K	CLK	Q_{n+1}
1	X	X	X	0
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

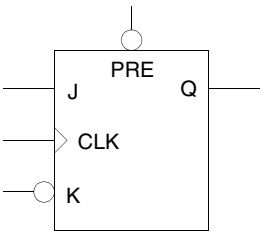
Input	Output
CLR, J, K, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/ MX		2
Others	1	1

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and MX.

JKF3A

ACT 1, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

JK Flip-Flop with active low Preset and K-Input

Truth Table

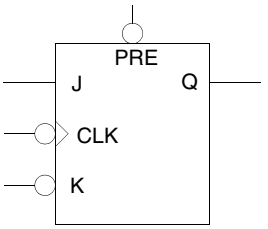
PRE	J	K	CLK	Q_{n+1}
0	X	X	X	1
1	0	0	↑	0
1	0	1	↑	Q
1	1	0	↑	!Q
1	1	1	↑	1

Input	Output
J, K, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
SX, SX-A, SX-S, eX	1	1

JKF3B

ACT 1, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

JK Flip-Flop with active low Preset, Clock, and K-Input

Truth Table

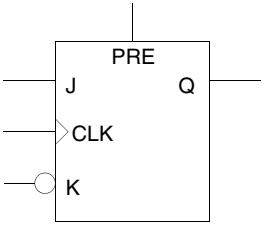
PRE	J	K	CLK	Q_{n+1}
0	X	X	X	1
1	0	0	↓	0
1	0	1	↓	Q
1	1	0	↓	!Q
1	1	1	↓	1

Input	Output
J, K, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
SX, SX-A, SX-S, eX	1	1

JKF3C

ACT 1, MX



Function

JK Flip-Flop with active high Preset and active low K-Input

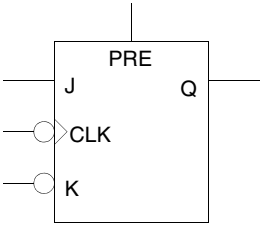
Truth Table

PRE	J	K	CLK	Q_{n+1}
1	X	X	X	1
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	!Q
0	1	1	↑	1

Input	Output
J, K, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

JKF3D



Function

JK Flip-Flop with active high Preset, and active low Clock and K-Inputs

Truth Table

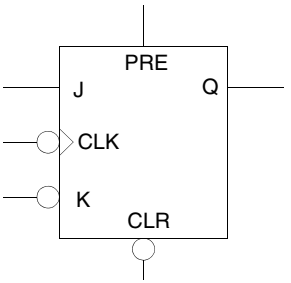
PRE	J	K	CLK	Q_{n+1}
1	X	X	X	1
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

Input	Output
J, K, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

JKF4B

ACT 1, MX



Function

JK Flip-Flop with active high Preset, active low Clear, Clock and K-Input

Truth Table

CLR	PRE	J	K	CLK	Q_{n+1}
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↓	0
1	0	0	1	↓	Q
1	0	1	0	↓	!Q
1	0	1	1	↓	1
0	1	X	X	X	*

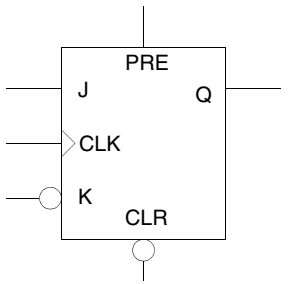
Input	Output
CLR, J, K, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

Your design should not allow both PRE and CLR to be asserted at the same time.

JKFPC

ACT 1, MX



Function

JK Flip-Flop with active high Preset, and active low Clear and K- Input

Truth Table

CLR	PRE	J	K	CLK	Q_{n+1}
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↑	0
1	0	0	1	↑	Q
1	0	1	0	↑	!Q
1	0	1	1	↑	1
0	1	X	X	X	*

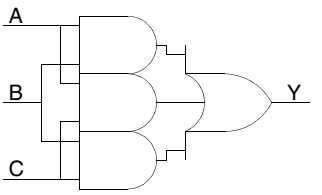
Input	Output
CLR, J, K, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

MAJ3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function

3-Input majority function

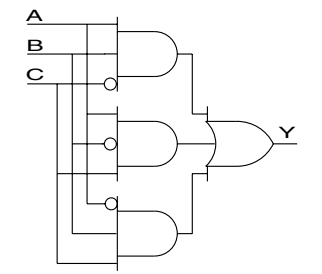
Truth Table

A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

Family	Modules	
	Seq	Comb
All		1

MAJ3X

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function

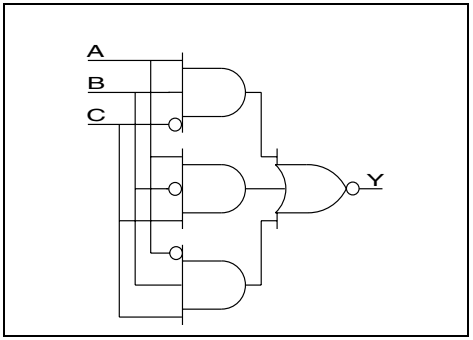
2 of 3 function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

MAJ3XI



Input	Output
A, B, C	Y

Function

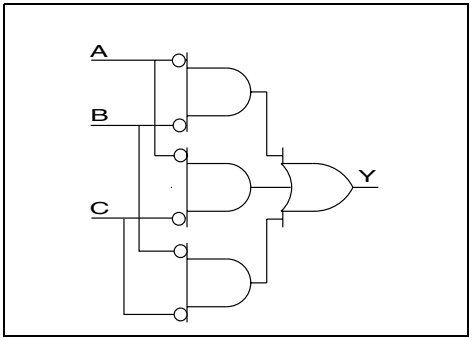
2 of 3 function with active low output

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

MIN3



Input	Output
A, B, C	Y

Function

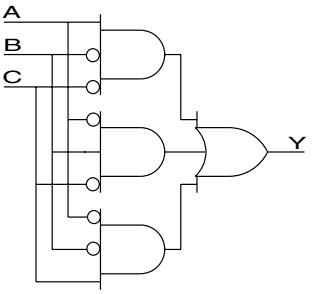
3-Input minority function

Truth Table

A	B	C	Y
X	0	0	1
0	0	X	1
0	X	0	1
X	1	1	0
1	X	1	0
1	1	X	0

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

MIN3X



Function

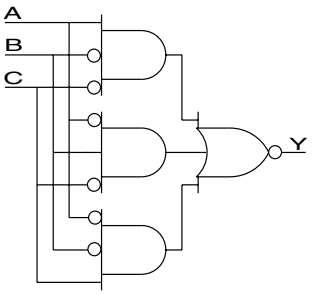
1 of 3 function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1



Input	Output
A, B, C	Y

Function

1 of 3 function with active low output

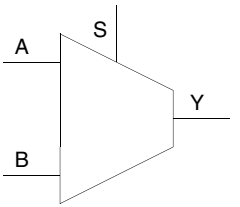
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

MX2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2 to 1 Multiplexer

Truth Table

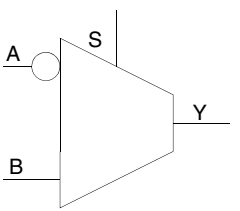
S	Y
0	A
1	B

Input	Output
A, B, S	Y

Family	Modules	
	Seq	Comb
All		1

MX2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2 to 1 Multiplexer with active low A-Input

Truth Table

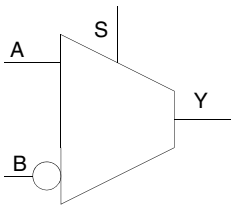
S	Y
0	!A
1	B

Input	Output
A, B, S	Y

Family	Modules	
	Seq	Comb
All		1

MX2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2 to 1 Multiplexer with active low B-Input

Truth Table

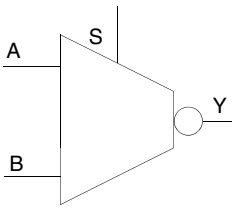
S	Y
0	A
1	!B

Input	Output
A, B, S	Y

Family	Modules	
	Seq	Comb
All		1

MX2C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2 to 1 Multiplexer with active low Output

Truth Table

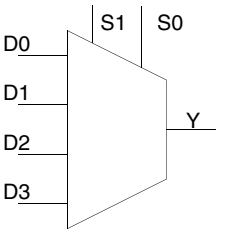
S	Y
0	!A
1	!B

Input	Output
A, B, S	Y

Family	Modules	
	Seq	Comb
All		1

MX4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4 to 1 Multiplexer

Truth Table

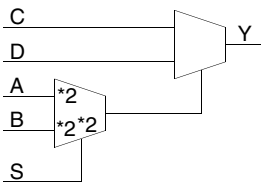
S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Input	Output
D0, S0, S1, D1, D2, D3	Y

Family	Modules	
	Seq	Comb
All		1

MXC1

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

Carry select multiplexer, used in adders

Truth Table

A	B	S	Y
0	X	0	C
1	X	0	D
X	0	1	C
X	1	1	D

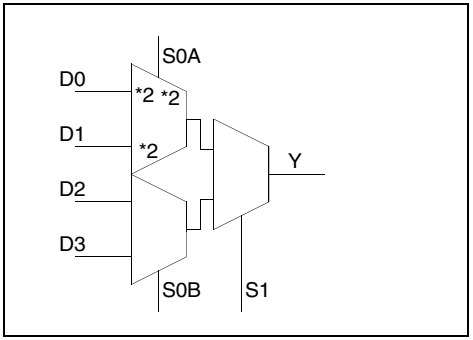
Input	Output
S, A, B, C, D	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and MX.

MXT

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function

Multiplexer with separate select lines

Truth Table

SOB	SOA	S1	Y
X	0	0	D0
X	1	0	D1
0	X	1	D2
1	X	1	D3

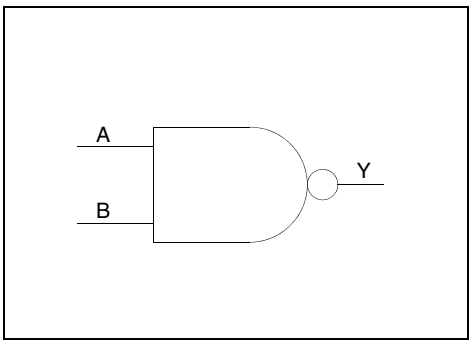
Input	Output
D0 , D1, D2, D3, S0A, S0B, S1	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

* A 2 on the symbol implies a 2 logic module delay on all families except ACT 1 and MX.

NAND2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input NAND

Truth Table

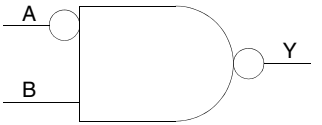
A	B	Y
X	0	1
0	X	1
1	1	0

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

NAND2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input NAND with active low A-Input

Truth Table

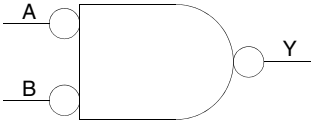
A	B	Y
X	0	1
0	1	0
1	X	1

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

NAND2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input NAND with active low Inputs

Truth Table

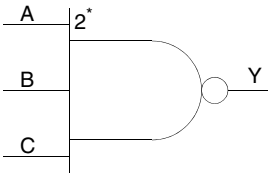
A	B	Y
0	0	0
X	1	1
1	X	1

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

NAND3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input NAND

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

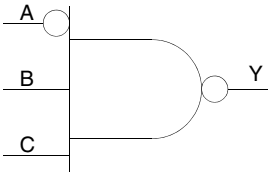
Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

NAND3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input NAND with active low A-Input

Truth Table

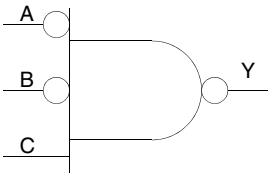
A	B	C	Y
X	X	0	1
X	0	X	1
0	1	1	0
1	X	X	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

NAND3B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input NAND with active low A- and B-Inputs

Truth Table

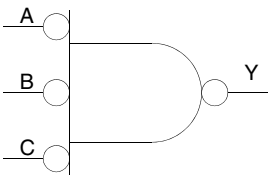
A	B	C	Y
X	X	0	1
0	0	1	0
X	1	X	1
1	X	X	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

NAND3C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input NAND with active low Inputs

Truth Table

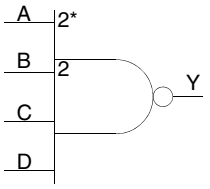
A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

NAND4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input NAND

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

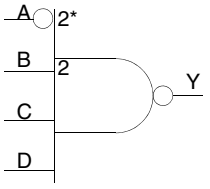
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except in SX, SX-A, SX-S, and eX.

NAND4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input NAND with active low A-Input

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	1	1	1	0
1	X	X	X	1

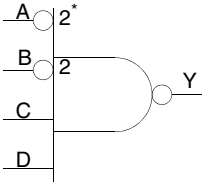
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

NAND4B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input NAND with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	1	1	0
X	1	X	X	1
1	X	X	X	1

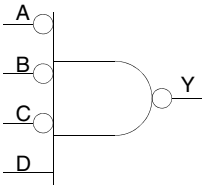
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

NAND4C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input NAND with active low A-, B- and C-Inputs

Truth Table

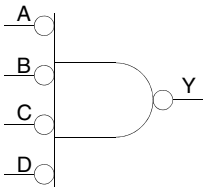
A	B	C	D	Y
X	X	X	0	1
0	0	0	1	0
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

NAND4D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C, D	Y

Function

4-Input NAND with active low Inputs

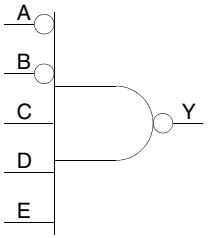
Truth Table

A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Family	Modules	
	Seq	Comb
All		1

NAND5B

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C, D, E	Y

Function

5-input NAND with active low A- and B-inputs

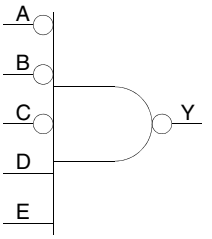
Truth Table

A	B	C	D	E	Y
1	X	X	X	X	1
X	1	X	X	X	1
X	X	0	X	X	1
X	X	X	0	X	1
X	X	X	X	0	1
0	0	1	1	1	0

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

NAND5C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input NAND with active low A-, B- and C-Inputs

Truth Table

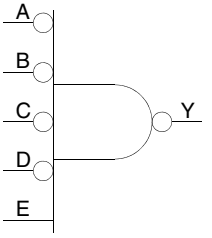
A	B	C	D	E	Y
X	X	X	X	0	1
X	X	X	0	X	1
0	0	0	1	1	0
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
All listed		1

NAND5D

Axcelerator



Function

5-Input NAND with active low A-, B-, C-, and D-Inputs

Truth Table

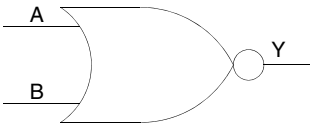
A	B	C	D	E	Y
X	X	X	X	0	1
X	X	X	1	X	1
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1
0	0	0	0	1	0

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
All listed		1

NOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input NOR

Truth Table

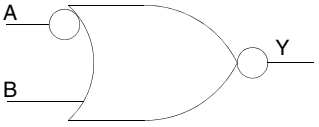
A	B	Y
0	0	1
X	1	0
1	X	0

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

NOR2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input NOR with active low A-Input

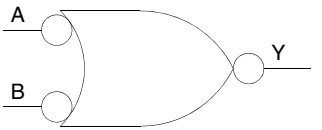
Truth Table

A	B	Y
0	X	0
1	0	1
X	1	0

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

NOR2B



Function

2-Input NOR with active low Inputs

Truth Table

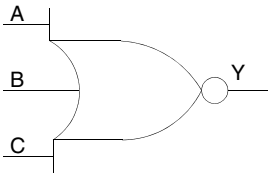
A	B	Y
X	0	0
0	X	0
1	1	1

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

NOR3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input NOR

Truth Table

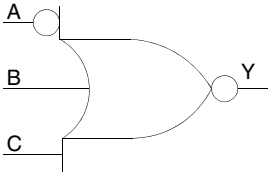
A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

NOR3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input NOR with active low A-Input

Truth Table

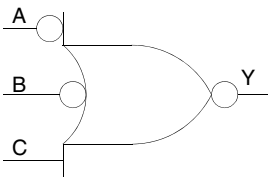
A	B	C	Y
0	X	X	0
1	0	0	1
X	X	1	0
X	1	X	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

NOR3B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input NOR with active low A- and B-Inputs

Truth Table

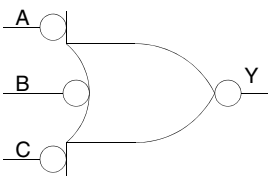
A	B	C	Y
X	0	X	0
0	X	X	0
1	1	0	1
X	X	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

NOR3C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input NOR with active low Inputs

Truth Table

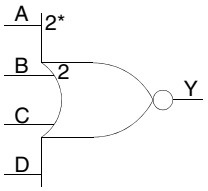
A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

NOR4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input NOR

Truth Table

A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

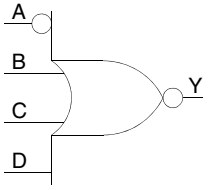
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except SX, SX-A, SX-S, and eX.

NOR4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input NOR with active low A-Input

Truth Table

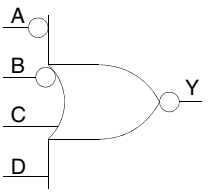
A	B	C	D	Y
0	X	X	X	0
1	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

NOR4B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input NOR with active low A- and B-Inputs

Truth Table

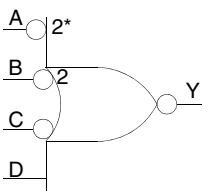
A	B	C	D	Y
X	0	X	X	0
0	X	X	X	0
1	1	0	0	1
X	X	X	1	0
X	X	1	X	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

NOR4C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input NOR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	0	1
X	X	X	1	0

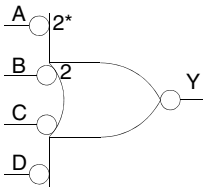
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

NOR4D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input NOR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

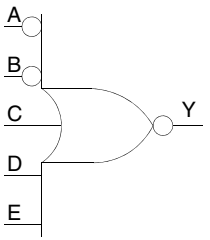
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

NOR5B

SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input NOR with active low A- and B-Inputs

Truth Table

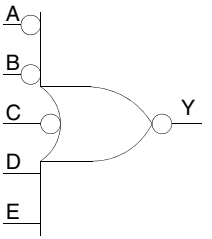
A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	1	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0
1	1	0	0	0	1

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

NOR5C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C, D, E	Y

Function

5-Input NOR with active low A-, B- and C-Inputs

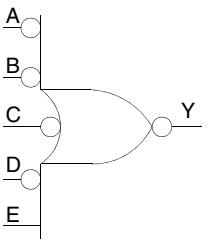
Truth Table

A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0
1	1	1	0	0	1

Family	Modules	
	Seq	Comb
All listed		1

NOR5D

Axcelerator



Input	Output
A, B, C, D, E	Y

Function

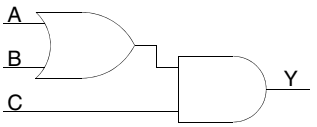
5-Input NOR with active low A-, B-, C-, and D-Inputs

Truth Table

A	B	C	D	E	Y
X	X	X	X	1	0
X	X	X	0	X	0
X	X	0	X	X	0
X	0	X	X	X	0
0	X	X	X	X	0
1	1	1	1	0	1

Family	Modules	
	Seq	Comb
All listed		1

OA1



Function

3 Input OR-AND

Truth Table

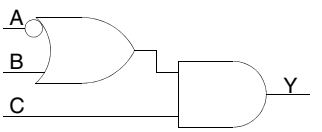
A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

OA1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3 Input OR-AND with active low A-Input

Truth Table

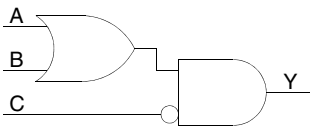
A	B	C	Y
X	X	0	0
0	X	1	1
1	0	X	0
X	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

OA1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3 Input OR-AND with active low C-Input

Truth Table

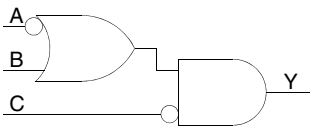
A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

OA1C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3 Input OR-AND with active low A- and C-Inputs

Truth Table

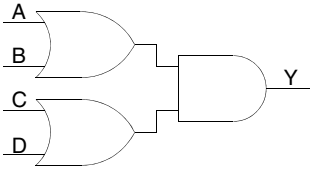
A	B	C	Y
0	X	0	1
X	X	1	0
1	0	X	0
X	1	0	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

OA2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-wide 4-Input OR-AND

Truth Table

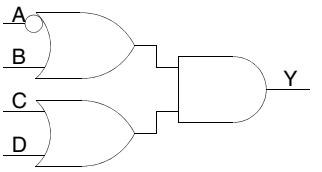
A	B	C	D	Y
X	X	0	0	0
0	0	X	X	0
X	1	X	1	1
X	1	1	X	1
1	X	X	1	1
1	X	1	X	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OA2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2 wide 4-Input OR-AND with active low A-Input

Truth Table

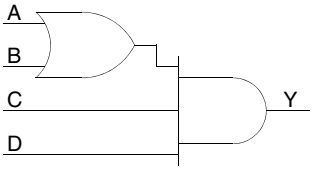
A	B	C	D	Y
X	X	0	0	0
0	X	X	1	1
0	X	1	X	1
1	0	X	X	0
X	1	X	1	1
X	1	1	X	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OA3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4- Input OR-AND

Truth Table

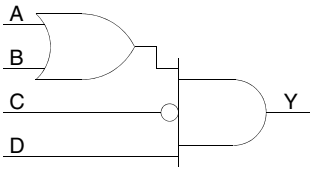
A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	X	X	0
X	1	1	1	1
1	X	1	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OA3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input OR-AND with active low C-Input

Truth Table

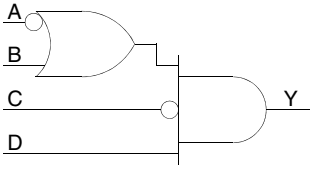
A	B	C	D	Y
X	X	X	0	0
0	0	X	X	0
X	1	0	1	1
X	X	1	X	0
1	X	0	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OA3B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input OR-AND with active low A- and C-Inputs

Truth Table

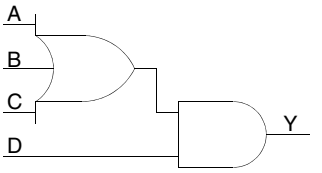
A	B	C	D	Y
X	X	X	0	0
0	X	0	1	1
X	X	1	X	0
1	0	X	X	0
X	1	0	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OA4

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input OR-AND

Truth Table

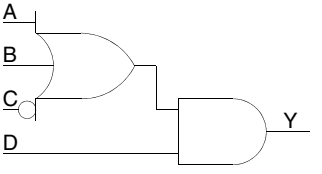
A	B	C	D	Y
X	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed		1

OA4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input OR-AND with active low C-Input

Truth Table

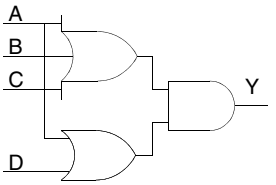
A	B	C	D	Y
X	X	X	0	0
X	X	0	1	1
0	0	1	X	0
X	1	X	1	1
1	X	X	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OA5

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input complex OR-AND

Truth Table

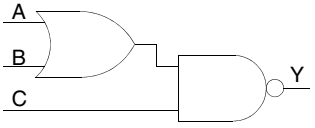
A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OAI1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input OR-AND-INVERT

Truth Table

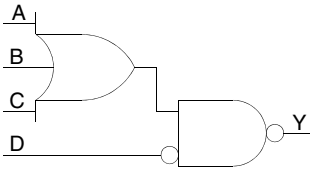
A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

OAI2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input OR-AND-INVERT with active low D-Input

Truth Table

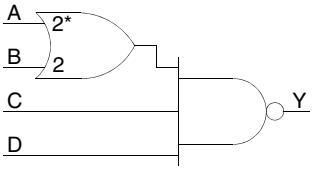
A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OAI3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4 Input OR-AND-INVERT

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

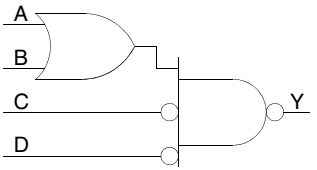
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

* A 2 implies 2 logic module delays only for ACT 1 and MX.

OAI3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4 Input OR-AND-INVERT with active low C- and D-Inputs

Truth Table

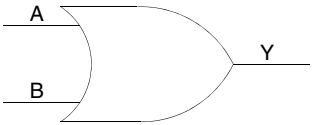
A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input OR

Truth Table

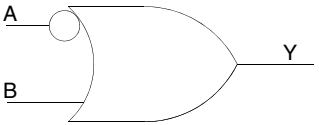
A	B	Y
0	0	0
X	1	1
1	X	1

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

OR2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input OR with active low A-Input

Truth Table

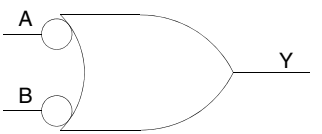
A	B	Y
0	X	1
1	0	0
X	1	1

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

OR2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input OR with active low Inputs

Truth Table

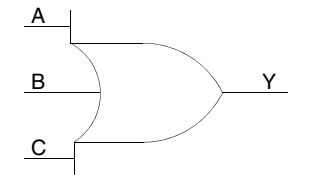
A	B	Y
X	0	1
0	X	1
1	1	0

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

OR3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input OR

Truth Table

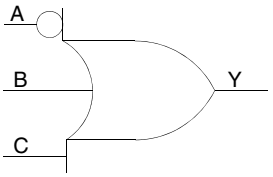
A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

OR3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input OR with active low A-Input

Truth Table

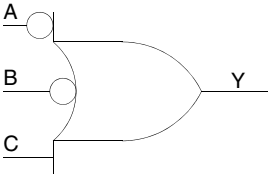
A	B	C	Y
0	X	X	1
1	0	0	0
X	X	1	1
X	1	X	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

OR3B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input OR with active low A- and B-Inputs

Truth Table

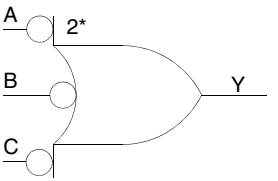
A	B	C	Y
X	0	X	1
0	X	X	1
1	1	0	0
X	X	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

OR3C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input OR with active low Inputs

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

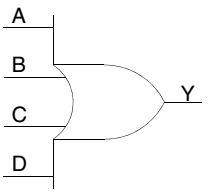
Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

OR4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input OR

Truth Table

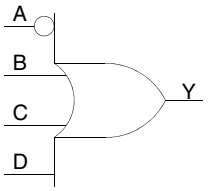
A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OR4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input OR with active low A-Input

Truth Table

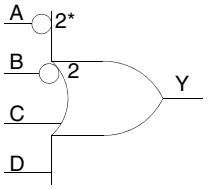
A	B	C	D	Y
0	X	X	X	1
1	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

OR4B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input OR with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
X	0	X	X	1
0	X	X	X	1
1	1	0	0	0
X	X	X	1	1
X	X	1	X	1

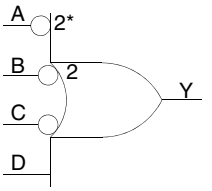
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

OR4C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input OR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	0	0
X	X	X	1	1

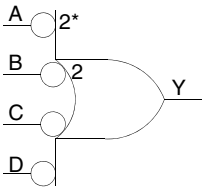
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

*A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

OR4D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

4-Input OR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

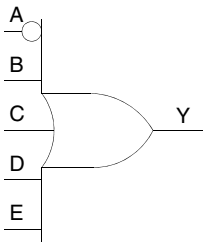
Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except for SX, SX-A, SX-S, eX.

OR5A

SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input OR with active low A- Input

Truth Table

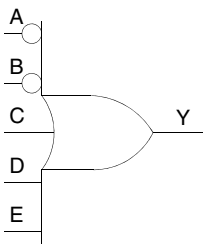
A	B	C	D	E	Y
0	X	X	X	1	1
X	1	X	X	X	1
X	X	1	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	0	0	0	0	0

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

OR5B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input OR with active low A- and B-Inputs

Truth Table

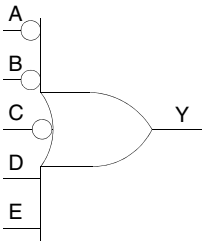
A	B	C	D	E	Y
X	0	X	X	X	1
0	X	X	X	X	1
1	1	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
All listed		1

OR5C

SX, SX-A, SX-S, eX, Axcelerator



Function

5-Input OR with active low A-, B- and C-Inputs

Truth Table

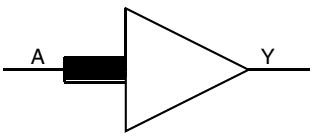
A	B	C	D	E	Y
0	X	X	X	X	1
X	0	X	X	X	1
X	X	0	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	1	1	0	0	0

Input	Output
A, B, C, D, E	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

QCLKINT

3200DX, MX, SX-A, SX-S



Function

Internal Clock Interface

Truth Table

A	Y
0	0
1	1

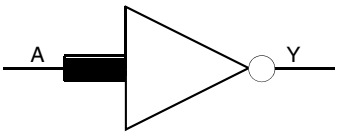
Input	Output
A	Y

NOTE: QCLKINT does not use any modules

For more information on the Global Clock Network, refer to Actel's Data Book.

QCLKINTI

SX-A, SX-S



Function

Internal Clock Interface

Truth Table

A	Y
0	1
1	0

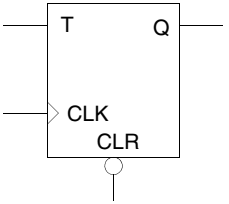
Input	Output
A	Y

NOTE: QCLKINTI does not use any modules

For more information on the Global Clock Network, refer to Actel's Data Book.

TF1A

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

T-Type Flip-Flop with active low Clear

Truth Table

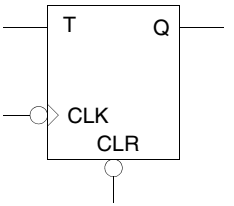
CLR	T	CLK	Q_{n+1}
0	X	X	0
1	1	↑	!Q
1	0	↑	Q

Input	Output
CLR, T, CLK	Q

Family	Modules	
	Seq	Comb
All listed	1	

TF1B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

T-Type Flip-Flop with active low Clear and Clock

Truth Table

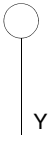
CLR	T	CLK	Q_{n+1}
0	X	X	0
1	1	↓	!Q
1	0	↓	Q

Input	Output
CLR, T, CLK	Q

Family	Modules	
	Seq	Comb
All listed	1	

VCC

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

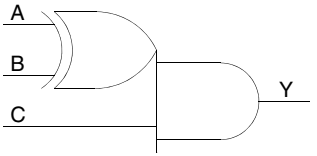
Power

Input	Output
	Y

NOTE: VCC does not use any modules.

XA1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input XOR-AND

Truth Table

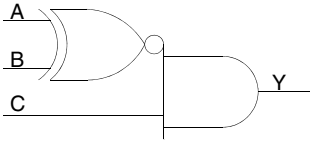
A	B	C	Y
X	X	0	0
0	0	X	0
0	1	1	1
1	0	1	1
1	1	X	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

XA1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input XNOR-AND

Truth Table

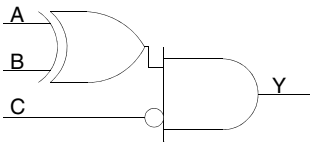
A	B	C	Y
X	X	0	0
0	0	1	1
0	1	X	0
1	0	X	0
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

XA1B

SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input XNOR-AND with active low C-input

Truth Table

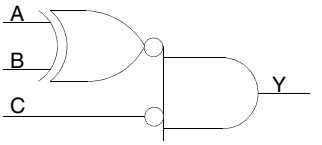
A	B	C	Y
X	X	1	0
0	0	X	0
1	0	0	1
0	1	0	1
1	1	X	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

XA1C

SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input XNOR-AND with active low C-input

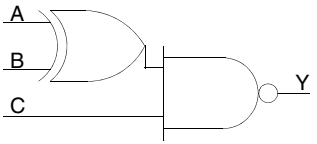
Truth Table

A	B	C	Y
X	X	1	0
0	0	0	1
1	0	X	0
0	1	X	0
1	1	0	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

XAI1



Function

3-Input XNOR-NAND

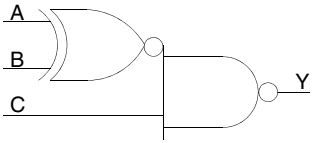
Truth Table

A	B	C	Y
X	X	0	1
0	0	X	1
1	0	1	0
0	1	1	0
1	1	X	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

XAI1A



Function

3-Input XNOR-NAND

Truth Table

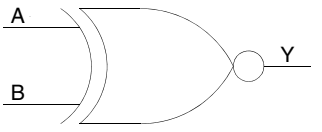
A	B	C	Y
X	X	0	1
0	0	1	0
1	0	X	1
0	1	X	1
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

XNOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2- Input XNOR

Truth Table

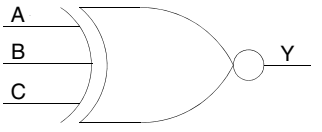
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

XNOR3

SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input XNOR

Truth Table

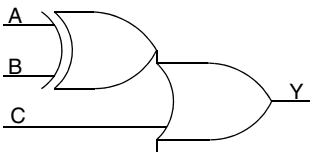
A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

XO1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input XOR-OR

Truth Table

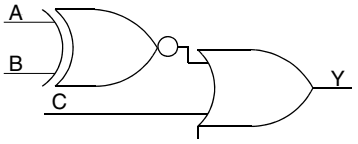
A	B	C	Y
0	0	0	0
X	X	1	1
0	1	X	1
1	0	X	1
1	1	0	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

XO1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input XNOR-OR

Truth Table

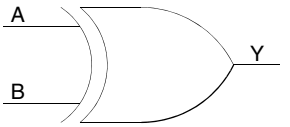
A	B	C	Y
0	0	0	1
X	X	1	1
0	1	0	0
1	0	0	0
1	1	0	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

XOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

2-Input XOR

Truth Table

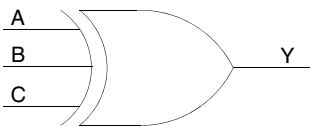
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Input	Output
A, B	Y

Family	Modules	
	Seq	Comb
All		1

XOR3

SX, SX-A, SX-S, eX, Axcelerator



Function

3-Input XOR

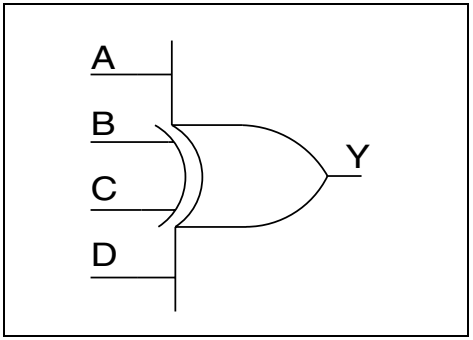
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

XOR4



Function

4-Input Exclusive OR Gate

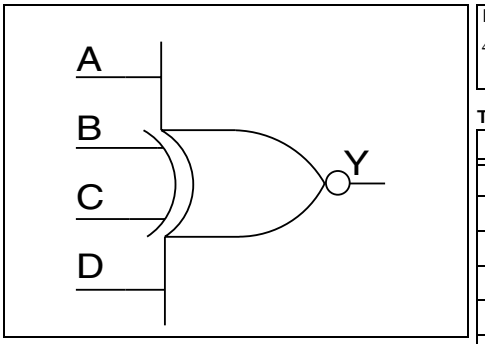
Truth Table

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed		2

XNOR4



Function

4-input Exclusive NOR gate

Truth Table

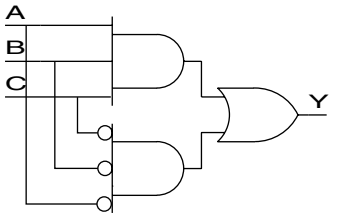
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed		2

ZOR3

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function

3-Input function

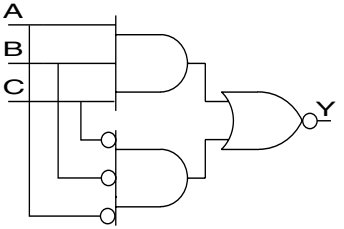
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

ZOR3I

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

Function

3-Input function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

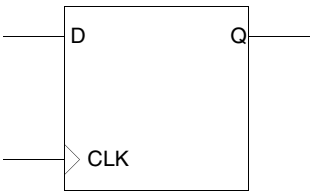
Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

CC-Module Flip Flops

These macros are useful in some radiation hostile applications. They sacrifice area in exchange for a lower single-event upset (SEU) rate caused by ion particle collisions. These special cells use two combinational modules to implement a register instead of using the dedicated registers in the array. (See the application note titled, *Design Techniques for RadHard Field Programmable Gate Arrays.*)

DF1_CC

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop

Truth Table

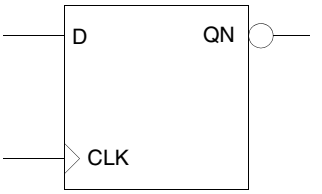
CLK	Q_{n+1}
↑	D

Input	Output
D, CLK	Q

Family	Modules	
	Seq	Comb
All		2

DF1A_CC

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active low Output

Truth Table

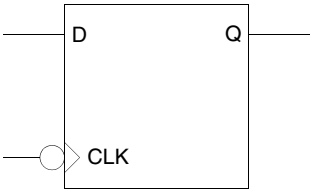
CLK	QN_{n+1}
↑	!D

Input	Output
D, CLK	QN

Family	Modules	
	Seq	Comb
All listed		2

DF1B_CC

ACT 2, ACT 3, 3200DX, MX SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop with active low Clock

Truth Table

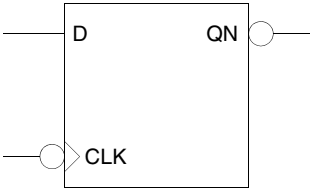
CLK	Q_{n+1}
↓	D

Input	Output
D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	

DF1C_CC

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active low Clock and Output

Truth Table

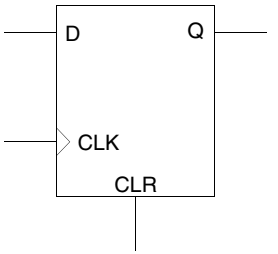
CLK	QN_{n+1}
↓	!D

Input	Output
D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2

DFC1_CC

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop, with active high Clear

Truth Table

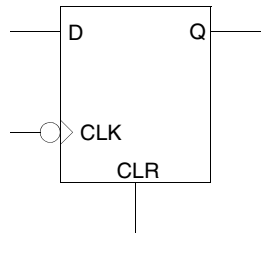
CLR	CLK	Q_{n+1}
1	X	0
0	↑	D

Input	Output
D, CLK, CLR	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2

DFC1A_CC

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop, with active high Clear, and active low Clock

Truth Table

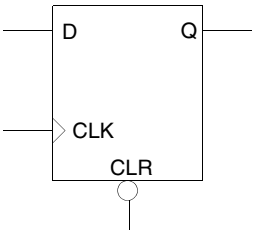
CLR	CLK	Q_{n+1}
1	X	0
0	↓	D

Input	Output
D, CLK, CLR	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2

DFC1B_CC

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop, with active low Clear

Truth Table

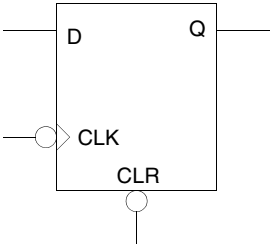
CLR	CLK	Q_{n+1}
0	X	0
1	↑	D

Input	Output
D, CLK, CLR	Q

Family	Modules	
	Seq	Comb
All listed		2

DFC1D_CC

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop, with active low Clear and Clock

Truth Table

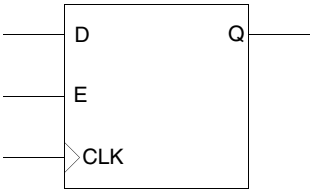
CLR	CLK	Q_{n+1}
0	X	0
1	↓	D

Input	Output
D, CLK, CLR	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	

DFE_CC

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with active high Enable

Truth Table

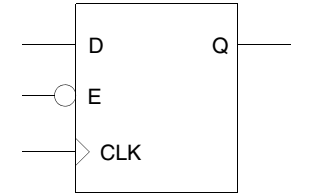
E	CLK	Q_{n+1}
0	X	Q
1	↑	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2

DFE1B_CC

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop with active low Enable

Truth Table

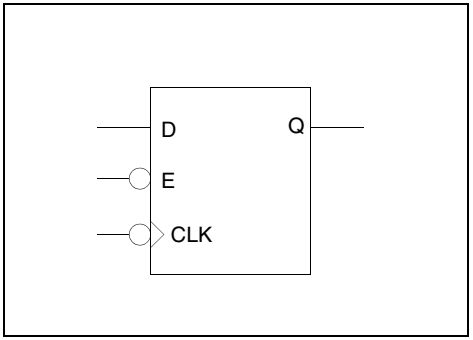
E	CLK	Q_{n+1}
1	X	Q
0	↑	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	

DFE1C_CC

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop with active low Enable and Clock

Truth Table

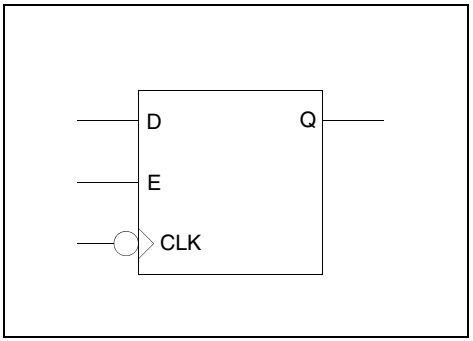
E	CLK	Q_{n+1}
1	X	Q
0	↓	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	

DFEA_CC

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with Enable and active low Clock

Truth Table

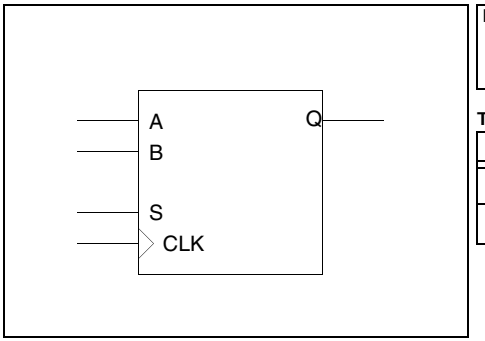
E	CLK	Q_{n+1}
0	X	Q
1	↓	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2

DFM_CC

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data

Truth Table

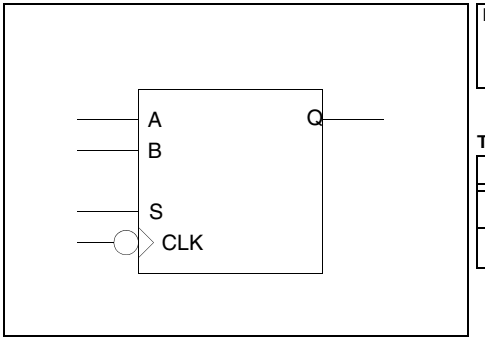
S	CLK	Q_{n+1}
0	↑	A
1	↑	B

Input	Output
A, B, S, CLK	Q

Family	Modules	
	Seq	Comb
All listed		2

DFMA_CC

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

Truth Table

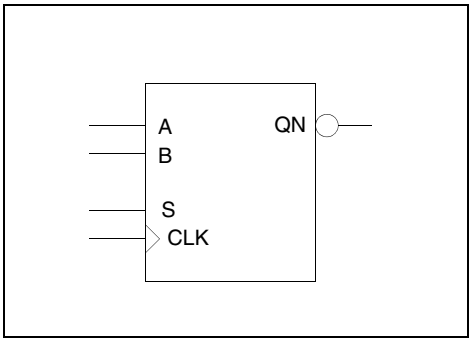
S	CLK	Q_{n+1}
0	↓	A
1	↓	B

Input	Output
A, B, S, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2

DFM1B_CC

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

Truth Table

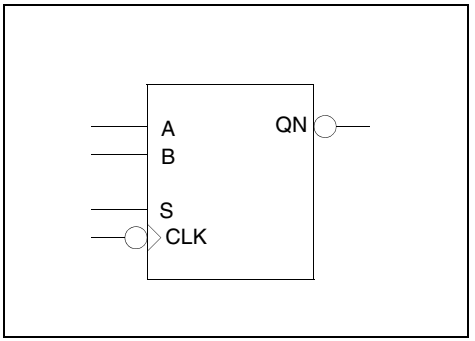
S	CLK	QN_{n+1}
0	↑	!A
1	↑	!B

Input	Output
A, B, S, CLK	QN

Family	Modules	
	Seq	Comb
All listed		2

DFM1C_CC

ACT 2, ACT 3, 3200DX, MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data and active low Clock and Output

Truth Table

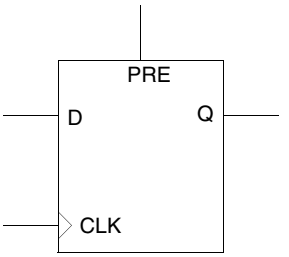
S	CLK	QN_{n+1}
0	↓	!A
1	↓	!B

Input	Output
A, B, S, CLK	QN

Family	Modules	
	Seq	Comb
All listed		2

DFP1_CC*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop with active high Preset

Truth Table

PRE	CLK	Q_{n+1}
1	X	1
0	↑	D

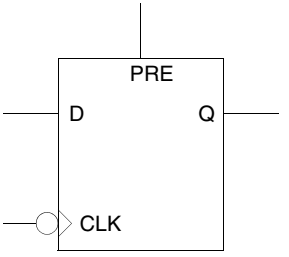
Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	1

* Identical to macro DFP1.

DFP1A_CC*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop with active high Preset, and active low Clock

Truth Table

PRE	CLK	Q_{n+1}
1	X	1
0	↓	D

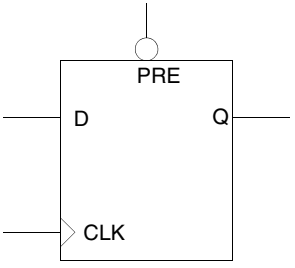
Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	1

* Identical to macro DFP1A.

DFP1B_CC*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

D-Type Flip-Flop with active low Preset

Truth Table

PRE	CLK	Q_{n+1}
0	X	1
1	↑	D

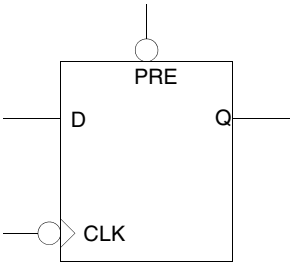
Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1B.

DFP1D_CC*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop with active low Preset and Clock

Truth Table

PRE	CLK	Q_{n+1}
0	X	1
1	↓	D

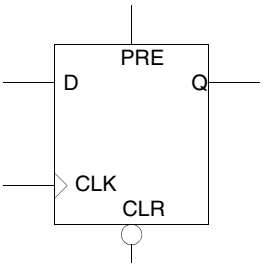
Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	

* Identical to macro DFP1D.

DFPC_CC*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	X	X	0
1	1	X	1
1	0	↑	D

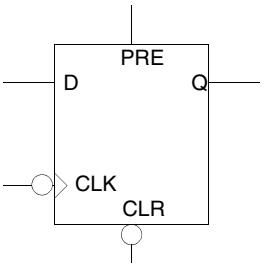
Input	Output
CLR, D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	1

* Identical to macro DFPC.

DFPCA_CC*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



Function

D-Type Flip-Flop with active high Preset, active low Clear, and active low Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	**

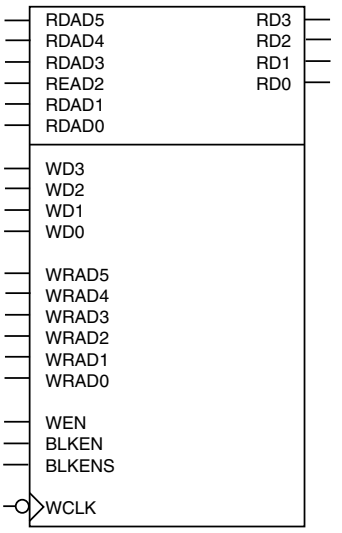
Input	Output
CLR, D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	1

* Identical to Macro DFPCA.

** Your design should not allow both PRE and CLR to be asserted at the same time.

Memory Macros



Function

64X4 dual-port RAM with falling Write clock and asynchronous Read

Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

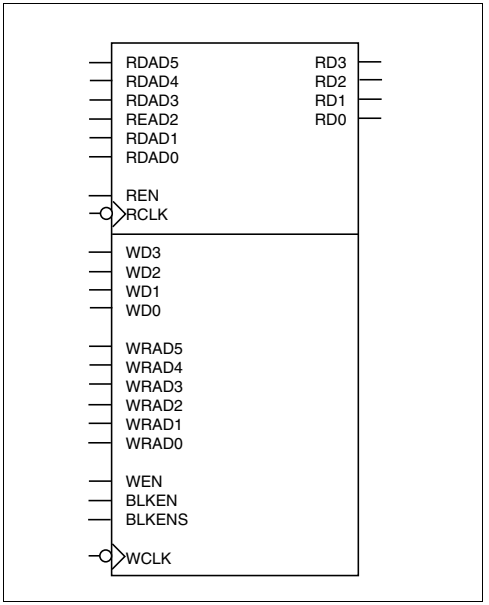
NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Family	Modules
	RAM
All listed	1



Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Function
64X4 dual-port RAM with falling Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

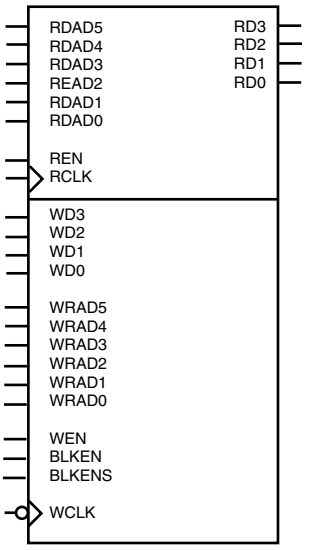
Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1



Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Function

64X4 dual-port RAM with falling Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

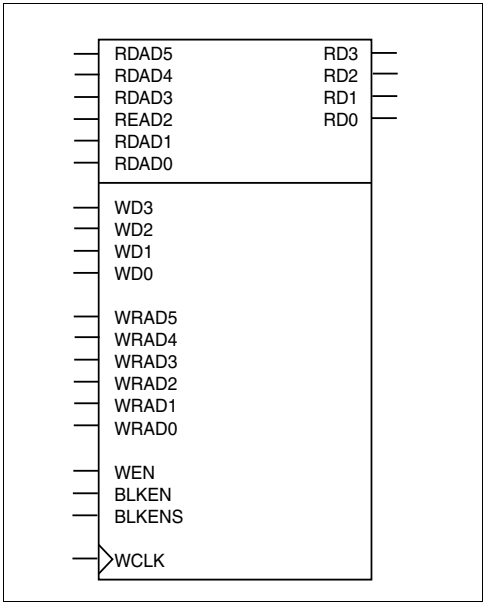
Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1



Function

64X4 dual-port RAM with rising Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

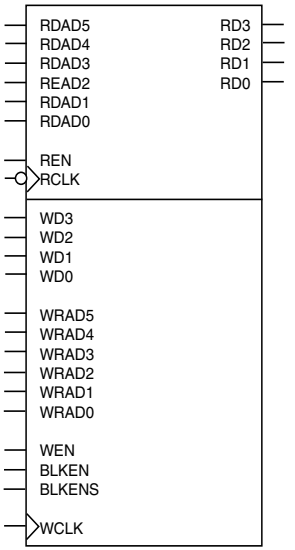
Output
RD3, RD2, RD1, RD0

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1



Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Function

64X4 dual-port RAM with rising Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

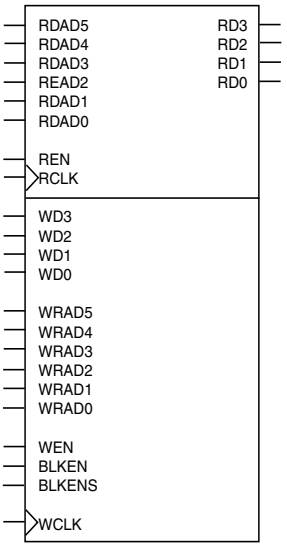
Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1



Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Function

64X4 dual-port RAM with rising Write clock and rising Read clock

Actel recommends that you do NOT use this macro. Contact Actel technical supoort for more information.

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

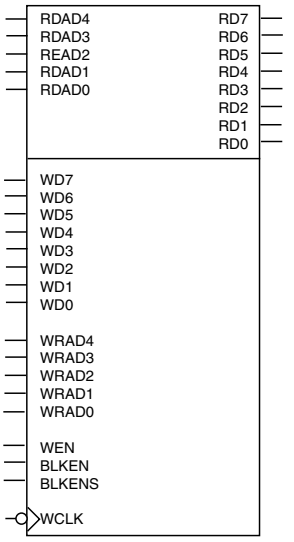
Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1



Function

32X8 dual-port RAM with falling Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

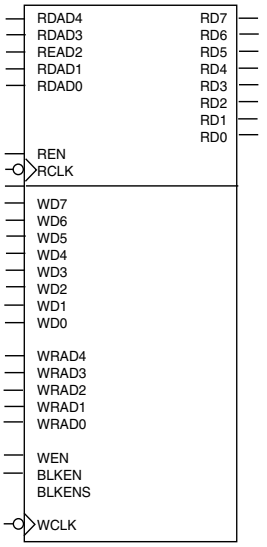
NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All listed	1



Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Function

32X8 dual-port RAM with falling Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

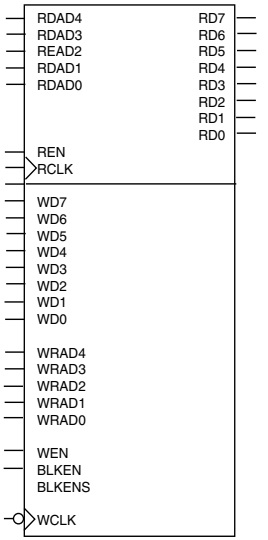
Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1



Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Function

32X8 dual-port RAM with falling Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

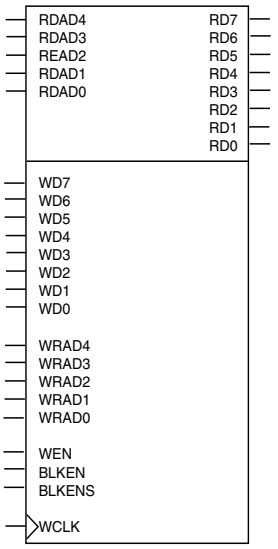
Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1



Function

32X8 dual-port RAM with rising Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0,
WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0,
WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

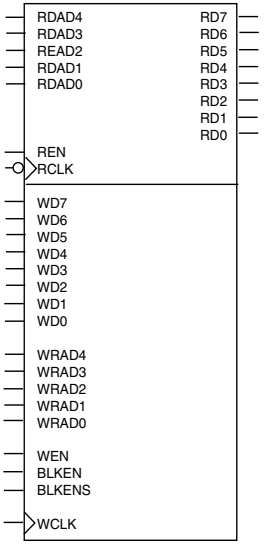
Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1



Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Function

32X8 dual-port RAM with rising Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

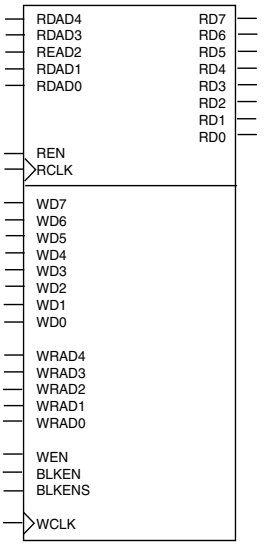
Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1



Function

32X8 dual-port RAM with rising Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

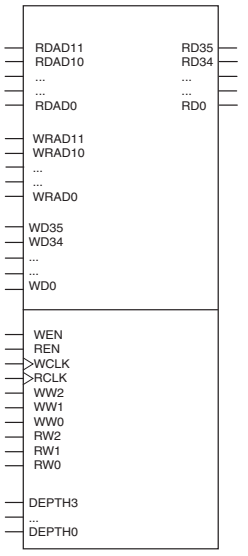
Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All listed	1



Input
RDAD11, ..., RDAD0
WRAD11, ..., WRAD0
WD35, ..., WD0,
WEN, REN, WCLK,
RCLK, WW2, WW1,
WW0, RW2, RW1, RW0,
DEPTH3, ..., DEPTH0

Output
RD35, ..., RD0

Function

Dual port completely independent fully synchronous RAM; the RAM blocks may be cascaded up to 16 by configuring the Depth3-0 ports.

Actel recommends you use ACTgen RAM blocks instead of RAM macros because ACTgen configures WW/RW to choose the best aspect ratio and cascades multiple blocks to achieve larger configurations.

For RAM64K36P, data appears on RD after 2 clock cycles on RCLK

Write Truth Table

WCLK	WEN	Action
1	1	WD written to WRAD
0	1	None
X	0	None

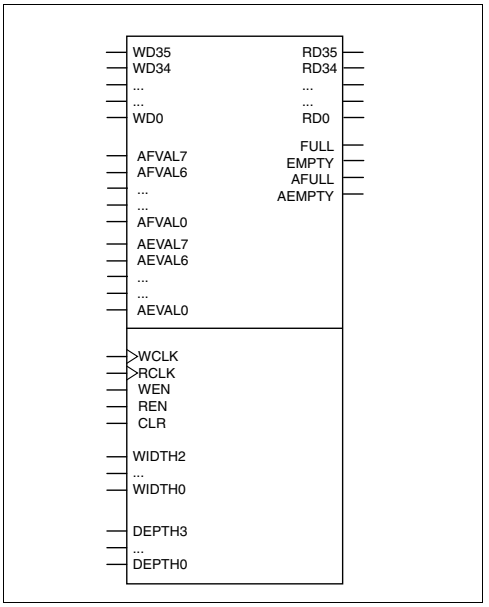
Read Truth Table

RCLK	REN	Action
1	1	RD is read from RDAD
0	1	RD is unchanged
X	0	Rd is unchanged

Family	Modules
	RAM
All listed	1

SRAM Port Aspect Ratios

Read/Write Depth	Read/Write Depth	Read/Write ADDR Bus	Read/Write Data Bus	RW/WW[2:0]
1	4096	ADDR[11:0]	DATA[0]	000
2	2048	ADDR[10:0]	DATA[1:0]	001
4	1024	ADDR[9:0]	DATA[3:0]	010
9	512	ADDR[8:0]	DATA[8:0]	011
18	256	ADDR[7:0]	DATA[17:0]	100
36	128	ADDR[6:0]	DATA[35:0]	101



Function

Dual port completely independent fully synchronous FIFO

For FIFO64K36P, data appears on READ after 2 clock cycles on RCLK. FIFO flag behavior is same as that of FIFO64K36

See the Axcelerator datasheet at http://www.actel.com for more information on this macro.

Input
WD35, ..., WD0,
AFVAL7, ..., AFVAL0,
AEVAL7, ..., AEVAL0,
WCLK, RCLK, WEN,
REN, CLR,
WIDTH2, ..., WIDTH0
DEPTH3, ..., DEPTH0

Output
RD35, ..., RD0
FULL, EMPTY, AFULL,
AEMPTY

Family	Modules
	RAM
All listed	1

FIFO Aspect Ratios Table 1

Data Width	FIFO Depth	Read/Write Data Bus	Width[2:0]
1	4096	DATA[0]	000
2	2048	DATA[1:0]	001
4	1024	DATA[3:0]	010
9	512	DATA[8:0]	011
18	256	DATA[17:0]	100
36	128	DATA[35:0]	101

FIFO Aspect Ratios Table 2

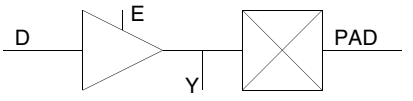
Depth	Cascaded Blocks	Full[a]	Address Bus WCNT/RCNT	AEVAL/AFVAL Step Size
00001	1	2^{12-W}	[15:W]	2^{8-W}
00011	2	2^{13-W}	[15:W]	2^{8-W}
00111	4	2^{14-W}	[15:W]	2^{8-W}
01111	8	2^{15-W}	[15:W]	2^{8-W}
11111	16	2^{16-W}	[15:W]	2^{8-W}

a. W = width in FIFO Aspect Ratios Table 1

I/O Macros

BIBUF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Bidirectional Buffer, High Slew (with Hidden Buffer at Y pin)

Truth Table

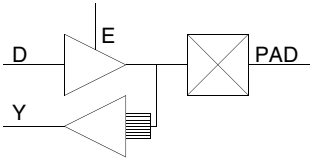
MODE	E	D	PAD	Y
OUTPUT	1	X	D	D
INPUT	0	X	X	PAD

Input	Output
D, E, PAD	PAD, Y

Family	Modules	
	Seq	I/O
All		1

CLKBIBUF

ACT1, ACT2, ACT3, 3200DX, 42MX, 54SX, 54SX-A, Axcelerator



Function

Bidirectional with input dedicated to hardwired clock network

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

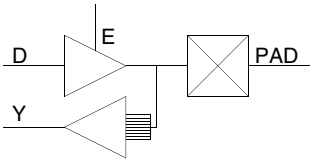
Input	Output
D, E, PAD	PAD, Y

Family	Modules	
	Seq	I/O
All listed		1

NOTE: Refer to the device-specific datasheet for more Clock Network information.

HCLKBIBUF

ACT1, ACT2, ACT3, 3200DX, 42MX, 54SX, 54SX-A, Axcelerator



Function

Bidirectional with input dedicated to hardwired clock network

HCLKs (hardwired clocks) can drive only the CLK pins of the dedicated R-Cells, RAM Clock Pins (Read and Write) and IO-REG Clock Pins. The HCLKs cannot drive any other pins of R-Cells, or any pins of C-cells; this rules out CC-Flipflops as well.

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

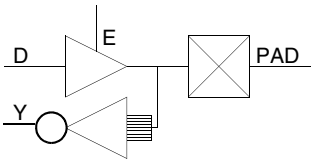
Input	Output
D, E, PAD	PAD, Y

Family	Modules	
	Seq	I/O
All listed		1

NOTE: Refer to the device-specific datasheet for more Clock Network information.

CLKBIBUFI

SX-A, SX-S



Function

Biderctional with inverted Input Dedicated to routed Clock Network

The CLKBIBUFI macro is intended for the SX72-A and SX72-S devices.

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	1
X	0	1	0
0	1	0	1
1	1	1	0

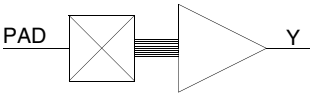
Input	Output
D, E, PAD	PAD, Y

Family	Modules	
	Seq	I/O
SX-A, SX-S		1

NOTE: Refer to the device-specific datasheet for more Clock Network information.

CLKBUF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

Input	Output
PAD	Y

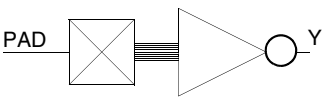
Family	Modules	
	Seq	I/O
All		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

CLKBUFI

SX, SX-A, SX-S, eX



Function

Inverting Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	1
1	0

Input	Output
PAD	Y

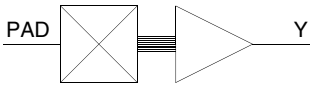
Family	Modules	
	Seq	I/O
SX, SX-A, SX-S, eX		1

NOTE 1: For an internal Clock net, refer to the CLKINTI macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

HCLKBUF

ACT 3, SX, SX-A, SX-S, eX, Axcelerator



Function

Dedicated high-speed S-Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

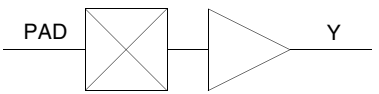
Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
All listed		1

NOTE: Refer to Actel's Databook for more Clock Network information.

INBUF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Input Buffer

Truth Table

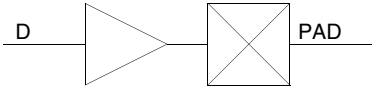
PAD	Y
0	0
1	1

Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
All listed		1

OUTBUF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Function

Output Buffer, High Slew

Truth Table

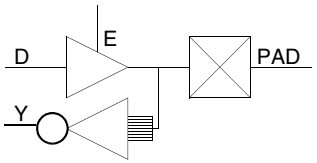
D	PAD
0	0
1	1

Input	Output
D	PAD

Family	Modules	
	Seq	I/O
All		1

QCLKBIBUFI

SX-A, SX-S



Function

Biderctional with inverted Input Dedicated to routed Clock Network

The QCLKBIBUFI macro is intended for the SX72-A and SX72-S devices.

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	1
X	0	1	0
0	1	0	1
1	1	1	0

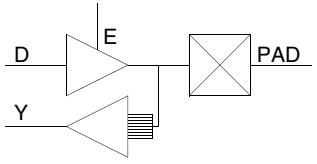
Input	Output
D, E, PAD	PAD, Y

Family	Modules	
	Seq	I/O
SX-A, SX-S		1

NOTE: Refer to Actel's Databook for more Clock Network information.

QCLKBIBUF

SX-A, SX-S



Function

Biderctional with Input Dedicated to routed Clock Network

The QCLKBIBUF macro is intended for the SX72-A and SX72-S devices.

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

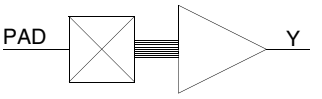
Input	Output
D, E, PAD	PAD, Y

Family	Modules	
	Seq	I/O
SX-A, SX-S		1

NOTE: Refer to Actel's Databook for more Clock Network information.

QCLKBUF

3200DX, MX , SX-A, SX-S



Function

Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

Input	Output
PAD	Y

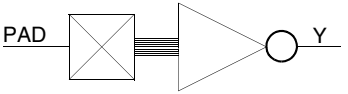
Family	Modules	
	Seq	I/O
All listed		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

QCLKBUFI

SX-A, SX-S



Function

Inverted Input for Dedicated Routed Clock Network

The QCLKBUFI macro is intended for the SX72-A and SX72-S devices.

Truth Table

PAD	Y
0	1
1	0

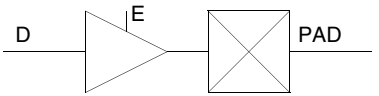
Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
SX-A, SX-S		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

TRIBUFF



Function

Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

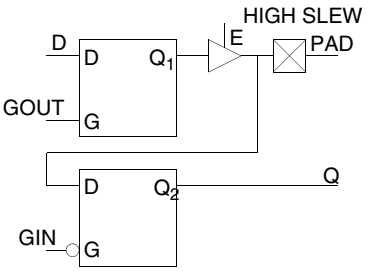
Input	Output
D, E	PAD

Family	Modules	
	Seq	I/O
All		1

NOTE: Refer to Actel's Databook for internal tristate implementation using multiplexers.

BBDLHS

ACT 2, 3200DX, MX



Function

Bidirectional with Input Latch and Output Latch

Truth Table

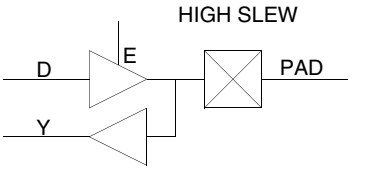
MODE	E	GOUT	GIN	PAD	Q
OUTPUT	1	0	1	PAD_{n-1}	Q_{n-1}
	1	1	0	D	D
INPUT	0	X	1	X	Q_{n-1}
	0	X	0	X	PAD
TRISTATE	0	X	X	Z	X

Input	Output
D, E, GOUT, GIN, PAD	PAD, Q

Family	Modules	
	Seq	I/O
All listed		1

BBHS

ACT 2, ACT 3, 3200DX, MX



Function

Bidirectional Buffer, High Slew

Truth Table

MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

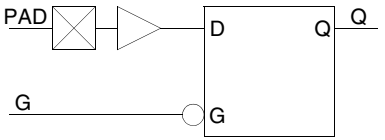
Input	Output
D, E, PAD	PAD, Y

Family	Modules	
	Seq	I/O
All listed		1

NOTE: For new designs, instead of BBHS we recommend that you use “BIBUF” on page 256.

IBDL

ACT 2, 3200DX, MX



Function

Input Buffer with Input Latch, with active low Clock

Truth Table

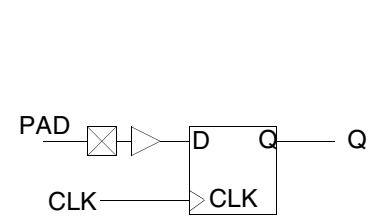
G	Q
1	Q_{n-1}
0	PAD

Input	Output
G, PAD	Q

Family	Modules	
	Seq	I/O
All listed		1

IR

ACT 2, 3200DX, MX



Function

Input Register

Truth Table

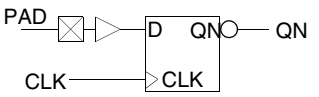
CLK	Q
↑	PAD

Input	Output
PAD, CLK	Q

Family	Modules	
	Seq	I/O
All listed	1	1

IRI

ACT 2, 3200DX, MX



Function

Input register with active Low output

Truth Table

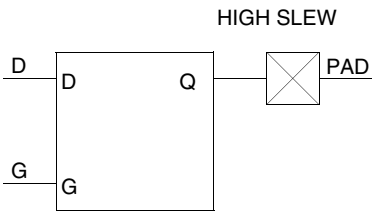
CLK	QN
↑	!PAD

Input	Output
PAD, CLK	QN

Family	Modules	
	Seq	I/O
All listed	1	1

OBDLHS

ACT 2, 3200DX, MX



Function

Output Buffer with Output Latch, High Slew

Truth Table

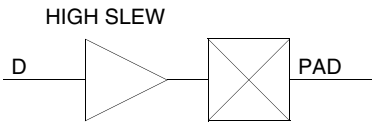
G	PAD
0	PAD_{n-1}
1	D

Input	Output
D, G	PAD

Family	Modules	
	Seq	I/O
All listed		1

OBHS

ACT 2, ACT 3, 3200DX, MX



Function

Output Buffer, High Slew

Truth Table

D	PAD
0	0
1	1

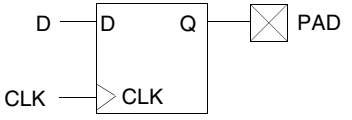
Input	Output
D	PAD

Family	Modules	
	Seq	I/O
All listed		1

NOTE: For new designs, instead of OBHS we recommend that you use “OUTBUF” on page 260.

ORH

ACT 2, 3200DX, MX



Function

Output Register, High Slew

Truth Table

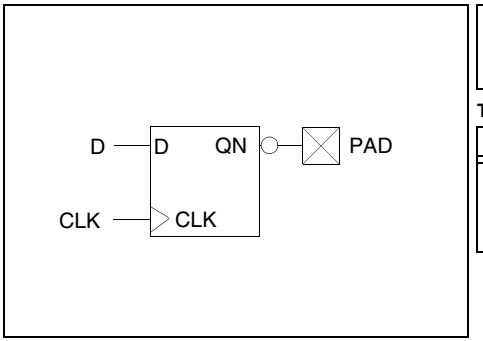
CLK	PAD_{n+1}
↑	D

Input	Output
D, CLK	PAD

Family	Modules	
	Seq	I/O
All listed	1	1

ORIH

ACT 2, 3200DX, MX



Function

Inverted Output Register, High Slew

Truth Table

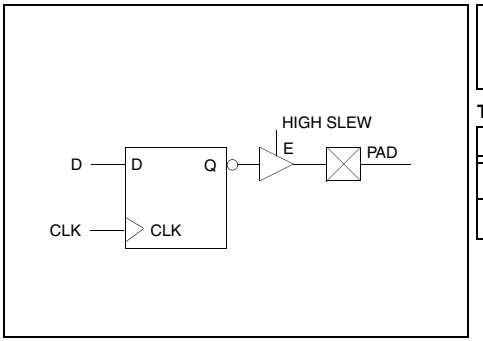
CLK	PAD_{n+1}
↑	!D

Input	Output
D, CLK	PAD

Family	Modules	
	Seq	I/O
All listed	1	1

ORITH

ACT 2, 3200DX, MX



Function

Inverted Output Register, Tristate Enable, High Slew

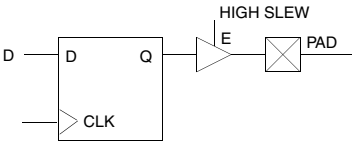
Truth Table

E	CLK	PAD_{n+1}
0	X	Z
1	↑	!D

Input	Output
D, E, CLK	PAD

Family	Modules	
	Seq	I/O
All listed	1	1

ORTH



Function

Output Register, Tristate Enable, High Slew

Truth Table

E	CLK	PAD_{n+1}
0	X	Z
1	↑	D

Input

D, E, CLK

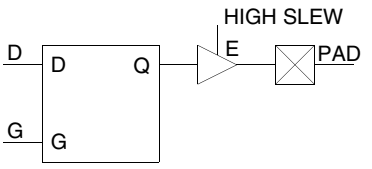
Output

PAD

Family	Modules	
	Seq	I/O
All listed	1	1

TBDLHS

ACT 2, 3200DX, MX



Function

Tristate Output with Latch, High Slew

Truth Table

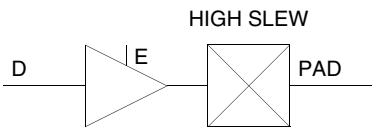
E	G	PAD
0	X	Z
1	1	D
1	0	PAD_{n-1}

Input	Output
D, E, G	PAD

Family	Modules	
	Seq	I/O
All listed		1

TBHS

ACT 2, ACT 3, 3200DX, MX



Function

Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

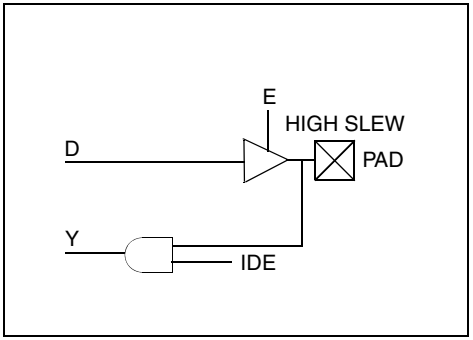
Input	Output
D, E	PAD

Family	Modules	
	Seq	I/O
All listed		1

NOTE: For new designs, instead of TBHS we recommend that you use “TRIBUFF” on page 263.

BBHSA

ACT 3



Function

Bidirectional buffer with AND gate, High Slew

Truth Table

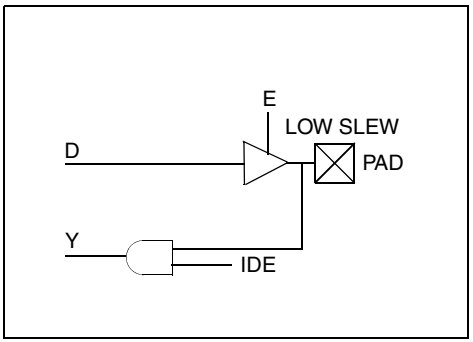
MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

Input	Output
D, E, IDE, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BBLSA

ACT 3



Function

Bidirectional buffer with AND gate, Low Slew

Truth Table

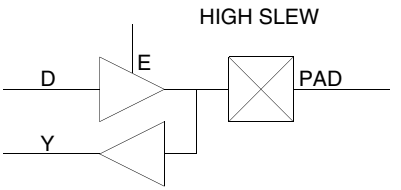
MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

Input	Output
D, E, IDE, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BBUFTH

ACT 3



Function

Bidirectional Buffer, Tristate Enable, High Slew

Truth Table

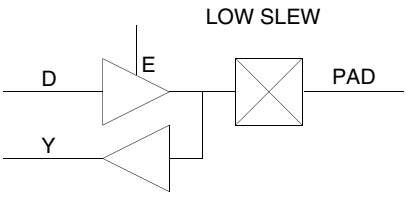
MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Input	Output
D, E, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BBUFTL

ACT 3



Function

Bidirectional Buffer, Tristate Enable, Low Slew

Truth Table

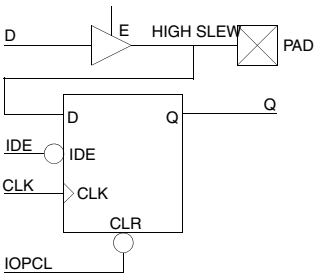
MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Input	Output
D, E, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BIECTH

ACT 3



Function

Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, High Slew

Truth Table

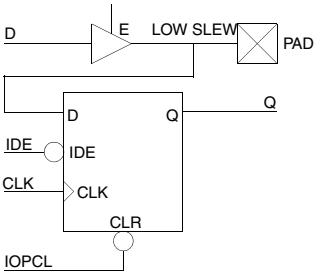
MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q_{n-1}
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q_{n-1}

Input	Output
D, E, IDE, CLK, IOPCL, PAD	PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

BIECTL

ACT 3



Function

Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, Low Slew

Truth Table

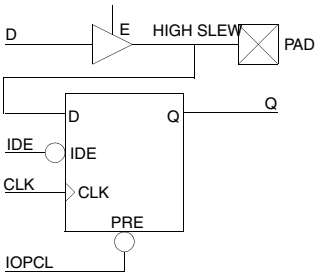
MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q_{n-1}
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q_{n-1}

Input	Output
D, E, IDE, CLK, IOPCL, PAD	PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

BIEPTH

ACT 3



Function

Bidirectional Input Register with Preset, Input Data Enable, Tristate Enable, High Slew

Truth Table

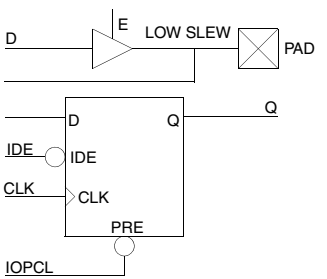
MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q_{n-1}
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q_{n-1}

Input	Output
D, E, IDE, CLK, IOPCL, PAD	PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

BIEPTL

ACT 3



Function

Bidirectional Input Register with Preset, Input Data Enable, Tristate Enable, Low Slew

Truth Table

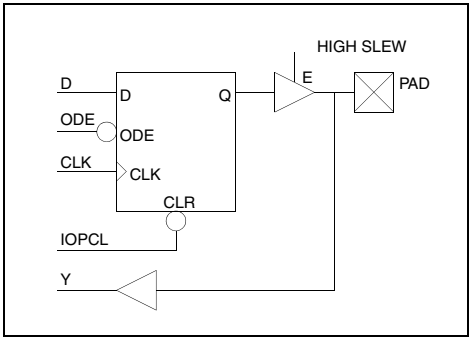
MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q_{n-1}
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q_{n-1}

Input	Output
D, E, IDE, CLK, IOPCL, PAD	PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

BRECTH

ACT 3



Function

Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

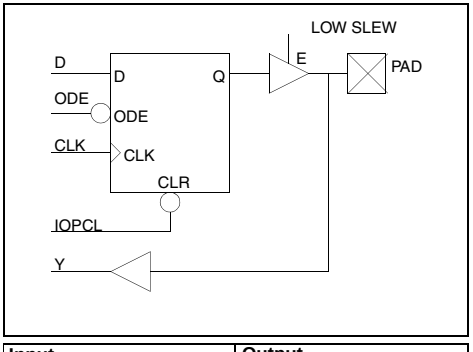
MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD_{n-1}	Y_{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BRECTL

ACT 3



Function

Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

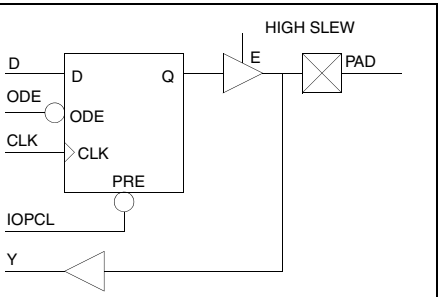
MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD_{n-1}	Y_{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BREPTH

ACT 3



Function

Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

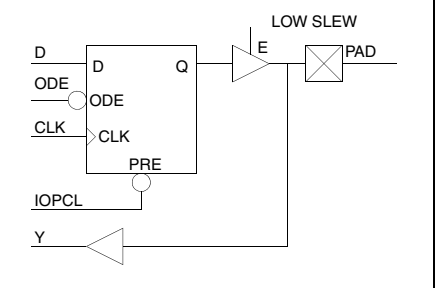
MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD_{n-1}	Y_{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BREPTL

ACT 3



Function

Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

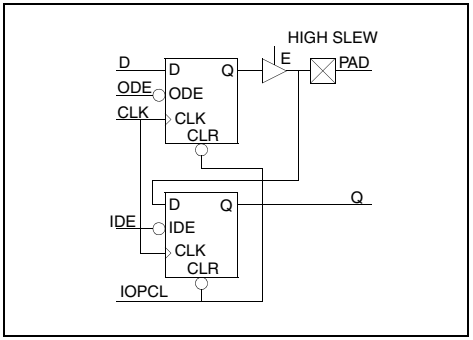
MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD_{n-1}	Y_{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

DECETH

ACT 3



Function

Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

Input	Output
D, E, IDE, CLK, IOPCL, PAD, ODE	PAD, Q

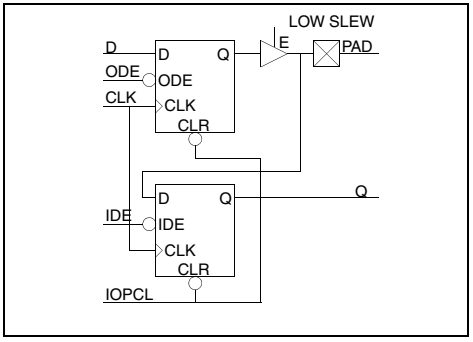
Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD_{n-1}	Q_{n-1}
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q_{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

DECETL

ACT 3



Function

Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

Input	Output
D, E, ODE, CLK, IOPCL, IDE, PAD	PAD, Q

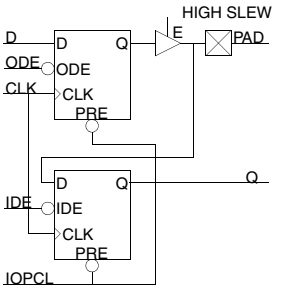
Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD_{n-1}	Q_{n-1}
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q_{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

DEPETH

ACT 3



Function

Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

Input	Output
D, E, ODE, CLK, IOPCL, IDE, PAD	PAD, Q

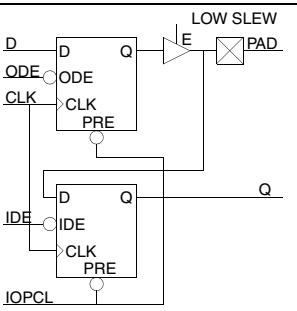
Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD_{n-1}	Q_{n-1}
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q_{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

DEPETL

ACT 3



Function

Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

Input	Output
D, E, ODE, CLK, IOPCL, IDE, PAD	PAD, Q

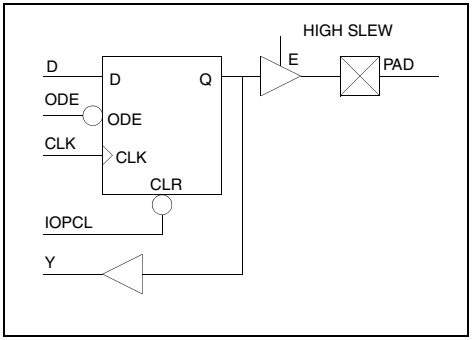
Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD_{n-1}	Q_{n-1}
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q_{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

FECTH

ACT 3



Function

Output Register with feedback, Clear, Output Data Enable, Tristate Enable, High Slew

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

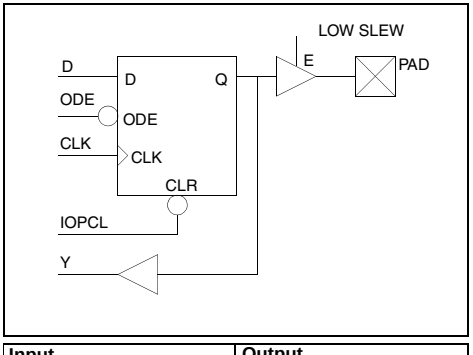
Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	PAD_{n-1}
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

FECTL

ACT 3



Function

Output Register with feedback, Clear, Output Data Enable, Tristate Enable, Low Slew

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

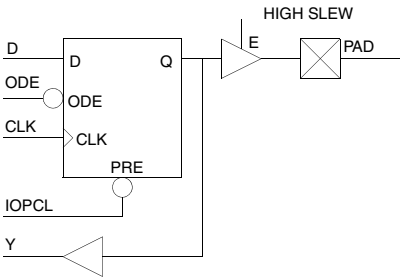
Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	PAD_{n-1}
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

FEPTH

ACT 3



Function

Output Register with feedback, Preset, Output Data Enable, Tristate Enable, High Slew

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

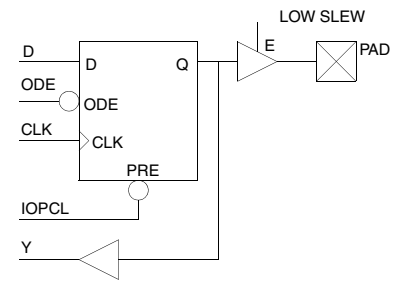
Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	PAD_{n-1}
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

FEPTL

ACT 3



Function

Output Register with feedback, Preset, Output Data Enable, Tristate Enable, Low Slew

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

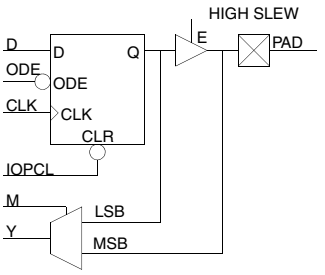
Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	PAD_{n-1}
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

FECTMH

ACT 3



Function

Output Register with Muxed Feedback, Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	X	PAD_{n-1}	X	Y_{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

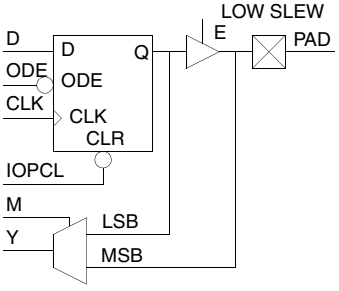
Input	Output
D, E, ODE, CLK, IOPCL, PAD, M	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

FECTML

ACT 3



Function

Output Register with Muxed Feedback, Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	X	PAD_{n-1}	X	Y_{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

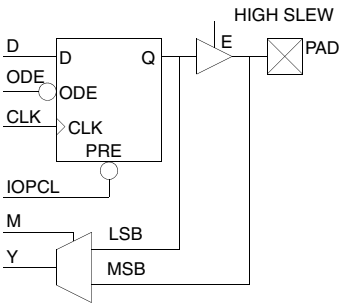
Input	Output
D, E, ODE, CLK, IOPCL, PAD, M	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

FEPTMH

ACT 3



Function

Output Register with Muxed Feedback, Preset, Output Data Enable, Tristate Enable, High Slew

Input	Output
D, E, ODE, CLK, IOPCL, PAD, M	PAD, Y

Truth Table [1]

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	X	PAD_{n-1}	X	Y_{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

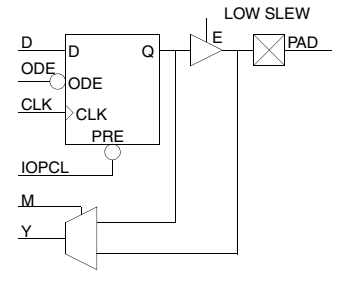
Family	Modules	
	Seq	I/O
ACT 3		1

1.NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

FEPTML

ACT 3



Function

Output Register with Muxed Feedback, Preset, Output Data Enable, Tristate Enable, Low Slew

Input	Output
D, E, ODE, CLK, IOPCL, PAD, M	PAD, Y

Truth Table [1]

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	X	PAD_{n-1}	X	Y_{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

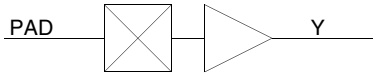
Family	Modules	
	Seq	I/O
ACT 3		1

1.NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

IBUF

ACT 3



Function

Input Buffer

Truth Table

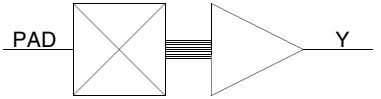
PAD	Y
0	0
1	1

Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
ACT 3		1

IOCLKBUF

ACT 3



Function

Dedicated I/O Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

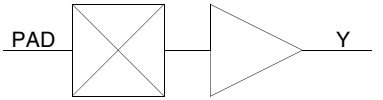
Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: Refer to Actel's Databook for more Clock Network information.

IOPCLBUF

ACT 3



Function

Dedicated I/O Preset Clear Buffer

Truth Table

PAD	Y
0	0
1	1

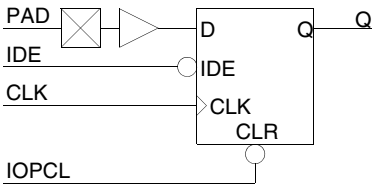
Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: Refer to Actel's Databook for more Clock Network information.

IREC

ACT 3



Function

Input Register, with Clear, Input Data Enable

Truth Table

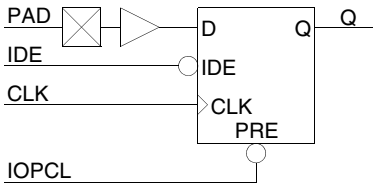
IOPCL	IDE	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	PAD

Input	Output
PAD, IDE, CLK, IOPCL	Q

Family	Modules	
	Seq	I/O
ACT 3		1

IREP

ACT 3



Function

Input Register, with Preset, Input Data Enable

Truth Table

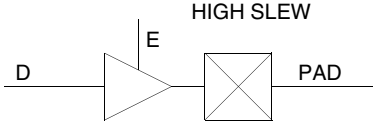
IOPCL	IDE	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	PAD

Input	Output
PAD, IDE, CLK, IOPCL	Q

Family	Modules	
	Seq	I/O
ACT 3		1

OBUFTH

ACT 3



Function

Output Buffer, Tristate Enable, High Slew

Truth Table

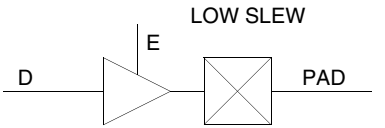
D	E	PAD
X	0	Z
0	1	0
1	1	1

Input	Output
D, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OBUFTL

ACT 3



Function

Output Buffer, Tristate Enable, Low Slew

Truth Table

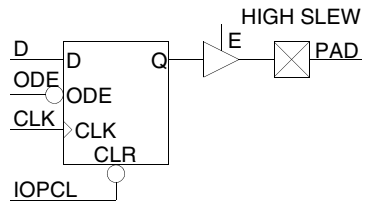
D	E	PAD
X	0	Z
0	1	0
1	1	1

Input	Output
D, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ORECTH

ACT 3



Function

Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

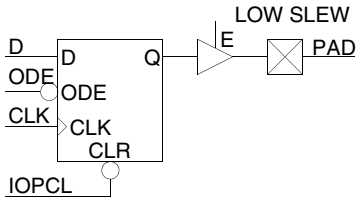
IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

Input	Output
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ORECTL

ACT 3



Function

Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

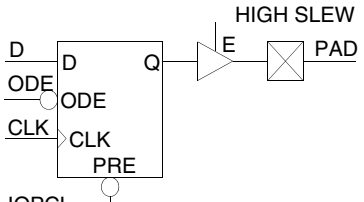
IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

Input	Output
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OREPTH

ACT 3



Function

Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

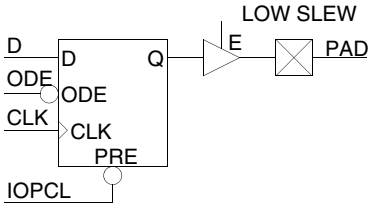
IOPCL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

Input	Output
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OREPTL

ACT 3



Function

Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

Input	Output
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

Axcelerator Input IO Macros

Names for the input buffers are composed of up to 4 parts:

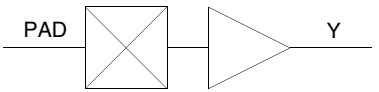
- A base name indicating the type of buffer :INBUF
- IO Technology like LVCMOS
- An optional number code 33,25,18 or 15 indicating a 3.3, 2.5, 1.8 OR 1.5 voltage level.
- An optional one character code (U/D) designating a pull-up/down resistor. When the buffer has no resistor, this code is omitted.

For Example:

- INBUF_LVCMOS25U - An input LVCMOS buffer with 2.5 CMOS voltage levels, pull-up resistor.
- INBUF_PCIX - An input PCIX buffer

INBUF_X

Axcelerator



Function
Global Input Buffer

Truth Table

PAD	Y
0	0
1	1

Input
PAD

Output
Y

Family

Family	Modules	
	Seq	I/O
All listed		1

Available INBUF_X Macro Types

Name	Description
INBUF	LVTTL Input buffer with 3.3v voltage level
INBUF_LVCMOS25	LVCMOS Input buffer with 2.5 CMOS voltage level
INBUF_LVCMOS25U	LVCMOS Input buffer with 2.5 CMOS voltage level, pull-up resistor
INBUF_LVCMOS25D	LVCMOS Input buffer with 2.5 CMOS voltage level, pull-down resistor
INBUF_LVCMOS18	LVCMOS Input buffer with 1.8 CMOS voltage level
INBUF_LVCMOS18U	LVCMOS Input buffer with 1.8 CMOS voltage level, pull-up resistor
INBUF_LVCMOS18D	LVCMOS Input buffer with 1.8 CMOS voltage level, pull-down resistor
INBUF_LVCMOS15	LVCMOS Input buffer with 1.5 CMOS voltage level
INBUF_LVCMOS15U	LVCMOS Input buffer with 1.5 CMOS voltage level, pull-up resistor
INBUF_LVCMOS15D	LVCMOS Input buffer with 1.5 CMOS voltage level, pull-down resistor
INBUF_PCI	PCI Input buffer
INBUF_PCIX	PCIX Input buffer
INBUF_GTLP25	GTLP Input buffer with 3.3 CMOS voltage level
INBUF_GTLP33	GTLP Input buffer with 2.5 CMOS voltage level
INBUF_ HSTL _I	HSTL Class I Input buffer
INBUF_SSTL2_I	SSTL2 Class I Input buffer
INBUF_SSTL2_II	SSTL2 Class II Input buffer
INBUF_SSTL3_I	SSTL3 Class I Input buffer
INBUF_SSTL3_II	SSTL3 Class II Input buffer

Bi-Directional IO Macros

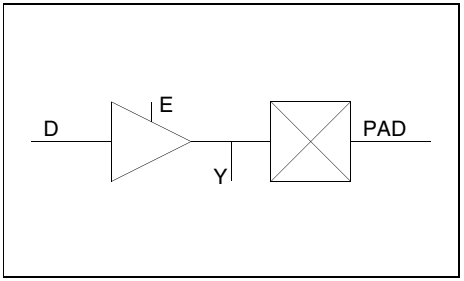
Names for the bi-directional buffers are composed of up to 4 parts:

- A base name indicating the type of buffer :BIBUF
- Optional IO Technology like LVCMOS
- An optional number code 8,12,16,24 indicating 1x, 2x, 3x or 4x-drive strength.
- An optional one character code (S/F) indicating high(F) slew or low(S) slew
- An optional one character code (U/D) designating a pull-up/down resistor. When the buffer has no resistor, this code is omitted.

For Example:

- BIBUF_LVCMOS25 - A bi-directional LVCMOS buffer with 2.5 CMOS voltage levels, pull-up resistor
- BIBUF_S_8- A bi-directional buffer with low slew and 1x drive strength

BIBUF_X



Function
Bidirectional Buffer, High Slew (with Hidden Buffer at Y pin)

Truth Table

MODE	E	D	PAD	Y
OUTPUT	1	X	D	D
INPUT	0	X	X	PAD

Family

Family	Modules	
	Seq	I/O
All		1

Input
D, E, PAD

Output
Y, PAD

Available BIBUF_X Macro Types

Name	Description
BIBUF_LVCMOS25	LVCMOS Bi-directional buffer with 2.5 CMOS voltage level
BIBUF_LVCMOS25U	LVCMOS Bi-directional buffer with 2.5 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS25D	LVCMOS Bi-directional buffer with 2.5 CMOS voltage level, pull-down resistor
BIBUF_LVCMOS18	LVCMOS Bi-directional buffer with 1.8 CMOS voltage level
BIBUF_LVCMOS18U	LVCMOS Bi-directional buffer with 1.8 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS18D	LVCMOS Bi-directional buffer with 1.8 CMOS voltage level, pull-down resistor
BIBUF_LVCMOS15	LVCMOS Bi-directional buffer with 1.5 CMOS voltage level
BIBUF_LVCMOS15U	LVCMOS Bi-directional buffer with 1.5 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS15D	LVCMOS Bi-directional buffer with 1.5 CMOS voltage level, pull-down resistor
BIBUF_PCI	PCI Bi-directional buffer
BIBUF_PCIX	PCIX Bi-directional buffer
BIBUF_GTLP25	GTLP Bi-directional buffer with 2.5 CMOS voltage level
BIBUF_GTLP33	GTLP Bi-directional buffer with 3.3 CMOS voltage level
BIBUF_F_8	Bi-directional buffer with high slew and 1x drive strength
BIBUF_F_8U	Bi-directional buffer with high slew and 1x drive strength, pull-up resistor
BIBUF_F_8U	Bi-directional buffer with high slew and 1x drive strength, pull-down resistor
BIBUF_F_12	Bi-directional buffer with high slew and 2x drive strength
BIBUF_F_12U	Bi-directional buffer with high slew and 2x drive strength, pull-up resistor
BIBUF_F_12D	Bi-directional buffer with high slew and 2x drive strength, pull-down resistor
BIBUF_F_16	Bi-directional buffer with high slew and 3x drive strength
BIBUF_F_16U	Bi-directional buffer with high slew and 3x drive strength, pull-up resistor
BIBUF_F_16D	Bi-directional buffer with high slew and 3x drive strength, pull-down resistor
BIBUF_F_24	Bi-directional buffer with high slew and 4x drive strength
BIBUF_F_24U	Bi-directional buffer with high slew and 4x drive strength, pull-up resistor
BIBUF_F_24D	Bi-directional buffer with high slew and 4x drive strength, pull-down resistor
BIBUF_S_8	Bi-directional buffer with low slew and 1x drive strength
BIBUF_S_8U	Bi-directional buffer with low slew and 1x drive strength, pull-up resistor
BIBUF_S_8U	Bi-directional buffer with low slew and 1x drive strength, pull-down resistor
BIBUF_S_12	Bi-directional buffer with low slew and 2x drive strength
BIBUF_S_12U	Bi-directional buffer with low slew and 2x drive strength, pull-up resistor
BIBUF_S_12D	Bi-directional buffer with low slew and 2x drive strength, pull-down resistor
BIBUF_S_16	Bi-directional buffer with low slew and 3x drive strength
BIBUF_S_16U	Bi-directional buffer with low slew and 3x drive strength, pull-up resistor
BIBUF_S_16D	Bi-directional buffer with low slew and 3x drive strength, pull-down resistor
BIBUF_S_24	Bi-directional buffer with low slew and 4x drive strength
BIBUF_S_24U	Bi-directional buffer with low slew and 4x drive strength, pull-up resistor
BIBUF_S_24D	Bi-directional buffer with low slew and 4x drive strength, pull-down resistor

Name	Description
BIBUF_SSTL2_I	SSTL2 Class I Bi-directional buffer with 2.5V CMOS Voltage Level
BIBUF_SSTL2_II	SSTL2 Class II Bi-directional buffer with 2.5V CMOS Voltage Level
BIBUF_SSTL3_I	SSTL3 Class I Bi-directional buffer with 3.3V CMOS Voltage Level
BIBUF_SSTL3_II	SSTL3 Class II Bi-directional buffer with 3.3V CMOS Voltage Level
BIBUF_HSTL_I	HSTL Class I Bi-directional buffer with 1.5V CMOS Voltage Level

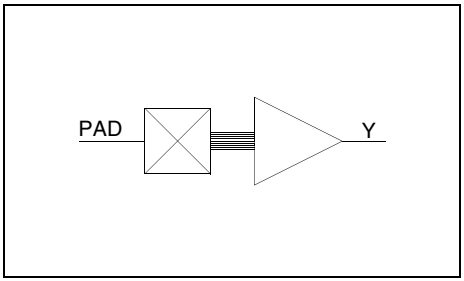
Clock Buffers

Names for the input buffers are composed of up to 3 parts:

- A base name indicating the type of buffer :CLKBUF
- IO Technology like LVCMOS
- An optional number code 33,25,18 or 15 indicating a 3.3,2.5, 1.8 OR 1.5 voltage level

CLKBUF_X

Axcelerator



Function
Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

Input
PAD

Output
Y

Family

Family	Modules	
	Seq	I/O
All		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

Available CLKBUF_X Macro Types

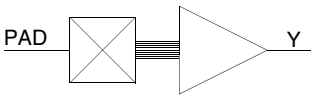
Name	Description
CLKBUF_LVCMOS25	LVCMOS Clock buffer with 2.5 CMOS voltage level
CLKBUF_LVCMOS18	LVCMOS Clock buffer with 1.8 CMOS voltage level
CLKBUF_LVCMOS15	LVCMOS Clock buffer with 1.5 CMOS voltage level
CLKBUF_PCI	PCI Clock buffer
CLKBUF_PCIX	PCIX Clock buffer
CLKBUF_GTLP25	GTLP Clock buffer with 2.5 CMOS voltage level
CLKBUF_GTLP33	GTLP Clock buffer with 3.3 CMOS voltage level
CLKBUF_ HSTL _I	HSTL Class I Clock buffer
CLKBUF_SSTL2_I	SSTL2 Class I Clock buffer
CLKBUF_SSTL2_II	SSTL2 Class II Clock buffer
CLKBUF_SSTL3_I	SSTL3 Class I Clock buffer
CLKBUF_SSTL3_II	SSTL3 Class II Clock buffer

HClock Buffers

Naming convention is identical to the naming for Clock Buffers.

HCLKBUF_X

Axcelerator



Function
Dedicated high-speed S-Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

Input
PAD

Output
Y

Family

Family	Modules	
	Seq	I/O
All		1

NOTE 1: Refer to Actel's Databook for more Clock Network information.

Available HCLKBUF_X Macro Types

Name	Description
HCLKBUF_LVCMOS25	LVCMOS Clock buffer with 2.5 CMOS voltage level
HCLKBUF_LVCMOS18	LVCMOS Clock buffer with 1.8 CMOS voltage level
HCLKBUF_LVCMOS15	LVCMOS Clock buffer with 1.5 CMOS voltage level
HCLKBUF_PCI	PCI Clock buffer
HCLKBUF_PCIX	PCIX Clock buffer
HCLKBUF_GTLP25	GTLP Clock buffer with 2.5 CMOS voltage level
HCLKBUF_GTLP33	GTLP Clock buffer with 3.3 CMOS voltage level
HCLKBUF_ HSTL _I	HSTL Class I Clock buffer
HCLKBUF_SSTL2_I	SSTL2 Class I Clock buffer
HCLKBUF_SSTL2_II	SSTL2 Class II Clock buffer
HCLKBUF_SSTL3_I	SSTL3 Class I Clock buffer
HCLKBUF_SSTL3_II	SSTL3 Class II Clock buffer

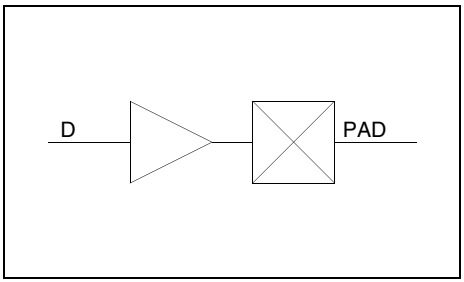
Output Buffers

Names for the bi-directional buffers are composed of up to 4 parts:

- A base name indicating the type of buffer :OUTBUF
- Optional IO Technology like LVCMOS
- An optional number code 8,12,16,24 indicating 1x, 2x, 3x or 4x-drive strength.
- An optional one character code (S/F) indicating high(F) slew or low(S) slew

OUTBUF_X

Axcelerator



Function
Output Buffer, High Slew

Truth Table

D	PAD
0	0
1	1

Input
D

Output
PAD

Family

Family	Modules	
	Seq	I/O
All		1

Available OUTBUF_X Macro Types

Name	Description
OUTBUF_LVCMOS25	LVCMOS Output buffer with 2.5 CMOS voltage level
OUTBUF_LVCMOS18	LVCMOS Output buffer with 1.8 CMOS voltage level
OUTBUF_LVCMOS15	LVCMOS Output buffer with 1.5 CMOS voltage level
OUTBUF_PCI	PCI Output buffer
OUTBUF_PCIX	PCIX Output buffer
OUTBUF_GTLP25	GTLP Output buffer with 2.5 CMOS voltage level
OUTBUF_GTLP33	GTLP Output buffer with 3.3 CMOS voltage level
OUTBUF_F_8	Output buffer with high slew and 1x drive strength
OUTBUF_F_12	Output buffer with high slew and 2x drive strength
OUTBUF_F_16	Output buffer with high slew and 3x drive strength
OUTBUF_F_24	Output buffer with high slew and 4x drive strength
OUTBUF_S_8	Output buffer with low slew and 1x drive strength
OUTBUF_S_12	Output buffer with low slew and 2x drive strength
OUTBUF_S_16	Output buffer with low slew and 3x drive strength
OUTBUF_S_24	Output buffer with low slew and 4x drive strength
OUTBUF_SSTL2_I	SSTL Class I Output buffer with 2.5V CMOS Voltage Level
OUTBUF_SSTL2_II	SSTL Class II Output buffer with 2.5V CMOS Voltage
OUTBUF_SSTL3_I	SSTL Class I Output buffer with 3.3V CMOS Voltage Level
OUTBUF_SSTL3_II	SSTL Class II Output buffer with 3.3V CMOS Voltage Level
OUTBUF_HSTL_I	HSTL Class I Output buffer with 1.5V CMOS Voltage Level

Tri-State Buffer Macros

Names for the bi-directional buffers are composed of up to 4 parts:

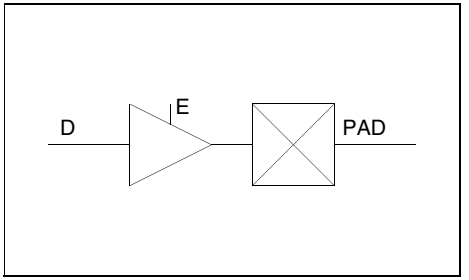
- A base name indicating the type of buffer :TRIBUFF
- Optional IO Technology like LVCMOS
- An optional number code 8,12,16,24 indicating 1x, 2x, 3x or 4x-drive strength.
- An optional one character code (S/F) indicating high(F) slew or low(S) slew
- An optional one character code (U/D) designating a pull-up/down resistor. When the buffer has no resistor, this code is omitted.

For Example:

- TRIBUFF_LVCMOS25 - A bi-directional LVCMOS buffer with 2.5 CMOS voltage levels, pull-up resistor
- TRIBUFF_S_8- A bi-directional buffer with low slew and 1x drive strength

TRIBUFF_X

Axcelerator



Function
Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

Family

Family	Modules	
	Seq	I/O
All		1

Input
D, E

Output
PAD

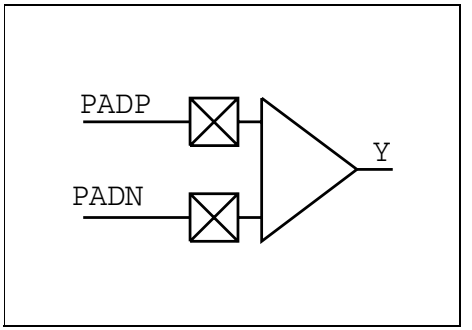
Available TRIBUFF_X Macro Types

Name	Description
TRIBUFF_LVCMOS25	LVCMOS Tri-state buffer with 2.5 CMOS voltage level
TRIBUFF_LVCMOS25U	LVCMOS Tri-state buffer with 2.5 CMOS voltage level, pull-up resistor
TRIBUFF_LVCMOS25D	LVCMOS Tri-state buffer with 2.5 CMOS voltage level, pull-down resistor
TRIBUFF_LVCMOS18	LVCMOS Tri-state buffer with 1.8 CMOS voltage level
TRIBUFF_LVCMOS18U	LVCMOS Tri-state buffer with 1.8 CMOS voltage level, pull-up resistor
TRIBUFF_LVCMOS18D	LVCMOS Tri-state buffer with 1.8 CMOS voltage level, pull-down resistor
TRIBUFF_LVCMOS15	LVCMOS Tri-state buffer with 1.5 CMOS voltage level
TRIBUFF_LVCMOS15U	LVCMOS Tri-state buffer with 1.5 CMOS voltage level, pull-up resistor
TRIBUFF_LVCMOS15D	LVCMOS Tri-state buffer with 1.5 CMOS voltage level, pull-down resistor
TRIBUFF_PCI	PCI Tri-state buffer
TRIBUFF_PCIX	PCIX Tri-state buffer
TRIBUFF_GTLP25	GTLP Tri-state buffer with 2.5 CMOS voltage level
TRIBUFF_GTLP33	GTLP Tri-state buffer with 3.3 CMOS voltage level
TRIBUFF_F_8	Tri-state buffer with high slew and 8 mA drive strength
TRIBUFF_F_8U	Tri-state buffer with high slew and 1x drive strength, pull-up resistor
TRIBUFF_F_8U	Tri-state buffer with high slew and 1x drive strength, pull-down resistor
TRIBUFF_F_12	Tri-state buffer with high slew and 2x drive strength
TRIBUFF_F_12U	Tri-state buffer with high slew and 2x drive strength, pull-up resistor
TRIBUFF_F_12D	Tri-state buffer with high slew and 2x drive strength, pull-down resistor
TRIBUFF_F_16	Tri-state buffer with high slew and 3x drive strength
TRIBUFF_F_16U	Tri-state buffer with high slew and 3x drive strength, pull-up resistor
TRIBUFF_F_16D	Tri-state buffer with high slew and 3x drive strength, pull-down resistor
TRIBUFF_F_24	Tri-state buffer with high slew and 4x drive strength
TRIBUFF_F_24U	Tri-state buffer with high slew and 4x drive strength, pull-up resistor

Name	Description
TRIBUFF_F_24D	Tri-state buffer with high slew and 4x drive strength, pull-down resistor
TRIBUFF_S_8	Tri-state buffer with low slew and 1x drive strength
TRIBUFF_S_8U	Tri-state buffer with low slew and 1x drive strength, pull-up resistor
TRIBUFF_S_8U	Tri-state buffer with low slew and 1x drive strength, pull-down resistor
TRIBUFF_S_12	Tri-state buffer with low slew and 2x drive strength
TRIBUFF_S_12U	Tri-state buffer with low slew and 2x drive strength, pull-up resistor
TRIBUFF_S_12D	Tri-state buffer with low slew and 2x drive strength, pull-down resistor
TRIBUFF_S_16	Tri-state buffer with low slew and 3x drive strength
TRIBUFF_S_16U	Tri-state buffer with low slew and 3x drive strength, pull-up resistor
TRIBUFF_S_16D	Tri-state buffer with low slew and 3x drive strength, pull-down resistor
TRIBUFF_S_24	Tri-state buffer with low slew and 4x drive strength
TRIBUFF_S_24U	Tri-state buffer with low slew and 4x drive strength, pull-up resistor
TRIBUFF_S_24D	Tri-state buffer with low slew and 4x drive strength, pull-down resistor
TRIBUFF_SSTL2_I	SSTL2 Class I Tri-state buffer with 2.5V CMOS Voltage Level
TRIBUFF_SSTL2_II	SSTL2 Class II Tri-state buffer with 2.5V CMOS Voltage Level
TRIBUFF_SSTL3_I	SSTL3 Class I Tri-state buffer with 3.3V CMOS Voltage Level
TRIBUFF_SSTL3_II	SSTL3 Class II Tri-state buffer with 3.3V CMOS Voltage Level
TRIBUFF_HSTL_I	HSTL Class I Tri-state buffer with 1.5V CMOS Voltage Level

INBUF_LVDS; INBUF_LVPECL

Axcelerator



Function
INBUF_LVDS and INBUF_LVPECL

Input
PADP; PADN

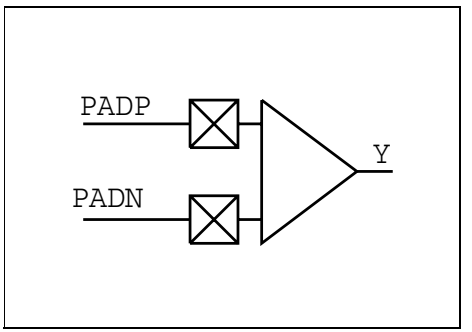
Output
Y

Available Differential Macro Types

Name	Description
INBUF_LVDS	
INBUF_LVPECL	

CLKBUF_LVDS; CLKBUF_LVPECL

Axcelerator



Function
CLKBUF_LVDS and CLKBUF_LVPECL

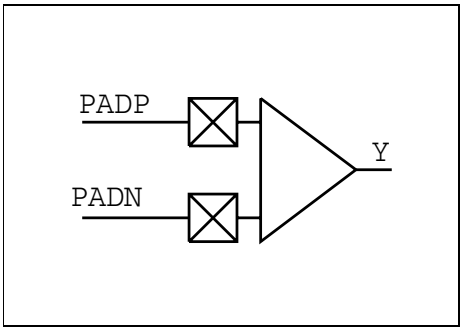
Input
PADP; PADN

Output
Y

Available Differential Macro Types

Name	Description
CLKBUF_LVDS	
CLKBUF_LVPECL	

HCLKBUF_LVDS; HCLKBUF_LVPECL



Function
HCLKBUF_LVDS and HCLKBUF_LVPECL

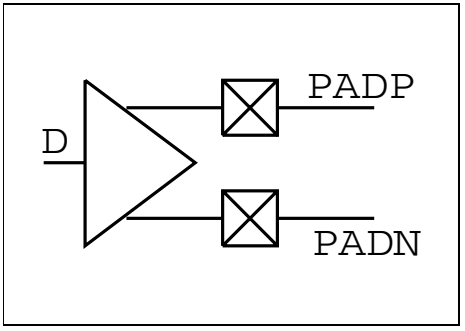
Input
PADP; PADN

Output
Y

Available Differential Macro Types

Name	Description
HCLKBUF_LVDS	
HCLKBUF_LVPECL	

OUTBUF_LVDS; OUTBUF_LVPECL



Function
OUTBUF_LVDS and OUTBUF_LVPECL

Input
D

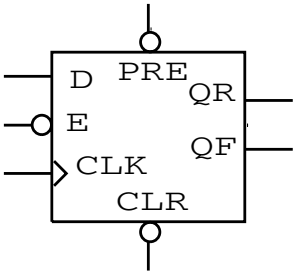
Output
PADP, PADN

Available Differential Macro Types

Name	Description
OUTBUF_LVDS	
OUTBUF_LVPECL	

DDR_REG macro

Axcelerator



Function

DDR (DDR) Register with activelow write and rad enables; please refer to the Axcelerator datasheet for more information on the DDR_REG

Truth Table

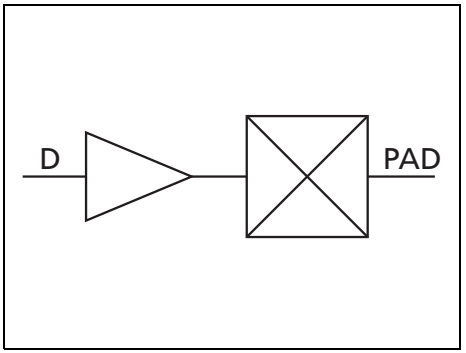
CLR	PRE	E	CLK	QR(n+1)	QF(n+1)
0	X	X	X	0	0
1	0	X	X	1	1
1	1	1	X	QR(n)	QF(n)
1	1	0	↑	D(↑)	X
1	1	0	↓	X	D(↓)

Input

D, CLK, E, PRE, CLR

Output

QR, QF



Function

SIMBUF is a VIRTUAL I/O used to bring out internal nets that are going to be connected to a top port in the design. This port will be used exclusively for simulation. This virtual I/O is removed by Designer during compile, then re-added in the back-annotated netlist.

Truth Table

D	PAD
0	0
1	1

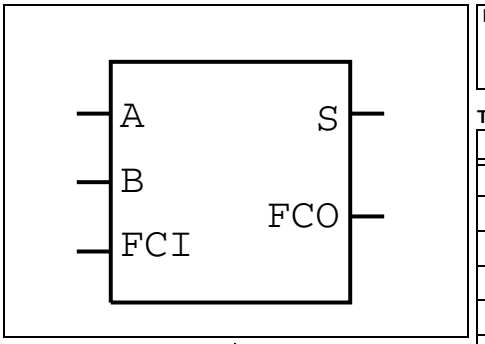
Input
D

Output
PAD

Family	I/O Tiles
All listed	0

Carry Chain Macros

ADD1 Axcelerator



Function

1 Bit Adder

Input
A, B, FCI

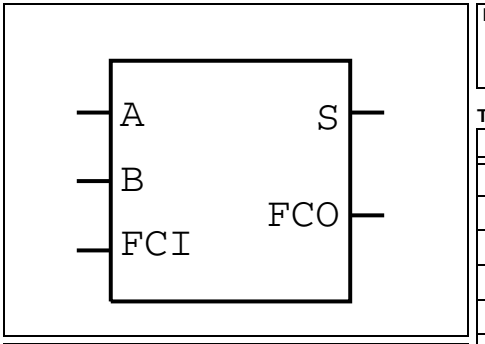
Output
S, FCO

Truth Table

A	B	FCI	S	FCO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Family	Modules
	COMB
All listed	1

SUB1 Axcelerator



Function

1 Bit Subtractor

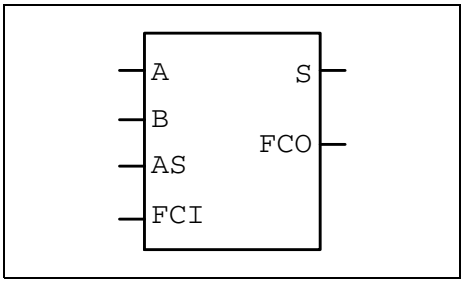
Input
A, B, FCI

Output
S, FCO

Truth Table

A	B	FCI	S	FCO
0	0	0	1	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

Family	Modules
	Comb
All listed	1



Input
AS, B, A, FCI

Output
S, FCO

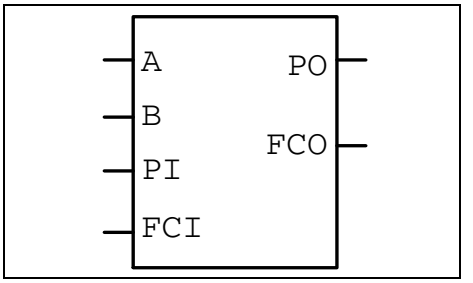
Function
1 Bit Add Sub macro

Truth Table

AS	B	A	FCI	S	FCO
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	1

Family

Family	Modules
	Comb
All listed	2



Input
A, B, PI, FCI

Output
PO, FCO

Function
1 Bit Multiplier

Truth Table

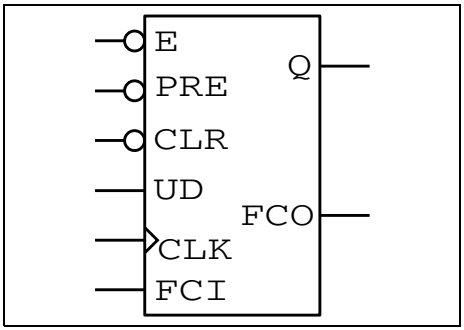
A	B	PI	FCI	PO	FCO
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	1

Family

Family	Modules
	Comb
All listed	1

ARCNTECP1

Axcelerator



Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	Q_n
See Equations		1	1	0	↑	See Equations	

Input
FCI, CLK, PRE, CLR, UD

Output
Q, FCO

$$Q_{n+1} = FCI \wedge UD \wedge Q_n$$

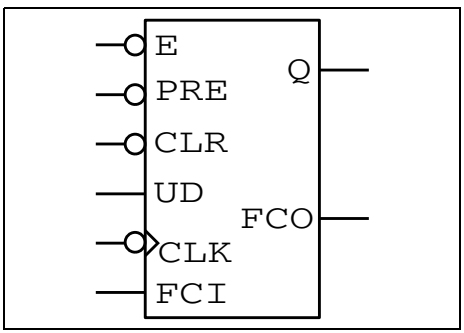
$$FCO = FCI.UD + FCI.Q_n + UD.Q_n$$

Family

Family	Modules	
	Comb	Seq
All listed	1	1

AFCNTECP1

Axcelerator



Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	Q_n
See Equations		1	1	0	↓	See Equations	

Input
FCI, CLK, PRE, CLR, UD

Output
Q, FCO

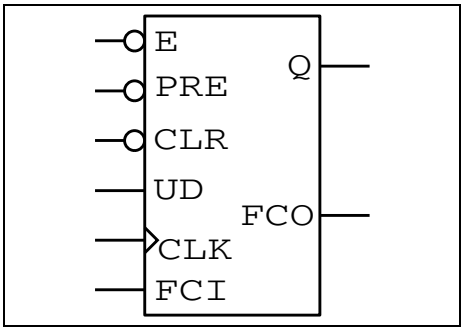
$$Q_{n+1} = FCI \wedge UD \wedge Q_n$$

$$FCO = FCI.UD + FCI.Q_n + UD.Q_n$$

Family

Family	Modules	
	Comb	Seq
All listed	1	1

SRCNTECP1



Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	Q_n
See Equations		1	1	0	↑	See Equations	

$$Q_{n+1} = FCI \wedge !UD \wedge Q_n$$

$$FCO = FCI.!UD + FCI.Q_n + !UD.Q_n$$

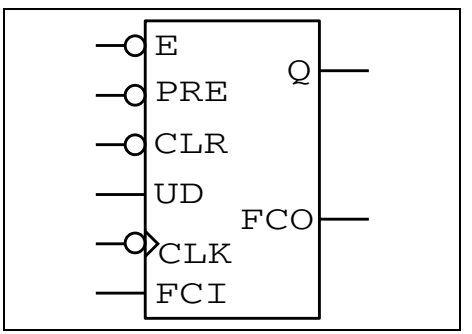
Input
FCI, CLK, PRE, CLR, UD

Output
Q, FCO

Family

Family	Modules	
	Comb	Seq
All listed	1	1

SFCNTECP1



Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	Q_n
See Equations		1	1	0	↓	See Equations	

$$Q_{n+1} = FCI \wedge !UD \wedge Q_n$$

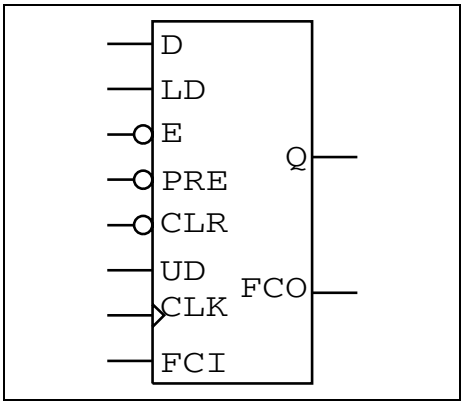
$$FCO = FCI.!UD + FCI.Q_n + !UD.Q_n$$

Input
FCI, CLK, PRE, CLR, UD

Output
Q, FCO

Family

Family	Modules	
	Comb	Seq
All listed	1	1



Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	O_n
X	X	1	1	0	1	0	↑	X	0
X	X	1	1	0	1	1	↑	X	1
See Equations		1	1	0	0	X	↑	See Equations	

Input
FCI, CLK, PRE, CLR, E, LD, D, and UD

Output
Q, FCO

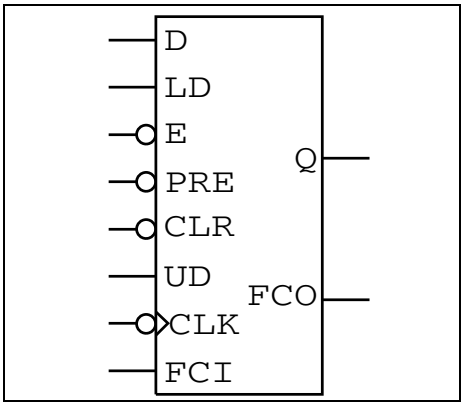
$$Q_{n+1} = FCI \wedge UD \wedge Q_n$$

$$FCO = FCI.UD + FCI.Q_n + UD.Q_n$$

Family

Family	Modules	
	Comb	Seq
All listed	2	1

AFCNTELDCP1



Function
1 Bit counter

Input
FCI, CLK, PRE, CLR, E, LD, D, and UD

Output
Q, FCO

Truth Table

FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	Q_n
X	X	1	1	0	1	0	↓	X	0
X	X	1	1	0	1	1	↓	X	1
See Equations		1	1	0	0	X	↓	See Equations	

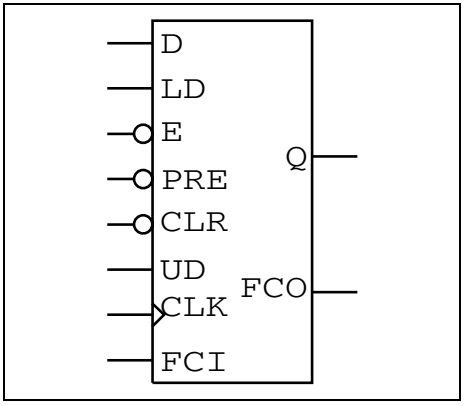
$$Q_{n+1} = FCI \wedge UD \wedge Q_n$$

$$FCO = FCI.UD + FCI.Q_n + UD.Q_n$$

Family

Family	Modules	
	Comb	Seq
All listed	2	1

SRCNTELDCP1



Function
1 Bit counter

Input
FCI, CLK, PRE, CLR, E, LD, D, and UD

Output
Q, FCO

Truth Table

FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	Q_n
X	X	1	1	0	1	0	↑	X	0
X	X	1	1	0	1	1	↑	X	1
See Equations		1	1	0	0	X	↑	See Equations	

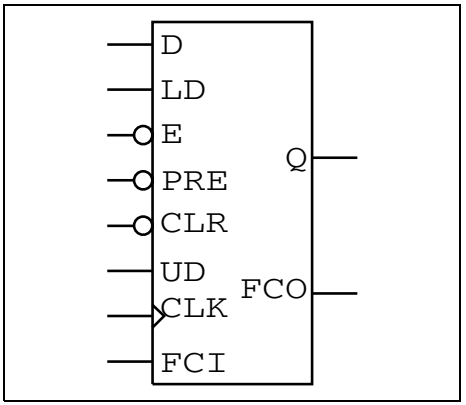
$$Q_{n+1} = FCI \wedge !UD \wedge Q_n$$

$$FCO = FCI.!UD + FCI.Q_n + !UD.Q_n$$

Family

Family	Modules	
	Comb	Seq
All listed	2	1

SFCNTELDCP1



Function
1 Bit counter

Truth Table

FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q_{n+1}
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	Q_n
X	X	1	1	0	1	0	↓	X	0
X	X	1	1	0	1	1	↓	X	1
See Equations		1	1	0	0	X	↓	See Equations	

Input
FCI, CLK, PRE, CLR, E, LD, D, and UD

Output
Q, FCO

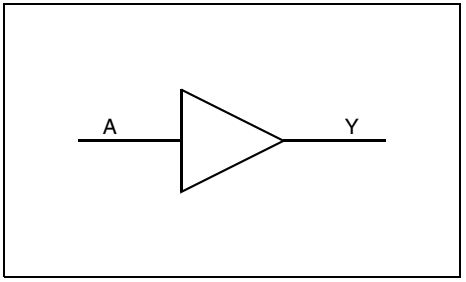
$$Q_{n+1} = FCI \wedge !UD \wedge Q_n$$

$$FCO = FCI.!UD + FCI.Q_n + !UD.Q_n$$

Family

Family	Modules	
	Comb	Seq
All listed	2	1

FCEND_BUFF



Function
Buffer, driven by the FCO pin of the last macro in the Carry-Chain

Truth Table

A	Y
0	0
1	1

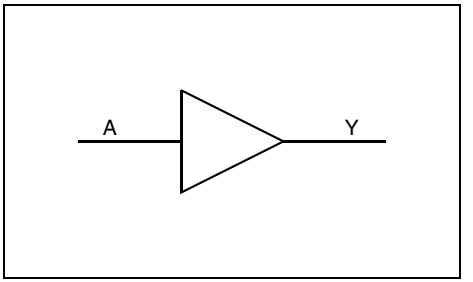
Input
A

Output
Y

Family

Family	Modules	
	Seq	COMB
All		1

FCEND_INV



Function
Inverter with Active Low output; driven by the FCO pin of the last macro in the Carry-Chain

Truth Table

A	Y
0	1
1	0

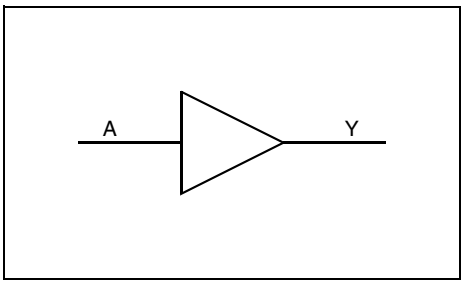
Input
A

Output
Y

Family

Family	Modules	
	Seq	COMB
All		1

FCINIT_BUFF



Function
Buffer, used to initialize the FCI pin of the first macro in the Carry-Chain with an external signal

Truth Table

A	Y
0	0
1	1

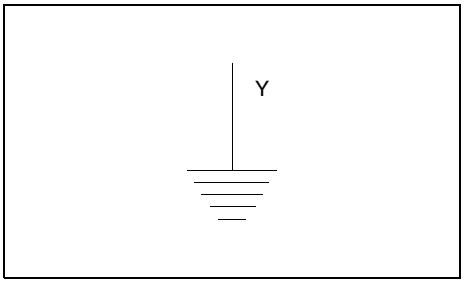
Input
A

Output
Y

Family

Family	Modules	
	Seq	COMB
All		1

FCINIT_GND

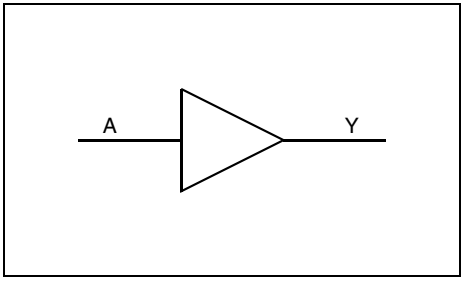


Function
Ground; used to initialize the FCI pin of the first macro in the Carry-Chain to GND

NOTE: Ground does not use any modules

Input	Output
	Y

FCINIT_INV



Function
Inverter with Active Low output; used to initialize the FCI pin of the first macro in the Carry-Chain with an external signal

Input	Output
A	Y

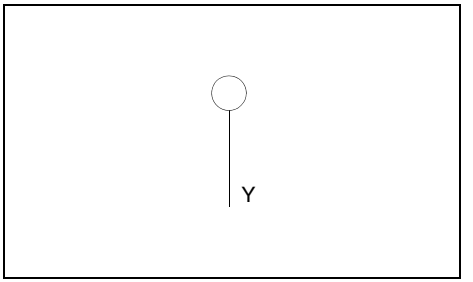
Truth Table

A	Y
0	1
1	0

Family

Family	Modules	
	Seq	COMB
All		1

FCINIT_VCC

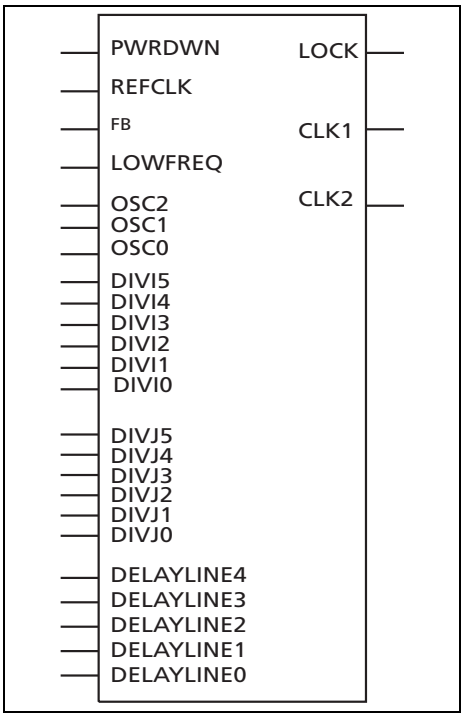


Function
Power; used to initialize the FCI pin of the first macro in the Carry-Chain to VCC

NOTE: VCC does not use any modules

Input	Output
A	Y

PLL Macros



Input
PWRDWN, REFCLK, LOWFREQ, OSC2, OSC1, OSC0, DIVI5, DIVI4, DIVI3, DIVI2, DIVI1, DIVI0, DIVJ5, DIVJ4, DIVJ3, DIVJ2, DIVJ1, DIVJ0, DELAYLINE4, DELAYLINE3, DELAYLINE2, DELAYLINE1, DELAYLINE0

Output
LOCK, CLK1, CLK2

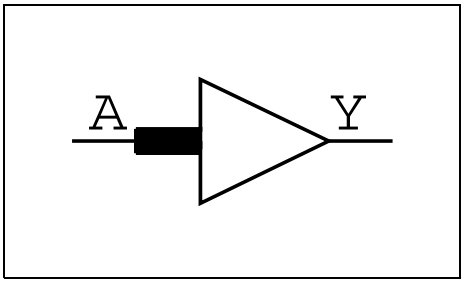
Function
PLL: PLL with internal feedback; PLLFB: PLL with external feedback.
NOTE: PLL and PLLFB are identical except for the FB pin; if you wish to use internal feedback, use the regular PLL.

Actel recommends that you use ACTgen to generate your PLLs; ACTgen calculates the settings for all the pins in the PLL for the required input-output frequency combinations.

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at http://www.actel.com.

PLLINT

Axcelerator



Function
PLL Int

Truth Table

A	Y
0	0
1	1

Input
A

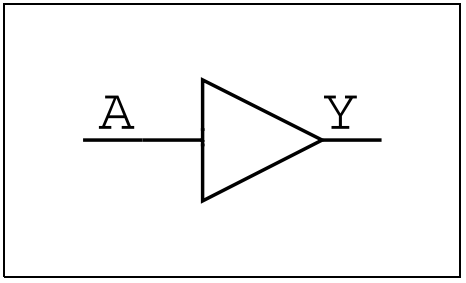
Output
Y

Connect only to the REFCLK input of PLL when the PLL is driven by a pad other than the one in the same super cluster.

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at http://www.actel.com.

PLLOUT

Axcelerator



Function
PLL OUT

Truth Table

A	Y
0	0
1	1

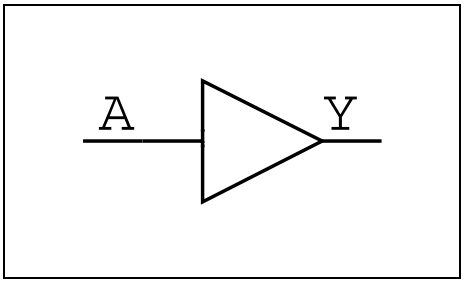
Input
A

Output
Y

Connect only to the CLK output of PLL when the PLL is driving a net other than the HCLK/RCLK networks.

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at http://www.actel.com.

PLLHCLK



Function
PLL HCLK

Truth Table

A	Y
0	0
1	1

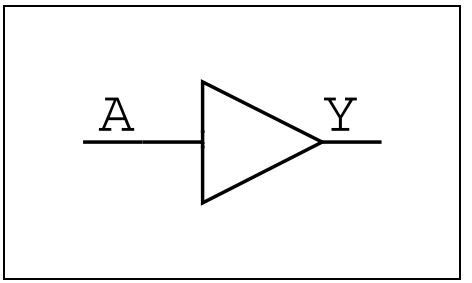
Connect only to the CLK output of the PLL; use it to drive the HCLK network.

Input
A

Output
Y

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at http://www.actel.com.

PLLRCLK



Function
PLL RCLK

Truth Table

A	Y
0	0
1	1

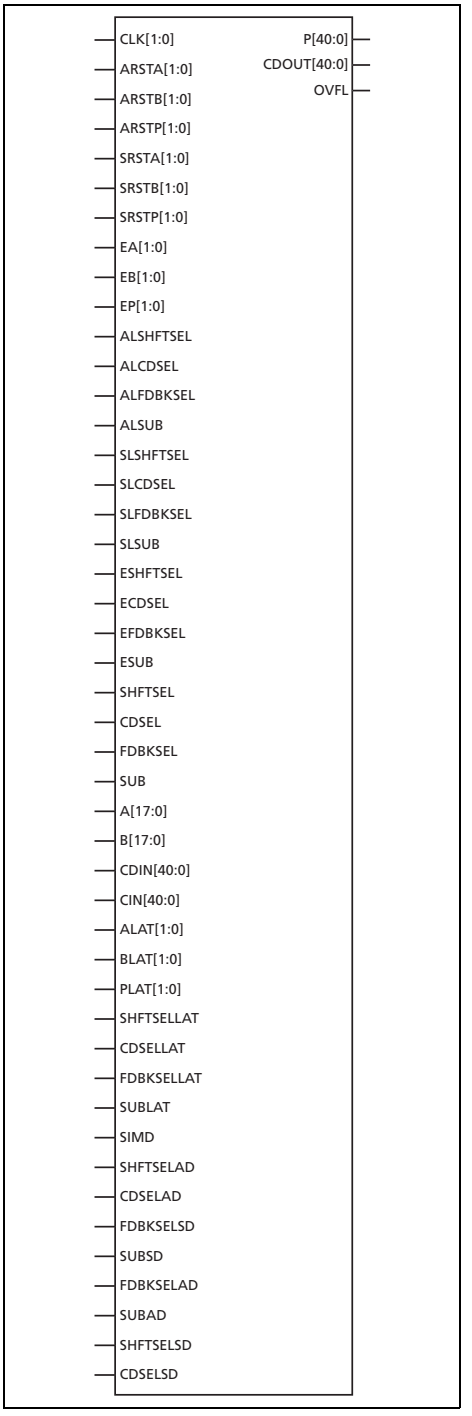
Connect only to the CLK output of the PLL; use it to drive the RCLK network.

Input
A

Output
Y

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at http://www.actel.com.

RTAX-DSP Math Macro



Function

18 bit x 18 bit signed (2's complement) multiply-accumulate MATH block

The MATH block can accumulate the current multiplication product with a previous result, a constant, a dynamic value, or a result from another MATH block. Each MATH block can also be fractured into two 9 bit x 9 bit multipliers. All the signals of the MATH block (except CIN, CDIN and CDOUT) have optional registers.

Major signals are in **bold**.

Table 1. Math18x18 Ports

Port Name	Direction	Type	Polarity	Description
SIMD	Input	Static	High	Single Instruction Multiple Data mode. When SIMD = 1, MATH block is fractured into two 9 bit x 9 bit multipliers When SIMD = 0, it is called the normal mode
CLK[1:0]	Input	Dynamic	Rising edge	Input clocks. • CLK[1] is the clock for A[17:9], B[17:9], P[40:18], OVFL, SHFTSEL, CDSEL, FDBKSEL and SUB registers • CLK[0] is the clock for A[8:0], B[8:0] and P[17:0] In normal mode, ensure CLK[1] = CLK[0]
A[17:0]	Input	Dynamic	High	Input data A
ALAT[1:0]	Input	Static	High	Bypass data A registers • ALAT[1] is for A[17:9]. Connect to 1, if not registered • ALAT[0] is for A[8:0]. Connect to 1, if not registered In normal mode, ensure ALAT[0] = ALAT[1]
ARSTA[1:0]	Input	Dynamic	Low	Asynchronous reset for data A registers. • ARSTA[1] is for A[17:9]. Connect to 1, if not registered • ARSTA[0] is for A[8:0]. Connect to 1, if not registered In normal mode, ensure ARSTA[1] = ARSTA[0]
SRSTA[1:0]	Input	Dynamic	Low	Synchronous reset for data A registers • SRSTA[1] is for A[17:9]. Connect to 1, if not registered • SRSTA[0] is for A[8:0]. Connect to 1, if not registered In normal mode, ensure SRSTA[1] = SRSTA[0]
EA[1:0]	Input	Dynamic	High	Enable for data A registers • EA[1] is for A[17:9]. Connect to 1, if not registered • EA[0] is for A[8:0]. Connect to 1, if not registered In normal mode, ensure EA[1] = EA[0]
B[17:0]	Input	Dynamic	High	Input data B
BLAT[1:0]	Input	Static	High	Bypass data B registers. • BLAT[1] is for B[17:9]. Connect to 1, if not registered. • BLAT[0] is for B[8:0]. Connect to 1, if not registered. In normal mode, ensure BLAT[0] = BLAT[1].
ARSTB[1:0]	Input	Dynamic	Low	Asynchronous reset for data B registers. • ARSTB[1] is for B[17:9]. Connect to 1, if not registered. • ARSTB[0] is for B[8:0]. Connect to 1, if not registered. In normal mode, ensure ARSTB[1] = ARSTB[0].
SRSTB[1:0]	Input	Dynamic	Low	Synchronous reset for data B registers. • SRSTB[1] is for B[17:9]. Connect to 1, if not registered. • SRSTB[0] is for B[8:0]. Connect to 1, if not registered. In normal mode, ensure SRSTB[1] = SRSTB[0].
EB[1:0]	Input	Dynamic	High	Enable for data B registers. • EB[1] is for B[17:9]. Connect to 1, if not registered. • EB[0] is for B[8:0]. Connect to 1, if not registered. In normal mode, ensure EB[1] = EB[0].

Table 1. Math18x18 Ports (Continued)

Port Name	Direction	Type	Polarity	Description
P[40:0]	Output		High	Result data. • Normal mode $P = C + (A \times B)$, when SUB = 0 $P = C - (A \times B)$, when SUB = 1 • SIMD mode $P_L = A_L \times B_L$ $P_H = C_H + (A_H \times B_H)$, when SUB = 0 $P_H = C_H - (A_H \times B_H)$, when SUB = 1 *Notation*: $A_L = A[8:0]$, $A_H = A[17:9]$ $B_L = B[8:0]$, $B_H = B[17:9]$ $P_L = P[17:0]$, $P_H = P[40:18]$ $C_H = C[40:18]$. See Table 4 on page 324 to see how operand C is obtained from CIN, P or CDIN.
OVFL	Output		High	Overflow. • Normal mode if C +/- (A x B) > (2^{40}) - 1, then OVFL = 1 if C +/- (A x B) < $-(2^{40})$, then OVFL = 1 otherwise, OVFL = 0 • SIMD mode if C_H +/- (A_H x B_H) > (2^{22}) - 1, then OVFL = 1 if C_H +/- (A_H x B_H) < $-(2^{22})$, then OVFL = 1 otherwise, OVFL = 0
PLAT[1:0]	Input	Static	High	Bypass result P registers. • PLAT[1] is for P[40:18] and OVFL. Connect to 1, if not registered • PLAT[0] is for P[17:0]. Connect to 1, if not registered In normal mode, ensure PLAT[0] = PLAT[1].
ARSTP[1:0]	Input	Dynamic	Low	Asynchronous reset for result P registers. • ARSTP[1] is for P[40:18] and OVFL. Connect to 1, if not registered. • ARSTP[0] is for P[17:0]. Connect to 1, if not registered In normal mode, ensure ARSTP[1] = ARSTP[0].
SRSTP[1:0]	Input	Dynamic	Low	Synchronous reset for result P registers. • SRSTP[1] is for P[40:18] and OVFL. Connect to 1, if not registered. • SRSTP[0] is for P[17:0]. Connect to 1, if not registered. In normal mode, ensure SRSTP[1] = SRSTP[0].
EP[1:0]	Input	Dynamic	High	Enable for result P registers. • EP[1] is for P[40:18] and OVFL. Connect to 1, if not registered. • EP[0] is for P[17:0]. Connect to 1, if not registered. In normal mode, ensure EP[1] = EP[0].
CDOUT[40:0]	Output	Cascade	High	Cascade output of result P. CDOUT is the same as P. The entire bus must either be dangling or drive an entire CDIN of another MATH block in cascaded mode.
CIN[40:0]	Input	Dynamic	High	Routed input for operand C. In SIMD mode, connect CIN[17:0] to 0. See Table 4 on page 324 to see how CIN is propagated to operand C.
CDIN[40:0]	Input	Cascade	High	Cascaded input for operand C. The entire bus must be driven by an entire CDOUT of another MATH block. See Table 4 on page 324 to see how CDIN is propagated to operand C.
SHFTSEL	Input	Dynamic	High	Arithmetic right-shift for operand C. When asserted, a 17-bit arithmetic right-shift is performed on operand C going into the accumulator. In SIMD mode, SHFTSEL is ignored. See Table 4 on page 324 to see how operand C is obtained from CIN, P or CDIN.

Table 1. Math18x18 Ports (Continued)

Port Name	Direction	Type	Polarity	Description
SHFTSELLAT	Input	Static	High	Bypass SHFTSEL register. Connect to 1, if not registered.
ALSHFTSEL	Input	Dynamic	Low	Asynchronous load for SHFTSEL register. Connect to 1, if not registered. When asserted, SHFTSEL register is loaded with SHFTSELAD.
SHFTSELAD	Input	Static	High	Asynchronous load data for SHFTSEL register.
SLSHFTSEL	Input	Dynamic	Low	Synchronous load for SHFTSEL register. Connect to 1, if not registered. See Table 2 on page 324
SHFTSELSD	Input	Static	Low	Synchronous load data for SHFTSEL register. See Table 2 on page 324
ESHFTSEL	Input	Dynamic	High	Enable for SHFTSEL register. Connect to 1, if not registered. See Table 2 on page 324
CDSEL	Input	Dynamic	High	Select CDIN for operand C. When CDSEL = 1, propagate CDIN. When CDSEL = 0, propagate CIN or P depending on FDBKSEL. In SIMD mode, CDSEL is ignored for CDIN[17:0] and only CDIN[40:18] is propagated. See Table 4 on page 324 to see how operand C is obtained from CIN, P or CDIN.
CDSELLAT	Input	Static	High	Bypass CDSEL register. Connect to 1, if not registered.
ALCDSEL	Input	Dynamic	Low	Asynchronous load for CDSEL register. Connect to 1, if not registered. When asserted, CDSEL register is loaded with CDSELAD.
CDSELAD	Input	Static	High	Asynchronous load data for CDSEL register.
SLCDSEL	Input	Dynamic	Low	Synchronous load for CDSEL register. Connect to 1, if not registered. See Table 2 on page 324.
CDSELSD	Input	Static	Low	Synchronous load data for CDSEL register. See Table 2 on page 324.
ECDSEL	Input	Dynamic	High	Enable for CDSEL register. Connect to 1, if not registered. See Table 2 on page 324.
FDBKSEL	Input	Dynamic	High	Select the feedback from P for operand C. When FDBKSEL = 1, propagate the current value of result P register. Ensure PLAT[1] = 0 and CDSEL = 0. When FDBKSEL = 0, propagate CIN. Ensure CDSEL = 0. To load P from CIN, ensure either A = 0 or B = 0. In SIMD mode, FDBKSEL is ignored for P[17:0] and only P[40:18] is propagated. See Table 4 on page 324 to see how operand C is obtained from CIN, P or CDIN.
FDBKSELLAT	Input	Static	High	Bypass FDBKSEL register. Connect to 1, if not registered.
ALFDBKSEL	Input	Dynamic	Low	Asynchronous load for FDBKSEL register. Connect to 1, if not registered. When asserted, FDBKSEL register is loaded with FDBKSELAD.
FDBKSELAD	Input	Static	High	Asynchronous load data for FDBKSEL register.
SLFDBKSEL	Input	Dynamic	Low	Synchronous load for FDBKSEL register. Connect to 1, if not registered. See Table 2 on page 324.
FDBKSELSD	Input	Static	Low	Synchronous load data for FDBKSEL register. See Table 2 on page 324.
EFDBKSEL	Input	Dynamic	High	Enable for FDBKSEL register. Connect to 1, if not registered. See Table 2.

Table 1. Math18x18 Ports (Continued)

Port Name	Direction	Type	Polarity	Description
SUB	Input	Dynamic	High	Subtract operation. When SUB = 1, perform Two's complement subtraction to get result P = C - (A x B). When SUB = 0, perform Two's complement addition to get result P = C + (A x B).
SUBLAT	Input	Static	High	Bypass SUB register. Connect to 1, if not registered.
ALSUB	Input	Dynamic	Low	Asynchronous load for SUB register. Connect to 1, if not registered. When asserted, SUB register is loaded with SUBAD.
SUBAD	Input	Static	High	Asynchronous load data for SUB register.
SLSUB	Input	Dynamic	Low	Synchronous load for SUB register. Connect to 1, if not registered. See Table 2.
SUBSD	Input	Static	Low	Synchronous load data for SUB register. See Table 2.
ESUB	Input	Dynamic	High	Enable for SUB register. Connect to 1, if not registered. See Table 2.

Table 2. Truth Table for Control Registers SHFTSEL, CDSEL, FDBKSEL and SUB

al	ad	lat	clk	en	sl	sd	d	q
0	x	x	x	x	x	x	x	ad
1	x	0	not rising	x	x	x	x	q
1	x	0	rising	0	x	x	x	q
1	x	0	rising	1	0	x	x	!sd
1	x	0	rising	1	1	x	x	d
1	x	1	x	0	x	x	x	q
1	x	1	x	1	0	x	x	!sd
1	x	1	x	1	1	x	x	d

Table 3. Truth Table for Data Registers A, B, P and OVFL

arst	lat	clk	en	srst	d	q
0	x	x	x	x	x	0
1	0	not rising	x	x	x	q
1	0	rising	0	x	x	q
1	0	rising	1	0	x	0
1	0	rising	1	1	x	d
1	1	x	0	x	x	q
1	1	x	1	0	x	0
1	1	x	1	1	x	d

Table 4. Truth Table for Propagating Data to Operand C

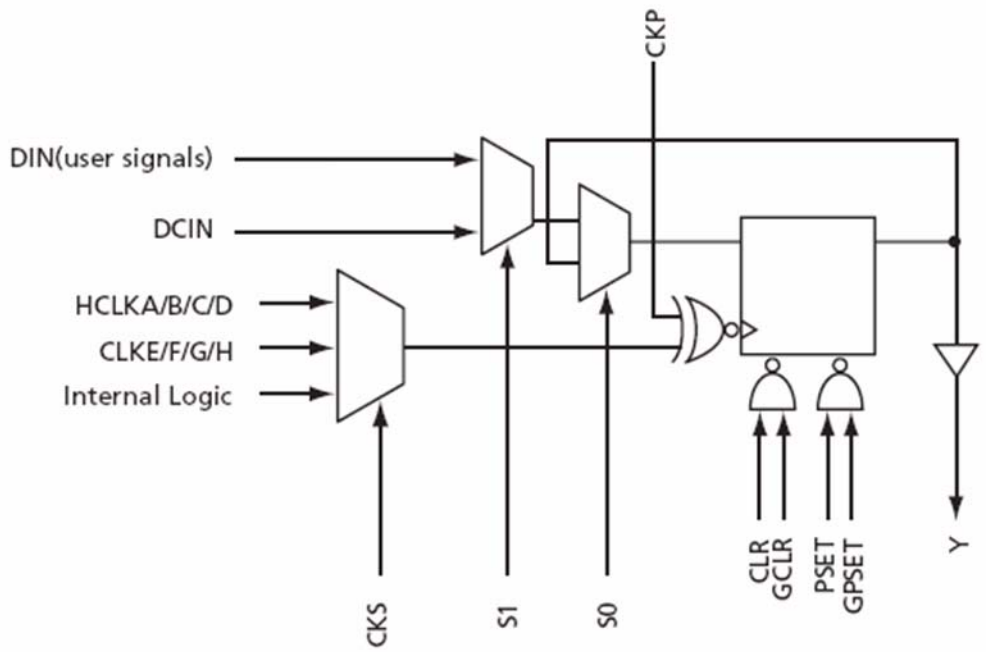
FDBKSEL	CDSEL	SHFTSEL	SIMD	Operand C
0	0	0	0	CIN[40:0]
0	0	x	1	CIN[40:0]

Table 4. Truth Table for Propagating Data to Operand C

FDBKSEL	CDSEL	SHFTSEL	SIMD	Operand C
0	0	1	0	{{17{CIN[40]}},CIN[40:17]}
x	1	0	0	CDIN[40:0]
x	1	x	1	{CDIN[40:18],CIN[17:0]}
x	1	1	0	{{17{CDIN[40]}},CDIN[40:17]}
1	0	0	0	P[40:0]
1	0	x	1	{P[40:18],CIN[17:0]}
1	0	1	0	{{17{P[40]}},P[40:17]}

Simulation Support for GCLR/GPSET in Axcelerator

In Axcelerator, during power up, all the sequential elements in the Fabric are set to 0 or 1 via a Global SET/CLR fuse. You can choose the SET/CLR option when generating the programming file. Each sequential element in the fabric has two additional controls, GCLR/GPSET, which are active only during power up. After power up GCLR/GPSET inputs are pulled high and user inputs are active (as shown in the figure below).



Since GPSET and GCLR are not user inputs, CAE macros do not have them. Libero IDE v9.0SP1 adds simulation support for the power up behavior of sequential elements.

In Libero IDE v9.0SP1 two additional precompiled Axcelerator libraries and one source file are provided for Axcelerator. In total there are three precompiled libraries for Verilog and three precompiled libraries for VHDL. The libraries are installed when you choose the AX family during installation. Libraries related to Axcelerator can be found under precompiled directories in the installation: <installation>/Designer/lib/modelsim/precompiled (as shown in the table below).

Table 1: Axcelerator Precompiled Libraries

Directory	Description	Power Up State
/vlog/axcelerator	Verilog library without gclr/gpset support	Legacy
/vlog/axcelerator_gpset	Verilog library with gpset support	1
/vlog/axcelerator_gclr	Verilog library with gclr support	0
/vhdl/axcelerator	VHDL library without gclr/gpset support	Legacy
/vhdl/axcelerator_gpset	VHDL library with gpset support	1
/vhdl/axcelerator_gclr	VHDL library without gclr support	0

By default, Libero IDE maps the simulation library to the old library, i.e. /vlog/axcelerator or /vhdl/axcelerator. If you want GPSET/GCLR behavior, you can map the library to one of the two new libraries.

At 0th time CLR/PRE is applied to every flip-flop or latch and is removed at some pre-defined time called POWERUP_TIME (100 ns). This pre-defined time can be modified by editing a define statement or con-

stant in the source files. During the power up time user controls do not impact the behavior of the sequential element. This is according to the silicon behavior where user inputs are inactive until the power up is complete. After the power up time the sequential element behaves normally.

Note: This solution is not viable for migration macros. If you have migration macros in the netlist, those macros are not initialized to 0 or 1.

Source libraries

One new Verilog source file and VHDL source file are present in the libraries directory. These source files are for those users who do not use precompiled libraries.

/src/vtl/95/axcelerator.vhd - legacy

/src/vtl/95/ax_gclr_gpset.vhd - with gpset/gclr support

/src/vlog/axcelerator.v - legacy

/src/vlog/ax_gclr_gpset.w - with gpset/gclr support

VHDL Source file

Two constants are defined inside the VTABLES package:

```
constant AX_FF_INIT_VALUE : std_ulogic := '0';
constant POWERUP_TIME : time := 100 ns;
```

AX_FF_INIT_VALUE defines the required power up state; POWERUP_TIME defines for how long GCLR and GPSET should be applied. You can modify these constants as required and compile the library. Settings for power up states 0/1 are listed below.

POWER UP STATE = 1

Set the constant value as below in VTABLES package

```
constant AX_FF_INIT_VALUE : std_ulogic := '1';
```

POWER UP STATE = 0

Set the constant value as below in VTABLES package

```
constant AX_FF_INIT_VALUE : std_ulogic := '0';
```

Verilog Source File

Like the Constants in VHDL, Verilog library has two definitions:

```
`define AX_FF_INIT_VALUE  1'b0
`define POWERUP_TIME 100
```

AX_FF_INIT_VALUE defines the required power up state. POWERUP_TIME defines for how long GCLR and GPSET should be applied. You can modify these definitions as required and compile the library. Settings for power up states 0/1 are listed below.

POWER UP STATE = 1

Set the definition as:

```
`define AX_FF_INIT_VALUE  1
```

POWER UP STATE = 0

Set the definition as:

```
`define AX_FF_INIT_VALUE  0
```