



Rate This Document

---

# ***Antifuse Macro Library Guide***

*for Software v9.0SP1*



---

## **Table of Contents**

### **Actel Corporation, Mountain View, CA 94043**

© 2010 Actel Corporation. All rights reserved.

Part Number: 5029009-25

Release: July 2010

No part of this document may be copied or reproduced in any form or by any means without prior written consent of Actel.

Actel makes no warranties with respect to this documentation and disclaims any implied warranties of merchantability or fitness for a particular purpose. Information in this document is subject to change without notice. Actel assumes no responsibility for any errors that may appear in this document.

This document contains confidential proprietary information that is not to be disclosed to any unauthorized person without prior written consent of Actel Corporation.

#### **Trademarks**

Actel and the Actel logo are registered trademarks of Actel Corporation.

Adobe and Acrobat Reader are registered trademarks of Adobe Systems, Inc.

All other products or brand names mentioned are trademarks or registered trademarks of their respective holders.

---

# Table of Contents

## Introduction

Definitions . . . . .	7
How to Use this Guide . . . . .	7
Restrictions . . . . .	7
Advanced Application Notes . . . . .	8
HDL Instantiation of Macros . . . . .	8
Migration Between Families . . . . .	8

## Lists

<b>List of Combinational Macros</b> . . . . .	9
<b>List of Sequential Macros</b> . . . . .	13
<b>List of CC Macros</b> . . . . .	15
<b>List of RAM Macros</b> . . . . .	17
<b>List of Input/Output Macros</b> . . . . .	19
<b>Alphabetical List of Macros</b> . . . . .	21
<b>Combinational/Sequential Macros</b> . . . . .	27
Combinational, AND . . . . .	29
Combinational, AND-OR . . . . .	37
Combinational, AND-OR-INVERT . . . . .	53
Combinational, AND-OR-INVERT . . . . .	57
Combinational, AND-XOR . . . . .	58
Combinational, AND-XOR-INVERT . . . . .	58
Combinational, 3-Input Gate . . . . .	60
Buffers . . . . .	67
Clock Interface . . . . .	68
Combinational, Module . . . . .	70
Carry Generator . . . . .	87
Sequential, D-Type Flip-Flop . . . . .	89
Sequential D-Type Flip-Flop with Enable . . . . .	95
Sequential, D-Type Flip-Flop with Multiplexed Data . . . . .	107
Sequential, D-Type Flip-Flop with Preset . . . . .	122
Sequential, D-Type Flip-Flop with Preset and Clear . . . . .	130
Sequential, Data Latch . . . . .	131
Sequential, Data Latch with Clear . . . . .	136
Sequential, Data Latch with Enable and Clear . . . . .	139

Sequential, Data Latch with Enable and Preset .....	.142
Data Latch .....	.144
Data Latch with Multiplexed Data .....	.147
Sequential, Data Latch with Preset .....	.153
Sequential, JK Flip-Flop .....	.155
Combinational, Wide Decode .....	.156
Combinational, Clock Net Interface .....	.160
Combinational, Half Adder .....	.163
Combinational, Inverters .....	.165
JK Flip-Flop .....	.168
Combinational, AND-OR .....	.172
Combinational, AND-OR-INVERT .....	.177
Combinational, Multiplexer .....	.178
Combinational, NAND .....	.181
Combinational, NOR .....	.189
Combinational, OR-AND .....	.196
Combinational, OR-AND-INVERT .....	.202
Combinational, OR .....	.207
Combinational, XOR-AND .....	.217
Combinational, XNOR-AND .....	.218
Combinational, XNOR-NAND .....	.219
Combinational, XNOR .....	.220
Combinational, XOR-OR .....	.221
Combinational, XOR .....	.222
Combinational, Gate .....	.225
<b>CC-Module Flip Flops .....</b>	<b>227</b>
<b>Memory Macros .....</b>	<b>239</b>
RAM Macros .....	.240
FIFO Macros .....	.253
<b>I/O Macros .....</b>	<b>255</b>
Input/Output, General Use .....	.256
ACT 2/XL/DX/MX I/O Macros .....	.264
ACT 3 I/O Macros .....	.271
Axcelerator Input IO Macros .....	.289
Bi-Directional IO Macros .....	.290
Clock Buffers .....	.293
HClock Buffers .....	.294
Output Buffers .....	.295
Tri-State Buffer Macros .....	.296
Differential I/O Macros .....	.298

DDR Macro .....	.300
SIMBUF Macro .....	.301
<b>Carry Chain Macros .....</b>	<b>303</b>
Carry Chain Macros .....	.304
<b>PLL Macros .....</b>	<b>315</b>
PLL Macros .....	.316
<b>RTAX-DSP Math Macro .....</b>	<b>319</b>
MATH18X18 Macro .....	.320
<b>Simulation Support for GCLR/GPSET in Axcelerator .....</b>	<b>327</b>



# Introduction

This guide includes macros for all Actel antifuse devices. For flash devices, see the *Fusion, IGLOO and ProASIC3 Macro Library Guide*.

## Definitions

### Macros

The Macro library consists of logic elements constructed of one or more ACT family modules. Modules may be of type sequential or combinatorial. The relative placement of two module-macros is predefined. The timing characteristics are a function of the fanout on the output of the macro.

### SmartGen Cores

SmartGen cores are described in Actel's publication *SmartGen Cores Reference Guide*.

## How to Use this Guide

### Family Inclusion Indicator

In the titlebar of each macro is a list indicating whether the cell is a member of the ACT 1, ACT 2, 3200DX, ACT 3, MX, SX, SX-A, eX, or Axcelerator library.

### Guidelines

1. All input pin loading is assumed to be a single load except macros that are built using two combinational modules or one sequential and one combinational module. These macros are assumed to have a load of two on some of their input pins.
2. All macros have output pin loading of zero except for the sequential macros that are built using two combinational modules only. These macros have an output pin loading of one.
3. All macros have logic levels equal to one except cells with pin delays of two. A "2" is added to the corresponding symbol in the macro section of this manual.

### Truth Table Nomenclature

Truth tables are arranged with *Inputs* before *Outputs*. The following symbol definitions apply.

- ↑ denotes rising edge clock
- ↓ denotes falling edge clock
- X in an input column denotes a 'don't care' or logic simulation state 'un-

known'

!Q denotes Q not

### Pin Delay Annotation

Two-module combinatorial macros contain extra delay on some or all of the pins. If a macro symbol in this guide displays a "2" on a pin, then two levels of logic delay exist on the input to output path.

Note: Many two-level logic functions in one family are implemented in a single module in another family, hence the "2" may apply to specific families only.

## Restrictions

### Special I/Os

Some I/O pins are able to connect to global control signals such as clock or clear. These I/O pins may be used as "normal" data input/output buffers or they may be used as "special" pins. The following constraints apply to I/O pins used as "special" pins.

All ACT 2, 3200DX, ACT 3, MX, SX, SX-A, and eX register cells may be clocked by either of the two global clock networks by connecting their CLK input to the output of a CLKBUF, CLKBIBUF, or CLKINT macro.

All ACT 2, 3200DX, ACT 3, MX, SX, SX-A, and eX register cells may be globally preset, reset or enabled by connecting the PRE, CLR, or E input to the output of a CLKBUF, CLKBIBUF, CLKINT macro.

All ACT 2, 3200DX, ACT 3, MX, SX, SX-A and eX I/O three-state buffers may be globally enabled by connecting their E input to the output of a CLKBUF, CLKBIBUF, OR CLKINT macro.

All ACT 3, SX, SX-A and eX register cells composed of sequential modules may be clocked by high speed clock buffer network by connecting their CLK input to the output of a HCLKBUF macro.

ACT 3 registered I/O macros may only be clocked by the IOCLKBUF macro.

ACT 3 registered I/O macros may *only* be asynchronously set or preset by the IOPCL macro.

## Advanced Application Notes

For Advanced Application notes, please go to the Actel website at <http://www.actel.com>.

## HDL Instantiation of Macros

Refer to the *HDL Coding Style Guide* for information on instantiating macros.

## Migration Between Families

Actel provides the capability of migrating a netlist created for one family to another family in some cases. Macros listed in this manual as being available in the old family will not be shown as available in the new family when the new macro is inefficient or when the function can be better implemented with different macros, however, the macro may be available in the

new family. Such macros are not recommended for new designs.

In all cases, if an HDL description is available, it is best to resynthesize, targeting the new family.

If an HDL description is not available, it is still generally best to do gate level retargeting to the new family.

If neither of the above is done, a netlist created for one family may be used in another family as follows: No special procedures are needed to use the netlist in Designer, but a migration library must be enabled in CAE environments as explained in individual CAE Interface Guides.

	Target Family						
Original Family	ACT 1/MX	ACT 2/ 3200DX/MX	ACT 3	SX	SX-A	eX	
ACT 1 or MX	X	YES	YES	NO	NO	NO	
ACT 2, 1200XL, 3200DX, MX	NO	X	YES**	YES**	YES**	YES**	
ACT 3	NO	NO	X	YES*	YES*	YES*	
SX	NO	NO	NO	X	YES	YES	
SX-A	NO	NO	NO	YES**	X	YES	
eX	NO	NO	NO	YES	YES	X	

\* Except registered I/O, IOCLK, and IOPCL

\*\* Except QCLK and RAM

---

# List of Combinational Macros

AND2 .....	29	AO3B .....	48
AND2A .....	29	AO3C .....	48
AND2B .....	30	AO4A .....	49
AND3 .....	30	AO5A .....	49
AND3A .....	31	AO6 .....	50
AND3B .....	31	AO6A .....	50
AND3C .....	32	AO7 .....	51
AND4 .....	32	AO8 .....	51
AND4A .....	33	AO9 .....	52
AND4B .....	33	AOI1 .....	52
AND4C .....	34	AOI1A .....	53
AND4D .....	34	AOI1B .....	53
AND5A .....	35	AOI1C .....	54
AND5B .....	35	AOI1D .....	54
AND5C .....	36	AOI2A .....	55
A01 .....	36	AOI2B .....	55
AO10 .....	37	AOI3A .....	56
AO11 .....	37	AOI4 .....	56
AO12 .....	38	AOI4A .....	57
AO13 .....	38	AOI5 .....	57
AO14 .....	39	AX1 .....	58
AO15 .....	39	AX1A .....	58
AO16 .....	40	AX1B .....	59
AO17 .....	40	AX1C .....	59
AO18 .....	41	AX1D .....	60
AO1A .....	41	AX1E .....	60
AO1B .....	42	AXO1 .....	61
AO1C .....	42	AXO2 .....	61
AO1D .....	43	AXO3 .....	62
AO1E .....	43	AXO5 .....	62
AO2 .....	44	AXO6 .....	63
AO2A .....	44	AXO7 .....	63
AO2B .....	45	AXO11 .....	64
AO2C .....	45	AXO12 .....	64
AO2D .....	46	AXO13 .....	65
AO2E .....	46	AXO14 .....	65
AO3 .....	47	AXO15 .....	66
AO3A .....	47	AXO17 .....	66

BUFA .....	67	DLM2A .....	147
BUFF .....	67	DLM2B .....	147
BUFD .....	68	DLM3 .....	148
CLKINT .....	68	DLM3A .....	148
HCLKINT .....	69	DLM4 .....	149
CLKINTI .....	69	DLM4A .....	149
CM7 .....	70	DLM8A .....	150
CM8 .....	71	DLM8B .....	151
CM8A .....	72	DLMA .....	152
CM8F .....	73	DLME1A .....	152
CM8INV .....	74	DLP1 .....	153
CMA9 .....	74	DLP1A .....	153
CMAF .....	75	DLP1B .....	154
CMB3 .....	75	DLP1C .....	154
CMB7 .....	76	DLP1D .....	155
CMBB .....	76	DLP1E .....	155
CMBF .....	77	DXAND7 .....	156
CMEA .....	77	DXAX7 .....	157
CMEB .....	78	DXNAND7 .....	157
CMEE .....	78	FA1 .....	158
CMEF .....	79	FA1A .....	158
CMF1 .....	79	FA1B .....	159
CMF2 .....	80	FA2A .....	159
CMF3 .....	80	GAND2 .....	160
CMF4 .....	81	GMX4 .....	160
CMF5 .....	81	GNAND2 .....	161
CMF6 .....	82	GND .....	161
CMF7 .....	82	GNOR2 .....	162
CMF8 .....	83	GOR2 .....	162
CMF9 .....	83	GXOR2 .....	163
CMFA .....	84	HA1 .....	163
CMFB .....	84	HA1A .....	164
CMFC .....	85	HA1B .....	164
CMFD .....	85	HA1C .....	165
CMFE .....	86	INV .....	165
CS1 .....	86	INVD .....	166
CS2 .....	87	INVA .....	166
CY2A .....	87	JKF .....	167
CY2B .....	89	JKF1B .....	168
DLEB .....	144	JKF2A .....	168
DLEC .....	144	JKF2B .....	169
DLM .....	145	JKF2C .....	169
DLM2 .....	145	JKF2D .....	170

JKF3A .....	170	NOR4B .....	194
JKF3B .....	171	NOR4C .....	194
JKF3C .....	171	NOR4D .....	195
JKF3D .....	172	NOR5B .....	195
JKF4B .....	173	NOR5C .....	196
JKFPC .....	173	NOR5D .....	196
MAJ3 .....	174	OA1 .....	197
MAJ3X .....	174	OA1A .....	198
MAJ3XI .....	175	OA1B .....	198
MIN3 .....	175	OA1C .....	199
MIN3X .....	176	OA2 .....	199
MIN3XI .....	177	OA2A .....	200
MX2 .....	178	OA3 .....	200
MX2A .....	178	OA3A .....	201
MX2B .....	179	OA3B .....	201
MX2C .....	179	OA4 .....	202
MX4 .....	180	OA4A .....	202
MXC1 .....	180	OA5 .....	203
MXT .....	181	OAI1 .....	203
NAND2 .....	181	OAI2A .....	204
NAND2A .....	182	OAI3 .....	204
NAND2B .....	182	OAI3A .....	205
NAND3 .....	183	OR2 .....	207
NAND3A .....	183	OR2A .....	207
NAND3B .....	184	OR2B .....	208
NAND3C .....	184	OR3 .....	208
NAND4 .....	185	OR3A .....	209
NAND4A .....	185	OR3B .....	209
NAND4B .....	186	OR3C .....	210
NAND4C .....	186	OR4 .....	210
NAND4D .....	187	OR4A .....	211
NAND5B .....	187	OR4B .....	211
NAND5C .....	188	OR4C .....	212
NAND5D .....	188	OR4D .....	212
NOR2 .....	189	OR5A .....	213
NOR2A .....	189	OR5B .....	213
NOR2B .....	190	OR5C .....	214
NOR3 .....	191	QCLKINT .....	214
NOR3A .....	191	QCLKINTI .....	215
NOR3B .....	192	TF1A .....	215
NOR3C .....	192	TF1B .....	216
NOR4 .....	193	VCC .....	216
NOR4A .....	193	XA1 .....	217

XA1A . . . . .	217
XA1B . . . . .	218
XA1C . . . . .	218
XAI1 . . . . .	219
XAI1A . . . . .	219
XNOR2 . . . . .	220
XNOR3 . . . . .	220
XO1 . . . . .	221
XO1A . . . . .	221
XOR2 . . . . .	222
XOR3 . . . . .	222
XOR4 . . . . .	223
XNOR4 . . . . .	224
ZOR3 . . . . .	225
ZOR3I . . . . .	225

---

# List of Sequential Macros

DF1 .....	89	DFM1B .....	108
DF1A .....	90	DFM1C .....	109
DF1B .....	90	DFM3 .....	109
DF1C .....	91	DFM3B .....	110
DFC1 .....	91	DFM3E .....	110
DFC1A .....	92	DFM3F .....	111
DFC1B .....	92	DFM3G .....	111
DFC1C .....	93	DFM4 .....	112
DFC1D .....	93	DFM4A .....	112
DFC1E .....	94	DFM4B .....	113
DFC1F .....	94	DFM4C .....	113
DFC1G .....	95	DFM4D .....	114
DFE .....	95	DFM4E .....	114
DFE1B .....	96	DFM5A .....	115
DFE1C .....	96	DFM5B .....	115
DFE2D .....	97	DFM6A .....	116
DFE3A .....	97	DFM6B .....	116
DFE3B .....	98	DFM7A .....	117
DFE3C .....	98	DFM7B .....	118
DFE3D .....	99	DFM8A .....	119
DFE4 .....	99	DFM8B .....	120
DFE4A .....	100	DFMA .....	121
DFE4B .....	100	DFMB .....	121
DFE4C .....	101	DFME1A .....	122
DFE4F .....	101	DFME1B .....	122
DFE4G .....	102	DFME2A .....	123
DFEA .....	102	DFME2B .....	123
DFEB .....	103	DFME3A .....	124
DFEC .....	103	DFME3B .....	124
DFED .....	104	DFMPCA .....	125
DFEG .....	104	DFMPCB .....	125
DFEH .....	105	DFP1 .....	126
IODFE .....	105	DFP1A .....	126
IODFEC .....	106	DFP1B .....	127
IODFEP .....	106	DFP1C .....	127
DFM .....	107	DFP1D .....	128
DFMEG .....	107	DFP1E .....	128
DFMEH .....	108	DFP1F .....	129

DFP1G .....	129
DFPC .....	130
DFPCA .....	130
DFPCB .....	131
DFPCC .....	131
DL1 .....	132
DL1A .....	132
DL1B .....	133
DL1C .....	133
DL2A .....	134
DL2B .....	134
DL2C .....	135
DL2D .....	136
DLC .....	136
DLC1 .....	137
DLC1A .....	137
DLC1F .....	138
DLC1G .....	138
DLCA .....	139
DLE .....	139
DLE1D .....	140
DLE2A .....	140
DLE2B .....	141
DLE2C .....	141
DLE3A .....	142
DLE3B .....	142
DLE3C .....	143
DLEA .....	143

---

## List of CC Macros

DF1_CC .....	228
DF1A_CC .....	228
DF1B_CC .....	229
DF1C_CC .....	229
DFC1_CC .....	230
DFC1A_CC .....	230
DFC1B_CC .....	231
DFC1D_CC .....	231
DFE_CC .....	232
DFE1B_CC .....	232
DFE1C_CC .....	233
DFEA_CC .....	233
DFM_CC.....	234
DFMA_CC .....	234
DFM1B_CC.....	235
DFM1C_CC.....	235
DFP1_CC* .....	236
DFP1A_CC* .....	236
DFP1B_CC* .....	237
DFP1D_CC* .....	237
DFPC_CC* .....	238
DFPCA_CC* .....	238



---

## List of RAM Macros

RAM4FA .....	240
RAM4FF .....	241
RAM4FR .....	242
RAM4RA .....	243
RAM4RF .....	244
RAM4RR .....	245
RAM8FA .....	246
RAM8FF .....	247
RAM8FR .....	248
RAM8RA .....	249
RAM8RF .....	250
RAM8RR .....	251
RAM64K36 /RAM64K36P .....	252
FIFO64K36/FIFO64K36P .....	253



---

# List of Input/Output Macros

BIBUF .....	256	BREPTL .....	276
CLKBIBUF .....	256	DECETH .....	277
HCLKBIBUF .....	257	DECETL .....	277
CLKBIBUFI .....	257	DEPETH .....	278
CLKBUF .....	258	DEPETL .....	278
CLKBUFI .....	258	FECTH .....	279
HCLKBUF .....	259	FECTL .....	279
INBUF .....	259	FEPTH .....	280
OUTBUF .....	260	FEPTL .....	280
QCLKBIBUFI .....	261	FECTMH .....	281
QCLKBIBUF .....	261	FECTML .....	281
QCLKBUF .....	262	FEPTMH .....	282
QCLKBUFI .....	262	FEPTML .....	282
TRIBUFF .....	263	IBUF .....	283
BBDLHS .....	264	IOCLKBUF .....	283
BBHS .....	264	IOPCLBUF .....	284
IBDL .....	265	IREC .....	284
IR .....	265	IREP .....	285
IRI .....	266	OBUFTH .....	285
OBDLHS .....	266	OBUFTL .....	286
OBHS .....	267	ORECTH .....	286
ORH .....	267	ORECTL .....	287
ORIH .....	268	OREPTH .....	287
ORITH .....	268	OREPTL .....	288
ORTH .....	269	INBUF_X .....	289
TBDLHS .....	270	BIBUF_X .....	291
TBHS .....	270	CLKBUF_X .....	293
BBHSA .....	271	HCLKBUF_X .....	294
BBLSA .....	271	OUTBUF_X .....	295
BBUFTH .....	272	TRIBUFF_X .....	296
BBUFTL .....	272	INBUF_LVDS; INBUF_LVPECL .....	298
BIECTH .....	273	CLKBUF_LVDS; CLKBUF_LVPECL .....	298
BIECTL .....	273	HCLKBUF_LVDS; HCLKBUF_LVPECL .....	299
BIEPTH .....	274	OUTBUF_LVDS; OUTBUF_LVPECL .....	299
BIEPTL .....	274	DDR_REG macro .....	300
BRECTH .....	275	SIMBUF .....	301
BRECTL .....	275	ADD1 .....	304
BREPTH .....	276	SUB1 .....	304

ADDSUB1 .....	305
MULT1 .....	306
ARCNTECP1 .....	307
AFCNTECP1 .....	307
SRCNTECP1 .....	308
SFCNTECP1 .....	308
ARCNTELDCP1 .....	309
AFCNTELDCP1 .....	310
SRCNTELDCP1 .....	310
SFCNTELDCP1 .....	311
FCEND_BUFF .....	311
FCEND_INV .....	312
FCINIT_BUFF .....	312
FCINIT_GND .....	313
FCINIT_INV .....	313
FCINIT_VCC .....	314
PLL; PLLFB .....	316
PLLINT .....	317
PLLOUT .....	317
PLLHCLK .....	318
PLLRCLOCK .....	318
MATH18X18 .....	320

---

# Alphabetical List of Macros

A01 . . . . .	36	AO2D . . . . .	46
ADD1 . . . . .	304	AO2E . . . . .	46
ADDSUB1 . . . . .	305	AO3 . . . . .	47
AFCNTECP1 . . . . .	307	AO3A . . . . .	47
AFCNTELDCP1 . . . . .	310	AO3B . . . . .	48
AND2 . . . . .	29	AO3C . . . . .	48
AND2A . . . . .	29	AO4A . . . . .	49
AND2B . . . . .	30	AO5A . . . . .	49
AND3 . . . . .	30	AO6 . . . . .	50
AND3A . . . . .	31	AO6A . . . . .	50
AND3B . . . . .	31	AO7 . . . . .	51
AND3C . . . . .	32	AO8 . . . . .	51
AND4 . . . . .	32	AO9 . . . . .	52
AND4A . . . . .	33	AOI1 . . . . .	52
AND4B . . . . .	33	AOI1A . . . . .	53
AND4C . . . . .	34	AOI1B . . . . .	53
AND4D . . . . .	34	AOI1C . . . . .	54
AND5A . . . . .	35	AOI1D . . . . .	54
AND5B . . . . .	35	AOI2A . . . . .	55
AND5C . . . . .	36	AOI2B . . . . .	55
AO10 . . . . .	37	AOI3A . . . . .	56
AO11 . . . . .	37	AOI4 . . . . .	56
AO12 . . . . .	38	AOI4A . . . . .	57
AO13 . . . . .	38	AOI5 . . . . .	57
AO14 . . . . .	39	ARCNTECP1 . . . . .	307
AO15 . . . . .	39	ARCNTELDCP1 . . . . .	309
AO16 . . . . .	40	AX1 . . . . .	58
AO17 . . . . .	40	AX1A . . . . .	58
AO18 . . . . .	41	AX1B . . . . .	59
AO1A . . . . .	41	AX1C . . . . .	59
AO1B . . . . .	42	AX1D . . . . .	60
AO1C . . . . .	42	AX1E . . . . .	60
AO1D . . . . .	43	AXO1 . . . . .	61
AO1E . . . . .	43	AXO2 . . . . .	61
AO2 . . . . .	44	AXO3 . . . . .	62
AO2A . . . . .	44	AXO5 . . . . .	62
AO2B . . . . .	45	AXO6 . . . . .	63
AO2C . . . . .	45	AXO7 . . . . .	63

AXOI1 .....	64	CMBF .....	77
AXOI2 .....	64	CMEA .....	77
AXOI3 .....	65	CMEB .....	78
AXOI4 .....	65	CMEE .....	78
AXOI5 .....	66	CMEF .....	79
AXOI7 .....	66	CMF1 .....	79
BBDLHS .....	264	CMF2 .....	80
BBHS .....	264	CMF3 .....	80
BBHSA .....	271	CMF4 .....	81
BBLSA .....	271	CMF5 .....	81
BBUFTH .....	272	CMF6 .....	82
BBUFTL .....	272	CMF7 .....	82
BIBUF .....	256	CMF8 .....	83
BIBUF_X .....	291	CMF9 .....	83
BIECTH .....	273	CMFA .....	84
BIECTL .....	273	CMFB .....	84
BIEPTH .....	274	CMFC .....	85
BIEPTL .....	274	CMFD .....	85
BRECTH .....	275	CMFE .....	86
BRECTL .....	275	CS1 .....	86
BREPTH .....	276	CS2 .....	87
BREPTL .....	276	CY2A .....	87
BUFA .....	67	CY2B .....	89
BUFD .....	68	DDR_REG macro .....	300
BUFF .....	67	DECETH .....	277
CLKBIBUF .....	256	DECETL .....	277
CLKBIBUFI .....	257	DEPETH .....	278
CLKBUF .....	258	DEPETL .....	278
CLKBUF_LVDS; CLKBUF_LVPECL .....	298	DF1 .....	89
CLKBUF_X .....	293	DF1_CC .....	228
CLKBUFI .....	258	DF1A .....	90
CLKINT .....	68	DF1A_CC .....	228
CLKINTI .....	69	DF1B .....	90
CM7 .....	70	DF1B_CC .....	229
CM8 .....	71	DF1C .....	91
CM8A .....	72	DF1C_CC .....	229
CM8F .....	73	DFC1 .....	91
CM8INV .....	74	DFC1_CC .....	230
CMA9 .....	74	DFC1A .....	92
CMAF .....	75	DFC1A_CC .....	230
CMB3 .....	75	DFC1B .....	92
CMB7 .....	76	DFC1B_CC .....	231
CMBB .....	76	DFC1C .....	93

DFC1D .....	93	DFM4C .....	113
DFC1D_CC .....	231	DFM4D .....	114
DFC1E .....	94	DFM4E .....	114
DFC1F .....	94	DFM5A .....	115
DFC1G .....	95	DFM5B .....	115
DFE .....	95	DFM6A .....	116
DFE_CC .....	232	DFM6B .....	116
DFE1B .....	96	DFM7A .....	117
DFE1B_CC .....	232	DFM7B .....	118
DFE1C .....	96	DFM8A .....	119
DFE1C_CC .....	233	DFM8B .....	120
DFE2D .....	97	DFMA .....	121
DFE3A .....	97	DFMA_CC .....	234
DFE3B .....	98	DFMB .....	121
DFE3C .....	98	DFME1A .....	122
DFE3D .....	99	DFME1B .....	122
DFE4 .....	99	DFME2A .....	123
DFE4A .....	100	DFME2B .....	123
DFE4B .....	100	DFME3A .....	124
DFE4C .....	101	DFME3B .....	124
DFE4F .....	101	DFMEG .....	107
DFE4G .....	102	DFMEH .....	108
DFEA .....	102	DFMPCA .....	125
DFEA_CC .....	233	DFMPCB .....	125
DFEB .....	103	DFP1 .....	126
DFEC .....	103	DFP1_CC* .....	236
DFED .....	104	DFP1A .....	126
DFEG .....	104	DFP1A_CC* .....	236
DFEH .....	105	DFP1B .....	127
DFM .....	107	DFP1B_CC* .....	237
DFM_CC .....	234	DFP1C .....	127
DFM1B .....	108	DFP1D .....	128
DFM1B_CC .....	235	DFP1D_CC* .....	237
DFM1C .....	109	DFP1E .....	128
DFM1C_CC .....	235	DFP1F .....	129
DFM3 .....	109	DFP1G .....	129
DFM3B .....	110	DFPC .....	130
DFM3E .....	110	DFPC_CC* .....	238
DFM3F .....	111	DFPCA .....	130
DFM3G .....	111	DFPCA_CC* .....	238
DFM4 .....	112	DFPCB .....	131
DFM4A .....	112	DFPCC .....	131
DFM4B .....	113	DL1 .....	132

DL1A . . . . .	132	DXAX7 . . . . .	157
DL1B . . . . .	133	DXNAND7 . . . . .	157
DL1C . . . . .	133	FA1 . . . . .	158
DL2A . . . . .	134	FA1A . . . . .	158
DL2B . . . . .	134	FA1B . . . . .	159
DL2C . . . . .	135	FA2A . . . . .	159
DL2D . . . . .	136	FCEND_BUFF . . . . .	311
DLC . . . . .	136	FCEND_INV . . . . .	312
DLC1 . . . . .	137	FCINIT_BUFF . . . . .	312
DLC1A . . . . .	137	FCINIT_GND . . . . .	313
DLC1F . . . . .	138	FCINIT_INV . . . . .	313
DLC1G . . . . .	138	FCINIT_VCC . . . . .	314
DLCA . . . . .	139	FECTH . . . . .	279
DLE . . . . .	139	FECTL . . . . .	279
DLE1D . . . . .	140	FECTMH . . . . .	281
DLE2A . . . . .	140	FECTML . . . . .	281
DLE2B . . . . .	141	FEPTH . . . . .	280
DLE2C . . . . .	141	FEPTL . . . . .	280
DLE3A . . . . .	142	FEPTMH . . . . .	282
DLE3B . . . . .	142	FEPTML . . . . .	282
DLE3C . . . . .	143	FIFO64K36/FIFO64K36P . . . . .	253
DLEA . . . . .	143	GAND2 . . . . .	160
DLEB . . . . .	144	GMX4 . . . . .	160
DLEC . . . . .	144	GNAND2 . . . . .	161
DLM . . . . .	145	GND . . . . .	161
DLM2 . . . . .	145	GNOR2 . . . . .	162
DLM2A . . . . .	147	GOR2 . . . . .	162
DLM2B . . . . .	147	GXOR2 . . . . .	163
DLM3 . . . . .	148	HA1 . . . . .	163
DLM3A . . . . .	148	HA1A . . . . .	164
DLM4 . . . . .	149	HA1B . . . . .	164
DLM4A . . . . .	149	HA1C . . . . .	165
DLM8A . . . . .	150	HCLKBIBUF . . . . .	257
DLM8B . . . . .	151	HCLKBUF . . . . .	259
DLMA . . . . .	152	HCLKBUF_LVDS; HCLKBUF_LVPECL . . . . .	299
DLME1A . . . . .	152	HCLKBUF_X . . . . .	294
DLP1 . . . . .	153	HCLKINT . . . . .	69
DLP1A . . . . .	153	IBDL . . . . .	265
DLP1B . . . . .	154	IBUF . . . . .	283
DLP1C . . . . .	154	INBUF . . . . .	259
DLP1D . . . . .	155	INBUF_LVDS; INBUF_LVPECL . . . . .	298
DLP1E . . . . .	155	INBUF_X . . . . .	289
DXAND7 . . . . .	156	INV . . . . .	165

INVA .....	166	NAND3B.....	184
INVD .....	166	NAND3C.....	184
IOCLKBUF .....	283	NAND4.....	185
IODFE .....	105	NAND4A.....	185
IODFEC .....	106	NAND4B.....	186
IODFEP .....	106	NAND4C.....	186
IOPCLBUF .....	284	NAND4D.....	187
IR .....	265	NAND5B.....	187
IREC .....	284	NAND5C.....	188
IREP .....	285	NAND5D.....	188
IRI .....	266	NOR2.....	189
JKF .....	167	NOR2A.....	189
JKF1B .....	168	NOR2B.....	190
JKF2A .....	168	NOR3.....	191
JKF2B .....	169	NOR3A.....	191
JKF2C .....	169	NOR3B.....	192
JKF2D .....	170	NOR3C.....	192
JKF3A .....	170	NOR4.....	193
JKF3B .....	171	NOR4A.....	193
JKF3C .....	171	NOR4B.....	194
JKF3D .....	172	NOR4C.....	194
JKF4B .....	173	NOR4D.....	195
JKFPC .....	173	NOR5B.....	195
MAJ3 .....	174	NOR5C.....	196
MAJ3X .....	174	NOR5D.....	196
MAJ3XI .....	175	OA1.....	197
MATH18X18 .....	320	OA1A.....	198
MIN3 .....	175	OA1B.....	198
MIN3X .....	176	OA1C.....	199
MIN3XI .....	177	OA2.....	199
MULT1 .....	306	OA2A.....	200
MX2 .....	178	OA3.....	200
MX2A .....	178	OA3A.....	201
MX2B .....	179	OA3B.....	201
MX2C .....	179	OA4.....	202
MX4 .....	180	OA4A.....	202
MXC1 .....	180	OA5.....	203
MXT .....	181	OAI1.....	203
NAND2 .....	181	OAI2A.....	204
NAND2A .....	182	OAI3.....	204
NAND2B .....	182	OAI3A.....	205
NAND3 .....	183	OBDLHS .....	266
NAND3A .....	183	OBHS .....	267

OBUFTH . . . . .	285	RAM4RF . . . . .	244
OBUFTL . . . . .	286	RAM4RR . . . . .	245
OR2 . . . . .	207	RAM64K36 /RAM64K36P . . . . .	252
OR2A . . . . .	207	RAM8FA . . . . .	246
OR2B . . . . .	208	RAM8FF . . . . .	247
OR3 . . . . .	208	RAM8FR . . . . .	248
OR3A . . . . .	209	RAM8RA . . . . .	249
OR3B . . . . .	209	RAM8RF . . . . .	250
OR3C . . . . .	210	RAM8RR . . . . .	251
OR4 . . . . .	210	SFCNTECP1 . . . . .	308
OR4A . . . . .	211	SFCNTELDCP1 . . . . .	311
OR4B . . . . .	211	SIMBUF . . . . .	301
OR4C . . . . .	212	SRCNTECP1 . . . . .	308
OR4D . . . . .	212	SRCNTELDCP1 . . . . .	310
OR5A . . . . .	213	SUB1 . . . . .	304
OR5B . . . . .	213	TBDLHS . . . . .	270
OR5C . . . . .	214	TBHS . . . . .	270
ORECTH . . . . .	286	TF1A . . . . .	215
ORECTL . . . . .	287	TF1B . . . . .	216
OREPTH . . . . .	287	TRIBUFF . . . . .	263
OREPTL . . . . .	288	TRIBUFF_X . . . . .	296
ORH . . . . .	267	VCC. . . . .	216
ORIH . . . . .	268	XA1 . . . . .	217
ORITH . . . . .	268	XA1A . . . . .	217
ORTH . . . . .	269	XA1B . . . . .	218
OUTBUF . . . . .	260	XA1C . . . . .	218
OUTBUF_LVDS; OUTBUF_LVPECL . . . . .	299	XAI1 . . . . .	219
OUTBUF_X . . . . .	295	XAI1A. . . . .	219
PLL; PLLFB . . . . .	316	XNOR2 . . . . .	220
PLLHCLK . . . . .	318	XNOR3 . . . . .	220
PLLIINT . . . . .	317	XNOR4. . . . .	224
PLLOUT . . . . .	317	XO1 . . . . .	221
PLLRCCLK . . . . .	318	XO1A . . . . .	221
QCLKBIBUF . . . . .	261	XOR2 . . . . .	222
QCLKBIBUFI . . . . .	261	XOR3 . . . . .	222
QCLKBUF . . . . .	262	XOR4 . . . . .	223
QCLKBUFI . . . . .	262	ZOR3 . . . . .	225
QCLKINT . . . . .	214	ZOR3I . . . . .	225
QCLKINTI . . . . .	215		
RAM4FA . . . . .	240		
RAM4FF . . . . .	241		
RAM4FR . . . . .	242		
RAM4RA . . . . .	243		

---

## **Combinational/Sequential Macros**



## AND2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input AND

### Truth Table

A	B	Y
X	0	0
0	X	0
1	1	1

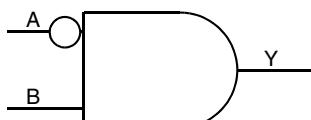
**Input**  
A, B

**Output**  
Y

Family	Modules	
	Seq	Comb
All		1

## AND2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input AND with active low A Input

### Truth Table

A	B	Y
X	0	0
0	1	1
1	X	0

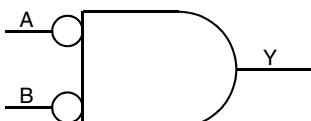
**Input**  
A, B

**Output**  
Y

Family	Modules	
	Seq	Comb
All		1

## AND2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input AND with active low Inputs

### Truth Table

A	B	Y
0	0	1
X	1	0
1	X	0

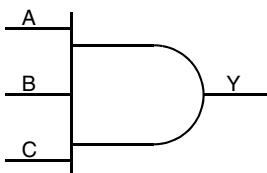
Input  
A, B

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## AND3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input AND

### Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

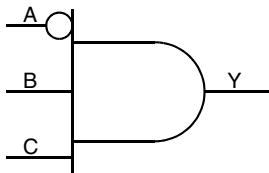
Input  
A, B,C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## AND3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input AND with active low A-Input

### Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	1	1	1
1	X	X	0

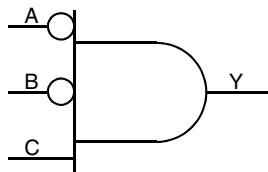
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## AND3B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input AND with active low A- and B-Inputs

### Truth Table

A	B	C	Y
X	X	0	0
0	0	1	1
X	1	X	0
1	X	X	0

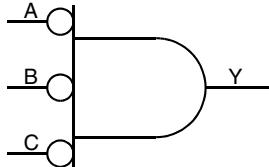
Input  
A, B,C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## AND3C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input AND with active low Inputs

### Truth Table

A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

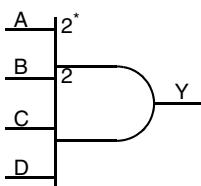
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## AND4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND

### Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

Input  
A, B, C, D

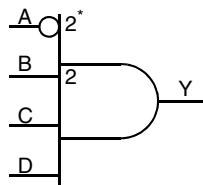
Output  
Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

\* A 2 on the symbol implies 2 logic module delays, only for ACT 1 and MX.

## AND4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND with active low A-Input

### Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	1	1	1	1
1	X	X	X	0

### Input

A, B, C, D

### Output

Y

### Family

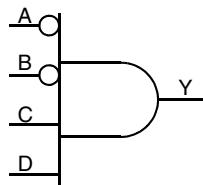
### Modules

	Seq	Comb
MX/ACT1		2
Others		1

\* A 2 on the symbol implies 2 logic module delays, only for ACT 1 and MX.

## AND4B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND with active low A- and B-Inputs

### Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	1	1	1
X	1	X	X	0
1	X	X	X	0

### Input

A, B, C, D

### Output

Y

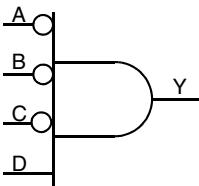
### Family

### Modules

	Seq	Comb
All		1

## AND4C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C, D	Y

### Function

4-Input AND with active low A-, B-, and C-Inputs

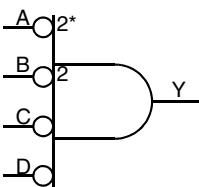
### Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	0	1	1
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Family	Modules	
	Seq	Comb
All		1

## AND4D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C, D	Y

### Function

4-Input AND with active low Inputs

### Truth Table

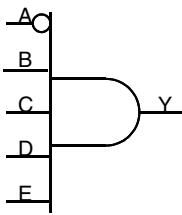
A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Family	Modules	
	Seq	Comb
SX, SX-A, eX		1
Others		2

\* A 2 on the symbol implies 2 logic module delays, except SX, SX-A, and eX.

## AND5A

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D, E

Output  
Y

### Function

5-Input AND with active low A input

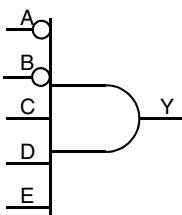
### Truth Table

A	B	C	D	E	Y
0	1	1	1	1	1
1	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Family	Modules	
	Seq	Comb
All listed		1

## AND5B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D, E

Output  
Y

### Function

5-Input AND with active low A-, and B-Inputs

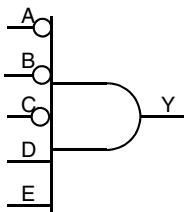
### Truth Table

A	B	C	D	E	Y
X	X	X	X	0	0
X	X	X	0	X	0
X	X	0	X	X	0
0	0	1	1	1	1
X	1	X	X	X	0
1	X	X	X	X	0

Family	Modules	
	Seq	Comb
All		1

## AND5C

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D, E

Output  
Y

### Function

5-Input AND with active low A-, B- and C-Inputs

### Truth Table

A	B	C	D	E	Y
0	0	0	1	1	1
1	X	X	X	X	0
X	1	X	X	X	0
X	X	1	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Family

Modules

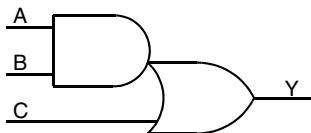
Seq Comb

SX, SX-A, eX, Axcelerator

1

## A01

ACT1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-OR

### Truth Table

A	B	C	Y
X	0	0	0
X	X	1	1
0	X	0	0
1	1	X	1

Family

Modules

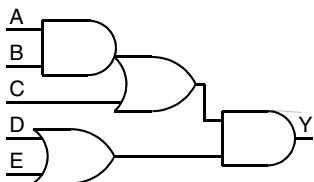
Seq Comb

All

1

## AO10

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input

A, B, C, D, E

Output

Y

### Function

5-Input AND-OR-AND

### Truth Table

A	B	C	D	E	Y
X	X	X	0	0	0
X	0	0	X	X	0
X	X	1	X	1	1
X	X	1	1	X	1
0	X	0	X	X	0
1	1	X	X	1	1
1	1	X	1	X	1

Family

Modules

Seq

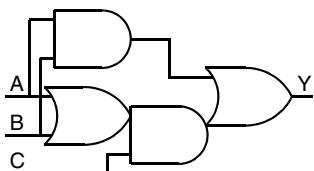
Comb

All except ACT1 and MX

1

## AO11

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input

A, B, C

Output

Y

### Function

3-Input AND-OR

### Truth Table

A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

Family

Modules

Seq

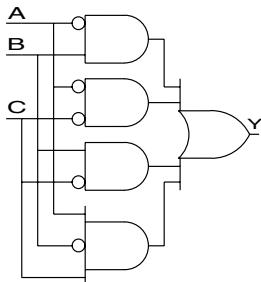
Comb

All except ACT1 and MX

1

## AO12

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

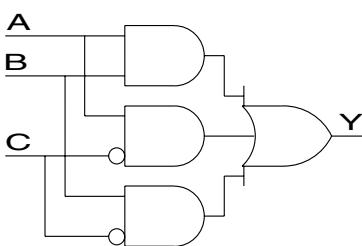
3-Input AND-OR

### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

## AO13

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input AND-OR

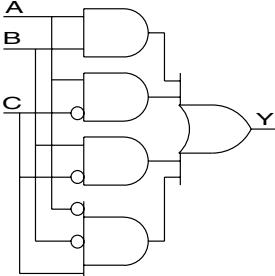
### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

## AO14

SX, SX-A, SX-S, eX, Axcelerator

	<b>Input</b> A, B, C	<b>Output</b> Y
-----------------------------------------------------------------------------------	-------------------------	--------------------

### Function

3-Input AND-OR

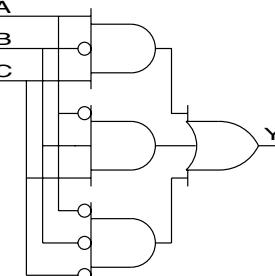
### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

## AO15

SX, SX-A, SX-S, eX, Axcelerator

	<b>Input</b> A, B, C	<b>Output</b> Y
------------------------------------------------------------------------------------	-------------------------	--------------------

### Function

3-Input AND-OR

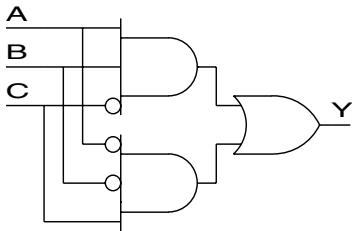
### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

## AO16

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

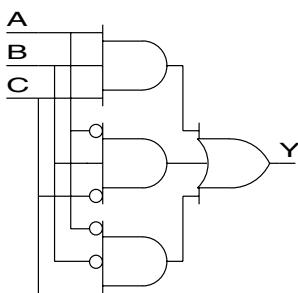
3-Input AND-OR

### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

## AO17

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-OR

### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

## Family

### Modules

Seq      Comb

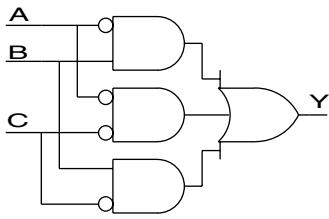
All listed

1

Family	Modules
Seq	Comb
All listed	1

## AO18

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-OR

### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

### Family

### Modules

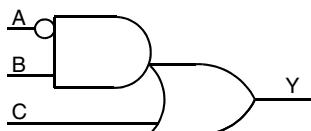
Seq      Comb

All listed

1

## AO1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-OR with active low A-Input

### Truth Table

A	B	C	Y
X	0	0	0
X	X	1	1
0	1	X	1
1	X	0	0

### Family

### Modules

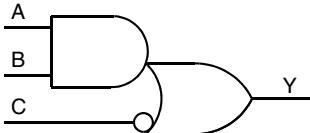
Seq      Comb

All listed

1

## AO1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-OR with active low C-Input

### Truth Table

A	B	C	Y
X	X	0	1
X	0	1	0
0	X	1	0
1	1	X	1

### Family

### Modules

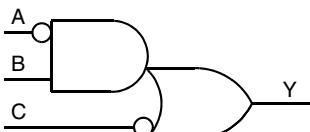
Seq      Comb

All

1

## AO1C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-OR with active low A- and C-Inputs

### Truth Table

A	B	C	Y
X	X	0	1
X	0	1	0
0	1	X	1
1	X	1	0

### Family

### Modules

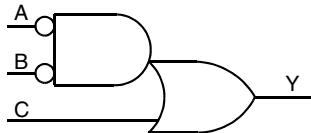
Seq      Comb

All

1

## AO1D

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input AND-OR with active low A- and B-Inputs

### Truth Table

A	B	C	Y
0	0	X	1
X	1	0	0
X	X	1	1
1	X	0	0

Input  
A, B, C

Output  
Y

### Family

### Modules

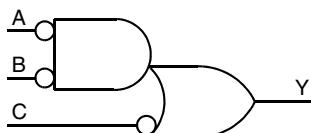
Seq      Comb

All listed above

1

## AO1E

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input AND-OR with active low Inputs

### Truth Table

A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

Input  
A, B, C

Output  
Y

### Family

### Modules

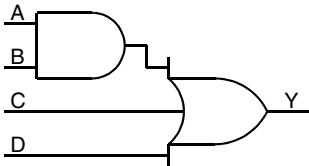
Seq      Comb

All listed above

1

## AO2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR

### Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	X	0	0	0
1	1	X	X	1

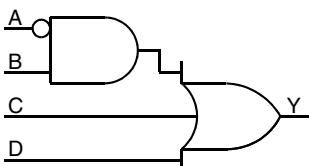
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
ALL		1

## AO2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR with active low A-Input

### Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	1	X	X	1
1	X	0	0	0

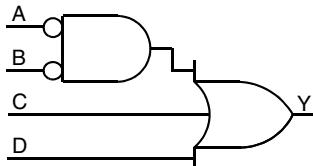
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
ALL		1

## AO2B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR with active low A and B-Inputs

### Truth Table

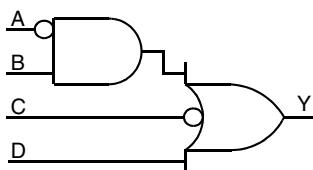
A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed above		1

## AO2C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR with active low A- and C-Inputs

### Truth Table

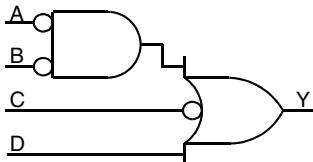
A	B	C	D	Y
1	X	1	0	0
X	0	1	0	0
0	1	X	X	1
X	X	0	X	1
X	X	X	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed above		1

## AO2D

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR with active low A-, B- and C-Inputs

### Truth Table

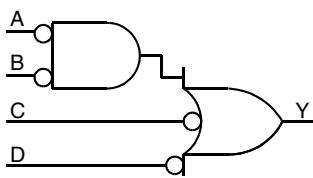
A	B	C	D	Y
X	X	0	X	1
0	0	X	X	1
X	1	1	0	0
X	X	X	1	1
1	X	1	0	0

<b>Input</b> A, B, C, D	<b>Output</b> Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed above		1

## AO2E

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR with active low Inputs

### Truth Table

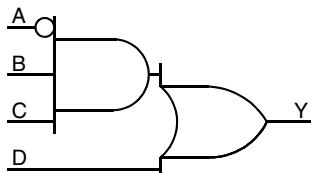
A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

<b>Input</b> A, B, C, D	<b>Output</b> Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed above		1

## AO3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR with active low A Input

### Truth Table

A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	1	1	X	1
1	X	X	0	0

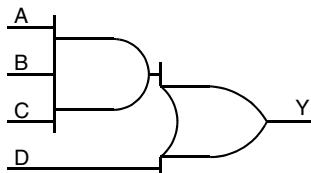
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
ALL		1

## AO3A

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR

### Truth Table

A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	X	X	0	0
1	1	1	X	1

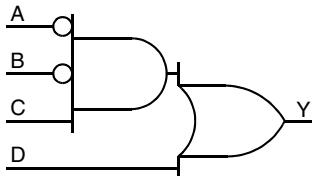
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
All listed above		1

## AO3B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4 Input AND-OR with active low A-, B- Inputs

### Truth Table

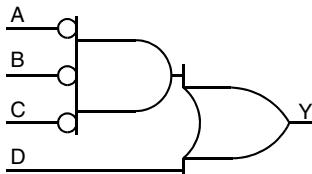
A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
0	0	1	X	1
X	1	X	0	0
1	X	X	0	0

<b>Input</b> A, B, C, D	<b>Output</b> Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed above		1

## AO3C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR with active low A-, B-, C- Inputs

### Truth Table

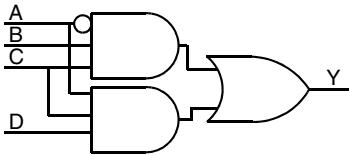
A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

<b>Input</b> A, B, C, D	<b>Output</b> Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed above		1

## AO4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input AND-OR

### Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	X	0	0
0	0	X	X	0
0	1	1	X	1
1	X	1	1	1
1	X	X	0	0
X	1	1	1	1

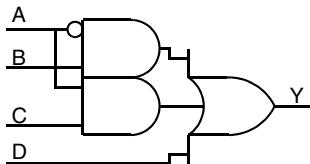
Family  
ALL

Modules  
Seq      Comb

1

## AO5A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input AND-OR

### Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
0	0	X	0	0
0	1	X	X	1
1	X	1	X	1
1	X	0	0	0
X	1	1	X	1

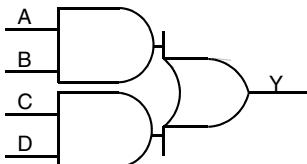
Family  
ALL

Modules  
Seq      Comb

1

## AO6

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



<b>Input</b>	<b>Output</b>
A, B, C, D	Y

### Function

2-wide 4-Inputs AND-OR

### Truth Table

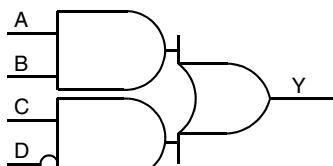
<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>	<b>Y</b>
X	0	X	0	0
X	0	0	X	0
X	X	1	1	1
0	X	X	0	0
0	X	0	X	0
1	1	X	X	1

### Modules

<b>Family</b>	<b>Modules</b>	
	<b>Seq</b>	<b>Comb</b>
All listed above		1

## AO6A

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



<b>Input</b>	<b>Output</b>
A, B, C, D	Y

### Function

2-wide 4-Inputs AND-OR with active low D-Input

### Truth Table

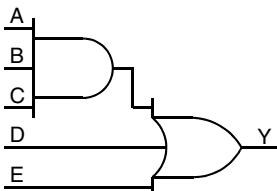
<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>	<b>Y</b>
X	0	0	X	0
X	X	1	0	1
X	0	X	1	0
0	X	0	X	0
0	X	X	1	0
1	1	X	X	1

### Modules

<b>Family</b>	<b>Modules</b>	
	<b>Seq</b>	<b>Comb</b>
All listed above		1

## AO7

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D, E

Output  
Y

### Function

5-Input AND-OR

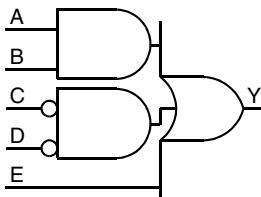
### Truth Table

A	B	C	D	E	Y
X	X	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	0	X	0	0	0
0	X	X	0	0	0
1	1	1	X	X	1

Family	Modules	
	Seq	Comb
All listed above		1

## AO8

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D, E

Output  
Y

### Function

5-Input AND-OR with active low C- and D-Inputs

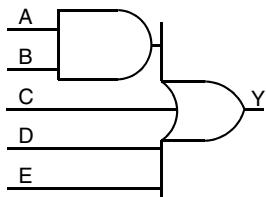
### Truth Table

A	B	C	D	E	Y
X	X	0	0	X	1
X	0	X	1	0	0
X	X	X	X	1	1
X	0	1	X	0	0
0	X	X	1	0	0
0	X	1	X	0	0
1	1	X	X	X	1

Family	Modules	
	Seq	Comb
All listed above		1

## AO9

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



<b>Input</b>	<b>Output</b>
A, B, C, D, E	Y

### Function

5-Input AND-OR

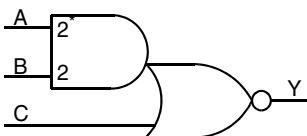
### Truth Table

<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>	<b>E</b>	<b>Y</b>
X	0	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1
0	X	0	0	0	0
1	1	X	X	X	1

<b>Family</b>	<b>Modules</b>	
	<b>Seq</b>	<b>Comb</b>
All listed above		1

## AOI1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



<b>Input</b>	<b>Output</b>
A, B, C	Y

### Function

3-Input AND-OR-INVERT

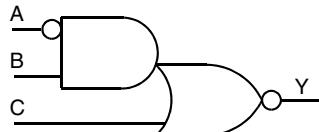
### Truth Table

<b>A</b>	<b>B</b>	<b>C</b>	<b>Y</b>
X	0	0	1
X	X	1	0
0	X	0	1
1	1	X	0

<b>Family</b>	<b>Modules</b>	
	<b>Seq</b>	<b>Comb</b>
ACT 1, MX		2
Others		1

## AOI1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input AND-OR-INVERT with active low A-Input

### Truth Table

A	B	C	Y
X	0	0	1
X	X	1	0
0	1	X	0
1	X	0	1

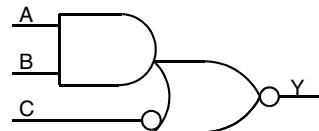
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
ALL		1

## AOI1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input AND-OR-INVERT with active low C-Input

### Truth Table

A	B	C	Y
X	X	0	0
X	0	1	1
0	X	1	1
1	1	X	0

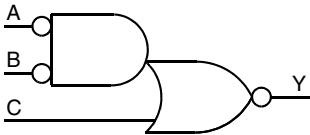
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
ALL		1

## AOI1C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3 Input AND-OR-INVERT with active low A- and B-Inputs

### Truth Table

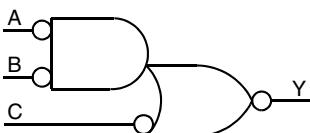
A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

<b>Input</b> A, B, C	<b>Output</b> Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed above		1

## AOI1D

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input AND-OR-INVERT with active low Inputs

### Truth Table

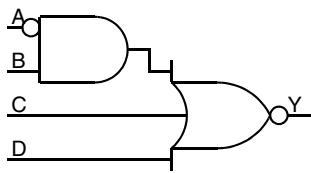
A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

<b>Input</b> A, B, C	<b>Output</b> Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All listed		1

## AOI2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR-INVERT with active low A-Input

### Truth Table

A	B	C	D	Y
X	0	0	0	1
X	X	X	1	0
X	X	1	X	0
0	1	X	X	0
1	X	0	0	1

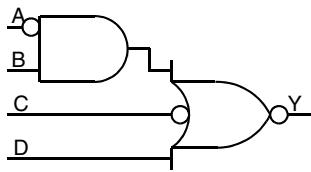
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
ALL		1

## AOI2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR-INVERT with active low A- and C-Inputs

### Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	1	0	1
X	X	X	1	0
0	1	X	X	0
1	X	1	0	1

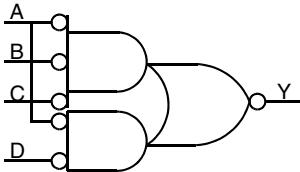
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
ALL		1

## AOI3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input AND-OR-INVERT with active low Inputs

### Truth Table

A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

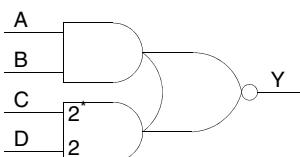
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
ALL		1

## AOI4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-wide 4-Inputs AND-OR-INVERT

### Truth Table

A	B	C	D	Y
X	0	X	0	1
X	0	0	X	1
X	X	1	1	0
0	X	X	0	1
0	X	0	X	1
1	1	X	X	0

Input  
A, B, C, D

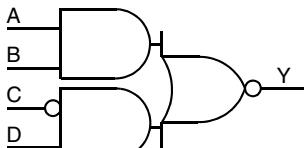
Output  
Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1
Others		2

\* A 2 on the symbol implies 2 logic module delays for all families except SX, SX-A, SX-S, and eX.

## AOI4A

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

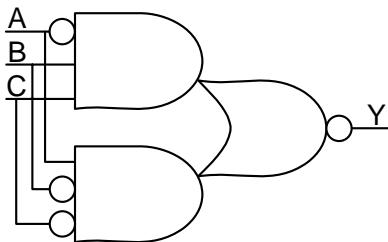
2-wide 4-Inputs AND-OR-INVERT with active low C-Input

### Truth Table

A	B	C	D	Y
X	0	X	0	1
X	X	0	1	0
X	0	1	X	1
0	X	X	0	1
0	X	1	X	1
1	1	X	X	0

## AOI5

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-OR-INVERT

### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0

Family	Modules
Seq	Comb
All listed	1

Family

Modules

Seq

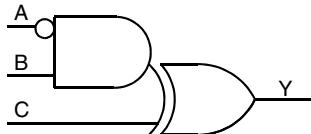
Comb

All listed

1

## AX1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-XOR with active low A-Input

### Truth Table

A	B	C	Y
X	0	0	0
X	0	1	1
0	1	0	1
0	1	1	0
1	X	0	0
1	X	1	1

Family

### Modules

Seq

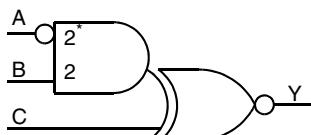
Comb

All listed

1

## AX1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-XOR-INVERT with active low A-Input

### Truth Table

A	B	C	Y
X	0	0	1
X	0	1	0
0	1	0	0
0	1	1	1
1	X	0	1
1	X	1	0

Family

### Modules

Seq

Comb

ACT 1, MX, SX, SX-A, SX-S, eX

1

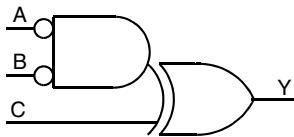
Others

2

\* A 2 on the symbol implies 2 logic module delays for all families except ACT 1, MX, SX, SX-A, SX-S and eX.

## AX1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-XOR with active low A- and B-Inputs

### Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
X	1	0	0
X	1	1	1
1	X	0	0
1	X	1	1

Family

Modules

Seq

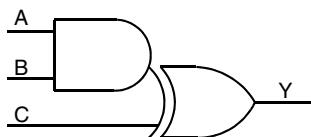
Comb

All

1

## AX1C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input AND-XOR

### Truth Table

A	B	C	Y
X	0	0	0
X	0	1	1
0	X	0	0
0	X	1	1
1	1	0	1
1	1	1	0

Family

Modules

Seq

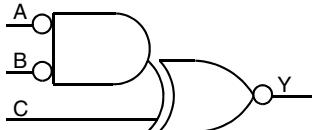
Comb

All listed

1

## AX1D

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input AND-XNOR

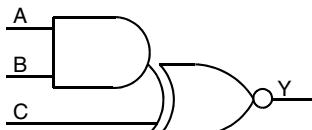
### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

## AX1E

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input AND-XNOR

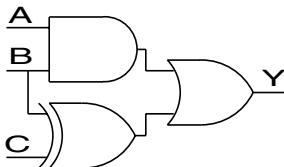
### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

## AXO1

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input Combinatorial Gate

### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	1

### Family

### Modules

Seq

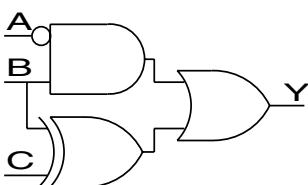
Comb

All listed

1

## AXO2

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input Combinatorial Gate

### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

### Family

### Modules

Seq

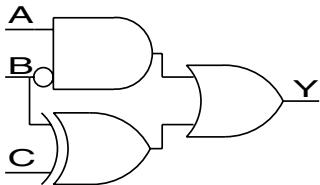
Comb

All listed

1

## AXO3

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input Combinatorial Gate

### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

### Family

### Modules

Seq

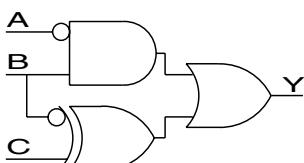
Comb

All listed

1

## AXO5

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input Combinatorial Gate

### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

### Family

### Modules

Seq

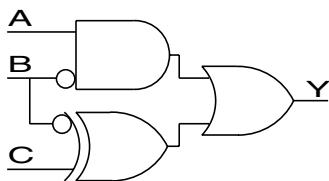
Comb

All listed

1

## AXO6

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input Combinatorial Gate

### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

### Family

### Modules

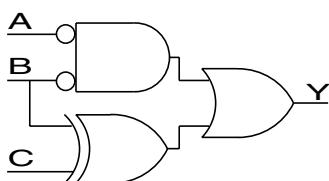
Seq

Comb

All listed	1
------------	---

## AXO7

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input Combinatorial Gate

### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

### Family

### Modules

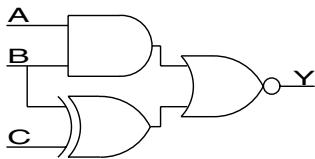
Seq

Comb

All listed	1
------------	---

## AXOI1

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input Combinatorial Gate

### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

Family

Modules

Seq

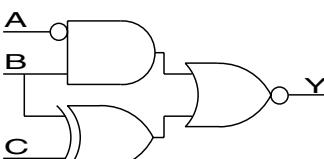
Comb

All listed

1

## AXOI2

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input Combinatorial Gate

### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Family

Modules

Seq

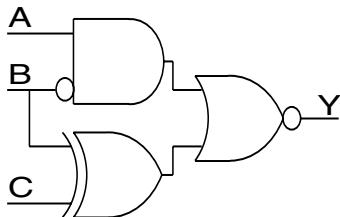
Comb

All listed

1

## AXO13

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input Combinatorial Gate

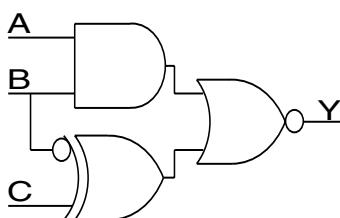
### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

## AXO14

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input Combinatorial Gate

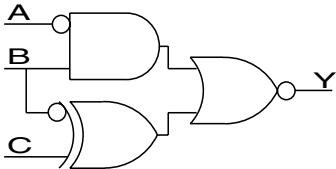
### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
All listed		1

## AXO15

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input Combinatorial Gate

### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Family

### Modules

Seq

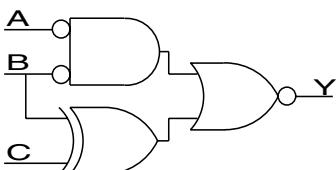
Comb

All listed

1

## AXO17

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input Combinatorial Gate

### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

Family

### Modules

Seq

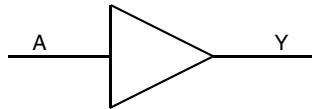
Comb

All listed

1

## BUFA

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Buffer, with active low Input and Output

### Truth Table

A	Y
0	0
1	1

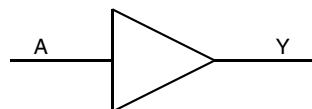
Input  
A

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## BUFF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Buffer

### Truth Table

A	Y
0	0
1	1

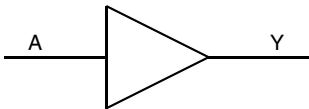
Input  
A

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## BUFD

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Buffer

NOTE: The Combiner will not remove this macro

### Truth Table

A	Y
0	0
1	1

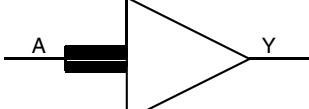
Input  
A

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## CLKINT

ACT 2, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Internal Clock Interface

### Truth Table

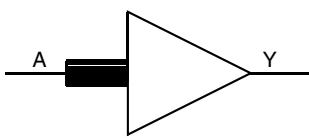
A	Y
0	0
1	1

Input  
A

Output  
Y

NOTE: CLKINT does not use any modules.

For more information on the Global Clock Network, refer to the latest Actel datasheet.

**Function**

Internal Clock Interface

**Truth Table**

A	Y
0	0
1	1

**Input**

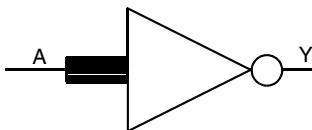
A

**Output**

Y

NOTE: CLKINT does not use any modules.

For more information on the Global Clock Network, refer to the latest Actel datasheet.

**Function**

Inverting Internal Clock Interface

**Truth Table**

A	Y
0	1
1	0

**Input**

A

**Output**

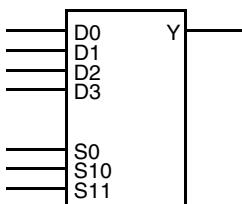
Y

NOTE: CLKINTI does not use any modules.

For more information on the Global Clock Network, refer to Actel's Databook.

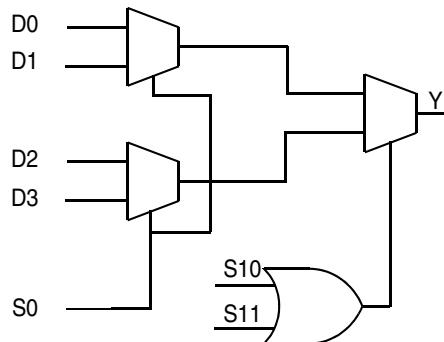
## CM7

ACT2/1200XL, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Full Combinational Module



Input	Output
D0, D1, D2, D3, S0, S10, S11	y

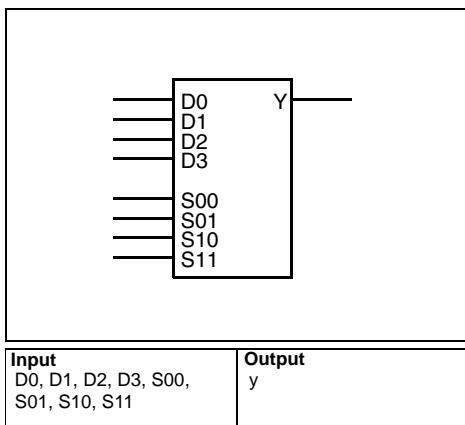
Truth Table

S11	S10	S0	Y
0	0	0	D0
0	0	1	D1
X	1	0	D2
1	X	0	D2
X	1	1	D3
1	X	1	D3

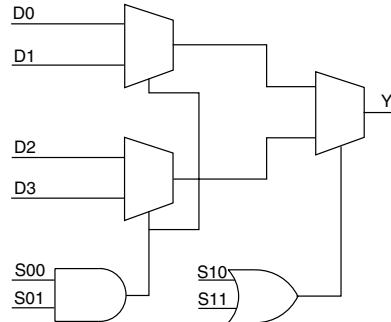
Family	Modules	
	Seq	Comb
All listed		1

## CM8

ACT2/1200XL, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



**Function**  
Full Combinational Module



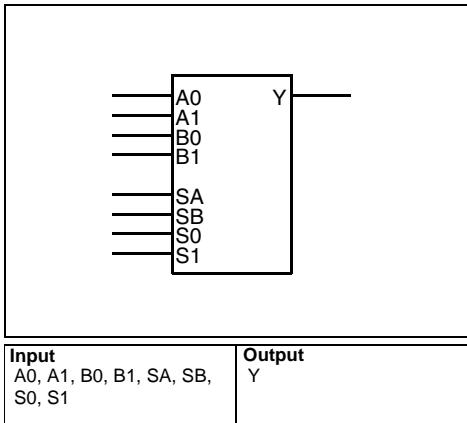
Truth Table

S11	S10	S01	S00	Y
0	0	X	0	D0
0	0	0	X	D0
0	0	1	1	D1
X	1	X	0	D2
X	1	0	X	D2
1	X	X	0	D2
1	X	0	X	D2
X	1	1	1	D3
1	X	1	1	D3

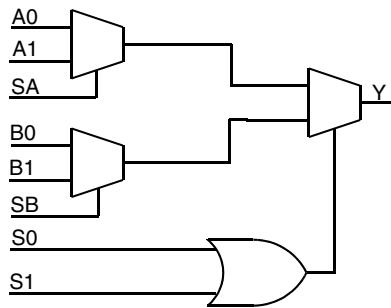
Family	Modules	
	Seq	Comb
All listed		1

## CM8A

ACT 1, MX



**Function**  
Full Combinational Module



**Input**  
A0, A1, B0, B1, SA, SB,  
S0, S1

**Output**  
Y

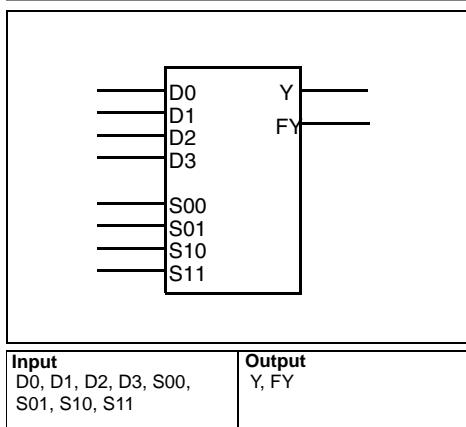
Truth Table

S0	S1	SA	SB	Y
0	0	0	X	A0
0	0	1	X	A1
1	X	X	0	B0
X	1	X	0	B0
1	X	X	1	B1
X	1	X	1	B1

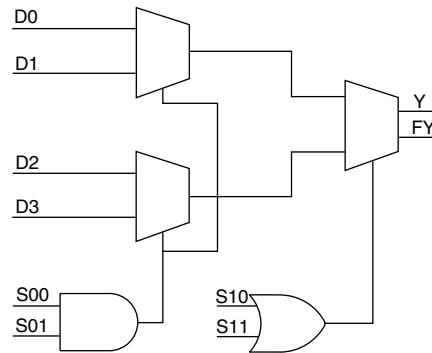
Family	Modules	
	Seq	Comb
ACT 1, MX		1

## CM8F

SX, SX-A, SX-S, eX, Axcelerator



**Function**  
Full Combinational Module with fast output



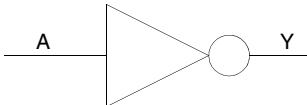
Truth Table

S11	S10	S01	S00	Y	FY
0	0	X	0	D0	D0
0	0	0	X	D0	D0
0	0	1	1	D1	D1
X	1	X	0	D2	D2
X	1	0	X	D2	D2
1	X	X	0	D2	D2
1	X	0	X	D2	D2
X	1	1	1	D3	D3
1	X	1	1	D3	D3

Family	Modules	
	Seq	Comb
All listed		1

## CM8INV

SX, SX-A, SX-S, eX, Axcelerator



### Function

Inverter with active low output

### Truth Table

A	Y
0	1
1	0

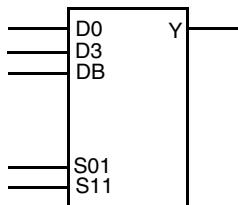
Input	Output
A	Y

Family	Modules	
	Seq	Comb
All listed		0

NOTE: This macro can drive any number of CM8 pins and will be absorbed into that module.

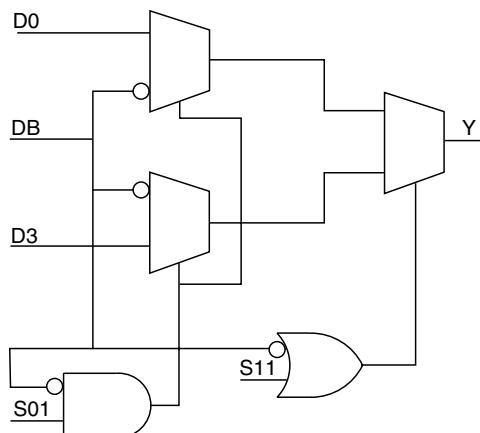
## CMA9

SX, SX-A, SX-S, eX, Axcelerator



### Function

Full Combinational Module

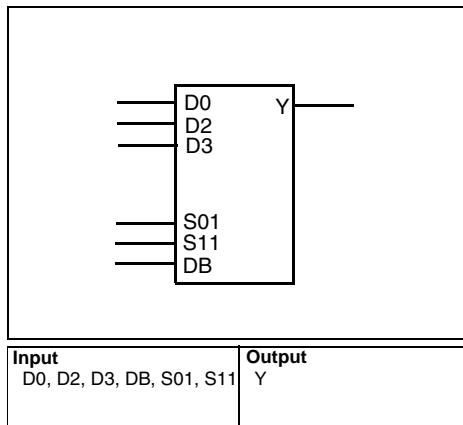


Input	Output
D0, D3, DB, S01, S11	Y

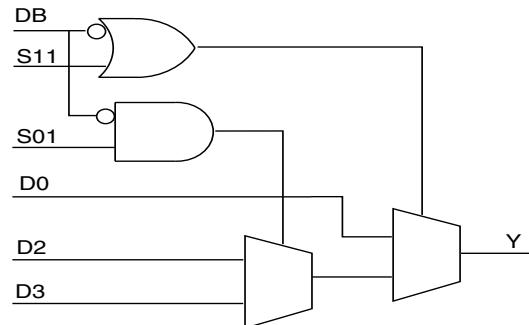
Family	Modules	
	Seq	Comb
All listed		1

## CMAF

SX, SX-A, SX-S, eX, Axcelerator



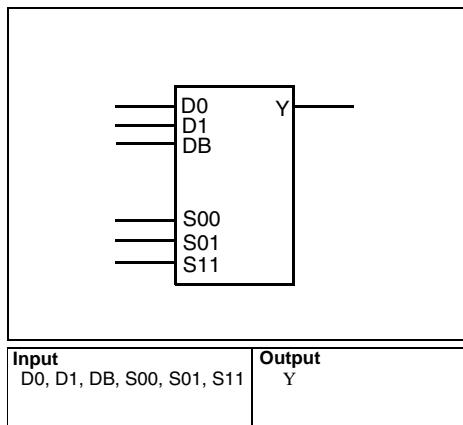
**Function**  
Full Combinational Module



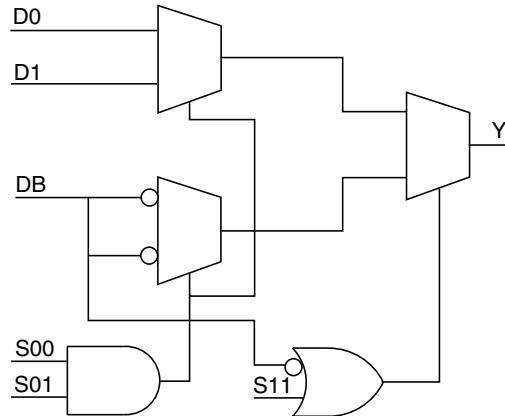
Family	Modules	
	Seq	Comb
All listed		1

## CMB3

SX, SX-A, SX-S, eX, Axcelerator



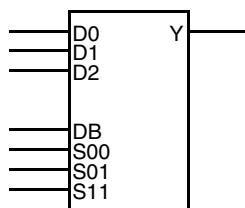
**Function**  
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

## CMB7

SX, SX-A, SX-S, eX, Axcelerator



**Input**

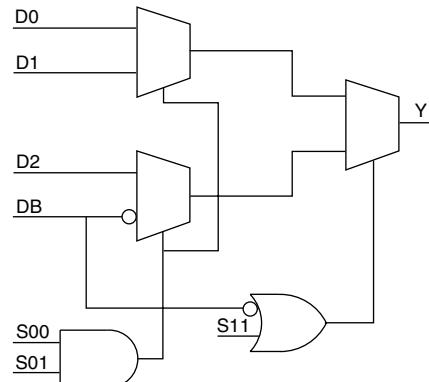
D0, D1, D2, DB, S00,  
S01, S11

**Output**

Y

### Function

Full Combinational Module



**Family**

**Modules**

Seq	Comb

1

**Input**

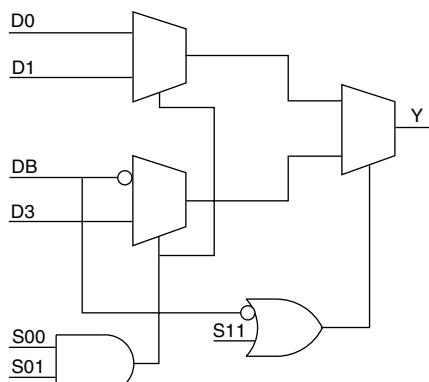
D0, D1, D3, DB, S00,  
S01, S11

**Output**

Y

### Function

Full Combinational Module



**Family**

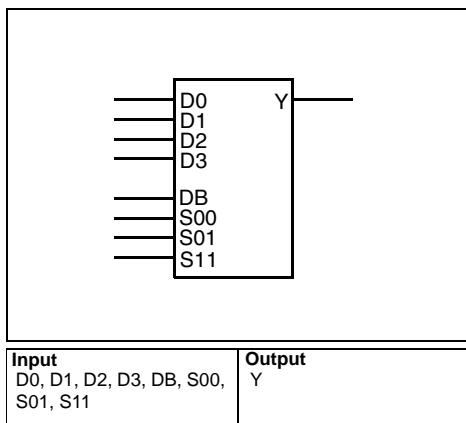
**Modules**

Seq	Comb

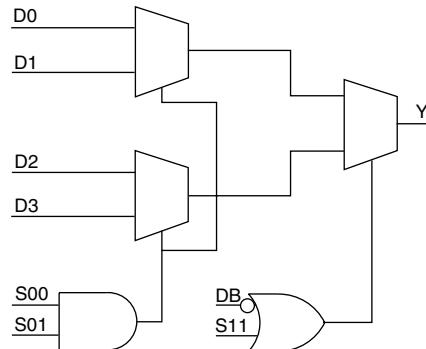
1

## CMBF

SX, SX-A, SX-S, eX, Axcelerator



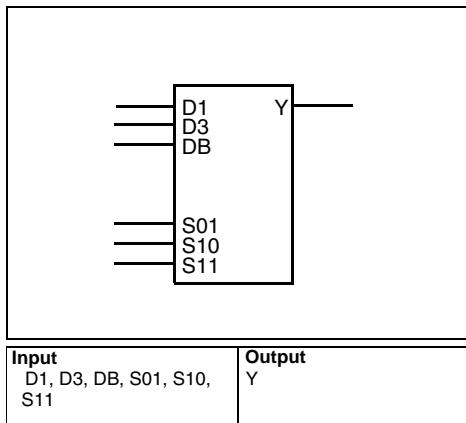
**Function**  
Full Combinational Module



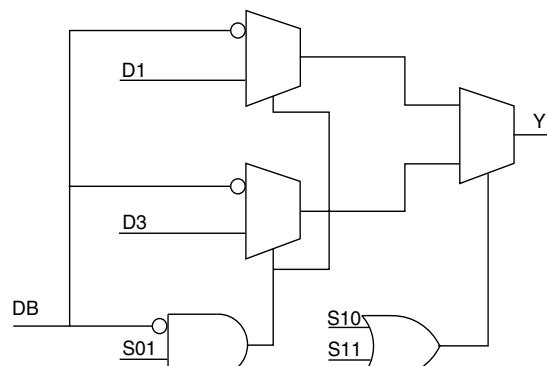
Family	Modules	
	Seq	Comb
All listed		1

## CMEA

SX, SX-A, SX-S, eX, Axcelerator



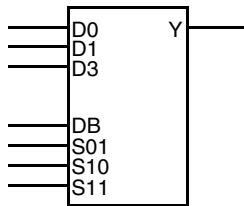
**Function**  
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

## CMEB

SX, SX-A, SX-S, eX, Axcelerator

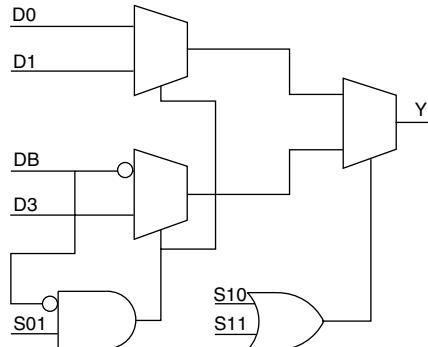


**Input**  
D0, D1, D3, DB, S01,  
S10, S11

**Output**  
Y

### Function

Full Combinational Module



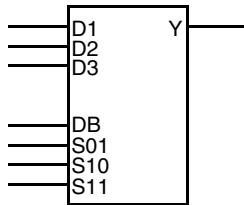
### Family

#### Modules

	Seq	Comb
All listed		1

## CMEE

SX, SX-A, SX-S, eX, Axcelerator

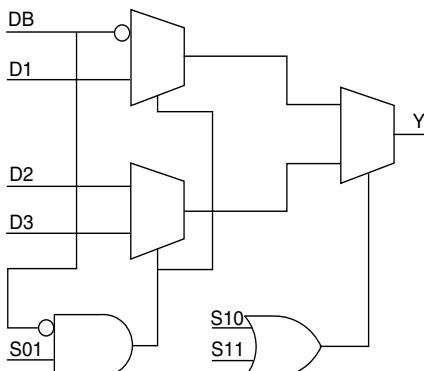


**Input**  
D1, D2, D3, DB, S01,  
S10, S11

**Output**  
Y

### Function

Full Combinational Module



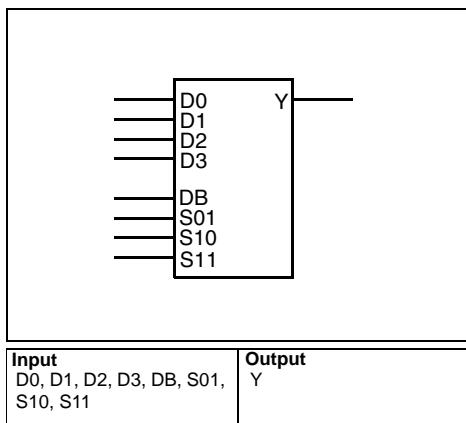
### Family

#### Modules

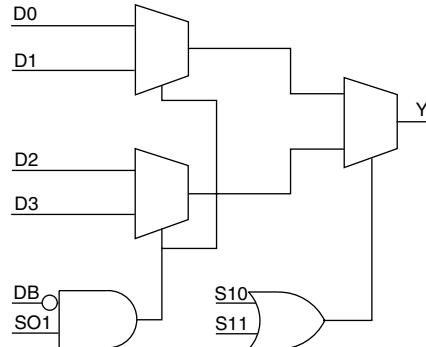
	Seq	Comb
All listed		1

## CMEF

SX, SX-A, SX-S, eX, Axcelerator



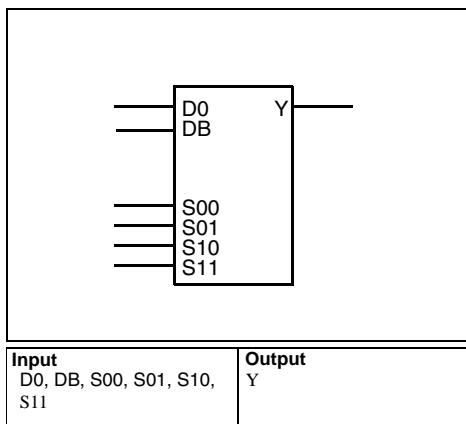
**Function**  
Full Combinational Module



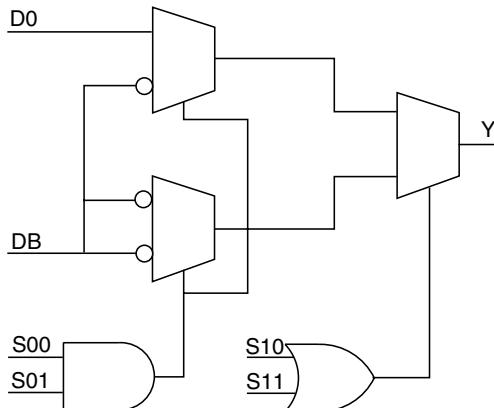
Family	Modules	
	Seq	Comb
All listed		1

## CMF1

SX, SX-A, SX-S, eX, Axcelerator



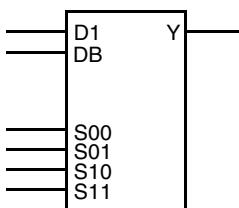
**Function**  
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

## CMF2

SX, SX-A, SX-S, eX, Axcelerator

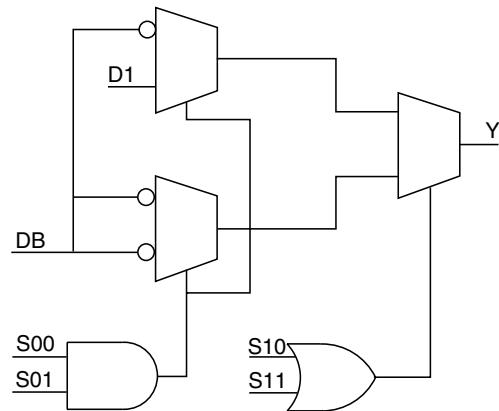


**Input**  
D1, DB, S00, S01, S10,  
S11

**Output**  
Y

### Function

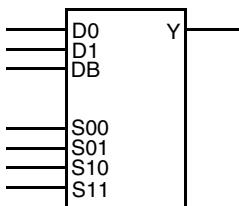
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

## CMF3

SX, SX-A, SX-S, eX, Axcelerator

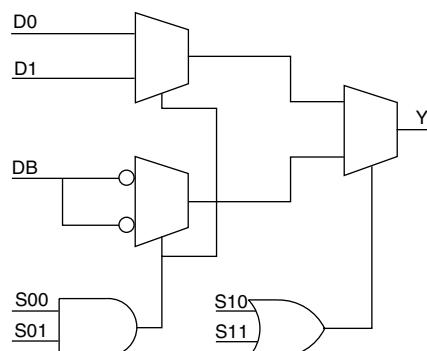


**Input**  
D0, D1, DB, S00, S01,  
S10, S11

**Output**  
Y

### Function

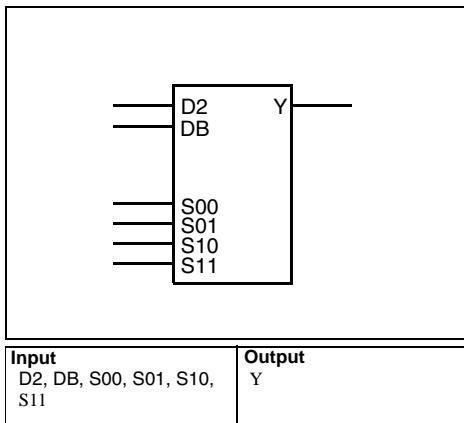
Full Combinational Module



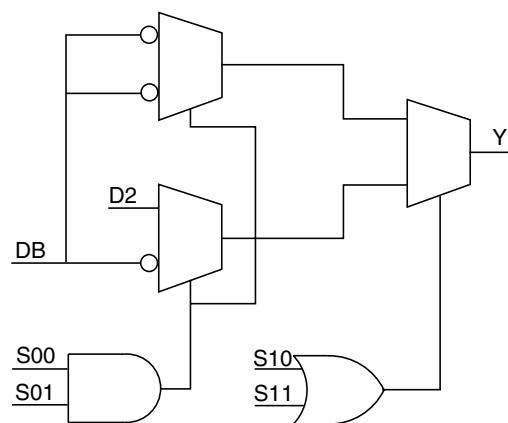
Family	Modules	
	Seq	Comb
All listed		1

## CMF4

SX, SX-A, SX-S, eX, Axcelerator



**Function**  
Full Combinational Module



**Input**

D2, DB, S00, S01, S10,  
S11

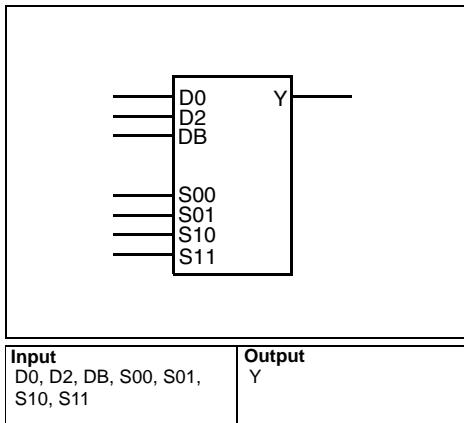
**Output**

Y

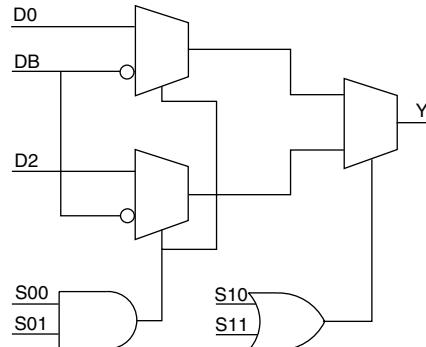
Family	Modules	
	Seq	Comb
All listed		1

## CMF5

SX, SX-A, SX-S, eX, Axcelerator



**Function**  
Full Combinational Module



**Input**

D0, D2, DB, S00, S01,  
S10, S11

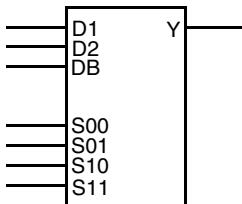
**Output**

Y

Family	Modules	
	Seq	Comb
All listed		1

## CMF6

SX, SX-A, SX-S, eX, Axcelerator

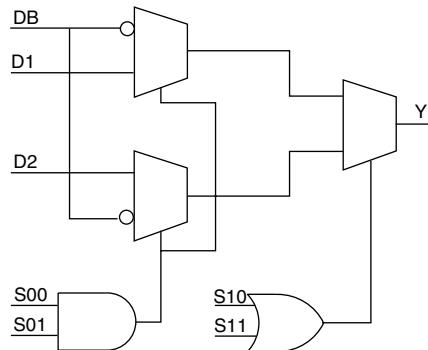


**Input**  
D1, D2, DB, S00, S01,  
S10, S11

**Output**  
Y

### Function

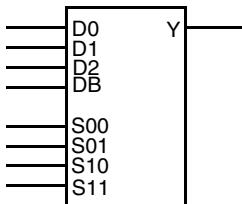
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

## CMF7

SX, SX-A, SX-S, eX, Axcelerator

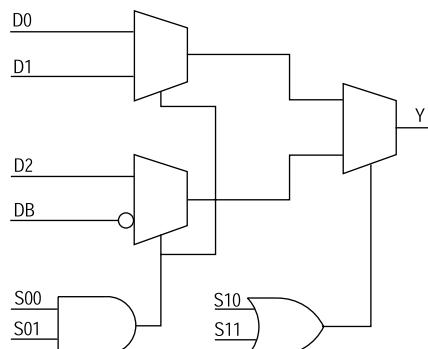


**Input**  
D0, D1, D2, DB, S00,  
S01, S10, S11

**Output**  
Y

### Function

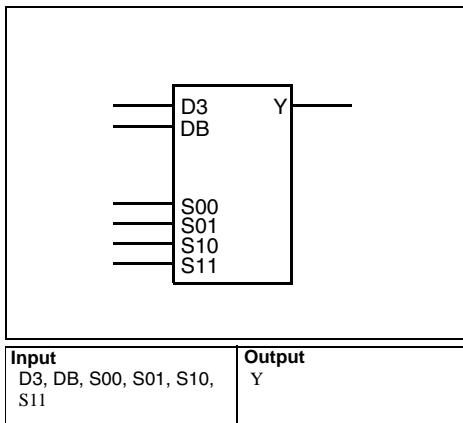
Full Combinational Module



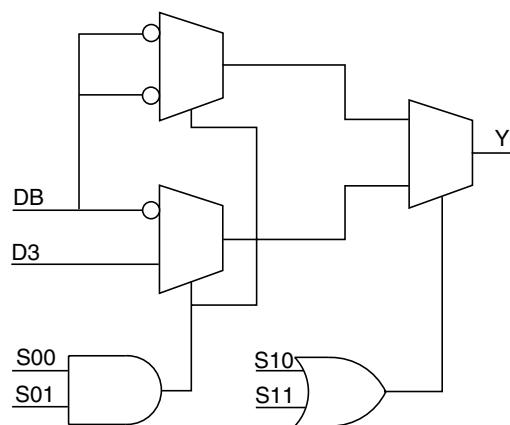
Family	Modules	
	Seq	Comb
All listed		1

## CMF8

SX, SX-A, SX-S, eX, Axcelerator



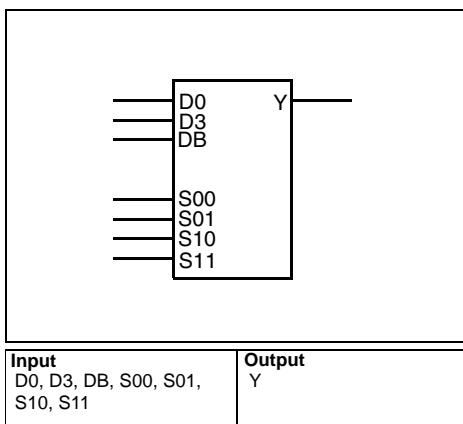
**Function**  
Full Combinational Module



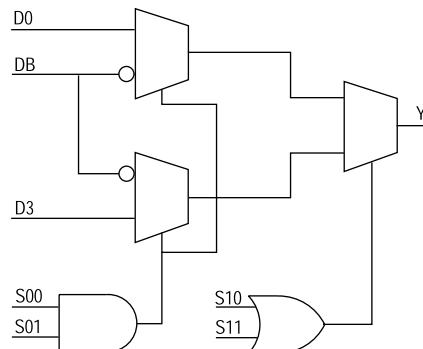
Family	Modules	
	Seq	Comb
All listed		1

## CMF9

SX, SX-A, SX-S, eX, Axcelerator



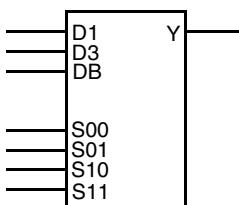
**Function**  
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

## CMFA

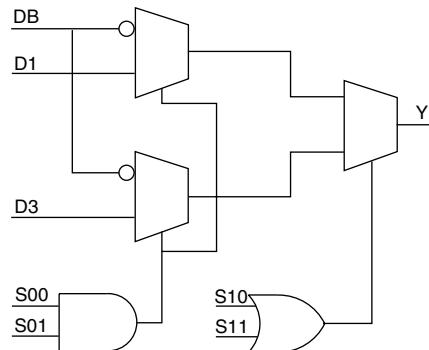
SX, SX-A, SX-S, eX, Axcelerator



Input	Output
D1, D3, DB, S00, S01, S10, S11	Y

### Function

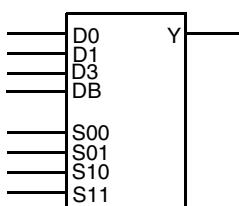
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

## CMFB

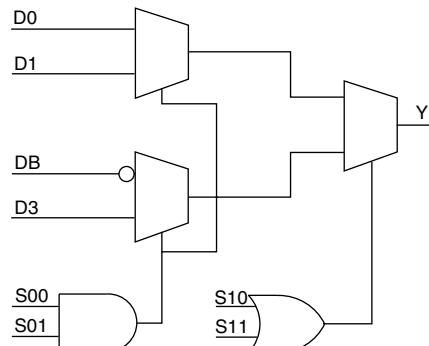
SX, SX-A, SX-S, eX, Axcelerator



Input	Output
D0, D1, D3, DB, S00, S01, S10, S11	Y

### Function

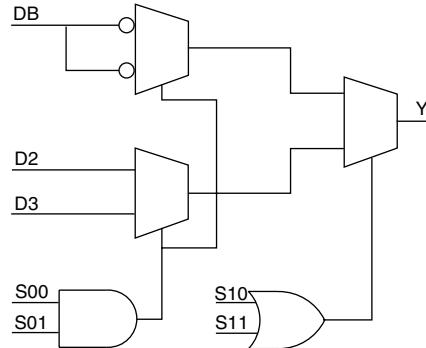
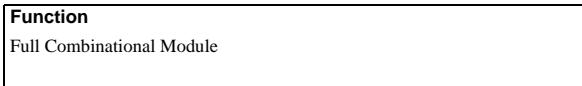
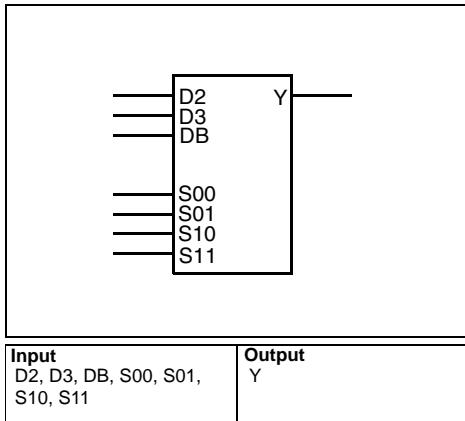
Full Combinational Module



Family	Modules	
	Seq	Comb
All listed		1

## CMFC

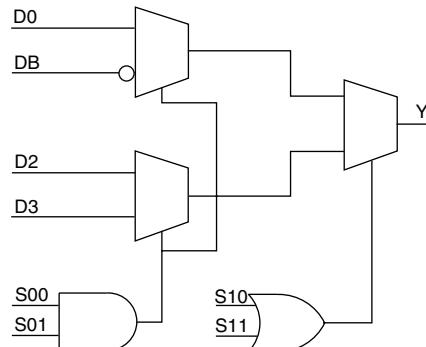
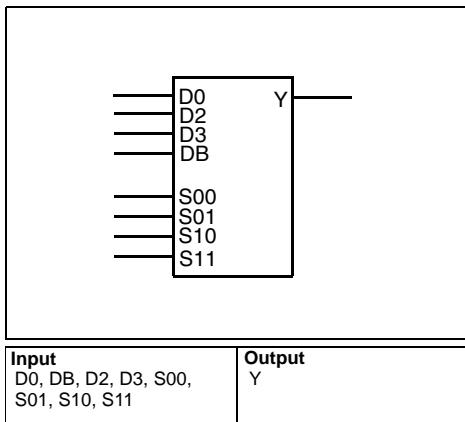
SX, SX-A, SX-S, eX, Axcelerator



Family	Modules	
	Seq	Comb
All listed		1

## CMFD

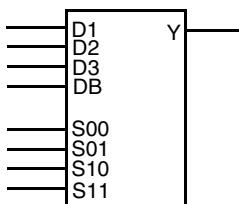
SX, SX-A, SX-S, eX, Axcelerator



Family	Modules	
	Seq	Comb
All listed		1

## CMFE

SX, SX-A, SX-S, eX, Axcelerator

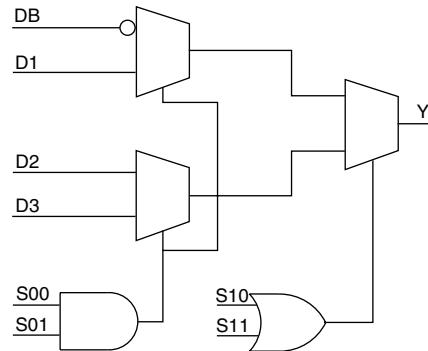


**Input**  
D1, D2, D3, DB, S00,  
S01, S10, S11

**Output**  
Y

### Function

Full Combinational Module



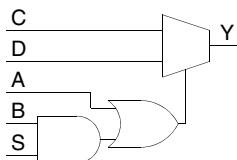
### Family

### Modules

	Seq	Comb
All listed		1

## CS1

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



**Input**  
A, S, B, C, D

**Output**  
Y

### Function

Carry Select for Implementing High Speed Adders

### Truth Table

A	S	B	C	D	Y
X	X	X	0	0	0
0	X	0	0	X	0
0	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	X	X	1	1
1	X	X	X	0	0
X	X	X	1	1	1

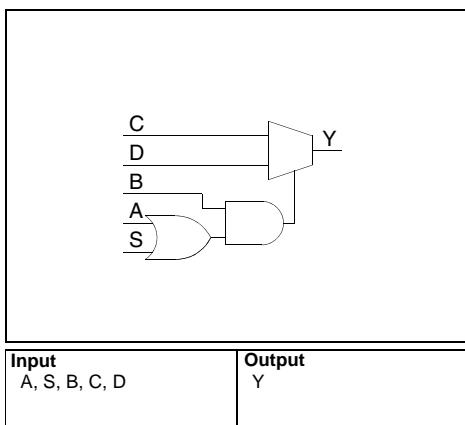
### Family

### Modules

	Seq	Comb
All listed		1

## CS2

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Carry Select for Implementing High Speed Adders

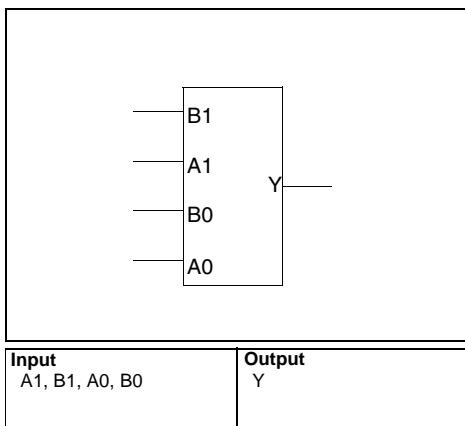
### Truth Table

A	S	B	C	D	Y
X	X	X	0	0	0
X	X	0	0	X	0
X	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	1	X	1	1
1	X	1	X	0	0
X	X	X	1	1	1

Family	Modules	
	Seq	Comb
All listed		1

## CY2A

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Carry Generator

### Truth Table

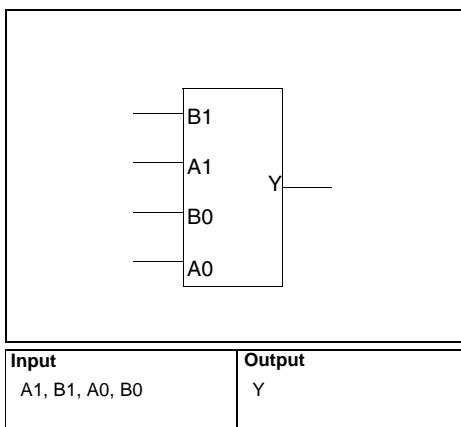
A1	B1	A0	B0	Y
X	0	X	0	0
X	0	0	X	0
0	0	X	X	0
0	X	X	0	0
0	X	0	X	0
X	1	1	1	1
1	X	1	1	1
1	1	X	X	1

Family	Modules	
	Seq	Comb
All listed		1



## CY2B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Carry Generator

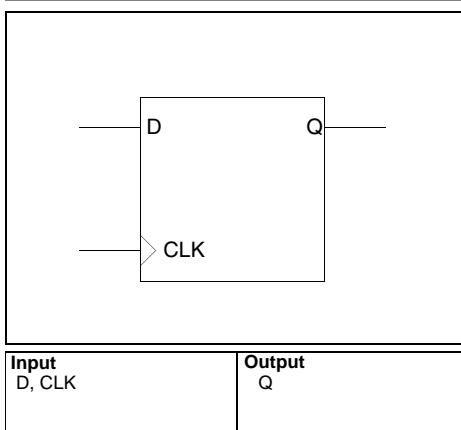
### Truth Table

A1	B1	A0	B0	Y
X	0	0	0	0
0	0	X	X	0
0	X	0	0	0
X	1	X	1	1
X	1	1	X	1
1	X	X	1	1
1	X	1	X	1
1	1	X	X	1

Family	Modules	
	Seq	Comb
All listed		1

## DF1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop

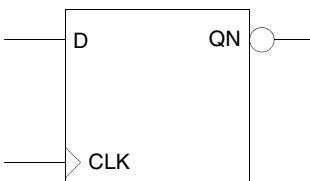
### Truth Table

CLK	Q <sub>n+1</sub>
↑	D

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

## DF1A

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active low Output

### Truth Table

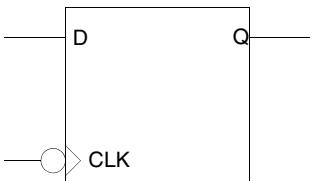
CLK	$QN_{n+1}$
↑	!D

Input D, CLK	Output QN
-----------------	--------------

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DF1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active low Clock

### Truth Table

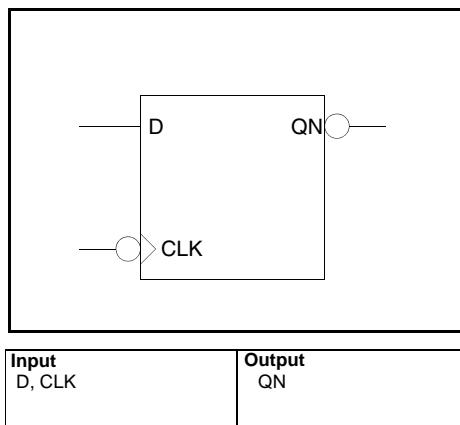
CLK	$Q_{n+1}$
↓	D

Input D, CLK	Output Q
-----------------	-------------

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DF1C

ACT 1, MX, ACT2/1200XL, ACT3, 3200DX, MX



### Function

D-Type Flip-Flop with active low Clock and Output

### Truth Table

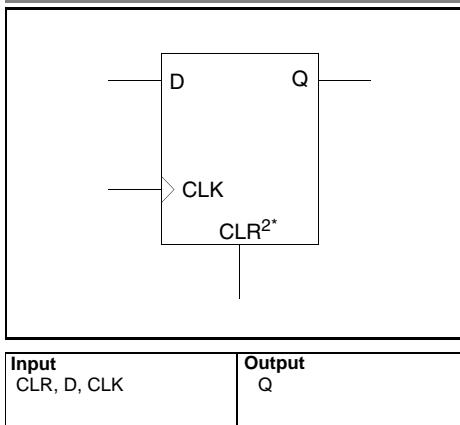
CLK	QN <sub>n+1</sub>
↓	!D

Input	Output
D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFC1

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active high Clear

### Truth Table

CLR	CLK	Q <sub>n+1</sub>
1	X	0
0	↑	D

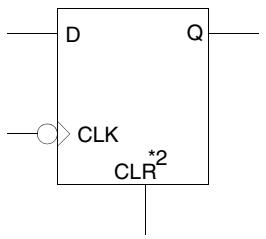
Input	Output
CLR, D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	1

\* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and MX.

## DFC1A

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active high Clear and active low Clock

### Truth Table

CLR	CLK	$Q_{n+1}$
1	X	0
0	↓	D

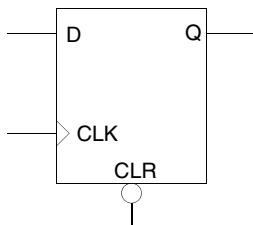
Input CLR, D, CLK	Output Q
----------------------	-------------

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	1

\* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and MX.

## DFC1B

ACT 1, ACT 2, ACT 3, 3200DX, MX SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active low Clear

### Truth Table

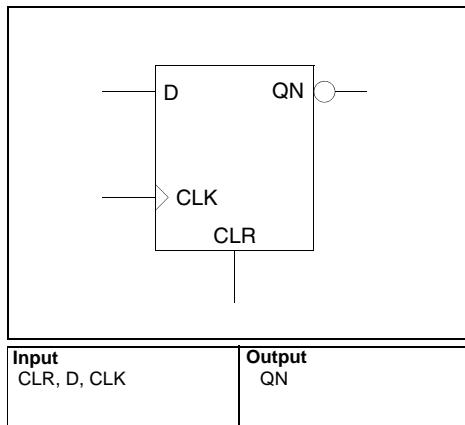
CLR	CLK	$Q_{n+1}$
0	X	0
1	↑	D

Input CLR, D, CLK	Output Q
----------------------	-------------

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

## DFC1C

ACT 1, MX



### Function

D-Type Flip-Flop with active high Clear and Clock

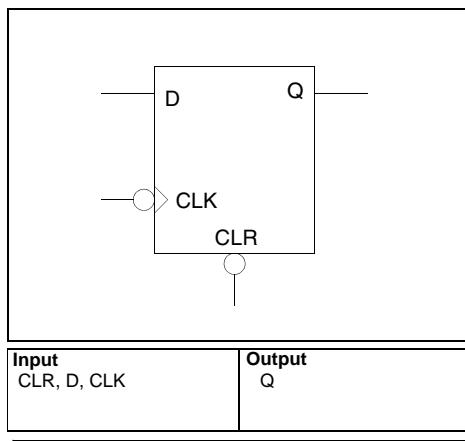
### Truth Table

CLR	CLK	$QN_{n+1}$
1	X	1
0	↑	$\neg D$

Family	Modules	
	Seq	Comb
ACT 1; MX		2

## DFC1D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Accelerator



### Function

D-Type Flip-Flop with active low Clear and Clock

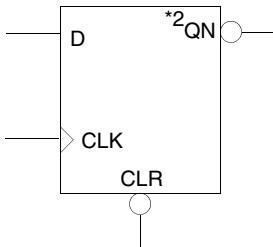
### Truth Table

CLR	CLK	$Q_{n+1}$
0	X	0
1	↓	D

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

## DFC1E

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active low Clear and Output

### Truth Table

CLR	CLK	QN <sub>n+1</sub>
0	X	1
1	↑	!D

Input  
CLR, D, CLK

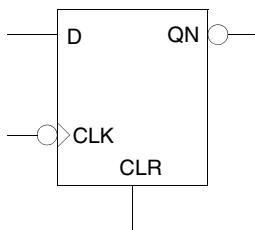
Output  
QN

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	1

\* A 2 on the symbol implies 2 logic module delays except for ACT1 and MX.

## DFC1F

ACT 1, MX



### Function

D-Type Flip-Flop with active high Clear, active low Clock and Output

### Truth Table

CLR	CLK	QN <sub>n+1</sub>
1	X	1
0	↓	!D

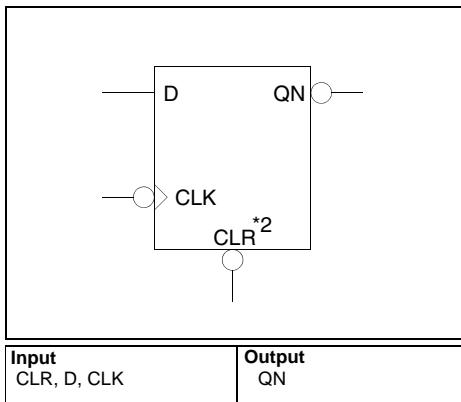
Input  
CLR, D, CLK

Output  
QN

Family	Modules	
	Seq	Comb
ACT 1, MX		2

## DFC1G

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active low Clear, Clock and Output

### Truth Table

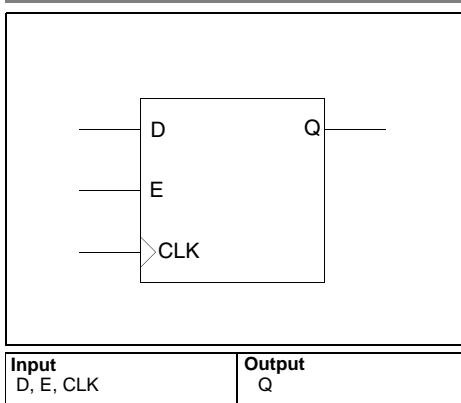
CLR	CLK	$Q_{n+1}$
0	X	1
1	↓	!D

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	1

\* A 2 on the symbol implies 2 logic module delays except for ACT1 and MX.

## DFE

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active high Enable

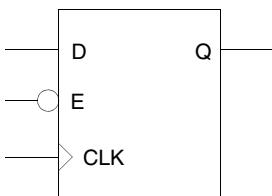
### Truth Table

E	CLK	$Q_{n+1}$
0	X	Q
1	↑	D

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

## DFE1B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active low Enable

### Truth Table

E	CLK	$Q_{n+1}$
1	X	Q
0	↑	D

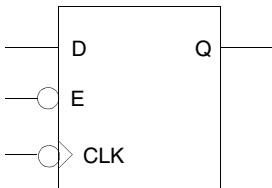
Input  
D, E, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

## DFE1C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active low Enable and Clock

### Truth Table

E	CLK	$Q_{n+1}$
1	X	Q
0	↓	D

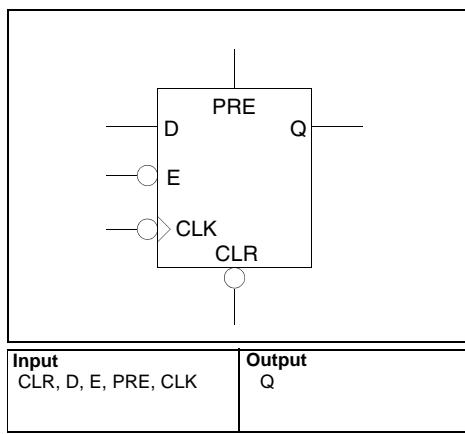
Input  
D, E, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

## DFE2D

ACT 1, MX



### Function

D-Type Flip-Flop with active high Preset, active low Enable, Clear, and Clock

### Truth Table

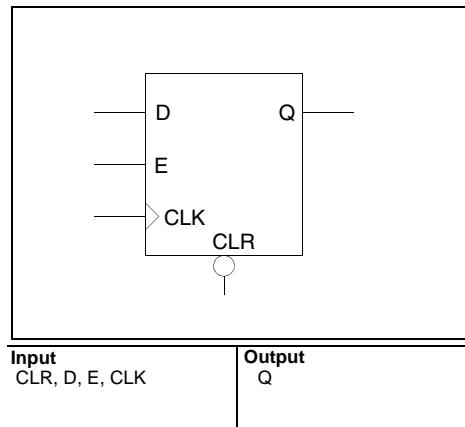
CLR	PRE	E	CLK	$Q_{n+1}$
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↓	D
0	1	X	X	*

Family	Modules	
	Seq	Comb
ACT 1, MX		2

\* Your design should not allow both PRE and CLR to be asserted at the same time.

## DFE3A

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop, with Enable and active low Clear

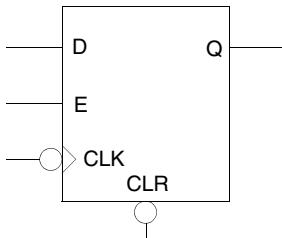
### Truth Table

CLR	E	CLK	$Q_{n+1}$
0	X	X	0
1	0	X	Q
1	1	↑	D

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

## DFE3B

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with Enable and active low Clear and Clock

### Truth Table

CLR	E	CLK	$Q_{n+1}$
0	X	X	0
1	0	X	Q
1	1	↓	D

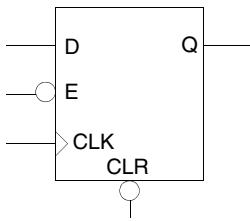
Input  
CLR, D, E, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFE3C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with Active Low Enable and Clear

### Truth Table

CLR	E	CLK	$Q_{n+1}$
0	X	X	0
1	1	X	Q
1	0	↑	D

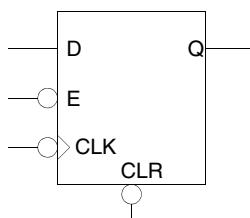
Input  
CLR, D, E, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

## DFE3D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active low Enable, Clear and Clock

### Truth Table

CLR	E	CLK	$Q_{n+1}$
0	X	X	0
1	1	X	Q
1	0	↓	D

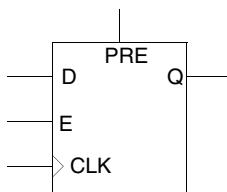
Input  
CLR, D, E, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFE4

ACT 1, MX



### Function

D-Type Flip-Flop with active high Enable and Preset

### Truth Table

PRE	E	CLK	$Q_{n+1}$
1	X	X	1
0	0	X	Q
0	1	↑	D

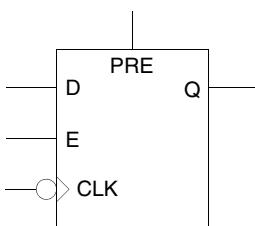
Input  
D, E, PRE, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

## DFE4A

ACT 1, MX



### Function

D-Type Flip-Flop with active high Enable and Preset, and active low Clock

### Truth Table

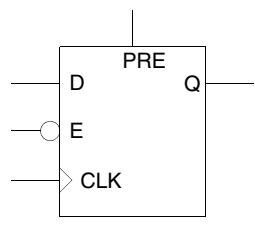
PRE	E	CLK	$Q_{n+1}$
1	X	X	1
0	0	X	Q
0	1	↓	D

Input	Output
D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

## DFE4B

ACT 1, MX



### Function

D-Type Flip-Flop with active low Enable, and active high Preset

### Truth Table

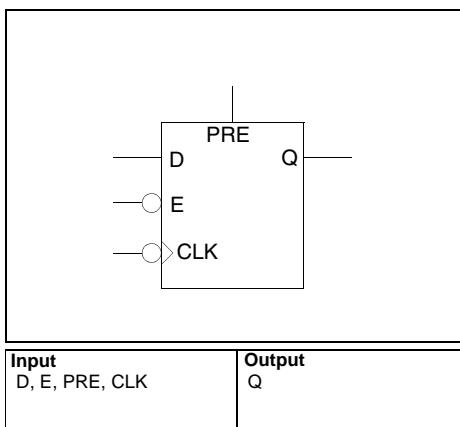
PRE	E	CLK	$Q_{n+1}$
1	X	X	1
0	1	X	Q
0	0	↑	D

Input	Output
D, E, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

## DFE4C

ACT 1, MX



### Function

D-Type Flip-Flop with active low Enable and Clock, and active high Preset

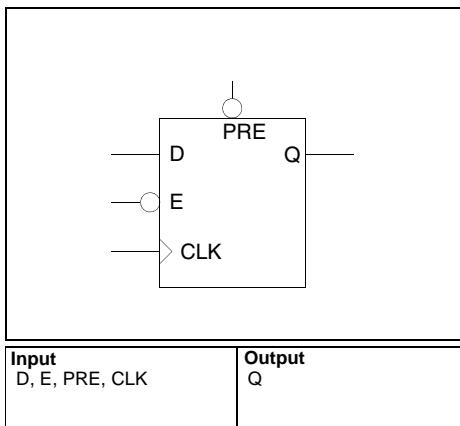
### Truth Table

PRE	E	CLK	$Q_{n+1}$
1	X	X	1
0	1	X	Q
0	0	↓	D

Family	Modules	
	Seq	Comb
ACT 1/MX		2

## DFE4F

SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active low Enable and Preset

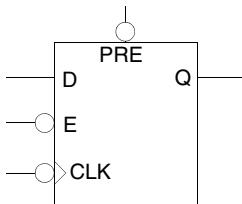
### Truth Table

PRE	E	CLK	$Q_{n+1}$
0	X	X	1
1	1	X	Q
1	0	↑	D

Family	Modules	
	Seq	Comb
All listed	1	

## DFE4G

SX, SX-A, SX-S, eX, Axcelerator



Input  
D, E, PRE, CLK

Output  
Q

### Function

D-Type Flip-Flop with active low Enable, Clock, and Preset

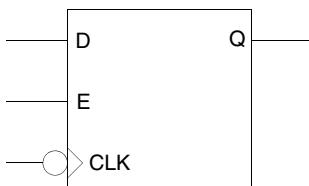
### Truth Table

PRE	E	CLK	$Q_{n+1}$
0	X	X	1
1	1	X	Q
1	0	↓	D

Family	Modules	
	Seq	Comb
All listed	1	

## DFEA

ACT 1, ACT 2, ACT 3, 3200DX, MX



Input  
D, E, CLK

Output  
Q

### Function

D-Type Flip-Flop, with Enable, and active low Clock

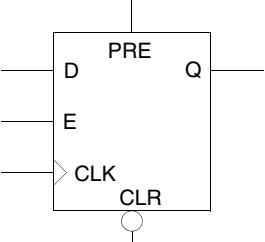
### Truth Table

E	CLK	$Q_{n+1}$
0	X	Q
1	↓	D

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	

## DFEB

ACT 1, MX

	<b>Input</b> CLR, D, E, PRE, CLK	<b>Output</b> Q
-----------------------------------------------------------------------------------	-------------------------------------	--------------------

### Function

D-Type Flip-Flop with Enable, Preset, and active low Clear

### Truth Table

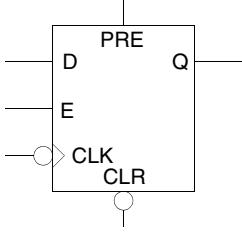
CLR	PRE	E	CLK	$Q_{n+1}$
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↑	D
0	1	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/MX		2

\*Your design should not allow both PRE and CLR to be asserted at the same time.

## DFEC

ACT 1, MX

	<b>Input</b> CLR, D, E, PRE, CLK	<b>Output</b> Q
-------------------------------------------------------------------------------------	-------------------------------------	--------------------

### Function

D-Type Flip-Flop with Enable, Preset, and active low Clear and Clock

### Truth Table

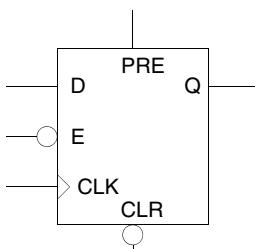
CLR	PRE	E	CLK	$Q_{n+1}$
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↓	D
0	1	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/MX		2

\* Your design should not allow both PRE and CLR to be asserted at the same time.

## DFED

ACT 1, MX



### Function

D-Type Flip-Flop with active low Enable and Clear, and active high Preset

### Truth Table

CLR	PRE	E	CLK	$Q_{n+1}$
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	$\uparrow$	D
0	1	X	X	*

Input  
CLR, D, E, PRE, CLK

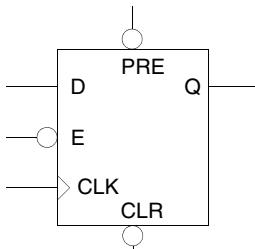
Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

\* Your design should not allow both PRE and CLR to be asserted at the same time.

## DFEG

SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active low Enable, Preset, and Clear

### Truth Table

CLR	PRE	E	CLK	$Q_{n+1}$
0	X	X	X	0
1	0	X	X	1
1	1	1	X	Q
1	1	0	$\uparrow$	D

Input  
CLR, D, E, PRE, CLK

Output  
Q

Family	Modules	
	Seq	Comb
All listed	1	

## DFEH

SX, SX-A, SX-S, eX, Axcelerator

CLR	PRE	E	CLK	$Q_{n+1}$
0	X	X	X	0
1	0	X	X	1
1	1	1	X	Q
1	1	0	↓	D

**Input**  
CLR, D, E, PRE, CLK

**Output**  
Q



Family	Modules	
	Seq	Comb
All listed	1	

## IODFE

ACT 3

E	CLK	$Q_{n+1}$
1	X	Q
0	↑	D

**Input**  
D, E, CLK

**Output**  
Q



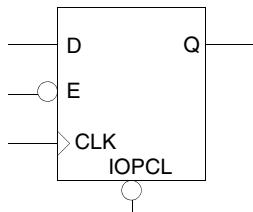
NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.

WARNING: Using the IODFE macro will disable the IOPCLBUF clock network.

NOTE 2: Uses an I/O module.

## IODFEC

ACT 3



### Function

D-Type Flip-Flop with active low Enable and Clear

### Truth Table

IOPCL	E	CLK	$Q_{n+1}$
0	X	X	0
1	1	X	Q
1	0	↑	D

**Input**  
IOPCL, D, E, CLK

**Output**  
Q

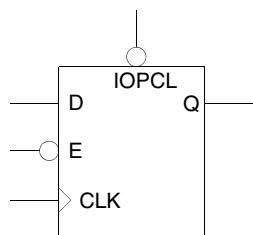
NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.

NOTE 2: Uses an I/O module.

NOTE 3: The IOPCL pin must be driven by the IOPCLBUF macro.

## IODFEP

ACT 3



### Function

D-Type Flip-Flop with active low Enable and Preset

### Truth Table

IOPCL	E	CLK	$Q_{n+1}$
0	X	X	1
1	1	X	Q
1	0	↑	D

**Input**  
IOPCL, D, E, CLK

**Output**  
Q

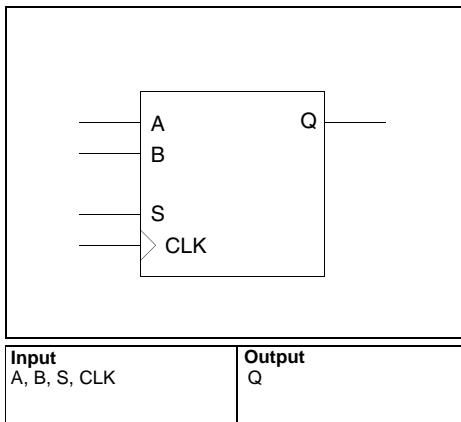
NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.

NOTE 2: The IOPCL pin must be driven by the IOPCLBUF macro.

NOTE 3: Uses an I/O module.

## DFM

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX, Axcelerator



Function		
D-Type Flip-Flop with 2-input Multiplexed Data		

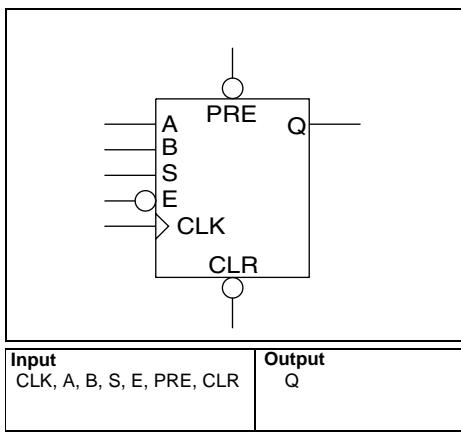
### Truth Table

S	CLK	$Q_{n+1}$
0	↑	A
1	↑	B

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFMEG

Axcelerator



Function					
D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Enable, Preset, and Clear					

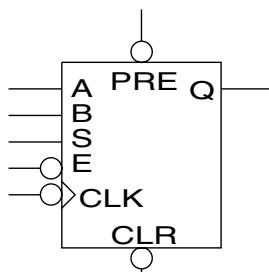
### Truth Table

CLR	PRE	E	S	CLK	$Q_{n+1}$
0	X	X	X	X	0
1	0	X	X	X	1
1	1	1	X	X	Q
1	1	0	0	↑	A
1	1	0	1	↑	B

Family	Modules	
	Seq	Comb
All listed	1	

## DFMEH

Axcelerator



**Input**  
CLK, A, B, S, E, PRE, CLR

**Output**  
Q

### Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable, Preset, and Clear

### Truth Table

CLR	PRE	E	S	CLK	$Q_{n+1}$
0	X	X	X	X	0
1	0	X	X	X	1
1	1	1	X	X	Q
1	1	0	0	↓	A
1	1	0	1	↓	B

### Family

### Modules

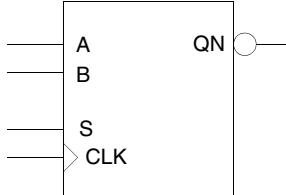
Seq Comb

All listed

1

## DFM1B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



**Input**  
A, B, S, CLK

**Output**  
QN

### Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

### Truth Table

S	CLK	$QN_{n+1}$
0	↑	!A
1	↑	!B

### Family

### Modules

Seq Comb

ACT 1/MX

2

Others

1

## DFM1C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX

	<p><b>Function</b> D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock and Output</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>S</th><th>CLK</th><th>QN<sub>n+1</sub></th></tr></thead><tbody><tr><td>0</td><td>↓</td><td>!A</td></tr><tr><td>1</td><td>↓</td><td>!B</td></tr></tbody></table> <p><b>Input</b> A, B, S, CLK</p> <p><b>Output</b> QN</p>	S	CLK	QN <sub>n+1</sub>	0	↓	!A	1	↓	!B
S	CLK	QN <sub>n+1</sub>								
0	↓	!A								
1	↓	!B								

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFM3

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX

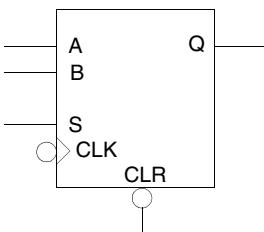
	<p><b>Function</b> D-Type Flip-Flop with 2-input Multiplexed Data, and active high Clear</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>CLR</th><th>S</th><th>CLK</th><th>Q<sub>n+1</sub></th></tr></thead><tbody><tr><td>1</td><td>x</td><td>x</td><td>0</td></tr><tr><td>0</td><td>1</td><td>↑</td><td>B</td></tr><tr><td>0</td><td>0</td><td>↑</td><td>A</td></tr></tbody></table> <p><b>Input</b> A, B, CLR, S, CLK</p> <p><b>Output</b> Q</p>	CLR	S	CLK	Q <sub>n+1</sub>	1	x	x	0	0	1	↑	B	0	0	↑	A
CLR	S	CLK	Q <sub>n+1</sub>														
1	x	x	0														
0	1	↑	B														
0	0	↑	A														

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	1

\* A 2 on the symbol implies 2 logic module delays except for ACT 1 and MX.

## DFM3B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX, Axcelerator



Input  
A, B, CLR, S, CLK

Output  
Q

### Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear and Clock

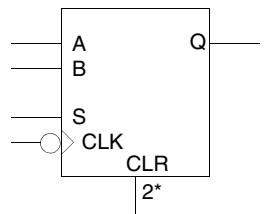
### Truth Table

CLR	S	CLK	$Q_{n+1}$
0	X	X	0
1	0	↓	A
1	1	↓	B

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFM3E

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



Input  
A, B, CLR, S, CLK

Output  
Q

### Function

D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock

### Truth Table

CLR	S	CLK	$Q_{n+1}$
1	X	X	0
0	0	↓	A
0	1	↓	B

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	1

\* A 2 on the symbol implies 2 logic module delays except for ACT 1 and MX.

## DFM3F

ACT 1, MX

CLR	S	CLK	QN <sub>n+1</sub>
1	X	X	1
0	0	↑	!A
0	1	↑	!B

**Input**  
A, B, CLR, S, CLK

**Output**  
QN



Family	Modules	
	Seq	Comb
ACT 1/MX		2

## DFM3G

ACT 1, MX

CLR	S	CLK	QN <sub>n+1</sub>
1	X	X	1
0	0	↓	!A
0	1	↓	!B

**Input**  
A, B, CLR, S, CLK

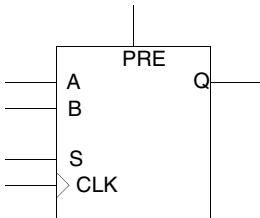
**Output**  
QN



Family	Modules	
	Seq	Comb
ACT 1/MX		2

## DFM4

ACT 1, MX



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active high Preset

### Truth Table

PRE	S	CLK	$Q_{n+1}$
1	X	X	1
0	0	↑	A
0	1	↑	B

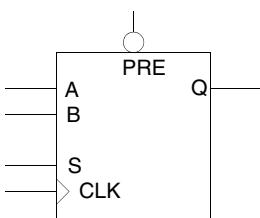
Input  
A, B, PRE, S, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

## DFM4A

ACT 1, MX, Axcelerator



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset

### Truth Table

PRE	S	CLK	$Q_{n+1}$
0	X	X	1
1	0	↑	A
1	1	↑	B

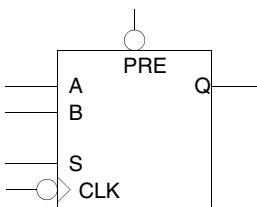
Input  
A, B, PRE, S, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

## DFM4B

ACT 1, MX, Axcelerator



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Clock

### Truth Table

PRE	S	CLK	$Q_{n+1}$
0	X	X	1
1	0	↓	A
1	1	↓	B

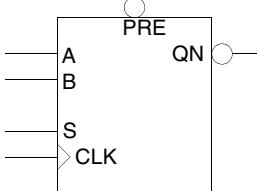
Input  
A, B, PRE, S, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

## DFM4C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Output

### Truth Table

PRE	S	CLK	$QN_{n+1}$
0	X	X	0
1	0	↑	!A
1	1	↑	!B

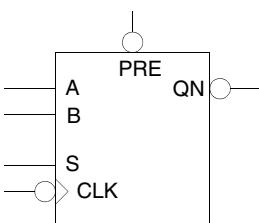
Input  
A, B, PRE, S, CLK

Output  
QN

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFM4D

ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX



Input	Output
A, B, PRE, S, CLK	QN

### Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset, Clock and Output

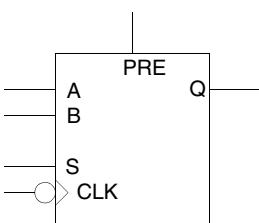
### Truth Table

PRE	S	CLK	QN <sub>n+1</sub>
0	X	X	0
1	0	↓	!A
1	1	↓	!B

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFM4E

ACT 1, MX



Input	Output
A, B, PRE, S, CLK	Q

### Function

D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clock

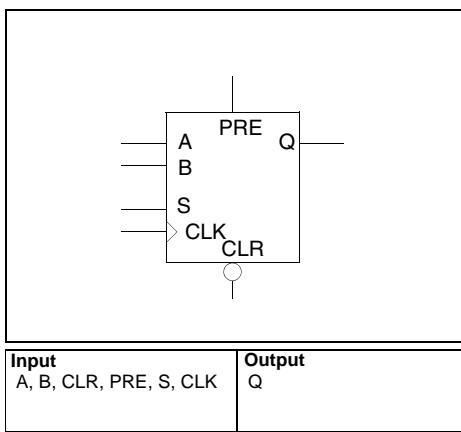
### Truth Table

PRE	S	CLK	Q <sub>n+1</sub>
1	X	X	1
0	0	↓	A
0	1	↓	B

Family	Modules	
	Seq	Comb
ACT 1/MX		2

## DFM5A

ACT 1, MX



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear

### Truth Table

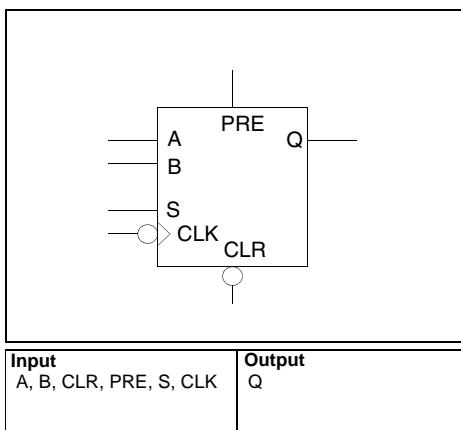
CLR	PRE	S	CLK	$Q_{n+1}$
0	0	X	X	0
1	1	X	X	1
1	0	0	↑	A
1	0	1	↑	B
0	1	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/MX		2

\* Your design should not allow both PRE and CLR to be asserted at the same time.

## DFM5B

ACT 1, MX



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear and Clock

### Truth Table

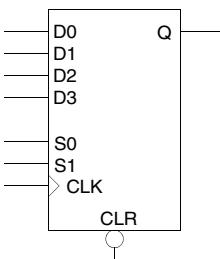
CLR	PRE	S	CLK	$Q_{n+1}$
0	0	X	X	0
1	1	X	X	1
1	0	0	↓	A
1	0	1	↓	B
0	1	X	X	*

Family	Modules	
	Seq	Comb
All listed		2

\* Your design should not allow both PRE and CLR to be asserted at the same time.

## DFM6A

ACT 2, ACT 3, 3200DX, MX



Input	Output
D0, D1, D2, D3, S0, S1, CLK, CLR	Q

### Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

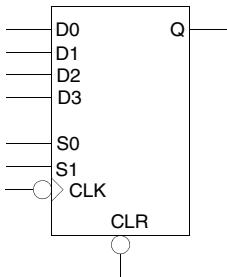
### Truth Table

CLR	S1	S0	CLK	Q <sub>n+1</sub>
0	X	X	X	0
1	0	0	↑	D0
1	0	1	↑	D1
1	1	0	↑	D2
1	1	1	↑	D3

Family	Modules	
	Seq	Comb
All listed	1	

## DFM6B

ACT 2, ACT 3, 3200DX, MX



Input	Output
D0, D1, D2, D3, S0, S1, CLK, CLR	Q

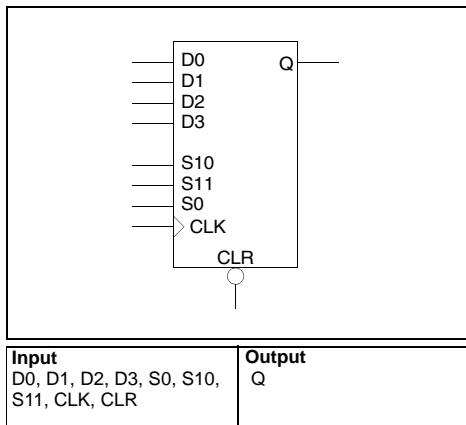
### Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and Clock

### Truth Table

CLR	S1	S0	CLK	Q <sub>n+1</sub>
0	X	X	X	0
1	0	0	↓	D0
1	0	1	↓	D1
1	1	0	↓	D2
1	1	1	↓	D3

Family	Modules	
	Seq	Comb
All listed	1	

**Function**

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

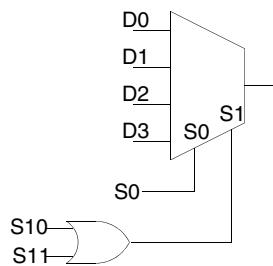
**Truth Table**

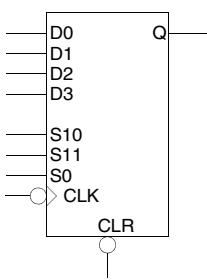
CLR	S11	S10	S0	CLK	Q <sub>n+1</sub>
0	X	X	X	X	0
1	0	0	0	↑	D0
1	0	0	1	↑	D1
1	1	X	0	↑	D2
1	X	1	0	↑	D2
1	1	X	1	↑	D3
1	X	1	1	↑	D3

Family	Modules	
	Seq	Comb
All listed	1	

NOTE 1: The DFM7A macro represents the full ACT 2, 3200DX and MX S-module.

NOTE 2: The following schematic describes the interconnections of the select lines.





Input	Output
D0, D1, D2, D3, S0, S10, S11, CLK, CLR	Q

**Function**

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

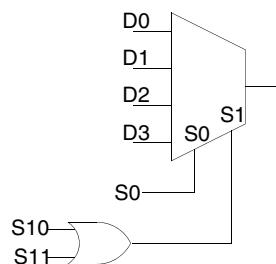
**Truth Table**

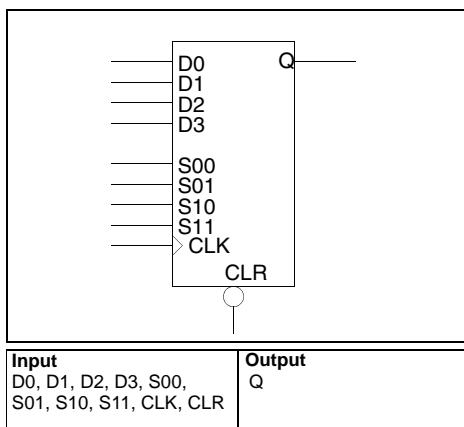
CLR	S11	S10	S0	CLK	Q <sub>n+1</sub>
0	X	X	X	X	0
1	0	0	0	↓	D0
1	0	0	1	↓	D1
1	1	X	0	↓	D2
1	X	1	0	↓	D2
1	1	X	1	↓	D3
1	X	1	1	↓	D3

Family	Modules	
	Seq	Comb
All listed	1	

NOTE 1: The DFM7B macro represents the full ACT 2, 3200DX and MX S-module.

NOTE 2: The following schematic describes the interconnections of the select lines.



**Function**

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

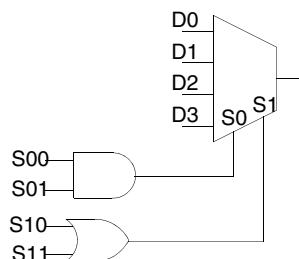
**Truth Table**

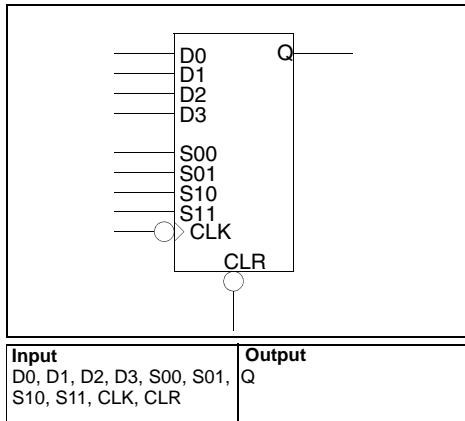
CLR	S11	S10	S01	S00	CLK	Q <sub>n+1</sub>
0	X	X	X	X	X	0
1	0	0	0	X	↑	D0
1	0	0	X	0	↑	D0
1	0	0	1	1	↑	D1
1	1	X	0	X	↑	D2
1	X	1	0	X	↑	D2
1	1	X	X	0	↑	D2
1	X	1	X	0	↑	D2
1	1	X	1	1	↑	D3
1	X	1	1	1	↑	D3

Family	Modules	
	Seq	Comb
ACT3	1	

NOTE 1: The DFM8A macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.





Function						
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock						

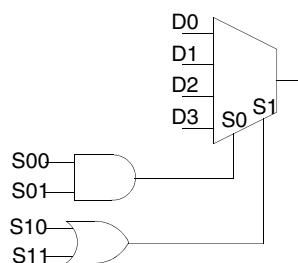
Truth Table

CLR	S11	S10	S01	S00	CLK	Q <sub>n+1</sub>
0	X	X	X	X	X	0
1	0	0	0	X	↓	D0
1	0	0	X	0	↓	D0
1	0	0	1	1	↓	D1
1	1	X	0	X	↓	D2
1	X	1	0	X	↓	D2
1	1	X	X	0	↓	D2
1	X	1	X	0	↓	D2
1	1	X	1	1	↓	D3
1	X	1	1	1	↓	D3

Family	Modules	
	Seq	Comb
ACT3	1	

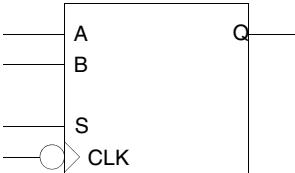
NOTE 1: The DFM8B macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



## DFMA

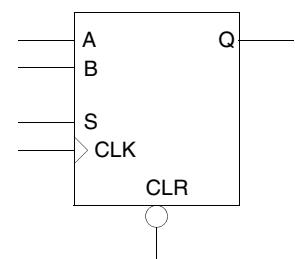
ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator

	<p><b>Function</b> D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>S</th><th>CLK</th><th><math>Q_{n+1}</math></th></tr></thead><tbody><tr><td>0</td><td>↓</td><td>A</td></tr><tr><td>1</td><td>↓</td><td>B</td></tr></tbody></table> <p><b>Input</b> A, B, S, CLK</p> <p><b>Output</b> Q</p>	S	CLK	$Q_{n+1}$	0	↓	A	1	↓	B
S	CLK	$Q_{n+1}$								
0	↓	A								
1	↓	B								

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFMB

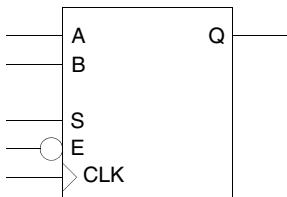
ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator

	<p><b>Function</b> D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>CLR</th><th>S</th><th>CLK</th><th><math>Q_{n+1}</math></th></tr></thead><tbody><tr><td>0</td><td>X</td><td>X</td><td>0</td></tr><tr><td>1</td><td>0</td><td>↑</td><td>A</td></tr><tr><td>1</td><td>1</td><td>↑</td><td>B</td></tr></tbody></table> <p><b>Input</b> A, B, CLR, S, CLK</p> <p><b>Output</b> Q</p>	CLR	S	CLK	$Q_{n+1}$	0	X	X	0	1	0	↑	A	1	1	↑	B
CLR	S	CLK	$Q_{n+1}$														
0	X	X	0														
1	0	↑	A														
1	1	↑	B														

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFME1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

2-bit D-Type Flip-Flop with Multiplexed Data, and active low Enable

### Truth Table

E	S	CLK	$Q_{n+1}$
1	X	X	Q
0	0	↑	A
0	1	↑	B

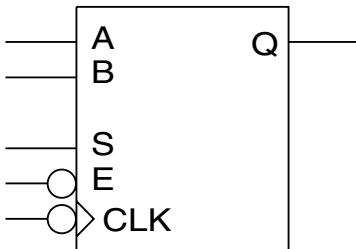
Input  
A, B, S, E, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFME1B

Axcelerator



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable

### Truth Table

E	S	CLK	$Q_{n+1}$
1	X	X	Q
0	0	↓	A
0	1	↓	B

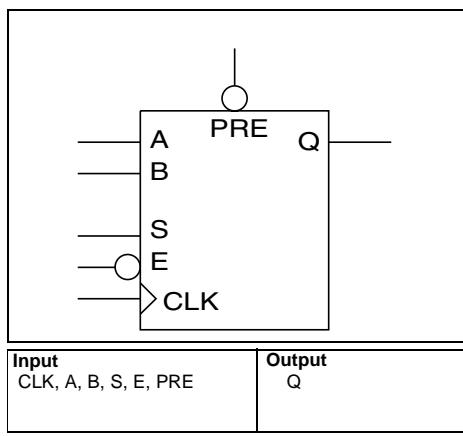
Input  
CLK, A, B, S, E,

Output  
Q

Family	Modules	
	Seq	Comb
All listed	1	

## DFME2A

Axcelerator



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Enable and Preset

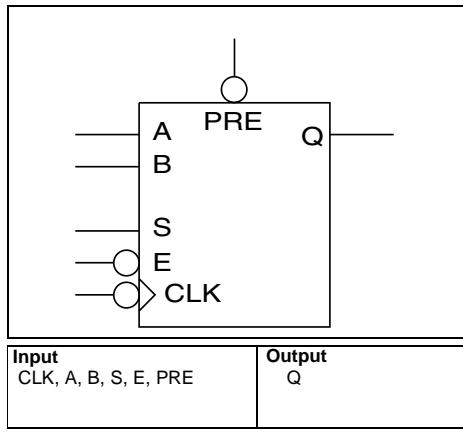
### Truth Table

PRE	E	S	CLK	$Q_{n+1}$
0	X	X	X	1
1	1	X	X	Q
1	0	0	↑	A
1	0	1	↑	B

Family	Modules	
	Seq	Comb
All listed	1	

## DFME2B

Axcelerator



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable and Preset

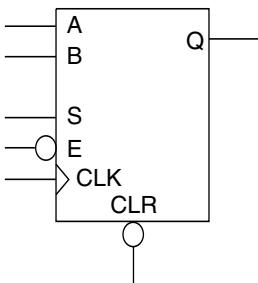
### Truth Table

PRE	E	S	CLK	$Q_{n+1}$
0	X	X	X	1
1	1	X	X	Q
1	0	0	↓	A
1	0	1	↓	B

Family	Modules	
	Seq	Comb
All listed	1	

## DFME3A

Axcelerator



**Input**  
CLK, A, B, S, E, CLR

**Output**  
Q

### Function

D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Enable and Clear

### Truth Table

CLR	E	S	CLK	$Q_{n+1}$
0	X	X	X	0
1	1	X	X	Q
1	0	0	↑	A
1	0	1	↑	B

Family

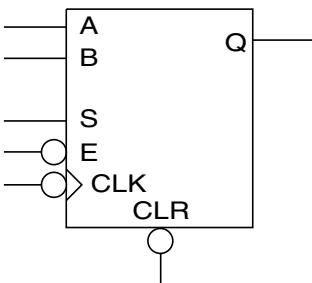
Modules

Seq	Comb
1	

All listed

## DFME3B

Axcelerator



**Input**  
CLK, A, B, S, E, CLR

**Output**  
Q

### Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Enable and Clear

### Truth Table

CLR	E	S	CLK	$Q_{n+1}$
0	X	X	X	0
1	1	X	X	Q
1	0	0	↓	A
1	0	1	↓	B

Family

Modules

Seq	Comb
1	

All listed

Family	Modules
Seq	Comb
All listed	1

## DFMPCA

Axcelerator

	<b>Input</b> CLK, A, B, S, E, PRE, CLR  <b>Output</b> Q
--	---------------------------------------------------------------------

### Function

D-Type Flip-Flop with 2-input Multiplexed Data, rising-edge triggered Clock, and active-low Preset and Clear

### Truth Table

CLR	PRE	S	CLK	$Q_{n+1}$
0	X	X	X	0
1	0	X	X	1
1	1	0	↑	A
1	1	1	↑	B

Family	Modules	
	Seq	Comb
All listed	1	

## DFMPCB

Axcelerator

	<b>Input</b> CLK, A, B, S, E, PRE, CLR  <b>Output</b> Q
--	---------------------------------------------------------------------

### Function

D-Type Flip-Flop with 2-input Multiplexed Data, falling-edge triggered Clock, and active-low Preset and Clear

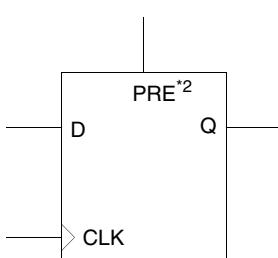
### Truth Table

CLR	PRE	S	CLK	$Q_{n+1}$
0	X	X	X	0
1	0	X	X	1
1	1	0	↓	A
1	1	1	↓	B

Family	Modules	
	Seq	Comb
All listed	1	

## DFP1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active high Preset

### Truth Table

PRE	CLK	$Q_{n+1}$
1	X	1
0	↑	D

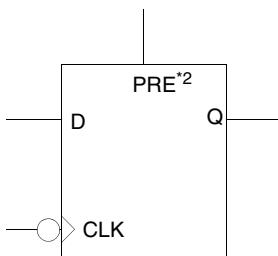
Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX, Axcelerator	1	1
Others		2

\* A 2 on the symbol implies 2 logic module delays only for SX, SX-A, SX-S, eX, and Axcelerator.

## DFP1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active high Preset, and active low Clock

### Truth Table

PRE	CLK	$Q_{n+1}$
1	X	1
0	↓	D

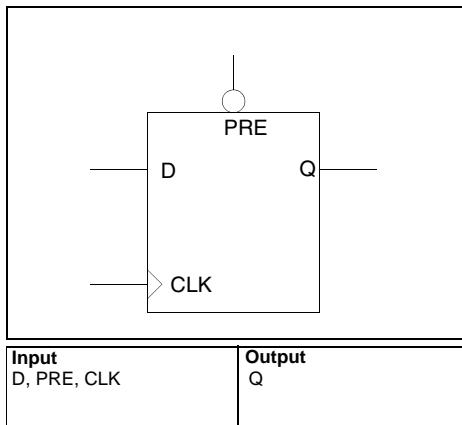
Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
SX, SX-A, eX, Axcelerator	1	1
Others		2

\* A 2 on the symbol implies 2 logic module delays only for SX, SX-A, SX-S, eX, and Axcelerator.

## DFP1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active low Preset

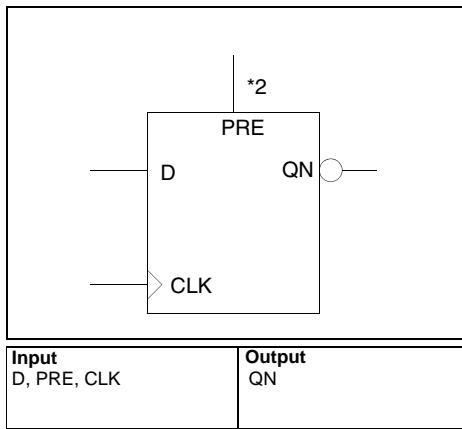
### Truth Table

PRE	CLK	$Q_{n+1}$
0	X	1
1	↑	D

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX, Axcelerator	1	
Others		2

## DFP1C

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active high Preset, and active low Output

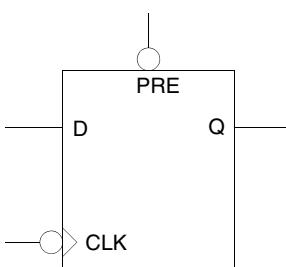
### Truth Table

PRE	CLK	$QN_{n+1}$
1	X	0
0	↑	!D

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	1

## DFP1D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active low Preset and Clock

### Truth Table

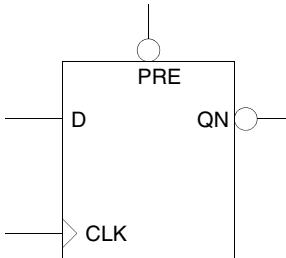
PRE	CLK	$Q_{n+1}$
0	X	1
1	↓	D

Input D, PRE, CLK	Output Q
----------------------	-------------

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX, and Axcelerator	1	
Others		2

## DFP1E

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active low Preset and Output

### Truth Table

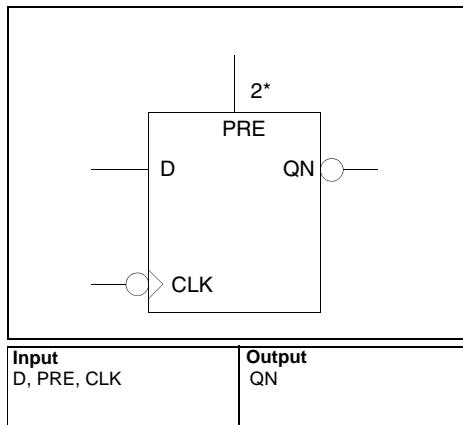
PRE	CLK	$QN_{n+1}$
0	X	0
1	↑	!D

Input D, PRE, CLK	Output QN
----------------------	--------------

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFP1F

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active high Preset, and active low Clock and Output

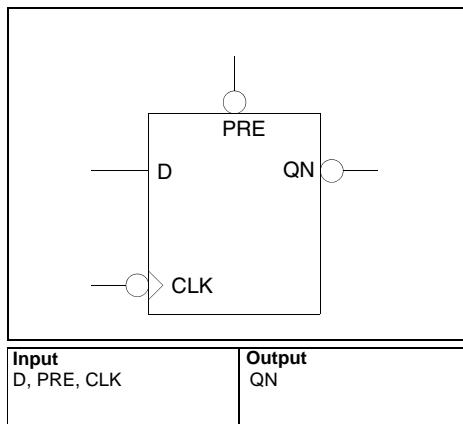
### Truth Table

PRE	CLK	QN <sub>n+1</sub>
1	X	0
0	↓	!D

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	1

## DFP1G

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active low Preset, Clock and Output

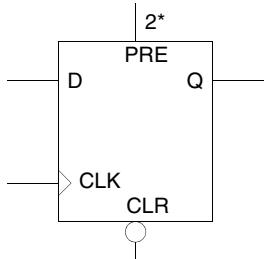
### Truth Table

PRE	CLK	QN <sub>n+1</sub>
0	X	0
1	↓	!D

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others	1	

## DFPC

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



**Input**

CLR, D, PRE, CLK

**Output**

Q

### Function

D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

### Truth Table

CLR	PRE	CLK	$Q_{n+1}$
0	0	X	0
1	1	X	1
1	0	↑	D
0	1	X	**

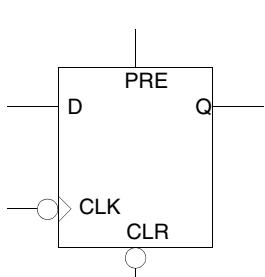
Family	Modules	
	Seq	Comb
Others	1	1
ACT 1, ACT2/1200XL, ACT 3, 3200DX, MX, SX, SX-A, SX-S		2

\* A 2 on the symbol implies 2 logic module delays only for SX, SX-A, SX-S, and eX.

\*\* In ACT 1/MX, your design should not allow both PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

## DFPCA

ACT 1, ACT 2, ACT 3, 3200DX, MX



**Input**

CLR, D, PRE, CLK

**Output**

Q

### Function

D-Type Flip-Flop with active high Preset, active low Clear and Clock

### Truth Table

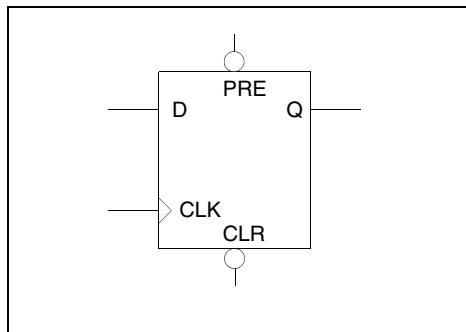
CLR	PRE	CLK	$Q_{n+1}$
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	*

Family	Modules	
	Seq	Comb
All		2

\* Your design should not allow both PRE and CLR to be asserted at the same time.

## DFPCB

SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop, with active low Clear, and Preset

### Truth Table

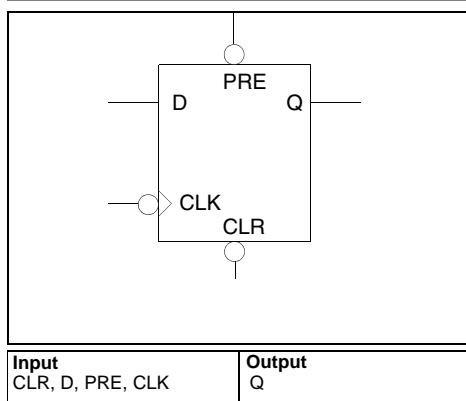
CLR	PRE	CLK	$Q_{n+1}$
0	X	X	0
1	0	X	1
1	1	↑	D

Input	Output
CLR, D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX, Axcelerator	1	

## DFPCC

SX, SX-A, SX-S, eX, Axcelerator



### Function

D-Type Flip-Flop with active low Preset, Clear and Clock

### Truth Table

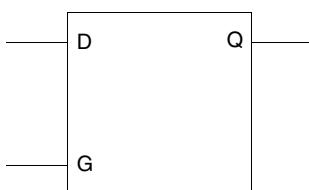
CLR	PRE	CLK	$Q_{n+1}$
0	X	X	0
1	0	X	1
1	1	↓	D

Input	Output
CLR, D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
All listed	1	

## DL1

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Data Latch

### Truth Table

G	$Q_{n+1}$
0	Q
1	D

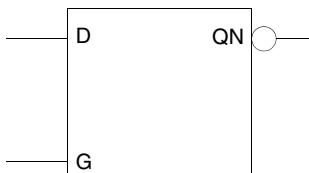
Input  
D, G

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1, MX, SX, SX-A, SX-S, eX		1
Others	1	

## DL1A

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



### Function

Data Latch with active low Output

### Truth Table

G	$QN_{n+1}$
0	QN
1	!D

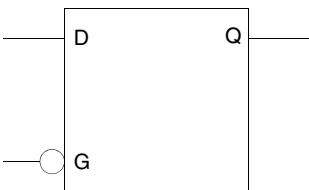
Input  
D, G

Output  
QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DL1B

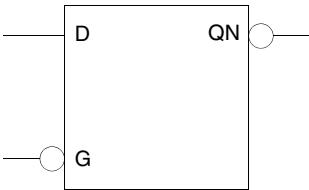
ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator

	<p><b>Function</b> Data Latch with active low Clock</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>G</th><th><math>Q_{n+1}</math></th></tr></thead><tbody><tr><td>1</td><td>Q</td></tr><tr><td>0</td><td>D</td></tr></tbody></table> <p><b>Input</b> D, G</p> <p><b>Output</b> Q</p>	G	$Q_{n+1}$	1	Q	0	D
G	$Q_{n+1}$						
1	Q						
0	D						

Family	Modules	
	Seq	Comb
ACT 1, MX, SX, SX-A, SX-S, eX		1
Others	1	

## DL1C

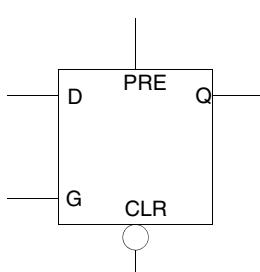
ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator

	<p><b>Function</b> Data Latch, with active low Clock and Output</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>G</th><th><math>QN_{n+1}</math></th></tr></thead><tbody><tr><td>1</td><td>QN</td></tr><tr><td>0</td><td>!D</td></tr></tbody></table> <p><b>Input</b> D, G</p> <p><b>Output</b> QN</p>	G	$QN_{n+1}$	1	QN	0	!D
G	$QN_{n+1}$						
1	QN						
0	!D						

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DL2A

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
CLR, D, G, PRE

Output  
Q

### Function

Data Latch with active low Clear and active high Preset

### Truth Table

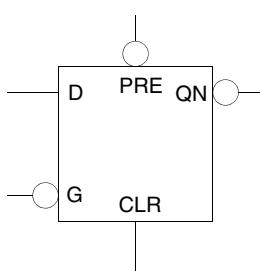
CLR	PRE	G	Q <sub>n+1</sub>
0	0	X	0
1	1	X	1
1	0	0	Q
1	0	1	D
0	1	X	*

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

\*In ACT 1 and MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

## DL2B

ACT 1, ACT 2, ACT3, 3200DX, MX



Input  
CLR, D, G, PRE

Output  
QN

### Function

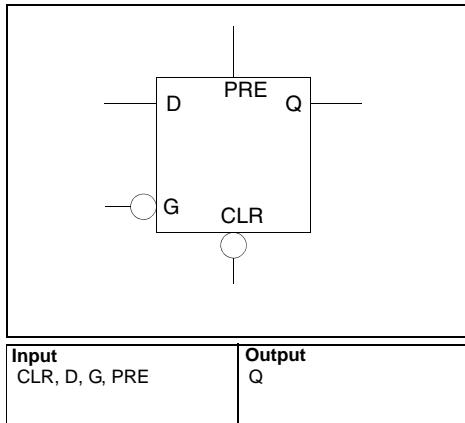
Data Latch with active high Clear and active low Preset, Clock, and Output

### Truth Table

CLR	PRE	G	QN <sub>n+1</sub>
1	1	X	1
0	0	X	0
0	1	1	QN
0	1	0	!D
1	0	X	*

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

\*In ACT 1 and MX, your design should not allow PRE and CLR to be asserted at the same time.  
In other families, CLR has priority over PRE.

**Function**

Data Latch with active low Clear, active high Preset, and active low Clock

**Truth Table**

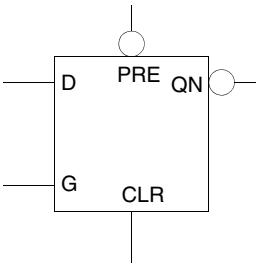
CLR	PRE	G	$Q_{n+1}$
0	0	X	0
1	1	X	1
1	0	1	Q
1	0	0	D
0	1	X	*

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

\*In ACT 1 and MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

## DL2D

ACT 1, ACT 2, ACT3, 3200DX, MX

	
<b>Input</b> CLR, D, G, PRE	<b>Output</b> QN

Function			
Data Latch with active high Clear and active low Preset and Output			

### Truth Table

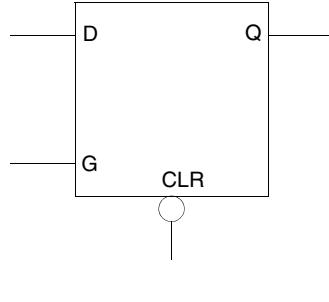
CLR	PRE	G	QN <sub>n+1</sub>
1	1	X	1
0	0	X	0
0	1	0	QN
0	1	1	!D
1	0	X	*

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

\*In ACT 1 and MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

## DLC

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator

	
<b>Input</b> CLR, D, G	<b>Output</b> Q

Function		
Data Latch with active low Clear		

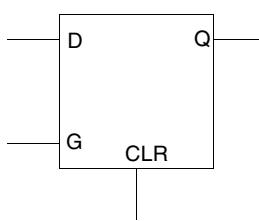
### Truth Table

CLR	G	Q <sub>n+1</sub>
0	X	0
1	0	Q
1	1	D

Family	Modules	
	Seq	Comb
ACT 1, MX, SX, SX-A, SX-S, eX		1
Others	1	

## DLC1

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Data Latch with active high Clear

### Truth Table

CLR	G	$Q_{n+1}$
1	X	0
0	0	Q
0	1	D

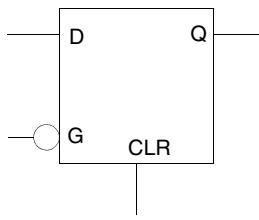
**Input**  
CLR, D, G

**Output**  
Q

Family	Modules	
	Seq	Comb
All		1

## DLC1A

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Data Latch with active high Clear and active low Clock

### Truth Table

CLR	G	$Q_{n+1}$
1	X	0
0	1	Q
0	0	D

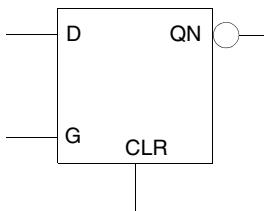
**Input**  
CLR, D, G

**Output**  
Q

Family	Modules	
	Seq	Comb
All		1

## DLC1F

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



### Function

Data Latch with active high Clear and active low Output

### Truth Table

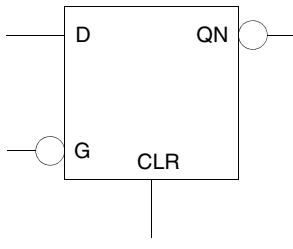
CLR	G	QN <sub>n+1</sub>
1	X	1
0	0	QN
0	1	!D

Input	Output
CLR, D, G	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

## DLC1G

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



### Function

Data Latch with active high Clear and active low Clock and Output

### Truth Table

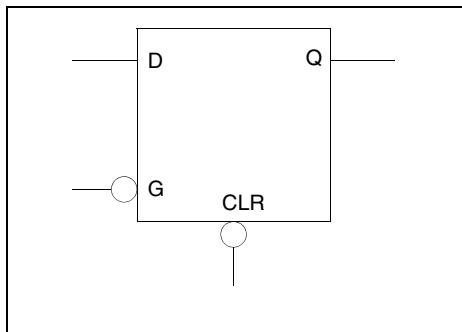
CLR	G	QN <sub>n+1</sub>
1	X	1
0	1	QN
0	0	!D

Input	Output
CLR, D, G	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

## DLCA

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Data Latch with active low Clear and Clock

### Truth Table

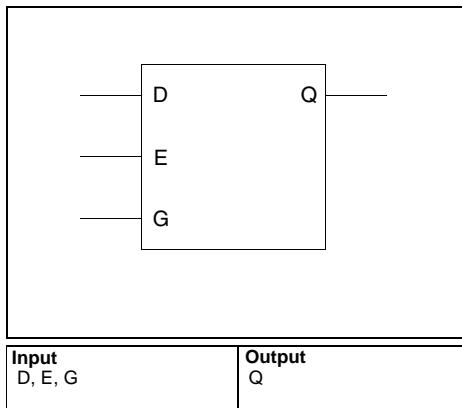
CLR	G	$Q_{n+1}$
0	X	0
1	1	Q
1	0	D

Input	Output
CLR, D, G	Q

Family	Modules	
	Seq	Comb
Others		1
ACT 2, 1200XL, ACT 3, 3200DX, MX	1	

## DLE

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



### Function

Data Latch with active high Enable

### Truth Table

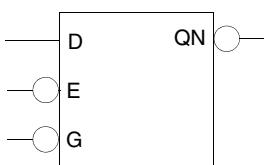
E	G	$Q_{n+1}$
0	X	Q
X	0	Q
1	1	D

Input	Output
D, E, G	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DLE1D

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



### Function

Data Latch with active low Enable and Clock and active low Output

### Truth Table

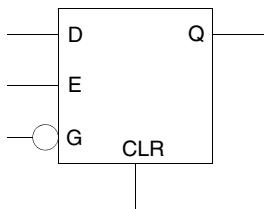
E	G	QN <sub>n+1</sub>
1	X	QN
X	1	QN
0	0	!D

Input D, E, G	Output QN
------------------	--------------

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DLE2A

ACT 1, MX



### Function

Data Latch with active high Enable and Clear, and active low Clock

### Truth Table

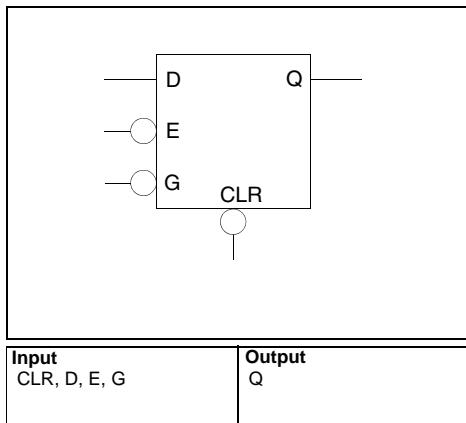
CLR	E	G	Q <sub>n+1</sub>
1	X	X	0
0	0	X	Q
0	X	1	Q
0	1	0	D

Input CLR, D, E, G	Output Q
-----------------------	-------------

Family	Modules	
	Seq	Comb
ACT 1/MX		1

## DLE2B

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator



### Function

Data Latch with active low Enable, Clear, and Clock

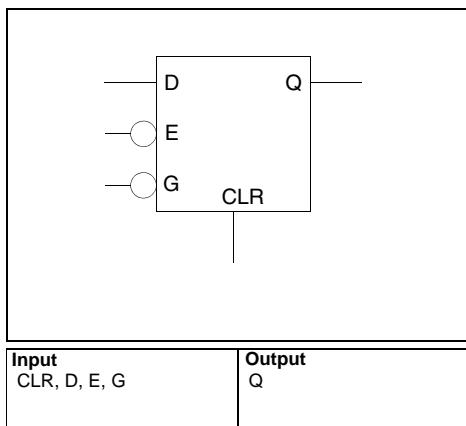
### Truth Table

CLR	E	G	$Q_{n+1}$
0	X	X	0
1	1	X	Q
1	X	1	Q
1	0	0	D

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DLE2C

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Data Latch with active low Enable and Clock, and active high Clear

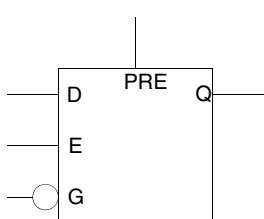
### Truth Table

CLR	E	G	$Q_{n+1}$
1	X	X	0
0	1	X	Q
0	X	1	Q
0	0	0	D

Family	Modules	
	Seq	Comb
All		1

## DLE3A

ACT 1, MX



Input  
D, E, G, PRE

Output  
Q

### Function

Data Latch with active high Enable and Preset, and active low Clock

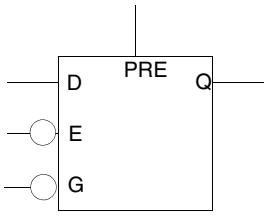
### Truth Table

PRE	E	G	$Q_{n+1}$
1	X	X	1
0	0	X	Q
0	1	0	D
0	X	1	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1

## DLE3B

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
D, E, G, PRE

Output  
Q

### Function

Data Latch with active low Enable and Clock, and active high Preset

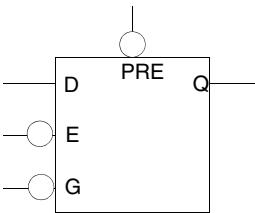
### Truth Table

PRE	E	G	$Q_{n+1}$
1	X	X	1
0	1	X	Q
0	X	1	Q
0	0	0	D

Family	Modules	
	Seq	Comb
All		1

## DLE3C

ACT 1, ACT 2, ACT3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator

	<b>Input</b> D, E, G, PRE	<b>Output</b> Q
-----------------------------------------------------------------------------------	------------------------------	--------------------

### Function

Data Latch with active low Enable, Preset, and Clock

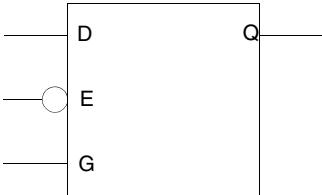
### Truth Table

PRE	E	G	$Q_{n+1}$
0	X	X	1
1	1	X	Q
1	X	1	Q
1	0	0	D

Family	Modules	
	Seq	Comb
All		1

## DLEA

ACT 1, ACT 2, ACT3, 3200DX, MX, Axcelerator

	<b>Input</b> D, E, G	<b>Output</b> Q
------------------------------------------------------------------------------------	-------------------------	--------------------

### Function

Data Latch with active low Enable and active high Clock

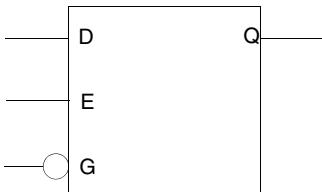
### Truth Table

E	G	$Q_{n+1}$
1	X	Q
X	0	Q
0	1	D

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DLEB

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

Data Latch with active high Enable, and active low Clock

### Truth Table

E	G	$Q_{n+1}$
0	X	Q
X	1	Q
1	0	D

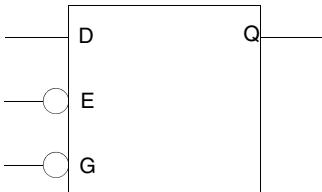
Input  
D, E, G

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DLEC

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

Data Latch with active low Enable and Clock

### Truth Table

E	G	$Q_{n+1}$
1	X	Q
X	1	Q
0	0	D

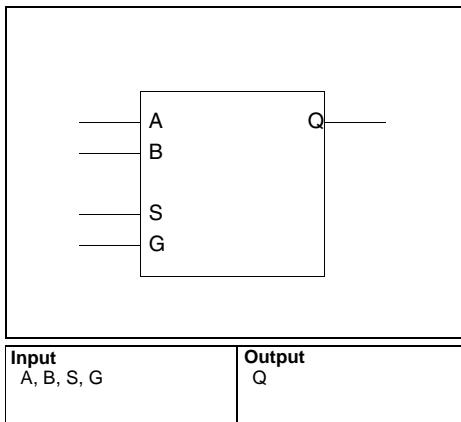
Input  
D, E, G

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DLM

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

Data Latch with 2-input Multiplexed Data

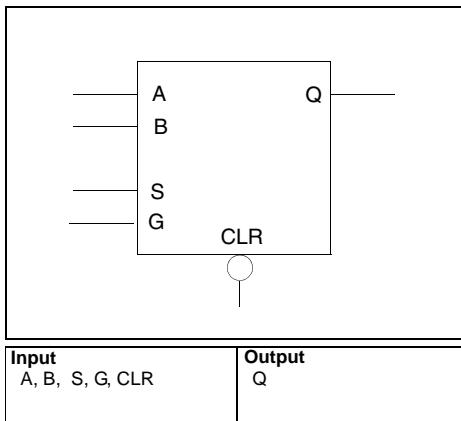
### Truth Table

S	G	$Q_{n+1}$
X	0	Q
0	1	A
1	1	B

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DLM2

ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

Data Latch with 2-input Multiplexed Data and Active-Low Clear

### Truth Table

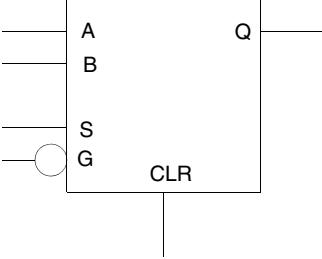
CLR	S	G	$Q_{n+1}$
0	X	X	0
1	X	0	Q
1	0	1	A
1	1	1	B

Family	Modules	
	Seq	Comb
All listed	1	



## DLM2A

ACT 1, MX

	<b>Input</b> A, B, CLR, S, G	<b>Output</b> Q
-----------------------------------------------------------------------------------	---------------------------------	--------------------

### Function

Data Latch with 2-input Multiplexed Data and Clear, and Active-Low Clock

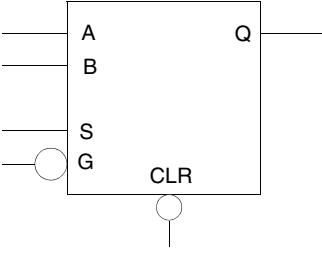
### Truth Table

CLR	S	G	$Q_{n+1}$
1	X	X	0
0	X	1	Q
0	0	0	A
0	1	0	B

Family	Modules	
	Seq	Comb
ACT 1/MX		1

## DLM2B

ACT 2, ACT 3, 3200DX, MX, Axcelerator

	<b>Input</b> A, B, CLR, S, G	<b>Output</b> Q
-------------------------------------------------------------------------------------	---------------------------------	--------------------

### Function

Data Latch with 2-input Multiplexed Data and Active-Low Clock and Clear

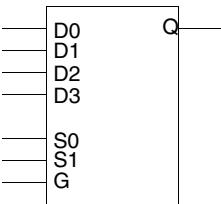
### Truth Table

CLR	S	G	$Q_{n+1}$
0	X	X	0
1	X	1	Q
1	0	0	A
1	1	0	B

Family	Modules	
	Seq	Comb
All listed	1	

## DLM3

ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

Data Latch with 4-input Multiplexed Data

### Truth Table

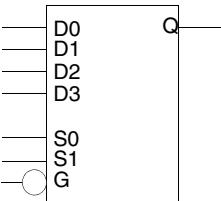
S1	S0	G	Q <sub>n+1</sub>
X	X	0	Q
0	0	1	D0
0	1	1	D1
1	0	1	D2
1	1	1	D3

Input	Output
D0, D1, D2, D3, S0, S1, G	Q

Family	Modules	
	Seq	Comb
All listed	1	

## DLM3A

ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

Data Latch with 4-input Multiplexed Data, and active low Clock

### Truth Table

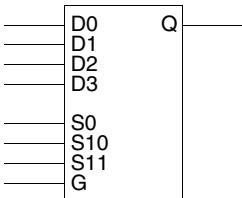
S1	S0	G	Q <sub>n+1</sub>
X	X	1	Q
0	0	0	D0
0	1	0	D1
1	0	0	D2
1	1	0	D3

Input	Output
D0, D1, D2, D3, S0, S1, G	Q

Family	Modules	
	Seq	Comb
All listed	1	

## DLM4

ACT 2, ACT 3, 3200DX, MX, Axcelerator

	<b>Input</b> D0, D1, D2, D3, S0, S10, S11, G	<b>Output</b> Q
-----------------------------------------------------------------------------------	----------------------------------------------------	--------------------

Function				
Data Latch with 4-input Multiplexed Data				

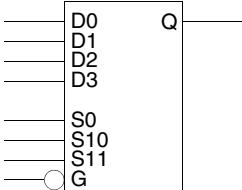
### Truth Table

S10	S11	S0	G	Q <sub>n+1</sub>
X	X	X	0	Q
0	0	0	1	D0
0	0	1	1	D1
X	1	0	1	D2
1	X	0	1	D2
X	1	1	1	D3
1	X	1	1	D3

Family	Modules	
	Seq	Comb
All listed	1	

## DLM4A

ACT 2, ACT 3, 3200DX, MX, Axcelerator

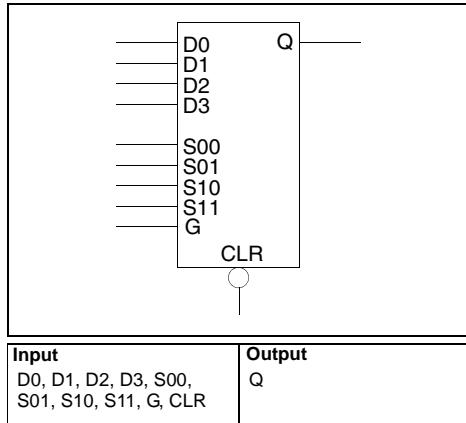
	<b>Input</b> D0, D1, D2, D3, S0, S10, S11, G	<b>Output</b> Q
-------------------------------------------------------------------------------------	----------------------------------------------------	--------------------

Function				
Data Latch with 4-input Multiplexed Data and active low Clock				

### Truth Table

S10	S11	S0	G	Q <sub>n+1</sub>
X	X	X	1	Q
0	0	0	0	D0
0	0	1	0	D1
X	1	0	0	D2
1	X	0	0	D2
X	1	1	0	D3
1	X	1	0	D3

Family	Modules	
	Seq	Comb
All listed	1	



**Function**  
D-Type Latch with 4-input Multiplexed Data and active low Clear

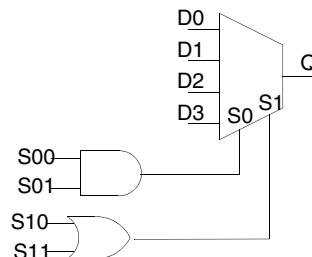
Truth Table

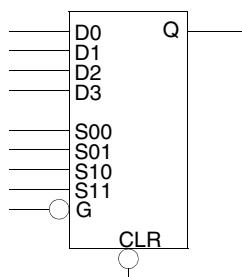
CLR	S11	S10	S01	S00	G	Q <sub>n+1</sub>
0	X	X	X	X	X	0
1	X	X	X	X	0	Q
1	0	0	0	X	1	D0
1	0	0	X	0	1	D0
1	0	0	1	1	1	D1
1	1	X	0	X	1	D2
1	X	1	0	X	1	D2
1	1	X	X	0	1	D2
1	X	1	X	0	1	D2
1	1	X	1	1	1	D3
1	X	1	1	1	1	D3

Family	Modules	
	Seq	Comb
ACT 3	1	

NOTE 1: The DLM8A macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.

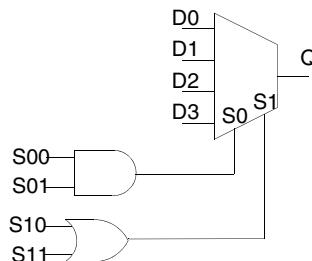


 <p><b>Input</b> D0, D1, D2, D3, S00, S01, S10, S11, G, CLR</p> <p><b>Output</b> Q</p>	<b>Function</b> D-Type Latch with 4-input Multiplexed Data and active low Clear and Clock																																																																																									
	<b>Truth Table</b>																																																																																									
<table border="1"> <thead> <tr> <th>CLR</th><th>S11</th><th>S10</th><th>S01</th><th>S00</th><th>G</th><th>Q<sub>n+1</sub></th></tr> </thead> <tbody> <tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td></tr> <tr><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>Q</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X</td><td>0</td><td>D0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>X</td><td>0</td><td>0</td><td>D0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>D1</td></tr> <tr><td>1</td><td>1</td><td>X</td><td>0</td><td>X</td><td>0</td><td>D2</td></tr> <tr><td>1</td><td>X</td><td>1</td><td>0</td><td>X</td><td>0</td><td>D2</td></tr> <tr><td>1</td><td>1</td><td>X</td><td>X</td><td>0</td><td>0</td><td>D2</td></tr> <tr><td>1</td><td>X</td><td>1</td><td>X</td><td>0</td><td>0</td><td>D2</td></tr> <tr><td>1</td><td>1</td><td>X</td><td>1</td><td>1</td><td>0</td><td>D3</td></tr> <tr><td>1</td><td>X</td><td>1</td><td>1</td><td>1</td><td>0</td><td>D3</td></tr> </tbody> </table>							CLR	S11	S10	S01	S00	G	Q <sub>n+1</sub>	0	X	X	X	X	X	0	1	X	X	X	X	1	Q	1	0	0	0	X	0	D0	1	0	0	X	0	0	D0	1	0	0	1	1	0	D1	1	1	X	0	X	0	D2	1	X	1	0	X	0	D2	1	1	X	X	0	0	D2	1	X	1	X	0	0	D2	1	1	X	1	1	0	D3	1	X	1	1	1	0	D3
CLR	S11	S10	S01	S00	G	Q <sub>n+1</sub>																																																																																				
0	X	X	X	X	X	0																																																																																				
1	X	X	X	X	1	Q																																																																																				
1	0	0	0	X	0	D0																																																																																				
1	0	0	X	0	0	D0																																																																																				
1	0	0	1	1	0	D1																																																																																				
1	1	X	0	X	0	D2																																																																																				
1	X	1	0	X	0	D2																																																																																				
1	1	X	X	0	0	D2																																																																																				
1	X	1	X	0	0	D2																																																																																				
1	1	X	1	1	0	D3																																																																																				
1	X	1	1	1	0	D3																																																																																				

Family	Modules	
	Seq	Comb
ACT 3	1	

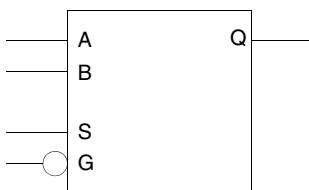
NOTE 1: The DLM8B macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



## DLMA

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

Data Latch with 2-input Multiplexed Data and active low Clock

### Truth Table

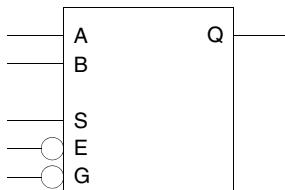
S	G	$Q_{n+1}$
X	1	Q
0	0	A
1	0	B

Input	Output
A, B, G, S	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DLME1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

2-bit Data Latch with Multiplexed Data and Enable and active low Clock and Enable

### Truth Table

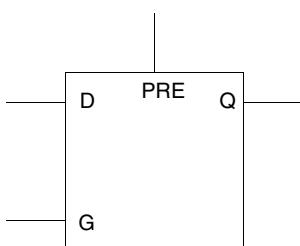
E	S	G	$Q_{n+1}$
1	X	X	Q
X	X	1	Q
0	0	0	A
0	1	0	B

Input	Output
A, B, E, G, S	Q

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DLP1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Data Latch with active high Preset and Clock

### Truth Table

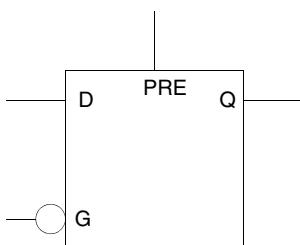
PRE	G	$Q_{n+1}$
1	X	1
0	0	Q
0	1	D

Input	Output
D, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

## DLP1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Data Latch with active high Preset and active low Clock

### Truth Table

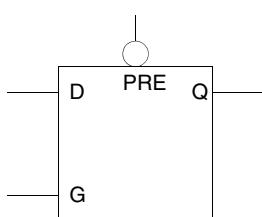
PRE	G	$Q_{n+1}$
1	X	1
0	1	Q
0	0	D

Input	Output
D, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

## DLP1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Data Latch with active low Preset and active high Clock

### Truth Table

PRE	G	$Q_{n+1}$
0	X	1
1	0	Q
1	1	D

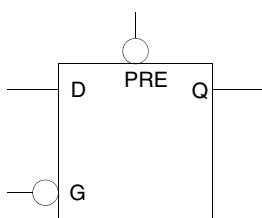
Input  
D, G, PRE

Output  
Q

Family	Modules	
	Seq	Comb
All		1

## DLP1C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Data Latch with active low Preset and Clock

### Truth Table

PRE	G	$Q_{n+1}$
0	X	1
1	1	Q
1	0	D

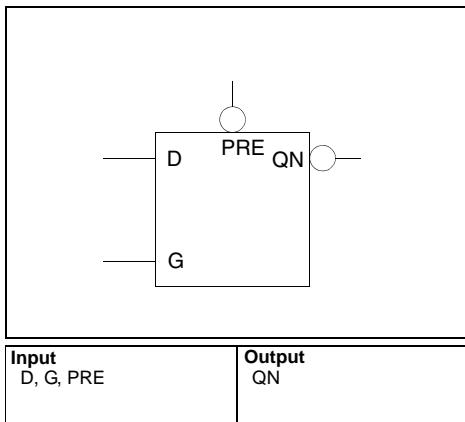
Input  
D, G, PRE

Output  
Q

Family	Modules	
	Seq	Comb
All		1

## DLP1D

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

Data Latch with active low Preset and Output, and active high Clock

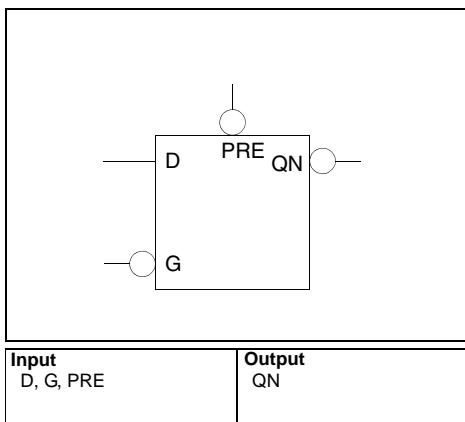
### Truth Table

PRE	G	QN <sub>n+1</sub>
0	X	0
1	0	QN
1	1	ID

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DLP1E

ACT 1, ACT 2, ACT 3, 3200DX, MX, Axcelerator



### Function

Data Latch with active low Preset, Clock, and Output

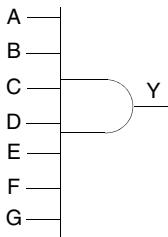
### Truth Table

PRE	G	Q <sub>n+1</sub>
0	X	0
1	0	!D
1	1	QN

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others	1	

## DXAND7

3200DX, MX



### Function

Seven-input AND Gate

### Truth Table

A through G	Y
All inputs = 1	1
Any input = 0	0

### Input

A, B, C, D, E, F, G

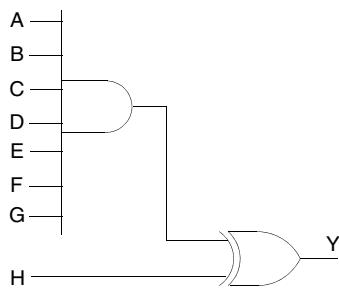
### Output

Y

Family	Modules	
	Seq	DX
3200DX/ MX		1

## DXAX7

3200DX, MX



### Function

Eight-input AND/Exclusive-OR Gate

### Truth Table

A through G	H	Y
Any input = 0	0	0
Any input = 0	1	1
All inputs = 1	0	1
All inputs = 1	1	0

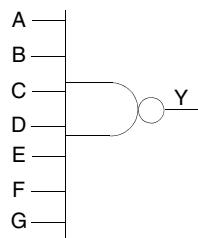
**Input**  
A, B, C, D, E, F, G, H

**Output**  
Y

Family	Modules	
	Seq	DX
3200DX/ MX		1

## DXNAND7

3200DX, MX



### Function

Seven-input NAND Gate

### Truth Table

A through G	Y
All inputs = 1	0
Any input = 0	1

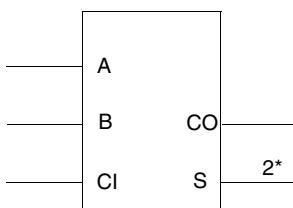
**Input**  
A, B, C, D, E, F, G

**Output**  
Y

Family	Modules	
	Seq	DX
3200DX/ MX		1

# FA1

ACT 1, MX, SX, SX-A, SX-S, eX, Axcelerator



**Input**  
A, B, CI

**Output**  
CO, S

## Function

1 bit adder with active high I/Os

## Truth Table

A	B	CI	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

## Family

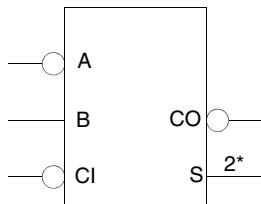
### Modules

Seq	Comb
	3
	2

\* A 2 on the symbol implies 2 logic module delays only in ACT 1 and MX.

# FA1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



**Input**  
A, B, CI

**Output**  
CO, S

## Function

1-bit Adder, with active low Carry In and Carry Out, and active low A-Input

## Truth Table

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0

## Family

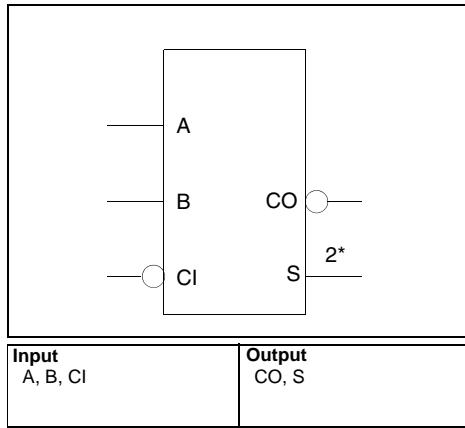
### Modules

Seq	Comb
	2

\* A 2 on the symbol implies 2 logic module delays in all families except SX and SXA.

## FA1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

1-bit Adder with active low Carry In and Carry Out

### Truth Table

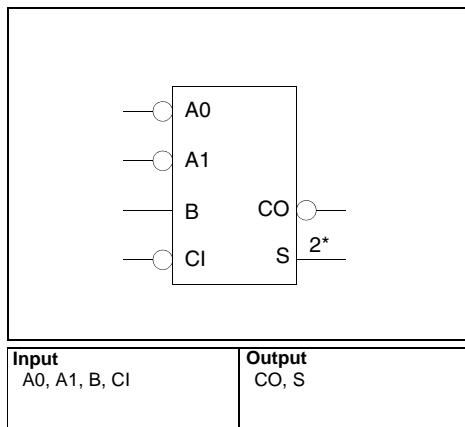
A	B	CI	CO	S
0	0	0	1	1
0	0	1	1	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1

Family	Modules	
	Seq	Comb
All		2

\* A 2 on the symbol implies 2 logic module delays in all families except SX and SXA.

## FA2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

1-bit Adder, with active low Carry In and Carry Out, and active low A0 and A1 Inputs, used in multipliers

### Truth Table 1

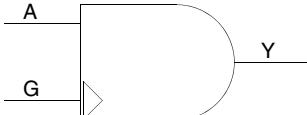
A0	A1	B	CI	CO	S
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	1	1	1
1	1	0	0	1	1

Family	Modules	
	Seq	Comb
All		2

\* A 2 on the symbol implies 2 logic module delays in all families.

## GAND2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input AND Clock Net

### Truth Table

A	G	Y
X	0	0
0	X	0
1	1	1

Input  
A, G

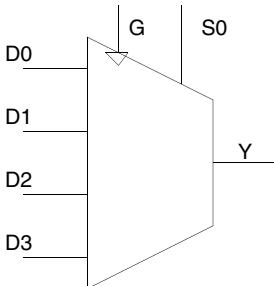
Output  
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a routed clock (RCLK) or hardwired clock (HCLK) if supported by your device.  
See your device datasheet for more info.

## GMX4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-to-1 Mux Clock Net

### Truth Table

G	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Input  
D0, D1, D2, D3, S0, G

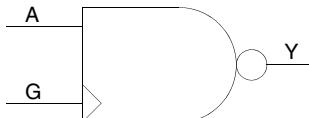
Output  
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a routed clock (RCLK) or hardwired clock (HCLK) if supported by your device.  
See your device datasheet for more info.

## GNAND2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input NAND Clock Net

### Truth Table

A	G	Y
X	0	1
0	X	1
1	1	0

Input  
A, G

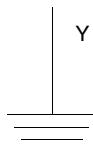
Output  
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a routed clock (RCLK) or hardwired clock (HCLK) if supported by your device.  
See your device datasheet for more info.

## GND

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Ground

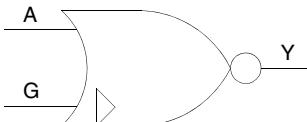
Input

Output  
Y

NOTE: Ground does not use any modules.

## GNOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input NOR Clock Net

### Truth Table

A	G	Y
0	0	1
X	1	0
1	X	0

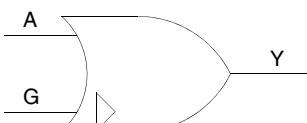
**Input**  
A, G

**Output**  
Y

Family	Modules	
	Seq	Comb
All		1

## GOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input OR Clock Net

### Truth Table

A	G	Y
0	0	0
X	1	1
1	X	1

**Input**  
A, G

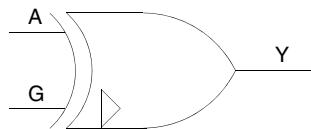
**Output**  
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a routed clock (RCLK) if supported by your device. See your device datasheet for more information.

## GXOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input XOR Clock Net

### Truth Table

A	G	Y
0	0	0
0	1	1
1	0	1
1	1	0

Input  
A, G

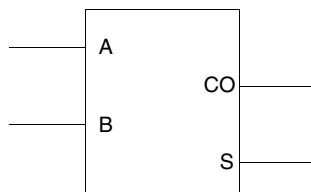
Output  
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a routed clock (RCLK) if supported by your device. See your device datasheet for more information.

## HA1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Half Adder

### Truth Table

A	B	CO	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

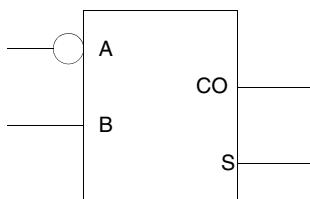
Input  
A, B

Output  
CO, S

Family	Modules	
	Seq	Comb
All		2

## HA1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Half-Adder with active low A-Input

### Truth Table

A	B	CO	S
0	0	0	1
0	1	1	0
1	0	0	0
1	1	0	1

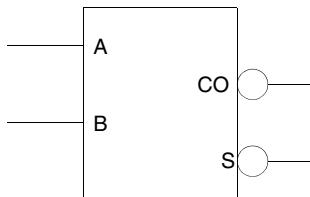
Input  
A, B

Output  
CO, S

Family	Modules	
	Seq	Comb
All		2

## HA1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Half-Adder with active low Carry Out and Sum

### Truth Table

A	B	CO	S
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	1

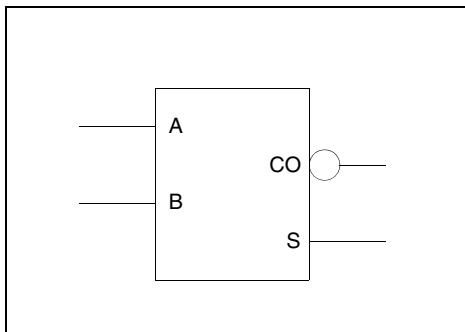
Input  
A, B

Output  
CO, S

Family	Modules	
	Seq	Comb
All		2

## HA1C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Half-Adder with active low Carry Out

### Truth Table

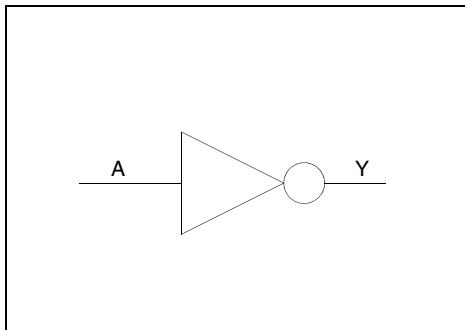
A	B	CO	S
0	0	1	0
0	1	1	1
1	0	1	1
1	1	0	0

Input	Output
A, B	CO, S

Family	Modules	
	Seq	Comb
All		2

## INV

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Inverter with active low Output

### Truth Table

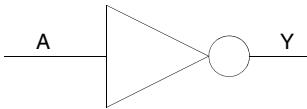
A	Y
0	1
1	0

Input	Output
A	Y

Family	Modules	
	Seq	Comb
All		1

## INVD

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Inverter with active low Output

NOTE: The Combiner will not remove this macro

### Truth Table

A	Y
0	1
1	0

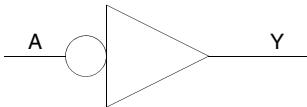
Input  
A

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## INVA

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Inverter with active low Input

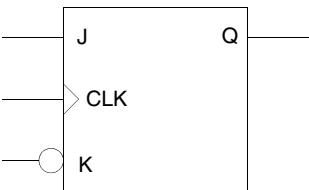
### Truth Table

A	Y
0	1
1	0

Input  
A

Output  
Y

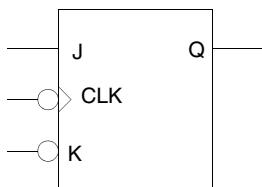
Family	Modules	
	Seq	Comb
All		1

	<p><b>Function</b> JK Flip-Flop with active low K-Input</p>																				
	<p><b>Truth Table</b></p> <table border="1"><thead><tr><th>J</th><th>K</th><th>CLK</th><th><math>Q_{n+1}</math></th></tr></thead><tbody><tr><td>0</td><td>0</td><td>↑</td><td>0</td></tr><tr><td>0</td><td>1</td><td>↑</td><td>Q</td></tr><tr><td>1</td><td>0</td><td>↑</td><td><math>\bar{Q}</math></td></tr><tr><td>1</td><td>1</td><td>↑</td><td>1</td></tr></tbody></table>	J	K	CLK	$Q_{n+1}$	0	0	↑	0	0	1	↑	Q	1	0	↑	$\bar{Q}$	1	1	↑	1
J	K	CLK	$Q_{n+1}$																		
0	0	↑	0																		
0	1	↑	Q																		
1	0	↑	$\bar{Q}$																		
1	1	↑	1																		
<b>Input</b> J, K, CLK	<b>Output</b> Q																				

Family	Modules	
	Seq	Comb
ACT 1/MX		2
SX, SX-A, SX-S, eX	1	1
Others	1	

## JKF1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
J, K, CLK

Output  
Q

### Function

JK Flip-Flop with active low Clock and K-Input

### Truth Table

J	K	CLK	$Q_{n+1}$
0	0	↓	0
0	1	↓	Q
1	0	↓	!Q
1	1	↓	1

### Family

### Modules

Seq      Comb

ACT 1/MX

2

SX, SX-A, SX-S, eX

1

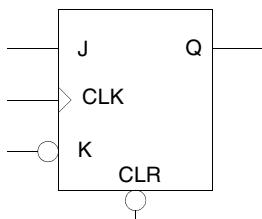
1

Others

1

## JKF2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
CLR, J, K, CLK

Output  
Q

### Function

JK Flip-Flop with active low Clear and K-Input

### Truth Table

CLR	J	K	CLK	$Q_{n+1}$
0	X	X	X	0
1	0	0	↑	0
1	0	1	↑	Q
1	1	0	↑	!Q
1	1	1	↑	1

### Family

### Modules

Seq      Comb

ACT 1/MX

2

SX, SX-A, SX-S, eX

1

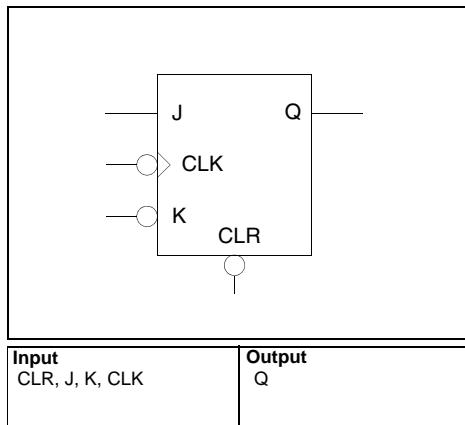
1

Others

1

## JKF2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

JK Flip-Flop with active low Clear, Clock, and K-Input

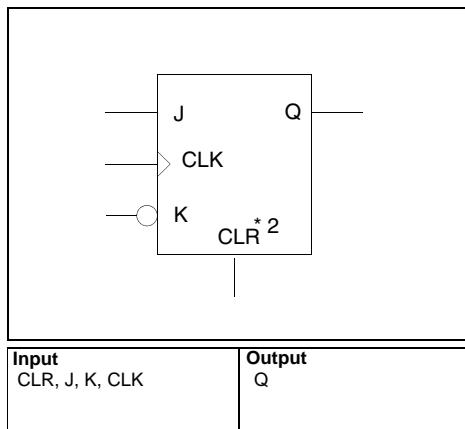
### Truth Table

CLR	J	K	CLK	$Q_{n+1}$
0	X	X	X	0
1	0	0	↓	0
1	0	1	↓	Q
1	1	0	↓	$\overline{Q}$
1	1	1	↓	1

Family	Modules	
	Seq	Comb
ACT 1/MX		2
SX, SX-A, SX-S, eX	1	1
Others	1	

## JKF2C

ACT 1, ACT 2, ACT 3, 3200DX, MX



### Function

JK Flip-Flop with active high Clear and active low K-Input

### Truth Table

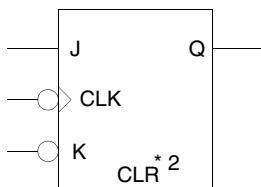
CLR	J	K	CLK	$Q_{n+1}$
1	X	X	X	0
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	$\overline{Q}$
0	1	1	↑	1

Family	Modules	
	Seq	Comb
ACT 1, MX		2
Others	1	1

\* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and MX.

## JKF2D

ACT 1, ACT 2, ACT 3, 3200DX, MX



**Input**  
CLR, J, K, CLK

**Output**  
Q

### Function

JK Flip-Flop with active high Clear and active low Clock and K-Input

### Truth Table

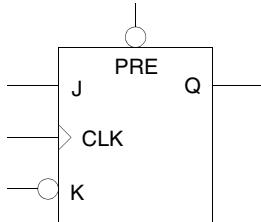
CLR	J	K	CLK	$Q_{n+1}$
1	X	X	X	0
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

Family	Modules	
	Seq	Comb
ACT 1 / MX		2
Others	1	1

\* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and MX.

## JKF3A

ACT 1, MX, SX, SX-A, SX-S, eX, Axcelerator



**Input**  
J, K, PRE, CLK

**Output**  
Q

### Function

JK Flip-Flop with active low Preset and K-Input

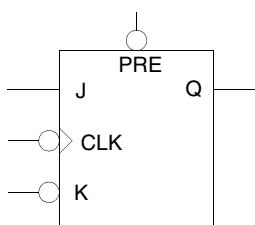
### Truth Table

PRE	J	K	CLK	$Q_{n+1}$
0	X	X	X	1
1	0	0	↑	0
1	0	1	↑	Q
1	1	0	↑	!Q
1	1	1	↑	1

Family	Modules	
	Seq	Comb
ACT 1/MX		2
SX, SX-A, SX-S, eX	1	1

## JKF3B

ACT 1, MX, SX, SX-A, SX-S, eX, Axcelerator

	<b>Input</b> J, K, PRE, CLK	<b>Output</b> Q
-----------------------------------------------------------------------------------	--------------------------------	--------------------

### Function

JK Flip-Flop with active low Preset, Clock, and K-Input

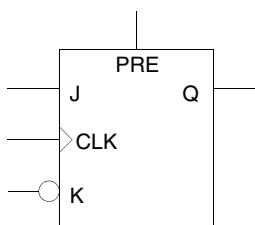
### Truth Table

PRE	J	K	CLK	$Q_{n+1}$
0	X	X	X	1
1	0	0	↓	0
1	0	1	↓	Q
1	1	0	↓	$\bar{Q}$
1	1	1	↓	1

Family	Modules	
	Seq	Comb
ACT 1/MX		2
SX, SX-A, SX-S, eX	1	1

## JKF3C

ACT 1, MX

	<b>Input</b> J, K, PRE, CLK	<b>Output</b> Q
-------------------------------------------------------------------------------------	--------------------------------	--------------------

### Function

JK Flip-Flop with active high Preset and active low K-Input

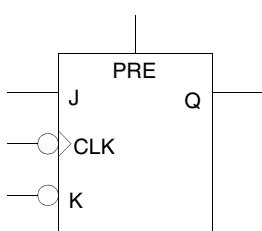
### Truth Table

PRE	J	K	CLK	$Q_{n+1}$
1	X	X	X	1
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	$\bar{Q}$
0	1	1	↑	1

Family	Modules	
	Seq	Comb
ACT 1/MX		2

# JKF3D

ACT 1, MX



## Function

JK Flip-Flop with active high Preset, and active low Clock and K-Inputs

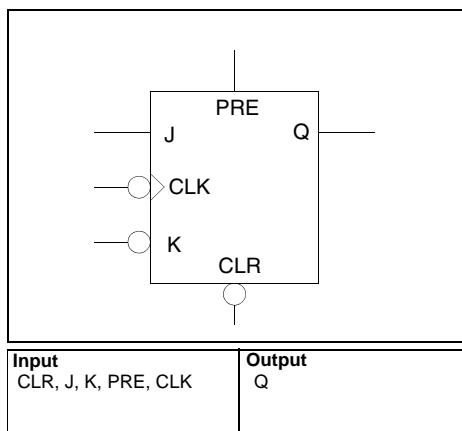
## Truth Table

PRE	J	K	CLK	$Q_{n+1}$
1	X	X	X	1
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	$\bar{Q}$
0	1	1	↓	1

Input  
J, K, PRE, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 1/MX		2

**Function**

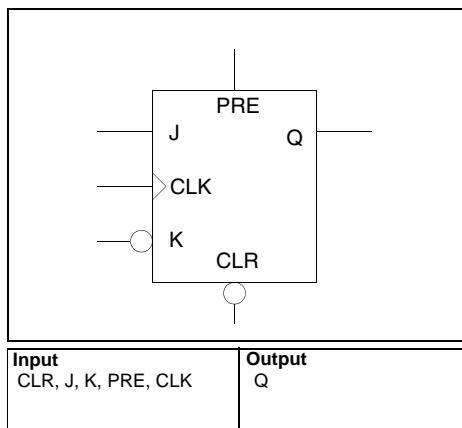
JK Flip-Flop with active high Preset, active low Clear, Clock and K-Input

**Truth Table**

CLR	PRE	J	K	CLK	$Q_{n+1}$
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↓	0
1	0	0	1	↓	Q
1	0	1	0	↓	!Q
1	0	1	1	↓	1
0	1	X	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/MX		2

Your design should not allow both PRE and CLR to be asserted at the same time.

**Function**

JK Flip-Flop with active high Preset, and active low Clear and K- Input

**Truth Table**

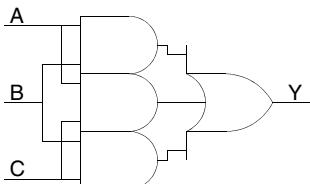
CLR	PRE	J	K	CLK	$Q_{n+1}$
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↑	0
1	0	0	1	↑	Q
1	0	1	0	↑	!Q
1	0	1	1	↑	1
0	1	X	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/MX		2

\* Your design should not allow both PRE and CLR to be asserted at the same time.

## MAJ3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input majority function

### Truth Table

A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

### Family

#### Modules

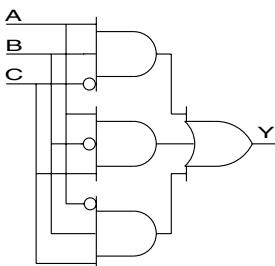
Seq      Comb

All

1

## MAJ3X

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

2 of 3 function

### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

### Family

#### Modules

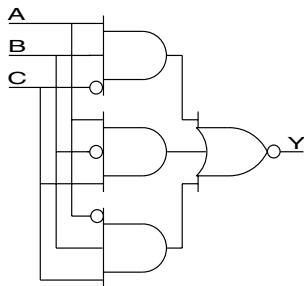
Seq      Comb

SX, SX-A, SX-S, eX

1

## MAJ3XI

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

2 of 3 function with active low output

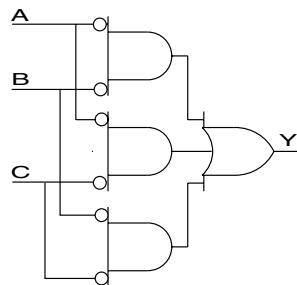
### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## MIN3

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

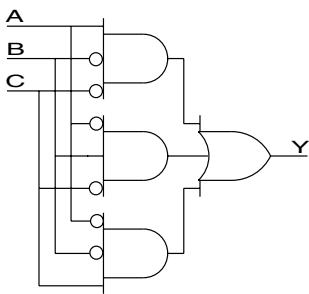
### Function

3-Input minority function

### Truth Table

A	B	C	Y
X	0	0	1
0	0	X	1
0	X	0	1
X	1	1	0
1	X	1	0
1	1	X	0

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

**Input**

A, B, C

**Output**

Y

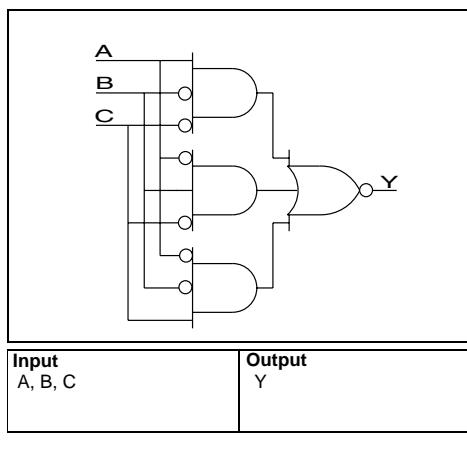
**Function**

1 of 3 function

**Truth Table**

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

**Function**

1 of 3 function with active low output

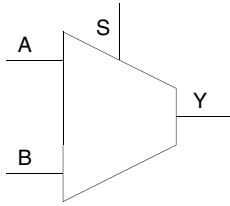
**Truth Table**

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

<b>Family</b>	<b>Modules</b>	
	<b>Seq</b>	<b>Comb</b>
SX, SX-A, SX-S, eX		1

## MX2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2 to 1 Multiplexer

### Truth Table

S	Y
0	A
1	B

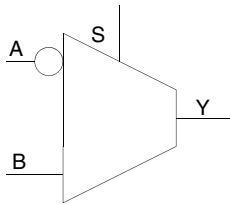
Input  
A, B, S

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## MX2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2 to 1 Multiplexer with active low A-Input

### Truth Table

S	Y
0	!A
1	B

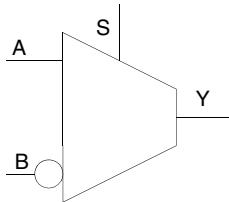
Input  
A, B, S

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## MX2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2 to 1 Multiplexer with active low B-Input

### Truth Table

S	Y
0	A
1	!B

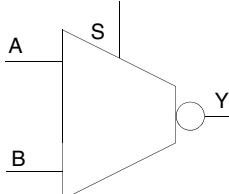
**Input**  
A, B, S

**Output**  
Y

Family	Modules	
	Seq	Comb
All		1

## MX2C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2 to 1 Multiplexer with active low Output

### Truth Table

S	Y
0	!A
1	!B

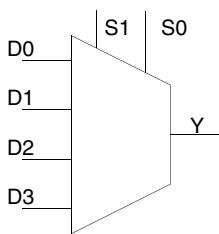
**Input**  
A, B, S

**Output**  
Y

Family	Modules	
	Seq	Comb
All		1

## MX4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
D0, S0, S1, D1, D2, D3

Output  
Y

### Function

4 to 1 Multiplexer

### Truth Table

S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

### Family

#### Modules

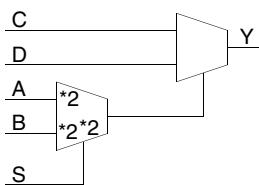
Seq	Comb

All

1

## MXC1

ACT 1, ACT 2, ACT 3, 3200DX, MX



Input  
S, A, B, C, D

Output  
Y

### Function

Carry select multiplexer, used in adders

### Truth Table

A	B	S	Y
0	X	0	C
1	X	0	D
X	0	1	C
X	1	1	D

### Family

#### Modules

Seq	Comb

ACT 1/MX

1

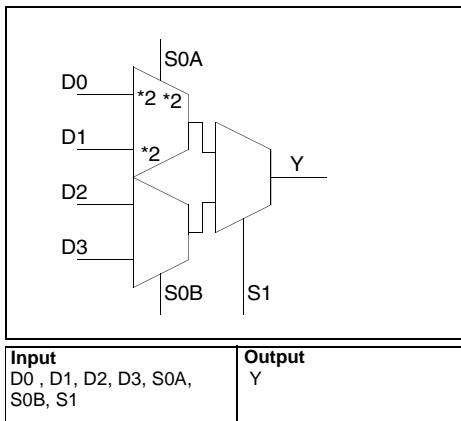
Others

2

A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and MX.

## MXT

ACT 1, ACT 2, ACT 3, 3200DX, MX



Function			
Multiplexer with separate select lines			

Truth Table

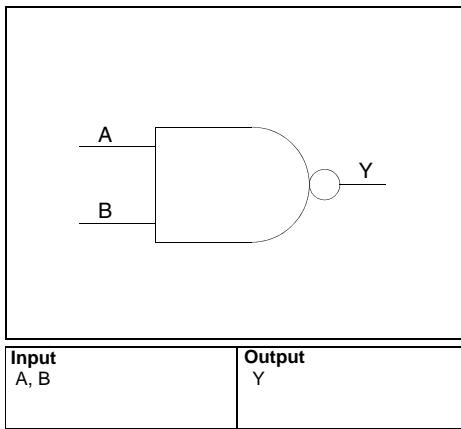
SOB	SOA	S1	Y
X	0	0	D0
X	1	0	D1
0	X	1	D2
1	X	1	D3

Family	Modules	
	Seq	Comb
ACT 1/MX		1
Others		2

\* A 2 on the symbol implies a 2 logic module delay on all families except ACT 1 and MX.

## NAND2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Accelerator



Function		
2-Input NAND		

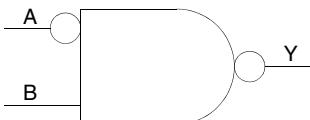
Truth Table

A	B	Y
X	0	1
0	X	1
1	1	0

Family	Modules	
	Seq	Comb
All		1

## NAND2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input NAND with active low A-Input

### Truth Table

A	B	Y
X	0	1
0	1	0
1	X	1

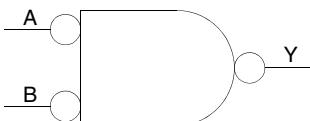
Input  
A, B

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NAND2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input NAND with active low Inputs

### Truth Table

A	B	Y
0	0	0
X	1	1
1	X	1

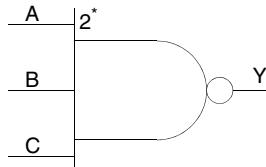
Input  
A, B

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NAND3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input NAND

### Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

Input  
A, B, C

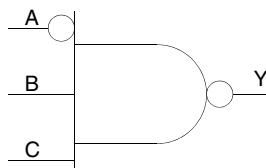
Output  
Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

\* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

## NAND3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input NAND with active low A-Input

### Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	1	1	0
1	X	X	1

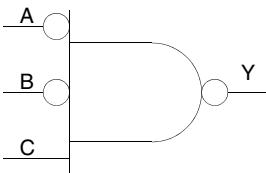
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NAND3B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input NAND with active low A- and B-Inputs

### Truth Table

A	B	C	Y
X	X	0	1
0	0	1	0
X	1	X	1
1	X	X	1

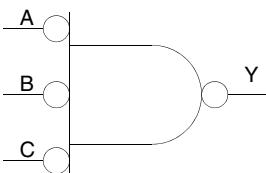
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NAND3C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input NAND with active low Inputs

### Truth Table

A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

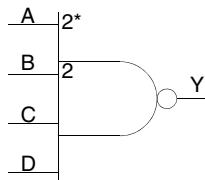
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NAND4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input NAND

### Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

### Family

### Modules

Seq

Comb

SX, SX-A, SX-S, eX

1

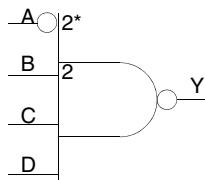
Others

2

\* A 2 on the symbol implies 2 logic module delays except in SX, SX-A, SX-S, and eX.

## NAND4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input NAND with active low A-Input

### Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	1	1	1	0
1	X	X	X	1

### Family

### Modules

Seq

Comb

ACT 1/MX

2

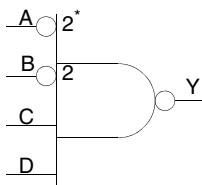
Others

1

\* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

## NAND4B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



**Input**  
A, B, C, D

**Output**  
Y

### Function

4-Input NAND with active low A- and B-Inputs

### Truth Table

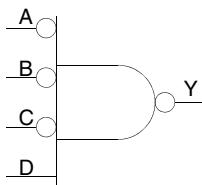
A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	1	1	0
X	1	X	X	1
1	X	X	X	1

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

\* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

## NAND4C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



**Input**  
A, B, C, D

**Output**  
Y

### Function

4-Input NAND with active low A-, B- and C-Inputs

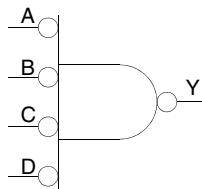
### Truth Table

A	B	C	D	Y
X	X	X	0	1
0	0	0	1	0
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Family	Modules	
	Seq	Comb
All		1

## NAND4D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input NAND with active low Inputs

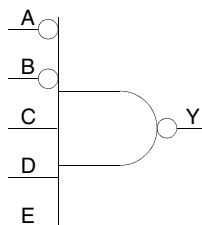
### Truth Table

A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Family	Modules	
	Seq	Comb
All		1

## NAND5B

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D, E

Output  
Y

### Function

5-input NAND with active low A- and B-inputs

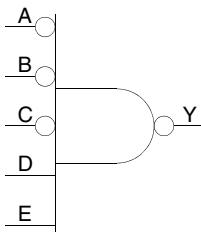
### Truth Table

A	B	C	D	E	Y
1	X	X	X	X	1
X	1	X	X	X	1
X	X	0	X	X	1
X	X	X	0	X	1
X	X	X	X	0	1
0	0	1	1	1	0

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## NAND5C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D, E

Output  
Y

### Function

5-Input NAND with active low A-, B- and C-Inputs

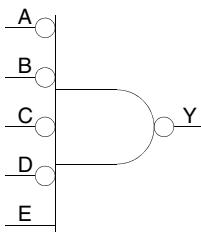
### Truth Table

A	B	C	D	E	Y
X	X	X	X	0	1
X	X	X	0	X	1
0	0	0	1	1	0
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1

Family	Modules	
	Seq	Comb
All listed		1

## NAND5D

Axcelerator



Input  
A, B, C, D, E

Output  
Y

### Function

5-Input NAND with active low A-, B-, C-, and D-Inputs

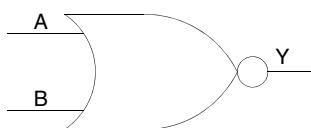
### Truth Table

A	B	C	D	E	Y
X	X	X	X	0	1
X	X	X	1	X	1
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1
0	0	0	0	1	0

Family	Modules	
	Seq	Comb
All listed		1

## NOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Accelerator



### Function

2-Input NOR

### Truth Table

A	B	Y
0	0	1
X	1	0
1	X	0

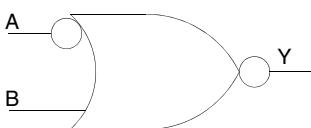
Input  
A, B

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NOR2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Accelerator



### Function

2-Input NOR with active low A-Input

### Truth Table

A	B	Y
0	X	0
1	0	1
X	1	0

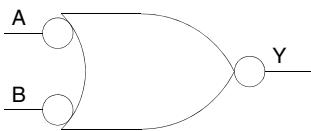
Input  
A, B

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NOR2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input NOR with active low Inputs

### Truth Table

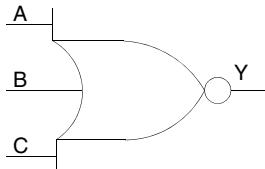
A	B	Y
X	0	0
0	X	0
1	1	1

Input A, B	Output Y

Family	Modules	
	Seq	Comb
All		1

## NOR3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input NOR

### Truth Table

A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

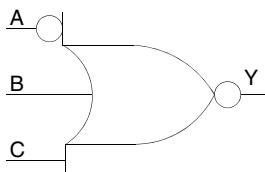
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NOR3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input NOR with active low A-Input

### Truth Table

A	B	C	Y
0	X	X	0
1	0	0	1
X	X	1	0
X	1	X	0

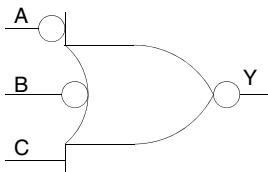
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NOR3B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input NOR with active low A- and B-Inputs

### Truth Table

A	B	C	Y
X	0	X	0
0	X	X	0
1	1	0	1
X	X	1	0

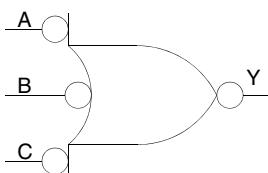
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NOR3C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input NOR with active low Inputs

### Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

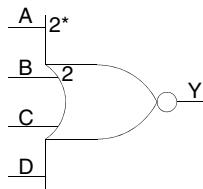
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## NOR4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input NOR

### Truth Table

A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

### Family

### Modules

Seq	Comb
	1
	2

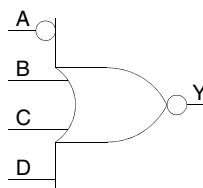
SX, SX-A, SX-S, eX

Others

\* A 2 on the symbol implies 2 logic module delays except SX, SX-A, SX-S, and eX.

## NOR4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input NOR with active low A-Input

### Truth Table

A	B	C	D	Y
0	X	X	X	0
1	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0

### Family

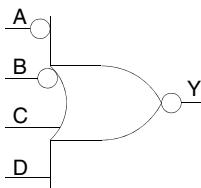
### Modules

Seq	Comb
	1

All

## NOR4B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input NOR with active low A- and B-Inputs

### Truth Table

A	B	C	D	Y
X	0	X	X	0
0	X	X	X	0
1	1	0	0	1
X	X	X	1	0
X	X	1	X	0

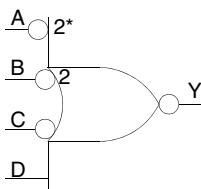
Family  
All

Modules  
Seq Comb

1

## NOR4C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input NOR with active low A-, B- and C-Inputs

### Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	0	1
X	X	X	1	0

Family  
ACT 1/MX  
Others

Modules  
Seq Comb

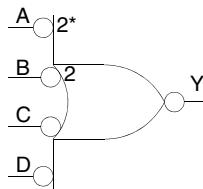
2

1

\* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

## NOR4D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input NOR with active low Inputs

### Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

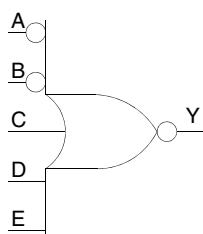
Family

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

\* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

## NOR5B

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D, E

Output  
Y

### Function

5-Input NOR with active low A- and B-Inputs

### Truth Table

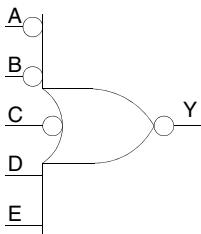
A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	1	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0
1	1	0	0	0	1

Family

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## NOR5C

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D, E

Output  
Y

### Function

5-Input NOR with active low A-, B- and C-Inputs

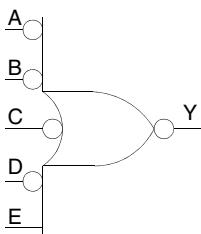
### Truth Table

A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0
1	1	1	0	0	1

Family	Modules	
	Seq	Comb
All listed		1

## NOR5D

Axcelerator



Input  
A, B, C, D, E

Output  
Y

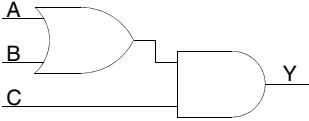
### Function

5-Input NOR with active low A-, B-, C-, and D-Inputs

### Truth Table

A	B	C	D	E	Y
X	X	X	X	1	0
X	X	X	0	X	0
X	X	0	X	X	0
X	0	X	X	X	0
0	X	X	X	X	0
1	1	1	1	0	1

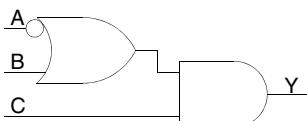
Family	Modules	
	Seq	Comb
All listed		1

	<p><b>Function</b> 3 Input OR-AND</p>																				
<p><b>Truth Table</b></p> <table border="1"><thead><tr><th>A</th><th>B</th><th>C</th><th>Y</th></tr></thead><tbody><tr><td>X</td><td>X</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>X</td><td>0</td></tr><tr><td>X</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>X</td><td>1</td><td>1</td></tr></tbody></table>		A	B	C	Y	X	X	0	0	0	0	X	0	X	1	1	1	1	X	1	1
A	B	C	Y																		
X	X	0	0																		
0	0	X	0																		
X	1	1	1																		
1	X	1	1																		
<p><b>Input</b> A, B, C</p>	<p><b>Output</b> Y</p>																				

Family	Modules	
	Seq	Comb
All		1

## OA1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3 Input OR-AND with active low A-Input

### Truth Table

A	B	C	Y
X	X	0	0
0	X	1	1
1	0	X	0
X	1	1	1

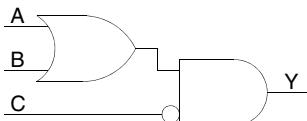
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## OA1B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3 Input OR-AND with active low C-Input

### Truth Table

A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

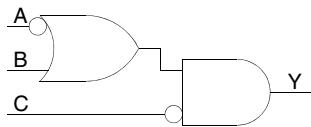
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## OA1C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3 Input OR-AND with active low A- and C-Inputs

### Truth Table

A	B	C	Y
0	X	0	1
X	X	1	0
1	0	X	0
X	1	0	1

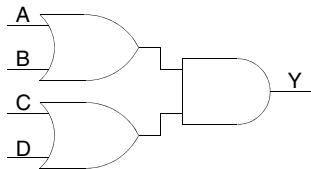
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## OA2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-wide 4-Input OR-AND

### Truth Table

A	B	C	D	Y
X	X	0	0	0
0	0	X	X	0
X	1	X	1	1
X	1	1	X	1
1	X	X	1	1
1	X	1	X	1

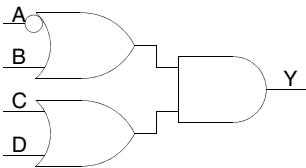
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## OA2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

2 wide 4-Input OR-AND with active low A-Input

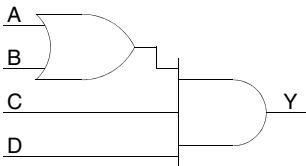
### Truth Table

A	B	C	D	Y
X	X	0	0	0
0	X	X	1	1
0	X	1	X	1
1	0	X	X	0
X	1	X	1	1
X	1	1	X	1

Family	Modules	
	Seq	Comb
All		1

## OA3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4- Input OR-AND

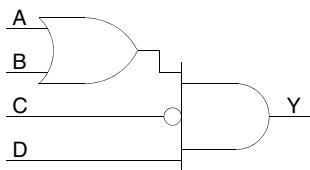
### Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	X	X	0
X	1	1	1	1
1	X	1	1	1

Family	Modules	
	Seq	Comb
All		1

## OA3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input OR-AND with active low C-Input

### Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	X	X	0
X	1	0	1	1
X	X	1	X	0
1	X	0	1	1

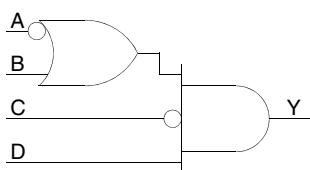
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## OA3B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input OR-AND with active low A- and C-Inputs

### Truth Table

A	B	C	D	Y
X	X	X	0	0
0	X	0	1	1
X	X	1	X	0
1	0	X	X	0
X	1	0	1	1

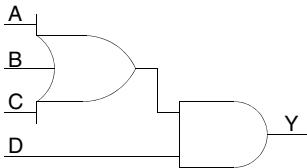
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## OA4

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input OR-AND

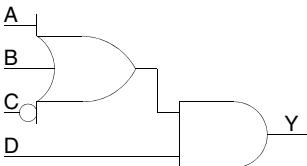
### Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	1	1

Family	Modules	
	Seq	Comb
All listed		1

## OA4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input OR-AND with active low C-Input

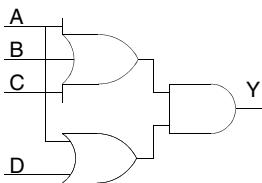
### Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	1	1
0	0	1	X	0
X	1	X	1	1
1	X	X	1	1

Family	Modules	
	Seq	Comb
All		1

## OA5

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C, D

Output  
Y

### Function

4-Input complex OR-AND

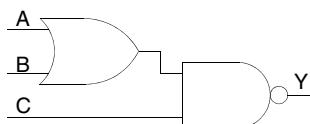
### Truth Table

A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

Family	Modules	
	Seq	Comb
All		1

## OAI1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input OR-AND-INVERT

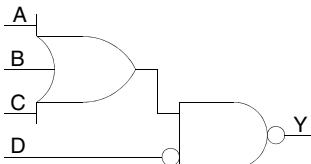
### Truth Table

A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

Family	Modules	
	Seq	Comb
All		1

## OA12A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



**Input**  
A, B, C, D

**Output**  
Y

### Function

4-Input OR-AND-INVERT with active low D-Input

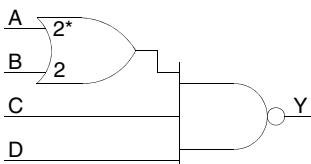
### Truth Table

A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

Family	Modules	
	Seq	Comb
All		1

## OA13

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



**Input**  
A, B, C, D

**Output**  
Y

### Function

4 Input OR-AND-INVERT

### Truth Table

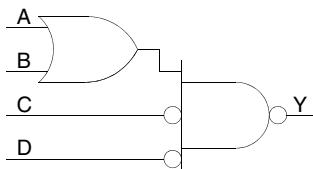
A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

\* A 2 implies 2 logic module delays only for ACT 1 and MX.

# OA13A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



## Function

4 Input OR-AND-INVERT with active low C- and D-Inputs

## Truth Table

A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

**Input**  
A, B, C, D

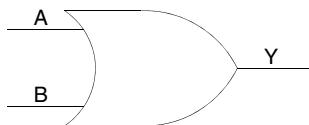
**Output**  
Y

Family	Modules	
	Seq	Comb
All		1



## OR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input OR

### Truth Table

A	B	Y
0	0	0
X	1	1
1	X	1

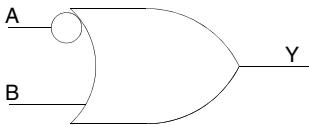
**Input**  
A, B

**Output**  
Y

Family	Modules	
	Seq	Comb
All		1

## OR2A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

2-Input OR with active low A-Input

### Truth Table

A	B	Y
0	X	1
1	0	0
X	1	1

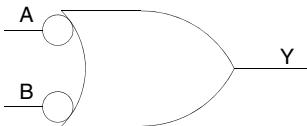
**Input**  
A, B

**Output**  
Y

Family	Modules	
	Seq	Comb
All		1

## OR2B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B	Y

### Function

2-Input OR with active low Inputs

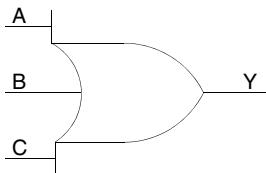
### Truth Table

A	B	Y
X	0	1
0	X	1
1	1	0

Family	Modules	
	Seq	Comb
All		1

## OR3

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input OR

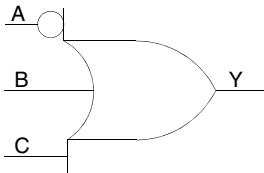
### Truth Table

A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

Family	Modules	
	Seq	Comb
All		1

## OR3A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input OR with active low A-Input

### Truth Table

A	B	C	Y
0	X	X	1
1	0	0	0
X	X	1	1
X	1	X	1

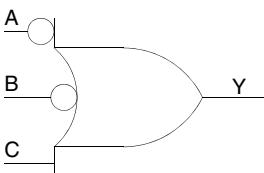
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## OR3B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input OR with active low A- and B-Inputs

### Truth Table

A	B	C	Y
X	0	X	1
0	X	X	1
1	1	0	0
X	X	1	1

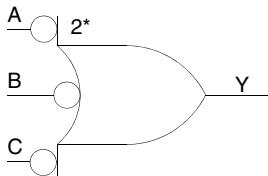
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## OR3C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input OR with active low Inputs

### Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

Input  
A, B, C

Output  
Y

### Family

### Modules

Seq      Comb

ACT 1/MX

2

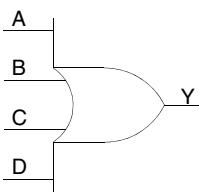
Others

1

\* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

## OR4

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input OR

### Truth Table

A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Input  
A, B, C, D

Output  
Y

### Family

### Modules

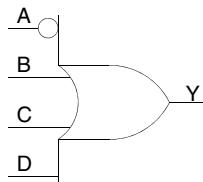
Seq      Comb

All

1

## OR4A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input OR with active low A-Input

### Truth Table

A	B	C	D	Y
0	X	X	X	1
1	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1

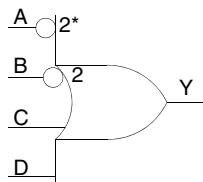
Input  
A, B, C, D

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## OR4B

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input OR with active low A- and B-Inputs

### Truth Table

A	B	C	D	Y
X	0	X	X	1
0	X	X	X	1
1	1	0	0	0
X	X	X	1	1
X	X	1	X	1

Input  
A, B, C, D

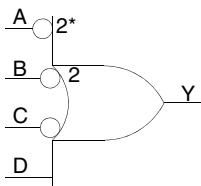
Output  
Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

\* A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

## OR4C

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input OR with active low A-, B- and C-Inputs

### Truth Table

A	B	C	D	Y
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	0	0
X	X	X	1	1

Input  
A, B, C, D

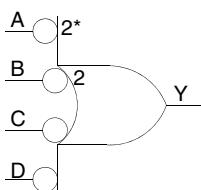
Output  
Y

Family	Modules	
	Seq	Comb
ACT 1/MX		2
Others		1

\*A 2 on the symbol implies 2 logic module delays only for ACT 1 and MX.

## OR4D

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

4-Input OR with active low Inputs

### Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

Input  
A, B, C, D

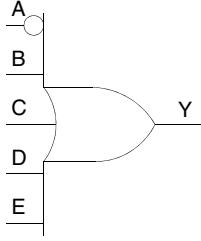
Output  
Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1
Others		2

\* A 2 on the symbol implies 2 logic module delays except for SX, SX-A, SX-S, eX.

## OR5A

SX, SX-A, SX-S, eX, Axcelerator

	<b>Input</b> A, B, C, D, E	<b>Output</b> Y
-----------------------------------------------------------------------------------	-------------------------------	--------------------

<b>Function</b>					
5-Input OR with active low A- Input					

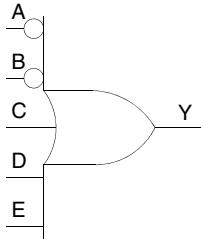
### Truth Table

A	B	C	D	E	Y
0	X	X	X	1	1
X	1	X	X	X	1
X	X	1	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	0	0	0	0	0

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## OR5B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator

	<b>Input</b> A, B, C, D, E	<b>Output</b> Y
------------------------------------------------------------------------------------	-------------------------------	--------------------

<b>Function</b>					
5-Input OR with active low A- and B-Inputs					

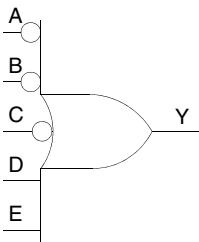
### Truth Table

A	B	C	D	E	Y
X	0	X	X	X	1
0	X	X	X	X	1
1	1	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1

Family	Modules	
	Seq	Comb
All listed		1

## OR5C

SX, SX-A, SX-S, eX, Axcelerator



### Function

5-Input OR with active low A-, B- and C-Inputs

### Truth Table

A	B	C	D	E	Y
0	X	X	X	X	1
X	0	X	X	X	1
X	X	0	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	1	1	0	0	0

Input  
A, B, C, D, E

Output  
Y

### Family

### Modules

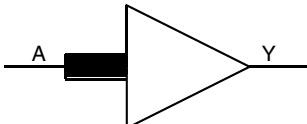
Seq      Comb

SX, SX-A, SX-S, eX

1

## QCLKINT

3200DX, MX, SX-A, SX-S



### Function

Internal Clock Interface

### Truth Table

A	Y
0	0
1	1

Input  
A

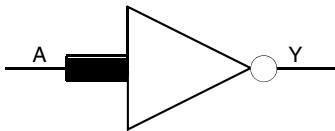
Output  
Y

NOTE: QCLKINT does not use any modules

For more information on the Global Clock Network, refer to Actel's Data Book.

## QCLKINTI

SX-A, SX-S



### Function

Internal Clock Interface

### Truth Table

A	Y
0	1
1	0

Input  
A

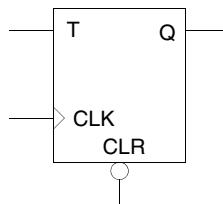
Output  
Y

NOTE: QCLKINTI does not use any modules

For more information on the Global Clock Network, refer to Actel's Data Book.

## TF1A

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Accelerator



### Function

T-Type Flip-Flop with active low Clear

### Truth Table

CLR	T	CLK	Q <sub>n+1</sub>
0	X	X	0
1	1	↑	!Q
1	0	↑	Q

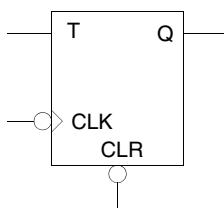
Input  
CLR, T, CLK

Output  
Q

Family	Modules	
	Seq	Comb
All listed	1	

## TF1B

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

T-Type Flip-Flop with active low Clear and Clock

### Truth Table

CLR	T	CLK	$Q_{n+1}$
0	X	X	0
1	1	↓	$\bar{Q}$
1	0	↓	Q

Input  
CLR, T, CLK

Output  
Q

Family	Modules	
	Seq	Comb
All listed	1	

## VCC

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Power

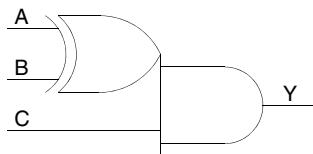
Input

Output  
Y

NOTE: VCC does not use any modules.

## XA1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input XOR-AND

### Truth Table

A	B	C	Y
X	X	0	0
0	0	X	0
0	1	1	1
1	0	1	1
1	1	X	0

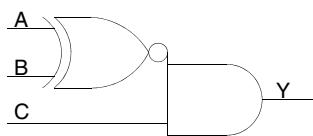
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## XA1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input XNOR-AND

### Truth Table

A	B	C	Y
X	X	0	0
0	0	1	1
0	1	X	0
1	0	X	0
1	1	1	1

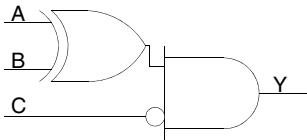
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## XA1B

SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input XNOR-AND with active low C-input

### Truth Table

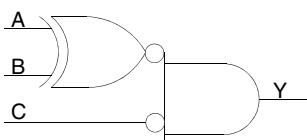
A	B	C	Y
X	X	1	0
0	0	X	0
1	0	0	1
0	1	0	1
1	1	X	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## XA1C

SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input XNOR-AND with active low C-input

### Truth Table

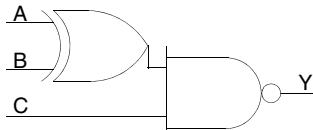
A	B	C	Y
X	X	1	0
0	0	0	1
1	0	X	0
0	1	X	0
1	1	0	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## XAI1

SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input XNOR-NAND

### Truth Table

A	B	C	Y
X	X	0	1
0	0	X	1
1	0	1	0
0	1	1	0
1	1	X	1

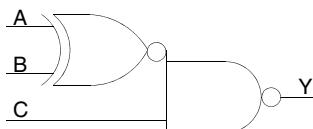
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## XAI1A

SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input XNOR-NAND

### Truth Table

A	B	C	Y
X	X	0	1
0	0	1	0
1	0	X	1
0	1	X	1
1	1	1	0

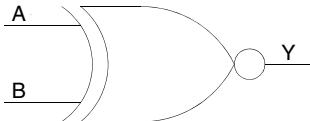
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## XNOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B	Y

### Function

2- Input XNOR

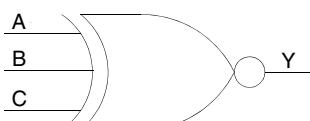
### Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Family	Modules	
	Seq	Comb
All		1

## XNOR3

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input XNOR

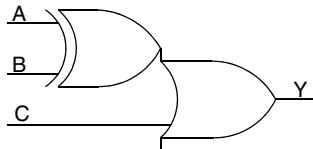
### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## XO1

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input XOR-OR

### Truth Table

A	B	C	Y
0	0	0	0
X	X	1	1
0	1	X	1
1	0	X	1
1	1	0	0

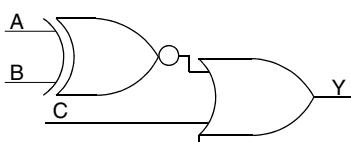
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## XO1A

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

3-Input XNOR-OR

### Truth Table

A	B	C	Y
0	0	0	1
X	X	1	1
0	1	0	0
1	0	0	0
1	1	0	1

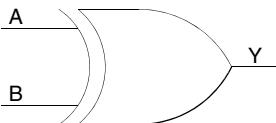
Input  
A, B, C

Output  
Y

Family	Modules	
	Seq	Comb
All		1

## XOR2

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B

Output  
Y

### Function

2-Input XOR

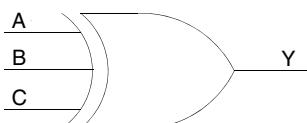
### Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Family	Modules	
	Seq	Comb
All		1

## XOR3

SX, SX-A, SX-S, eX, Axcelerator



Input  
A, B, C

Output  
Y

### Function

3-Input XOR

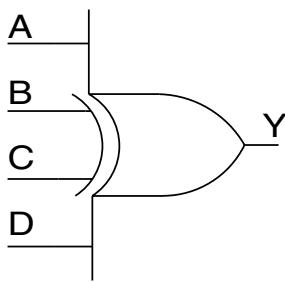
### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## XOR4

Accelerator



### Function

4-Input Exclusive OR Gate

### Truth Table

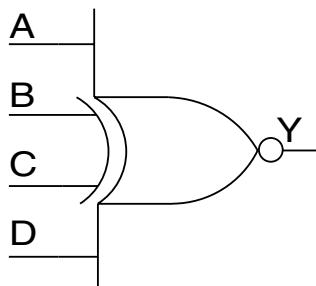
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed		2

## XNOR4

Axcelerator



### Function

4-input Exclusive NOR gate

### Truth Table

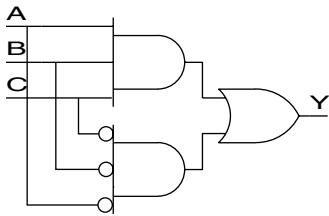
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	0
1	1	1	1	1

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All listed		2

## ZOR3

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input function

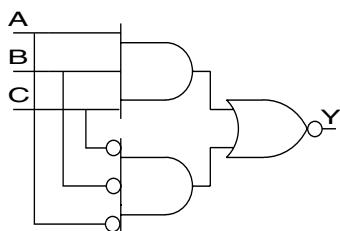
### Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1

## ZOR3I

SX, SX-A, SX-S, eX, Axcelerator



Input	Output
A, B, C	Y

### Function

3-Input function

### Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
SX, SX-A, SX-S, eX		1



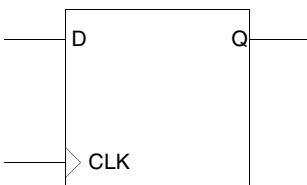
---

## **CC-Module Flip Flops**

These macros are useful in some radiation hostile applications. They sacrifice area in exchange for a lower single-event upset (SEU) rate caused by ion particle collisions. These special cells use two combinational modules to implement a register instead of using the dedicated registers in the array. (See the application note titled, *Design Techniques for RadHard Field Programmable Gate Arrays.*)

## DF1\_CC

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



### Function

D-Type Flip-Flop

### Truth Table

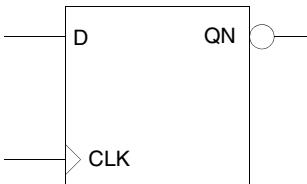
CLK	$Q_{n+1}$
↑	D

Input D, CLK	Output Q
-----------------	-------------

Family	Modules	
	Seq	Comb
All		2

## DF1A\_CC

ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active low Output

### Truth Table

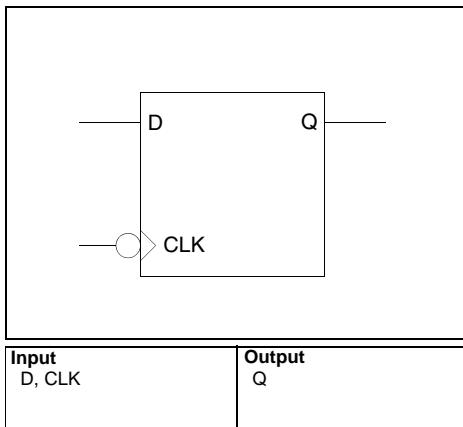
CLK	$QN_{n+1}$
↑	!D

Input D, CLK	Output QN
-----------------	--------------

Family	Modules	
	Seq	Comb
All listed		2

## DF1B\_CC

ACT 2, ACT 3, 3200DX, MX SX, SX-A, SX-S, eX



### Function

D-Type Flip-Flop with active low Clock

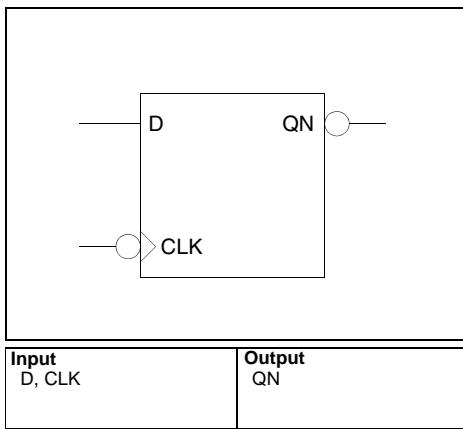
### Truth Table

CLK	$Q_{n+1}$
↓	D

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	

## DF1C\_CC

ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active low Clock and Output

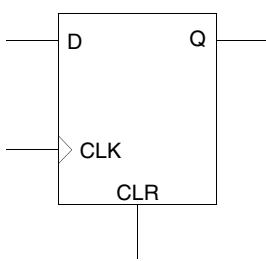
### Truth Table

CLK	$QN_{n+1}$
↓	!D

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2

## DFC1\_CC

ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop, with active high Clear

### Truth Table

CLR	CLK	$Q_{n+1}$
1	X	0
0	↑	D

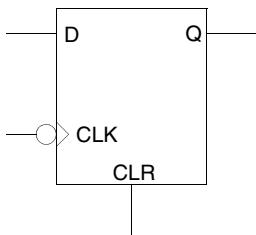
Input  
D, CLK, CLR

Output  
Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2

## DFC1A\_CC

ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop, with active high Clear, and active low Clock

### Truth Table

CLR	CLK	$Q_{n+1}$
1	X	0
0	↓	D

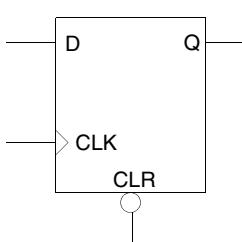
Input  
D, CLK, CLR

Output  
Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2

## DFC1B\_CC

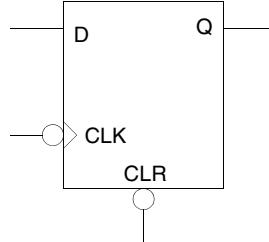
ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX

	<p><b>Function</b> D-Type Flip-Flop, with active low Clear</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>CLR</th><th>CLK</th><th><math>Q_{n+1}</math></th></tr></thead><tbody><tr><td>0</td><td>X</td><td>0</td></tr><tr><td>1</td><td>↑</td><td>D</td></tr></tbody></table> <p><b>Input</b> D, CLK, CLR</p> <p><b>Output</b> Q</p>	CLR	CLK	$Q_{n+1}$	0	X	0	1	↑	D
CLR	CLK	$Q_{n+1}$								
0	X	0								
1	↑	D								

Family	Modules	
	Seq	Comb
All listed		2

## DFC1D\_CC

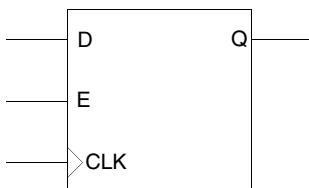
ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX

	<p><b>Function</b> D-Type Flip-Flop, with active low Clear and Clock</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>CLR</th><th>CLK</th><th><math>Q_{n+1}</math></th></tr></thead><tbody><tr><td>0</td><td>X</td><td>0</td></tr><tr><td>1</td><td>↓</td><td>D</td></tr></tbody></table> <p><b>Input</b> D, CLK, CLR</p> <p><b>Output</b> Q</p>	CLR	CLK	$Q_{n+1}$	0	X	0	1	↓	D
CLR	CLK	$Q_{n+1}$								
0	X	0								
1	↓	D								

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	

## DFE\_CC

ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with active high Enable

### Truth Table

E	CLK	$Q_{n+1}$
0	X	Q
1	↑	D

Input  
D, E, CLK

Output  
Q

ACT 2, ACT3, 3200DX, MX

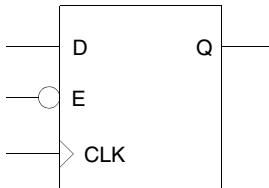
### Modules

Seq      Comb

2

## DFE1B\_CC

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



### Function

D-Type Flip-Flop with active low Enable

### Truth Table

E	CLK	$Q_{n+1}$
1	X	Q
0	↑	D

Input  
D, E, CLK

Output  
Q

ACT 2, ACT3, 3200DX, MX

SX, SX-A, SX-S, eX

### Modules

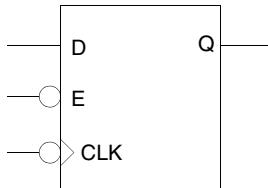
Seq      Comb

2

1

## DFE1C\_CC

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



### Function

D-Type Flip-Flop with active low Enable and Clock

### Truth Table

E	CLK	$Q_{n+1}$
1	X	Q
0	↓	D

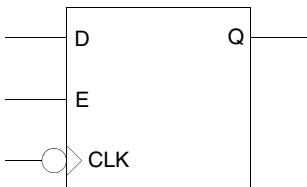
**Input**  
D, E, CLK

**Output**  
Q

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	

## DFEA\_CC

ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with Enable and active low Clock

### Truth Table

E	CLK	$Q_{n+1}$
0	X	Q
1	↓	D

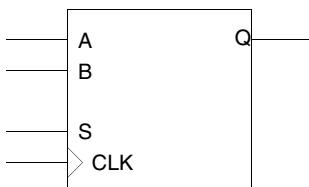
**Input**  
D, E, CLK

**Output**  
Q

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2

## DFM\_CC

ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with 2-input Multiplexed Data

### Truth Table

S	CLK	$Q_{n+1}$
0	↑	A
1	↑	B

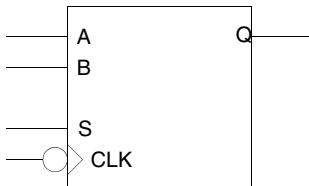
Input  
A, B, S, CLK

Output  
Q

Family	Modules	
	Seq	Comb
All listed		2

## DFMA\_CC

ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

### Truth Table

S	CLK	$Q_{n+1}$
0	↓	A
1	↓	B

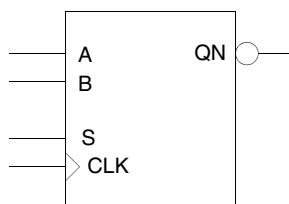
Input  
A, B, S, CLK

Output  
Q

Family	Modules	
	Seq	Comb
ACT 2, ACT3, 3200DX, MX		2

## DFM1B\_CC

ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

### Truth Table

S	CLK	QN <sub>n+1</sub>
0	↑	!A
1	↑	!B

### Input

A, B, S, CLK

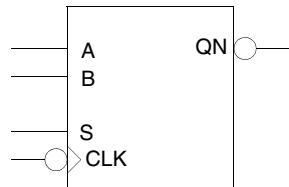
### Output

QN

Family	Modules	
	Seq	Comb
All listed		2

## DFM1C\_CC

ACT 2, ACT 3, 3200DX, MX



### Function

D-Type Flip-Flop with 2-input Multiplexed Data and active low Clock and Output

### Truth Table

S	CLK	QN <sub>n+1</sub>
0	↓	!A
1	↓	!B

### Input

A, B, S, CLK

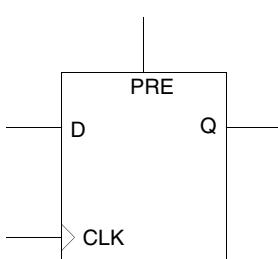
### Output

QN

Family	Modules	
	Seq	Comb
All listed		2

## DFP1\_CC\*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



### Function

D-Type Flip-Flop with active high Preset

### Truth Table

PRE	CLK	$Q_{n+1}$
1	X	1
0	↑	D

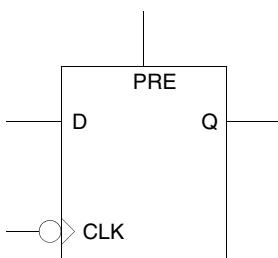
Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	1

\* Identical to macro DFP1.

## DFP1A\_CC\*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



### Function

D-Type Flip-Flop with active high Preset, and active low Clock

### Truth Table

PRE	CLK	$Q_{n+1}$
1	X	1
0	↓	D

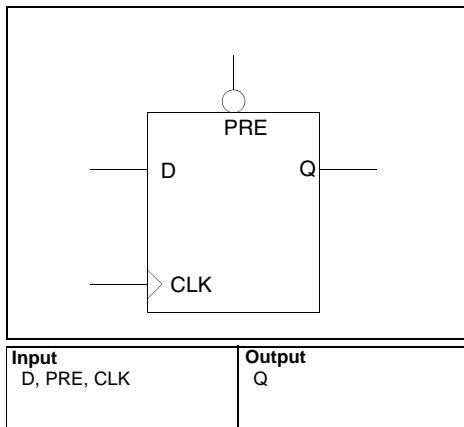
Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	1

\* Identical to macro DFP1A.

## DFP1B\_CC\*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



**Function**  
D-Type Flip-Flop with active low Preset

Truth Table

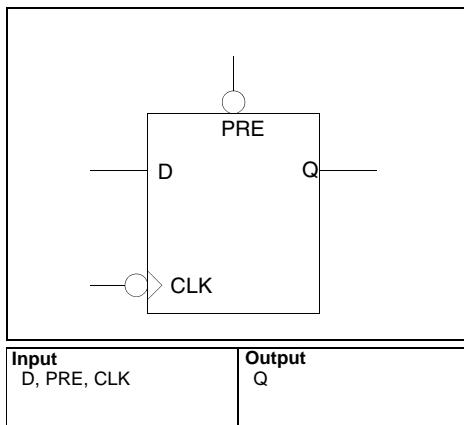
PRE	CLK	$Q_{n+1}$
0	X	1
1	↑	D

Family	Modules	
	Seq	Comb
All		2

\* Identical to macro DFP1B.

## DFP1D\_CC\*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



**Function**  
D-Type Flip-Flop with active low Preset and Clock

Truth Table

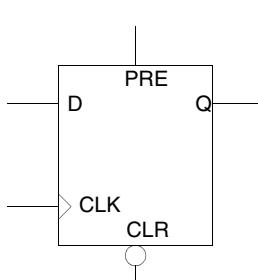
PRE	CLK	$Q_{n+1}$
0	X	1
1	↓	D

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	

\* Identical to macro DFP1D.

## DFPC\_CC\*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



### Function

D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

### Truth Table

CLR	PRE	CLK	$Q_{n+1}$
0	X	X	0
1	1	X	1
1	0	↑	D

Input  
CLR, D, PRE, CLK

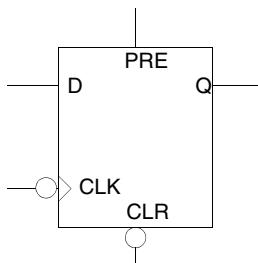
Output  
Q

Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	1

\* Identical to macro DFPC.

## DFPCA\_CC\*

ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX



### Function

D-Type Flip-Flop with active high Preset, active low Clear, and active low Clock

### Truth Table

CLR	PRE	CLK	$Q_{n+1}$
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	**

Input  
CLR, D, PRE, CLK

Output  
Q

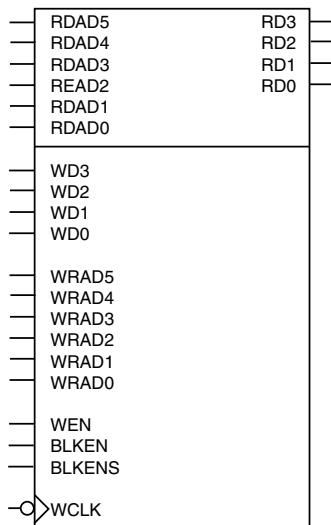
Family	Modules	
	Seq	Comb
ACT 2, ACT 3, 3200DX, MX		2
SX, SX-A, SX-S, eX	1	1

\* Identical to Macro DFPCA.

\*\* Your design should not allow both PRE and CLR to be asserted at the same time.

---

## *Memory Macros*

**Function**

64X4 dual-port RAM with falling Write clock and asynchronous Read

**Truth Table**

<b>WCLK</b>	<b>BLKEN</b>	<b>WEN</b>	<b>Action</b>
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

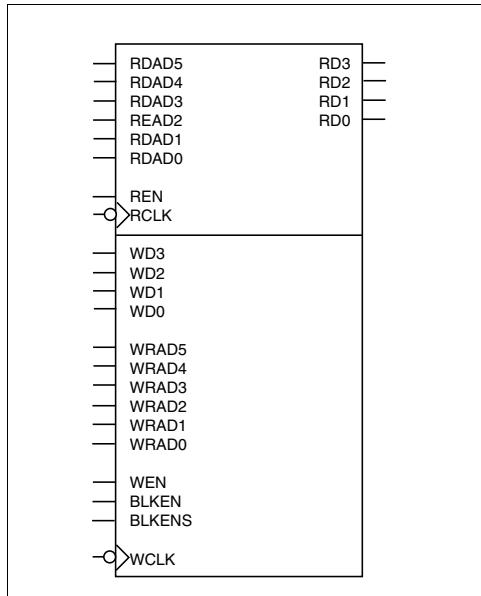
NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

**Input**  
RDAD5, RDAD4,  
RDAD3, RDAD2,  
RDAD1, RDAD0, WD3,  
WD2, WD1, WD0,  
WRAD5, WRAD4,  
WRAD3, WRAD2,  
WRAD1, WRAD0, WEN,  
BLKEN, BLKENS, WCLK

**Output**  
RD3, RD2, RD1, RD0

<b>Family</b>	<b>Modules</b>
	<b>RAM</b>
All listed	1



Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

**Function**

64X4 dual-port RAM with falling Write clock and falling Read clock

**Write Truth Table**

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

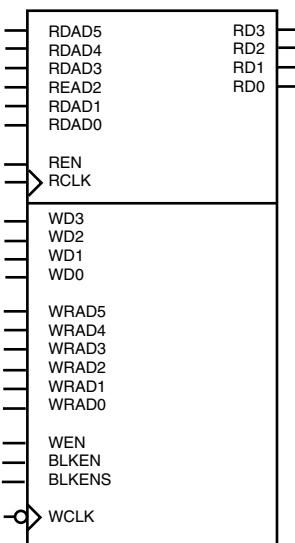
**Read Truth Table**

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1



Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

**Function**

64X4 dual-port RAM with falling Write clock and rising Read clock

**Write Truth Table**

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

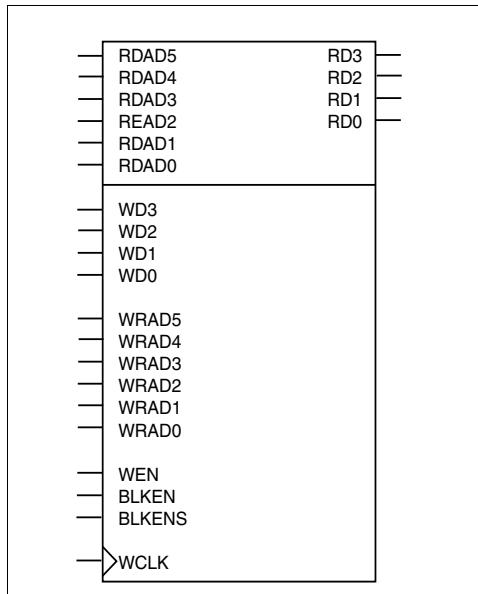
**Read Truth Table**

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1

**Function**

64X4 dual-port RAM with rising Write clock and asynchronous Read

**Write Truth Table**

<b>WCLK</b>	<b>BLKEN</b>	<b>WEN</b>	<b>Action</b>
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

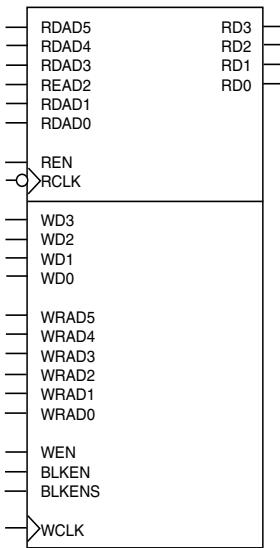
NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

<b>Input</b>
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

<b>Output</b>
RD3, RD2, RD1, RD0

<b>Family</b>	<b>Modules</b>
	<b>RAM</b>
All listed	1



Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS

Output
RD3, RD2, RD1, RD0

**Function**

64X4 dual-port RAM with rising Write clock and falling Read clock

**Write Truth Table**

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

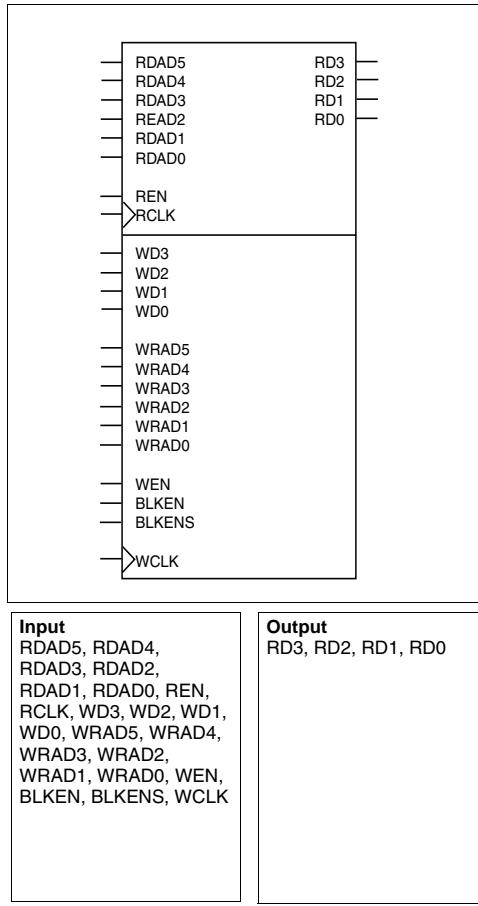
**Read Truth Table**

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1

**Function**

64X4 dual-port RAM with rising Write clock and rising Read clock

**Actel recommends that you do NOT use this macro. Contact  
Actel technical support for more information.****Write Truth Table**

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

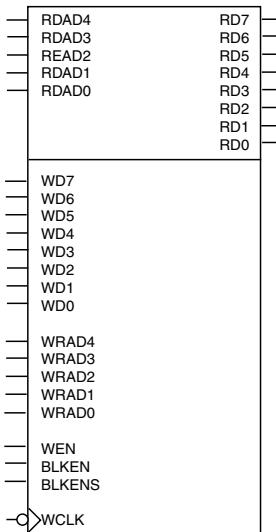
**Read Truth Table**

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All listed	1

**Function**

32X8 dual-port RAM with falling Write clock and asynchronous Read

**Write Truth Table**

<b>WCLK</b>	<b>BLKEN</b>	<b>WEN</b>	<b>Action</b>
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

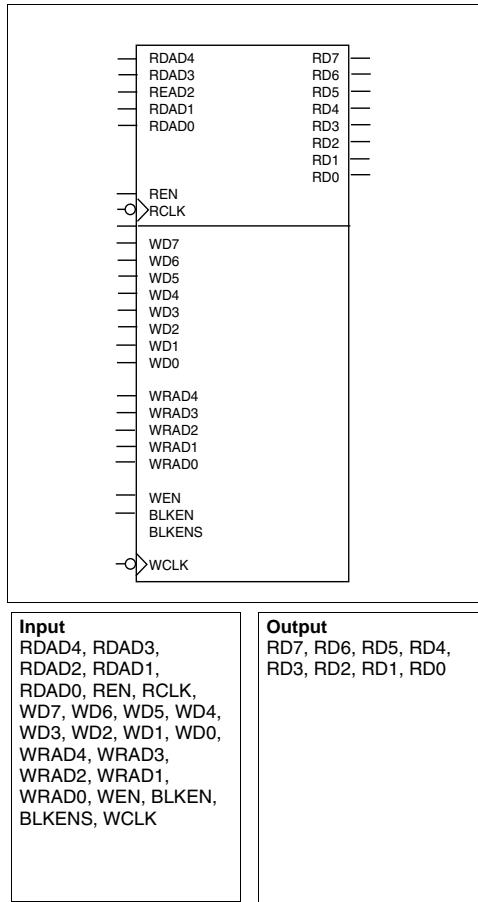
NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

**Input**  
RDAD4, RDAD3,  
RDAD2, RDAD1,  
RDAD0, WD7, WD6,  
WD5, WD4, WD3, WD2,  
WD1, WD0, WRAD4,  
WRAD3, WRAD2,  
WRAD1, WRAD0, WEN,  
BLKEN, BLKENS, WCLK

**Output**  
RD7, RD6, RD5, RD4,  
RD3, RD2, RD1, RD0

<b>Family</b>	<b>Modules</b>
	<b>RAM</b>
All listed	1

**Input**

RDAD4, RDAD3,  
RDAD2, RDAD1,  
RDAD0, REN, RCLK,  
WD7, WD6, WD5, WD4,  
WD3, WD2, WD1, WD0,  
WRAD4, WRAD3,  
WRAD2, WRAD1,  
WRAD0, WEN, BLKEN,  
BLKENS, WCLK

**Output**

RD7, RD6, RD5, RD4,  
RD3, RD2, RD1, RD0

**Function**

32X8 dual-port RAM with falling Write clock and falling Read clock

**Write Truth Table**

<b>WCLK</b>	<b>BLKEN</b>	<b>WEN</b>	<b>Action</b>
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

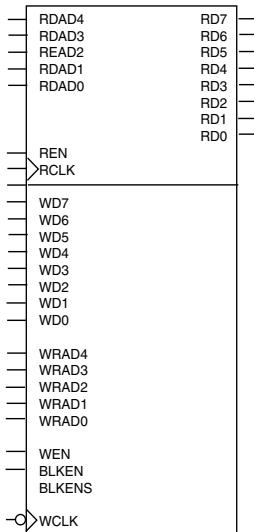
**Read Truth Table**

<b>RCLK</b>	<b>REN</b>	<b>Action</b>
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

<b>Family</b>	<b>Modules</b>
	<b>RAM</b>
All listed	1

**Function**

32X8 dual-port RAM with falling Write clock and rising Read clock

**Write Truth Table**

<b>WCLK</b>	<b>BLKEN</b>	<b>WEN</b>	<b>Action</b>
↓	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

**Read Truth Table**

<b>RCLK</b>	<b>REN</b>	<b>Action</b>
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

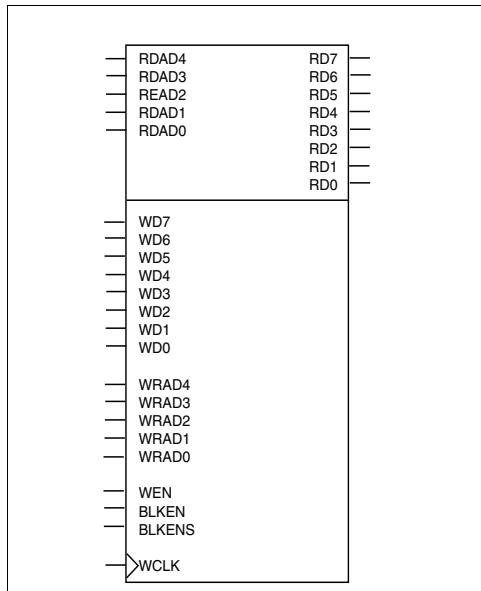
**Input**  
RDAD4, RDAD3,  
RDAD2, RDAD1,  
RDAD0, REN, RCLK,  
WD7, WD6, WD5, WD4,  
WD3, WD2, WD1, WD0,  
WRAD4, WRAD3,  
WRAD2, WRAD1,  
WRAD0, WEN, BLKEN,  
BLKENS, WCLK

**Output**  
RD7, RD6, RD5, RD4,  
RD3, RD2, RD1, RD0

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

<b>Family</b>	<b>Modules</b>
	<b>RAM</b>
All listed	1

**Function**

32X8 dual-port RAM with rising Write clock and asynchronous Read

**Write Truth Table**

<b>WCLK</b>	<b>BLKEN</b>	<b>WEN</b>	<b>Action</b>
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

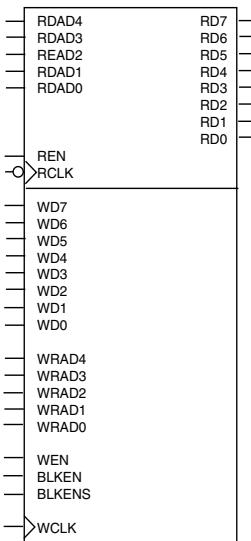
NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

<b>Input</b>	<b>Output</b>
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK	RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

<b>Family</b>	<b>Modules</b>
	<b>RAM</b>
All listed	1

**Input**

RDAD4, RDAD3,  
RDAD2, RDAD1,  
RDAD0, REN, RCLK,  
WD7, WD6, WD5, WD4,  
WD3, WD2, WD1, WD0,  
WRAD4, WRAD3,  
WRAD2, WRAD1,  
WRAD0, WEN, BLKEN,  
BLKENS, WCLK

**Output**

RD7, RD6, RD5, RD4,  
RD3, RD2, RD1, RD0

**Function**

32X8 dual-port RAM with rising Write clock and falling Read clock

**Write Truth Table**

<b>WCLK</b>	<b>BLKEN</b>	<b>WEN</b>	<b>Action</b>
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

**Read Truth Table**

<b>RCLK</b>	<b>REN</b>	<b>Action</b>
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

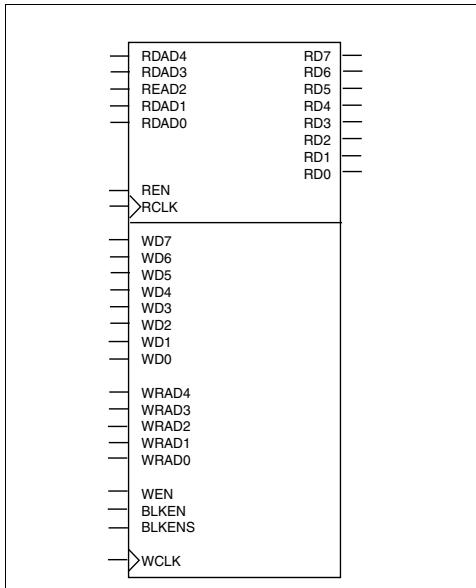
NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

<b>Family</b>	<b>Modules</b>
	<b>RAM</b>
All listed	1

# RAM8RR

3200DX, MX



**Input**  
RDAD4, RDAD3,  
RDAD2, RDAD1,  
RDAD0, REN, RCLK,  
WD7, WD6, WD5, WD4,  
WD3, WD2, WD1, WD0,  
WRAD4, WRAD3,  
WRAD2, WRAD1,  
WRAD0, WEN, BLKEN,  
BLKENS, WCLK

**Output**  
RD7, RD6, RD5, RD4,  
RD3, RD2, RD1, RD0

## Function

32X8 dual-port RAM with rising Write clock and rising Read clock

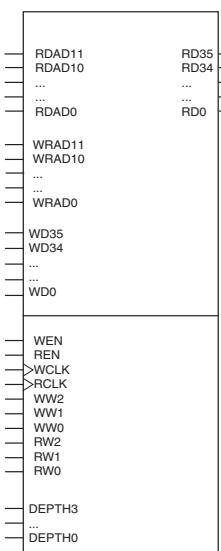
## Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WRAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

## Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Family	Modules
	RAM
All listed	1

**Function**

Dual port completely independent fully synchronous RAM; the RAM blocks may be cascaded up to 16 by configuring the Depth3-0 ports.

Actel recommends you use ACTgen RAM blocks instead of RAM macros because ACTgen configures WW/RW to choose the best aspect ratio and cascades multiple blocks to achieve larger configurations.

For RAM64K36P, data appears on RD after 2 clock cycles on RCLK

**Write Truth Table**

WCLK	WEN	Action
1	1	WD written to WRAD
0	1	None
X	0	None

**Read Truth Table**

RCLK	REN	Action
1	1	RD is read from RDAD
0	1	RD is unchanged
X	0	Rd is unchanged

**Input**  
RDAD11, ..., RDAD0  
WRAD11, ..., WRAD0  
WD35, ..., WD0,  
WEN, REN, WCLK,  
RCLK, WW2, WW1,  
WW0, RW2, RW1, RW0,  
DEPTH3, ..., DEPTH0

**Output**  
RD35, ..., RD0

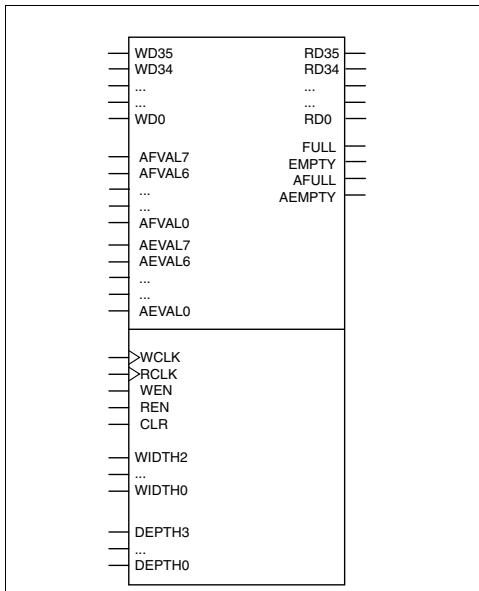
Family	Modules
	RAM
All listed	1

## SRAM Port Aspect Ratios

Read/Write Depth	Read/Write Depth	Read/Write ADDR Bus	Read/Write Data Bus	RW/WW[2:0]
1	4096	ADDR[11:0]	DATA[0]	000
2	2048	ADDR[10:0]	DATA[1:0]	001
4	1024	ADDR[9:0]	DATA[3:0]	010
9	512	ADDR[8:0]	DATA[8:0]	011
18	256	ADDR[7:0]	DATA[17:0]	100
36	128	ADDR[6:0]	DATA[35:0]	101

## FIFO64K36/FIFO64K36P

Axcelerator



### Function

Dual port completely independent fully synchronous FIFO  
For FIFO64K36P, data appears on READ after 2 clock cycles on RCLK. FIFO flag behavior is same as that of FIFO64K36

See the Axcelerator datasheet at <http://www.actel.com> for more information on this macro.

Input	Output
WD35, ..., WD0, AFVAL7, ..., AFVAL0, AEVAL7, ..., AEVAL0, WCLK, RCLK, WEN, REN, CLR, WIDTH2, ..., WIDTH0 DEPTH3, ..., DEPTH0	RD35, ..., RD0 FULL, EMPTY, AFULL, AEMPTY

Family	Modules
	RAM
All listed	1

FIFO Aspect Ratios Table 1

Data Width	FIFO Depth	Read/Write Data Bus	Width[2:0]
1	4096	DATA[0]	000
2	2048	DATA[1:0]	001
4	1024	DATA[3:0]	010
9	512	DATA[8:0]	011
18	256	DATA[17:0]	100
36	128	DATA[35:0]	101

FIFO Aspect Ratios Table 2

<b>Depth</b>	<b>Cascaded Blocks</b>	<b>Full<sup>a</sup></b>	<b>Address Bus WCNT/RCNT</b>	<b>AEVAL/AFVAL Step Size</b>
00001	1	$2^{12-W}$	[15:W]	$2^{8-W}$
00011	2	$2^{13-W}$	[15:W]	$2^{8-W}$
00111	4	$2^{14-W}$	[15:W]	$2^{8-W}$
01111	8	$2^{15-W}$	[15:W]	$2^{8-W}$
11111	16	$2^{16-W}$	[15:W]	$2^{8-W}$

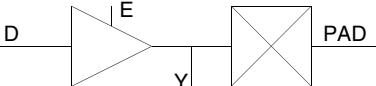
a. W = width in FIFO Aspect Ratios Table 1

---

## *I/O Macros*

## BIBUF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator


<b>Input</b> D, E, PAD <b>Output</b> PAD, Y

### Function

Bidirectional Buffer, High Slew (with Hidden Buffer at Y pin)

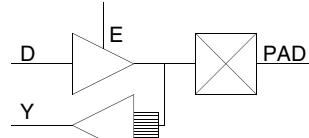
### Truth Table

MODE	E	D	PAD	Y
OUTPUT	1	X	D	D
INPUT	0	X	X	PAD

Family	Modules	
	Seq	I/O
All		1

## CLKBIBUF

ACT1, ACT2, ACT3, 3200DX, 42MX, 54SX, 54SX-A, Axcelerator


<b>Input</b> D, E, PAD <b>Output</b> PAD, Y

### Function

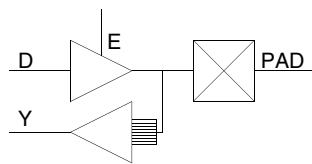
Bidirectional with input dedicated to hardwired clock network

### Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

Family	Modules	
	Seq	I/O
All listed		1

NOTE: Refer to the device-specific datasheet for more Clock Network information.



**Input**  
D, E, PAD

**Output**  
PAD, Y

<b>Family</b>	<b>Modules</b>	
	<b>Seq</b>	<b>I/O</b>
All listed		1

#### Function

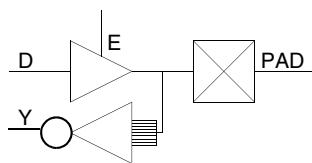
Bidirectional with input dedicated to hardwired clock network

HCLKs (hardwired clocks) can drive only the CLK pins of the dedicated R-Cells, RAM Clock Pins (Read and Write) and IO-REG Clock Pins. The HCLKs cannot drive any other pins of R-Cells, or any pins of C-cells; this rules out CC-Flipflops as well.

#### Truth Table

<b>D</b>	<b>E</b>	<b>PAD</b>	<b>Y</b>
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

NOTE: Refer to the device-specific datasheet for more Clock Network information.



**Input**  
D, E, PAD

**Output**  
PAD, Y

<b>Family</b>	<b>Modules</b>	
	<b>Seq</b>	<b>I/O</b>
SX-A, SX-S		1

#### Function

Bidirectional with inverted Input Dedicated to routed Clock Network

The CLKBIBUFI macro is intended for the SX72-A and SX72-S devices.

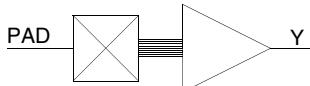
#### Truth Table

<b>D</b>	<b>E</b>	<b>PAD</b>	<b>Y</b>
X	0	Z	X
X	0	0	1
X	0	1	0
0	1	0	1
1	1	1	0

NOTE: Refer to the device-specific datasheet for more Clock Network information.

## CLKBUF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Accelerator



Input	Output
PAD	Y

### Function

Input for Dedicated Routed Clock Network

### Truth Table

PAD	Y
0	0
1	1

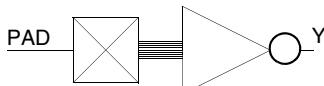
Family	Modules	
	Seq	I/O
All		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

## CLKBUFI

SX, SX-A, SX-S, eX



Input	Output
PAD	Y

### Function

Inverting Input for Dedicated Routed Clock Network

### Truth Table

PAD	Y
0	1
1	0

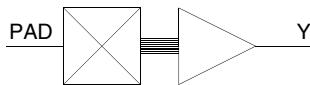
Family	Modules	
	Seq	I/O
SX, SX-A, SX-S, eX		1

NOTE 1: For an internal Clock net, refer to the CLKINTI macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

## HCLKBUF

ACT 3, SX, SX-A, SX-S, eX, Axcelerator



### Function

Dedicated high-speed S-Module Clock Buffer

### Truth Table

PAD	Y
0	0
1	1

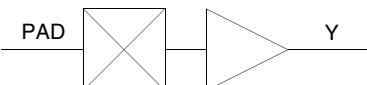
Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
All listed		1

NOTE: Refer to Actel's Databook for more Clock Network information.

## INBUF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



### Function

Input Buffer

### Truth Table

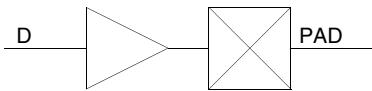
PAD	Y
0	0
1	1

Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
All listed		1

# OUTBUF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX, Axcelerator



## Function

Output Buffer, High Slew

## Truth Table

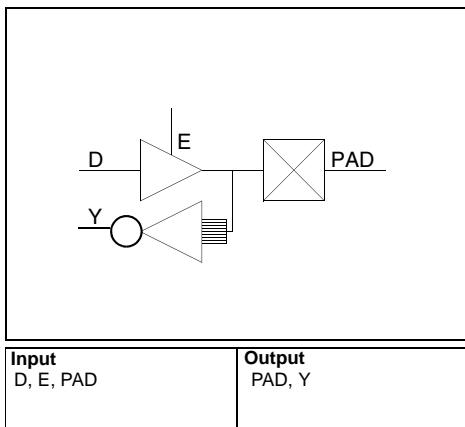
D	PAD
0	0
1	1

Input	Output
D	PAD

Family	Modules	
	Seq	I/O
All		1

## QCLKBIBUFI

SX-A, SX-S



### Function

Bidirectional with inverted Input Dedicated to routed Clock Network

The QCLKBIBUFI macro is intended for the SX72-A and SX72-S devices.

### Truth Table

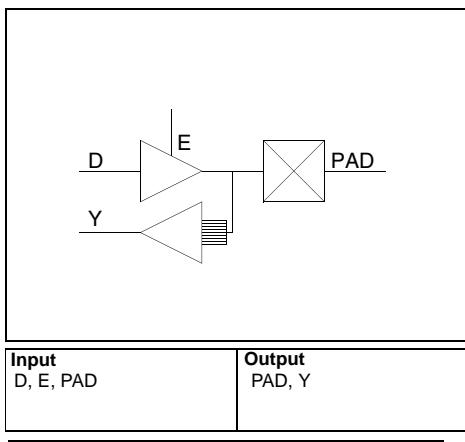
D	E	PAD	Y
X	0	Z	X
X	0	0	1
X	0	1	0
0	1	0	1
1	1	1	0

Family	Modules	
	Seq	I/O
SX-A, SX-S		1

NOTE: Refer to Actel's Databook for more Clock Network information.

## QCLKBIBUF

SX-A, SX-S



### Function

Bidirectional with Input Dedicated to routed Clock Network

The QCLKBIBUF macro is intended for the SX72-A and SX72-S devices.

### Truth Table

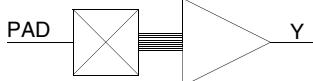
D	E	PAD	Y
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

Family	Modules	
	Seq	I/O
SX-A, SX-S		1

NOTE: Refer to Actel's Databook for more Clock Network information.

## QCLKBUF

3200DX, MX , SX-A, SX-S



### Function

Input for Dedicated Routed Clock Network

### Truth Table

PAD	Y
0	0
1	1

Input	Output
PAD	Y

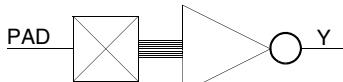
Family	Modules	
	Seq	I/O
All listed		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

## QCLKBUFI

SX-A, SX-S



### Function

Inverted Input for Dedicated Routed Clock Network

The QCLKBUFI macro is intended for the SX72-A and SX72-S devices.

### Truth Table

PAD	Y
0	1
1	0

Input	Output
PAD	Y

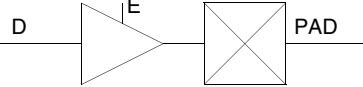
Family	Modules	
	Seq	I/O
SX-A, SX-S		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

# TRIBUFF

ACT 1, ACT 2, ACT 3, 3200DX, MX, SX, SX-A, SX-S, eX

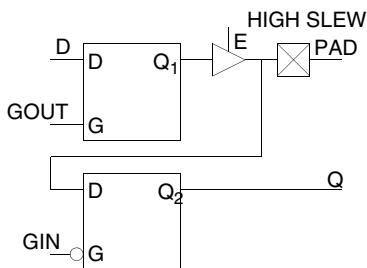
	<p><b>Function</b> Tristate Output, High Slew</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>E</th><th>PAD</th></tr></thead><tbody><tr><td>0</td><td>Z</td></tr><tr><td>1</td><td>D</td></tr></tbody></table>	E	PAD	0	Z	1	D
E	PAD						
0	Z						
1	D						
<b>Input</b> D, E	<b>Output</b> PAD						

Family	Modules	
	Seq	I/O
All		1

NOTE: Refer to Actel's Databook for internal tristate implementation using multiplexers.

## BBDLHS

ACT 2, 3200DX, MX



### Function

Bidirectional with Input Latch and Output Latch

### Truth Table

MODE	E	GOUT	GIN	PAD	Q
OUTPUT	1	0	1	PAD <sub>n-1</sub>	Q <sub>n-1</sub>
	1	1	0	D	D
INPUT	0	X	1	X	Q <sub>n-1</sub>
	0	X	0	X	PAD
TRISTATE	0	X	X	Z	X

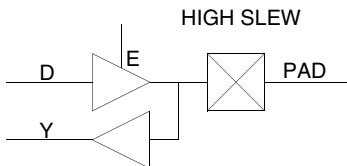
Input  
D, E, GOUT, GIN, PAD

Output  
PAD, Q

Family	Modules	
	Seq	I/O
All listed		1

## BBHS

ACT 2, ACT 3, 3200DX, MX



### Function

Bidirectional Buffer, High Slew

### Truth Table

MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Input  
D, E, PAD

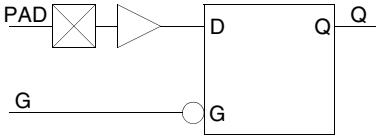
Output  
PAD, Y

Family	Modules	
	Seq	I/O
All listed		1

NOTE: For new designs, instead of BBHS we recommend that you use "BIBUF" on page 256.

## IBDL

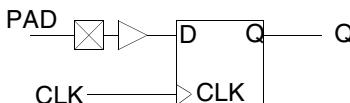
ACT 2, 3200DX, MX

	<p><b>Function</b> Input Buffer with Input Latch, with active low Clock</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>G</th><th>Q</th></tr></thead><tbody><tr><td>1</td><td><math>Q_{n-1}</math></td></tr><tr><td>0</td><td>PAD</td></tr></tbody></table> <p><b>Input</b> G, PAD</p> <p><b>Output</b> Q</p>	G	Q	1	$Q_{n-1}$	0	PAD
G	Q						
1	$Q_{n-1}$						
0	PAD						

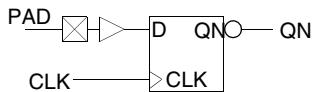
Family	Modules	
	Seq	I/O
All listed		1

## IR

ACT 2, 3200DX, MX

	<p><b>Function</b> Input Register</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>CLK</th><th>Q</th></tr></thead><tbody><tr><td>↑</td><td>PAD</td></tr></tbody></table> <p><b>Input</b> PAD, CLK</p> <p><b>Output</b> Q</p>	CLK	Q	↑	PAD
CLK	Q				
↑	PAD				

Family	Modules	
	Seq	I/O
All listed	1	1

**Function**

Input register with active Low output

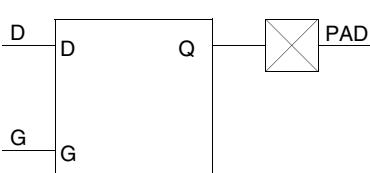
**Truth Table**

CLK	QN
↑	!PAD

Input  
PAD, CLKOutput  
QN

Family	Modules	
	Seq	I/O
All listed	1	1

HIGH SLEW

**Function**

Output Buffer with Output Latch, High Slew

**Truth Table**

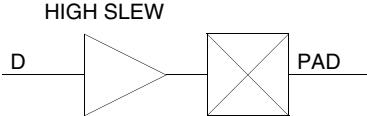
G	PAD
0	PAD <sub>n-1</sub>
1	D

Input  
D, GOutput  
PAD

Family	Modules	
	Seq	I/O
All listed		1

## OBHS

ACT 2, ACT 3, 3200DX, MX

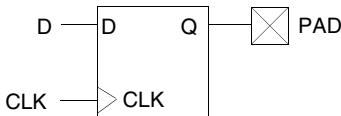
 <p>HIGH SLEW</p> <p>D ————— ————— X ————— PAD</p>	<p><b>Function</b> Output Buffer, High Slew</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>D</th><th>PAD</th></tr></thead><tbody><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></tbody></table> <p><b>Input</b> D</p> <p><b>Output</b> PAD</p>	D	PAD	0	0	1	1
D	PAD						
0	0						
1	1						

Family	Modules	
	Seq	I/O
All listed		1

NOTE: For new designs, instead of OBHS we recommend that you use "OUTBUF" on page 260.

## ORH

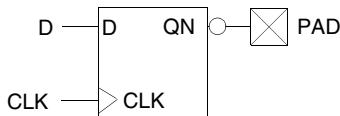
ACT 2, 3200DX, MX

 <p>D ————— ———— Q ————— X ————— PAD</p> <p>CLK ————— ———— CLK</p>	<p><b>Function</b> Output Register, High Slew</p> <p><b>Truth Table</b></p> <table border="1"><thead><tr><th>CLK</th><th>PAD<sub>n+1</sub></th></tr></thead><tbody><tr><td>↑</td><td>D</td></tr></tbody></table> <p><b>Input</b> D, CLK</p> <p><b>Output</b> PAD</p>	CLK	PAD <sub>n+1</sub>	↑	D
CLK	PAD <sub>n+1</sub>				
↑	D				

Family	Modules	
	Seq	I/O
All listed	1	1

## ORIH

ACT 2, 3200DX, MX



### Function

Inverted Output Register, High Slew

### Truth Table

CLK	$PAD_{n+1}$
↑	!D

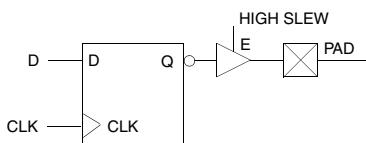
**Input**  
D, CLK

**Output**  
PAD

Family	Modules	
	Seq	I/O
All listed	1	1

## ORITH

ACT 2, 3200DX, MX



### Function

Inverted Output Register, Tristate Enable, High Slew

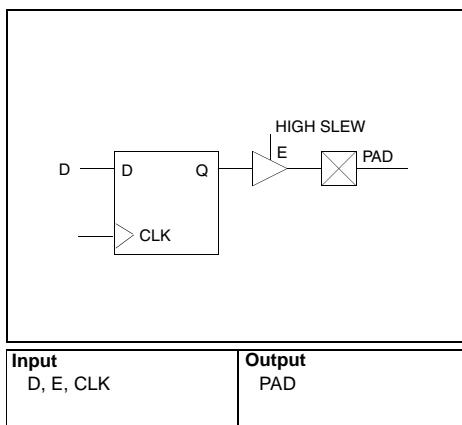
### Truth Table

E	CLK	$PAD_{n+1}$
0	X	Z
1	↑	!D

**Input**  
D, E, CLK

**Output**  
PAD

Family	Modules	
	Seq	I/O
All listed	1	1

**Function**

Output Register, Tristate Enable, High Slew

**Truth Table**

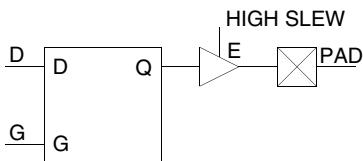
E	CLK	PAD <sub>n+1</sub>
0	X	Z
1	↑	D

Input	Output
D, E, CLK	PAD

Family	Modules	
	Seq	I/O
All listed	1	1

## TBDLHS

ACT 2, 3200DX, MX



### Function

Tristate Output with Latch, High Slew

### Truth Table

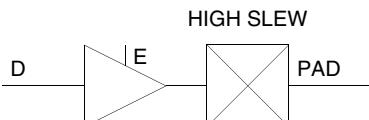
E	G	PAD
0	X	Z
1	1	D
1	0	PAD <sub>n-1</sub>

Input	Output
D, E, G	PAD

Family	Modules	
	Seq	I/O
All listed		1

## TBHS

ACT 2, ACT 3, 3200DX, MX



### Function

Tristate Output, High Slew

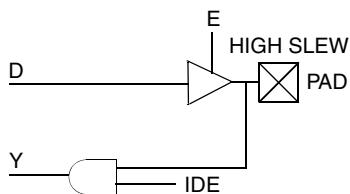
### Truth Table

E	PAD
0	Z
1	D

Input	Output
D, E	PAD

Family	Modules	
	Seq	I/O
All listed		1

NOTE: For new designs, instead of TBHS we recommend that you use "TRIBUFF" on page 263.

**Function**

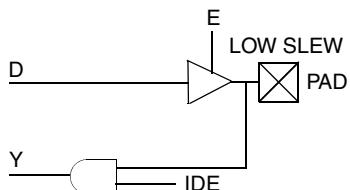
Bidirectional buffer with AND gate, High Slew

**Truth Table**

MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

**Input**  
D, E, IDE, PAD**Output**  
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

**Function**

Bidirectional buffer with AND gate, Low Slew

**Truth Table**

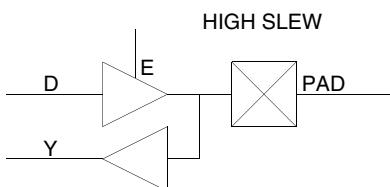
MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

**Input**  
D, E, IDE, PAD**Output**  
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

## BBUFTH

ACT 3



### Function

Bidirectional Buffer, Tristate Enable, High Slew

### Truth Table

MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

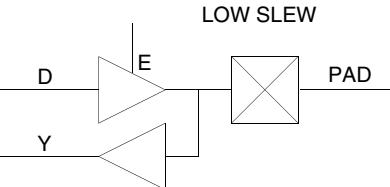
Input  
D, E, PAD

Output  
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

## BBUFTL

ACT 3



### Function

Bidirectional Buffer, Tristate Enable, Low Slew

### Truth Table

MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

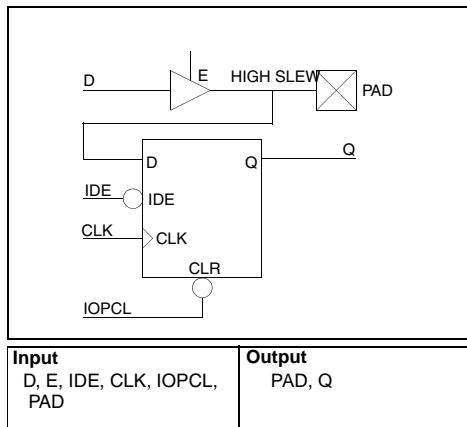
Input  
D, E, PAD

Output  
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

## BIECTH

ACT 3



### Function

Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, High Slew

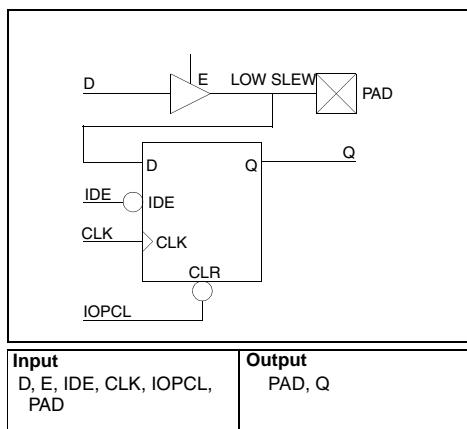
### Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q <sub>n-1</sub>
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q <sub>n-1</sub>

Family	Modules	
	Seq	I/O
ACT 3		1

## BIECTL

ACT 3



### Function

Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, Low Slew

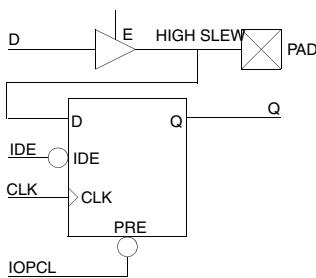
### Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q <sub>n-1</sub>
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q <sub>n-1</sub>

Family	Modules	
	Seq	I/O
ACT 3		1

## BIEPTH

ACT 3



Input	Output
D, E, IDE, CLK, IOPCL, PAD	PAD, Q

**Function**

Bidirectional Input Register with Preset, Input Data Enable, Tristate Enable, High Slew

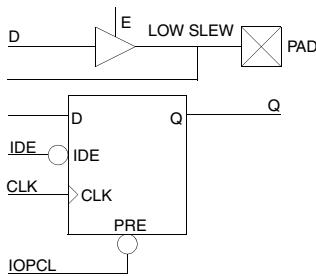
**Truth Table**

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q <sub>n-1</sub>
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q <sub>n-1</sub>

Family	Modules	
	Seq	I/O
ACT 3		1

## BIEPTL

ACT 3



Input	Output
D, E, IDE, CLK, IOPCL, PAD	PAD, Q

**Function**

Bidirectional Input Register with Preset, Input Data Enable, Tristate Enable, Low Slew

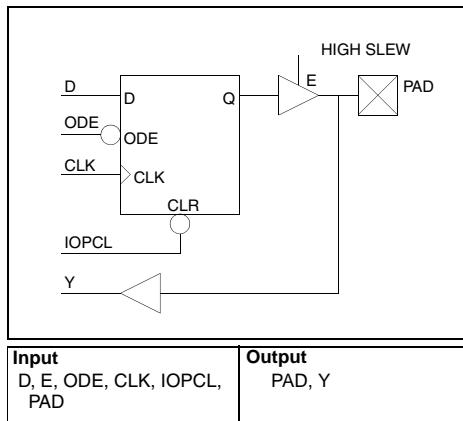
**Truth Table**

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q <sub>n-1</sub>
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q <sub>n-1</sub>

Family	Modules	
	Seq	I/O
ACT 3		1

## BRECH

ACT 3



### Function

Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

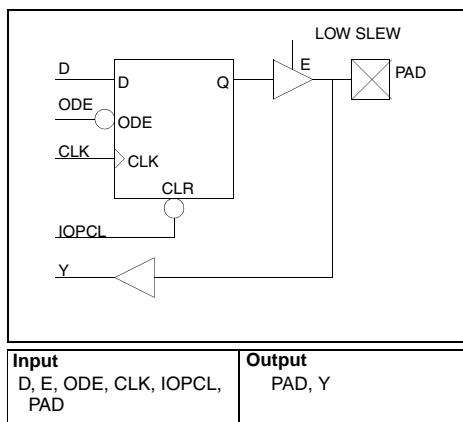
### Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD <sub>n-1</sub>	Y <sub>n-1</sub>
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

## BRECTL

ACT 3



### Function

Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

### Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD <sub>n-1</sub>	Y <sub>n-1</sub>
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

## BREPTH

ACT 3

<b>Input</b> D, E, ODE, CLK, IOPCL, PAD  <b>Output</b> PAD, Y

Function						
Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew						

### Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD <sub>n-1</sub>	Y <sub>n-1</sub>
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

## BREPTL

ACT 3

<b>Input</b> D, E, ODE, CLK, IOPCL, PAD  <b>Output</b> PAD, Y

Function						
Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew						

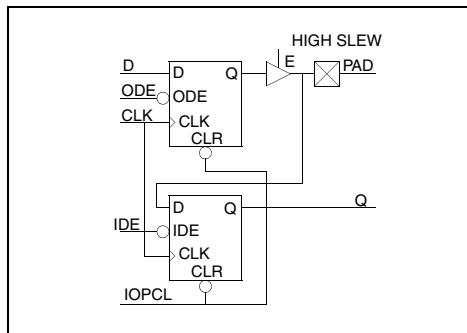
### Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD <sub>n-1</sub>	Y <sub>n-1</sub>
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

## DECETH

ACT 3



Input	Output
D, E, IDE, CLK, IOPCL, PAD, ODE	PAD, Q

### Function

Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

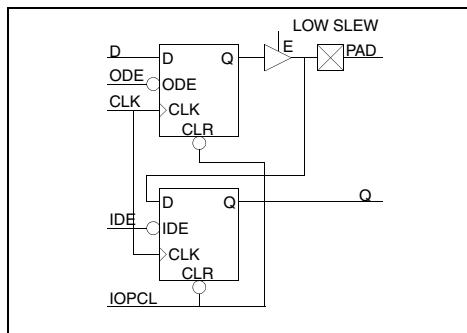
### Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD <sub>n-1</sub>	Q <sub>n-1</sub>
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q <sub>n-1</sub>

Family	Modules	
	Seq	I/O
ACT 3		1

## DECETL

ACT 3



Input	Output
D, E, ODE, CLK, IOPCL, IDE, PAD	PAD, Q

### Function

Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

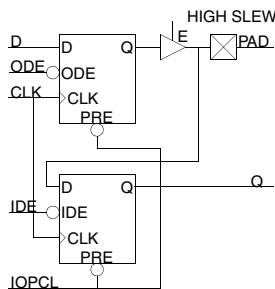
### Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD <sub>n-1</sub>	Q <sub>n-1</sub>
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q <sub>n-1</sub>

Family	Modules	
	Seq	I/O
ACT 3		1

## DEPETH

ACT 3



### Function

Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

### Truth Table

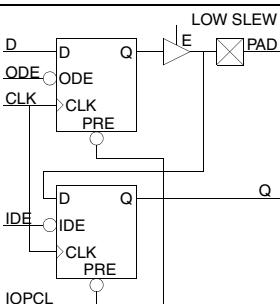
MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD <sub>n-1</sub>	Q <sub>n-1</sub>
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q <sub>n-1</sub>

Input		Output	
D, E, ODE, CLK, IOPCL, IDE, PAD	PAD, Q		

Family	Modules	
	Seq	I/O
ACT 3		1

## DEPETL

ACT 3



### Function

Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

### Truth Table

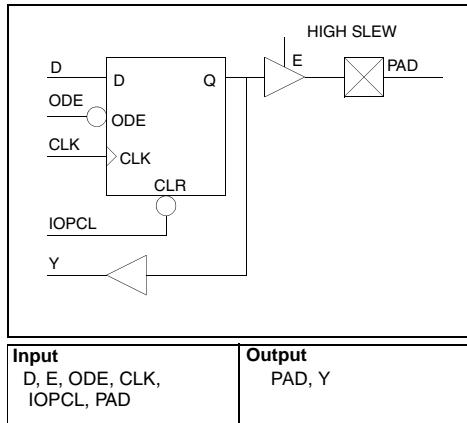
MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	X	PAD <sub>n-1</sub>	Q <sub>n-1</sub>
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD
	0	1	X	1	X	X	Q <sub>n-1</sub>

Input		Output	
D, E, ODE, CLK, IOPCL, IDE, PAD	PAD, Q		

Family	Modules	
	Seq	I/O
ACT 3		1

## FECTH

ACT 3



### Function

Output Register with feedback, Clear, Output Data Enable, Tristate Enable, High Slew

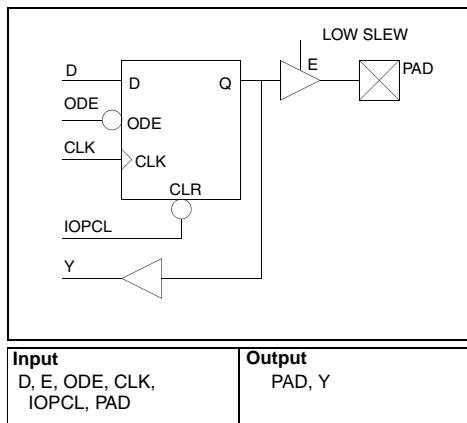
### Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	$Y_{n-1}$	$PAD_{n-1}$
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	$Y_{n-1}$	Z

Family	Modules	
	Seq	I/O
ACT 3		1

## FECTL

ACT 3



### Function

Output Register with feedback, Clear, Output Data Enable, Tristate Enable, Low Slew

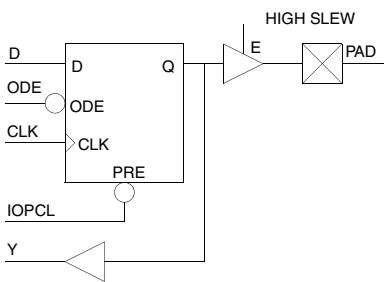
### Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	$Y_{n-1}$	$PAD_{n-1}$
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	$Y_{n-1}$	Z

Family	Modules	
	Seq	I/O
ACT 3		1

## FEPTH

ACT 3



### Function

Output Register with feedback, Preset, Output Data Enable, Tristate Enable, High Slew

### Truth Table

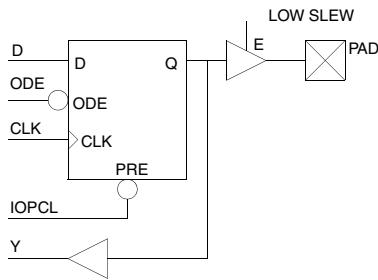
E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	$Y_{n-1}$	$PAD_{n-1}$
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	$Y_{n-1}$	Z

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

## FEPTL

ACT 3



### Function

Output Register with feedback, Preset, Output Data Enable, Tristate Enable, Low Slew

### Truth Table

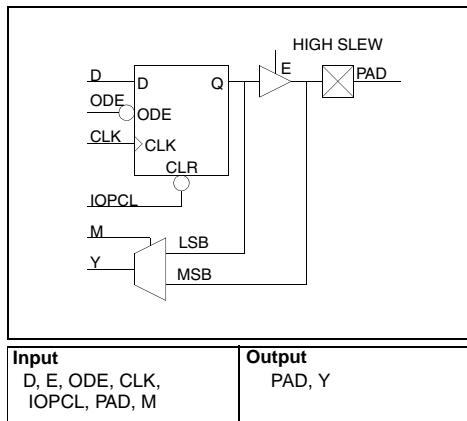
E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	$Y_{n-1}$	$PAD_{n-1}$
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	$Y_{n-1}$	Z

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

## FECTMH

ACT 3



### Function

Output Register with Muxed Feedback, Clear, Output Data Enable, Tristate Enable, High Slew

### Truth Table

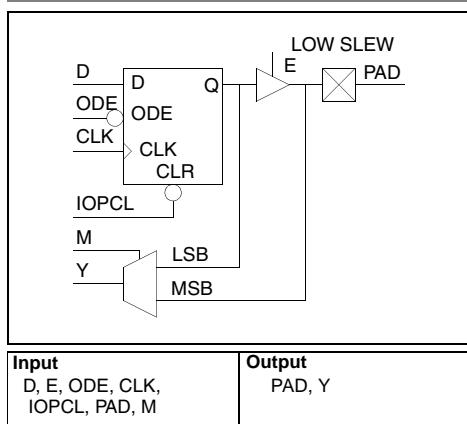
MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	X	PAD <sub>n-1</sub>	X	Y <sub>n-1</sub>
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

## FECTML

ACT 3



### Function

Output Register with Muxed Feedback, Clear, Output Data Enable, Tristate Enable, Low Slew

### Truth Table

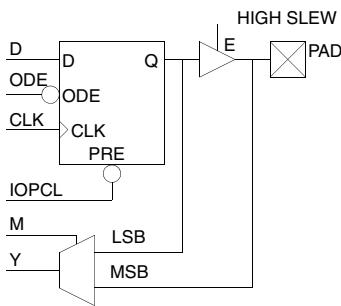
MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	X	PAD <sub>n-1</sub>	X	Y <sub>n-1</sub>
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

## FEPTMH

ACT 3



### Function

Output Register with Muxed Feedback, Preset, Output Data Enable, Tristate Enable, High Slew

### Truth Table 1

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	X	PAD <sub>n-1</sub>	X	Y <sub>n-1</sub>
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

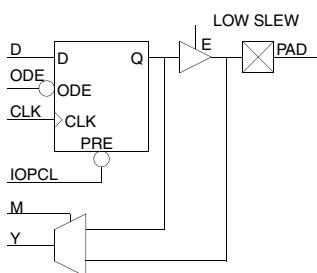
Family	Modules	
	Seq	I/O
ACT 3		1

1.NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

## FEPTML

ACT 3



### Function

Output Register with Muxed Feedback, Preset, Output Data Enable, Tristate Enable, Low Slew

### Truth Table 1

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	X	PAD <sub>n-1</sub>	X	Y <sub>n-1</sub>
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

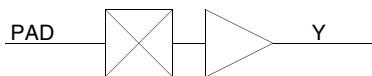
Family	Modules	
	Seq	I/O
ACT 3		1

1.NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

## IBUF

ACT 3



### Function

Input Buffer

### Truth Table

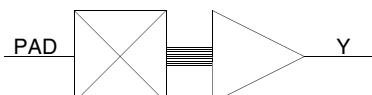
PAD	Y
0	0
1	1

Input PAD	Output Y
--------------	-------------

Family	Modules	
	Seq	I/O
ACT 3		1

## IOCLKBUF

ACT 3



### Function

Dedicated I/O Module Clock Buffer

### Truth Table

PAD	Y
0	0
1	1

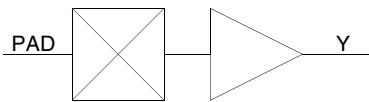
Input PAD	Output Y
--------------	-------------

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: Refer to Actel's Databook for more Clock Network information.

## IOPCLBUF

ACT 3



### Function

Dedicated I/O Preset Clear Buffer

### Truth Table

PAD	Y
0	0
1	1

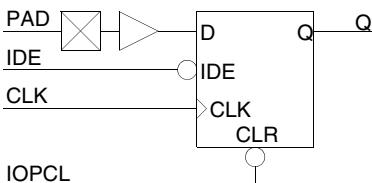
Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: Refer to Actel's Databook for more Clock Network information.

## IREC

ACT 3



### Function

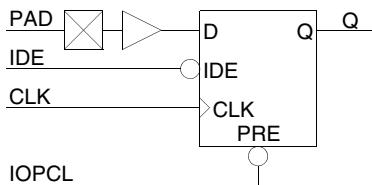
Input Register, with Clear, Input Data Enable

### Truth Table

IOPCL	IDE	CLK	Q <sub>n+1</sub>
0	X	X	0
1	1	X	Q
1	0	↑	PAD

Input	Output
PAD, IDE, CLK, IOPCL	Q

Family	Modules	
	Seq	I/O
ACT 3		1

**Function**

Input Register, with Preset, Input Data Enable

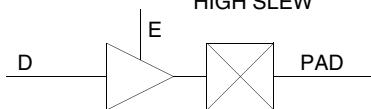
**Truth Table**

IOPCL	IDE	CLK	$Q_{n+1}$
0	X	X	1
1	1	X	Q
1	0	↑	PAD

Input  
PAD, IDE, CLK, IOPCLOutput  
Q

Family	Modules	
	Seq	I/O
ACT 3		1

HIGH SLEW

**Function**

Output Buffer, Tristate Enable, High Slew

**Truth Table**

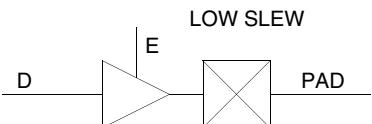
D	E	PAD
X	0	Z
0	1	0
1	1	1

Input  
D, EOutput  
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

## OBUFTL

ACT 3



### Function

Output Buffer, Tristate Enable, Low Slew

### Truth Table

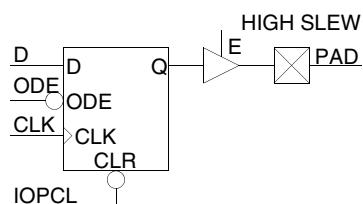
D	E	PAD
X	0	Z
0	1	0
1	1	1

Input	Output
D, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

## ORECTH

ACT 3



### Function

Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

### Truth Table

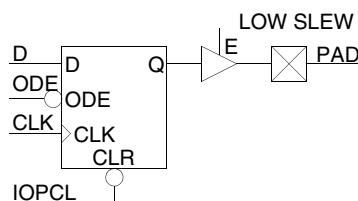
IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

Input	Output
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

## ORECTL

ACT 3



### Function

Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

### Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

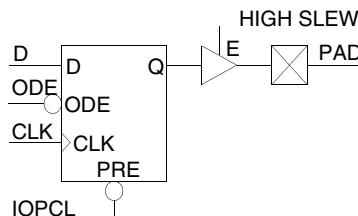
Input  
D, ODE, CLK, IOPCL, E

Output  
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

## OREPTH

ACT 3



### Function

Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

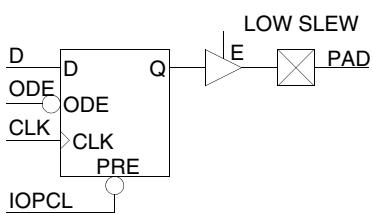
### Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

Input  
D, ODE, CLK, IOPCL, E

Output  
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

**Function**

Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

**Truth Table**

IOPCL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

**Input**  
D, ODE, CLK, IOPCL, E**Output**  
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

## Axcelerator Input IO Macros

Names for the input buffers are composed of up to 4 parts:

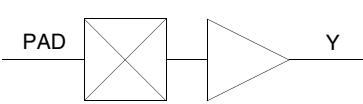
- A base name indicating the type of buffer :INBUF
- IO Technology like LVCMOS
- An optional number code 33,25,18 or 15 indicating a 3.3, 2.5, 1.8 OR 1.5 voltage level.
- An optional one character code (U/D) designating a pull-up/down resistor. When the buffer has no resistor, this code is omitted.

For Example:

- INBUF\_LVCMOS25U - An input LVCMOS buffer with 2.5 CMOS voltage levels, pull-up resistor.
- INBUF\_PCIX - An input PCIX buffer

### INBUF\_X

Axcelerator

		<b>Function</b> Global Input Buffer						
<b>Input</b> PAD		<b>Truth Table</b>						
<b>Output</b> Y		<table border="1"><tr><th>PAD</th><th>Y</th></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table>	PAD	Y	0	0	1	1
PAD	Y							
0	0							
1	1							
<b>Family</b>		<b>Modules</b>						
<table border="1"><thead><tr><th>Family</th><th>Seq</th><th>I/O</th></tr></thead><tbody><tr><td>All listed</td><td></td><td>1</td></tr></tbody></table>		Family	Seq	I/O	All listed		1	
Family	Seq	I/O						
All listed		1						

#### Available INBUF\_X Macro Types

Name	Description
INBUF	LVTTL Input buffer with 3.3v voltage level
INBUF_LVCMOS25	LVCMOS Input buffer with 2.5 CMOS voltage level
INBUF_LVCMOS25U	LVCMOS Input buffer with 2.5 CMOS voltage level, pull-up resistor
INBUF_LVCMOS25D	LVCMOS Input buffer with 2.5 CMOS voltage level, pull-down resistor
INBUF_LVCMOS18	LVCMOS Input buffer with 1.8 CMOS voltage level
INBUF_LVCMOS18U	LVCMOS Input buffer with 1.8 CMOS voltage level, pull-up resistor
INBUF_LVCMOS18D	LVCMOS Input buffer with 1.8 CMOS voltage level, pull-down resistor
INBUF_LVCMOS15	LVCMOS Input buffer with 1.5 CMOS voltage level
INBUF_LVCMOS15U	LVCMOS Input buffer with 1.5 CMOS voltage level, pull-up resistor
INBUF_LVCMOS15D	LVCMOS Input buffer with 1.5 CMOS voltage level, pull-down resistor
INBUF_PCI	PCI Input buffer
INBUF_PCIX	PCIX Input buffer
INBUF_GTLPI25	GTLPI Input buffer with 3.3 CMOS voltage level
INBUF_GTLPI33	GTLPI Input buffer with 2.5 CMOS voltage level
INBUF_HSTL_I	HSTL Class I Input buffer
INBUF_SSTL2_I	SSTL2 Class I Input buffer
INBUF_SSTL2_II	SSTL2 Class II Input buffer
INBUF_SSTL3_I	SSTL3 Class I Input buffer
INBUF_SSTL3_II	SSTL3 Class II Input buffer

---

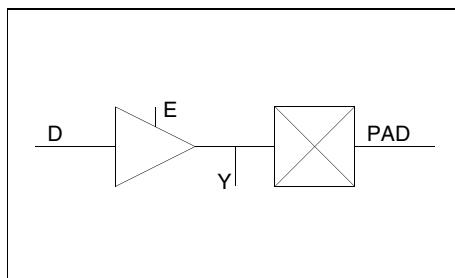
## Bi-Directional IO Macros

Names for the bi-directional buffers are composed of up to 4 parts:

- A base name indicating the type of buffer :BIBUF
- Optional IO Technology like LVCMOS
- An optional number code 8,12,16,24 indicating 1x, 2x, 3x or 4x-drive strength.
- An optional one character code (S/F) indicating high(F) slew or low(S) slew
- An optional one character code (U/D) designating a pull-up/down resistor. When the buffer has no resistor, this code is omitted.

For Example:

- BIBUF\_LVCMOS25 - A bi-directional LVCMOS buffer with 2.5 CMOS voltage levels, pull-up resistor
- BIBUF\_S\_8- A bi-directional buffer with low slew and 1x drive strength



**Input**  
D, E, PAD

**Output**  
Y, PAD

### Function

Bidirectional Buffer, High Slew (with Hidden Buffer at Y pin)

### Truth Table

MODE	E	D	PAD	Y
OUTPUT	1	X	D	D
INPUT	0	X	X	PAD

### Family

Family	Modules	
	Seq	I/O
All		1

### Available BIBUF\_X Macro Types

Name	Description
BIBUF_LVCMOS25	LVCMOS Bi-directional buffer with 2.5 CMOS voltage level
BIBUF_LVCMOS25U	LVCMOS Bi-directional buffer with 2.5 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS25D	LVCMOS Bi-directional buffer with 2.5 CMOS voltage level, pull-down resistor
BIBUF_LVCMOS18	LVCMOS Bi-directional buffer with 1.8 CMOS voltage level
BIBUF_LVCMOS18U	LVCMOS Bi-directional buffer with 1.8 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS18D	LVCMOS Bi-directional buffer with 1.8 CMOS voltage level, pull-down resistor
BIBUF_LVCMOS15	LVCMOS Bi-directional buffer with 1.5 CMOS voltage level
BIBUF_LVCMOS15U	LVCMOS Bi-directional buffer with 1.5 CMOS voltage level, pull-up resistor
BIBUF_LVCMOS15D	LVCMOS Bi-directional buffer with 1.5 CMOS voltage level, pull-down resistor
BIBUF_PCI	PCI Bi-directional buffer
BIBUF_PCIX	PCIX Bi-directional buffer
BIBUF_GTLPI25	GTLPI Bi-directional buffer with 2.5 CMOS voltage level
BIBUF_GTLPI33	GTLPI Bi-directional buffer with 3.3 CMOS voltage level
BIBUF_F_8	Bi-directional buffer with high slew and 1x drive strength
BIBUF_F_8U	Bi-directional buffer with high slew and 1x drive strength, pull-up resistor
BIBUF_F_8U	Bi-directional buffer with high slew and 1x drive strength, pull-down resistor
BIBUF_F_12	Bi-directional buffer with high slew and 2x drive strength
BIBUF_F_12U	Bi-directional buffer with high slew and 2x drive strength, pull-up resistor
BIBUF_F_12D	Bi-directional buffer with high slew and 2x drive strength, pull-down resistor
BIBUF_F_16	Bi-directional buffer with high slew and 3x drive strength
BIBUF_F_16U	Bi-directional buffer with high slew and 3x drive strength, pull-up resistor
BIBUF_F_16D	Bi-directional buffer with high slew and 3x drive strength, pull-down resistor
BIBUF_F_24	Bi-directional buffer with high slew and 4x drive strength
BIBUF_F_24U	Bi-directional buffer with high slew and 4x drive strength, pull-up resistor
BIBUF_F_24D	Bi-directional buffer with high slew and 4x drive strength, pull-down resistor
BIBUF_S_8	Bi-directional buffer with low slew and 1x drive strength
BIBUF_S_8U	Bi-directional buffer with low slew and 1x drive strength, pull-up resistor
BIBUF_S_8U	Bi-directional buffer with low slew and 1x drive strength, pull-down resistor
BIBUF_S_12	Bi-directional buffer with low slew and 2x drive strength
BIBUF_S_12U	Bi-directional buffer with low slew and 2x drive strength, pull-up resistor
BIBUF_S_12D	Bi-directional buffer with low slew and 2x drive strength, pull-down resistor
BIBUF_S_16	Bi-directional buffer with low slew and 3x drive strength
BIBUF_S_16U	Bi-directional buffer with low slew and 3x drive strength, pull-up resistor
BIBUF_S_16D	Bi-directional buffer with low slew and 3x drive strength, pull-down resistor
BIBUF_S_24	Bi-directional buffer with low slew and 4x drive strength
BIBUF_S_24U	Bi-directional buffer with low slew and 4x drive strength, pull-up resistor
BIBUF_S_24D	Bi-directional buffer with low slew and 4x drive strength, pull-down resistor

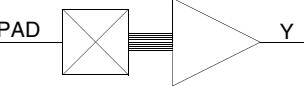
---

Name	Description
BIBUF_SSTL2_I	SSTL2 Class I Bi-directional buffer with 2.5V CMOS Voltage Level
BIBUF_SSTL2_II	SSTL2 Class II Bi-directional buffer with 2.5V CMOS Voltage Level
BIBUF_SSTL3_I	SSTL3 Class I Bi-directional buffer with 3.3V CMOS Voltage Level
BIBUF_SSTL3_II	SSTL3 Class II Bi-directional buffer with 3.3V CMOS Voltage Level
BIBUF_HSTL_I	HSTL Class I Bi-directional buffer with 1.5V CMOS Voltage Level

## Clock Buffers

Names for the input buffers are composed of up to 3 parts:

- A base name indicating the type of buffer :CLKBUF
- IO Technology like LVCMSOS
- An optional number code 33,25,18 or 15 indicating a 3.3,2.5, 1.8 OR 1.5 voltage level

CLKBUF_X		Axcelerator								
	<p><b>Function</b> Input for Dedicated Routed Clock Network</p>									
<b>Input</b> PAD		<p><b>Truth Table</b></p> <table border="1"><thead><tr><th>PAD</th><th>Y</th></tr></thead><tbody><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></tbody></table>	PAD	Y	0	0	1	1		
PAD	Y									
0	0									
1	1									
<b>Output</b> Y		<p><b>Family</b></p> <table border="1"><thead><tr><th rowspan="2">Family</th><th colspan="2">Modules</th></tr><tr><th>Seq</th><th>I/O</th></tr></thead><tbody><tr><td>All</td><td></td><td>1</td></tr></tbody></table>	Family	Modules		Seq	I/O	All		1
Family	Modules									
	Seq	I/O								
All		1								

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

### Available CLKBUF\_X Macro Types

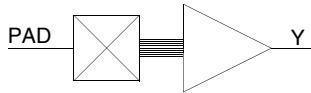
Name	Description
CLKBUF_LVCMOS25	LVCMOS Clock buffer with 2.5 CMOS voltage level
CLKBUF_LVCMOS18	LVCMOS Clock buffer with 1.8 CMOS voltage level
CLKBUF_LVCMOS15	LVCMOS Clock buffer with 1.5 CMOS voltage level
CLKBUF_PCI	PCI Clock buffer
CLKBUF_PCIX	PCIX Clock buffer
CLKBUF_GTLPI25	GTLPI Clock buffer with 2.5 CMOS voltage level
CLKBUF_GTLPI33	GTLPI Clock buffer with 3.3 CMOS voltage level
CLKBUF_HSTL_I	HSTL Class I Clock buffer
CLKBUF_SSTL2_I	SSTL2 Class I Clock buffer
CLKBUF_SSTL2_II	SSTL2 Class II Clock buffer
CLKBUF_SSTL3_I	SSTL3 Class I Clock buffer
CLKBUF_SSTL3_II	SSTL3 Class II Clock buffer

## HClock Buffers

Naming convention is identical to the naming for Clock Buffers.

### HCLKBUF\_X

Axcelerator



#### Function

Dedicated high-speed S-Module Clock Buffer

#### Truth Table

PAD	Y
0	0
1	1

**Input**  
PAD

**Output**  
Y

#### Family

Family	Modules	
	Seq	I/O
All		1

NOTE 1: Refer to Actel's Databook for more Clock Network information.

#### Available HCLKBUF\_X Macro Types

Name	Description
HCLKBUF_LVCMOS25	LVCmos Clock buffer with 2.5 CMOS voltage level
HCLKBUF_LVCMOS18	LVCmos Clock buffer with 1.8 CMOS voltage level
HCLKBUF_LVCMOS15	LVCmos Clock buffer with 1.5 CMOS voltage level
HCLKBUF_PCI	PCI Clock buffer
HCLKBUF_PCIX	PCIX Clock buffer
HCLKBUF_GTLPI25	GTLPI Clock buffer with 2.5 CMOS voltage level
HCLKBUF_GTLPI33	GTLPI Clock buffer with 3.3 CMOS voltage level
HCLKBUF_HSTL_I	HSTL Class I Clock buffer
HCLKBUF_SSTL2_I	SSTL2 Class I Clock buffer
HCLKBUF_SSTL2_II	SSTL2 Class II Clock buffer
HCLKBUF_SSTL3_I	SSTL3 Class I Clock buffer
HCLKBUF_SSTL3_II	SSTL3 Class II Clock buffer

## Output Buffers

Names for the bi-directional buffers are composed of up to 4 parts:

- A base name indicating the type of buffer :OUTBUF
- Optional IO Technology like LVCMOS
- An optional number code 8,12,16,24 indicating 1x, 2x, 3x or 4x-drive strength.
- An optional one character code (S/F) indicating high(F) slew or low(S) slew

OUTBUF_X		Axcelerator								
		<b>Function</b> Output Buffer, High Slew								
<b>Truth Table</b>		<table border="1"><thead><tr><th>D</th><th>PAD</th></tr></thead><tbody><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></tbody></table>	D	PAD	0	0	1	1		
D	PAD									
0	0									
1	1									
<b>Family</b>										
<table border="1"><thead><tr><th rowspan="2">Family</th><th colspan="2">Modules</th></tr><tr><th>Seq</th><th>I/O</th></tr></thead><tbody><tr><td>All</td><td></td><td>1</td></tr></tbody></table>		Family	Modules		Seq	I/O	All		1	
Family	Modules									
	Seq	I/O								
All		1								

### Available OUTBUF\_X Macro Types

Name	Description
OUTBUF_LVCMOS25	LVCMOS Output buffer with 2.5 CMOS voltage level
OUTBUF_LVCMOS18	LVCMOS Output buffer with 1.8 CMOS voltage level
OUTBUF_LVCMOS15	LVCMOS Output buffer with 1.5 CMOS voltage level
OUTBUF_PCI	PCI Output buffer
OUTBUF_PCIX	PCIX Output buffer
OUTBUF_GTLPI25	GTLPI Output buffer with 2.5 CMOS voltage level
OUTBUF_GTLPI33	GTLPI Output buffer with 3.3 CMOS voltage level
OUTBUF_F_8	Output buffer with high slew and 1x drive strength
OUTBUF_F_12	Output buffer with high slew and 2x drive strength
OUTBUF_F_16	Output buffer with high slew and 3x drive strength
OUTBUF_F_24	Output buffer with high slew and 4x drive strength
OUTBUF_S_8	Output buffer with low slew and 1x drive strength
OUTBUF_S_12	Output buffer with low slew and 2x drive strength
OUTBUF_S_16	Output buffer with low slew and 3x drive strength
OUTBUF_S_24	Output buffer with low slew and 4x drive strength
OUTBUF_SSTL2_I	SSTL Class I Output buffer with 2.5V CMOS Voltage Level
OUTBUF_SSTL2_II	SSTL Class II Output buffer with 2.5V CMOS Voltage
OUTBUF_SSTL3_I	SSTL Class I Output buffer with 3.3V CMOS Voltage Level
OUTBUF_SSTL3_II	SSTL Class II Output buffer with 3.3V CMOS Voltage Level
OUTBUF_HSTL_I	HSTL Class I Output buffer with 1.5V CMOS Voltage Level

## Tri-State Buffer Macros

Names for the bi-directional buffers are composed of up to 4 parts:

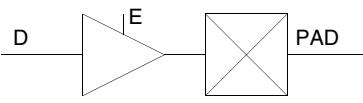
- A base name indicating the type of buffer :TRIBUFF
- Optional IO Technology like LVCMOS
- An optional number code 8,12,16,24 indicating 1x, 2x, 3x or 4x-drive strength.
- An optional one character code (S/F) indicating high(F) slew or low(S) slew
- An optional one character code (U/D) designating a pull-up/down resistor. When the buffer has no resistor, this code is omitted.

For Example:

- TRIBUFF\_LVCMOS25 - A bi-directional LVCMOS buffer with 2.5 CMOS voltage levels, pull-up resistor
- TRIBUFF\_S\_8- A bi-directional buffer with low slew and 1x drive strength

### TRIBUFF\_X

Axcelerator

	<b>Function</b> Tristate Output, High Slew								
<b>Truth Table</b>									
<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>E</th><th>PAD</th></tr> </thead> <tbody> <tr> <td>0</td><td>Z</td></tr> <tr> <td>1</td><td>D</td></tr> </tbody> </table>	E	PAD	0	Z	1	D			
E	PAD								
0	Z								
1	D								
<b>Family</b>									
<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">Family</th><th colspan="2">Modules</th></tr> <tr> <th>Seq</th><th>I/O</th></tr> </thead> <tbody> <tr> <td>All</td><td></td><td>1</td></tr> </tbody> </table>	Family	Modules		Seq	I/O	All		1	
Family		Modules							
	Seq	I/O							
All		1							
<b>Input</b> D, E	<b>Output</b> PAD								

### Available TRIBUFF\_X Macro Types

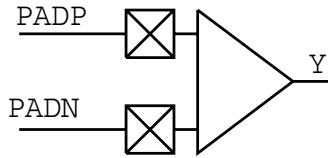
Name	Description
TRIBUFF_LVCMOS25	LVCMOS Tri-state buffer with 2.5 CMOS voltage level
TRIBUFF_LVCMOS25U	LVCMOS Tri-state buffer with 2.5 CMOS voltage level, pull-up resistor
TRIBUFF_LVCMOS25D	LVCMOS Tri-state buffer with 2.5 CMOS voltage level, pull-down resistor
TRIBUFF_LVCMOS18	LVCMOS Tri-state buffer with 1.8 CMOS voltage level
TRIBUFF_LVCMOS18U	LVCMOS Tri-state buffer with 1.8 CMOS voltage level, pull-up resistor
TRIBUFF_LVCMOS18D	LVCMOS Tri-state buffer with 1.8 CMOS voltage level, pull-down resistor
TRIBUFF_LVCMOS15	LVCMOS Tri-state buffer with 1.5 CMOS voltage level
TRIBUFF_LVCMOS15U	LVCMOS Tri-state buffer with 1.5 CMOS voltage level, pull-up resistor
TRIBUFF_LVCMOS15D	LVCMOS Tri-state buffer with 1.5 CMOS voltage level, pull-down resistor
TRIBUFF_PCI	PCI Tri-state buffer
TRIBUFF_PCIX	PCIX Tri-state buffer
TRIBUFF_GTLP25	GTLP Tri-state buffer with 2.5 CMOS voltage level
TRIBUFF_GTLP33	GTLP Tri-state buffer with 3.3 CMOS voltage level
TRIBUFF_F_8	Tri-state buffer with high slew and 8 mA drive strength
TRIBUFF_F_8U	Tri-state buffer with high slew and 1x drive strength, pull-up resistor
TRIBUFF_F_8U	Tri-state buffer with high slew and 1x drive strength, pull-down resistor
TRIBUFF_F_12	Tri-state buffer with high slew and 2x drive strength
TRIBUFF_F_12U	Tri-state buffer with high slew and 2x drive strength, pull-up resistor
TRIBUFF_F_12D	Tri-state buffer with high slew and 2x drive strength, pull-down resistor
TRIBUFF_F_16	Tri-state buffer with high slew and 3x drive strength
TRIBUFF_F_16U	Tri-state buffer with high slew and 3x drive strength, pull-up resistor
TRIBUFF_F_16D	Tri-state buffer with high slew and 3x drive strength, pull-down resistor
TRIBUFF_F_24	Tri-state buffer with high slew and 4x drive strength
TRIBUFF_F_24U	Tri-state buffer with high slew and 4x drive strength, pull-up resistor

Name	Description
TRIBUFF_F_24D	Tri-state buffer with high slew and 4x drive strength, pull-down resistor
TRIBUFF_S_8	Tri-state buffer with low slew and 1x drive strength
TRIBUFF_S_8U	Tri-state buffer with low slew and 1x drive strength, pull-up resistor
TRIBUFF_S_8U	Tri-state buffer with low slew and 1x drive strength, pull-down resistor
TRIBUFF_S_12	Tri-state buffer with low slew and 2x drive strength
TRIBUFF_S_12U	Tri-state buffer with low slew and 2x drive strength, pull-up resistor
TRIBUFF_S_12D	Tri-state buffer with low slew and 2x drive strength, pull-down resistor
TRIBUFF_S_16	Tri-state buffer with low slew and 3x drive strength
TRIBUFF_S_16U	Tri-state buffer with low slew and 3x drive strength, pull-up resistor
TRIBUFF_S_16D	Tri-state buffer with low slew and 3x drive strength, pull-down resistor
TRIBUFF_S_24	Tri-state buffer with low slew and 4x drive strength
TRIBUFF_S_24U	Tri-state buffer with low slew and 4x drive strength, pull-up resistor
TRIBUFF_S_24D	Tri-state buffer with low slew and 4x drive strength, pull-down resistor
TRIBUFF_SSTL2_I	SSTL2 Class I Tri-state buffer with 2.5V CMOS Voltage Level
TRIBUFF_SSTL2_II	SSTL2 Class II Tri-state buffer with 2.5V CMOS Voltage Level
TRIBUFF_SSTL3_I	SSTL3 Class I Tri-state buffer with 3.3V CMOS Voltage Level
TRIBUFF_SSTL3_II	SSTL3 Class II Tri-state buffer with 3.3V CMOS Voltage Level
TRIBUFF_HSTL_I	HSTL Class I Tri-state buffer with 1.5V CMOS Voltage Level

## Differential I/O Macros

### INBUF\_LVDS; INBUF\_LVPECL

Axcelerator



#### Function

INBUF\_LVDS and INBUF\_LVPECL

**Input**  
PADP; PADN

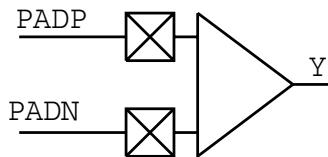
**Output**  
Y

#### Available Differential Macro Types

Name	Description
INBUF_LVDS	
INBUF_LVPECL	

### CLKBUF\_LVDS; CLKBUF\_LVPECL

Axcelerator



#### Function

CLKBUF\_LVDS and CLKBUF\_LVPECL

**Input**  
PADP; PADN

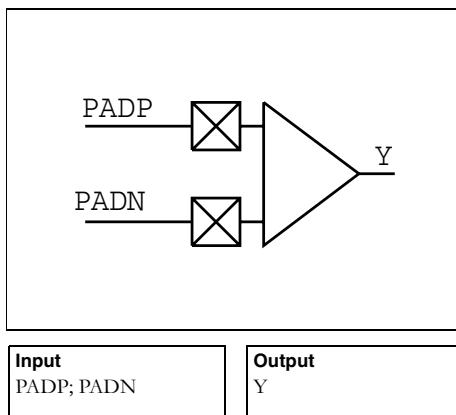
**Output**  
Y

#### Available Differential Macro Types

Name	Description
CLKBUF_LVDS	
CLKBUF_LVPECL	

## HCLKBUF\_LVDS; HCLKBUF\_LVPECL

Accelerator



### Function

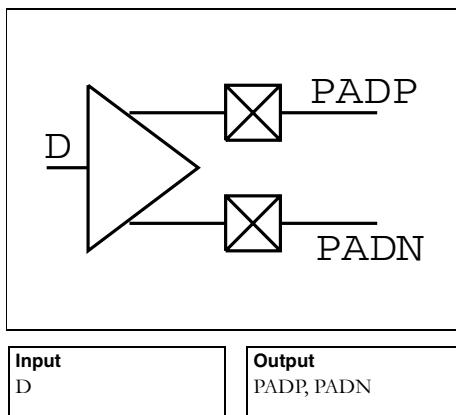
HCLKBUF\_LVDS and HCLKBUF\_LVPECL

### Available Differential Macro Types

Name	Description
HCLKBUF_LVDS	
HCLKBUF_LVPECL	

## OUTBUF\_LVDS; OUTBUF\_LVPECL

Accelerator



### Function

OUTBUF\_LVDS and OUTBUF\_LVPECL

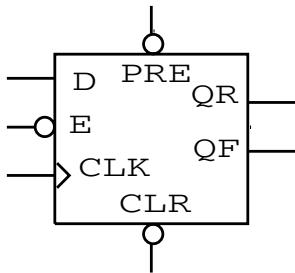
### Available Differential Macro Types

Name	Description
OUTBUF_LVDS	
OUTBUF_LVPECL	

## DDR Macro

### DDR\_REG macro

Axcelerator



#### Function

DDR (DDR) Register with activelow write and rad enables; please refer to the Axcelerator datasheet for more information on the DDR\_REG

#### Truth Table

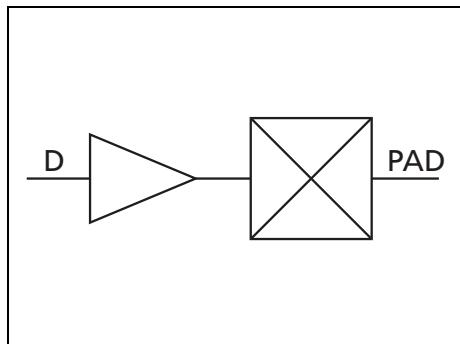
CLR	PRE	E	CLK	QR(n+1)	QF(n+1)
0	X	X	X	0	0
1	0	X	X	1	1
1	1	1	X	QR(n)	QF(n)
1	1	0	↑	D(↑)	X
1	1	0	↓	X	D(↓)

#### Input

D, CLK, E, PRE, CLR

#### Output

QR, QF

**Function**

SIMBUF is a VIRTUAL I/O used to bring out internal nets that are going to be connected to a top port in the design. This port will be used exclusively for simulation. This virtual I/O is removed by Designer during compile, then re-added in the back-annotated netlist.

**Truth Table**

D	PAD
0	0
1	1

Family	I/O Tiles
All listed	0

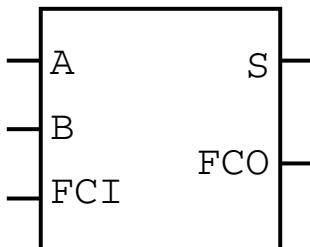


---

## *Carry Chain Macros*

## ADD1

Axcelerator



Input	Output
A, B, FCI	S, FCO

### Function

1 Bit Adder

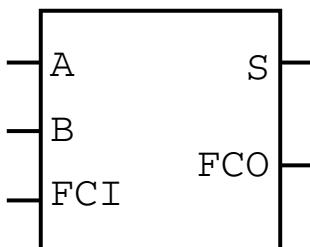
### Truth Table

A	B	FCI	S	FCO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Family	Modules
	COMB
All listed	1

## SUB1

Axcelerator



Input	Output
A, B, FCI	S, FCO

### Function

1 Bit Subtractor

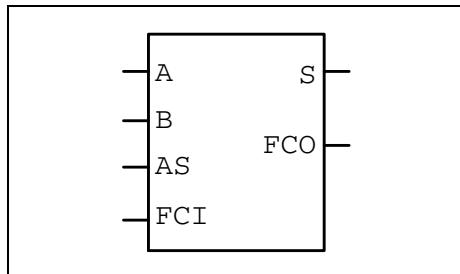
### Truth Table

A	B	FCI	S	FCO
0	0	0	1	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

Family	Modules
	Comb
All listed	1

# ADDSUB1

Axcelerator



**Input**  
AS, B, A, FCI

**Output**  
S, FCO

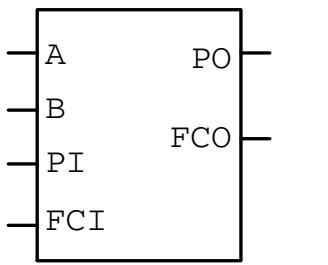
**Function**  
1 Bit Add Sub macro

**Truth Table**

AS	B	A	FCI	S	FCO
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	1

**Family**

Family	Modules
	Comb
All listed	2



**Input**  
A, B, PI, FCI

**Output**  
PO, FCO

**Function**  
1 Bit Multiplier

**Truth Table**

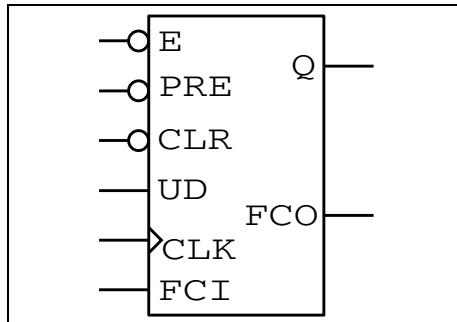
A	B	PI	FCI	PO	FCO
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1
1	1	1	1	1	1

**Family**

Family	Modules
	Comb
All listed	1

## ARCNTECP1

Axcelerator



### Function

1 Bit counter

### Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	$Q_{n+1}$
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	$Q_n$
See Equations	1	1	0	↑	See Equations		

**Input**  
FCI, CLK, PRE, CLR,  
UD

**Output**  
Q, FCO

$$Q_{n+1} = FCI \wedge UD \wedge Q_n$$

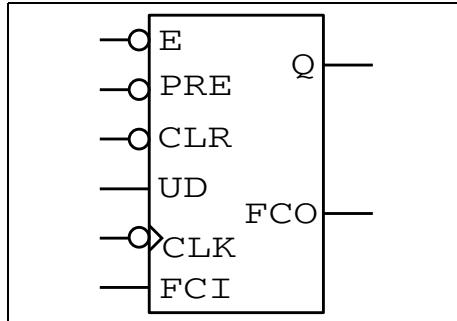
$$FCO = FCI \cdot UD + FCI \cdot Q_n + UD \cdot Q_n$$

### Family

Family	Modules	
	Comb	Seq
All listed	1	1

## AFCNTECP1

Axcelerator



### Function

1 Bit counter

### Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	$Q_{n+1}$
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	$Q_n$
See Equations	1	1	0	↓	See Equations		

**Input**  
FCI, CLK, PRE, CLR,  
UD

**Output**  
Q, FCO

$$Q_{n+1} = FCI \wedge UD \wedge Q_n$$

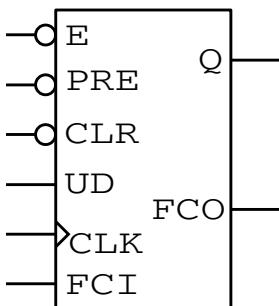
$$FCO = FCI \cdot UD + FCI \cdot Q_n + UD \cdot Q_n$$

### Family

Family	Modules	
	Comb	Seq
All listed	1	1

## SRCNTECP1

Axcelerator



### Function

1 Bit counter

### Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	$Q_{n+1}$
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	$Q_n$
See Equations	1	1	0	↑		See Equations	

$$Q_{n+1} = FCI \wedge !UD \wedge Q_n$$

**Input**  
FCI, CLK, PRE, CLR,  
UD

**Output**  
Q, FCO

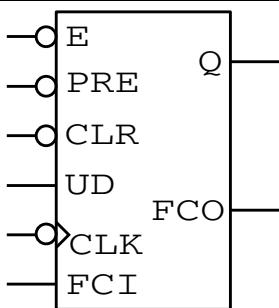
$$FCO = FCI \cdot !UD + FCI \cdot Q_n + !UD \cdot Q_n$$

### Family

Family	Modules	
	Comb	Seq
All listed	1	1

## SFCNTECP1

Axcelerator



### Function

1 Bit counter

### Truth Table

FCI	UD	PRE	CLR	E	CLK	FCO	$Q_{n+1}$
X	X	0	X	X	X	X	1
X	X	1	0	X	X	X	0
X	X	1	1	1	X	X	$Q_n$
See Equations	1	1	0	↓		See Equations	

$$Q_{n+1} = FCI \wedge !UD \wedge Q_n$$

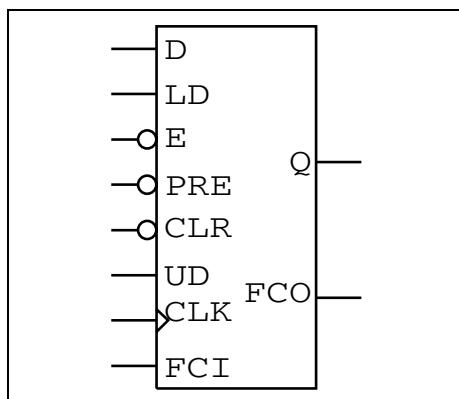
**Input**  
FCI, CLK, PRE, CLR,  
UD

**Output**  
Q, FCO

$$FCO = FCI \cdot !UD + FCI \cdot Q_n + !UD \cdot Q_n$$

### Family

Family	Modules	
	Comb	Seq
All listed	1	1

**Function**

1 Bit counter

**Truth Table**

FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	$Q_{n+1}$
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	$O_n$
X	X	1	1	0	1	0	$\uparrow$	X	0
X	X	1	1	0	1	1	$\uparrow$	X	1
See Equations		1	1	0	0	X	$\uparrow$	See Equations	

$$Q_{n+1} = FCI \wedge UD \wedge Q_n$$

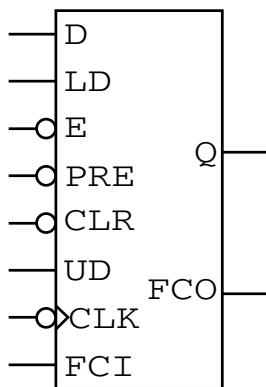
$$FCO = FCI \cdot UD + FCI \cdot Q_n + UD \cdot Q_n$$

**Family**

Family	Modules	
	Comb	Seq
All listed	2	1

## AFCNTELDGP1

Axcelerator



**Function**  
1 Bit counter

**Truth Table**

FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q <sub>n+1</sub>
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	Q <sub>n</sub>
X	X	1	1	0	1	0	↓	X	0
X	X	1	1	0	1	1	↓	X	1
See Equations		1	1	0	0	X	↓	See Equations	

### Input

FCI, CLK, PRE, CLR,  
E, LD, D, and UD

### Output

Q, FCO

$$Q_{n+1} = FCI \wedge UD \wedge Q_n$$

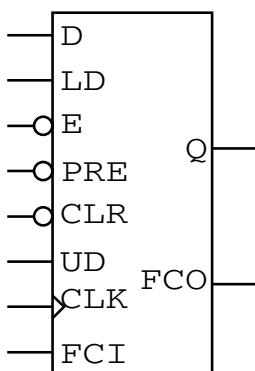
$$FCO = FCI \cdot UD + FCI \cdot Q_n + UD \cdot Q_n$$

### Family

Family	Modules	
	Comb	Seq
All listed	2	1

## SRCNTELDGP1

Axcelerator



**Function**  
1 Bit counter

**Truth Table**

FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q <sub>n+1</sub>
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	Q <sub>n</sub>
X	X	1	1	0	1	0	↑	X	0
X	X	1	1	0	1	1	↑	X	1
See Equations		1	1	0	0	X	↑	See Equations	

### Input

FCI, CLK, PRE, CLR,  
E, LD, D, and UD

### Output

Q, FCO

$$Q_{n+1} = FCI \wedge !UD \wedge Q_n$$

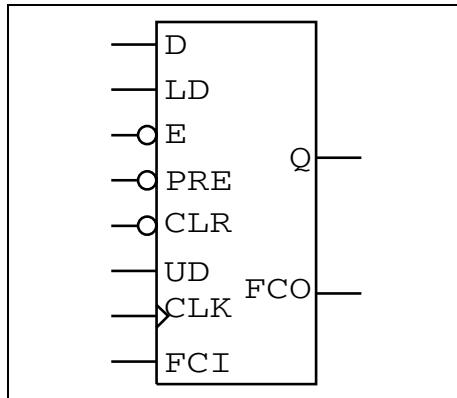
$$FCO = FCI \cdot !UD + FCI \cdot Q_n + !UD \cdot Q_n$$

### Family

Family	Modules	
	Comb	Seq
All listed	2	1

## SFCNTELDPC1

Axcelerator



### Function

1 Bit counter

### Truth Table

FCI	UD	PRE	CLR	E	LD	D	CLK	FCO	Q <sub>n+1</sub>
X	X	0	X	X	X	X	X	X	1
X	X	1	0	X	X	X	X	X	0
X	X	1	1	1	X	X	X	X	Q <sub>n</sub>
X	X	1	1	0	1	0	↓	X	0
X	X	1	1	0	1	1	↓	X	1
See Equations		1	1	0	0	X	↓	See Equations	

$$Q_{n+1} = \text{FCI} \wedge \neg \text{UD} \wedge Q_n$$

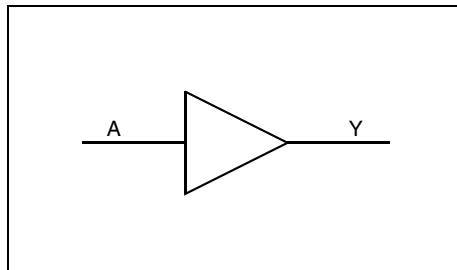
$$\text{FCO} = \text{FCI} \cdot \neg \text{UD} + \text{FCI} \cdot Q_n + \neg \text{UD} \cdot Q_n$$

### Family

Family	Modules	
	Comb	Seq
All listed	2	1

## FCEND\_BUFF

Axcelerator

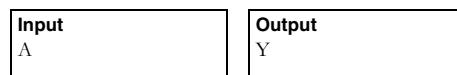


### Function

Buffer, driven by the FCO pin of the last macro in the Carry-Chain

### Truth Table

A	Y
0	0
1	1

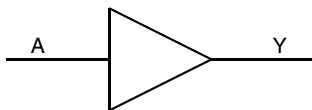


### Family

Family	Modules	
	Seq	COMB
All		1

## FCEND\_INV

Axcelerator



### Function

Inverter with Active Low output; driven by the FCO pin of the last macro in the Carry-Chain

### Truth Table

A	Y
0	1
1	0

### Input

A

### Output

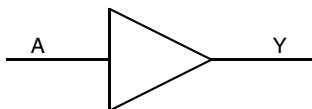
Y

### Family

Family	Modules	
	Seq	COMB
All		1

## FCINIT\_BUFF

Axcelerator



### Function

Buffer, used to initialize the FCI pin of the first macro in the Carry-Chain with an external signal

### Truth Table

A	Y
0	0
1	1

### Input

A

### Output

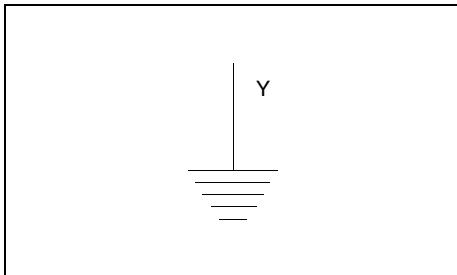
Y

### Family

Family	Modules	
	Seq	COMB
All		1

## FCINIT\_GND

Axcelerator



### Function

Ground; used to initialize the FCI pin of the first macro in the Carry-Chain to GND

NOTE: Ground does not use any modules

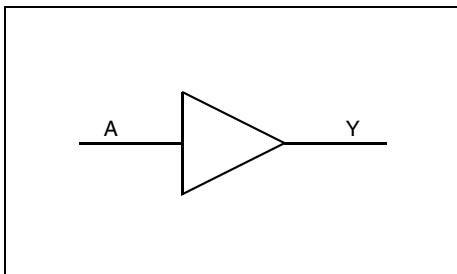
Input

Output

Y

## FCINIT\_INV

Axcelerator



### Function

Inverter with Active Low output; used to initialize the FCI pin of the first macro in the Carry-Chain with an external signal

### Truth Table

A	Y
0	1
1	0

### Family

Family	Modules	
	Seq	COMB
All		1

Input

A

Output

Y



Y

**Function**

Power; used to initialize the FCI pin of the first macro in the Carry-Chain to VCC

NOTE: VCC does not use any modules

**Input**

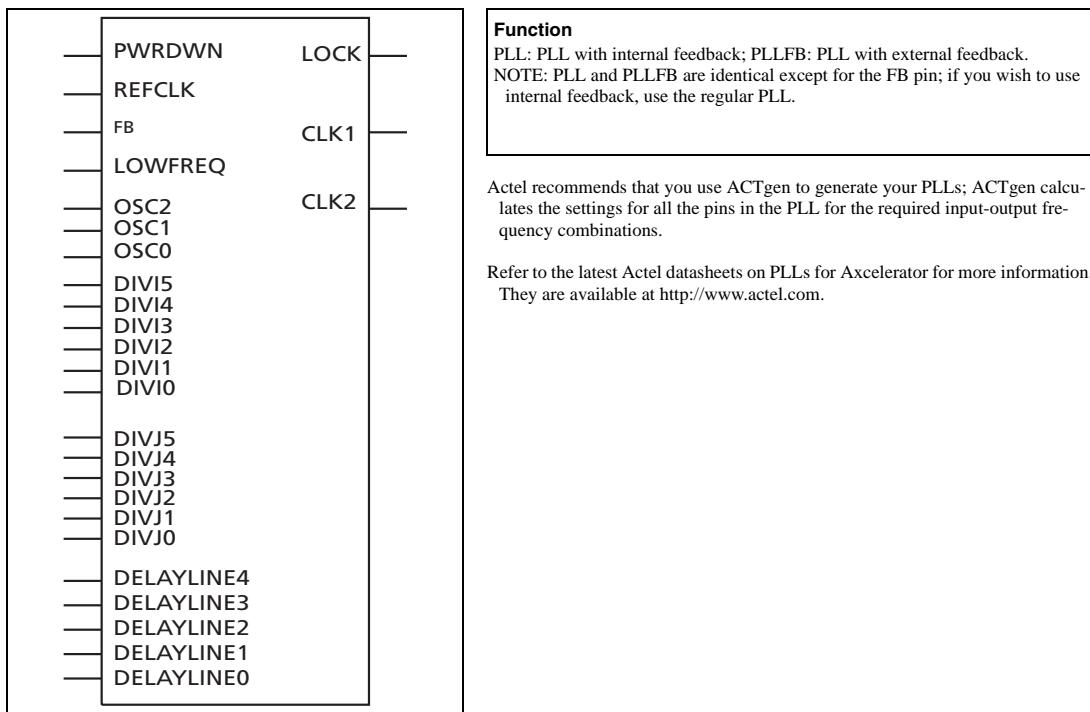
A

**Output**

Y

---

## *PLL Macros*

**Function**

PLL: PLL with internal feedback; PLLFB: PLL with external feedback.  
NOTE: PLL and PLLFB are identical except for the FB pin; if you wish to use internal feedback, use the regular PLL.

Actel recommends that you use ACTgen to generate your PLLs; ACTgen calculates the settings for all the pins in the PLL for the required input-output frequency combinations.

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information.  
They are available at <http://www.actel.com>.

**Input**

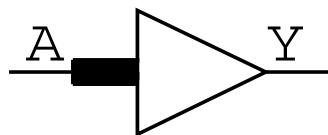
PWRDWN, REFCLK,  
LOWFREQ, OSC2, OSC1,  
OSC0, DIVI5, DIVI4,  
DIVI3, DIVI2, DIVI1,  
DIVI0, DIVJ5, DIVJ4,  
DIVJ3, DIVJ2, DIVJ1,  
DIVJ0, DELAYLINE4,  
DELAYLINE3,  
DELAYLINE2,  
DELAYLINE1,  
DELAYLINE0

**Output**

LOCK, CLK1, CLK2

## PLLINT

Axcelerator



### Function

PLL Int

### Truth Table

A	Y
0	0
1	1

### Input

A

### Output

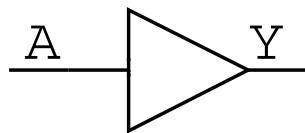
Y

Connect only to the REFCLK input of PLL when the PLL is driven by a pad other than the one in the same super cluster.

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at <http://www.actel.com>.

## PLLOUT

Axcelerator



### Function

PLL OUT

### Truth Table

A	Y
0	0
1	1

### Input

A

### Output

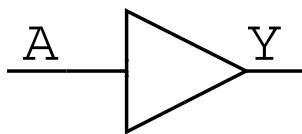
Y

Connect only to the CLK output of PLL when the PLL is driving a net other than the HCLK/RCLK networks.

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at <http://www.actel.com>.

## PLLHCLK

Axcelerator



**Function**  
PLL HCLK

**Truth Table**

A	Y
0	0
1	1

Connect only to the CLK output of the PLL; use it to drive the HCLK network.

**Input**

A

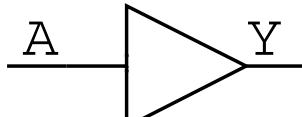
**Output**

Y

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at <http://www.actel.com>.

## PLLRCLK

Axcelerator



**Function**  
PLL RCLK

**Truth Table**

A	Y
0	0
1	1

Connect only to the CLK output of the PLL; use it to drive the RCLK network.

**Input**

A

**Output**

Y

Refer to the latest Actel datasheets on PLLs for Axcelerator for more information. They are available at <http://www.actel.com>.

---

## *RTAX-DSP Math Macro*

CLK[1:0]	P[40:0]
ARSTA[1:0]	CDOUT[40:0]
ARSTB[1:0]	OVFL
ARSTP[1:0]	
SRSTA[1:0]	
SRSTB[1:0]	
SRSTP[1:0]	
EA[1:0]	
EB[1:0]	
EP[1:0]	
ALSHFTSEL	
ALCDSEL	
ALFDBKSEL	
ALSUB	
SLSHFTSEL	
SLCDSEL	
SLFDBKSEL	
SLSUB	
ESHFTSEL	
ECDSEL	
EFDBKSEL	
ESUB	
SHFTSEL	
CDSEL	
FDBKSEL	
SUB	
A[17:0]	
B[17:0]	
CDIN[40:0]	
CIN[40:0]	
ALAT[1:0]	
BLAT[1:0]	
PLAT[1:0]	
SHFTSELLAT	
CDSELLAT	
FDBKSELLAT	
SUBLAT	
SIMD	
SHFTSELAD	
CDSELAD	
FDBKSELSD	
SUBSD	
FDBKSELAD	
SUBAD	
SHFTSELSD	
CDSELSD	

**Function**

18 bit x 18 bit signed (2's complement) multiply-accumulate MATH block

The MATH block can accumulate the current multiplication product with a previous result, a constant, a dynamic value, or a result from another MATH block. Each MATH block can also be fractured into two 9 bit x 9 bit multipliers. All the signals of the MATH block (except CIN, CDIN and CDOUT) have optional registers.

Major signals are in **bold**.

Table 1. Math18x18 Ports

Port Name	Direction	Type	Polarity	Description
SIMD	Input	Static	High	Single Instruction Multiple Data mode. When SIMD = 1, MATH block is fractured into two 9 bit x 9 bit multipliers When SIMD = 0, it is called the normal mode
CLK[1:0]	Input	Dynamic	Rising edge	Input clocks. • CLK[1] is the clock for A[17:9], B[17:9], P[40:18], OVFL, SHFTSEL, CDSEL, FDBKSEL and SUB registers • CLK[0] is the clock for A[8:0], B[8:0] and P[17:0] In normal mode, ensure CLK[1] = CLK[0]
A[17:0]	Input	Dynamic	High	Input data A
ALAT[1:0]	Input	Static	High	Bypass data A registers • ALAT[1] is for A[17:9]. Connect to 1, if not registered • ALAT[0] is for A[8:0]. Connect to 1, if not registered In normal mode, ensure ALAT[0] = ALAT[1]
ARSTA[1:0]	Input	Dynamic	Low	Asynchronous reset for data A registers. • ARSTA[1] is for A[17:9]. Connect to 1, if not registered • ARSTA[0] is for A[8:0]. Connect to 1, if not registered In normal mode, ensure ARSTA[1] = ARSTA[0]
SRSTA[1:0]	Input	Dynamic	Low	Synchronous reset for data A registers • SRSTA[1] is for A[17:9]. Connect to 1, if not registered • SRSTA[0] is for A[8:0]. Connect to 1, if not registered In normal mode, ensure SRSTA[1] = SRSTA[0]
EA[1:0]	Input	Dynamic	High	Enable for data A registers • EA[1] is for A[17:9]. Connect to 1, if not registered • EA[0] is for A[8:0]. Connect to 1, if not registered In normal mode, ensure EA[1] = EA[0]
B[17:0]	Input	Dynamic	High	Input data B
BLAT[1:0]	Input	Static	High	Bypass data B registers. • BLAT[1] is for B[17:9]. Connect to 1, if not registered. • BLAT[0] is for B[8:0]. Connect to 1, if not registered. In normal mode, ensure BLAT[0] = BLAT[1].
ARSTB[1:0]	Input	Dynamic	Low	Asynchronous reset for data B registers. • ARSTB[1] is for B[17:9]. Connect to 1, if not registered. • ARSTB[0] is for B[8:0]. Connect to 1, if not registered. In normal mode, ensure ARSTB[1] = ARSTB[0].
SRSTB[1:0]	Input	Dynamic	Low	Synchronous reset for data B registers. • SRSTB[1] is for B[17:9]. Connect to 1, if not registered. • SRSTB[0] is for B[8:0]. Connect to 1, if not registered. In normal mode, ensure SRSTB[1] = SRSTB[0].
EB[1:0]	Input	Dynamic	High	Enable for data B registers. • EB[1] is for B[17:9]. Connect to 1, if not registered. • EB[0] is for B[8:0]. Connect to 1, if not registered. In normal mode, ensure EB[1] = EB[0].

Table 1. Math18x18 Ports (Continued)

Port Name	Direction	Type	Polarity	Description
P[40:0]	Output		High	<p>Result data.</p> <ul style="list-style-type: none"> <li>Normal mode  <math>P = C + (A \times B)</math>, when SUB = 0  <math>P = C - (A \times B)</math>, when SUB = 1           </li> <li>SIMD mode  <math>P_L = A_L \times B_L</math>  <math>P_H = C_H + (A_H \times B_H)</math>, when SUB = 0  <math>P_H = C_H - (A_H \times B_H)</math>, when SUB = 1           </li> </ul> <p><i>Notation:</i></p> $A_L = A[8:0], A_H = A[17:9]$ $B_L = B[8:0], B_H = B[17:9]$ $P_L = P[17:0], P_H = P[40:18]$ $C_H = C[40:18].$ <p>See Table 4 on page 324 to see how operand C is obtained from CIN, P or CDIN.</p>
OVFL	Output		High	<p>Overflow.</p> <ul style="list-style-type: none"> <li>Normal mode            if <math>C +/- (A \times B) &gt; (2^{40}) - 1</math>, then OVFL = 1            if <math>C +/- (A \times B) &lt; -(2^{40})</math>, then OVFL = 1            otherwise, OVFL = 0         </li> <li>SIMD mode            if <math>C_H +/- (A_H \times B_H) &gt; (2^{22}) - 1</math>, then OVFL = 1            if <math>C_H +/- (A_H \times B_H) &lt; -(2^{22})</math>, then OVFL = 1            otherwise, OVFL = 0         </li> </ul>
PLAT[1:0]	Input	Static	High	<p>Bypass result P registers.</p> <ul style="list-style-type: none"> <li>PLAT[1] is for P[40:18] and OVFL. Connect to 1, if not registered</li> <li>PLAT[0] is for P[17:0]. Connect to 1, if not registered</li> </ul> <p>In normal mode, ensure PLAT[0] = PLAT[1].</p>
ARSTP[1:0]	Input	Dynamic	Low	<p>Asynchronous reset for result P registers.</p> <ul style="list-style-type: none"> <li>ARSTP[1] is for P[40:18] and OVFL. Connect to 1, if not registered.</li> <li>ARSTP[0] is for P[17:0]. Connect to 1, if not registered</li> </ul> <p>In normal mode, ensure ARSTP[1] = ARSTP[0].</p>
SRSTP[1:0]	Input	Dynamic	Low	<p>Synchronous reset for result P registers.</p> <ul style="list-style-type: none"> <li>SRSTP[1] is for P[40:18] and OVFL. Connect to 1, if not registered.</li> <li>SRSTP[0] is for P[17:0]. Connect to 1, if not registered.</li> </ul> <p>In normal mode, ensure SRSTP[1] = SRSTP[0].</p>
EP[1:0]	Input	Dynamic	High	<p>Enable for result P registers.</p> <ul style="list-style-type: none"> <li>EP[1] is for P[40:18] and OVFL. Connect to 1, if not registered.</li> <li>EP[0] is for P[17:0]. Connect to 1, if not registered.</li> </ul> <p>In normal mode, ensure EP[1] = EP[0].</p>
CDOU[40:0]	Output	Cascade	High	<p>Cascade output of result P.</p> <p>CDOU is the same as P. The entire bus must either be dangling or drive an entire CDIN of another MATH block in cascaded mode.</p>
CIN[40:0]	Input	Dynamic	High	<p>Routed input for operand C.</p> <p>In SIMD mode, connect CIN[17:0] to 0.</p> <p>See Table 4 on page 324 to see how CIN is propagated to operand C.</p>
CDIN[40:0]	Input	Cascade	High	<p>Cascaded input for operand C.</p> <p>The entire bus must be driven by an entire CDOU of another MATH block.</p> <p>See Table 4 on page 324 to see how CDIN is propagated to operand C.</p>
SHFTSEL	Input	Dynamic	High	<p>Arithmetic right-shift for operand C.</p> <p>When asserted, a 17-bit arithmetic right-shift is performed on operand C going into the accumulator.</p> <p>In SIMD mode, SHFTSEL is ignored.</p> <p>See Table 4 on page 324 to see how operand C is obtained from CIN, P or CDIN.</p>

Table 1. Math18x18 Ports (Continued)

Port Name	Direction	Type	Polarity	Description
SHFTSELLAT	Input	Static	High	Bypass SHFTSEL register. Connect to 1, if not registered.
ALSHFTSEL	Input	Dynamic	Low	Asynchronous load for SHFTSEL register. Connect to 1, if not registered. When asserted, SHFTSEL register is loaded with SHFTSELAD.
SHFTSELAD	Input	Static	High	Asynchronous load data for SHFTSEL register.
SLSHFTSEL	Input	Dynamic	Low	Synchronous load for SHFTSEL register. Connect to 1, if not registered. See Table 2 on page 324
SHFTSELSD	Input	Static	Low	Synchronous load data for SHFTSEL register. See Table 2 on page 324
ESHFTSEL	Input	Dynamic	High	Enable for SHFTSEL register. Connect to 1, if not registered. See Table 2 on page 324
<hr/>				
CDSEL	Input	Dynamic	High	Select CDIN for operand C. When CDSEL = 1, propagate CDIN. When CDSEL = 0, propagate CIN or P depending on FDBKSEL. In SIMD mode, CDSEL is ignored for CDIN[17:0] and only CDIN[40:18] is propagated. See Table 4 on page 324 to see how operand C is obtained from CIN, P or CDIN.
CDSELLAT	Input	Static	High	Bypass CDSEL register. Connect to 1, if not registered.
ALCDSEL	Input	Dynamic	Low	Asynchronous load for CDSEL register. Connect to 1, if not registered. When asserted, CDSEL register is loaded with CDSELAD.
CDSELAD	Input	Static	High	Asynchronous load data for CDSEL register.
SLCDSEL	Input	Dynamic	Low	Synchronous load for CDSEL register. Connect to 1, if not registered. See Table 2 on page 324.
CDSELSD	Input	Static	Low	Synchronous load data for CDSEL register. See Table 2 on page 324.
ECDSEL	Input	Dynamic	High	Enable for CDSEL register. Connect to 1, if not registered. See Table 2 on page 324.
<hr/>				
FDBKSEL	Input	Dynamic	High	Select the feedback from P for operand C. When FDBKSEL = 1, propagate the current value of result P register. Ensure PLAT[1] = 0 and CDSEL = 0. When FDBKSEL = 0, propagate CIN. Ensure CDSEL = 0. To load P from CIN, ensure either A = 0 or B = 0. In SIMD mode, FDBKSEL is ignored for P[17:0] and only P[40:18] is propagated. See Table 4 on page 324 to see how operand C is obtained from CIN, P or CDIN.
FDBKSELLAT	Input	Static	High	Bypass FDBKSEL register. Connect to 1, if not registered.
ALFDBKSEL	Input	Dynamic	Low	Asynchronous load for FDBKSEL register. Connect to 1, if not registered. When asserted, FDBKSEL register is loaded with FDBKSELAD.
FDBKSELAD	Input	Static	High	Asynchronous load data for FDBKSEL register.
SLFDBKSEL	Input	Dynamic	Low	Synchronous load for FDBKSEL register. Connect to 1, if not registered. See Table 2 on page 324.
FDBKSELSD	Input	Static	Low	Synchronous load data for FDBKSEL register. See Table 2 on page 324.
EFDBKSEL	Input	Dynamic	High	Enable for FDBKSEL register. Connect to 1, if not registered. See Table 2.
<hr/>				

Table 1. Math18x18 Ports (Continued)

Port Name	Direction	Type	Polarity	Description
SUB	Input	Dynamic	High	Subtract operation. When SUB = 1, perform Two's complement subtraction to get result P = C - (A x B). When SUB = 0, perform Two's complement addition to get result P = C + (A x B).
SUBLAT	Input	Static	High	Bypass SUB register. Connect to 1, if not registered.
ALSUB	Input	Dynamic	Low	Asynchronous load for SUB register. Connect to 1, if not registered. When asserted, SUB register is loaded with SUBAD.
SUBAD	Input	Static	High	Asynchronous load data for SUB register.
SLSUB	Input	Dynamic	Low	Synchronous load for SUB register. Connect to 1, if not registered. See Table 2.
SUBSD	Input	Static	Low	Synchronous load data for SUB register. See Table 2.
ESUB	Input	Dynamic	High	Enable for SUB register. Connect to 1, if not registered. See Table 2.

Table 2. Truth Table for Control Registers SHFTSEL, CDSEL, FDBKSEL and SUB

al	ad	lat	clk	en	sl	sd	d	q
0	x	x	x	x	x	x	x	ad
1	x	0	not rising	x	x	x	x	q
1	x	0	rising	0	x	x	x	q
1	x	0	rising	1	0	x	x	!sd
1	x	0	rising	1	1	x	x	d
1	x	1	x	0	x	x	x	q
1	x	1	x	1	0	x	x	!sd
1	x	1	x	1	1	x	x	d

Table 3. Truth Table for Data Registers A, B, P and OVFL

arst	lat	clk	en	srst	d	q
0	x	x	x	x	x	0
1	0	not rising	x	x	x	q
1	0	rising	0	x	x	q
1	0	rising	1	0	x	0
1	0	rising	1	1	x	d
1	1	x	0	x	x	q
1	1	x	1	0	x	0
1	1	x	1	1	x	d

Table 4. Truth Table for Propagating Data to Operand C

FDBKSEL	CDSEL	SHFTSEL	SIMD	Operand C
0	0	0	0	CIN[40:0]
0	0	x	1	CIN[40:0]

---

Table 4. Truth Table for Propagating Data to Operand C

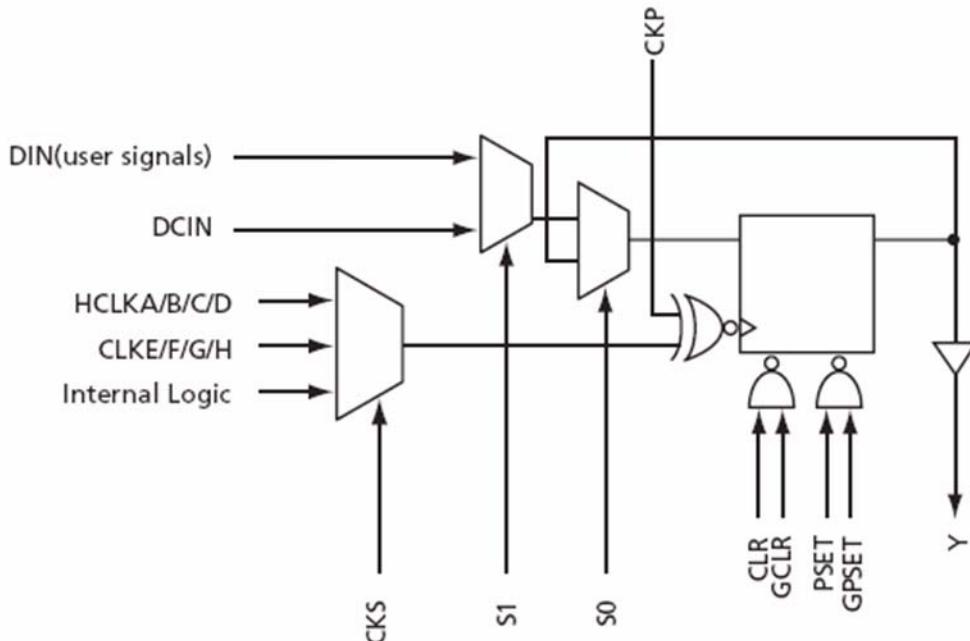
<b>FDBKSEL</b>	<b>CDSEL</b>	<b>SHFTSEL</b>	<b>SIMD</b>	<b>Operand C</b>
0	0	1	0	{ {17{CIN[40]}}, CIN[40:17] }
x	1	0	0	CDIN[40:0]
x	1	x	1	{ CDIN[40:18], CIN[17:0] }
x	1	1	0	{ {17{CDIN[40]}}, CDIN[40:17] }
1	0	0	0	P[40:0]
1	0	x	1	{ P[40:18], CIN[17:0] }
1	0	1	0	{ {17{P[40]}}, P[40:17] }



---

## *Simulation Support for GCLR/GPSET in Axcelerator*

In Axcelerator, during power up, all the sequential elements in the Fabric are set to 0 or 1 via a Global SET/CLR fuse. You can choose the SET/CLR option when generating the programming file. Each sequential element in the fabric has two additional controls, GCLR/GPSET, which are active only during power up. After power up GCLR/GPSET inputs are pulled high and user inputs are active (as shown in the figure below).



Since GPSET and GCLR are not user inputs, CAE macros do not have them. Libero IDE v9.0SP1 adds simulation support for the power up behavior of sequential elements.

In Libero IDE v9.0SP1 two additional precompiled Axcelerator libraries and one source file are provided for Axcelerator. In total there are three precompiled libraries for Verilog and three precompiled libraries for VHDL. The libraries are installed when you choose the AX family during installation. Libraries related to Axcelerator can be found under precompiled directories in the installation:

<installation>/Designer/lib/modelsim/precompiled (as shown in the table below).

**Table 1: Axcelerator Precompiled Libraries**

Directory	Description	Power Up State
/vlog/accelerator	Verilog library without gclr/gpset support	Legacy
/vlog/accelerator_gpset	Verilog library with gpset support	1
/vlog/accelerator_gclr	Verilog library with gclr support	0
/vhdl/accelerator	VHDL library without gclr/gpset support	Legacy
/vhdl/accelerator_gpset	VHDL library with gpset support	1
/vhdl/accelerator_gclr	VHDL library without gclr support	0

By default, Libero IDE maps the simulation library to the old library, i.e.

/vlog/accelerator or /vhdl/accelerator. If you want GPSET/GCLR behavior, you can map the library to one of the two new libraries.

At 0th time CLR/PRE is applied to every flip-flop or latch and is removed at some pre-defined time called POWERUP\_TIME (100 ns). This pre-defined time can be modified by editing a define statement or con-

---

stant in the source files. During the power up time user controls do not impact the behavior of the sequential element. This is according to the silicon behavior where user inputs are inactive until the power up is complete. After the power up time the sequential element behaves normally.

Note: This solution is not viable for migration macros. If you have migration macros in the netlist, those macros are not initialized to 0 or 1.

## Source libraries

One new Verilog source file and VHDL source file are present in the libraries directory. These source files are for those users who do not use precompiled libraries.

```
/src/vtl/95/accelerator.vhd - legacy  
/src/vtl/95/ax_gclr_gpset.vhd - with gpset/gclr support  
/src/vlog/accelerator.v - legacy  
/src/vlog/ax_gclr_gpset.w - with gpset/gclr support
```

## VHDL Source file

Two constants are defined inside the VTABLES package:

```
constant AX_FF_INIT_VALUE : std_ulogic := '0';  
constant POWERUP_TIME : time := 100 ns;
```

AX\_FF\_INIT\_VALUE defines the required power up state; POWERUP\_TIME defines for how long GCLR and GPSET should be applied. You can modify these constants as required and compile the library. Settings for power up states 0/1 are listed below.

### POWER UP STATE = 1

Set the constant value as below in VTABLES package

```
constant AX_FF_INIT_VALUE : std_ulogic := '1';
```

### POWER UP STATE = 0

Set the constant value as below in VTABLES package

```
constant AX_FF_INIT_VALUE : std_ulogic := '0';
```

## Verilog Source File

Like the Constants in VHDL, Verilog library has two definitions:

```
`define AX_FF_INIT_VALUE 1'b0  
`define POWERUP_TIME 100
```

AX\_FF\_INIT\_VALUE defines the required power up state. POWERUP\_TIME defines for how long GCLR and GPSET should be applied. You can modify these definitions as required and compile the library. Settings for power up states 0/1 are listed below.

### POWER UP STATE = 1

Set the definition as:

```
`define AX_FF_INIT_VALUE 1
```

### POWER UP STATE = 0

Set the definition as:

```
`define AX_FF_INIT_VALUE 0
```

