IGLOO Icicle Evaluation Kit User's Guide

Microsemi

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Introduction

Thank you for purchasing the IGLOO® Icicle Evaluation Kit. The IGLOO Icicle board is a low cost, portable, low power demonstration platform powered by USB cable, external power or rechargeable lithium-ion battery (Suggested part number LIR2450). The IGLOO Icicle board, as well as the low cost programming stick (LCPS), is RoHS-compliant. The Icicle board and the LCPS are completely lead (Pb) free. The kits are packaged in recyclable materials made from recycled materials.

Documentation Contents

Chapter 1 – IGLOO Icicle Evaluation Kit describes the contents of the IGLOO Icicle evaluation kit.

Chapter 2 – Using the IGLOO Icicle Evaluation Board describes how to program the board and evaluate power usage. It also provides a design example and ideas for simple projects.

Appendix B – Sample Design AGL125-QNG132 Device provides a basic sample design for the AGL125-QNG132 device.

Appendix C – AGL125-QNG132 Pin Connections provides tables listing FPGAs and their connections.

Appendix D – Product Support describes Microsemi support services.

Documentation Assumptions

This user's guide assumes the following:

- You intend to use Microsemi Libero® System-on-Chip (SoC) software.
- You have installed and are familiar with Libero software v8.2 or later.
- You are familiar with PCs and the Windows® operating system.

Reference Documentation

IGLOO Icicle Evaluation Kit schematics of the main IGLOO Icicle board:

www.microsemi.com/soc/products/hardware/devkits_boards/igloo_icicle.aspx#docs

IGLOO Icicle Evaluation Kit Allegro board layout file:

www.microsemi.com/soc/products/hardware/devkits_boards/igloo_icicle.aspx#docs

IGLOO FPGA Fabric User's Guide:

www.microsemi.com/soc/documents/IGLOO_UG.pdf

Abbreviations and Acronyms

Table 1 • **Acronyms Used**

Acronyms	Description
Icicle	Name given to the small "icicle sized" board featuring the AGL125 device which is very low power, hence cool, hence the marketing name "Icicle"
LCPS	Low cost programming stick
DMM	Digital multimeter
FPGA	Field programmable gate array
ULSICC	User low static ICC macro

1 – IGLOO Icicle Evaluation Kit

Kit Contents

The RoHS-compliant environmentally friendly IGLOO Icicle Evaluation Kit is packaged in a recyclable cardboard box made from recycled materials. The box contains the following items:

- IGLOO Icicle evaluation board with AGL125-QNG132 Device
  - Option to be battery powered via lithium-ion battery and a built-in charger from USB cable (Suggested part number is LIR2450).
  - Ability to measure current on VCCI, which is shared with all I/O banks, and VCC for accurate power analysis
  - Lowest power 125 k system-gate FPGA in the world
  - Ultra-low power consumption in dynamic, static, and Flash*Freeze modes
  - Low power enables a long battery life for a typical portable device
  - Ability to switch VCC from 1.2 V to 1.5 V as needed
  - Ultra-small QN132 (8 x 8 mm) device fitted inside a ring of connectors for a VQ100 device. The evaluation board has been designed for use with either package.
  - Optional board power connector for an external supply, but none is needed when connected to a USB cable
- Low cost programming stick containing built-in FlashPro3 programmer
  - Plugs directly into IGLOO Icicle evaluation board. A USB 2.0 high-speed cable plugs into the LCPS for programming of the IGLOO device.
- Libero Software License
  - Gold edition with free license includes best-in-class third-party tools
  - Supports system-on-chip designs, up to 1 M system gates within the IGLOO family, and all features of the IGLOO device included with the IGLOO Icicle evaluation board
  - User's Guide and tutorial available on website
  - Printed Circuit Board (PCB) layout in Allegro format available on website
  - Sample design available on website

Board Description

The Icicle evaluation board enables you to measure power consumption (dynamic, static, and Flash*Freeze mode) with the core operating at either 1.2 V or 1.5 V. When using the board in conjunction with Microsemi's power analysis tools, you will have a clear picture of application power consumption at each stage in your design. In addition, the Libero SoC tool suite now includes Power-Driven Layout (PDL), which can reduce the power consumption of designs up to 30 percent.

The evaluation board is the size of a small cell phone, measuring 1.4 inches x 3.6 inches and supports an AGL125 IGLOO device in the 8 x 8 mm QN132 package. The evaluation board consumes less than 150 mW and can extend the life of an optional rechargeable lithium ion battery over seven times that of the competitive solutions. All components used on the board, such as LEDs (2 mA), resets (µA range), and oscillator (2–3 mA), are low power components, including the green (Rev B board) or blue (Rev D board) OLED display 96 x 16 (0.8 inches) for quick demos. Also included on the evaluation board is a USB-to-UART interface to allow Hyperterminal on a PC to communicate with the IGLOO device on the board.

The ring of copper pads around the center QN132 package is there for alternatively mounting an IGLOO device in the VQ100 package. This provides flexibility in what you can attach to this board if you remove the existing device. Cross-device pin compatibility with AGL030, AGL060, and AGL125 (fitted to existing board) is better in the VQ100 package, which is why the board has been designed with this flexibility. All the VQ100 pins are wired to the corresponding pins of the QN132 package.

The left hand side of the board has a programming connector which allows the LCPS to be attached to the board to program the IGLOO AGL125-QNG132 device. The connector on the right hand side of the board is for accessory boards. It is a 38 pin connector. A set of the FPGA I/O pins are connected to this connector as well as some power pins. Spare I/Os from the FPGA have been wired to pads on the board for debug purposes.

A top silkscreen of the Rev B board is shown in Figure 1-1 on page 6. A bottom silkscreen is shown in Figure 1-2 on page 7. The location of the lithium ion rechargeable cell can be seen as the large round area shown on the silkscreen/

The Rev D (blue OLED) boards exhibit lower power than the Rev B (green OLED) version owing to the elimination of various leakage paths, achieved by making all the switches and LEDs on the board Active Low instead of Active High. A top silkscreen of the Rev D board is shown in Figure 1-3 on page 7. A bottom silkscreen is shown in Figure 1-2 on page 7.

Note: In Rev D board layout, components are placed very close so that silkscreen is also grouped together. Due to this reason, jumper locations for JP5 and JP6 are marked incorrectly on silkscreen. Refer to the Figure 1-3 on page 7 for the correct physical locations of jumpers JP5 and JP6.

Silk Screens

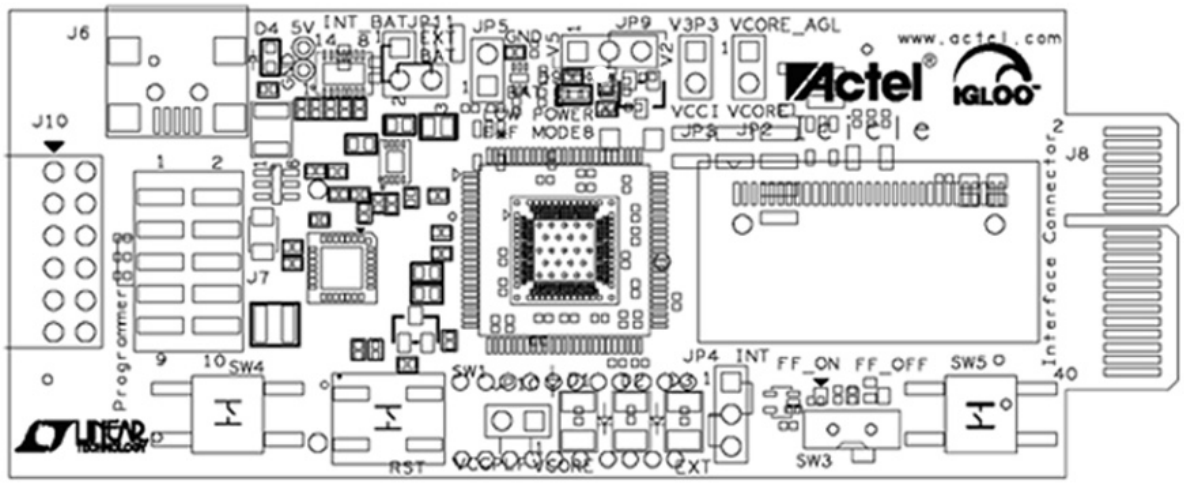

***Figure 1-1* • Rev B IGLOO Icicle Board – Top Silkscreen**

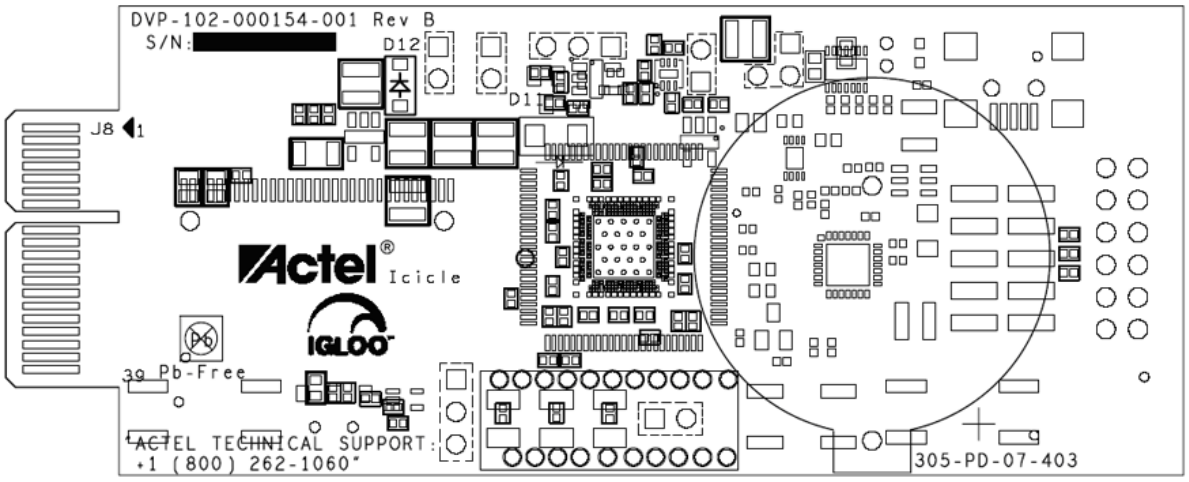

***Figure 1-2* • Rev B IGLOO Icicle Board – Bottom Silkscreen**

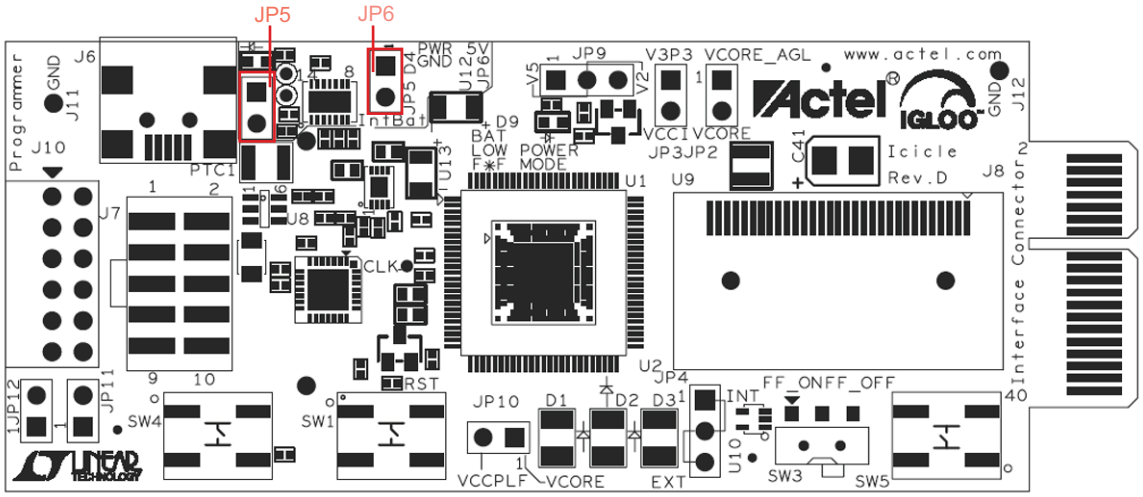

***Figure 1-3* • Rev D IGLOO Icicle Board – Top Silkscreen**

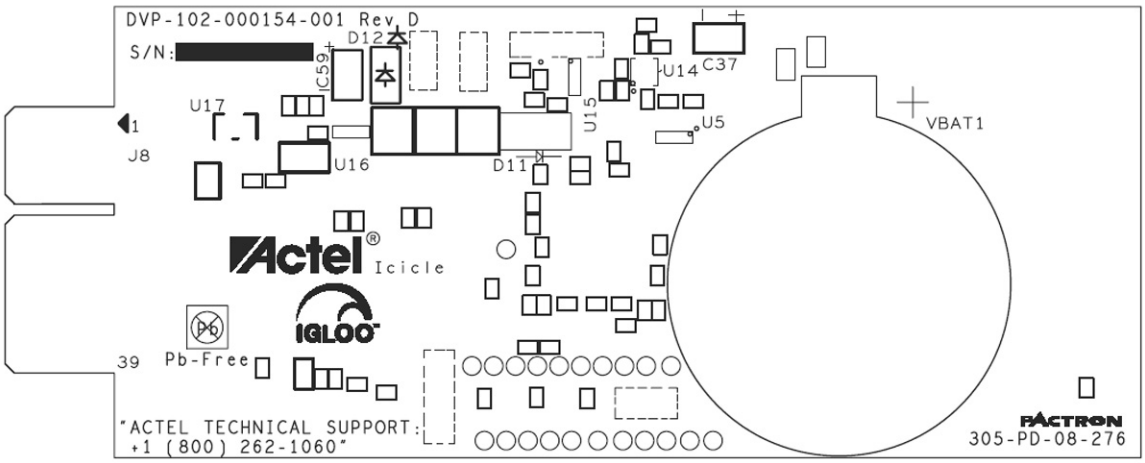

Figure 1-4 • **Rev D IGLOO Icicle Board – Bottom Silkscreen**

The main Microsemi technical support number is shown on the bottom left of the bottom silkscreen to aid in answering support questions.

Circuit Diagram

The circuit diagram for the IGLOO Icicle Evaluation Kit is available on the IGLOO Icicle Kit CD as well as on Microsemi SoC Products Group's website. Refer to these schematic sheets when reading this subsection.

Third Party Connector

The Accessory Board Connector, or Interface Connector, is shown in the schematics. This sub-circuit is shown in Figure 1-5.

This connector can be used to connect additional cards, some of which are in development by partners and third parties. The possibilities are numerous and include memory interfaces with Flash and SRAM, keyboard interfaces for embedded applications, LCD display panel interfaces, motor control interfaces and several other application areas. Use GPIOA_1, GPIOA_2, GPIOA_4, and GPIOA_31 signal lines for critical signals such as clock and reset because proper series termination has been provided on these particular signal lines.

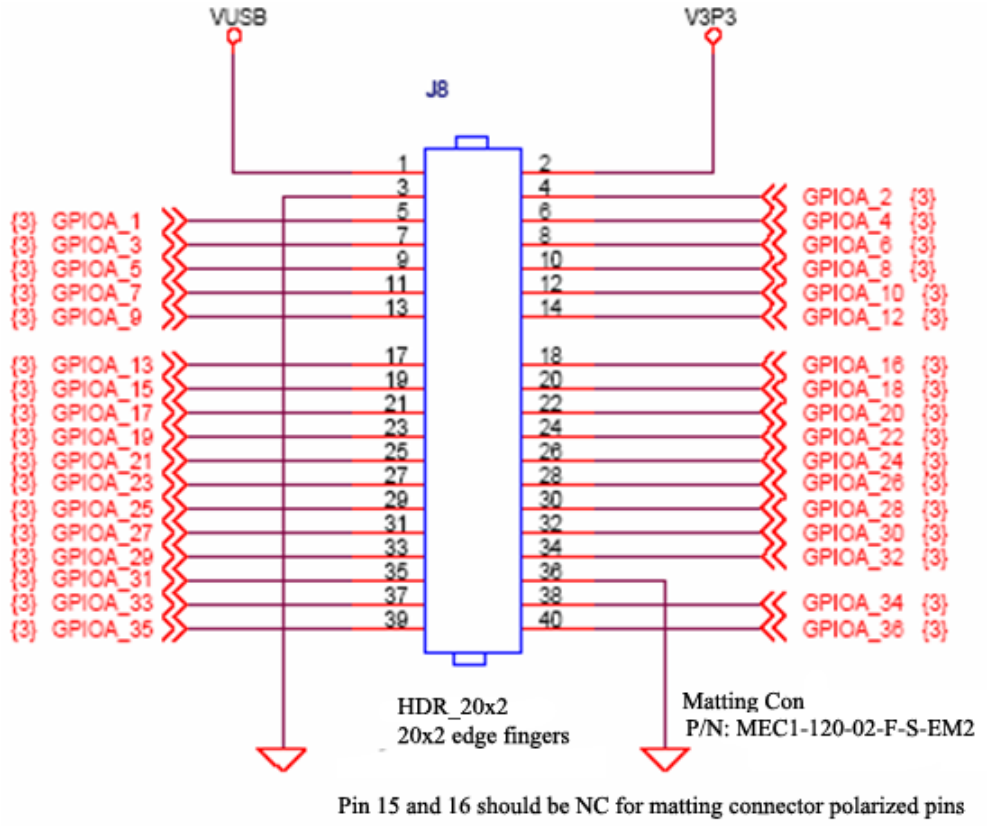

***Figure 1-5* • Accessory Board Connector**

Note: Pins 15 and 16 are not present on the header. These pins form the cut-out for the interface to ensure correct orientation.

OLED Display Module

The OLED display module used on the first version (Rev B boards) of the IGLOO Icicle Evaluation Kit is a 96x16 green OLED display from OSRAM. See Figure 1-6. The second version (Rev D boards) of the IGLOO Icicle Evaluation Kit contains a blue OLED display and has a serial I^2C interface instead of a parallel interface.The OLED interconnections on Rev B and Rev D boards are shown in Figure 1-7 and Figure 1-8 on page 11. The module is folded over with a flexible PCB interface so that the interface is soldered to the board below the flexible strip. The strip attaches the module panel. The display used on Rev B boards is the Pictiva 96X16 OLED Module, SSD0303, Hilo 1-bit H36XX-OS096016PP08MXXB10 from OSRAM. The display used on Rev D boards is the PACER 96x16 OLED module, PMO13701 using SSD0300 as driver IC. The datasheet for the display can be found on the IGLOO Icicle Evaluation Kit CD.

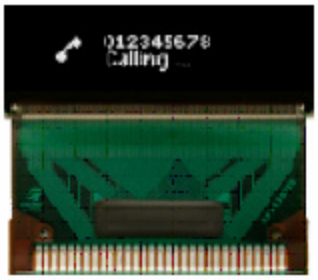

***Figure 1-6* • OLED Display Module**

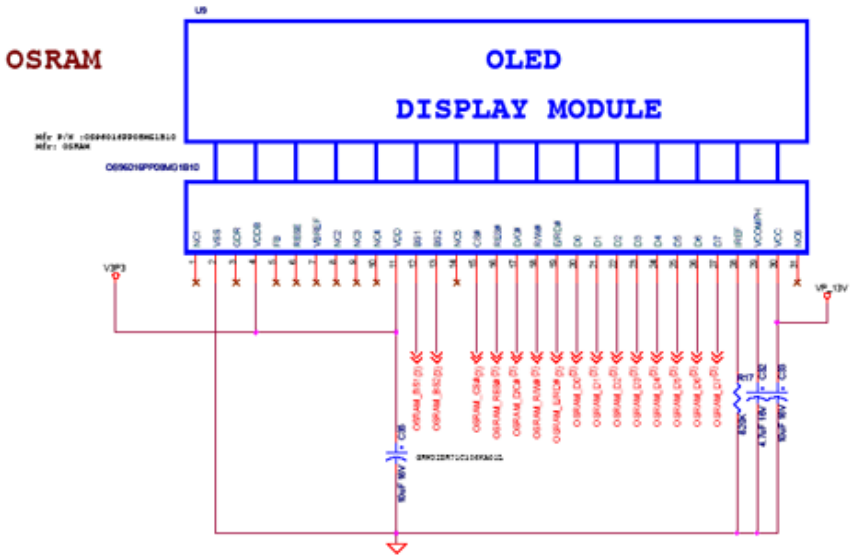

***Figure 1-7* • OLED Display Module Interconnects (Rev B boards)**

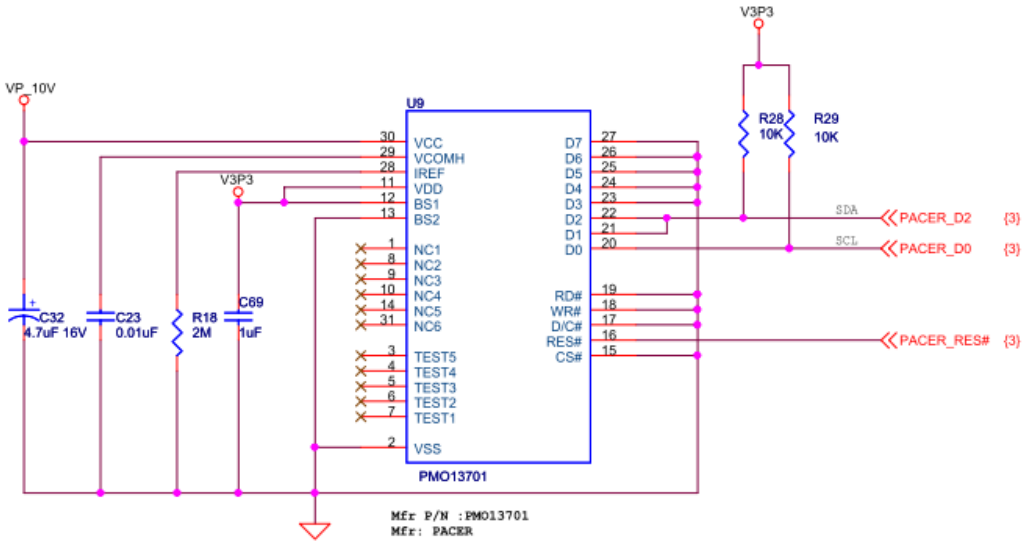

***Figure 1-8* • OLED Display Module Interconnects (Rev D boards)**

Resistor-Set Oscillator

The oscillator used on the IGLOO Icicle Evaluation Kit is a precision resistor-set oscillator. The LTC1799CS5 oscillator is from Linear Technologies and provides the ability for an end user to change the frequency of the board oscillator by simply changing a resistor on the board. Figure 1-9 shows the schematic in detail. The oscillator has a 1 kHz to 33 MHz Frequency Range with a Frequency Error of <1.5% over a frequency range of 5 kHz to 20 MHz (Tamb = 25°C) with ±40 ppm/°C Temperature Stability.

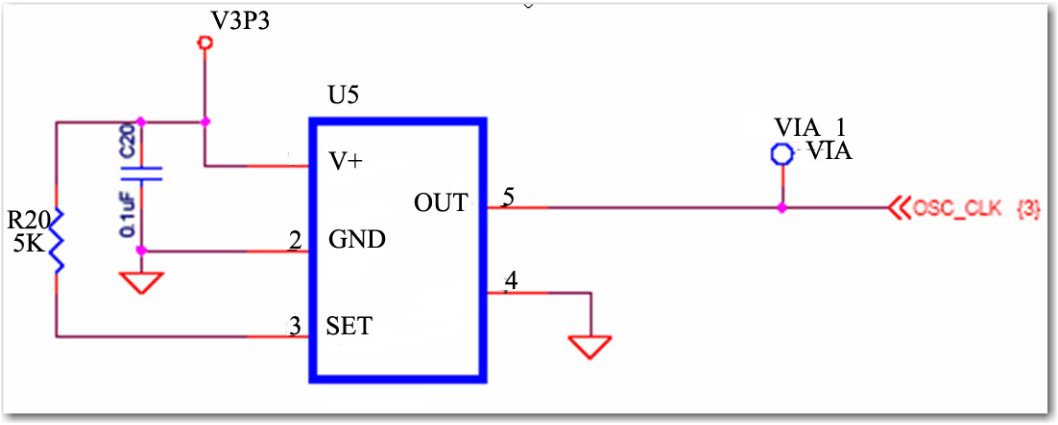

***Figure 1-9* • The Resistor-Set Oscillator**

The formula for determining the frequency is shown in EQ 1-1:

$$f_{OSC} = 10\ \text{MHz} \bullet \left(\frac{10k}{N \bullet R_{SET}}\right) \qquad N = \begin{cases} 100, \text{ DIV Pin} = V+ \\ 10, \text{ DIV Pin} = \text{Open} \\ 1, \text{ DIV Pin} = \text{GND} \end{cases}$$

EQ 1-1

It can be seen that R20 in the circuit has a 5 kΩ value, which owing to the fact that the DIV pin is connected to ground will give an f_{OSC} of 20 MHz on this board. Having a resistor-set oscillator makes changing the frequency a low-cost and flexible option for the end-user.

It should be noted that lowest power will be observed at lower frequency values. Datasheets for the oscillator are provided for reference on the IGLOO Icicle Evaluation Kit CD. Many circuits only need a 32.768 kHz watch crystal frequency and will be far more power optimal than the equivalent circuit running at 20 MHz. The end user can experiment with circuit frequency to determine how IGLOO may help save power under different intended modes of operation.

Power Management

There are five main components to power management used on the IGLOO Icicle Stick:

1. Automatic switchover circuit/USB Power Manager

   USB–powered board that can powered externally. It can also be powered by an internal lithium ion rechargeable battery. There is a recharge circuit built into the board.

   USB interface is also serial UART
2. Buck boost DC to DC converter (3.3 V) — for VPUMP etc.
3. VLDO linear regulator — 1.2 V/1.5 V output
4. Current sense circuit
5. High voltage supply for the OLED display

In addition, external power can be applied to the board. It is possible to disconnect the internal battery and add external sources, for example, add a solar cell array or add a crank up generator to JP5 connector on Rev B boards or JP6 connector on Rev D boards.

Automatic Changeover Circuit

The automatic switchover circuits used in Rev B and Rev D boards are shown in Figure 1-10 on page 13 and Figure 1-11 on page 14 and is on the main IGLOO Icicle schematics.

Rev B

JP11 is a three pin header which is used to select where the power is coming from.

- Pins (1, 2) select power supply from LTC4088 regulator
- Pins (2, 3) select power supply from external solar cell header JP5

Rev D

JP6 is used to select power supply source that is either on-board LTC4088 regulator or external power source. Short the jumper JP6 to select on-board LTC4088 regulator as power supply or add external source like solar cell array across JP6.

Note: There is no JP11 on Rev D boards instead JP6 is used for the selecting power supply source.

The LTC4088 regulator provides diode protection with low voltage drop of 0.1 V cf. 0.7 V of normal diode and provides seamless recharge of the lithium battery. The lithium battery can be mounted on the back of the board. It should be noted that the USB connection on the main IGLOO Icicle board can provide all the power for running the board, recharging the battery, and providing power to any accessory card, provided it meets certain power restrictions. When an external power supply is connected, it has been demonstrated that a solar cell's output can be connected to the JP5 connector on Rev B boards or JP6 connector on Rev D boards and have full running of the board with a small low-cost (inefficient) solar cell in sunlight.

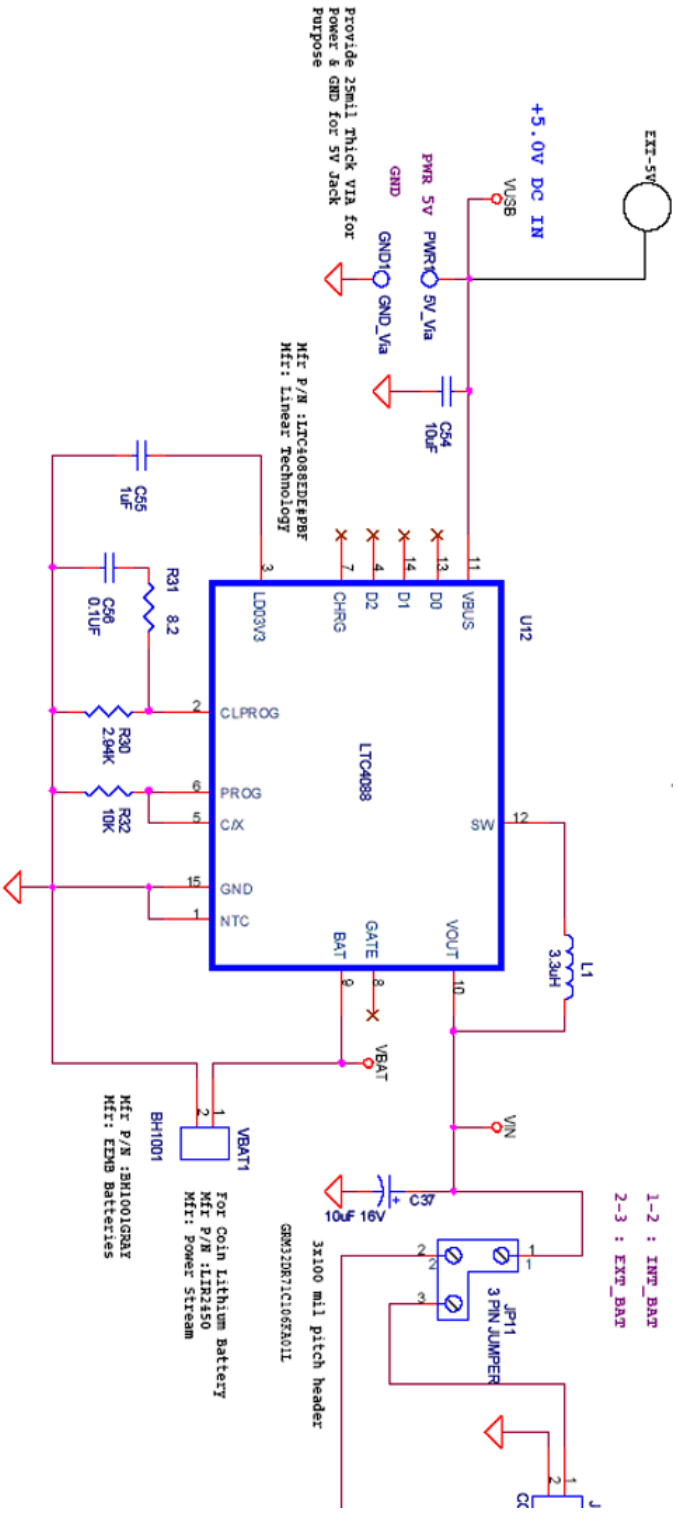

Figure 1-10 • **Automatic Switchover Circuit/USB Power Manager (Rev B Boards)**

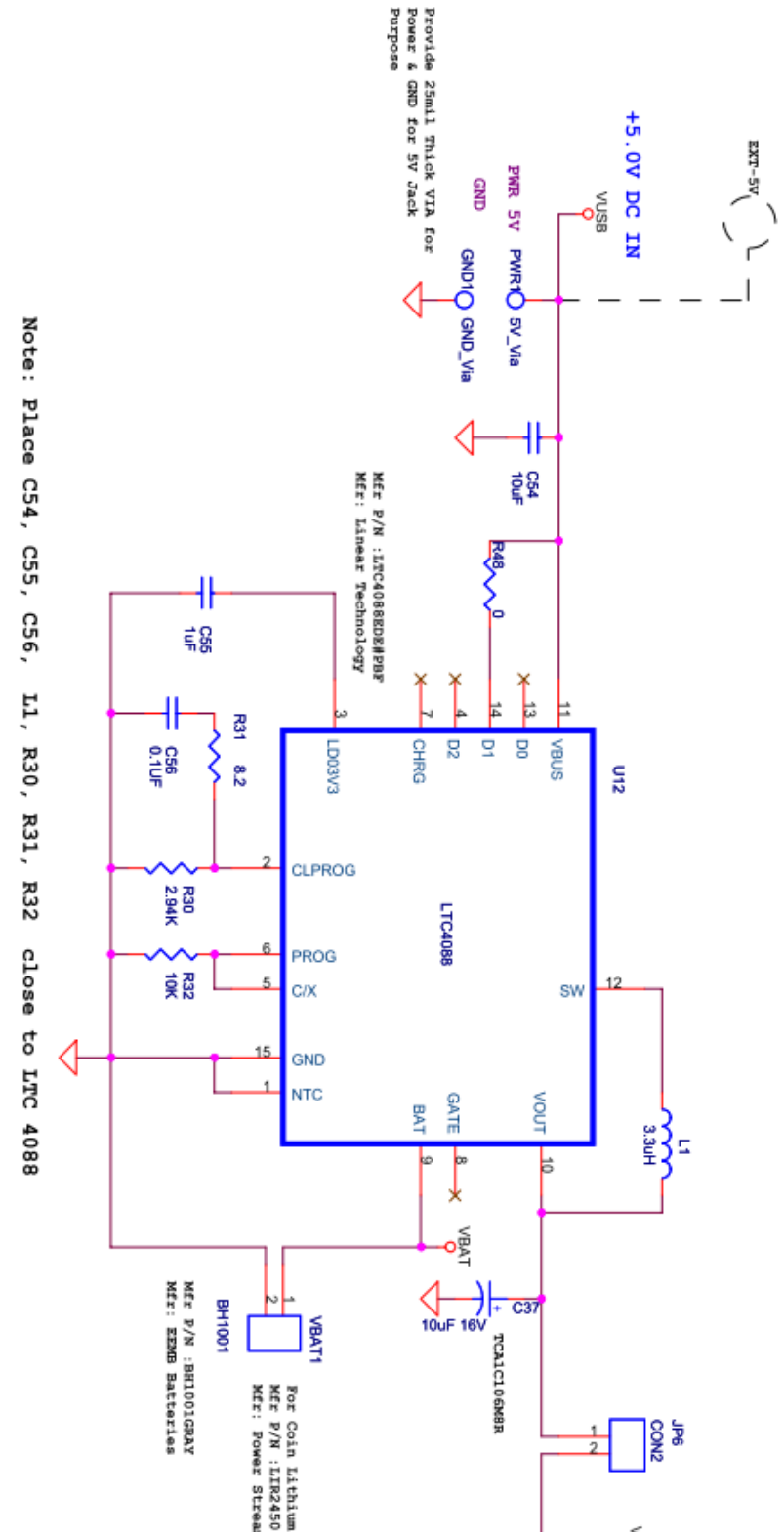

Figure 1-11 • **Automatic Switchover Circuit/USB Power Manager (Rev D Boards)**

The suggested battery model on the boards is a Power Stream LR2450, which has a good recharge capability. The board can be powered directly from the LR2450 for many hours with the supplied demo running. The nominal capacity of the battery is 120 mAh. See Table 1-1.

***Table 1-1* • Battery Capacity**

Model	Nominal Voltage (V)	Nominal Capacity (mAh)	Max Pulse Discharge Current (mA)	Diameter (mm)		Weight (g)	Max Discharge Current (mA)	Cycle Life (Times)
				C(Diameter)	T (Thickness)			
LIR2450	3.60	120	180	24.5	5.0	5.2	35	500

Buck-Boost DC-Converter

The Buck-Boost DC-DC convertor uses a Linear Technologies LTC3538 part. The circuit is shown in Figure 1-12.

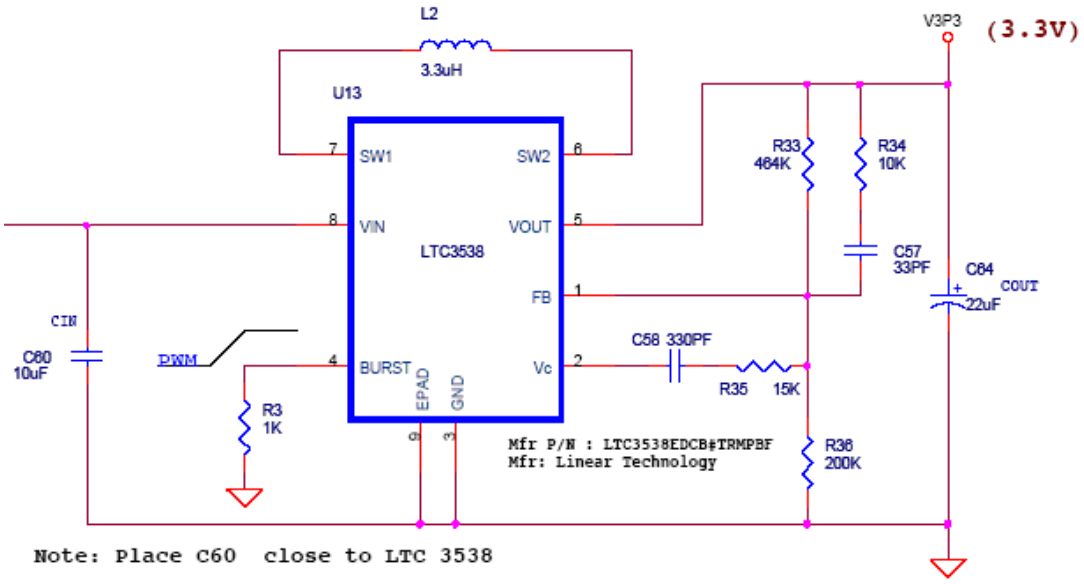

***Figure 1-12* • Buck–Boost Circuit**

The input voltage VIN for this Buck-Boost DC-DC converter is coming either from the on-board LTC4088 regulator or external power supply like solar cell based on corresponding jumper settings.

VLDO Regulator for VCC Generation of 1.5 V and 1.2 V

The Very Low Drop-Out (VLDO) linear regulator circuit based on the LTC3025 (see Figure 1-13 on page 16) is the circuit that provides the core voltage VCC for the IGLOO part. The AGL125 part can operate with VCC at both 1.5 V and 1.2 V. Power consumption will be less at the lower setting of the core voltage. However, programming must occur at 1.5 V.

The VLDO circuitry provides a jumper to allow the core voltage to be selected one of two ways:

- The jumper can be permanently set at 1.5 V. This allows measurements of power consumption at this value of core voltage and to allow programming.

  or

- The jumper can be set at 1.2 V with an automatic electronic switch to 1.5 V during programming.

The LTC3025 has a low bandgap reference of 0.4 V, so no bandgap offset zener is required to get the output voltage down to 1.2 V. This is common with many higher bandgap reference regulators.

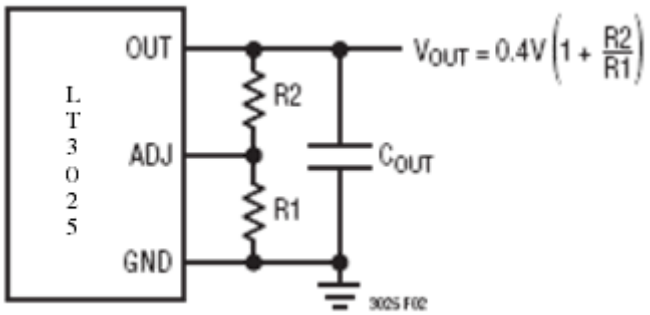

***Figure 1-13* • Formula for LTC3025 Regulator**

The overall circuit for the 1.5 V and 1.2 V generation appears Figure 1-14.:

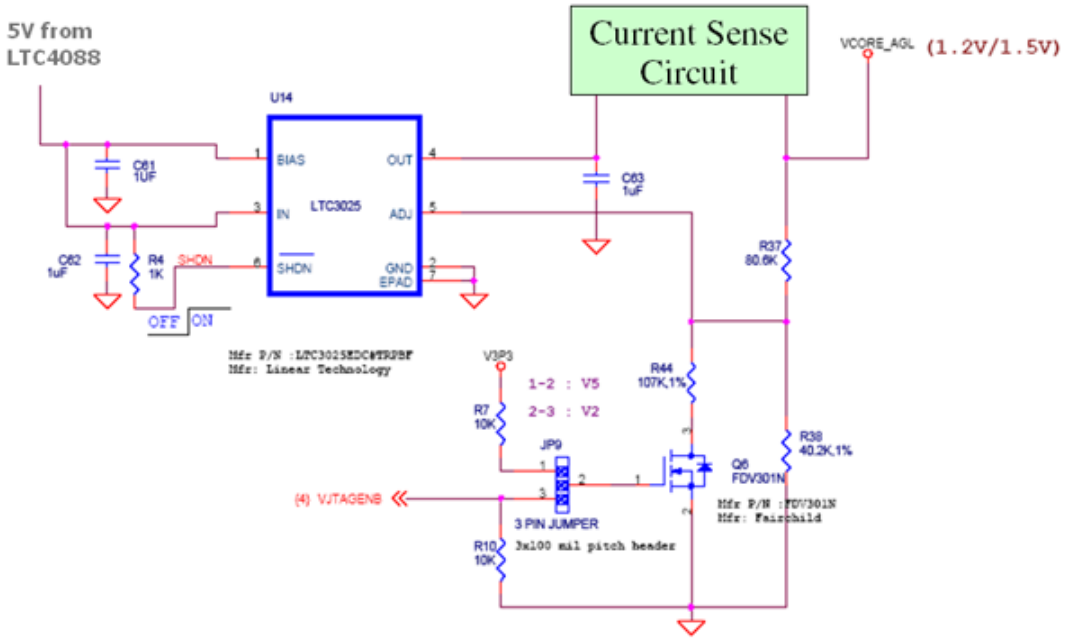

***Figure 1-14* • VLDO Regulator Circuit for VCC of 1.2 V or 1.5 V**

JP9 in (1, 2) position ties the gate of the MOSFET Q6 to a high value, switching the MOSFET on and putting R44 in parallel with R38. This lowers the resistance of the lower resistor in the divider chain and raises the voltage to 1.5 V. When JP9 is in the (2, 3) position, the MOSFET Q6 is off, as the gate is tied to ground through R10. In this case, the divider chain is simply R37 and R38 and the voltage generated is 1.2 V. Notice that pin 3 is also tied to a signal called VJTAGENB. The VJTAGENB signal is provided by the LCPS and is activated at the start of programming and maintains a high state during programming. This signal is used to switch the MOSFET Q6 on during programming,. This places R44 in parallel with R38 during programming and raises the supply voltage to 1.5 V during programming. When programming is complete, VJTAGENB goes low and with JP9 in the (2, 3 position, the core voltage returns to 1.2 V.

This circuitry is quite simple for users of IGLOO technology. It is references to illustrate how a single voltage variable regulator may be used to generate two voltages with very low cost circuitry and with little additional board space being used.

Current Sense Circuit

As a convenience feature for demonstration purposes, the IGLOO Icicle board contains a current sense circuit to illuminate an LED when the current consumed by the FPGA drops below a certain level. This indicates that the FPGA is in Flash*Freeze mode. A self detection circuit triggers the LED if the FPGA current goes below 100 µA on the 1.5 V/1.2 V VCC rail. It shows true F*F requiring no FPGA current consumption. The LED D9 employed for this purpose is a special low-current (2 mA) LED. It retains good battery life while demonstrating that the circuit is in Flash*Freeze.

The circuit is shown in Figure 1-15.

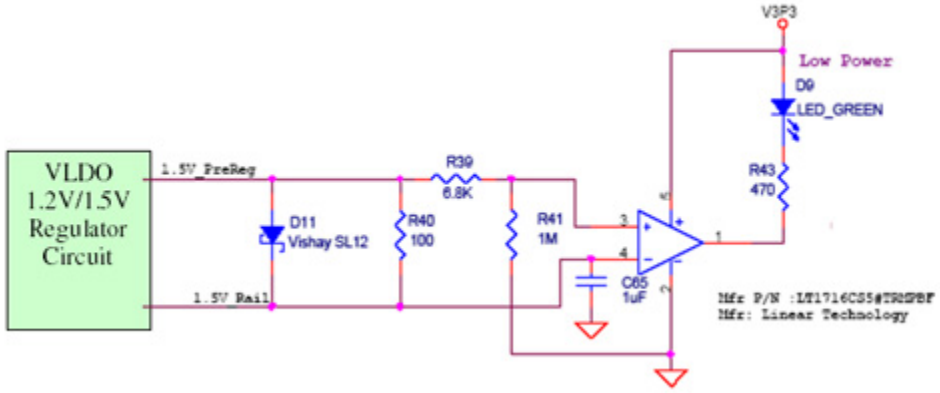

***Figure 1-15* • Current Sense Circuit**

Hi–Voltage Supply for OLED Display

The OLED display device needs a low current, high voltage supply to operate correctly. This is provided by the LT1615 module shown in Figure 1-16 and Figure 1-17 on page 19.

The Step-Up DC/DC converter LT1615 is used to generate 13 V OLED supply on Rev B boards and 10 V OLED supply on Rev D boards.

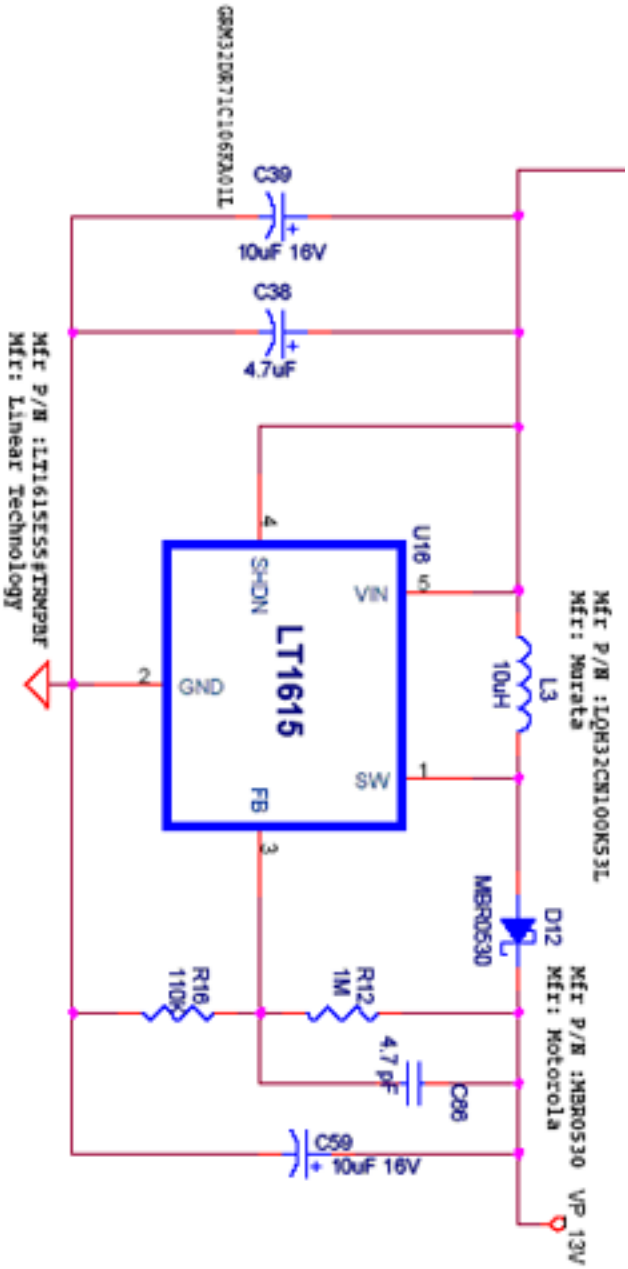

***Figure 1-16* • High-Voltage Power Supply Circuit (Rev B Boards)**

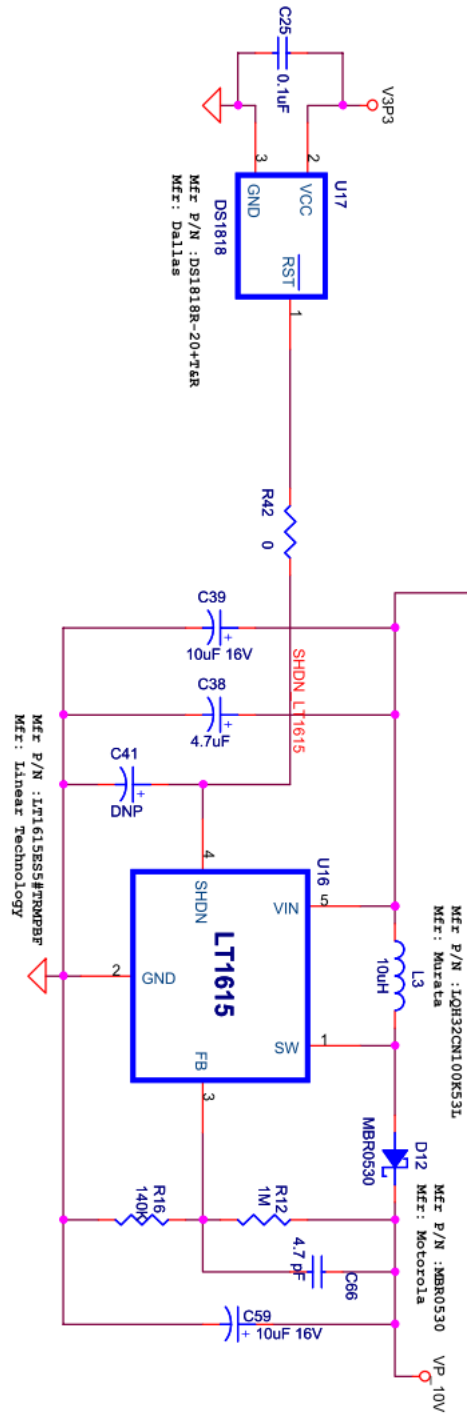

***Figure 1-17* • High-Voltage Power Supply Circuit (Rev D Boards)**

User Interaction

A variety of different user interaction cases are provided.

Simple Interaction

- Three test LEDs: D1, D2, and D3
  - Rev B (green OLED) boards, all are driven by active high outputs from the FPGA.
  - Rev D (blue OLED) boards, all are driven by active low outputs from the FPGA.
- Two test switches: SW4 and SW5 push button
  - Rev B (green OLED) boards, both provide active high signals to the FPGA
  - Rev D (blue OLED) boards, both provide active low signals to the FPGA

  Switches are mounted either side of board and OLED display with SW4 being the left most switch and SW5 being the right most switch.

  This allows more effective "thumb play" when hand-held
- Flash*Freeze switch for ultra low power consumption: SW3 slider (the Flash*Freeze input to the FPGA is Schmitt-triggered via U10, the Texas Instruments SN74AUP1G17 component)
- System reset push button switch: SW1 (active low, provides 100 ms active low pulse)
- This is the closest switch to the FPGA
- Test points for measuring current consumption of the AGL125

Complex Interaction

- Keyboard on accessory card is a possibility
- OLED display
- Hyperterminal running on PC via USB-to-UART interface allows for far more complex interfaces

Lowering Power by Switching off VCCPLF

The lowest possible power is obtained by switching off VCCPLF if the PLL is not being used. The default setting of JP10 is to have the shunt connected to provide core voltage to the PLL circuitry in the IGLOO device. To remove power to the PLL circuitry, remove the shunt across J10 (located on the bottom of the board to the right of the reset switch and to the left of the LEDs D1, D2, and D3). See Figure 1-18 on page 21.

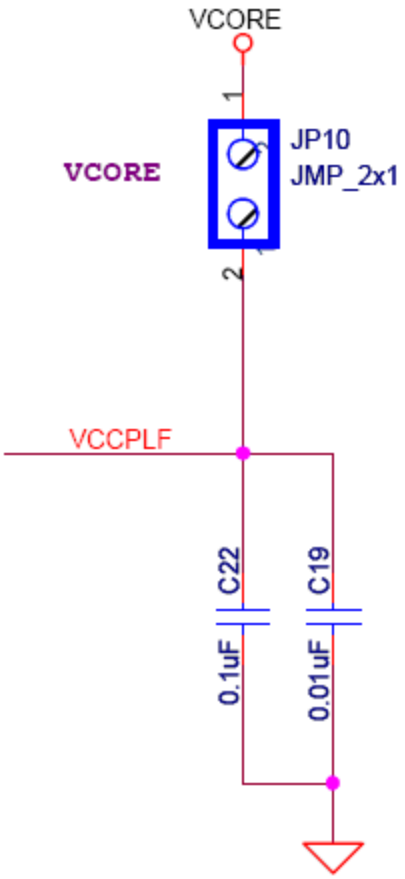

***Figure 1-18* • JP10for Removing Power to VCCPLF**

Lowering Power – Other Techniques

All the main switches in the Rev B (green OLED) board, with the exception of the reset switch, are Active High logic. They have pull down resistors on the board to ensure that they are grounded when inactive. If the switches are left unused in a design, then the Designer software will add a pull-up by default. This creates a leakage path and in Flash*Freeze mode you will see this extra current on the VCCI rail. To show the true Flash*Freeze current on the VCCI rail, you need to use the switches even though they are not needed in the design. In the Rev D (blue OLED) board, all the switches are Active Low logic. The Rev D board avoids the leakage path problem described above.

A similar statement holds true for the 1 k Ohm pull-down on TRST. If you wish to demonstrate the minimum possible Flash*Freeze current on the VCCI rail, you will need to account for this current by subtract it from your readings, or remove the resistor from the board.

Current Measurement

Look at the following notes that describe how to select a Digital Multimeter (DMM) before looking at how to measure different aspects of current on the board. The IGLOO Icicle board has been designed for the AGL125 in both the VQG100 and the QNG132 packages.

When examining the schematics, look at both the connectors for the AGL125-VQG100 as well as the connectors for the AGL132. The connections are shared between the schematics. The JP2 and JP3 jumpers for provide core voltage and 3.3 V VCCI I/O bank voltage. Not only do they supply voltages to the AGL125-VQG100 but they also supply these same voltages to QNG132 packaged version of the device.

Notes on Selecting a DMM

Selecting a DMM suitable for measuring current is important if the measurements obtained are to be meaningful. If the DMM impedance is too high, then the resulting voltage drop will make the measurements, even if accurate, liable to misinterpretation as the circuit will have been changed owing to a voltage drop. The best laboratory standard multimeters for current measurement in the pA range have incredibly low impedances (mΩ) at the µA range. This ultra low impedance result is almost no voltage drop to the circuit being measured.

When selecting a DMM for measuring microamps of current, it is recommended that you double check the internal impedance of the DMM when set to the mA range and the µA range respectively. On many lower cost DMMs, the µA range is obtained by a large value of resistance, often several hundred to a couple of thousand Ω. Unfortunately, it is this impedance which will cause the voltage being applied to the circuit to drop and cause false measurements of current. The impedance of any DMM on a current measuring range should be as low as possible (ideally less than 10 Ω when measuring microamps) so as not to cause a voltage drop to the circuit that you are measuring. If the impedance on the smallest current measuring range is too high, it is often much lower (and in a range of acceptably low values) once you move to the next highest current range on the DMM. For example, moving from the µA range to the mA range will often allow much more accurate measurements even though the resolution will be less. This occurs because the voltage drop will be minimized. Use a second DMM to check the impedance of the first DMM in different range settings so that you know the limits of your test equipment.

FPGA Current Measurement

JP2 is to the right of JP3 at the top of the board and is labeled VCORE below the jumper and VCORE_AGL above the jumper on the silkscreen. See Figure A-1 on page 34. You can measure the current consumed by the core of the FPGA alone by placing a DMM with sufficient resolution for microamps (mA scale usually is sufficient with three digits after decimal place) across JP2 and removing the shunt. Change the core voltage using JP9, and measurements can be made with the FPGA core running at 1.5 V or 1.2 V.

Apart from the current consumed by the core, current can also be consumed by the I/O banks on the device. JP3, positioned to the left of JP2, can be used to measure the current consumed by the I/O banks. Pin 1 of JP3 is wired to 3.3 V and with the shunt in place, this voltage is applied to VCCI of the FPGA, which is connected to pin 2 of JP3. A DMM placed across JP3 will therefore enable the current consumed by the LVTTL I/O banks to be measured. For the Icicle board there are no choices of alternative settings of VCCI for the FPGA other than 3.3 V.

An advanced user can, at their own risk, disconnect the shunt and apply their own voltages to pin 2 of JP3 in order to experiment with operating the I/O banks at a different voltage. Refer to the IGLOO datasheet before attempting such modifications to the IGLOO Icicle board.

Total Board Current Measurement

The total current consumed by the board could be measured from a meter inserted into the lead attached to the USB connection, but this would also account for the current used to recharge the Li-Ion battery. An alternative point for measuring total board current on Rev B boards is to use JP11 and an external supply connected to JP5. Remove the shunt across JP11 and insert a DMM between pins (2,3) of JP11. Do not insert a DMM into the circuit at pins (1,2) of JP11 because the output of the LTC4088 USB Change Over Circuit is very sensitive to inductance. Inserting a DMM across pins (1,2) will insert a large inductance giving rise to undesirable fluctuations in power rail circuitry across the board. Similarly JP6 on Rev D boards can be used as an alternative point for measuring total board current.

Typical current consumption of the board with the OLED display being driven will be up to 150 mA. The IGLOO AGL125 will be a very small percentage of this consumption. In Flash*Freeze mode at a VCC of 1.2 V, current consumption of the FPGA will be down to 18µA or less. Even when not in Flash*Freeze mode, the current consumption is quite minimal. Typically in the order of a few hundreds of microamps with a typical active-I/O design running at 20 MHz.

It should be noted that the accessory-card/interface-card connection will consume power if a card that is powered from the IGLOO Icicle board is connected to it. Both VUSB at 5 V and 3.3 V are connected to pins 1 and 2 respectively of the interface header. USB under high-power can supply up to 500mA for a device. If the Icicle board is assumed to consume a peak of 150 mA, then up to 350 mA could be available for a daughter card. However, this is not conservative enough.

To allow for some margin of error, it is safer to assume that the accessory card connected to the interface board should have a maximum current draw of 300 mA at 5 V or 300 mA on the 3.3 V line. It is recommended that total power consumption of the accessory board should always be less than 1.5W. Although the Icicle board can supply 300 mA on both the 5 V pin and the 3.3 V pin, peak current should not be drawn at these two voltage levels simultaneously. Remember that current is consumed by the I/O pins connected to the accessory card. The 1.5 W peak power draw limit of the accessory board should be observed when designing accessory boards that are to be powered solely by the IGLOO Icicle board.

Board Stack-Up, Layers of Board

The board is formed on an eight layer PCB. The layers are four signal layers and four interspersed planes. The layers are arranged this way:

1. Top Signal layer (on which FPGA is mounted) Figure A-2 on page 35
2. Ground Plane
3. Signal Layer Figure A-3 on page 36
4. Power Plane Figure A-4 on page 37
5. Ground Plane
6. Signal Layer Figure A-5 on page 38
7. Ground Plane
8. Bottom Signal Layer Figure A-6 on page 39

This particular stack-up allows for the signals from the QN132 package to be routed efficiently and with good signal integrity.

Low–Cost Programming Stick for the Icicle Board

The LCPS is a special version for the FlashPro3 programming circuitry that is compatible with FlashPro3 and the generic FlashPro programming software. The LCPS, like the IGLOO Icicle board, is RoHS–compliant and is completely lead (Pb) free. To use the LCPS with the FlashPro software, all you need to do is to select the FlashPro3 from the list of programmer types. The LCPS behaves exactly as if it were a regular encased FlashPro3 programmer. The LCPS is designed for use with the IGLOO Icicle board alone and is not supplied as a separately orderable item from Microsemi Corporation. The 12-pin female connector socket is designed to interface to the 12 pin right–angle male header on the Icicle evaluation kit. One of the pins is a special VJTAGENB signal that goes high when programming is taking place and returns to a low level when programming has completed. The Icicle board uses this signal to effect a change in the value of VCC from 1.2 V to 1.5 V which is required for programming all IGLOO devices.

The LCPS is built on a four layer PCB with the layers arranged in the following stack-up:

1. Top signal layer
2. Ground plane
3. Power plane
4. Bottom signal layer

The top silkscreen is shown in Figure 1-19.

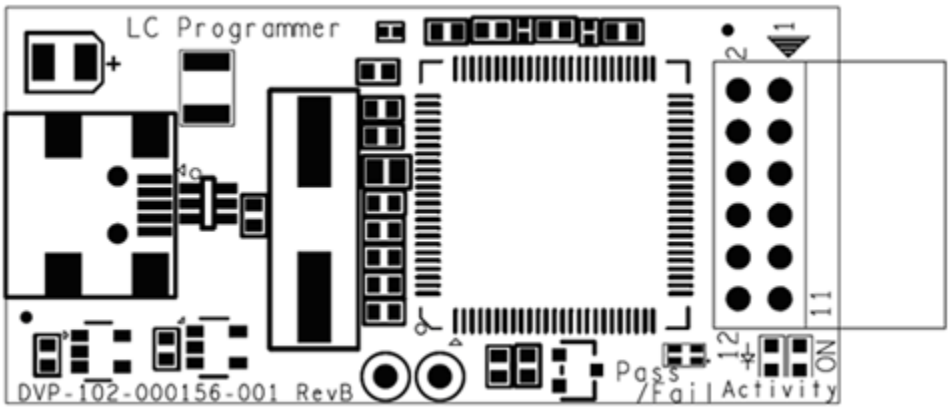

***Figure 1-19* • LCPS–Top Silkscreen**

The bottom silkscreen is shown in Figure 1-20.

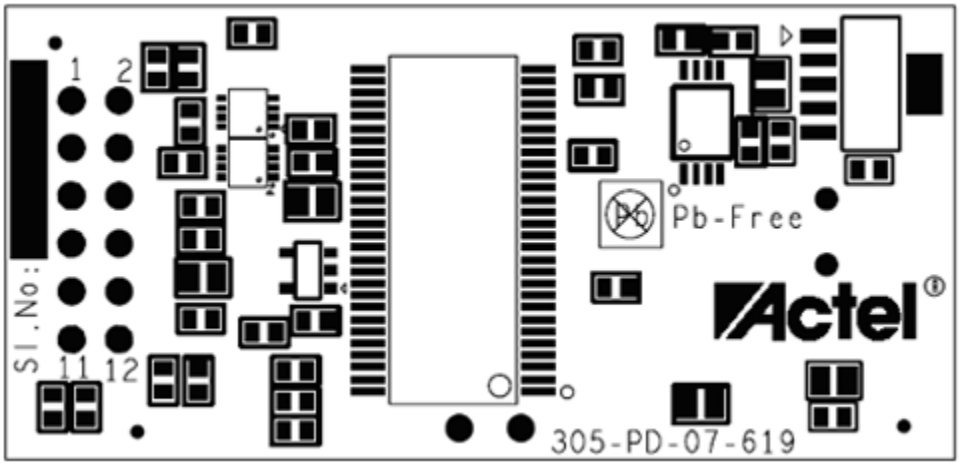

***Figure 1-20* • LCPS–Bottom Silkscreen**

You do not need to have the LCPS connected to the IGLOO Icicle board to operate the IGLOO Icicle board once the FPGA has been programmed. The IGLOO Icicle board only needs the LCPS connected when programming the IGLOO AGL125-QNG132.

2 – Using the IGLOO Icicle Evaluation Board

Programming the Board

To program a design into the IGLOO Icicle evaluation board:

1. Attach the LCPS board to the IGLOO Icicle evaluation board.
2. Attach a USB cable to the LCPS. This allows a programming data file, in program data base format (*.pdb) or STAPL format (*.stp), to be downloaded via the FlashPro software to the IGLOO AGL125-QNG132 device fitted to the board.
3. A separate USB connection is required for the IGLOO Icicle Board if the lithium ion rechargeable battery is not fully charged or if no other power source is attached to the IGLOO Icicle Board.

When using the FlashPro software, the programmer to select is the FlashPro3. The LCPS is functionally equivalent to a FlashPro programmer but designed specifically for use with the Icicle evaluation kit.

Power Sequencing

The ALG125 does not have any special power sequencing requirements.

Measuring Power

Once the IGLOO Icicle evaluation board is programmed and powered up, you can evaluate power usage by current consumption through the board.

Some key power advantages of the IGLOO FPGAs are:

- Flash*Freeze technology enables easy entry and exit from the static low power mode where IGLOO consumes as little as 5 µW (AGL030 die size) while retaining the contents of the system memory and data registers.
- Sleep (and shutdown) mode allows the IGLOO FPGA core power supply (or all power supplies) to be powered down when functionally is not required while the rest of the system remains powered.
- The user low static ICC macro (ULSICC) reduces IGLOO FPGA dynamic and static power consumption. The ULSICC macro, when enabled, disables the FlashROM, reducing the overall power of the device.

Table 2-1 gives a summary of the power modes available with IGLOO devices in general and is extracted from www.microsemi.com/soc/documents/IGLOO_UG.pdf.

Table 2-1 • **IGLOO Power Modes Summary**

Mode		VCCI	VCC	Core	Clocks	ULSICC Macro	To Enter Mode	To Resume Operation	Trigger
Active		On	On	On	On	N/A	Initiate clock	None	Trigger
Static	Idle	On	On	On	Off	N/A	Stock clock	Initiate clock	External
	Flash*Freeze type 1	On	On	On	On*	N/A	Assert FF pin	Deassert FF pin	External
	Flash*Freeze type 2	On	On	On	On*	Used to enter Flash*Freeze mode	Assert FF pin and assert LSICC	Deassert FF pin	External
Sleep		On	Off	Off	Off	N/A	Shut down VCC	Turn on VCC supply	External
Shutdown		Off	Off	Off	Off	N/A	Shut down VCC and VCCI supplies	Turn on VCC and VCCI supplies	External

*Note: *External clocks can be left toggling while the device is in Flash*Freeze mode. Clocks generated by the embedded PLL will be turned off automatically.*

Dynamic Power

Run the design with the oscillator enabled and the Flash*Freeze switch open (right most position of SW3).

Static Power

You need to disable the oscillator. No provision is made on the IGLOO Icicle Board for easily doing this without modifying components added to the board. However, it is possible to switch off the PLL circuits by removing the shunt across JP10, which will disconnect VCCPLF from the FPGA. This will not be true static power as the clock spine, within the FPGA, will still be toggling and current will be consumed. This is due to logic transitions taking place with charge and discharge of capacitors internal to the FPGA.

Standby Power

Keep the oscillator enabled and switch SW3 to the closed (left–most) position to put the device into Flash*Freeze mode.

To assist you, SW3 has additional labeling on the silkscreen with FF_ON appearing to the left of the switch and FF_OFF appearing to the right of the switch. The 3-pin header JP4 has a shunt that is normally placed across pins (2,3) to allow the Flash*Freeze signal to be provided by an external switch, in this case, SW3. When the shunt on JP4 is placed on pins (1,2), the Flash*Freeze signal is internally provided from GPIOB_1 IO100RSB1 from pin A14 of the QN132 packaged device. This allows you to experiment with type 1 and type 2 Flash*Freeze operation. Flash*Freeze type 2 uses the User Low Static ICC (ULSICC) macro to provide an internally generated Flash*Freeze signal.

Deep Sleep

An additional mode that is available with IGLOO silicon is the deep sleep mode; this is a low power mode when Flash*Freeze is asserted and the oscillator is disabled.

No provision has been made for exploring the deep sleep mode with the Icicle evaluation kit since there is no provision for disabling the oscillator. Typically an additional 1- 2 µA of core current can be saved by going into this deep sleep mode.

Design Example

The sample design included with the IGLOO Icicle Evaluation Kit CD allows you to quickly assess that the board is working. It allows you to see the operation of Flash*Freeze technology in preserving the system state of the design in a very low power "stand-by" mode of operation, typical of portable devices. If the lithium ion rechargeable battery is fully charged at this stage there is no need to have power applied to the USB connector.

The Icicle demo board is assembled with a Pictiva 96x16 Organic Light Emitting Diode (OLED). The OLED display has a controller chip (SSD1303) embedded in the assembly to simplify the user interface to the display. One of the functions of the AGL125 is to interface to OLED and give users the ability to display data or a custom message.

Figure 2-1 shows a high level functional block diagram of the OLED assembly.

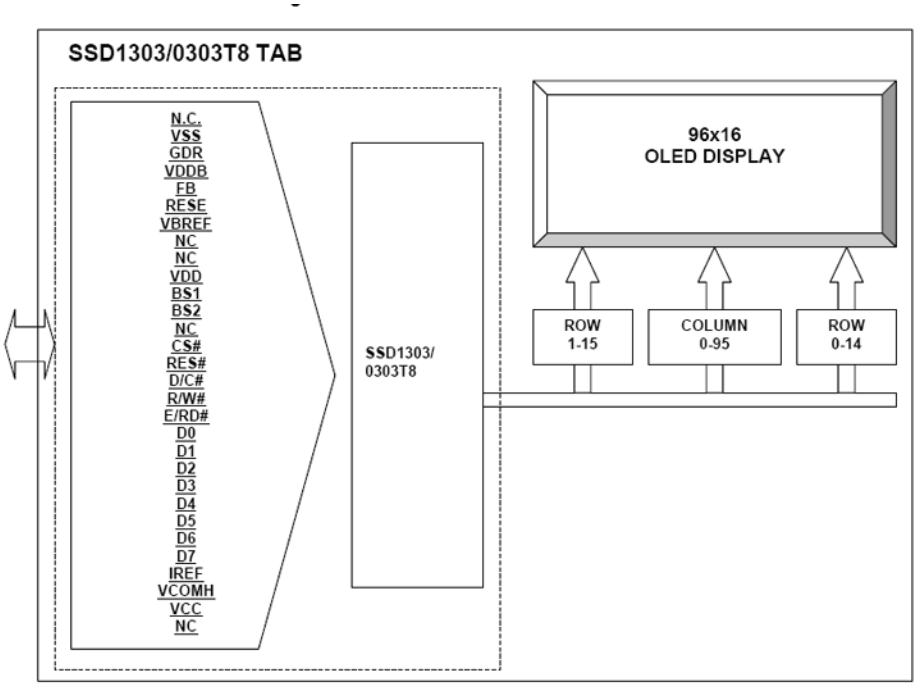

***Figure 2-1* • High Level OLED Functional Block Diagram**

Upon power up, the display will default to a random pattern. To display the message associated with the default design shipped with the Icicle Evaluation Kit, push SW1 to reset the board and then press SW5 to enable and initialize the display. The message IGLOO will be displayed. When SW5 is pushed a second time, the message will then scroll continuously across the display. At this point, any further pushing will have no affect on the display.

Once the message is scrolling, pushing SW1 will reset the board and freeze the message. To re-initialize the display, push SW5 once and to re-activate the scroll, push SW5 a second time.

If the Flash*Freeze mode is initiated while the display is active, the display retains its current state. At this point, the FPGA is no longer driving the display. Since the information has already been written to the OLED assembly, the display will continue to show the same message. Upon exiting the Flash*Freeze mode, the display will also retain its current state and function as described above.

The code developed to initialize and drive the display is comprised of three components:

- The control state machine PLL (pll_20_1)
- The oled_sm.vhd)
- The top level (icicle_top.vhd).

The PLL is used to derive internal clocks from the 20 MHz input clock on the board. The state machine contains all of the logic to initialize and drive the message described above onto the display. The top level ties everything together and also adds a counter of which the top bits are routed to LEDs D1-D3 for a quick indication that the FPGA is running.

The state machine design can be modified to alter the message that is displayed. The current design uses the parallel interface to the display. All of the initialization values are coded into the state machine and accessed after a board reset. The display used on the board has two banks that can be written to and are referred to as Bank0 and Bank1. Bank 0 corresponds to the upper 8 rows on the display and Bank1 the lower 8 rows.

Although the display is 96 columns wide, the buffer on the display is actually 132 wide. During the initialization process, all 132 columns for both banks are written with '0'. This is an important step, if not done when scrolling is enabled, the random data in columns 97 - 132 will be displayed. This data is coded into the design in two constant arrays, one for each bank. This data can be modified to change the display output, keeping in mind that each bit is controlling a pixel on the display.

Design Ideas and Sample Projects

Some ideas for some designs that you can implement on an IGLOO Icicle board are listed below.

Morse Code Flasher

Outline: Morse code is a sequence of dots and dashes with the dashes approximately three times the duration of a dot. Set up a design to interpret presses of one of the switches on the board to display the characters being pressed on the OLED display.

Key Point: You will need to measure the timing of various presses of a button using a counter. From that you will be able to decode the pressing of the switch so that you will be able to distinguish a single short press "." or "dit" from a long press "-" or "dah". A ".- " combination will be displayed as the letter "A". Establishing the speed of the dots will be important to correct decoding at various speeds.

Simple Hyperterminal on PC

Outline: Use the USB-UART interface on the IGLOO Icicle board to allow characters typed on the PC to be displayed on the OLED display. Allow the keys on the IGLOO Icicle board to switch something on the hyperterminal, e.g. enabling the CAPS lock on the PC or switching to a different font on the PC.

Key Point: Two-way communication.

Stock Ticker Display

Outline: Use the USB-UART interface on the IGLOO Icicle board to receive stock ticker information from a small applet running on the PC that is receiving a set of stock prices from the internet. The stock prices should be displayed on the OLED display of the IGLOO Icicle board as stock symbol, price, and change in price (positive preceded by "+" and negative preceded by "-").

Key Point: The change in price could be a percentage or an actual change. Try using one of the buttons on the board to supply a request to the PC to change the information from actual difference to percentage.

Note: The calculation of the conversion from actual difference to percentage is being done on the PC, not on the IGLOO Icicle board.

16-Key DTMF Oscillator Using Accessory Card (or USB-UART via PC)

Outline: Using an accessory card containing a 16-key keypad and a piezo-electric sounder, write an application to generate the two audio tones generated by a 16-key keypad. There is one tone for each row and one tone for each column. When a key is pressed, the tone for the row and the tone for the column should both be generated. The DTMF tones are listed in Figure 2-2 on page 29.

The frequencies are the same as used by regular telephone handsets. The far right column does not appear on regular telephones but exists on military phones and the tones are used by telephone companies to prioritize certain calls. If you only have a 12-key keypad, just generate the subset of the tones. For a short key press, the tones should be generated for approximately 100 ms with a 100 ms gap before the tone pair for the next key is generated. If a key is held longer, you can continue to generate the tone.

Key Point: All tones generated should be within ± 5% of the listed frequency. Consideration needs to be made of how to sum the two tones to be fed to the sounder. In American military telephones each of the right hand column keys was assigned a precedence code for routing of traffic; D was Priority or code "P", C was Immediate or code "O", B was Flash or code "F" and A was Flash Overide.

The A key and "Flash Overide" were not a precedence level as such, but were an operational extension to enable certain important calls to still get through the system if it was busy handling flash calls during an emergency.

Note: This project could also be done using a PC if an accessory board is not available. Use the PC to transfer the digits pressed to the IGLOO Icicle board via the USB-UART interface. A simple Hi Impedance crystal headset could be attached to the board to act as the sounder in one possible implementation of this project.

	1209 Hz	1336 Hz	1477 Hz	1633 Hz
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

***Figure 2-2* • DTMF Tones**

3 – List of Changes

The following table lists critical changes that were made in this revision of the User's Guide.

Date	Changes	Page
Revision 5 (February 2012)	Modified first paragraph of the "Introduction" section (SAR 36717).	3
	Modified "Kit Contents" and "Board Description" (SAR 36717).	5
	Modified "Rev D" section (SAR 36717).	12
	Modified text placed above Table 1-1 (SAR 36717).	15
Revision 4 (January 2012)	The title of the document was changed from *IGLOO Icicle Board User's Guide* to *IGLOO Icicle Evaluation Kit User's Guide*. Libero IDE was changed to Libero System-on-Chip (SoC) software.	N/A
Revision 3 (July 2011)	Figure 1-3 • Rev D IGLOO Icicle Board – Top Silkscreen was modified to point out JP5 and JP6 headers, and a note added for clarification (SAR 20914).	7
	Modified the "OLED Display Module" section (SAR 23884).	10
	Added Figure 1-8 • OLED Display Module Interconnects (Rev D boards) (SAR 23884).	11
	Modified the "Power Management" section and "Automatic Changeover Circuit" section (SAR 23884).	12
	Added Figure 1-11 • Automatic Switchover Circuit/USB Power Manager (Rev D Boards) (SAR 23884).	14
	Modified the "Hi–Voltage Supply for OLED Display" section (SAR 23884).	18
	Added Figure 1-17 • High-Voltage Power Supply Circuit (Rev D Boards) (SAR 23884).	19
	Modified the "Total Board Current Measurement" section (SAR 23884).	22

A – Board Stackup and Printed Layers

This Appendix contains the figures listed below. Revision B boards are located on the left side of the page and revision D boards are on the right side.

Figure A-1 on page 34 shows the top silkscreen where the FPGA is mounted.

Figure A-2 on page 35 shows layer 1 (or top) signal layer. The IGLOO AGL125 FPGA is mounted on this layer.

Figure A-3 on page 36 shows the layer 3 signal layer.

Figure A-4 on page 37 shows the layer 4 power plane.

Figure A-5 on page 38 shows the layer 6 signal layer.

Figure A-6 on page 39 shows the layer 8 (or bottom) signal layer and the bottom silkscreen.

Figure A-7 on page 40 shows a mirrored image of the previous images to make text readable.

Note: The ground planes are not shown. No information can be obtained from a printed version of those layers as they will print as solid black.

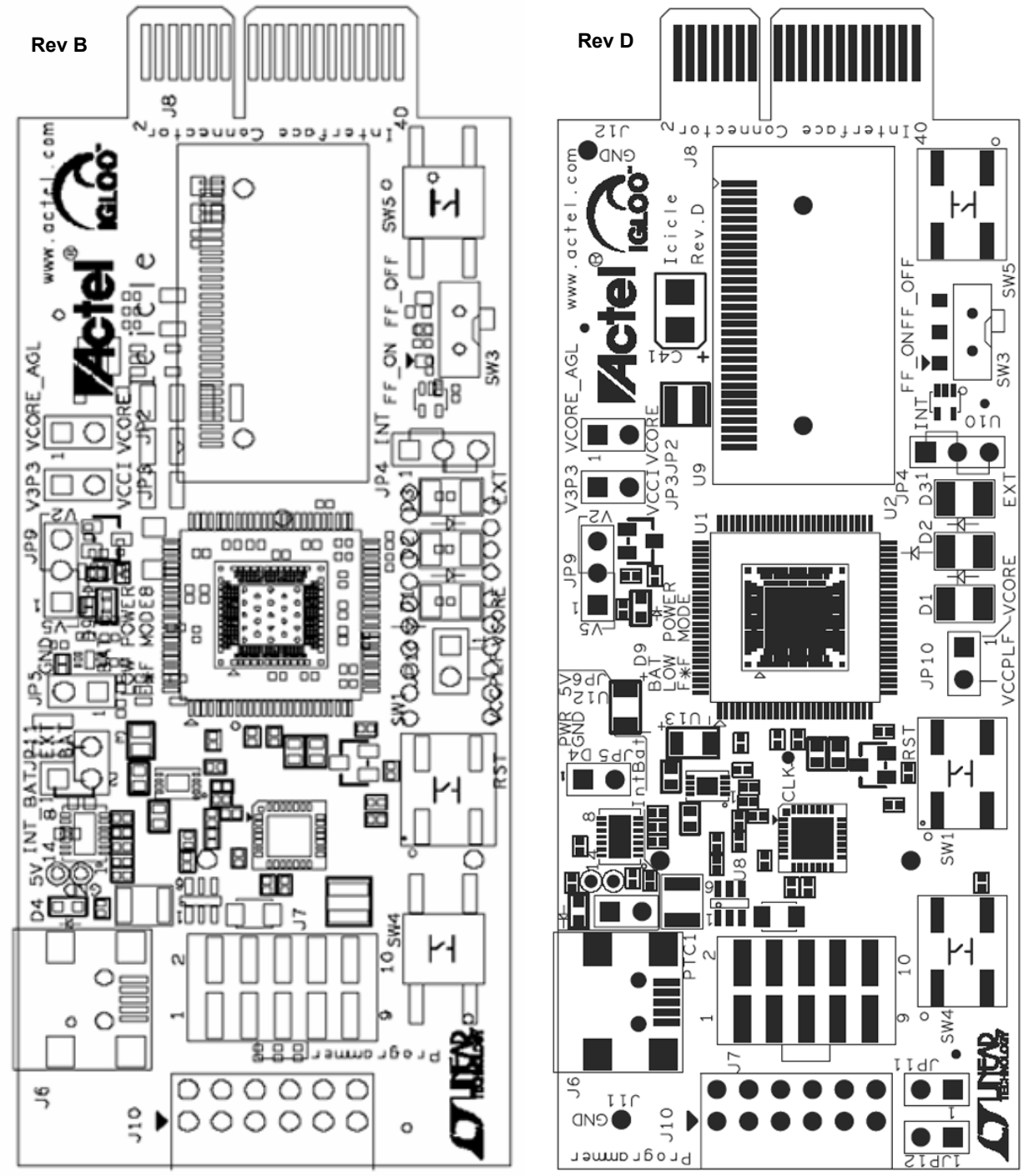

***Figure A-1* • Top Silkscreen (Rev B left, Rev D right)**

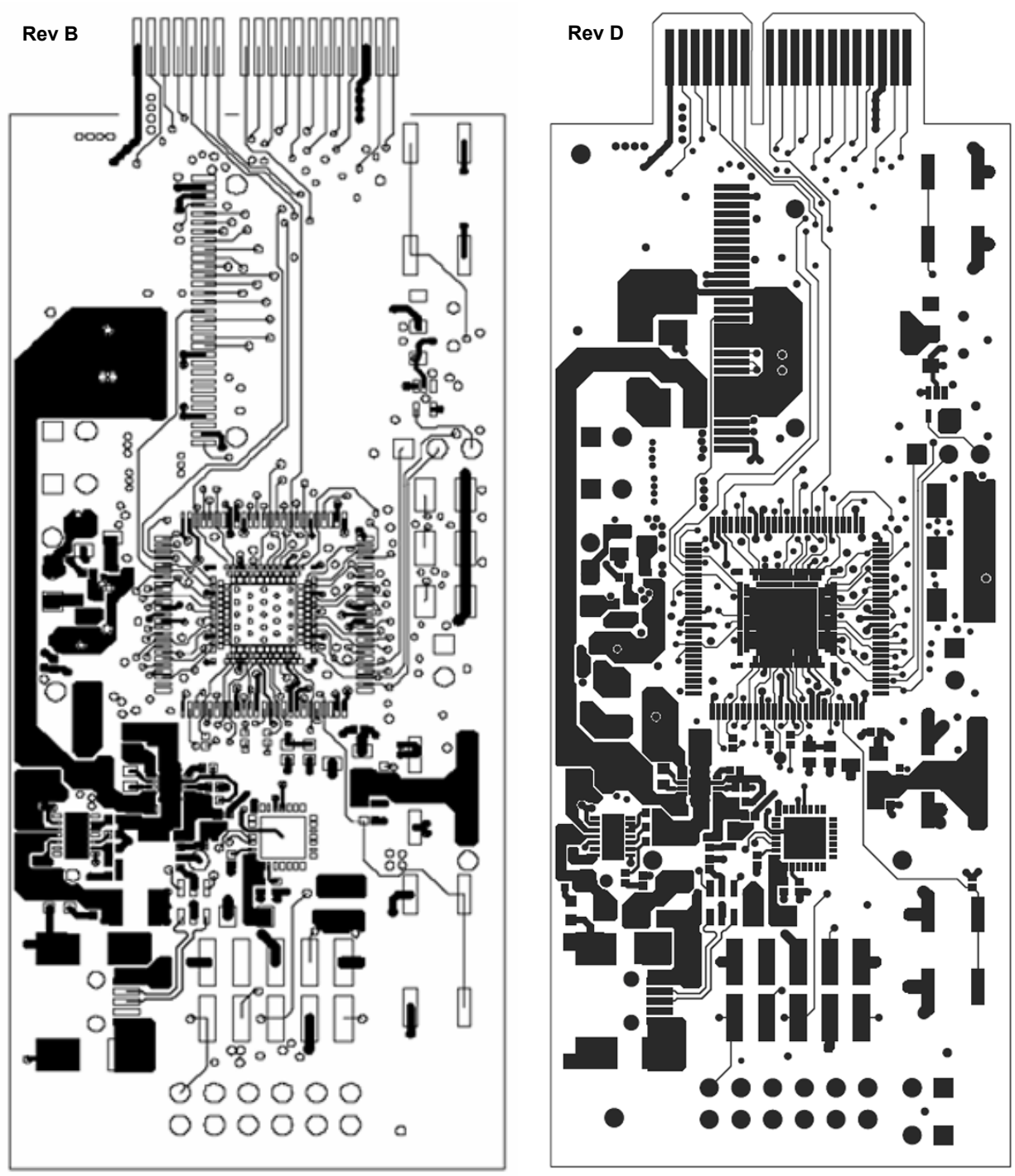

Figure A-2 **• Top Signal Layer (Rev B left, Rev D right)**

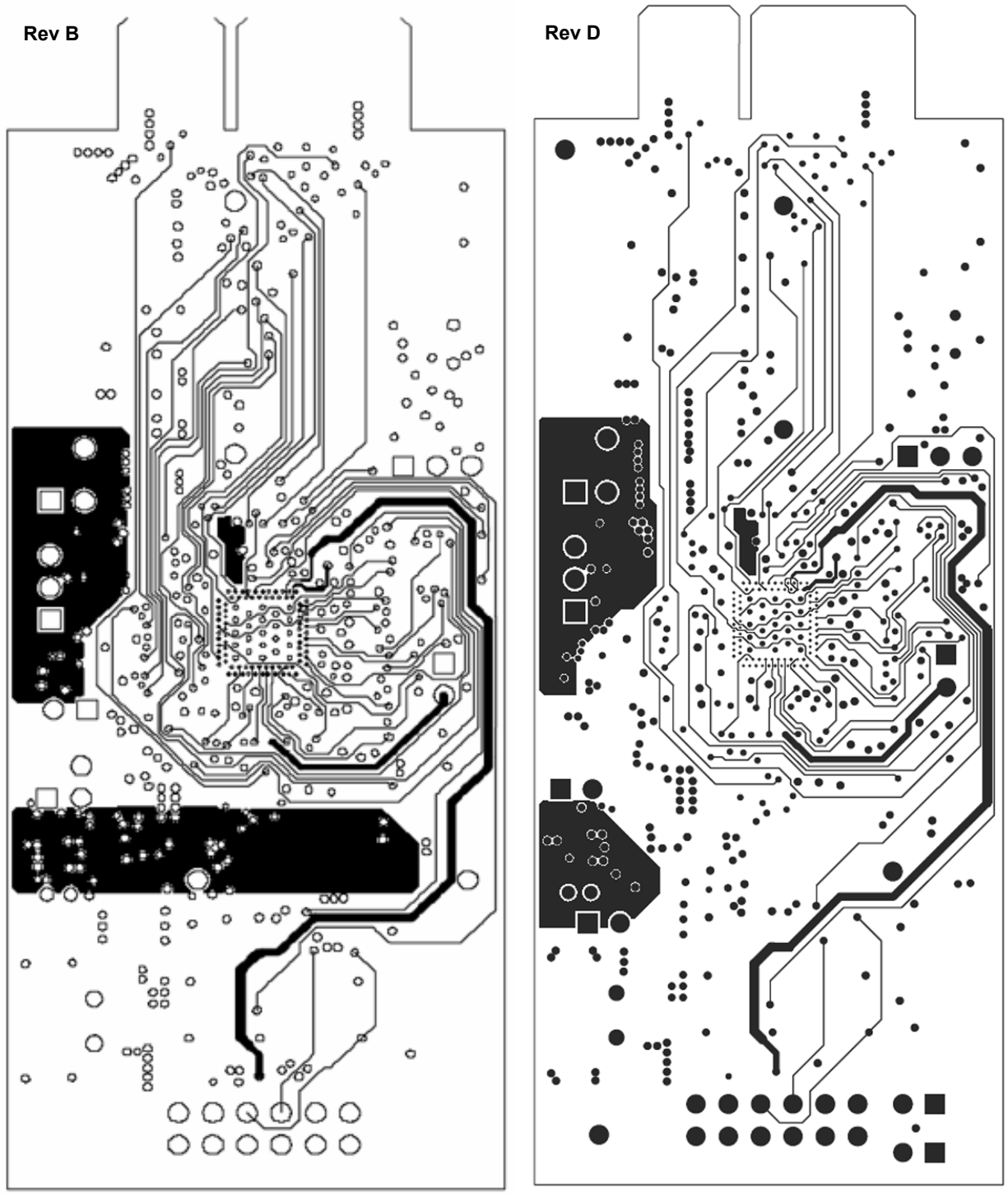

Figure A-3 **• Layer 3 – Signal Layer (Rev B left, Rev D right)**

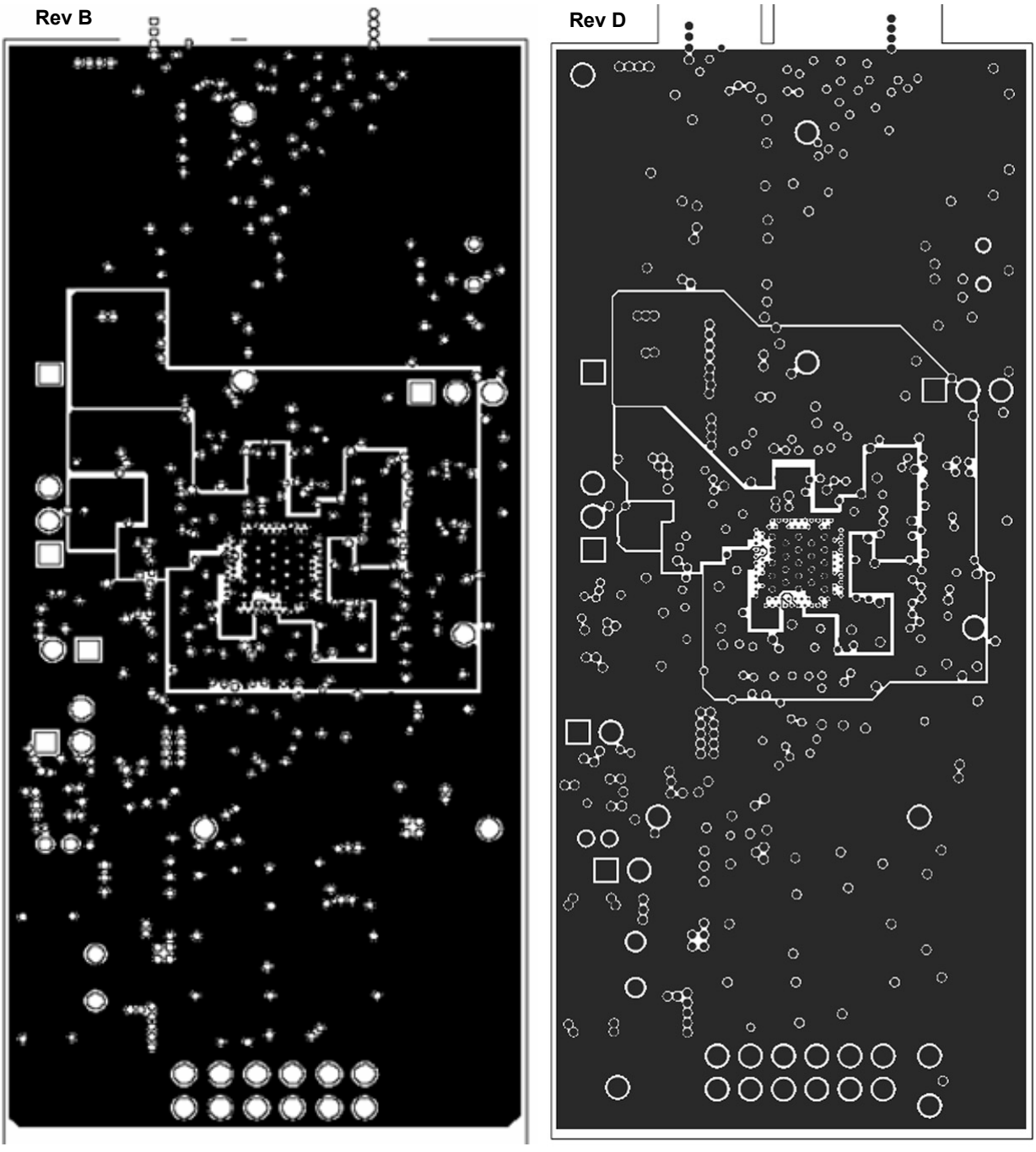

Figure A-4 **• Power Plane (Rev B left, Rev D right)**

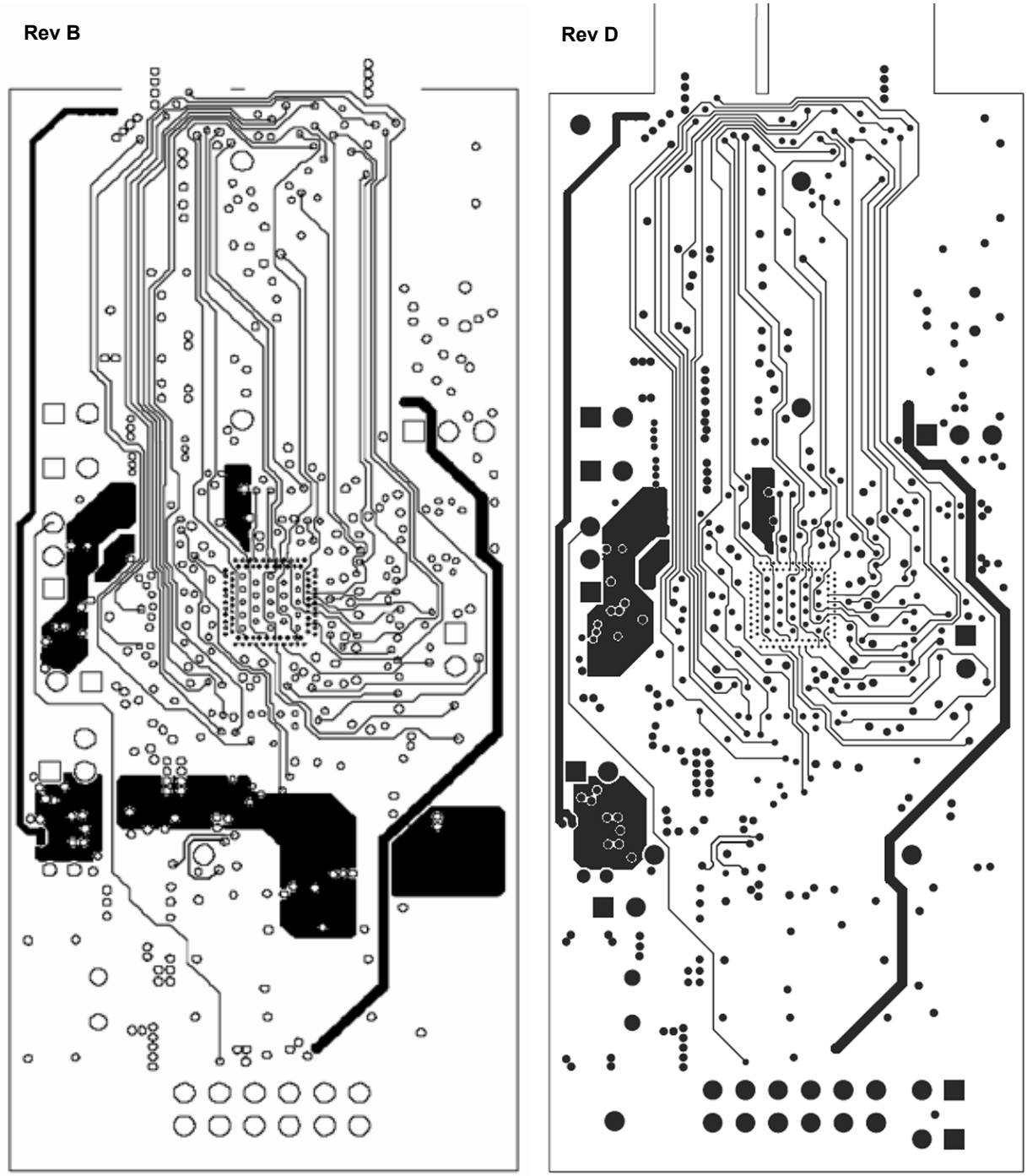

Figure A-5 **• Signal Layer – Layer 6 (Rev B left, Rev D right)**

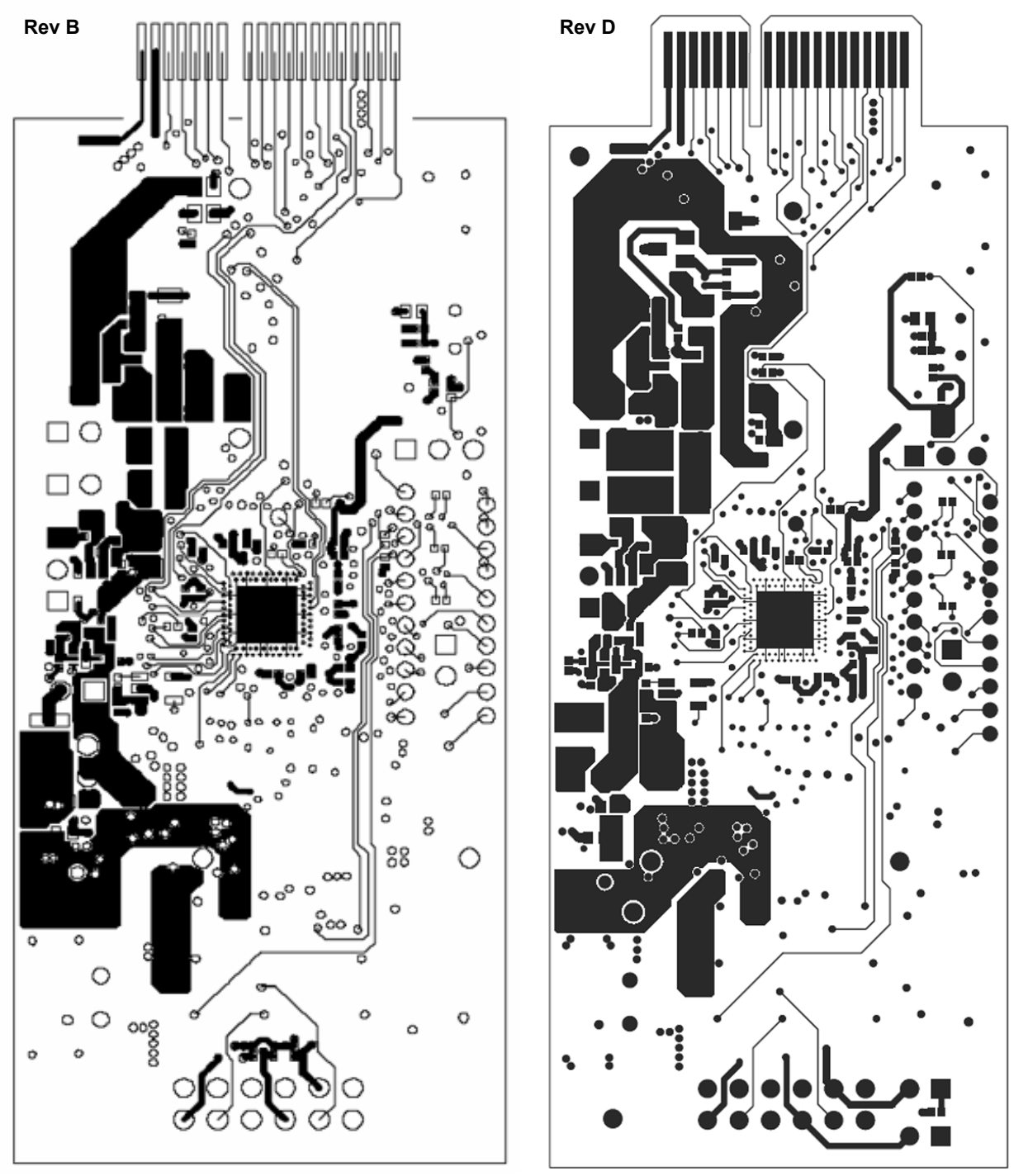

Figure A-6 **• Bottom Layer – Layer 8 (Rev B left, Rev D right)**

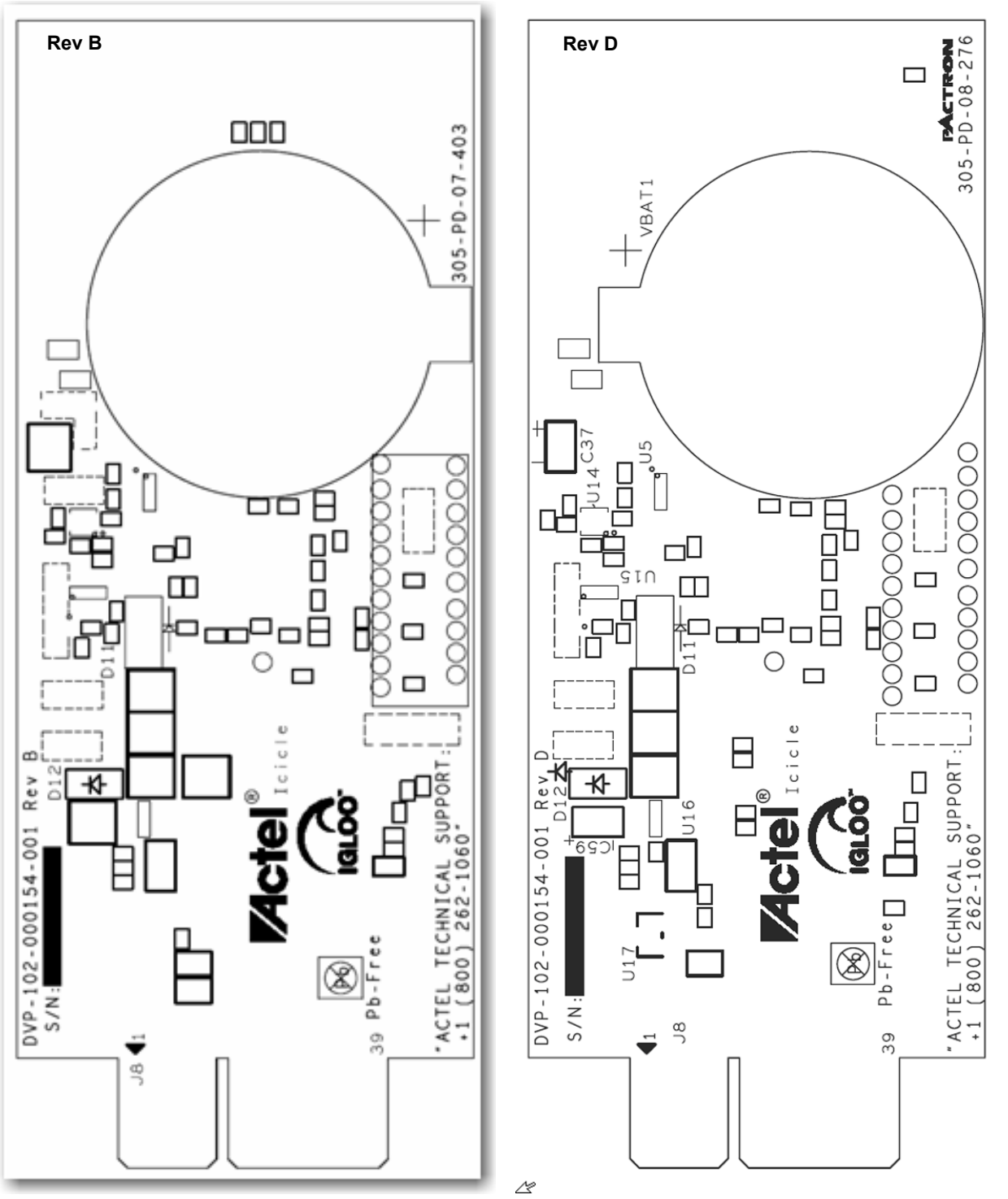

***Figure A-7* • Bottom Silkscreen (Rev B left, Rev D right)**

B – Sample Design AGL125-QNG132 Device

This Appendix provides a basic sample design for the AGL125-QNG132 device on the Rev B (green OLED) board. An alternative design is on the CD for the Rev D (blue OLED) board.

Note: Additional files are included in the FPGA design files directory on the IGLOO Icicle Evaluation Kit CD.

```
-- ICICLE_TOP.vhd

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity icicle_top is
    port (clock_20m     :   in  std_logic;                      -- 20 MHz input clock
          resetn        :   in  std_logic;                      -- active low board
reset, connected to sw1
          send_data     :   in  std_logic;                      -- connect to sw5
          led           :   out std_logic_vector(3 downto 1);          -- LED outputs
          -- DEBUG SIGNALs
          state_reg_out : out std_logic_vector(5 downto 0);
          clk_out       : out std_logic;
          idone_out     : out std_logic;

          -- OLED INTERFACE SIGNALS
          osram_resn    :   out std_logic;                      -- OLED reset signal
          osram_bs1     :   out std_logic;                      -- OLED comm mode
          osram_bs2     :   out std_logic;                      -- OLED comm mode
         osram_csn     :   out std_logic;                    -- active low chip select
          osram_d_c     :   out std_logic;                      -- data/command, 1 =
data, 0 = command
        osram_r_w    :   out std_logic;                  -- read write signal, 0 = write
          osram_e_rd    :   out std_logic;                      -- enable
          osram_d       :   out std_logic_vector(7 downto 0)    -- data output to oled
          -- UART SIGNALS
 --         uart_rx       : in  std_logic;
 --         uart_tx       : out std_logic
         );
end icicle_top;

architecture behav of icicle_top is

signal clock_1m  : std_logic;
signal send_data_sync   : std_logic;
signal send_data_sync1   : std_logic;
signal send_data_sync2   : std_logic;
signal send_data_sync3   : std_logic;
signal sw_cnt            : std_logic_vector(2 downto 0);
signal clock_500k        : std_logic;
signal clock_250k        : std_logic;
signal clock_125k        : std_logic;
signal count             : std_logic_vector(27 downto 0);

component PLL_20_1
    port(POWERDOWN  : in std_logic;
         CLKA       : in std_logic;
         LOCK       : out  std_logic;
         GLA        : out  std_logic
         );
end component;
```

```
component oled_sm
    port (clock_1m :   in  std_logic;                       -- 2 MHz input clock_2m to
state machine
          resetn:   in  std_logic;                      -- active low board reset
          led_int:    in  std_logic_vector(3 downto 1);
          send_data : in std_logic;
          -- DEBUG SIGNALS
          state_reg_out : out std_logic_vector(5 downto 0);
          idone_out     : out std_logic;

          -- OLED INTERFACE SIGNALS
          osram_resn  :   out std_logic;                    -- OLED reset signal
          osram_bs1   :   out std_logic;                    -- OLED comm mode
          osram_bs2   :   out std_logic;                    -- OLED comm mode
          osram_csn   :   out std_logic;                   -- active low chip select
         osram_d_c   :   out std_logic;                   -- data/command, 1 = data,
0 = command
        osram_r_w   :   out std_logic;                   -- read write signal, 0 = write
          osram_e_rd  :   out std_logic;                    -- enable
          osram_d     :   out std_logic_vector(7 downto 0)    -- data output to oled
         );
end component;

COMPONENT CLKBUF
    port(PAD    : in    STD_LOGIC;
         Y      : out   STD_LOGIC);
END COMPONENT;

--component JV_UART
--    port( resetn            : in    std_logic;                    -- system reset
--          clk             : in    std_logic;                   -- sm bus clock input
--          rx              : in    std_logic;                    -- sm bus data input
--          tx              : out   std_logic;                   -- sm bus data output
--          p_addr            : out   std_logic_vector( 7 downto 0);  -- SMBus address
recieved
--          p_cmnd            : out   std_logic_vector( 7 downto 0);  -- SMBus function
recieved
--         p_dout          : out   std_logic_vector(15 downto 0);  -- SMBus data recieved
--         p_pend          : out   std_logic;                  -- active high data pending
--          p_clear           : in    std_logic;                    -- active high
pending bit clear
--          m_addr            : out   std_logic_vector( 7 downto 0);  -- address for
memory access
--         p_din           : in    std_logic_vector(15 downto 0)   -- parallel data input
--);
--end component;



begin

clk_out <= clock_125k;

process(resetn, send_data_sync)
    begin
        if (resetn = '0') then
            sw_cnt <= "000";
        elsif rising_edge (send_data_sync) then
            sw_cnt <= sw_cnt + "001";
        end if;
end process;

led(1)  <= count(27);
led(2)  <= count(26);
```

```
led(3)  <= count(25);

counter: process(resetn, clock_20m)
    begin
        if (resetn = '0') then
            count   <= x"0000000";
        elsif rising_edge(clock_20m) then
            count    <= count + '1';
        end if;
end process counter;


PLL_20_1_inst   :   PLL_20_1
    port map (POWERDOWN => '1',
              CLKA      => clock_20m,
              LOCK      => open,
              GLA       => clock_1m
             );

half_clk1: process (resetn, clock_1m)
    begin
        if (resetn = '0') then
            clock_500k <= '0';
        elsif rising_edge(clock_1m) then
            clock_500k <= not clock_500k;
        end if;
end process half_clk1;

half_clk2: process (resetn, clock_500k)
    begin
        if (resetn = '0') then
            clock_250k <= '0';
        elsif rising_edge(clock_500k) then
            clock_250k <= not clock_250k;
        end if;
end process half_clk2;

half_clk3: process (resetn, clock_250k)
    begin
        if (resetn = '0') then
            clock_125k <= '0';
        elsif rising_edge(clock_250k) then
            clock_125k <= not clock_125k;
        end if;
end process half_clk3;

oled_sm_inst    :   oled_sm
    port map ( clock_1m    => clock_125k,
               resetn      => resetn,
               state_reg_out    => state_reg_out,
               idone_out    => idone_out,
               osram_resn  => osram_resn,
               led_int   => sw_cnt,
               send_data   => send_data_sync,
               osram_bs1   => osram_bs1,
               osram_bs2   => osram_bs2,
               osram_csn   => osram_csn,
               osram_d_c   => osram_d_c,
               osram_r_w   => osram_r_w,
               osram_e_rd  => osram_e_rd,
               osram_d     => osram_d
              );

sync:process (resetn, clock_125k)
```

```
    begin
        if (resetn = '0') then
            send_data_sync1 <= '1';
            send_data_sync2 <= '1';
            send_data_sync3 <= '1';
        elsif rising_edge (clock_125k) then
            send_data_sync1  <= send_data;
            send_data_sync2  <= send_data_sync1;
            send_data_sync3  <= send_data_sync2;
        end if;
end process sync;

send_data_sync  <= not(not send_data_sync3 and not send_data_sync2 and not
send_data_sync1);


--JV_UART_inst : JV_UART
--port map( resetn       => resetn,
--          clk          => clock_20m,
--          rx           => uart_rx,
--          tx           => uart_tx,
--          p_addr       => smb_addr,   -- recieved address
--          p_cmnd       => smb_cmnd,   -- recieved command
--          p_dout       => smb_data,   -- recieved data
--          p_pend       => smb_pend,   -- data pending
--          p_clear      => smb_clear,  -- p_pend bit clear
--          m_addr       => sm_addr,    -- read address
--          p_din        => sm_data     -- data from dmem or nvm
--);
--

end behav;
```

Additional files that will be of interest are included in the FPGA design files directory on the IGLOO Icicle Kit CD. These files are provided so that you can completely recompile the design yourself.

- VHDL driver for the OLED display
- OLED_SM.vhd

C – AGL125-QNG132 Pin Connections

This Appendix provides pin out tables that list the FPGA pins that are connect to board peripherals. Table C-1 is sorted by pin numbers.

***Table C-1* • AGL125-QNG132 Pin Connections—Sorted by Pin Number**

Pin Number	Pin Name	Icicle Evaluation Kit Function	Notes
A1	GAB2/IO69RSB1	GPIOA_1	Connects to Pin 5 of J8
A2	IO130RSB1	GPIOA_22	Connects to Pin 24 of J8
A3	VCCIB1	VCCI	Connects to Pin 2 of JP3
A4	GFC1/IO126RSB1	GPIOA_25	Connects to Pin 29 of J8
A5	GFB0/IO123RSB1	OSC_CLK	Output of oscillator
A6	VCCPLF	VCCPLF	Connects to Pin 2 of JP10
A7	GFA1/IO121RSB1	GPIOA_4	Connects to Pin 6 of J8
A8	GFC2/IO118RSB1	TP31	GPIO to test point
A9	IO115RSB1	TP19	GPIO to test point
A10	VCC	VCC	Connects to Pin 2 of JP2
A11	GEB1/IO110RSB1	GPIOA_6	Connects to Pin 8 of J8
A12	GEA0/IO107RSB1	NC	No connection
A13	GEC2/IO104RSB1	SWITCH5	Connects to Pins (2, 4) of SW5
A14	IO100RSB1	GPIOB_1	
A15	VCC	VCC	Connects to Pin 2 of JP2
A16	IO99RSB1	GPIOA_23	Connects to Pin 27 of J8
A17	IO96RSB1	LED1	Connects to D1
A18	IO94RSB1	LED3	Connects to D3
A19	IO91RSB1	TP20	GPIO to test point
A20	IO85RSB1	GPIOA_27	Connects to Pin 31 of J8
A21	IO79RSB1	GPIOA_28	Connects to Pin 30 of J8
A22	VCC	VCC	Connects to Pin 2 of JP2
A23	GDB2/IO71RSB1	GPIOA_8	Connects to Pin 10 of J8
A24	TDI	TDI	Connects to Pin 6 of J10
A25	TRST	TRST	Connects to Pin 8 of J10

***Table C-1* • AGL125-QNG132 Pin Connections—Sorted by Pin Number (continued)**

Pin Number	Pin Name	Icicle Evaluation Kit Function	Notes
A26	GDC1/IO61RSB0	GPIOA_10	Connects to Pin 12 of J8
A27	VCC	VCC	Connects to Pin 2 of JP2
A28	IO60RSB0	GPIOA_34	Connects to Pin 38 of J8
A29	GCC2/IO59RSB0	TP8	GPIO to test point
A30	GCA2/IO57RSB0	TP27	GPIO to test point
A31	GCA0/IO56RSB0	GPIOA_12	
A32	GCB1/IO53RSB0	TP28	GPIO to test point
A33	IO49RSB0	NC	No connection
A34	VCC	VCC	Connects to Pin 2 of JP2
A35	IO44RSB0	GPIOA_29	Connects to Pin 33 of J8
A36	GBA2/IO41RSB0	GPIOA_17	Connects to Pin 21 of J8
A37	GBB1/IO38RSB0	GPIOA_18	Connects to Pin 20 of J8
A38	GBC0/IO35RSB0	OSRAM_RES#	Connects to Pin 16 of OLED
A39	VCCIB0	VCCI	Connects to Pin 2 of JP3
A40	IO28RSB0	OSRAM_D4	Connects to Pin 24 of OLED
A41	IO22RSB0	OSRAM_D5	Connects to Pin 25 of OLED
A42	IO18RSB0	TP13	GPIO to test point
A43	IO14RSB0	TP14	GPIO to test point
A44	IO11RSB0	GPIO_36	Connects to Pin 40 of J8
A45	IO07RSB0	OSRAM_BS1	Connects to Pin 12 of OLED
A46	VCC	VCC	Connects to Pin 2 of JP2
A47	GAC1/IO05RSB0	OSRAM_BS2	Connects to Pin 13 of OLED
A48	GAB0/IO02RSB0	OSRAM_E/RD#	Connects to Pin 19 of OLED
B1	IO68RSB1	GPIOA_20	Connects to Pin 22 of J8
B2	GAC2/IO131RSB1	GPIOA_26	Connects to Pin 28 of J8
B3	GND	GND	
B4	GFC0/IO125RSB1	TP32	GPIO to test point
B5	VCOMPLF	GND	
B6	GND	GND	
B7	GFB2/IO119RSB1	TP33	GPIO to test point

***Table C-1* • AGL125-QNG132 Pin Connections—Sorted by Pin Number (continued)**

Pin Number	Pin Name	Icicle Evaluation Kit Function	Notes
B8	IO116RSB1	TP34	GPIO to test point
B9	GND	GND	
B10	GEB0/IO109RSB1	GPIOA_7	Connects to Pin 11 of J8
B11	VMV1	VCCI	Connects to Pin 2 of JP3
B12	FF/GEB2/IO105RSB1	IGLOO_FF	Connects to Pin 2 of JP4
B13	IO101RSB1	TP21	GPIO to test point
B14	GND	GND	
B15	IO98RSB1	TP22	GPIO to test point
B16	IO95RSB1	LED2	Connects to D2
B17	GND	GND	
B18	IO87RSB1	OSRAM_D1	Connects to Pin 21 of OLED
B19	IO81RSB1	OSRAM_D2	Connects to Pin 22 of OLED
B20	GND	GND	
B21	GNDQ	GND	
B22	TMS	TMS	Connects to Pin 3 of J10
B23	TDO	TDO	Connects to Pin 9 of J10
B24	GDC0/IO62RSB0	GPIOA_9	Connects to Pin 13 of J8
B25	GND	GND	
B26	NC	NC	No connection
B27	GCB2/IO58RSB0	GPIOA_11	No connection
B28	GND	GND	
B29	GCB0/IO54RSB0	TP29	GPIO to test point
B30	GCC1/IO51RSB0	GPIOA_15	Connects to Pin 19 of J8
B31	GND	GND	
B32	GBB2/IO43RSB0	GPIOA_16	Connects to Pin 18 of J8
B33	VMV0	VCCI	Connects to Pin 2 of JP3
B34	GBA0/IO39RSB0	AGL_UART_TXD	Connects to RXD Pin 25 of U7
B35	GBC1/IO36RSB0	OSRAM_CS#	Connects to Pin 15 of OLED
B36	GND	GND	
B37	IO26RSB0	GPIOA_30	Connects to Pin 32 of J8

***Table C-1* • AGL125-QNG132 Pin Connections—Sorted by Pin Number (continued)**

Pin Number	Pin Name	Icicle Evaluation Kit Function	Notes
B38	IO21RSB0	TP15	GPIO to test point
B39	GND	GND	
B40	IO13RSB0	OSRAM_D7	Connects to Pin 27 of OLED
B41	IO08RSB0	TP16	GPIO to test point
B42	GND	GND	
B43	GAC0/IO04RSB0	OSRAM_D/C#	Connects to Pin 17 of OLED
B44	GNDQ	GND	
C1	GAA2/IO67RSB1	PBRESET_N	Connects to Pins (2, 4) of SW1
C2	IO132RSB1	GPIOA_21	
C3	VCC	Vcc	Connects to Pin 2 of JP2
C4	GFB1/IO124RSB1	GPIOA_2	Connects to Pin 4 of J8
C5	GFA0/IO122RSB1	GPIOA_3	Connects to Pin 7 of J8
C6	GFA2/IO120RSB1	GPIOA_5	Connects to Pin 9 of J8
C7	IO117RSB1	TP23	GPIO to test point
C8	VCCIB1	VCCI	Connects to Pin 2 of JP3
C9	GEA1/IO108RSB1	SWITCH4	Connects to Pins (2, 4) of SW4
C10	GNDQ	GND	
C11	GEA2/IO106RSB1	NC	No connection
C12	IO103RSB1	GPIOA_33	Connects to Pin 37 of J8
C13	VCCIB1	VCCI	Connects to Pin 2 of JP3
C14	IO97RSB1	GPIOA_24	Connects to Pin 26 of J8
C15	IO93RSB1	OSRAM_D0	Connects to Pin 20 of OLED
C16	IO89RSB1	TP25	GPIO to test point
C17	IO83RSB1	GPIOA_35	Connects to Pin 39 of J8
C18	VCCIB1	VCCI	Connects to Pin 2 of JP3
C19	TCK	TCK	Connects to Pin 2 of J10
C20	VMV1	VCCI	Connects to Pin 2 of JP3
C21	VPUMP	VPUMP	Connects to Pin 10 of J10
C22	VJTAG	VJTAG	Connects to Pin 7 of J10
C23	VCCIB0	VCCI	Connects to Pin 2 of JP3

***Table C-1* • AGL125-QNG132 Pin Connections—Sorted by Pin Number (continued)**

Pin Number	Pin Name	Icicle Evaluation Kit Function	Notes
C24	NC	NC	No connection
C25	NC	NC	No connection
C26	GCA1/IO55RSB0	GPIOA_13	Connects to Pin 17 of J8
C27	GCC0/IO52RSB0	GPIOA_14	No connection
C28	VCCIB0	VCCI	Connects to Pin 2 of JP3
C29	IO42RSB0	OSRAM_D3	Connects to Pin 23 of OLED
C30	GNDQ	GND	
C31	GBA1/IO40RSB0	AGL_UART_RXD	Connects to TXD Pin 26 of U7
C32	GBB0/IO37RSB0	GPIOA_19	Connects to Pin 23 of J8
C33	VCC	VCC	Connects to Pin 2 of JP2
C34	IO24RSB0	TP17	GPIO to test point
C35	IO19RSB0	OSRAM_D6	Connects to Pin 26 of OLED
C36	IO16RSB0	GPIOA_31	Connects to Pin 35 of J8
C37	IO10RSB0	GPIOA_32	Connects to Pin 34 of J8
C38	VCCIB0	VCCI	Connects to Pin 2 of JP2
C39	GAB1/IO03RSB0	OSRAM_R/W#	Connects to Pin 18 of OLED
C40	VMV0	VCCI	Connects to Pin 2 of JP3
D1	GND	GND	
D2	GND	GND	
D3	GND	GND	
D4	GND	GND	

Table C-2 is sorted by kit function.

***Table C-2* • AGL125-QNG132 Pin Connections—Sorted by Kit Function**

Icicle Kit Function	Pin Number	Pin Name	Notes
AGL_UART_RXD	C31	GBA1/IO40RSB0	Connects to TXD Pin 26 of U7
AGL_UART_TXD	B34	GBA0/IO39RSB0	Connects to RXD Pin 25 of U7
GND	B3	GND	
GND	B5	VCOMPLF	
GND	B6	GND	
GND	B9	GND	
GND	B14	GND	
GND	B17	GND	
GND	B20	GND	
GND	B21	GNDQ	
GND	B25	GND	
GND	B28	GND	
GND	B31	GND	
GND	B36	GND	
GND	B39	GND	
GND	B42	GND	
GND	B44	GNDQ	
GND	C10	GNDQ	
GND	C30	GNDQ	
GND	D1	GND	
GND	D2	GND	
GND	D3	GND	
GND	D4	GND	
GPIO_36	A44	IO11RSB0	Connects to Pin 40 of J8
GPIOA_1	A1	GAB2/IO69RSB1	Connects to Pin 5 of J8
GPIOA_2	C4	GFB1/IO124RSB1	Connects to Pin 4 of J8
GPIOA_3	C5	GFA0/IO122RSB1	Connects to Pin 7 of J8
GPIOA_4	A7	GFA1/IO121RSB1	Connects to Pin 6 of J8
GPIOA_5	C6	GFA2/IO120RSB1	Connects to Pin 9 of J8

Table C-2 • **AGL125-QNG132 Pin Connections—Sorted by Kit Function (continued)**

Icicle Kit Function	Pin Number	Pin Name	Notes
GPIOA_6	A11	GEB1/IO110RSB1	Connects to Pin 8 of J8
GPIOA_7	B10	GEB0/IO109RSB1	Connects to Pin 11 of J8
GPIOA_8	A23	GDB2/IO71RSB1	Connects to Pin 10 of J8
GPIOA_9	B24	GDC0/IO62RSB0	Connects to Pin 13 of J8
GPIOA_10	A26	GDC1/IO61RSB0	Connects to Pin 12 of J8
GPIOA_11	B27	GCB2/IO58RSB0	No connection
GPIOA_12	A31	GCA0/IO56RSB0	
GPIOA_13	C26	GCA1/IO55RSB0	Connects to Pin 17 of J8
GPIOA_14	C27	GCC0/IO52RSB0	No connection
GPIOA_15	B30	GCC1/IO51RSB0	Connects to Pin 19 of J8
GPIOA_16	B32	GBB2/IO43RSB0	Connects to Pin 18 of J8
GPIOA_17	A36	GBA2/IO41RSB0	Connects to Pin 21 of J8
GPIOA_18	A37	GBB1/IO38RSB0	Connects to Pin 20 of J8
GPIOA_19	C32	GBB0/IO37RSB0	Connects to Pin 23 of J8
GPIOA_20	B1	IO68RSB1	Connects to Pin 22 of J8
GPIOA_21	C2	IO132RSB1	
GPIOA_22	A2	IO130RSB1	Connects to Pin 24 of J8
GPIOA_23	A16	IO99RSB1	Connects to Pin 27 of J8
GPIOA_24	C14	IO97RSB1	Connects to Pin 26 of J8
GPIOA_25	A4	GFC1/IO126RSB1	Connects to Pin 29 of J8
GPIOA_26	B2	GAC2/IO131RSB1	Connects to Pin 28 of J8
GPIOA_27	A20	IO85RSB1	Connects to Pin 31 of J8
GPIOA_28	A21	IO79RSB1	Connects to Pin 30 of J8
GPIOA_29	A35	IO44RSB0	Connects to Pin 33 of J8
GPIOA_30	B37	IO26RSB0	Connects to Pin 32 of J8
GPIOA_31	C36	IO16RSB0	Connects to Pin 35 of J8
GPIOA_32	C37	IO10RSB0	Connects to Pin 34 of J8
GPIOA_33	C12	IO103RSB1	Connects to Pin 37 of J8
GPIOA_34	A28	IO60RSB0	Connects to Pin 38 of J8
GPIOA_35	C17	IO83RSB1	Connects to Pin 39 of J8

Table C-2 • **AGL125-QNG132 Pin Connections—Sorted by Kit Function (continued)**

Icicle Kit Function	Pin Number	Pin Name	Notes
GPIOB_1	A14	IO100RSB1	
IGLOO_FF	B12	FF/GEB2/IO105RSB1	Connects to Pin 2 of JP4
LED1	A17	IO96RSB1	Connects to D1
LED2	B16	IO95RSB1	Connects to D2
LED3	A18	IO94RSB1	Connects to D3
NC	A12	GEA0/IO107RSB1	No connection
NC	A33	IO49RSB0	No connection
NC	B26	NC	No connection
NC	C11	GEA2/IO106RSB1	No connection
NC	C24	NC	No connection
NC	C25	NC	No connection
OSC_CLK	A5	GFB0/IO123RSB1	Output of oscillator
OSRAM_BS1	A45	IO07RSB0	Connects to Pin 12 of OLED
OSRAM_BS2	A47	GAC1/IO05RSB0	Connects to Pin 13 of OLED
OSRAM_CS#	B35	GBC1/IO36RSB0	Connects to Pin 15 of OLED
OSRAM_D/C#	B43	GAC0/IO04RSB0	Connects to Pin 17 of OLED
OSRAM_D0	C15	IO93RSB1	Connects to Pin 20 of OLED
OSRAM_D1	B18	IO87RSB1	Connects to Pin 21 of OLED
OSRAM_D2	B19	IO81RSB1	Connects to Pin 22 of OLED
OSRAM_D3	C29	IO42RSB0	Connects to Pin 23 of OLED
OSRAM_D4	A40	IO28RSB0	Connects to Pin 24 of OLED
OSRAM_D5	A41	IO22RSB0	Connects to Pin 25 of OLED
OSRAM_D6	C35	IO19RSB0	Connects to Pin 26 of OLED
OSRAM_D7	B40	IO13RSB0	Connects to Pin 27 of OLED
OSRAM_D7	B40	IO13RSB0	Connects to Pin 27 of OLED
OSRAM_E/RD#	A48	GAB0/IO02RSB0	Connects to Pin 19 of OLED
OSRAM_R/W#	C39	GAB1/IO03RSB0	Connects to Pin 18 of OLED
OSRAM_RES#	A38	GBC0/IO35RSB0	Connects to Pin 16 of OLED
PBRESET_N	C1	GAA2/IO67RSB1	Connects to Pins (2, 4) of SW1
SWITCH4	C9	GEA1/IO108RSB1	Connects to Pins (2, 4) of SW4

Table C-2 • **AGL125-QNG132 Pin Connections—Sorted by Kit Function (continued)**

Icicle Kit Function	Pin Number	Pin Name	Notes
SWITCH5	A13	GEC2/IO104RSB1	Connects to Pins (2, 4) of SW5
TCK	C19	TCK	Connects to Pin 2 of J10
TDI	A24	TDI	Connects to Pin 6 of J10
TDO	B23	TDO	Connects to Pin 9 of J10
TMS	B22	TMS	Connects to Pin 3 of J10
TP13	A42	IO18RSB0	GPIO to test point
TP14	A43	IO14RSB0	GPIO to test point
TP15	B38	IO21RSB0	GPIO to test point
TP16	B41	IO08RSB0	GPIO to test point
TP17	C34	IO24RSB0	GPIO to test point
TP19	A9	IO115RSB1	GPIO to test point
TP20	A19	IO91RSB1	GPIO to test point
TP21	B13	IO101RSB1	GPIO to test point
TP22	B15	IO98RSB1	GPIO to test point
TP23	C7	IO117RSB1	GPIO to test point
TP25	C16	IO89RSB1	GPIO to test point
TP27	A30	GCA2/IO57RSB0	GPIO to test point
TP28	A32	GCB1/IO53RSB0	GPIO to test point
TP29	B29	GCB0/IO54RSB0	GPIO to test point
TP31	A8	GFC2/IO118RSB1	GPIO to test point
TP32	B4	GFC0/IO125RSB1	GPIO to test point
TP33	B7	GFB2/IO119RSB1	GPIO to test point
TP34	B8	IO116RSB1	GPIO to test point
TP8	A29	GCC2/IO59RSB0	GPIO to test point
TRST	A25	TRST	Connects to Pin 8 of J10
Vcc	A10	VCC	Connects to Pin 2 of JP2
Vcc	A15	VCC	Connects to Pin 2 of JP2
Vcc	A22	VCC	Connects to Pin 2 of JP2
Vcc	A27	VCC	Connects to Pin 2 of JP2
Vcc	A34	VCC	Connects to Pin 2 of JP2

Table C-2 • **AGL125-QNG132 Pin Connections—Sorted by Kit Function (continued)**

Icicle Kit Function	Pin Number	Pin Name	Notes
VCC	A46	VCC	Connects to Pin 2 of JP2
VCC	C3	VCC	Connects to Pin 2 of JP2
VCC	C33	VCC	Connects to Pin 2 of JP2
VCCI	A3	VCCIB1	Connects to Pin 2 of JP3
VCCI	A39	VCCIB0	Connects to Pin 2 of JP3
VCCI	B11	VMV1	Connects to Pin 2 of JP3
VCCI	B33	VMV0	Connects to Pin 2 of JP3
VCCI	C8	VCCIB1	Connects to Pin 2 of JP3
VCCI	C13	VCCIB1	Connects to Pin 2 of JP3
VCCI	C18	VCCIB1	Connects to Pin 2 of JP3
VCCI	C20	VMV1	Connects to Pin 2 of JP3
VCCI	C23	VCCIB0	Connects to Pin 2 of JP3
VCCI	C28	VCCIB0	Connects to Pin 2 of JP3
VCCI	C38	VCCIB0	Connects to Pin 2 of JP2
VCCI	C40	VMV0	Connects to Pin 2 of JP3
VCCPLF	A6	VCCPLF	Connects to Pin 2 of JP10
VJTAG	C22	VJTAG	Connects to Pin 7 of J10
VPUMP	C21	VPUMP	Connects to Pin 10 of J10

D – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 650.318.8044

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

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