UG0208
User Guide
SmartFusion Development Kit

Microsemi
Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 7.1

The following is a summary of the changes in revision 7.1 of this document.

- Libero SoC software license information was updated from Gold to Silver. For more information, see Software Installation, page 7.
- Component description, connection section of OLED, OLED manufacturing test, and board image are updated.

1.2 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- The part number of the kit was changed from A2F500-DEV-KIT to A2F500-DEV-KIT-2 throughout the document (SAR 43384).
- The OLED DISPLAY component in the development kit was updated from "blue OLED PMO13701" to "white OLED PMO18701" (SAR 43382).

1.3 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Modified Figure 1, page 3 (SAR 35559)
- Modified Table 3, page 8 (SAR 35559)
- Modified Installation and Settings, page 7 (SAR 35559)
- Added Figure 11, page 20 (SAR 35559)
- Modified Table 28, page 40 (SAR 35448)
- Modified Step 1 in Programming the A2F500-DEV-KIT-2 Board (SmartFusion cSoC Device), page 71 (SAR 38192)

1.4 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Pinout for the mixed signal header has been corrected for pins 74, 77 and 78 under Pinout Definition, page 51 section SAR(31646).
- Updated the performance note listed under the Pinout Definition, page 51 (SAR 32503).

1.5 Revision 4.0

Replaced Figure 43, page 44 (SAR 33509).

1.6 Revision 3.0

Updated Table 36, page 51 (SAR 31535).

1.7 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Changed the kit name from A2F-DEV-KIT to A2F500-DEV-KIT throughout the document (SAR 26186).
- Changed the device number from A2F200 to A2F500 throughout the document and updated required figures to reflect A2F500 device in the entire document.
- Changed number of OBDs to 3 in Table 2, page 5.
- Updated the A2F200 key features table to Table 1, page 4.

- Added references to Keil and IAR software support with SmartFusion cSoCs to the Software Installation, page 7.
- Added a reference to the *Installing IP Cores and Drivers User's Guide* document.
- Updated Figure 5, page 18 and the RS485 Interface, page 29 figures as per the new board.
- Corrected the jumper number for OBD and ADC loopback related configurations in Table 11, page 22.
- The Low-Cost Programming Stick Header, page 43 is new.
- Updated the FlashPro4 Programming Header, page 45 section with proper figure and jumper settings.
- Replaced the LVDS I/Os section with the A2F500 Digital I/O Expansion Header, page 48, which explains LVDS pairs also.
- Updated Table 37, page 53.
- Added a reference to the *Configuring Serial Terminal Emulation Programs tutorial*.

1.8 Revision 1.0

Revision 1.0 was the first publication of this document.

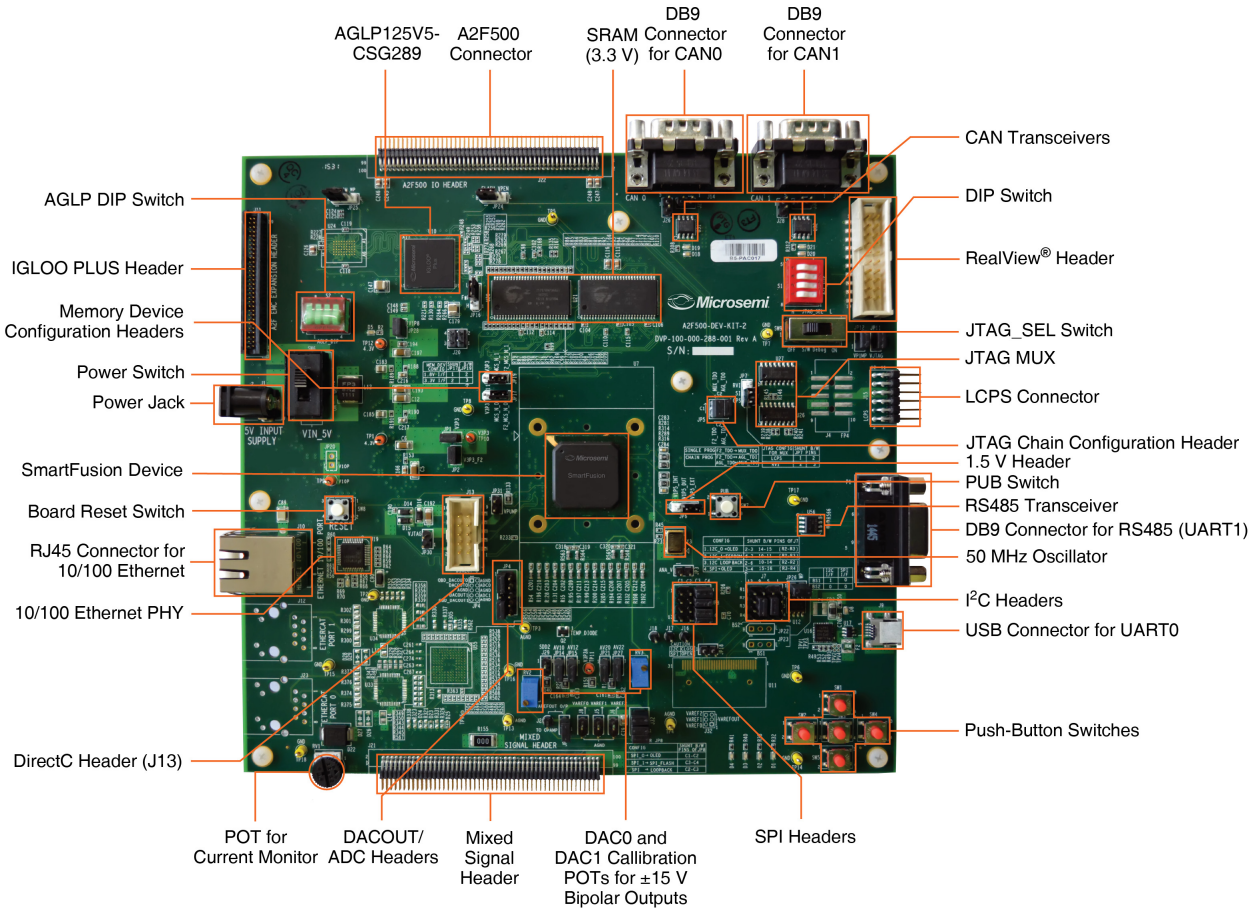
2 Introduction

The RoHS-compliant SmartFusion® Development Kit (A2F500-DEV-KIT-2) enables designers to develop applications that involve one or more of the following:

- Microcontroller applications
- Real-time operating system (RTOS)/OS development
- Embedded ARM Cortex-M3 processor based systems
- Motor control
- System management
- Power sequencing, trimming, and management
- Touch screen display control
- Audio processing
- FieldBus demonstrator
- EtherCAT
- Industrial network

The board also provides a standard 100-pin mixed signal header for interfacing to the analog pins. This provides access for plugging in a daughter board with a mixed signal interface.

Figure 1 • **A2F500-DEV-KIT-2**



2.1 Kit Contents

The following table lists the contents of the SmartFusion Development Kit.

Table 1 • **Kit Contents - A2F500-DEV-KIT-2**

Item	Quantity
SmartFusion Development Board with SmartFusion A2F500M3G-FGG484ES device	1
Low-cost programming stick (LCPS) or FlashPro 4 programmer	1
5 V power supply with international adapters	1
USB 2.0 A to mini-B cable	2
Quickstart card	1

2.2 SmartFusion Development Kit Web Resources

The SmartFusion Development Kit web resources are available on the Microsemi website: www.microsemi.com/soc/products/hardware/devkits_boards/smartfusion_dev.aspx#rsc.

2.3 Board Description

The SmartFusion Development Kit Board is designed to provide a development platform for users to evaluate all the features of the world's only customizable system-on-chip (cSoC) with a hard ARM Cortex-M3 processor powered microcontroller subsystem (MSS) along with programmable analog.

The board supports a SmartFusion cSoC device in an FG484 package. To enable the MSS, analog, and evaluation of features, the board includes the following:

- Ethernet, EtherCAT, and USB-to-UART interface for communication with Ethernet and UART peripherals of the SmartFusion MSS
- Static random access memory (SRAM), parallel flash, SPI flash, and electrically erasable programmable read-only memory (EEPROM) that interface with EMC, SPI, and I2C peripherals of the SmartFusion MSS
- Digital-to-analog converter (DAC) that interfaces either to SPI port 0 or SPI port 1 of the SmartFusion MSS
- I2C interface and temperature monitoring
- Mixed signal header for daughter card interfacing
- RealView ICE Simulation Unit (RVI) header for application programming and debug from either Keil ULINK or IAR J-link

The board includes a FlashPro4 programming header to enable programming and debugging from Microsemi design tools FlashPoint and SoftConsole.

The following table lists SmartFusion Development Kit Board Components.

Table 2 • **SmartFusion Development Kit Board Components**

Name	Description
A2F500M3G-FGG484ES	Microsemi SmartFusion cSoC with hard ARM Cortex-M3 processor
CURRENT SENSING	Current monitoring using thumbwheel POT (RV1)
PWM CIRCUIT	Pulse Width Modulation Resistor Capacitor (PWMRC) circuit
OBD	Three one-bit DACs used in comparator
I2C EEPROM	512 Kbit I2C EEPROM ST M24512-WMN6TP connected to I2C port 1 of the SmartFusion MSS
SPI FLASH	8 MByte SPI flash Atmel AT25DF641-MWH-T connected to SPI port 1 of the SmartFusion MSS
SPI DAC	12-bit SPI DAC AD5320 with option to interface either to SPI port 0 or SPI port 1 of the SmartFusion MSS
OSC-50	50 MHz clock oscillator
OSC-20	20 MHz/20 PPM clock oscillator
OSC-32	32.768 KHz low power oscillator
USB/UART	USB-to-UART adapter chip CP2102 and connector interfacing with UART Port 0 of the SmartFusion MSS
RS485	RS485 with DB9 female connector interfacing with MAX3240CSA, connected to UART port 1 of the SmartFusion MSS
ETHERNET	RJ45 connector (Ethernet jack with magnetics) interfacing with National Semiconductor 10/100 PHY chip DP83848C in RMII mode, interfacing with Ethernet port of the SmartFusion MSS (on-chip MAC and external PHY)
AGLP125-CS289	IGLOO® PLUS FPGA implementing level converter between 3.3 V and 1.8 V to connect 1.8 V PSRAM/flash with external memory controller (EMC, which has native voltage level of 3.3 V) of the SmartFusion MSS
EXPANSION	When external memory controller (EMC) is not used, the I/Os are available as 3.3 V GPIOs.
Asynchronous SRAM	Two 16-Mbit SRAM Cypress CY7C1061DV33-10ZSXI connected to each region of the EMC interface of the SmartFusion MSS
FLASH	Two 64-Mbit parallel flash memory Numonyx JS28F640J3D-75 connected to each region of the EMC interface of the SmartFusion MSS
LG_PSRAM	128-Mbit, 1.8 V asynchronous PSRAM Micron MT45W8MW16BGX connected to the EMC interface of the SmartFusion MSS. This provides the option of bigger memory as an alternative to the SRAM for memory intensive applications.
LG_FLASH	128-Mbit, 1.8 V, parallel flash memory Numonyx JS28F128P30T85 873824 connected to the EMC interface of the SmartFusion MSS. This provides the option of bigger memory as an alternative to the flash for memory intensive applications.
CAN_IF	Two CAN interfaces with DB9 female connector interfacing with MAXIMMAX3051 CAN transceiver connected to four GPIOs of the SmartFusion MSS
ETHERCAT_IF	Two RJ45 connectors (Ethernet jack with magnetics) for EtherCAT ports interfacing with Beckhoff ET1100 and Micrel KS8721BL and connecting to the SmartFusion cSoC via soft SPI implemented in the fabric using six general purpose I/Os
RVI HEADER	RVI header for application programming and debug from Keil ULINK or IAR J-Link

Table 2 • **SmartFusion Development Kit Board Components *(continued)***

Name	Description
FP4 Programming HEADER	Flashpro4 programming header for FPGA and cSoC programming and debugging with Microsemi tools
PROG HDR	Direct-C programming header
TEMP DIODE	Temperature diode
BATT BACKUP	Battery backup circuit
DIPSWITCH	Two 4-switch DIP switch packs for GPIO
LEDS	Four active Low LEDs that can be connected to any user I/O for debug to power-on the board
PUSH-BUTTON RESET	Push-button system reset for SmartFusion System
MIXED_CONN100	To power-on the board mixed signal header
PUSH-BUTTON SWITCHES	Six push-button switches for test and navigation and PUB
MIXED_CONN100	Mixed signal header
A2F500_CONN100	Microsemi SmartFusion A2F500M3F-FG484ES additional I/O connector

3 Installation and Settings

3.1 Software Installation

Download and install the latest release of Microsemi Libero SoC v11.7, v9.0 or later, from the Microsemi website and register for your free Silver license. For instructions on how to install Libero SoC and SoftConsole, see the *Libero Software Installation and Licensing Guide*.

Refer to the Installing IP Cores and Drivers User Guide for download and installation of Microsemi DirectCores, SGCores, and Driver firmware cores that must be localized on the personal computer where Microsemi's Libero is installed when designing with Microsemi FPGAs and cSoCs. Microsemi has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem. Microsemi SmartFusion is supported by the latest release of IAR Systems, the IAR Embedded Workbench for ARM. Refer to Designing SmartFusion with IAR Systems document for more information.

Microsemi SmartFusion cSoC is also supported by the latest release of Keil, the MDK-ARM Microcontroller Development Kit. Refer to the Designing SmartFusion with Keil document for more information.

3.2 Hardware Installation

The FlashPro4 (FP4) programmer plugs directly into the A2F500-DEV-KIT-2 board. This allows programming A2F500 and AGLP125 devices in chain mode or individually with appropriate jumper settings (JP5).

3.2.1 Jumper Settings

The recommended default jumpers settings is shown in the following figure and defined in Table 3, page 8. Connect the jumpers with the default settings to enable the pre-programmed demonstration design to function correctly.

Figure 2 • **Jumper Locations**

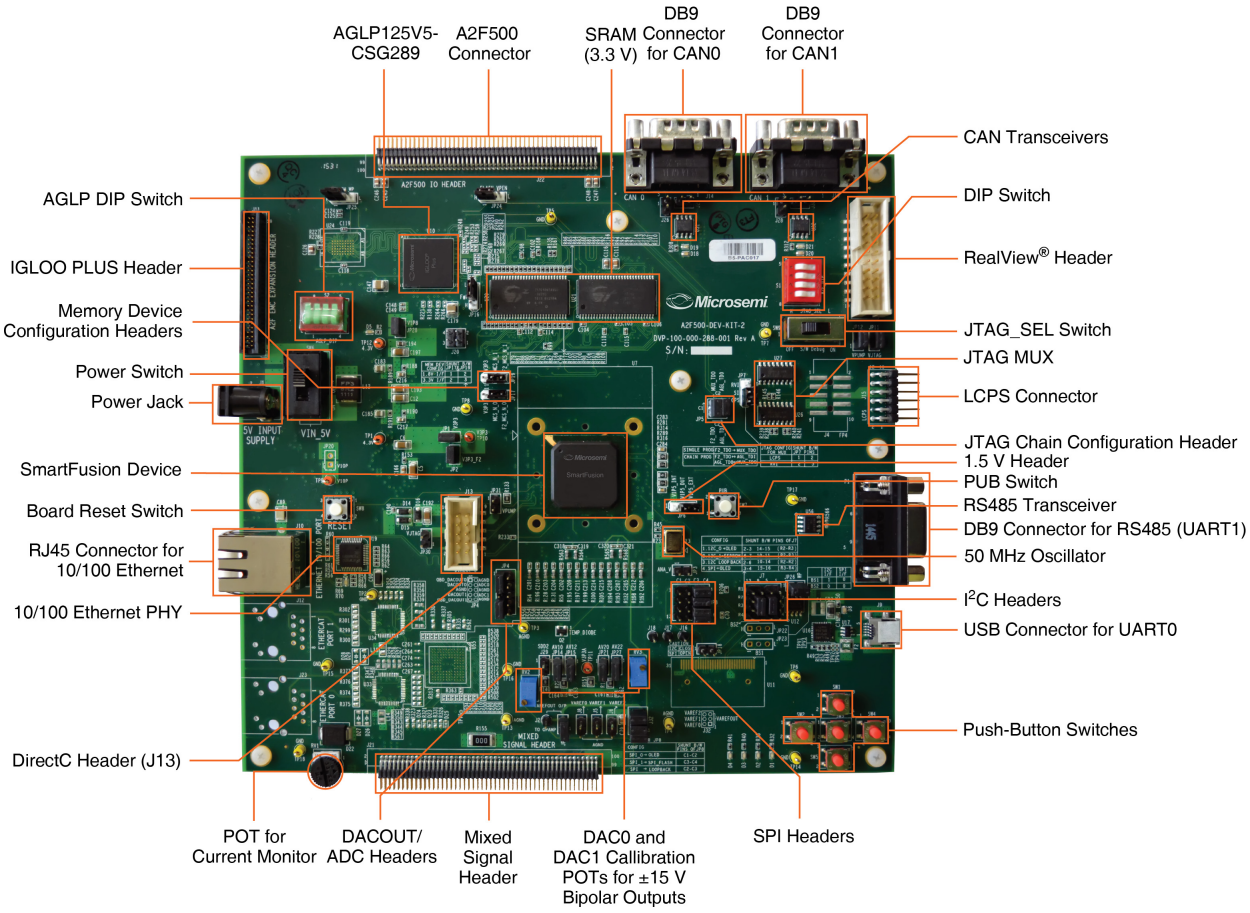


Table 3 • **Jumper Settings**

Jumper	Function	Default Setting	Notes
JP1	Jumper to select first 3.3 V power supply for board	1–2 Closed	
JP2	Jumper to select second 3.3 V power supply for board	1–2 Closed	
JP3	Jumper for SPI DAC output VOUT	Open	
JP4	Jumper settings to use comparator		Pins 2, 6,10 are connected to AGND
	Pin 3–4 = DACOUT0 to ADC0	Open	
	Pin 7–8 = DACOUT1 to ADC1	Open	
	Pin 1–3 = DACOUT0 to OBD_DACOUT0	Closed	
	Pin 7–9 = DACOUT1 to OBD_DACOUT1	Closed	

Table 3 • **Jumper Settings *(continued)***

Jumper	Function	Default Setting	Notes
JP5	Jumper for JTAG device option (A2F500 and AGLP125)		
	Pin 1–3 = A2F500 in chain	Open	
	Pin 1–2 and Pin 4-3 = A2F500 and AGLP125 daisy chained	Closed	
JP6	Jumper to select either 1.5 V external regulator or SmartFusion cSoC device 1.5 V internal regulator		
	Pin 1–2 = 1.5 V internal	Open	
	Pin 3–2 = 1.5 V external	Closed	
JP7	Jumper to select between RVI header or LCPS header for application debug		
	Pin 1–2 = LCPS for SoftConsole	Closed	
	Pin 2–3 = RVI for Keil U-link/ IAR J-link	Open	
J7[1]	Jumper/Header for SPI_0, I^2C, EEPROM, OLED, and I^2C loopback		
	I2C0 to OLED		
	Pin 2–3 = I2C_0_SCL to OLED_SCL	Closed	Configuration 1: I2C0 -> OLED and I2C1 -> EEPROM
	Pin 14–15 = I2C_0_SDA to OLED_SDA_IN	Closed	
	I2C1 to EEPROM		
	Pin 6–7 = I2C_1_SCL to EEPROM_SCL	Closed	
	Pin 10–11 = I2C_1_SDA to EEPROM_SDA	Closed	
	I2C0 and I2C1 Loopback		Configuration 2: I2C0 <-> I2C1 (Loop Back)
	Pin 2–6 = I2C_0_SCL to I2C_1_SCL	Open	
	Pin 10–14 = I2C_1_SDA to I2C_0_SDA	Open	
	SPI to OLED		Configuration 3: SPI -> OLED and I2C1 -> EEPROM
	Pin 3–4 = SPI_SCK to OLED_SCL	Open	
	Pin 15–16 = SPI_SDA to OLED_SDA	Open	
	I2C1 to EEPROM		
	Pin 6–7 = I2C_1_SCL to EEPROM_SCL	Closed	
	Pin 10–11 = I2C_1_SDA to EEPROM_SDA	Closed	
J20	From AGLP125 CS289	Closed	These pins are brought out for future and test-ing purpose.
	Pin 1=AGLP_3.3V_SIG1		
	Pin 2=AGLP_3.3V_SIG2		
	Pin 3=AGLP_3.3V_SIG3		
	Pin 4=AGLP_3.3V_SIG4		

Table 3 • **Jumper Settings *(continued)***

Jumper	Function	Default Setting	Notes
JP8[1]	**Jumper/Header for SPI, OLED, SPI flash, and loopback**		
	SPI_0 to OLED		
	Pin 1–2 = SPI_0_OUT to OLED_SDA_IN (Need shunt pin 15–16 jumper on J7)	Open	Configuration 1: SPI_0 to OLED and SPI_1 to SPI flash
	Pin 5–6 = SDI_0_IN to OLED_SDA_OUT	Open	
	Pin 9–10 = SCLK_0_OUT to OLED_SCL (Need shunt pin 3–4 jumper on J7)	Open	
	Pin 13–14 = SS_0_OUT to OLED_CS#	Open	
	SPI_1 to SPI flash		
	Pin 3–4 = SDI_1_IN to SPI_1_SO (SO output of SPI flash)	Closed	
	Pin 7–8 = SDO_1_OUT to SPI_1_SI (SI input of SPI flash)	Closed	
	Pin 11–12 = SCLK_1_OUT to SPI_1_SCK (SCK input of SPI flash)	Closed	
	Pin 15–16 = SS_1_OUT to SPI_CS_N (CS# input of SPI flash)	Closed	
	SPI0 to SPI1 (loopback)		Configuration 2: SPI0 and SPI1 loopback
	Pin 2–3 = SDO_0_OUT to SDI_1_IN	Open	
	Pin 6–7 = SDI_0_IN to SDO_1_OUT	Open	
	Pin 10–11 = SCLK_0_OUT to SCLK_1_OUT	Open	
	Pin 14–15 = SS_0_OUT to SS_1_OUT	Open	
JP11	Jumper to connect 3.3 V to VJTAG	1–2 Closed	
JP12	Jumper to connect 3.3 V to VPUMP	1–2 Closed	
JP13	VREF_OUT to OP_AMP (U44A & U51A) positive	1–2 Closed	
JP14	OP_AMP (U44C) output to ABPS0 of FPGA fabric	1–2 Open	
JP15	OP_AMP (U44C) output to ABPS4 of FPGA fabric	1–2 Open	
JP16	Jumper to control F*F of AGLP125 device		
	Pin 1–2 = F*F connected to 3.3 V (deasserted)	Open	
	Pin 2–3 = F*F connected to GND (asserted)	Closed	
JP17	Jumper to select between 1.8 V and 3.3 V memory Interface connected to region 0 of EMC		To keep 3.3 V devices tri-stated
	Pin 1–2 = 1.8 V interface	Open	
	Pin 2–3 = 3.3 V interface	Closed	
JP18[1]	Jumper to connect OLED_SDA_OUT and OLED_SDA_IN		
	Pin 1–2 = Closed for I2C configuration mode	Closed	
	Pin 1–2 = Open for SPI mode		

Table 3 • **Jumper Settings *(continued)***

Jumper	Function	Default Setting	Notes
JP19	Jumper to select between 1.8 V and 3.3 V memory interface connected to EMC		To keep 3.3 V devices tristated
	Pin 1–2 = 1.8 V interface	Open	
	Pin 2–3 = 3.3 V interface	Closed	
JP20	Jumper to select positive 10 V power supply for board	Closed	
JP21	OP_AMP (U51C) output to ABPS1 of FPGA fabric	1–2 Open	
JP22[1]	Jumper to connect OLED_BS1 (MCU interface selection Input) to 3.3 V or GND		
	Pin 1–2 = 3.3 V (needed for I2C mode)	Open	
	Pin 2–3 = GND (needed for SPI mode)	Closed	
JP23[1]	Jumper to connect OLED_BS2 (MCU interface selection input) to 3.3 V or GND		
	Pin 1–2 = 3.3 V	Closed	
	Pin 2–3 = GND (needed for both I2C & SPI modes)	Open	
JP24	Jumper to connect FLASH_VPEN of 64-Mbit parallel flash connected to both regions of EMC		Identified as FLASH
	Pin 1–2 = FLASH_VPEN to 3.3 V (enabled)	Closed	
	Pin 2–3 = FLASH_VPEN to GND (disabled)	Open	
JP25	Jumper to connect FLASH_WP# of 128-Mbit parallel flash		Identified as LG_FLASH
	Pin 1–2 = FLASH_WP# to 1.8 V (disabled)	Open	
	Pin 2–3 = FLASH_WP# to GND (enabled)	Closed	
JP26	Jumper to connect WE_N of EEPROM to 3.3 V		
	Pin 1–2 = 3.3 V (EEPROM write disabled)	Closed	
JP27	OP_AMP (U51C) output to ABPS5 of FPGA fabric		
JP28	Jumper to select 1.8 V power supply for board	1–2 Closed	
JP30	Jumper to connect VJTAG of PROG HDR to 3.3 V	Open	
JP31	Jumper to connect VPUMP of PROG HDR to 3.3 V	Open	
J32	VAREFOUT to ADC0, ADC1, ADC2 VAREF inputs		
	1–2 VAREFOUT to VAREF0	Closed	
	3–4 VAREFOUT to VAREF1	Closed	
	5–6 VAREFOUT to VAREF2	Closed	

1. The latest revision of SmartFusion Advanced Development Kit (A2F500-DEV-KIT-2) does not have an OLED component on the board.

3.3 LED Settings

The recommended settings are listed in the following table.

Table 4 • **SmartFusion Development Kit LEDs**

LED	SmartFusion Pin	Comment
D1	B19	Test LED for user application
D2	B20	Test LED for user application
D3	C19	Test LED for user application
D4	H17	Test LED for user application
D5	N/A	5 V Power Supply Indicator LED. This LED is ON when board is powered on
D6	N/A	SPEED LED: The LED is ON when device is in 100 Mbps and OFF when in 10 Mbps.
D8	N/A	UART over USB link indicator LED

3.4 DIP Switch Settings

The recommended DIP switch settings are listed in the following table.

Table 5 • **SmartFusion Development Board DIP Switches**

DIP Switch (S1)	SmartFusion Pin	Comment
DIP1	H20	Test switch for user application
DIP2	C21	Test switch for user application
DIP3	D21	Test switch for user application
DIP4	F19	Test switch for user application

The following table lists the SmartFusion Development Kit test points.

Table 6 • **SmartFusion Development Kit Test Points**

Test Point	Comment
TP1, TP12	5 V power supply (measures 4.3 V due to diode drop)
TP2, TP5, TP6, TP7, TP8	Digital ground (GND)
TP3, TP4, TP13	Analog ground (AGND)
TP9	10 V rail for OLED
TP10	3.3 V supply for SmartFusion
TP11	3.3 V analog supply

3.5 Push-Button Switch Settings

The recommended push-button switch settings are listed in the following table.

Table 7 • **SmartFusion Development Kit Push-Button Switches**

Push-Button Switch	SmartFusion Pin	Comment
SW1	G19	Test and navigation switch
SW2	G20	Test and navigation switch

Table 7 • **SmartFusion Development Kit Push-Button Switches**

SW3	G21	Test and navigation switch
SW4	E1	Test and navigation switch
SW5	E14	Test and navigation switch
SW6	N/A	Switch ON 5 V DC into SmartFusion cSoC device regulators
SW7	W7	Push-button switch for PUB. This negative active switch is connected to the PUB pin, which is a digital input to the FPGA fabric. PUB is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator.
SW8	R1	System reset for DUT
SW9	R16 (JTAGSEL)	Switch to select A2F500 programming with FlashPro4 or Cortex-M3 processor debug. OFF position selects A2F500 programming and ON position selects Cortex-M3 processor for application debug.

3.5.1 Testing the Hardware

If the board is shipped directly from Microsemi, it contains a test program that determines whether the board works properly. If while using the board you suspect that the board is damaged, you can rerun the Manufacturing Test, page 69 to verify the key components of the board functionality.

4 Hardware Components

4.1 SmartFusion cSoC Description and Connections

The SmartFusion Development Kit Board is populated with a SmartFusion A2F500M3G-FGG484ES, the world's only cSoC with hard ARM Cortex-M3 processor. The key features of the SmartFusion cSoC are listed below and in Table 8, page 15.

The MSS consists of the following:

- 100 MHz 32-Bit ARM Cortex-M3 1.25 DMIPS/MHz throughput from zero wait state memory
- Internal memories
  - Embedded flash memory (eNVM), 64 Kbytes to 512 Kbytes
  - Embedded high-speed SRAM (eSRAM), 16 Kbytes to 64 Kbytes, implemented in two physical blocks to enable simultaneous access from two different masters
- Multi-layer AHB communications matrix
  - Provides up to 16 Gbps of on-chip memory bandwidth
- 10/100 Ethernet MAC with RMII interface
- Programmable external memory controller, which supports:
  - Asynchronous memories
  - NOR flash, SRAM, PSRAM
  - Synchronous SRAMs
- Two I^2C peripherals
- Two 16550 compatible UARTs
- Two SPI peripherals
- Two 32-bit timers
- 32-bit watchdog timer
- 8-Channel DMA controller
- Clock sources
  - 1.5 MHz to 20 MHz main oscillator
  - Battery-backed 32 KHz low-power oscillator with real-time counter (RTC)
  - 100 MHz embedded RC oscillator 1% accurate
  - Embedded PLL with 4 output phases
- High-performance FPGA fabric
- Based on Microsemi's proven ProASIC®3 FPGA fabric
- Analog front-end (AFE)
- Up to three 12-Bit SAR ADCs
- One first-order DAC (sigma-delta) per ADC
- Up to five new high-performance analog signal conditioning blocks (SCB) per device
- Two high-speed comparators
- Analog compute engine (ACE)
  - Offloads CPU from analog initialization and processing of ADC, DAC, and SCBs
  - Sample sequence engine for ADC and DAC parameter set-up
  - Post-processing engine for functions such as low-pass filtering and linear transformation

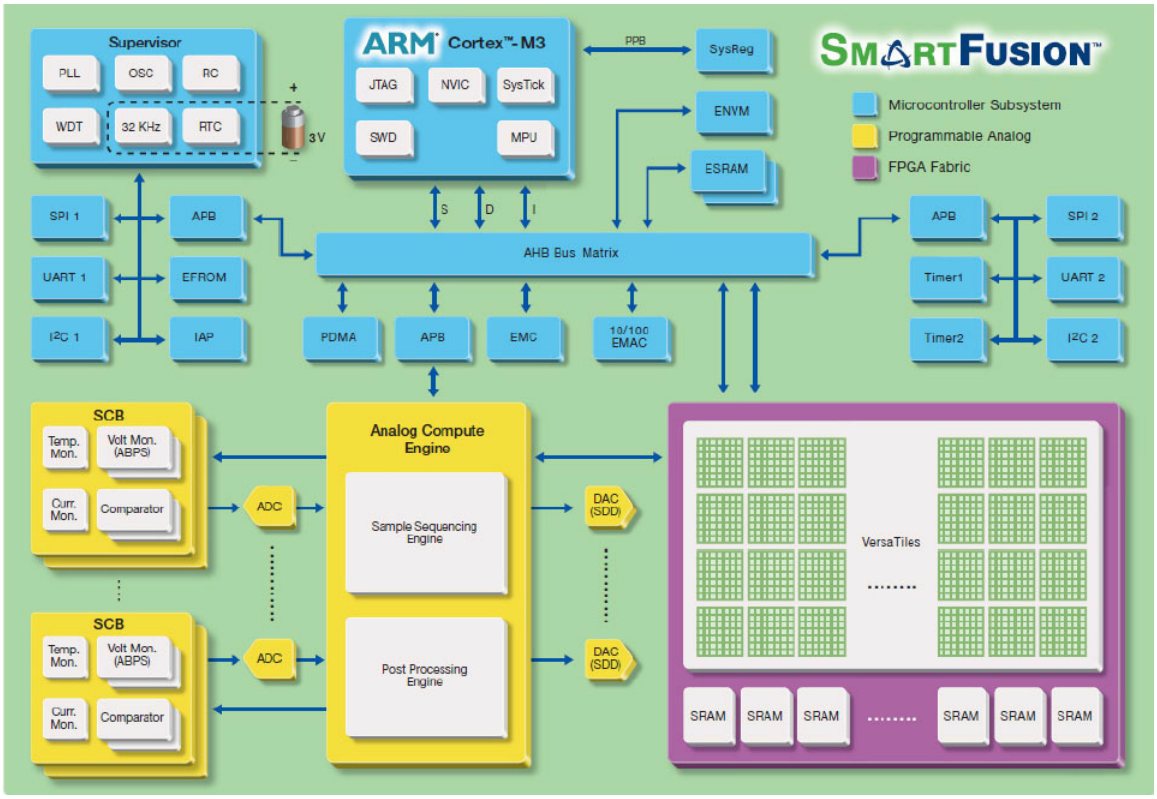
The following table list the I/Os of SmartFusion.

Table 8 • **A2F500 I/Os**

Device	Package
A2F500	FG484
Direct analog input	12
Total analog input	32
Total analog output	3
MSS I/Os[1, 2]	41
FPGA I/Os	128
Total I/Os	204

1. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for the MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, and 3.3 V) standards.
2. 9 MSS I/Os are primarily for 10/00 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, and 3.3 V) standards.

Figure 3 • **SmartFusion Block Diagram**



4.2 I/O Pin Connections

The pin list is provided in the Pin List, page 53.

4.3 SmartFusion cSoC Hard ARM Cortex-M3 Processor

The SmartFusion cSoC comes with a hard Cortex-M3 advanced processor-based MSS. The ARM Cortex-M3 microcontroller is a low power processor that features low gate count, low predictable interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response features. SmartFusion cSoCs use the R1P1 version of the Cortex- M3 processor core. Some of the important subsystems are listed below:

- Memory protection unit (MPU)
- Single-cycle multiplication and hardware divide
- JTAG debug (4 wire), serial wire debug (SWD - 2 wire) and serial wire viewer (SWV) interfaces

The development board is populated with components to enable development using the MSS. These components include SRAM, PSRAM, flash, SPI flash, I2C, EEPROM, SPI DAC, communication interfaces such as Ethernet, and USB-to-UART.

4.4 Power Sources

This board is powered through an external 5 V power supply brick.

4.4.1 SmartFusion Power Sources

Seven voltage rails (10 V, 5 V, 3.3 V, 1.8 V, 1.5 V, and ± 15 V) are provided on the board:

- A single regulator, Linear LT3684EMSE (3.3 V, 2 A), supplies both analog and digital 3.3 V going to the SmartFusion cSoC device. Sufficient isolation is provided through low-pass filter and layout to prevent noise from the digital domain to propagate to the analog domain.
- Linear LT3684EMSE (1.8 V, 2 A), supplies 1.8 V rails.
- Linear LT3684EMSE (1.5 V, 2 A), supplies 1.5 V rails.
- A single regulator, Linear LT1615, supplies both the +15 V and -15 V with 4 mA rating required by the DAC comparators.

5 Components Description and Operation

5.1 VAREF Connections

The SmartFusion cSoC has one external VAREF input pin for each of the ADCs. The internal VAREF is brought out as an output, available as VAREFOUT output pin. There are multiple options available to drive the VAREF0 and VAREF1 from either external VAREF or the internal VAREF through VAREFOUT output of the FPGA fabric.

Figure 4 • **VAREF Jumper Selections**

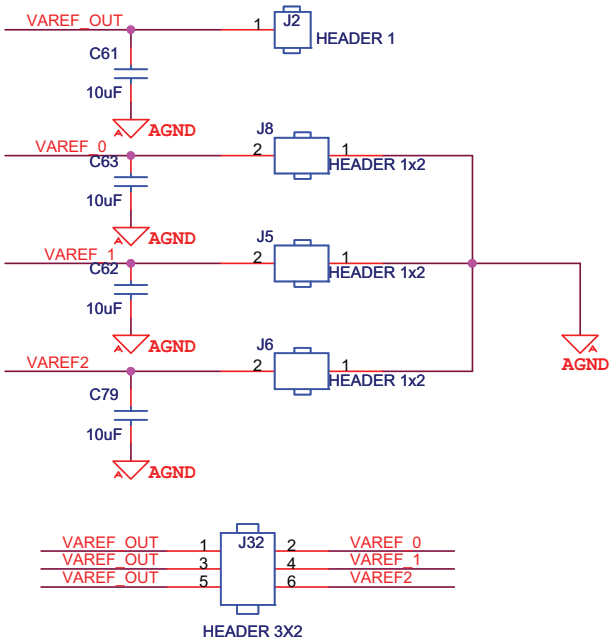


Table 9 • **Use as Internal VAREF**

Jumper	Function
J32	1–2 VAREFOUT to VAREF0
	3–4 VAREFOUT to VAREF1
	5–6 VAREFOUT to VAREF2

Note: VAREF0 corresponds to ADC[3:0], CM[1:0], TM[1:0]

Note: VAREF1 corresponds to ADC[7:4], CM[3:2], TM[3:2]

Note: VAREF2 corresponds to ADC[11:8], CM4, TM4 (A2F500 only)

Table 10 • **Using External VAREF**

VAREF	Jumper Settings	Comment
VAREF0	J32: 1–2	Open
	Connect external voltage across J8 pins 1–2	Do not place a jumper on J8

Table 10 • **Using External VAREF**

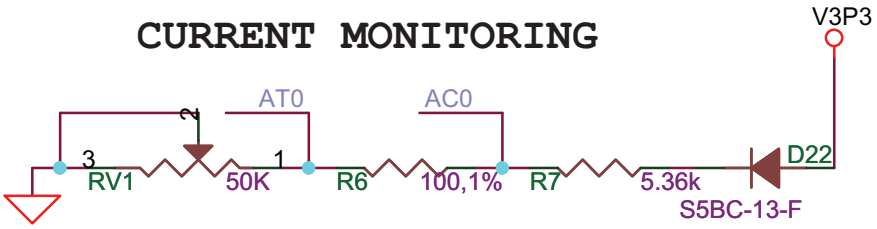
VAREF1	J32: 3–4	Open
	Connect external voltage across J5 pins 1–2	Do not place a jumper on J5
VAREF2	J32: 5–6	Open
	Connect external voltage across J6 pins 1–2	Do not place a jumper on J6

Note: You need an external VAREF to monitor voltages greater than 2.56 V on the DC/AC/AT channels. An internal VREF is sufficient to monitor voltages less than 2.56 V on the ADC/AC/AT channels. All ABPS channels can monitor voltages greater than 2.56 V using an internal VREF.

5.2 Current Sensing Circuit

For applications using the embedded current monitor, a current sensing circuit is provided on the SmartFusion Development Kit board. The current monitoring is performed across AC0 and AT0 pins of the SmartFusion cSoC device. The voltage across the potentiometer can be monitored via the AT0 pin. The current sensing circuits is for the 3.3 V voltage rail as shown in the following figure.

Figure 5 • **Current Sensing**



Note: The current monitoring circuit on the SmartFusion Development Kit board is connected to the SmartFusion cSoC devices CM0 and TM0 inputs. CM0 can also be used to monitor the voltage across the potentiometer. This input does not have a prescaler circuit. Because of the value chosen for the potentiometer, the full-scale input is reached after turning the potentiometer about one quarter of the maximum travel. Although this will not damage the SmartFusion cSoC device, you may notice the potentiometer is very sensitive.

5.3 PWM Circuit

The PWM RC circuit depicted in Figure 3-3 and Figure 3-4 on page 21 can be used with Microsemi CorePWM instantiated in the FPGA fabric to generate various voltage waveforms. These voltage waveforms can be displayed through the mixed signal header. In addition, one PWM RC circuit source is routed to the AV input pin of an analog quad. This AV pin can be used to monitor the generated voltage with high accuracy, depending on the ADC resolution configured in the FPGA fabric.

The following figure shows the A2F500 pins driving PWM and the PWM circuit.

Figure 6 • **PWM Pins**

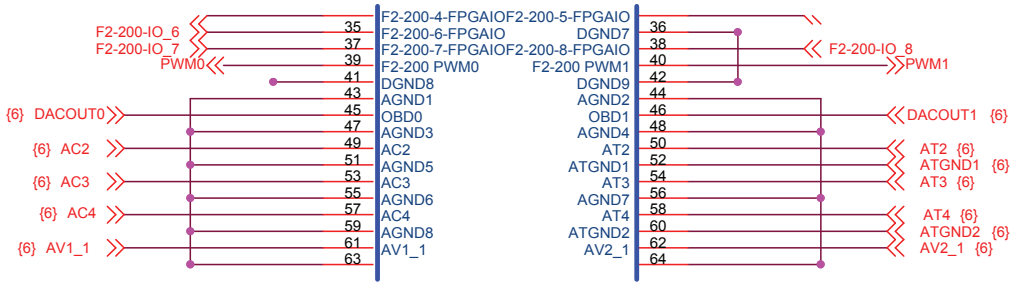
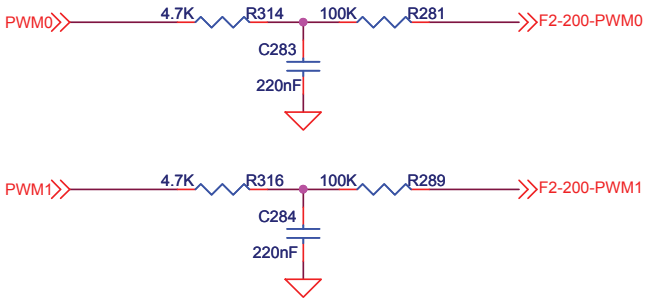


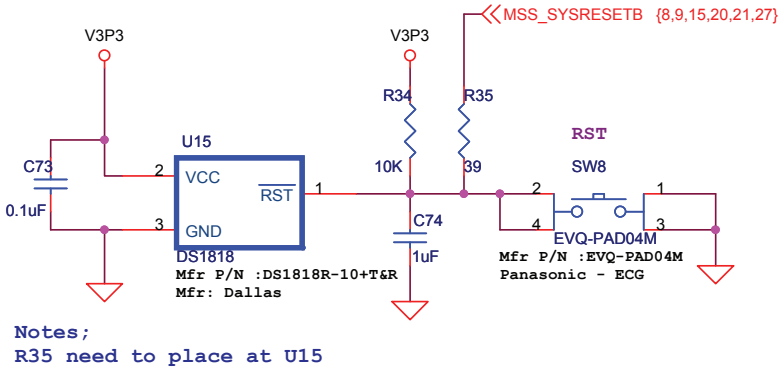
Figure 7 • **PWM Circuit**



5.4 Push-Button System Reset

A push-button system reset switch with a Schmitt trigger is provided on the board. The Schmitt trigger reduces noise on the system reset push-button. SmartFusion MSS reset is synchronized with this reset.

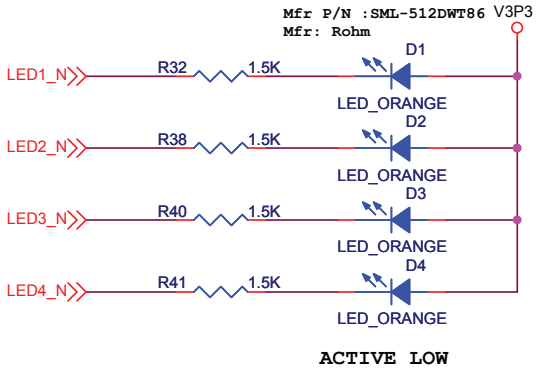
Figure 8 • **Push-Button System Reset**



5.5 Push-Button, DIP Switches, and User LEDs

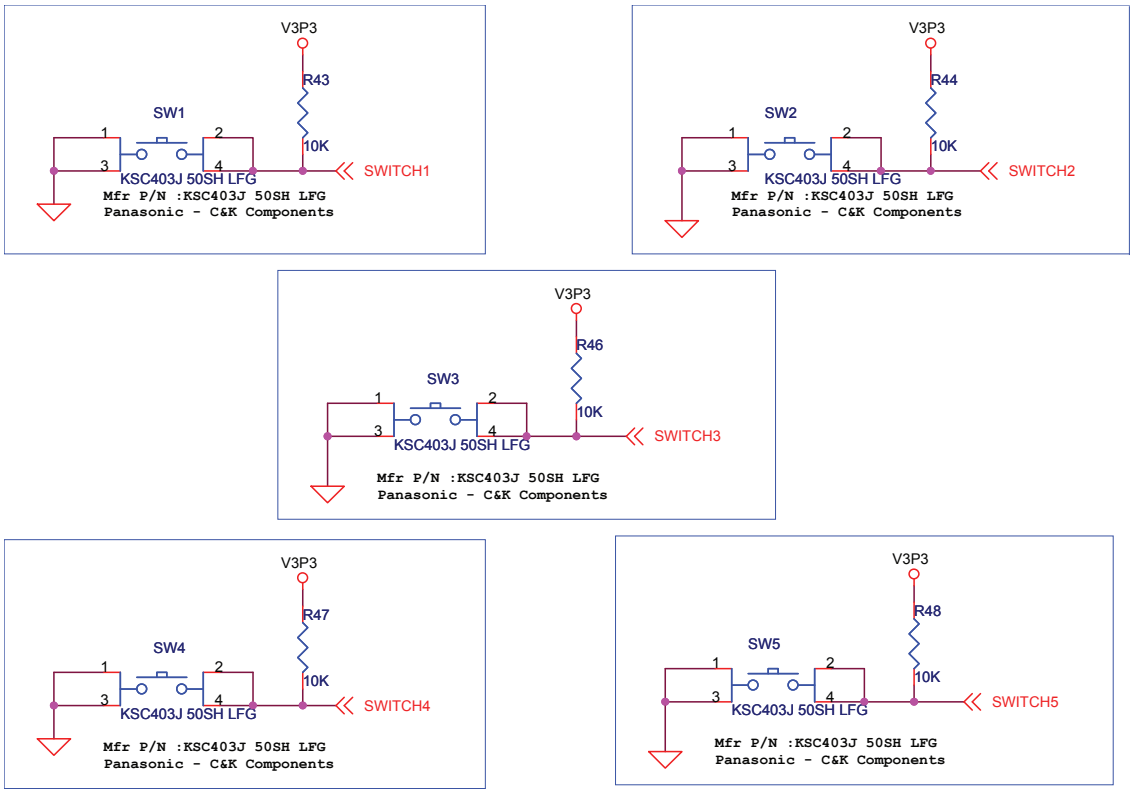
Push-button switches and user LEDs can also be used for debugging and for various applications, such as gaming.

Figure 9 • **Test LEDs**



The board provides users access to four active Low LEDs, which are connected to the SmartFusion pins B19, B20, C19, and H17.

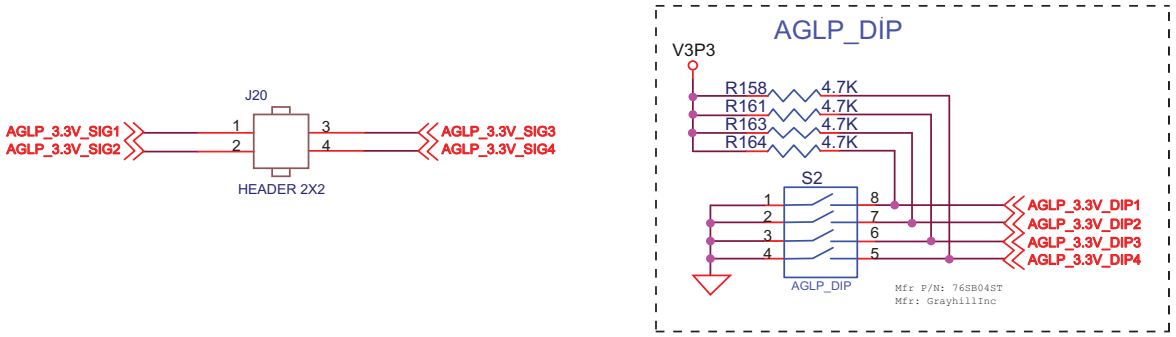
Figure 10 • **Push-Button Switches**



The board comes with Two four input DIP switches.

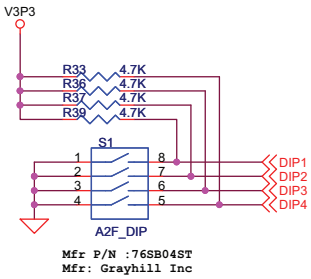
The inputs of AGLP_DIP switch are connected to pins N13,P16,R2,T2 of Bank 2 of the AGLP125 CS289.

Figure 11 • **AGLP_ DIP**



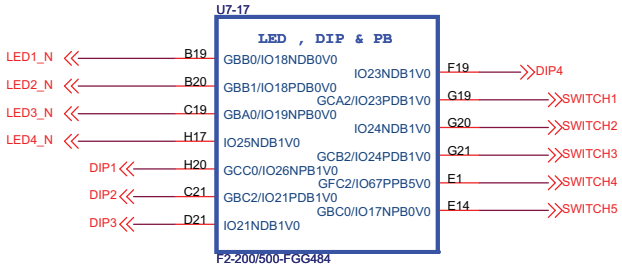
The inputs of A2F_ DIP switch are connected to pins H20, C21, D21, and F19 of the SmartFusion cSoC.

Figure 12 • **Input Push-Button Switch**



In addition, the board includes five push-button switches that are connected to pins G19, G20, G21, E1, and F14 of the SmartFusion cSoC.

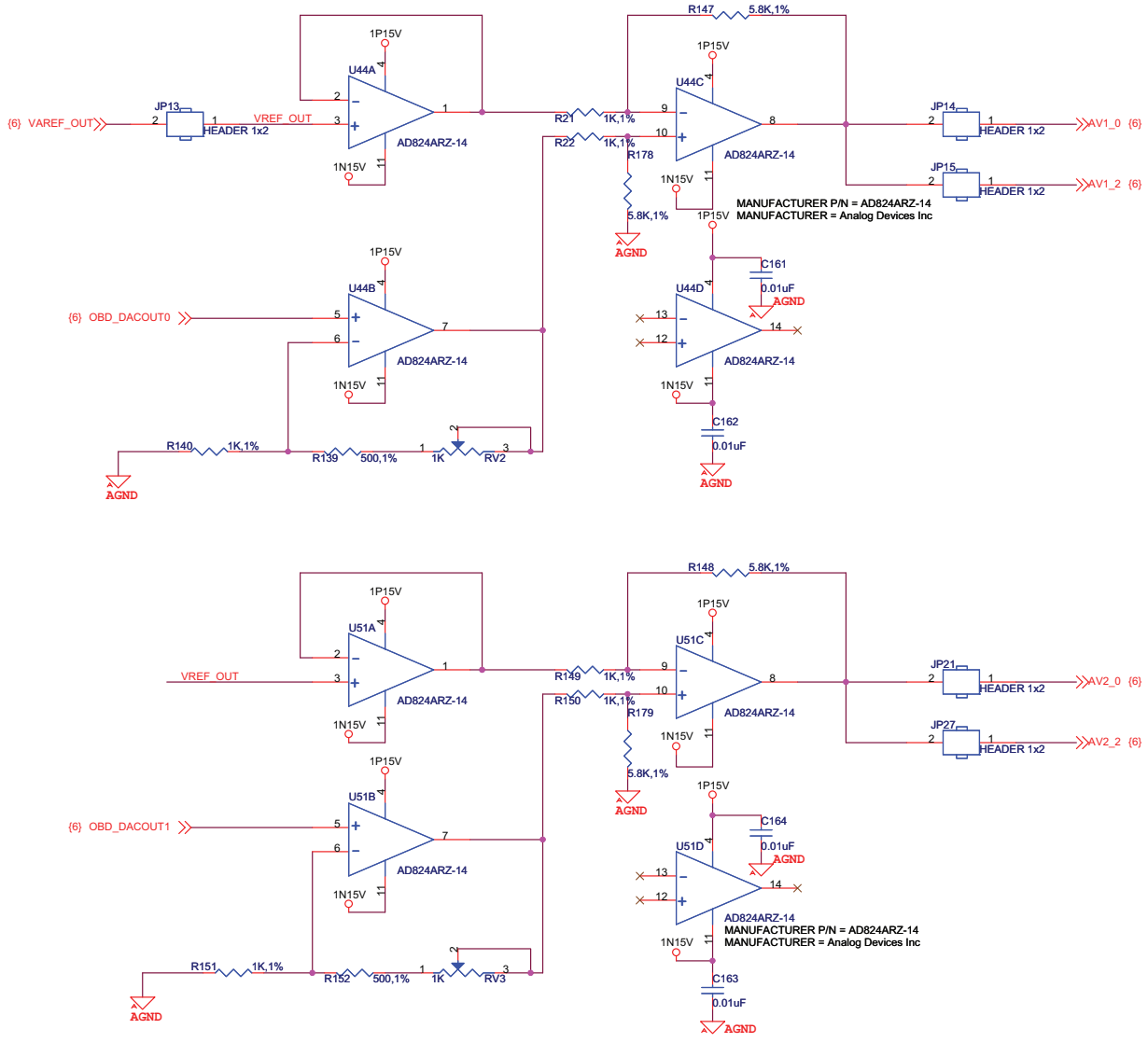
Figure 13 • **LED, DIP, and Push-Button I/Os**



5.6 One-Bit DAC Circuit

For applications that require conversion from a digital to analog domain, two analog conditioning circuits are provided. This is useful in closed-loop applications. Figure 3-11 shows the circuit. Table 3-5 on page 25 and Table 3-6 on page 26 show the jumper settings.

Figure 14 • **OBD_DACOUT**



The one-bit DACs (OBDs) can be used in two applications.

These circuits take the OBD output of the SmartFusion quad and feed it back to the SmartFusion analog inputs of ADC0 and ADC1. This is useful in closed-loop applications.

Table 11 • **OBD Output to Loopback to ADC**

Jumper	Pin	Function
JP4	3-4	DACOUT0 to ADC0
	7-8	DACOUT1 to ADC1

The OBDs can also be fed into a voltage gain circuit as shown in Figure 14, page 21 and described in the following tale. In this application, the OBD sweep of 0-2.56 V can be translated to -15 V to +15 V. This is useful in closed-loop applications for ABPS channels with prescalers.

Table 12 • **OBD Connections for Voltage Gain**

Jumper	Pin	Pin
JP4	1–3	DACOUT0 to OBD_DACOUT0
	7–9	DACOUT1 to OBD_DACOUT1
JP13	1–2	Connect VAREF_OUT to bias the opamp

The output of the Opamp can be configured to be monitored by the ABPS channel. This can be done as below:

Table 13 • **Output of the Opamps to ABPS Channels**

Jumper	Pin	Pin	Function
JP14	1	2	OP_AMP (U44C) output to ABPS0 of FPGA fabric
JP15	1	2	OP_AMP (U44C) output to ABPS4 of FPGA fabric
JP21	1	2	OP_AMP (U51C) output to ABPS1 of FPGA fabric
JP27	1	2	OP_AMP (U51C) output to ABPS5 of FPGA fabric

5.7 OLED Display

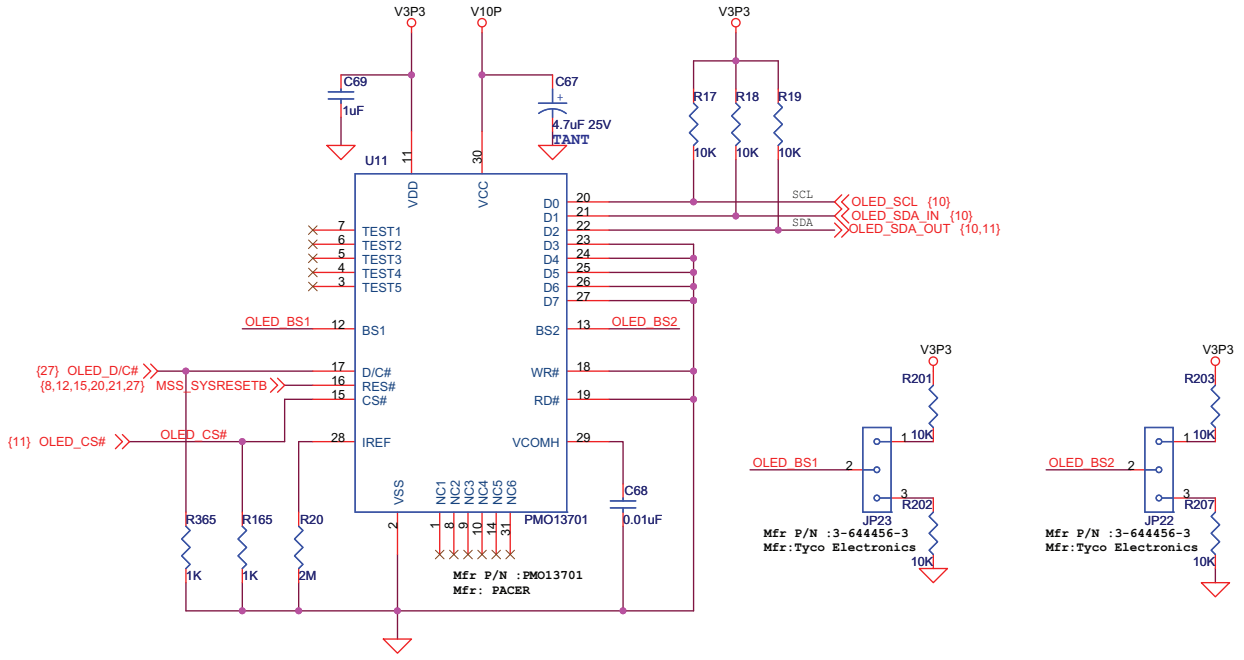
A 9616-pixel low-power OLED is made available on the board for display. This low-power device, WHITE OLED, requires 3.3 V and 10 V power supplies. Either one of the SmartFusion MSS I2C0 or SPI0 can be interfaced with the OLED.

The OLED displays sharp gaming images or text. For example, the SmartFusion RTC current time or time between two events can be displayed on the OLED. Figure 15, page 23 shows the OLED connections on the board along with jumpers for BS1 and BS2 and the jumper settings for accessing the OLED from SPI0.

Note: The latest revision of SmartFusion Advanced Development kit (A2F500-DEV-KIT-2) does not have an OLED component on the board.

For accessing the OLED from I2C0 and SPI0, see Jumper Settings, page 23.

Figure 15 • **OLED Connections**



5.7.1 Jumper Settings

Table 14 • **Interface MSS I2C0 to the OLED**

Jumper	Pin	Pin	Connection Details
J7	2	3	I2C_0_SCL to OLED_SCL
	14	15	I2C_0_SDA to OLED_SDA_IN
JP18	1	2	Closed
JP23	1	2	OLED_BS1 connected to 3.3 V
JP22	2	3	OLED_BS2 connected to GND

Table 15 • **Interface MSS SPI0 to the OLED**

Jumper	Pin	Pin	Connection Details
J7	3	4	SPI_SCK to OLED_SCL
	15	16	SPI_SDA to OLED_SDA
JP8	1	2	SPI_0_OUT to OLED_SDA_IN
	5	6	SDI_0_IN to OLED_SDA_OUT
	9	10	SCLK_0_OUT to OLED_SCL
	13	14	SS_0_OUT to OLED_CS#
JP18	1	2	Open
JP23	2	3	OLED_BS1 connected to GND
JP22	2	3	OLED_BS2 connected to GND

Figure 16 • **JP8 Jumper Details**

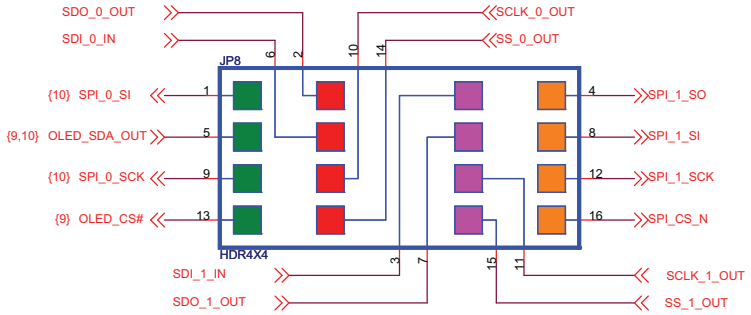


Figure 17 • **MSS SPI0 and SPI1 Settings**

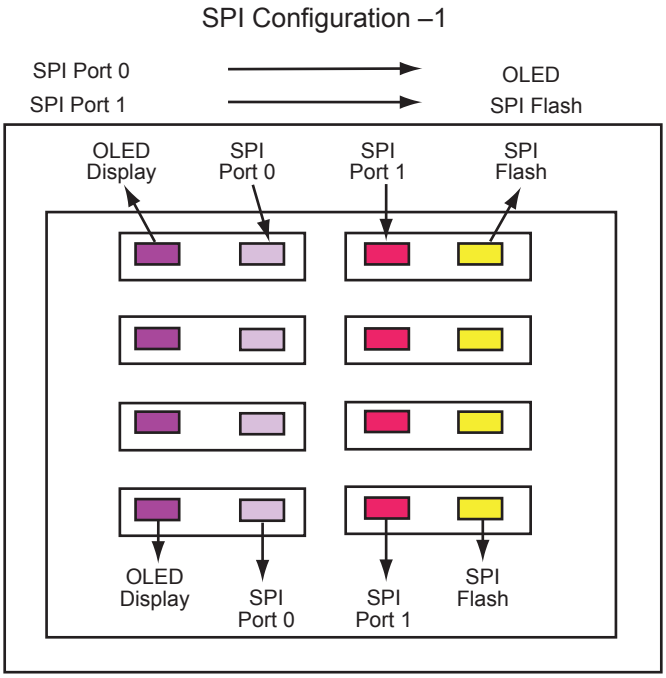


Table 16 • **MSS SPI0 and MSS SPI1 Loopback and Off-Board SPI Device Connections**

Jumper	Pin	Signal	Connection Details

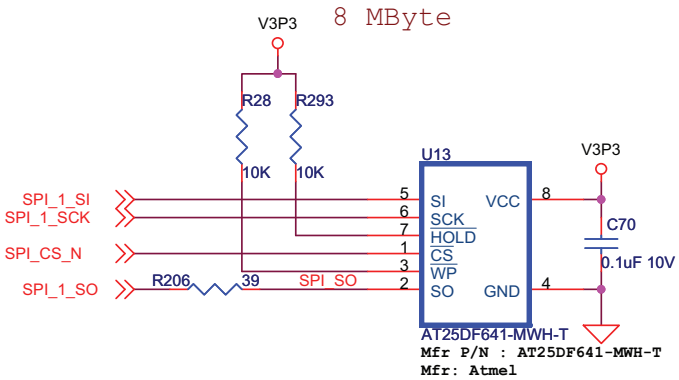
Table 16 • **MSS SPI0 and MSS SPI1 Loopback and Off-Board SPI Device Connections**

JP8	6	SPI0_SDI	To interface any SPI device to MSS SPI0
	2	SPI0_SDO	
	10	SPI0_SCK	
	14	SPI0_SS	
	3	SPI1_SDI	To interface any SPI device to MSS SPI1
	7	SPI1_SDO	
	11	SPI1_SCK	
	15	SPI1_SS	
	6	7	MSS SPI0 and SPI1 loopback
	2	3	
	10	11	
	14	15	

5.8 SPI Flash

One 8-MByte SPI flash SST26VF064B-104I/MN is also offered on the board. This can optionally be interfaced to either the SPI0 or SPI1 peripherals of the SmartFusion MSS. Figure 18, page 25 and Figure 19, page 26 show the SPI flash circuit and the jumper settings to access it from SPI1.

Figure 18 • **SPI Flash**



Note: SPI Flash Part number has been changed please refer to PCN1502 for more information.

Table 17 • **MSS SPI1 to SPI Flash**

Jumper	Pin	Pin	Connection Details
JP8	3	4	SDI_1_IN to SPI_1_SO (SO output of SPI flash)
	7	8	SDO_1_OUT to SPI_1_SI (SI input of SPI flash)
	11	12	SCLK_1_OUT to SPI_1_SCK (SCK input of SPI flash)
	15	16	SS_1_OUT to SPI_CS_N (CS# input of SPI flash)

5.9 SPI DAC

One 12-bit SPI DAC AD5320 is available on the board. This can be optionally interfaced to either the SPI0 or SPI1 of the SmartFusion MSS. The following figure shows the SPI DAC instance along with the

header that must be connected to the SPI_x_SDI, SPI_x_SCK, SPI_x_SS, and SPI_x_SDO pins of SPI0 or SPI1.

Figure 19 • **SPI DAC**

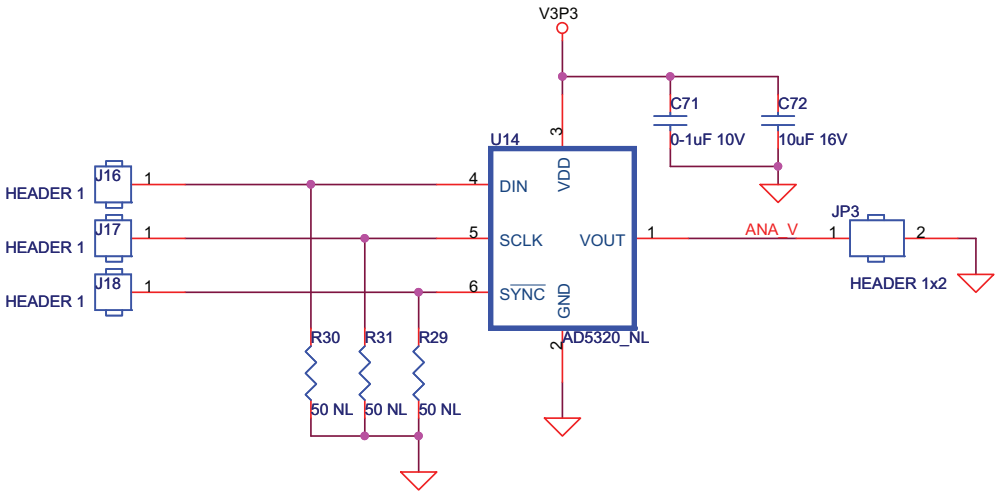


Table 18 • **To Interface MSS SP10 or MSS SPI1 to SPI DAC**

Jumper	Pin	Signal	Header/Jumper	Signal	Connection Details
JP8	6	SPI0_SDI	J16	DIN	To Interface SPI DAC to MSS SPI0
	2	SPI0_SDO	JP3 (Pin1)	VOUT	
	10	SPI0_SCK	J17	SCK	
	14	SPI0_SS	J18	SYNC#	
	3	SPI1_SDI	J16	DIN	To Interface SPI DAC to MSS SPI1
	7	SPI1_SDO	JP3 (Pin1)	VOUT	
	11	SPI1_SCK	J17	SCK	
	15	SPI1_SS	J18	SYNC#	

5.10 I²C EEPROM

One 512-Kbit I2C EEPROM ST M24512-WMN6TP is available on the board to interface with I2C Port1 of the SmartFusion MSS. Alternatively the EtherCAT chip, Beckhoff ET1100, can interface with the EEPROM.

Figure 20, page 27, Figure 21, page 27, and Figure 22, page 28 show the EEPROM connections, I2C interface, and header with jumper settings for access to EEPROM.

Figure 20 • **I²C EEPROM**

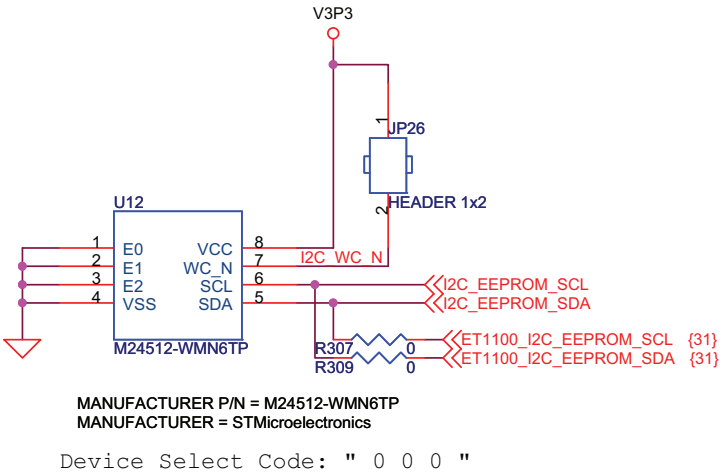


Table 19 • **To Interface MSS I2C1 to EEPROM**

Jumper	Pin	Pin	Connection Details
J7	6	7	I2C_1_SCL to EEPROM_SCL
	14	15	I2C_1_SDA to EEPROM_SDA
JP26	Closed		To write protect EEPROM (WE_N)

Figure 21 • **I²C Interface Terminations**

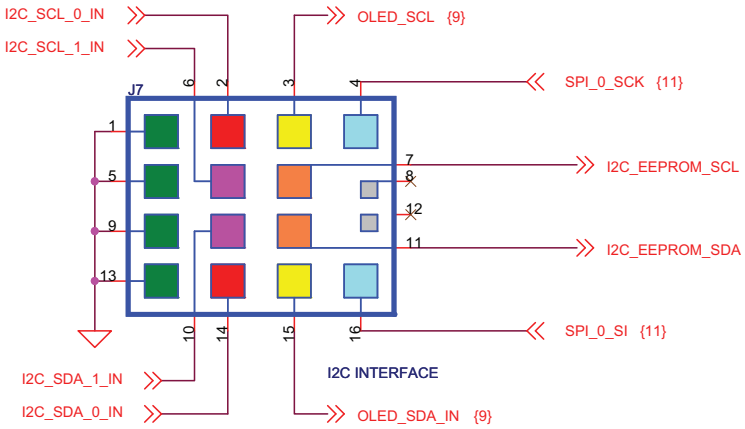
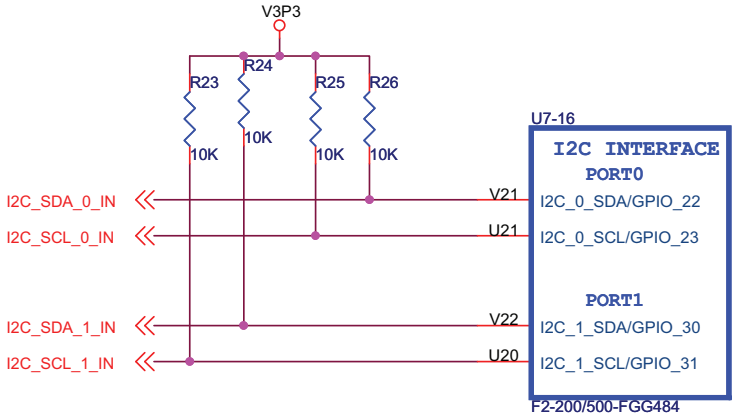


Table 20 • **To Interface EtherCAT ET1100 to EEPROM**

EEPROM PIN	ET1100 PIN	Connection details	Comment
5	G11	EEPROM CLK of ET1100 to SCL of EEPROM	When MSS I²C1 is not driving EEPROM
6	F11	EEPROM DATA of ET1100 to SDA of EEPROM	
JP26	Closed	To write protect EEPROM (WE_N)	

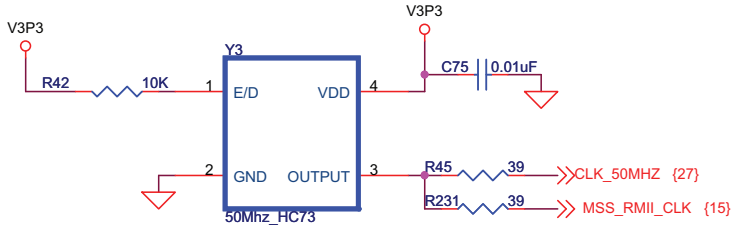
Figure 22 • **I²C Interface Terminations**



5.11 Clock Oscillator

A 50 MHz clock oscillator with 20 PPM is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock and connected to the PHY to provide the RMII_CLK. An on-chip SmartFusion PLL can be configured to generate a wide range of high- precision clock frequencies.

Figure 23 • **50 MHz RC OSC**



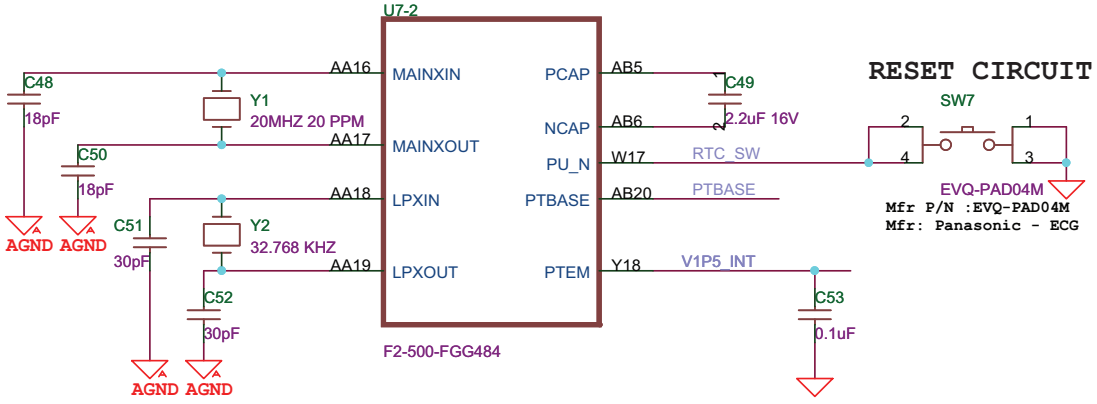
5.11.1 20 MHz Oscillator

A 20 MHz resonator of 20 PPM is placed across the MAINXIN and MAINXOUT pins of the SmartFusion cSoC with the appropriate 18 pF capacitors. This is used to generate high precision clock for Ethernet MAC and also in RTC based applications.

5.11.2 32.768 KHz (low power) Oscillator

A 32.768 KHz resonator, CM519, is placed across the LPXIN and LPXOUT pins of the SmartFusion cSoC with the appropriate 30 pF capacitors. This low-power resonator is useful in RTC based applications.

Figure 24 • **20 MHz and 32.768 KHz Oscillators**



5.12 USB-to-UART Interface

Included on the development board is a USB-to-UART interface with ESD protection (Figure 3-22). This interface includes an integrated USB-to-UART bridge controller (U16) to provide a standard UART connection with the SmartFusion MSS UART0 port.

One application of the USB-to-UART interface is to allow HyperTerminal on a PC to communicate with the SmartFusion cSoC. HyperTerminal is a serial communications application program that can be installed in the Windows operating system. A basic HyperTerminal program is usually distributed with Windows.

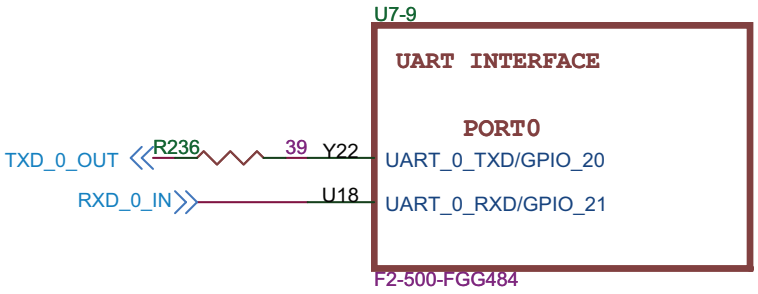
With a USB driver properly installed, and the correct COM port and communication settings selected, you can use the HyperTerminal program to communicate with a design running on the SmartFusion cSoC.

The following table lists the supported UART parameters, such as baud rate, for HyperTerminal application.

Table 21 • **UART HyperTerminal Settings**

Supported HyperTerminal Parameters			
Baud Rates	**Data Bits**	**Parity Types**	**STOP BIT**
110	5, 6, 7, 8	NO/ODD/EVEN/MARK (1)/SPACE (0)	ONE/ONE-HALF/TWO
300			
1200			
2400			
4800			
9600			
19200			
38400			
57600			
115200			
230400			
460800			
921600			

Figure 25 • **USB-to-UART**



5.13 RS485 Interface

Included on the development board is an RS485 with DB9 female connector, interfacing with the MAX3240CSA connected to UART port 1 (Figure 26, page 30, Figure 27, page 30, and Figure 28,

page 31) of the SmartFusion MSS. This is provided for applications that require RS485, for which the UART port needs to be used in MODEM mode.

Figure 26 • **RS485**

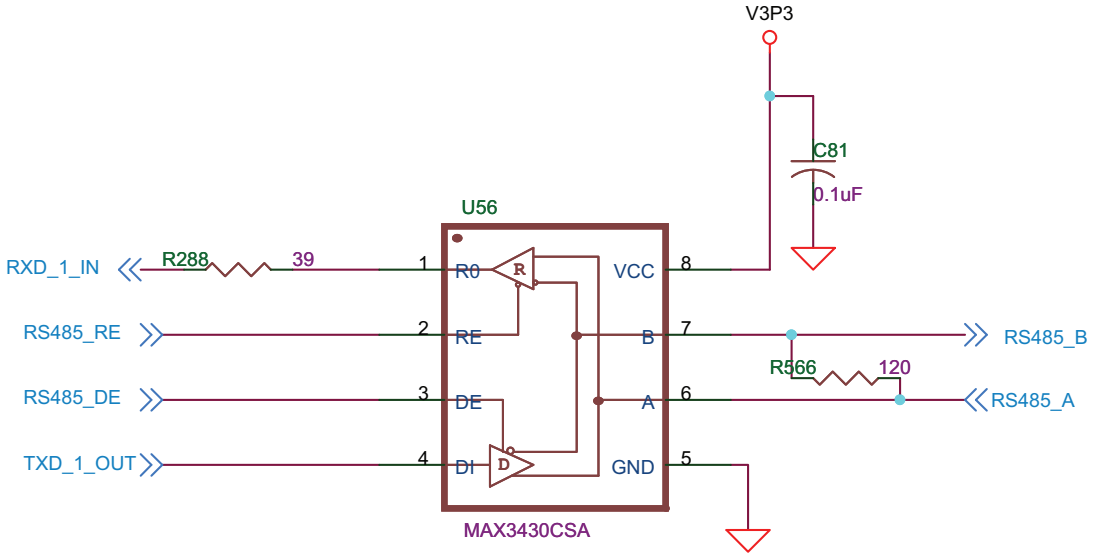


Figure 27 • **SmartFusion UART Port 1**

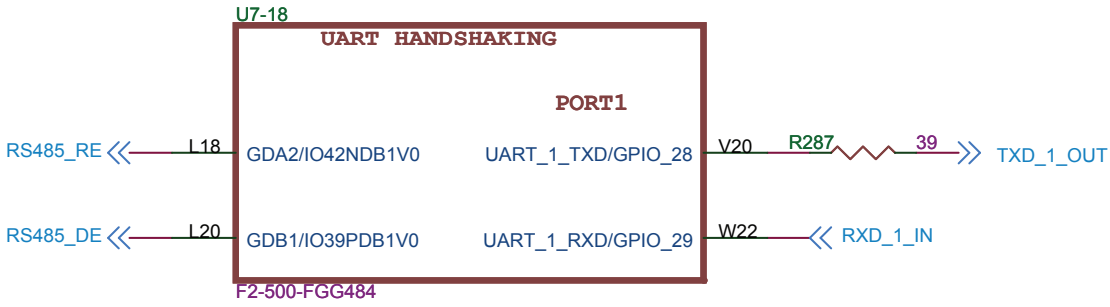
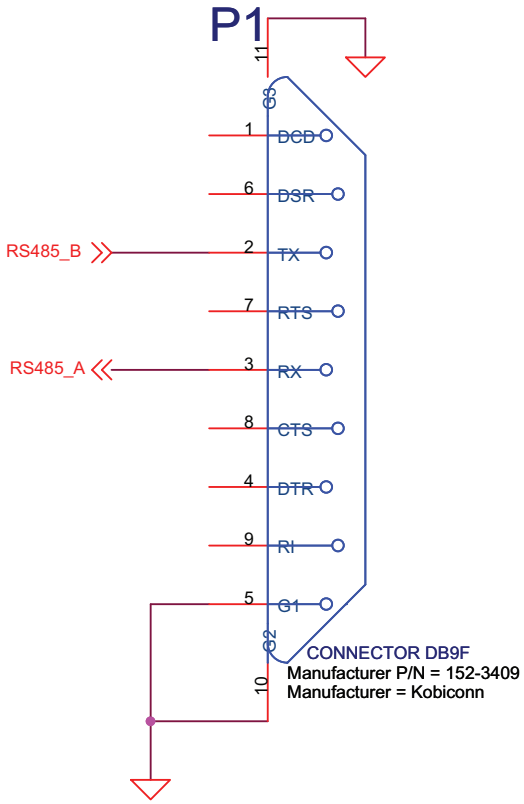


Figure 28 • **DB9 Connector**



5.14 Ethernet Interface

One Ethernet interface, configured for RMII full duplex mode, and a low-power 10/100 Mbps single-port Ethernet physical layer transceiver (U19) are provided on-board (Figure 3-27 on page 36). The Ethernet physical layer features integrated sub-layers to support both 10BASE-T and 100BASE-TX Ethernet protocols. These sub-layers ensure compatibility and interoperability with many other standards-based Ethernet solutions.

The Ethernet RJ45 interface and physical layer, the interface with the SmartFusion MSS Ethernet media access controller (MAC) which supports RMII, serves many purposes. For example, this interface can be used to access the SmartFusion cSoC to monitor the ADC data over a network. The embedded system memory and control registers can be accessed and processed remotely to support system management.

5.14.1 Clocking Scheme for RMII CLK

The 10/100 MAC RMII interface requires a 50 MHz clock. The PHY device also requires a 50 MHz 20 PPM clock for proper operation. While there are a few possible ways of providing the clock, the following two schemes are discussed:

Clocking Scheme 1: From 50 MHz clock oscillator

- 50 MHz oscillator goes as input to CCC and to the X1 clock input of Ethernet PHY through GPIO
- The GLC output of CCC, which is also at 50 MHz, feeds MAC_CLK of 10/100 MAC

Clocking Scheme 2: From 20 MHz clock oscillator

- 20 MHz oscillator goes as input to CCC. GLC output of CCC is configured at 50 MHz
- The GLC output of CCC feeds MAC_CLK of 10/100 MAC
- The same GLC output of CCC feeds X1 clock input of Ethernet PHY through GPIO

Figure 29 • **Ethernet Clocking**

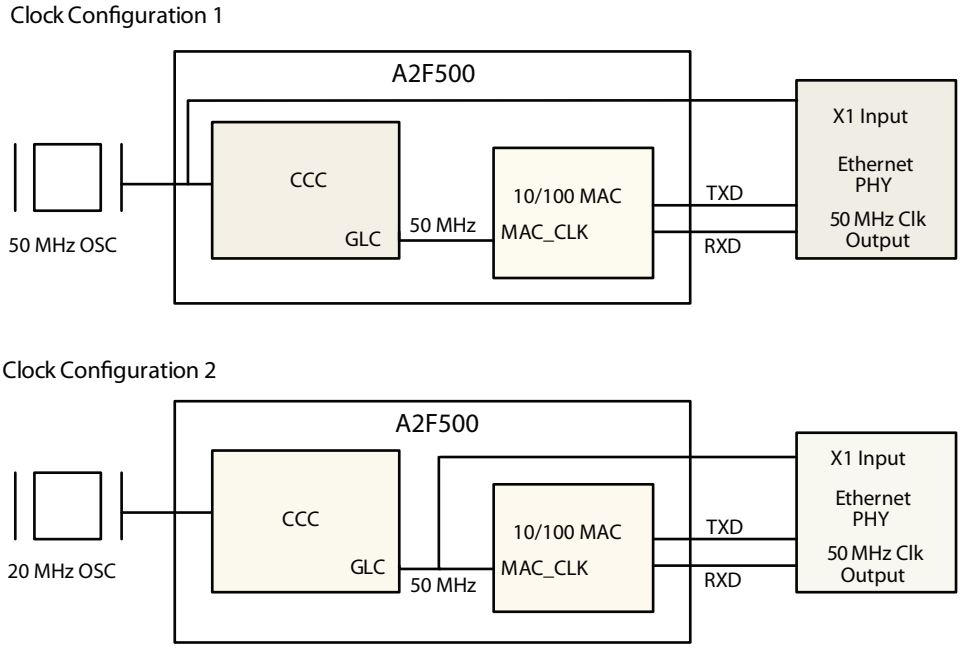
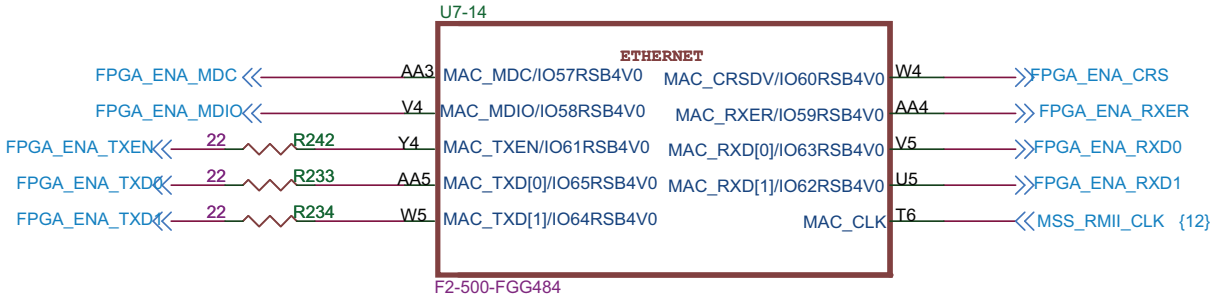


Figure 30 • **Ethernet Interface**



5.15 Memory Section Overview

The SmartFusion MSS provides options to interface with a variety of external memory devices such as NOR flash and synchronous or asynchronous SRAM for large applications code. The external memory controller (EMC) interface of SmartFusion MSS is 3.3 V LVTTL compliant. This interfaces directly with

3.3 V SRAM and flash devices. On the development board, two 16-Mbit SRAM Cypress CY7C1061DV33-10ZSXI and two 64-Mbit parallel flash memory Numonyx JS28F640J3D-75 memories interface with EMC region0 and region1. Microsemi expects these memories to be used in most SmartFusion applications.

For applications that require larger SRAM memory than this, an alternative 128-Mbit, 1.8 V asynchronous PSRAM Micron® MT45W8MW16BGX is also offered. Given that memories of this size are only available at 1.8 V, coupled with the fact that the EMC interface does not allow region0 and region1 to

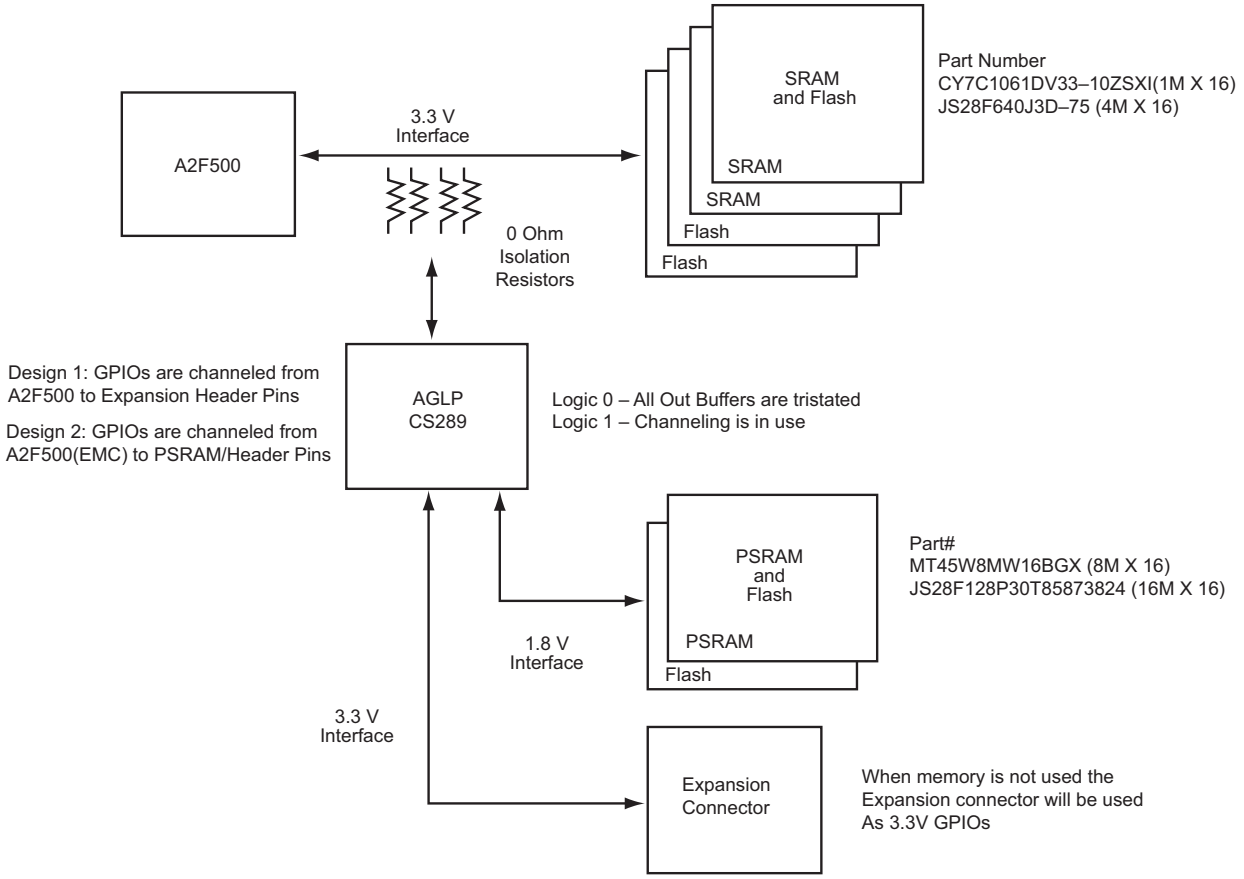
be completely independent of each other due to shared chip select, 128-Mbit, 1.8 V, parallel flash memory Numonyx JS28F128P30T85 873824 is mounted on the board as a companion for the 1.8 V SRAM. This requires a 3.3 V to 1.8 V conversion to interface the 3.3 V EMC with these 1.8 V memories.

If the EMC is not used, the shared EMC I/Os are available as 3.3 V GPIO at the expansion connector. To provide the option of a 1.8 V interface and to make the EMC I/Os available to user application, an AGLP125 FPGA is used as an I/O translator on the board. Based on the EMC configuration selected, the AGLP125 can be programmed either as a 3.3 V to 1.8 V level converter or I/O extender (with all 3.3 V

and 1.8 V memories held in tristate). This device can be selectively programmed by choosing appropriate jumper settings to select the JTAG chain.

The following figure captures the memory section overview.

Figure 31 • **Memory Top Level**



5.15.1 3.3 V Memory Section

Mounted on the development board are two instances of 16-Mbit asynchronous SRAM. Also included are two 64-Mbit parallel flash memories (FLASH). Both instances of the asynchronous SRAM are connected to region0 of the EMC interface of the SmartFusion MSS. Similarly both instances of the flash are connected to region1 of the EMC interface of the SmartFusion MSS. These operate at 3.3 V and are directly interfaced to the EMC. The AGLP125 FPGA is not used in this case and is held in Flash*Freeze mode to avoid any power consumption.

The following table gives the summary of jumper settings needed to access the 3.3 V memories.

Table 22 • **Jumper Settings to Interface EMC with 3.3 V Memories (SRAM and flash)**

Jumper	Pin	Pin	Connection Details
JP17	2	3	EMC chip select for region0 to CS1 of SRAM
JP19	2	3	EMC chip select for region1 to CS1 of flash
JP24	1	2	FLASH_VPEN to 3.3 V (to enable 3.3 V flash)
JP16	2	3	To keep AGLP125 in Flash*Freeze mode

5.15.2 Asynchronous SRAM Memory Components

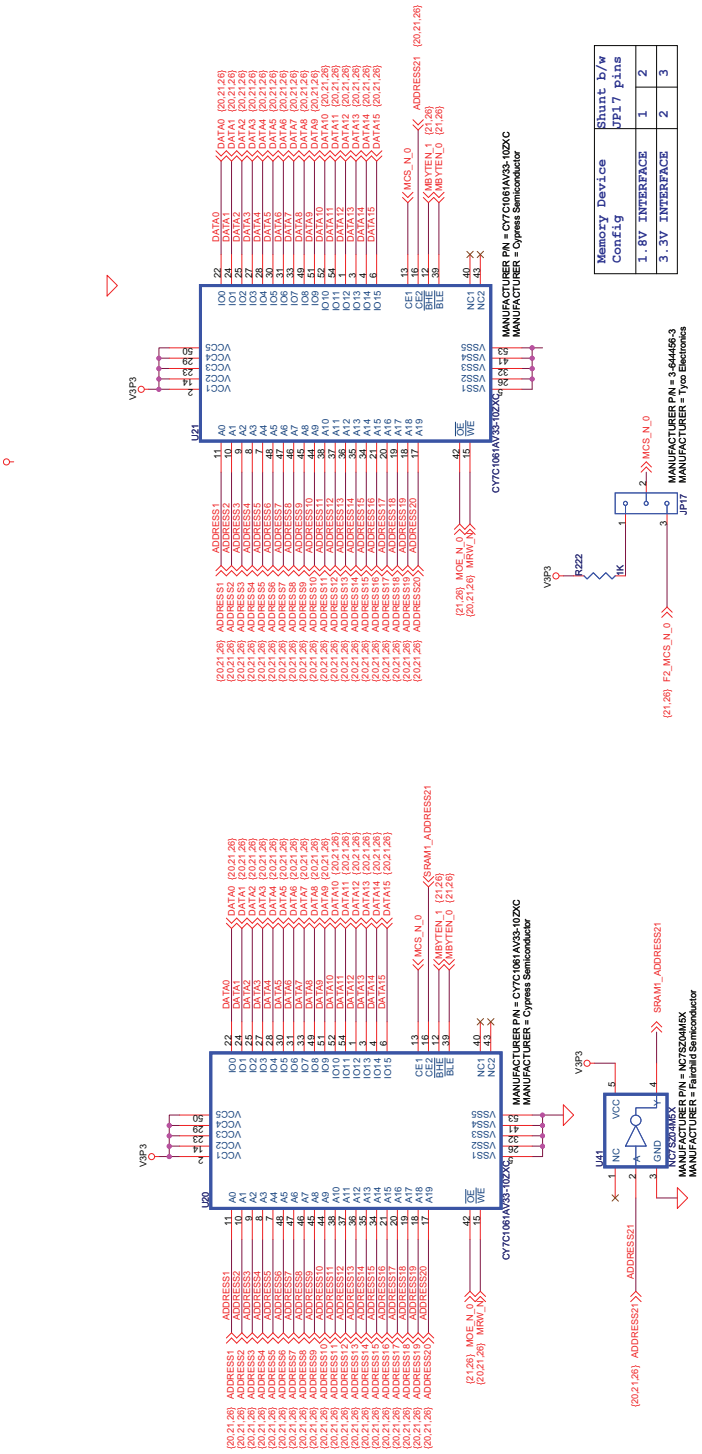
The 3.3 V asynchronous SRAMs populated on the board are 16-Mbit SRAM Cypress CY7C1061DV33-10ZSXI (PSRAM), as shown in Figure 32, page 35. These interface with the EMC port of the SmartFusion MSS. They provide a reasonable off-chip memory at high speed that the hard ARM Cortex-M3 processor can use for applications such as RTOS.

Performance Note: The following table lists the External Memory Controller settings for 100 MHz and 80 MHz system performance. A slower speed device might work at higher speed—but it is not always guaranteed. These are obtained on the development board with an application that uses asynchronous SRAM extensively.

Table 23 • **EMC Settings for 3.3 V Asynchronous SRAM Performance**

Port Size: Half Word		
	System Clock Frequency FCLK (HCLK)	
Latency in FCLK(HCLK) Cycles	100 MHz	80 MHz
Read Latency for First Access	1	1
Read Latency for Remaining Accesses	1	1
Write Latency	0	0

Figure 32 • **PSRAM Connections**



5.15.3 Parallel Flash Memory Components (Flash)

Two 64-Mbit parallel flash memories, Numonyx JS28F640J3D-75, are the 3.3 V flash memory instances populated on the board (Figure 3-30 on page 41). They interface with the EMC port of the SmartFusion MSS and provide off-chip high-speed nonvolatile memory that the hard ARM Cortex-M3 processor can use for applications such as storing compressed Linux images, which can be uncompressed using the SmartFusion MSS eNVM and stored into asynchronous SRAM.

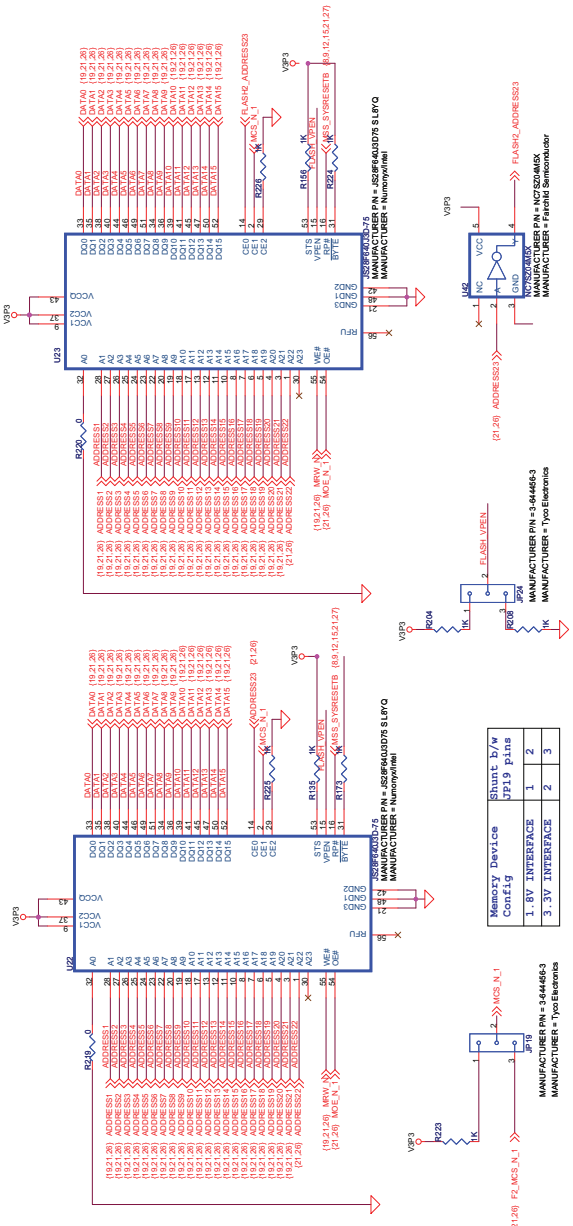
Performance Note: The following table lists the EMC settings for 100 MHz and 80 MHz system performance. These are obtained on the development board with an application that uses parallel flash extensively.

Table 24 • **EMC Settings for 3.3 V Parallel Flash Performance**

Port Size: Half Word		
	System Clock Frequency FCLK (HCLK)	
Latency in FCLK(HCLK) Cycles	100 MHz	80 MHz
Read Latency for First Access	5	4
Read Latency for Remaining	1	1
Write Latency	0	0

Note: Ensure to keep the AGLP125 device in Flash*Freeze mode by closing pins 2-3 of JP16.

Figure 33 • **Flash Connections**



5.15.4 1.8 V Memory Section Overview

Included on the development board one instance of 128-Mbit, 1.8 V, high density asynchronous SRAM (LG_PSRAM) interfacing region0 of the SmartFusion MSS EMC interface and 128-Mbit, 1.8 V, parallel flash memory (LG_FLASH) interfacing region1 of the EMC interface of SmartFusion MSS (Figure 3-31 on page 43). These operate at 1.8 V. The AGLP125 device must be programmed with the 3.3 V to 1.8 V converter design to access these memories. The following table lists the summary of jumper settings needed to access the 1.8 V memories.

Table 25 • **Jumper Settings to Interface EMC with 1.8 V Memories (LG_SRAM and LG_FLASH)**

Jumper	Pin	Pin	Connection Details
Program AGLP125 with 3.3 V to 1.8 V Conversion Design			

Table 25 • Jumper Settings to Interface EMC with 1.8 V Memories (LG_SRAM and LG_FLASH)

JP17	1	2	To keep 3.3 V SRAM in tristate (deselect)
JP19	1	2	To keep 3.3 V flash in tristate (deselect)
JP24	2	3	FLASH_VPEN to GND (to disable 3.3 V flash)
JP16	1	2	To keep AGLP125 in active mode
JP25	1	2	FLASH_WP# to VCC (to disable protect)

5.15.5 Large PSRAM Memory Component (LG_PSRAM)

One 128-Mbit, 1.8 V asynchronous SRAM, Micron MT45W8MW16BGX, is the PSRAM mounted on the board (Figure 3-31 on page 43). This memory interfaces with region0 of the SmartFusion MSS EMC. It provides extensive off-chip memory that the hard ARM Cortex-M3 processor can use for applications such as operating systems and three frames of buffering for WVGA display.

Note: PSRAM component is no longer populated in the latest revision of this board. For more information, see *PCN1502: Change in SmartFusion Development Kit (A2F500-DEV-KIT-2) hardware*.

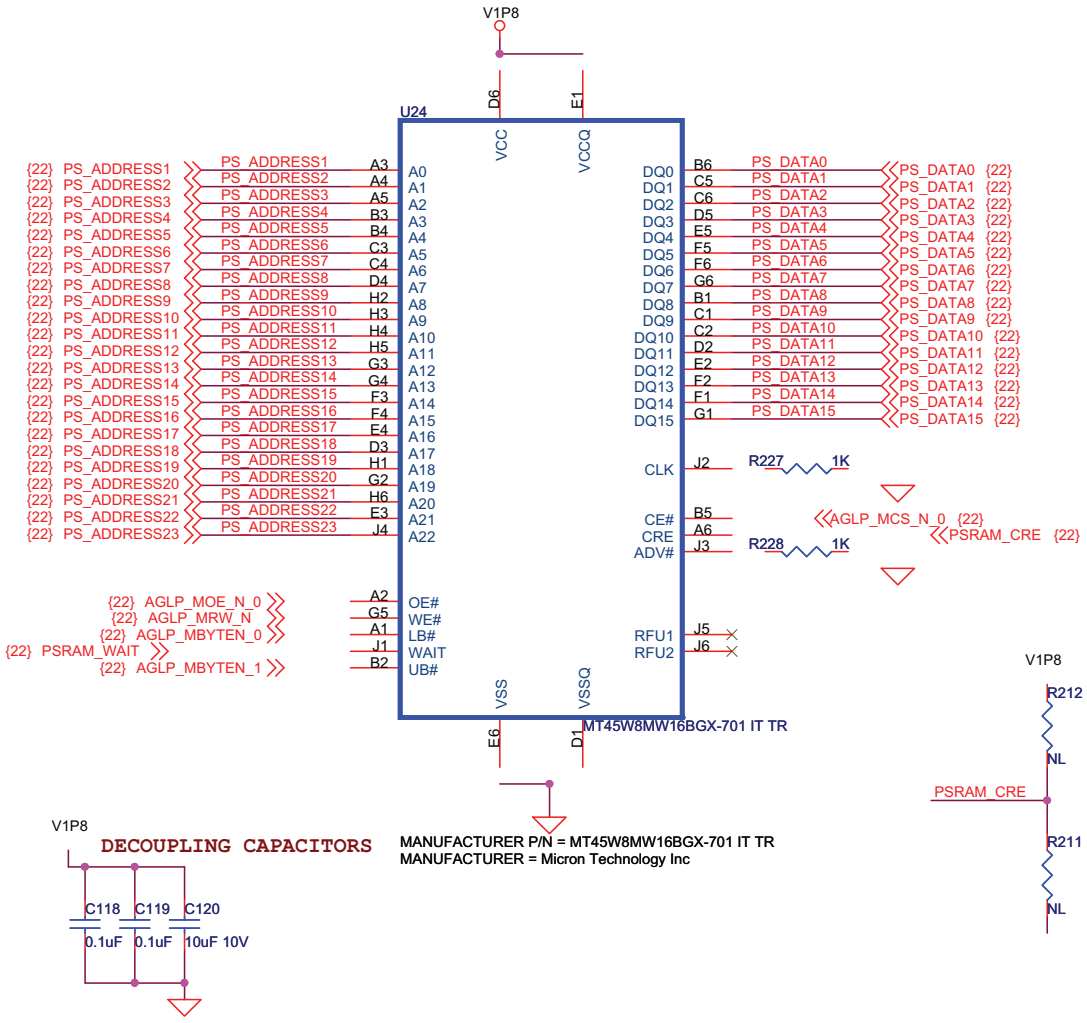
The following table lists the EMC settings for 100 MHz and 80 MHz system performance. These are obtained on the development board with an application that uses Large PSRAM extensively.

Table 26 • EMC Settings for 1.8 V PSRAM Performance

Port Size: Half Word		
	System Clock Frequency FCLK (HCLK)	
Latency in FCLK (HCLK) Cycles	100 MHz	80 MHz
Read Latency for First Access	5	4
Read Latency for Remaining Accesses	5	4
Write Latency	3	2

Note: The AGLP125 device should be programmed with the 3.3 V to 1.8 V converter design. Also it must be put in operational mode by closing pins 1-2 of JP16.

Figure 34 • **1.8 V SRAM**



5.15.6 Large Parallel Flash Memory Component (LG_FLASH)

One 128 Mbit, 1.8 V, parallel flash memory, Numonyx JS28F128P30T85 873824, is the LG_FLASH mounted on the board (Figure 3-32). This memory interfaces with region0 of the SmartFusion MSS EMC. It provides a larger off-chip nonvolatile memory that the hard ARM Cortex-M3 processor can use for applications such as storing compressed Linux images, which can be uncompressed within SmartFusion MSS eNVM and stored into LG_SRAM.

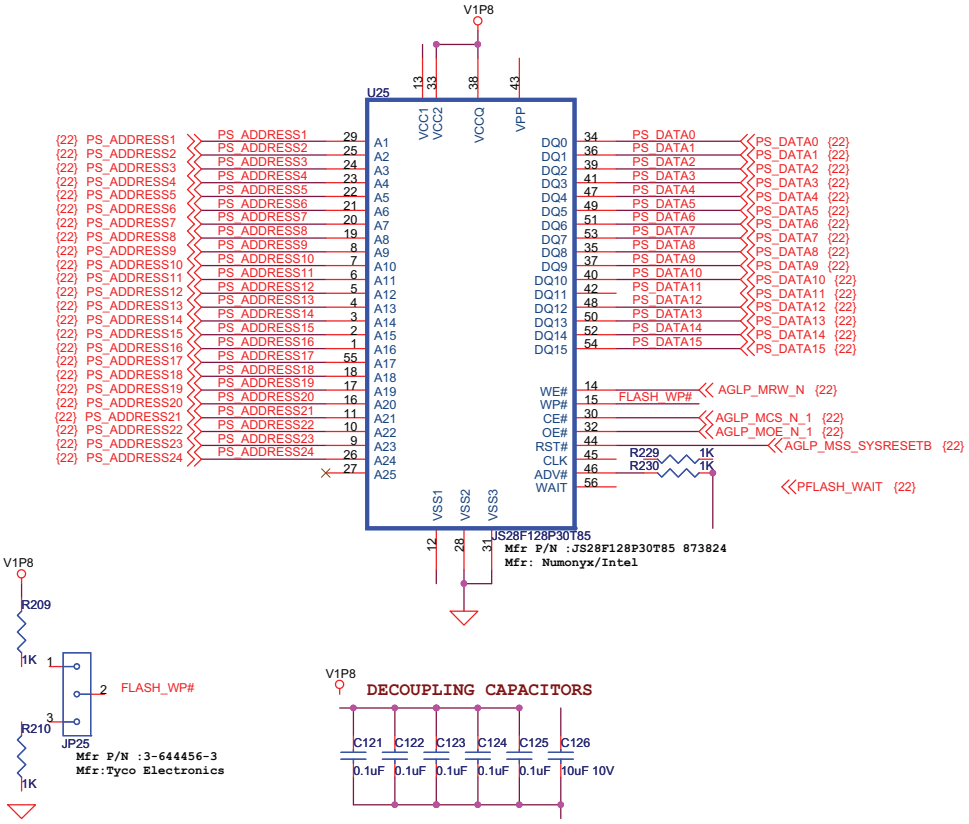
Performance Note: The following table lists the EMC settings for 100 MHz and 80 MHz system performance. These are obtained on the development board with an application that uses LG_FLASH.

Table 27 • **EMC Settings for 1.8 V Parallel Flash Performance**

Port Size: Half Word		
	System Clock Frequency FCLK (HCLK)	
Latency in FCLK (HCLK) Cycles	100 MHz	80 MHz
Read Latency for First Access	7	6
Read Latency for Remaining Accesses	2	2
Write Latency	0	0

Note: The AGLP125 device should be programmed with the 3.3 V to 1.8 V converter design. Also it must be put in operational mode by closing pins 1-2 of JP16.

Figure 35 • **1.8 V Flash**



5.16 Using EMC I/Os as User I/Os

When user applications do not require the EMC interface, the shared EMC I/Os can be used as general purpose I/Os. On the A2F500-DEV-KIT-2 board, this requires the mounted AGLP125 FPGA to be programmed with an IN to OUT design that provides a through path via the FPGA to the expansion connector for 3.3 V I/O. In addition, the jumper settings lists in the following table are needed.

Table 28 • **Using I/O Expander When EMC Is Not Used at All**

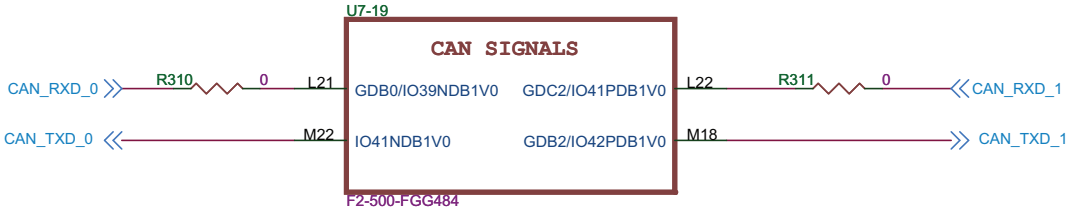
Jumper	Pin	Pin	Connection Details
Program AGLP125 with design that provides IN-OUT paths at 3.3 V			
JP17	1	2	To keep 3.3 V SRAM in tristate (deselect)
JP19	1	2	To keep 3.3 V flash in tristate (deselect)
JP24	2	3	FLASH_VPEN to GND (to disable 3.3 V flash)
JP16	1	2	To keep AGLP125 in Active mode
JP25	2	3	FLASH_WP# to GND

5.17 Controller Area Network Interface

Included on the development board are two controller area network interfaces. Controller area network (CAN) is an automobile standard designed to allow microcontrollers and devices to communicate with each other within an automotive system without a host computer. While it is designed for automotive applications, currently it is used in other applications such as industrial automation, avionics, and medical

equipment. Each CAN interface is implemented with a DB9 female connector interfacing with a MAXIMMAX3051 CAN transceiver and uses two GPIOs of the A2F500 device, with the SmartFusion MSS acting as microcontroller. These can be used in applications such as FieldBus.

Figure 36 • **CAN Interface**



5.18 Ethernet for Control Automation Technology Interface

Included on the development board is an ethernet for control automation technology (EtherCAT) interface (Figure 3-34, Figure 3-35, and Figure 3-36 on page 47). EtherCAT is an open, high performance, and Ethernet-based FieldBus system. EtherCAT applies Ethernet to automation applications that require short data update times with low communication jitter and low hardware costs.

Typical industrial automation networks are characterized by short data length per node, typically less than the minimum payload of an Ethernet frame. Using one frame per node per cycle therefore leads to low bandwidth utilization and thus poor overall network performance. EtherCAT therefore takes a different approach, called "processing on the fly."

Each interface uses an RJ45 connector (Ethernet jack with Magnetics), interfacing with Beckhoff ET1100 and Micrel KS8721BL and connecting to the FPGA fabric via a soft CoreSPI interface that is implemented in the FPGA array. This interface uses six GPIOs.

The Beckhoff ET1100 ASIC interfaces with the I2C EEPROM. When EEPROM is used by EtherCAT, it is not available for the I2C1 interface of the SmartFusion MSS to I2C1 interface. The following table lists the jumper settings.

Table 29 • **EtherCat Jumper Setting to Interface EtherCAT ET1100 to EEPROM**

EEPROM PIN	ET1100 PIN	Connection Details	Comments
5	G11	EEPROM CLK of ET1100 to SCL of EEPROM	When MSS I2C1 is not driving EEPROM
6	F11	EEPROM DATA of ET1100 to SDA of EEPROM	
JP26	Closed	To write protect EEPROM (WE_N)	

The following figure shows the EtherCAT interface.

Figure 37 • **EtherCAT Block Diagram**

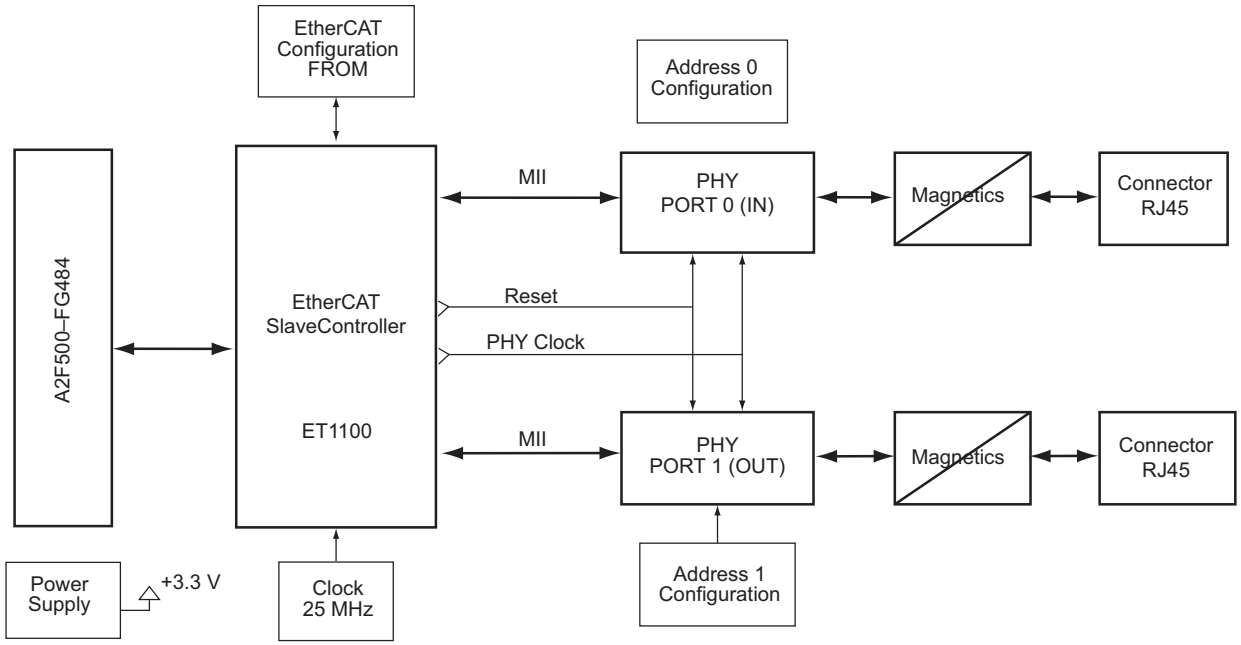


Figure 38 • **EtherCat Port0**

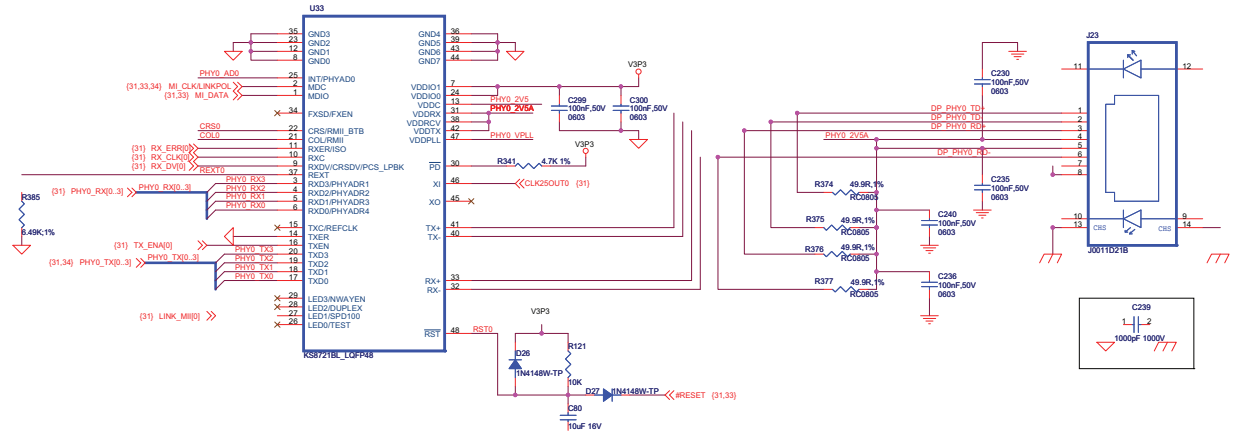
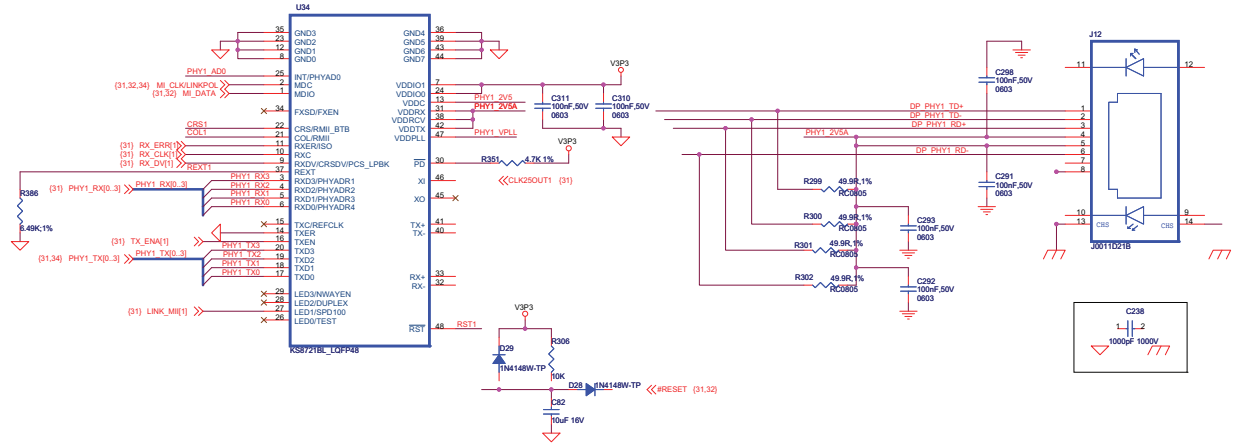


Figure 39 • **EtherCat Port1**



5.18.1 Low-Cost Programming Stick Header

The board provides a low-cost programming stick (LCPS) header to connect a LCPS for programming. The SmartFusion A2F500 can be programmed by the LCPS. The LCPS programs the device through the JTAG pins. The LCPS can be used to debug software application with SoftConsole. The 12-pin female connector socket is designed to interface to the 12-pin right-angle male header on the SmartFusion Development Kit board.

Refer to the schematic shown in the following figure. Jumper settings are shown in Table 30, page 43for A2F500 programming and SoftConsole application debug.

Figure 40 • **JTAG Header Schematic for LCPS Connection**

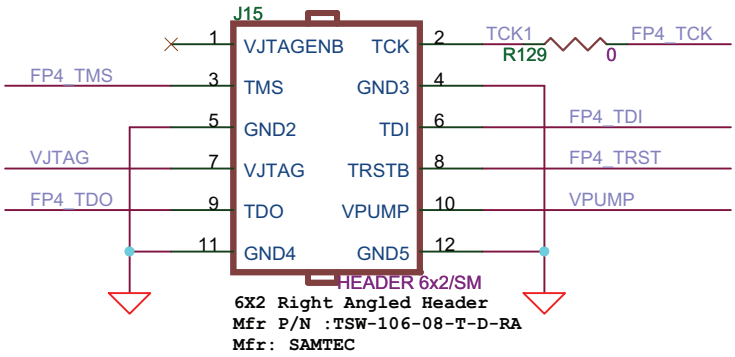


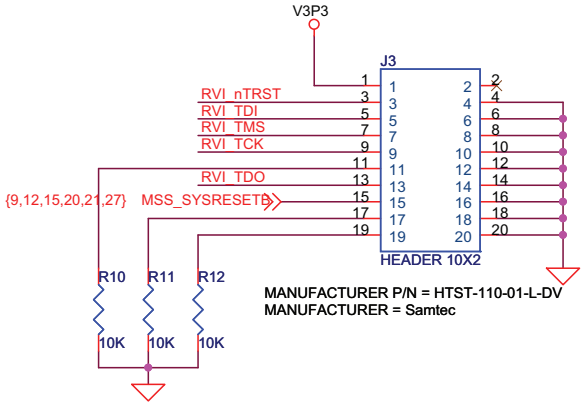
Table 30 • **Jumper Settings for A2F500 Programming and SoftConsole Debug**

Jumper	Pin	Pin	Connection Details
SW9	OFF		JTAG selection for programming and Cortex-M3 processor Debug
JP11	1	2	To provide 3.3 V to VJTAG
JP12	1	2	To provide 3.3 V to VPUMP
JP5	1	3	To select A2F500 in JTAG chain
JP7	1	2	LCPS for SoftConsole application debug

5.19 RealView Header

One 10X2 RealView header is provided on the board for debugging. This header allows plugging in the Keil ULINK debugger or IAR J-Link debugger to easily debug or configure the hard ARM Cortex-M3 processor during board power-up.

Figure 41 • **RVI Header**



The jumper settings shown in the following table are needed for debug with Keil ULINK or IAR J-Link.

Table 31 • **RVI Header Jumper Settings to Debug with Keil ULINK or IAR J-Link**

Jumper/Switch	Pin	Pin	Connection Details
SW9	ON		To select Cortex-M3 processor JTAG
JP5	1	3	To select A2F500 in JTAG chain
JP7	2	3	To select Real View JTAG header

5.20 Direct-C Programming Interface

On the development board, a standard FlashPro4 10-pin connector is provided to support DirectC programming (Microsemi's in-system programming solution with DirectC). This connector interfaces with five GPIOs and follows the same pinout as FlashPro4. This can be used to program a Microsemi FPGA on another board (Figure 3-40) with either hard ARM Cortex-M3 processor or a soft processor implemented in an FPGA array, such as Cortex-M1. Table 3-24 shows the configuration details for the target board.

Figure 42 • **DirectC Programming**

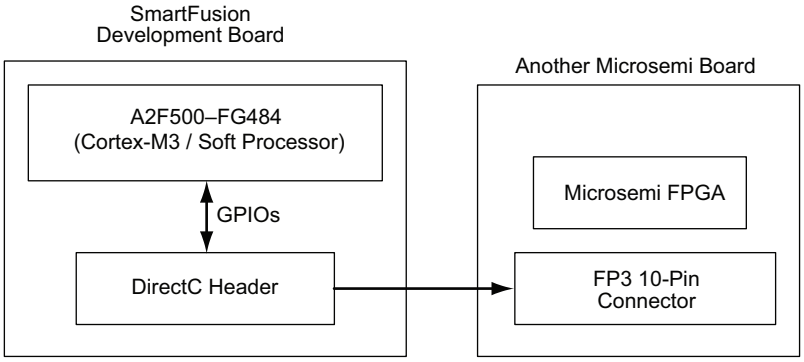


Figure 43 • **DirectC Header**

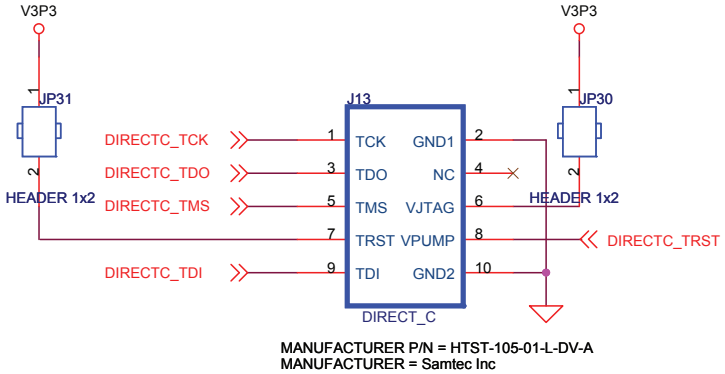


Table 32 • **VPUMP/VJTAG Configuration on Target Board**

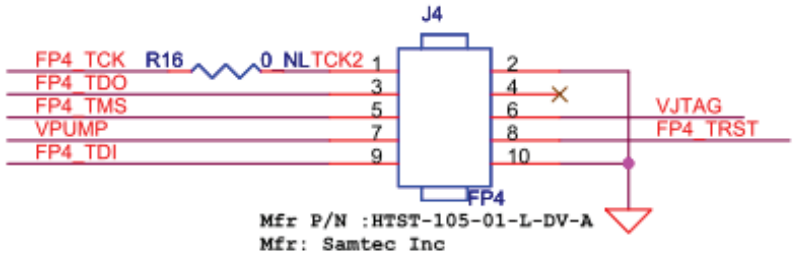
VPUMP/VJTAG	JP30	JP31
Connected to 3.3 V	Open	Closed
Powered through FP4	Closed	Closed

5.21 FlashPro4 Programming Header

The SmartFusion cSoC device on this Development Kit Board can be programmed using a FlashPro4 programmer (Figure 3-41). Using the jumper settings in Table 33, page 45, A2F500 and AGLP125 devices can be programmed independently or in chain mode.

In addition, FlashPro4 is used for software debugging by SoftConsole.

Figure 44 • **FlashPro4 Header**

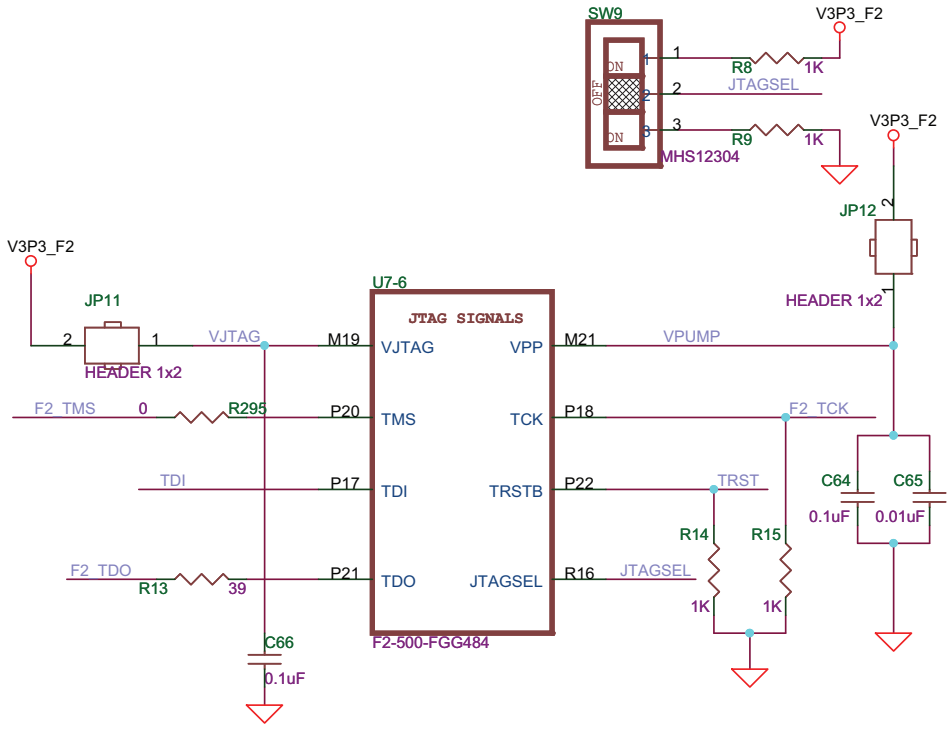


To program A2F500, the jumper settings shown in Table 3-25 are required.

Table 33 • **A2F500 Programming with FlashPro4**

Jumper/Switch	Pin	Pin	Connection Details
SW9		Off	To select A2F500 JTAG
JP11	1	2	To provide 3.3 V VJTAG
JP12	1	2	To provide 3.3 V VPUMP
JP5	1	3	To select A2F500 in JTAG chain
JP7	1	2	To select FP4 JTAG header

Figure 45 • **SmartFusion JTAG**

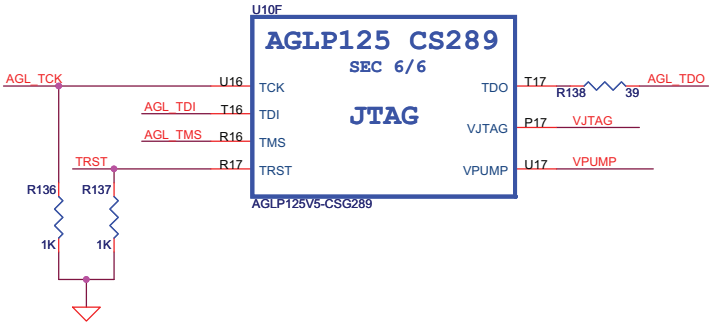


To program AGLP125 with FlashPro4, the settings shown in the following table are required.

Table 34 • **AGLP125 Programming with FlashPro4**

Jumper/Switch	Pin	Pin	Connection Details
SW9		OFF	To select programming JTAG Port
JP11	1	2	To provide 3.3 V VJTAG
JP12	1	2	To provide 3.3 V VPUMP
JP5 settings to bring A2F500 and AGP125 into JTAG chain for programming			
JP5	1	2	To connect A2F500_TDO to AGLP125_TDI (marked C2 "->")
JP5	3	4	To connect AGLP125_TDO to MUX_TDO (marked C2 "<-")
JP7	1	2	To select FlashPro4 JTAG Header
JP16	2	3	To bring AGLP125 out of Flash*Freeze

Figure 46 • **IGLOO PLUS JTAG**



To debug applications with SoftConsole, which uses FlashPro4, the settings shown in following table are required.

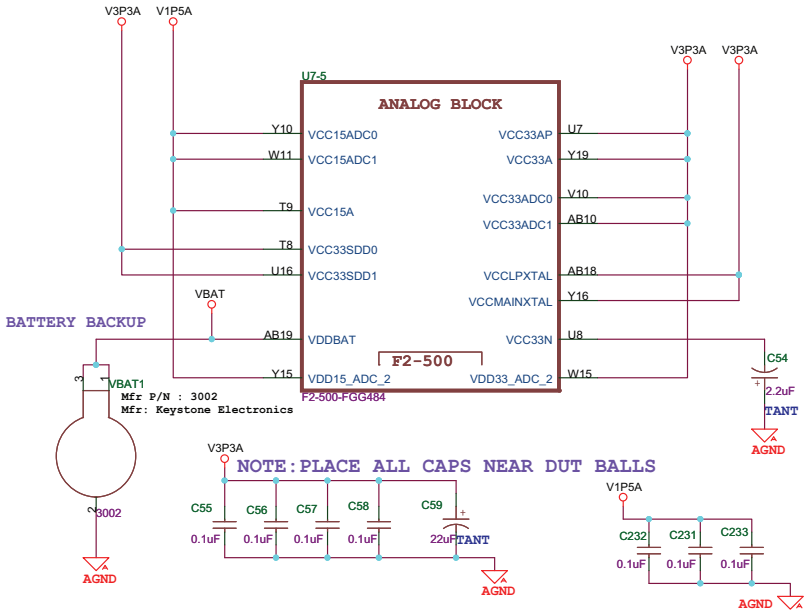
Table 35 • **SoftConsole Debug Settings for FlashPro4**

Jumper/Switch	Pin	Pin	Connection Details
SW9		On	To select Cortex-M3 processor JTAG for SC
JP11	1	2	To provide 3.3 V VJTAG
JP12	1	2	To provide 3.3 V VPUMP
JP5	1	3	To connect A2F500_TDO to MUX_TDO (marked C1 "->"). This brings A2F500 in JTAG chain.
JP7	1	2	To select FlashPro4 JTAG header

5.21.1 Battery Back-Up

A 3.0 V Lithium ion battery, CR2032, is provided on the board. This connects to the VDDBAT input of the SmartFusion cSoC. This is useful in demonstrating battery backup and power-down modes of the SmartFusion cSoC.

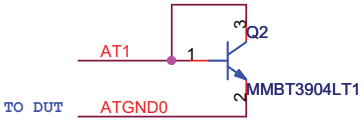
Figure 47 • **Battery Backup**



5.21.2 Temperature Diode

A temperature diode is provided on the board to measure ambient temperature. This is used in battery charging and MPM applications. This diode is connected to the AT1 input of the SmartFusion cSoC.

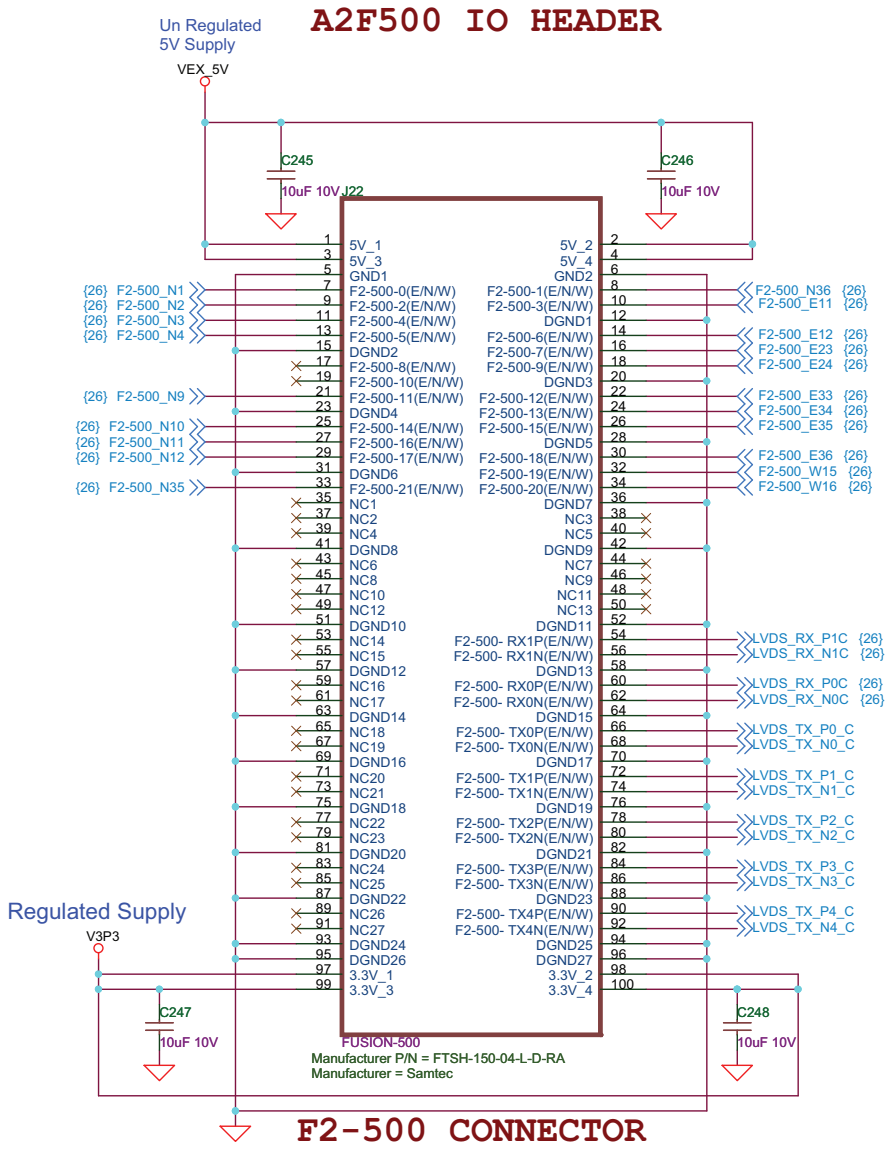
Figure 48 • **Temperature Diode**



5.22 A2F500 Digital I/O Expansion Header

The board provides a digital I/O expansion header to interface with a daughter board with a digital interface. This digital header provides an interface to A2F500 fabric I/Os which includes seven pairs of LVDS TX/RX I/Os with proper termination. This enables designers to interface touch screen and LCD modules to the SmartFusion A2F500 device. Refer to the schematic shown in the following figure for the pinout definition.

Figure 49 • **A2F500 Digital I/O Expansion Header**

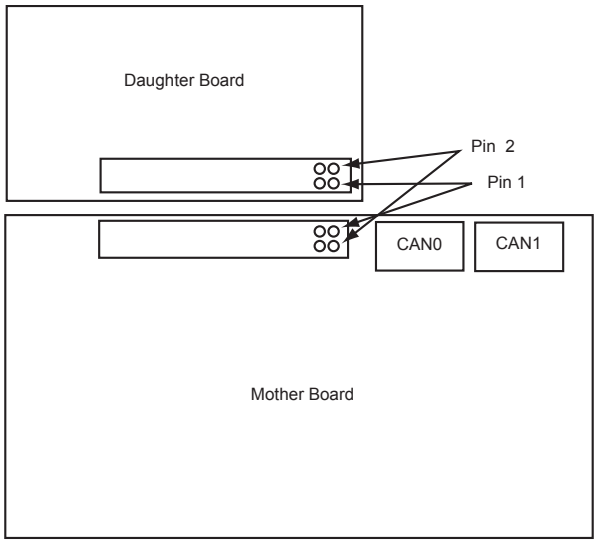


The instructions given below must be followed while designing daughter board to ensure the correct orientation of the digital I/O expansion header on the mother board and daughter board. The A2F500 I/O expansion header can be obtained from Samtec, using the following part numbers:

- Mother board header 2x50 50 mil pitch: Samtec FTSH-150-04-L-D-RA (populated on the development board)
- Daughter board header 2X50 50 mil pitch: Samtec CLP-150-02-L-DH

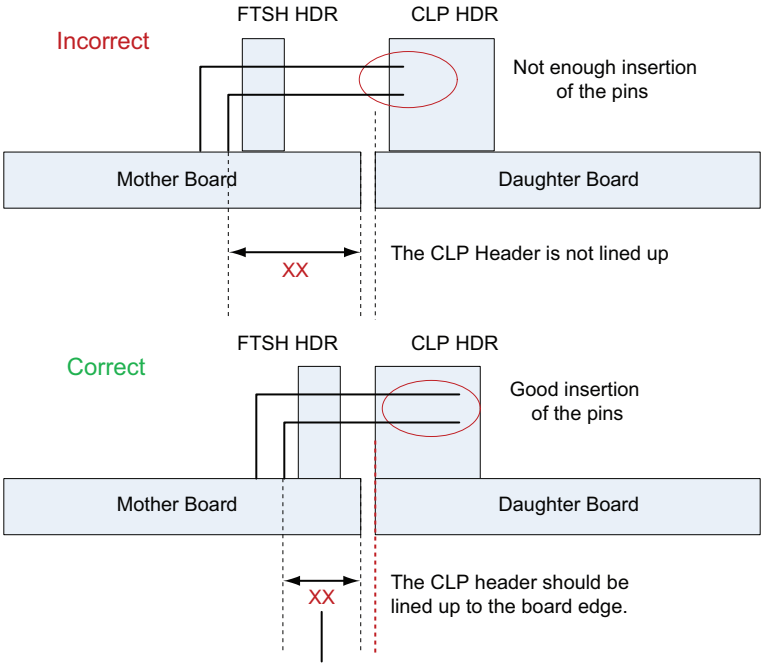
The following figure (top view) indicates the orientation of the digital I/O expansion headers on the mother board and daughter board.

Figure 50 • **Top View of A2F500 Digital I/O Expansion Headers Correct Orientation**



Note: On the mother board there are two CAN ports just adjacent to the A2F500 digital I/O expansion header, so the daughter card header needs to be placed in such a way that a full insertion is possible between the two headers.

Figure 51 • **Correct Insertion of Daughter Board**



When designing a daughter board to plug into an A2F500-DEV-KIT-2:

- Ensure the CLP header edge is lined up against the edge of the board.
- This will provide maximum insertion into the SmartFusion evaluation board.
- Use the SmartFusion Development Kit PCB files (www.microsemi.com/soc/download/rsc/?f=A2F500_DEV_KIT_BF).

5.23 Mixed Signal Header

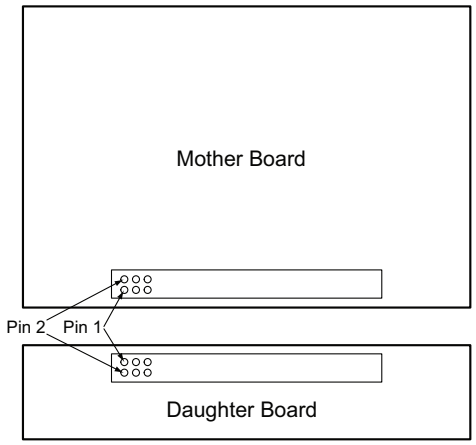
The mixed signal header can be obtained from Samtec, using the following part numbers:

- Mother board header 2X50 50 mil pitch: Samtec FTSH-150-04-L-D-RA (populated in the development board)
- Daughter board header 2X50 50 mil pitch: Samtec CLP-150-02-L-DH

The detailed instructions given below must be followed to ensure the correct orientation and insertion into the mother board.

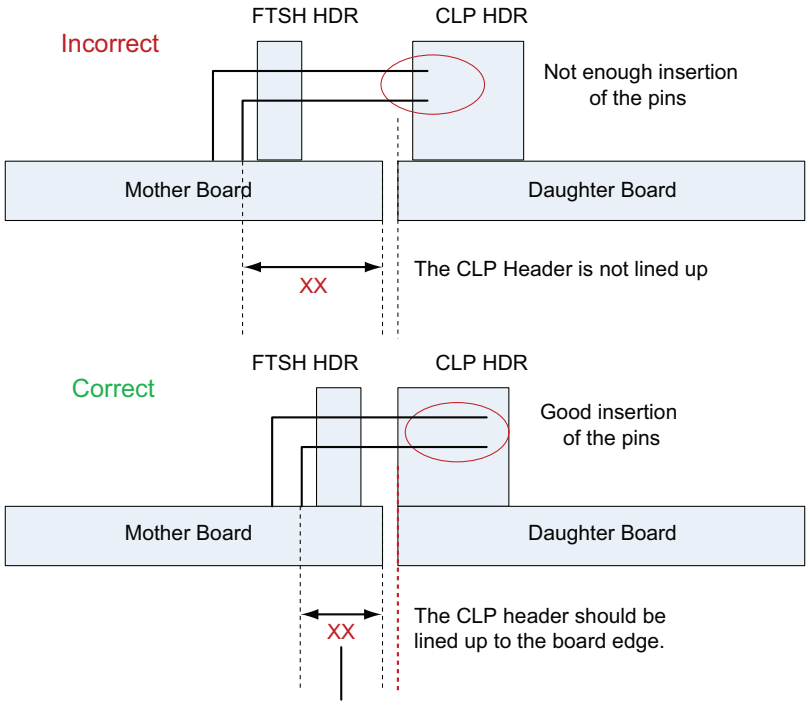
The following figure (top view) indicates the orientation of the mixed signal headers on the mother board and daughter board.

Figure 52 • **Top View of Mixed Signal Headers Correct Orientation**



Ensure that the header is placed such that a full insertion is possible between the two headers.

Figure 53 • **Correct Insertion of Daughter Board**



Note: XX is the critical length. Ensure that the connector is placed close enough so there is a good connection with the mating connector. This is applicable when designing the daughter board or the mother board.

When designing a daughter board to plug into an A2F500-DEV-KIT-2:

- Ensure the CLP header edge is lined up against the edge of the board.
- This will provide maximum insertion into the SmartFusion development and evaluation boards.

When designing a mother board for an existing daughter board (MPM DB, for example):

- Ensure that the length, denoted by XX, is kept less than 150 mils.
- Use the SmartFusion Development Kit PCB files: www.microsemi.com/soc/download/rsc/?f=A2F500_DEV_KIT_BF

5.23.1 Pinout Definition

The following table lists the pinout definition for the mixed signal header.

Table 36 • **Pinout Definition**

J21-Pin	Net Name	Pin Number	Description	J21-Pin	Net Name	Pin Number	Description
1	5V	Power	Power	2	5V	Power	Power
3	5V	Power	Power	4	5V	Power	Power
5	DGND	DGND	Digital ground	6	DGND	DGND	Digital ground
7	MSS_GP_IO_0	V1	MSS I/Os[1]	8	MSS_GP_IO_1	R3	MSS I/Os[1]
9	MSS_GP_IO_2	W1	MSS I/Os[1]	10	MSS_GP_IO_3	Y1	MSS I/Os[1]
11	MSS_GP_IO_4	AA1	MSS I/Os[1]	12	DGND	DGND	Digital ground
13	MSS_GP_IO_5	U2	MSS I/Os[1]	14	MSS_GP_IO_6	V2	MSS I/Os[1]
15	DGND	DGND	Digital ground	16	MSS_GP_IO_7	W2	MSS I/Os[1]
17	MSS_GP_IO_8	T3	MSS I/Os[1]	18	MSS_GP_IO_9	V3	MSS I/Os[1]
19	MSS_GP_IO_10	U3	MSS I/Os[1]	20	DGND	DGND	Digital ground
21	MSS_GP_IO_11	T4	MSS I/Os[1]	22	MSS_GP_IO_12	AA2	MSS I/Os[1]
23	DGND	DGND	Digital ground	24	MSS_GP_IO_13	AB2	MSS I/Os[1]
25	MSS_GP_IO_14	AB3	MSS I/Os[1]	26	MSS_GP_IO_15	Y3	MSS I/Os[1]
27	F2-200-IO_0	E3	FPGA I/Os[1]	28	DGND	DGND	Digital ground
29	F2-200-IO_1	F3	FPGA I/Os[1]	30	F2-200-IO_2	G4	FPGA I/Os[1]
31	DGND	DGND	Digital ground	32	F2-200-IO_3	H5	FPGA I/Os[1]
33	F2-200-IO_4	H6	FPGA I/Os[1]	34	F2-200-IO_5	J6	FPGA I/Os[1]
35	F2-200-IO_6	B22	FPGA I/Os[1]	36	DGND		Digital ground
37	F2-200-IO_7	C22	FPGA I/Os[1]	38	F2-200-IO_8	F1	FPGA I/Os[1]
39	PWM0	E22	Has External RC*[1]	40	PWM1	F22	Has External RC*[1]
41	DGND	DGND	Digital ground	42	DGND	DGND	Digital ground
43	AGND	AGND	Analog ground	44	AGND	AGND	Analog ground
45	DACOUT0	V7	SDD0[2]	46	DACOUT1	Y17	SDD1[2]
47	AGND	AGND	Analog ground	48	AGND	AGND	Analog ground
49	AC2	AB13	CM2[2]	50	AT2	AB12	TM2[2]
51	AGND	AGND	Analog ground	52	ATGND1		GNDTM1[2]
53	AC3	AA11	CM3[2]	54	AT3	Y12	TM3[2]
55	AGND	AGND	Analog ground	56	AGND		Analog ground
57	AC4	W13	CM4[2]	58	AT4	T13	TM4

Table 36 • **Pinout Definition *(continued)***

J21-Pin	Net Name	Pin Number	Description	J21-Pin	Net Name	Pin Number	Description
59	AGND	AGND	Analog ground	60	ATGND2		GNDTM2[2]
61	AV1_1	W9	ABPS2[2]	62	AV2_1	AB7	ABPS3[2]
63	AGND	AGND	Analog ground	64	AGND	AGND	Analog ground
65	AV1_3	W12	ABPS6[2]	66	AV2_3	Y11	ABPS7[2]
67	AGND	AGND	Analog ground	68	AGND	AGND	Analog ground
69	AV2_4	W14	ABPS9[2]	70	AV1_4	Y13	ABPS8[2]
71	AGND	AGND	Analog ground	72	AGND	AGND	Analog ground
73	ADC2	V9	ADC2[2]	74	ADC3	AB8	ADC3[2]
75	AGND	AGND	Analog ground	76	AGND	AGND	Analog ground
77	ADC4	U12	ADC4[2]	78	ADC5	V12	ADC5[2]
79	AGND	AGND	Analog ground	80	AGND	AGND	Analog ground
81	ADC6	V11	ADC6[2]	82	ADC7	T12	ADC7[2]
83	AGND	AGND	Analog ground	84	AGND	AGND	Analog ground
85	ADC8	V14	ADC8[2]	86	ADC9	AA14	ADC9[2]
87	AGND	AGND	Analog ground	88	AGND	AGND	Analog ground
89	ADC10	AA13	ADC10[2]	90	ADC11	U14	ADC11[2]
91	AC1	U9	CM1[2]	92	AGND	AGND	Analog ground
93	AGND	AGND	Analog ground	94	AGND	AGND	Analog ground
95	DGND	DGND	Digital ground	96	DGND	DGND	Digital ground
97	3.3V	Power	Power	98	3.3V	Power	Power
99	3.3V	Power	Power	100	3.3V	Power	Power

1. Digital signal
2. Analog signal

6 Pin List

The following table is the pin list applicable to the SmartFusion A2F500M3G-FGG484ES devices.

Table 37 • **Pin List**

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
A1	GND1	GND
A2	NC2	NC
A3	NC5	NC
A4	GND7	GND
A5	EMC_CS0_N/GAB0/IO05NDB0V0	F2_MCS_N_0
A6	EMC_CS1_N/GAB1/IO05PDB0V0	F2_MCS_N_1
A7	GND8	GND
A8	EMC_AB[0]/IO06NDB0V0	GND
A9	EMC_AB[1]/IO06PDB0V0	ADDRESS1
A10	GND2	GND
A11	NC1	NC
A12	EMC_AB[7]/IO12PDB0V0	ADDRESS7
A13	GND3	GND
A14	EMC_AB[12]/IO14NDB0V0	ADDRESS12
A15	EMC_AB[13]/IO14PDB0V0	ADDRESS13
A16	GND4	GND
A17	IO16NDB0V0	F2-500_N35
A18	IO16PDB0V0	F2-500_N36
A19	GND5	GND
A20	NC3	NC
A21	NC4	NC
A22	GND6	GND
B1	EMC_DB[15]/GAA2/IO88PDB5V0	DATA15
B2	GND12	GND
B3	NC41	NC
B4	NC42	NC
B5	VCCFPGAIOB0_3	V3P3_F2
B6	EMC_RW_N/GAA1/IO02PDB0V0	MRW_N
B7	IO04PPB0V0	F2-500_N12
B8	VCCFPGAIOB0_4	V3P3_F2
B9	EMC_BYTEN[0]/GAC0/IO07NDB0V0	MBYTEN_0

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
B10	EMC_AB[2]/IO09NDB0V0	ADDRESS2
B11	EMC_AB[3]/IO09PDB0V0	ADDRESS3
B12	EMC_AB[6]/IO12NDB0V0	ADDRESS6
B13	EMC_AB[14]/IO15NDB0V0	ADDRESS14
B14	EMC_AB[15]/IO15PDB0V0	ADDRESS15
B15	VCCFPGAIOB0_1	V3P3_F2
B16	EMC_AB[18]/IO18NDB0V0	ADDRESS18
B17	EMC_AB[19]/IO18PDB0V0	ADDRESS19
B18	VCCFPGAIOB0_2	V3P3_F2
B19	GBB0/IO24NDB0V0	LED1_N
B20	GBB1/IO24PDB0V0	LED2_N
B21	GND13	GND
B22	GBA2/IO27PDB1V0	F2-200-IO_6
C1	EMC_DB[14]/GAB2/IO88NDB5V0	DATA14
C2	NC9	NC
C3	NC11	NC
C4	IO01NDB0V0	F2-500_N3
C5	IO01PDB0V0	F2-500_N4
C6	EMC_CLK/GAA0/IO02NDB0V0	EM_CLK
C7	IO03PPB0V0	F2-500_N10
C8	IO04NPB0V0	F2-500_N11
C9	EMC_BYTEN[1]/GAC1/IO07PDB0V0	MBYTEN_1
C10	EMC_OEN1_N/IO08PDB0V0	MOE_N_1
C11	GND14	GND
C12	VCCFPGAIOB0_5	V3P3_F2
C13	EMC_AB[8]/IO13NDB0V0	ADDRESS8
C14	EMC_AB[16]/IO17NDB0V0	ADDRESS16
C15	EMC_AB[17]/IO17PDB0V0	ADDRESS17
C16	EMC_AB[24]/IO20NDB0V0	ADDRESS24
C17	EMC_AB[22]/IO19NDB0V0	ADDRESS22
C18	EMC_AB[23]/IO19PDB0V0	ADDRESS23
C19	GBA0/IO23NPB0V0	LED3_N
C20	NC10	NC
C21	GBC2/IO30PDB1V0	DIP2
C22	GBB2/IO27NDB1V0	F2-200-IO_7
D1	GND15	GND

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
D2	EMC_DB[12]/IO87NDB5V0	DATA12
D3	EMC_DB[13]/GAC2/IO87PDB5V0	DATA13
D4	NC14	NC
D5	NC15	NC
D6	GND19	GND
D7	IO00NPB0V0	F2-500_N1
D8	IO03NPB0V0	F2-500_N9
D9	GND20	GND
D10	EMC_OEN0_N/IO08NDB0V0	MOE_N_0
D11	EMC_AB[10]/IO11NDB0V0	ADDRESS10
D12	EMC_AB[11]/IO11PDB0V0	ADDRESS11
D13	EMC_AB[9]/IO13PDB0V0	ADDRESS9
D14	GND16	GND
D15	GBC1/IO22PPB0V0	OLED_D/C#
D16	EMC_AB[25]/IO20PDB0V0	ADDRESS25
D17	GND17	GND
D18	GBA1/IO23PPB0V0	PDI3/SPI_DO
D19	NC12	NC
D20	NC13	NC
D21	IO30NDB1V0	DIP3
D22	GND18	GND
E1	GFC2/IO84PPB5V0	SWITCH4
E2	VCCFPGAIOB5_1	V3P3_F2
E3	GFA2/IO85PDB5V0	F2-200-IO_0
E4	GND22	GND
E5	NC18	NC
E6	GNDQ1	GND
E7	VCCFPGAIOB0_12	V3P3_F2
E8	IO00PPB0V0	F2-500_N2
E9	NC19	NC
E10	VCCFPGAIOB0_6	V3P3_F2
E11	EMC_AB[4]/IO10NDB0V0	ADDRESS4
E12	EMC_AB[5]/IO10PDB0V0	ADDRESS5
E13	VCCFPGAIOB0_13	V3P3_F2
E14	GBC0/IO22NPB0V0	SWITCH5
E15	NC16	NC

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
E16	VCCFPGAIOB0_7	V3P3_F2
E17	VCOMPLA1	GND
E18	IO25NPB1V0	F2-500_E35
E19	GND21	GND
E20	NC17	NC
E21	VCCFPGAIOB1_1	V3P3_F2
E22	IO32NDB1V0	F2-200-PWM0
F1	GFB1/IO82PPB5V0	F2-200-IO_8
F2	IO84NPB5V0	RMII_50MHZ_CLK
F3	GFB2/IO85NDB5V0	F2-200-IO_1
F4	EMC_DB[10]/IO86NPB5V0	DATA10
F5	VCCFPGAIOB5_2	V3P3_F2
F6	VCCPLL0	VCCPLA
F7	VCOMPLA0	GND
F8	NC23	NC
F9	NC24	NC
F10	NC20	NC
F11	NC21	NC
F12	NC22	NC
F13	EMC_AB[20]/IO21NDB0V0	ADDRESS20
F14	EMC_AB[21]/IO21PDB0V0	ADDRESS21
F15	GNDQ2	GND
F16	VCCPL1	VCCPLB
F17	IO25PPB1V0	F2-500_E36
F18	VCCFPGAIOB1_2	V3P3_F2
F19	IO28NDB1V0	DIP4
F20	IO31PDB1V0	F2-500_E24
F21	IO31NDB1V0	F2-500_E23
F22	IO32PDB1V0	F2-200-PWM1
G1	GND23	GND
G2	GFB0/IO82NPB5V0	PDI0/SPI_CLK
G3	EMC_DB[9]/GEC1/IO80PDB5V0	DATA9
G4	GFC1/IO83PPB5V0	F2-200-IO_2
G5	EMC_DB[11]/IO86PPB5V0	DATA11
G6	GNDQ4	GND
G7	NC25	NC

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
G8	GND28	GND
G9	VCCFPGAIOB0_11	V3P3_F2
G10	GND24	GND
G11	VCCFPGAIOB0_8	V3P3_F2
G12	GND25	GND
G13	VCCFPGAIOB0_9	V3P3_F2
G14	GND26	GND
G15	VCCFPGAIOB0_10	V3P3_F2
G16	GNDQ3	GND
G17	IO26PDB1V0	F2-500_E34
G18	IO26NDB1V0	F2-500_E33
G19	GCA2/IO28PDB1V0	SWITCH1
G20	IO33NDB1V0	SWITCH2
G21	GCB2/IO33PDB1V0	SWITCH3
G22	GND27	GND
H1	EMC_DB[7]/GEB1/IO79PDB5V0	DATA7
H2	VCCFPGAIOB5_3	V3P3_F2
H3	EMC_DB[8]/GEC0/IO80NDB5V0	DATA8
H4	GND33	GND
H5	GFC0/IO83NPB5V0	F2-200-IO_3
H6	GFA1/IO81PDB5V0	F2-200-IO_4
H7	GND34	GND
H8	VCC4	V1P5_DUT
H9	GND35	GND
H10	VCC1	V1P5_DUT
H11	GND29	GND
H12	VCC2	V1P5_DUT
H13	GND30	GND
H14	VCC3	V1P5_DUT
H15	GND31	GND
H16	VCCFPGAIOB1_3	V3P3_F2
H17	IO29NDB1V0	LED4_N
H18	GCC2/IO29PDB1V0	PDI4/SPI_IRQ
H19	GND32	GND
H20	GCC0/IO35NPB1V0	DIP1
H21	VCCFPGAIOB1_4	V3P3_F2

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
H22	GCB0/IO34NDB1V0	CLK_50MHZ
J1	EMC_DB[6]/GEB0/IO79NDB5V0	DATA6
J2	EMC_DB[5]/GEA1/IO78PDB5V0	DATA5
J3	EMC_DB[4]/GEA0/IO78NDB5V0	DATA4
J4	EMC_DB[3]/GEC2/IO77PPB5V0	DATA3
J5	VCCFPGAIOB5_4	V3P3_F2
J6	GFA0/IO81NDB5V0	F2-200-IO_5
J7	VCCFPGAIOB5_5	V3P3_F2
J8	GND40	GND
J9	VCC8	V1P5_DUT
J10	GND36	GND
J11	VCC5	V1P5_DUT
J12	GND37	GND
J13	VCC6	V1P5_DUT
J14	GND38	GND
J15	VCC7	V1P5_DUT
J16	GND39	GND
J17	IO37PDB1V0	F2-500_E12
J18	VCCFPGAIOB1_5	V3P3_F2
J19	GCA0/IO36NDB1V0	DIRECTC_TCK
J20	GCA1/IO36PDB1V0	DIRECTC_TDO
J21	GCC1/IO35PPB1V0	DIRECTC_TMS
J22	GCB1/IO34PDB1V0	DIRECTC_TRST
K1	GND41	GND
K2	EMC_DB[0]/GEA2/IO76NDB5V0	DATA0
K3	EMC_DB[1]/GEB2/IO76PDB5V0	DATA1
K4	IO74PPB5V0	LVDS_RX_P1C
K5	EMC_DB[2]/IO77NPB5V0	DATA2
K6	IO75PDB5V0	F2-500_W16
K7	GND46	GND
K8	VCC12	V1P5_DUT
K9	GND47	GND
K10	VCC9	V1P5_DUT
K11	GND42	GND
K12	VCC10	V1P5_DUT
K13	GND43	GND

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
K14	VCC11	V1P5_DUT
K15	GND44	GND
K16	VCCFPGAIOB1_6	V3P3_F2
K17	IO37NDB1V0	F2-500_E11
K18	GDA1/IO40PDB1V0	PDI6/EEPROM_Loaded
K19	GDA0/IO40NDB1V0	DIRECTC_TDI
K20	GDC1/IO38PDB1V0	PDI1/SPI_SEL
K21	GDC0/IO38NDB1V0	PDI2/SPI_DI
K22	GND45	GND
L1	IO73PDB5V0	LVDS_RX_P0C
L2	IO73NDB5V0	LVDS_RX_N0C
L3	IO72PPB5V0	LVDS_TX_P4
L4	GND52	GND
L5	IO74NPB5V0	LVDS_RX_N1C
L6	IO75NDB5V0	F2-500_W15
L7	VCCFPGAIOB5_6	V3P3_F2
L8	GND53	GND
L9	VCC16	V1P5_DUT
L10	GND48	GND
L11	VCC13	V1P5_DUT
L12	GND49	GND
L13	VCC14	V1P5_DUT
L14	GND50	GND
L15	VCC15	V1P5_DUT
L16	GND51	GND
L17	GNDQ5	GND
L18	GDA2/IO42NDB1V0	RS485_RE
L19	VCCFPGAIOB1_7	V3P3_F2
L20	GDB1/IO39PDB1V0	RS485_DE
L21	GDB0/IO39NDB1V0	CAN_RXD_0
L22	GDC2/IO41PDB1V0	CAN_RXD_1
M1	IO71PDB5V0	LVDS_TX_P3
M2	IO71NDB5V0	LVDS_TX_N3
M3	VCCFPGAIOB5_7	V3P3_F2
M4	IO72NPB5V0	LVDS_TX_N4
M5	GNDQ6	GND

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
M6	IO68PDB5V0	LVDS_TX_P0
M7	GND58	GND
M8	VCC20	V1P5_DUT
M9	GND59	GND
M10	VCC17	V1P5_DUT
M11	GND54	GND
M12	VCC18	V1P5_DUT
M13	GND55	GND
M14	VCC19	V1P5_DUT
M15	GND56	GND
M16	VCCFPGAIOB1_8	V3P3_F2
M17	NC26	NC
M18	GDB2/IO42PDB1V0	CAN_TXD_1
M19	VJTAG	VJTAG
M20	GND57	GND
M21	VPP	VPUMP
M22	IO41NDB1V0	CAN_TXD_0
N1	GND60	GND
N2	IO70PDB5V0	LVDS_TX_P2
N3	IO70NDB5V0	LVDS_TX_N2
N4	VCC_RCOSC	VCC_OSC
N5	VCCFPGAIOB5_8	V3P3_F2
N6	IO68NDB5V0	LVDS_TX_N0
N7	VCCFPGAIOB5_9	V3P3_F2
N8	GND65	GND
N9	VCC24	V1P5_DUT
N10	GND61	GND
N11	VCC21	V1P5_DUT
N12	GND62	GND
N13	VCC22	V1P5_DUT
N14	GND63	GND
N15	VCC23	V1P5_DUT
N16	GND87	GND
N17	NC27	NC
N18	VCCFPGAIOB1_9	V3P3_F2
N19	VCCENVM	V1P5_DUT

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
N20	GNDENVM	GND
N21	NC28	NC
N22	GND64	GND
P1	IO69NDB5V0	LVDS_TX_N1
P2	IO69PDB5V0	LVDS_TX_P1
P3	GNDRCOSC	GND
P4	GND70	GND
P5	NC29	NC
P6	NC30	NC
P7	GND71	GND
P8	VCC28	V1P5_DUT
P9	GND72	GND
P10	VCC25	V1P5_DUT
P11	GND66	GND
P12	VCC26	V1P5_DUT
P13	GND67	GND
P14	VCC27	V1P5_DUT
P15	GND68	GND
P16	VCCFPGAIOB1_10	V3P3_F2
P17	TDI	TDI
P18	TCK	F2_TCK
P19	GND69	GND
P20	TMS	F2_TMS
P21	TDO	F2_TDO
P22	TRSTB	TRST
R1	MSS_RESET_N	MSS_SYSRESETB
R2	VCCFPGAIOB5_10	V3P3_F2
R3	GPIO_1/IO55RSB4V0	MSS_GP_IO_1
R4	NC35	NC
R5	NC36	NC
R6	NC37	NC
R7	NC38	NC
R8	GND76	GND
R9	VCC32	V1P5_DUT
R10	GND73	GND
R11	VCC29	V1P5_DUT

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
R12	GND74	GND
R13	VCC30	V1P5_DUT
R14	GND75	GND
R15	VCC31	V1P5_DUT
R16	JTAGSEL	JTAGSEL
R17	NC31	NC
R18	NC32	NC
R19	NC33	NC
R20	NC45	NC
R21	VCCFPGAIOB1_11	V3P3_F2
R22	NC34	NC
T1	GND77	GND
T2	VCCMSSIOB4_1	V3P3_F2
T3	GPIO_8/IO48RSB4V0	MSS_GP_IO_8
T4	GPIO_11/IO66RSB4V0	MSS_GP_IO_11
T5	GND80	GND
T6	MAC_CLK	MSS_RMII_CLK
T7	VCCMSSIOB4_2	V3P3_F2
T8	VCC33SDD0	V3P3A
T9	VCC15A	V1P5A
T10	GNDAQ0	AGND
T11	GND33ADC01	AGND
T12	ADC7	ADC7
T13	TM4	AT4
T14	VAREF2	VAREF2
T15	VAREFOUT	VAREF_OUT
T16	VCCMSSIOB2_1	V3P3_F2
T17	SPI_1_DO/GPIO_24	SDO_1_OUT
T18	GND78	GND
T19	NC43	NC
T20	NC44	NC
T21	VCCMSSIOB2_2	V3P3_F2
T22	GND79	GND
U1	GND81	GND
U2	GPIO_5/IO51RSB4V0	MSS_GP_IO_5
U3	GPIO_10/IO67RSB4V0	MSS_GP_IO_10

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
U4	VCCMSSIOB4_3	V3P3_F2
U5	MAC_RXD[1]/IO62RSB4V0	FPGA_ENA_RXD1
U6	NC39	NC
U7	VCC33AP	V3P3A
U8	VCC33N	AGND
U9	CM1	AC1
U10	VAREF0	VAREF_0
U11	GND33ADC11	AGND
U12	ADC4	ADC4
U13	GNDTM2	ATGND2
U14	ADC11	ADC11
U15	GNDVAREF	AGND
U16	VCC33SDD1	V3P3A
U17	SPI_0_DO/GPIO_16	SDO_0_OUT
U18	UART_0_RXD/GPIO_21	RXD_0_IN
U19	VCCMSSIOB2_3	V3P3_F2
U20	I2C_1_SCL/GPIO_31	I2C_SCL_1_IN
U21	I2C_0_SCL/GPIO_23	I2C_SCL_0_IN
U22	GND82	GND
V1	GPIO_0/IO56RSB4V0	MSS_GP_IO_0
V2	GPIO_6/IO50RSB4V0	MSS_GP_IO_6
V3	GPIO_9/IO47RSB4V0	MSS_GP_IO_9
V4	MAC_MDIO/IO58RSB4V0	FPGA_ENA_MDIO
V5	MAC_RXD[0]/IO63RSB4V0	FPGA_ENA_RXD0
V6	GND84	GND
V7	SDD0	DACOUT0
V8	ABPS1	AV2_0
V9	ADC2	ADC2
V10	VCC33ADC0	V3P3A
V11	ADC6	ADC6
V12	ADC5	ADC5
V13	ABPS5	AV2_2
V14	ADC8	ADC8
V15	GND33_ADC2_1	AGND
V16	NC40	NC
V17	GND83	GND

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
V18	SPI_0_DI/GPIO_17	SDI_0_IN
V19	SPI_1_DI/GPIO_25	SDI_1_IN
V20	UART_1_TXD/GPIO_28	TXD_1_OUT
V21	I2C_0_SDA/GPIO_22	I2C_SDA_0_IN
V22	I2C_1_SDA/GPIO_30	I2C_SDA_1_IN
W1	GPIO_2/IO54RSB4V0	MSS_GP_IO_2
W2	GPIO_7/IO49RSB4V0	MSS_GP_IO_7
W3	GND86	GND
W4	MAC_CRSDV/IO60RSB4V0	FPGA_ENA_CRS
W5	MAC_TXD[1]/IO64RSB4V0	FPGA_ENA_TXD1
W6	SDD2	SDD2
W7	GNDA0	AGND
W8	TM0	AT0
W9	ABPS2	AV1_1
W10	GND33ADC02	AGND
W11	VCC15ADC1	V1P5A
W12	ABPS6	AV1_3
W13	CM4	AC4
W14	ABPS9	AV2_4
W15	VDD33_ADC_2	V3P3A
W16	GNDA1	AGND
W17	PU_N	RTC_SW
W18	GNDSDD1	AGND
W19	SPI_0_CLK/GPIO_18	SCLK_0_OUT
W20	GND85	GND
W21	SPI_1_SS/GPIO_27	SS_1_OUT
W22	UART_1_RXD/GPIO_29	RXD_1_IN
Y1	GPIO_3/IO53RSB4V0	MSS_GP_IO_3
Y2	VCCMSSIOB4_4	V3P3_F2
Y3	GPIO_15/IO43RSB4V0	MSS_GP_IO_15
Y4	MAC_TXEN/IO61RSB4V0	FPGA_ENA_TXEN
Y5	VCCMSSIOB4_5	V3P3_F2
Y6	GNDSDD0	AGND
Y7	CM0	AC0
Y8	GNDTM0	ATGND0
Y9	ADC0	ADC0

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
Y10	VCC15ADC0	V1P5A
Y11	ABPS7	AV2_3
Y12	TM3	AT3
Y13	ABPS8	AV1_4
Y14	GND33_ADC_2	AGND
Y15	VDD15_ADC_2	V1P5A
Y16	VCCMAINXTAL	V3P3A
Y17	SDD1	DACOUT1
Y18	PTEM	V1P5_INT
Y19	VCC33A	V3P3A
Y20	SPI_0_SS/GPIO_19	SS_0_OUT
Y21	VCCMSSIOB2_4	V3P3_F2
Y22	UART_0_TXD/GPIO_20	TXD_0_OUT
AA1	GPIO_4/IO52RSB4V0	MSS_GP_IO_4
AA2	GPIO_12/IO46RSB4V0	MSS_GP_IO_12
AA3	MAC_MDC/IO57RSB4V0	FPGA_ENA_MDC
AA4	MAC_RXER/IO59RSB4V0	FPGA_ENA_RXER
AA5	MAC_TXD[0]/IO65RSB4V0	FPGA_ENA_TXD0
AA6	ABPS0	AV1_0
AA7	TM1	AT1
AA8	ADC1	ADC1
AA9	GND15ADC1	AGND
AA10	GND33ADC10	AGND
AA11	CM3	AC3
AA12	GNDTM1	ATGND1
AA13	ADC10	ADC10
AA14	ADC9	ADC9
AA15	GND15_ADC2	AGND
AA16	MAINXIN	N16866974
AA17	MAINXOUT	N16866972
AA18	LPXIN	N16866585
AA19	LPXOUT	N16866595
AA20	NC6	NC
AA21	NC7	NC
AA22	SPI_1_CLK/GPIO_26	SCLK_1_OUT
AB1	GND9	GND

Table 37 • **Pin List *(continued)***

A2F500 Pin Number	A2F500 Pin Name	Board Signal Name
AB2	GPIO_13/IO45RSB4V0	MSS_GP_IO_13
AB3	GPIO_14/IO44RSB4V0	MSS_GP_IO_14
AB4	GND11	GND
AB5	PCAP	N16866617
AB6	NCAP	N16866619
AB7	ABPS3	AV2_1
AB8	ADC3	ADC3
AB9	GND15ADC0	AGND
AB10	VCC33ADC1	V3P3A
AB11	VAREF1	VAREF_1
AB12	TM2	AT2
AB13	CM2	AC2
AB14	ABPS4	AV1_2
AB15	GNDAQ1	AGND
AB16	GNDMAINXTAL	AGND
AB17	GNDLPXTAL	AGND
AB18	VCCLPXTAL	V3P3A
AB19	VDDBAT	VBAT
AB20	PTBASE	PTBASE
AB21	NC8	NC
AB22	GND10	GND

7 Board Stackup

7.1 A2F500-DEV-KIT-2 Board Stack-Up

The SmartFusion Development Kit board is built on a 14-layer printed circuit board (PCB). The silkscreen is provided in Figure 55, page 68. The full PCB design layout is provided on the SmartFusion Development Kit web page:
www.microsemi.com/soc/products/hardware/devkits_boards/smartfusion_dev.aspx.

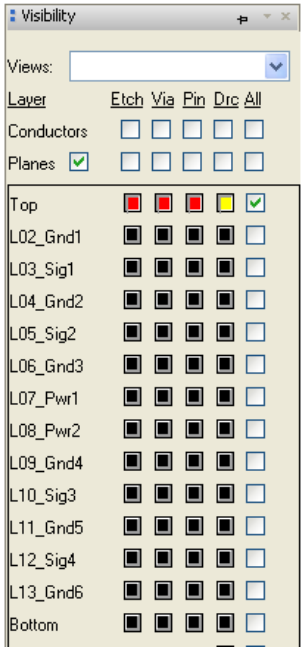
To view the PCB design layout files, you can use Allegro Free Physical Viewer, which can be downloaded from the Cadence website Allegro download page:
www.cadence.com/products/pcb/Pages/Downloads.aspx.

The layers are arranged in the following order:

- Layer 1: Top signal
- Layer 2: GND1
- Layer 3: Signal1
- Layer 4: GND2
- Layer 5: Signal2
- Layer 6: GND3
- Layer 7: PWR 1
- Layer 8: PWR 2
- Layer 9: GND4
- Layer 10: Signal 3
- Layer 11: GND 5
- Layer 12: Signal 4
- Layer 13: GND 6
- Layer 14: Bottom signal

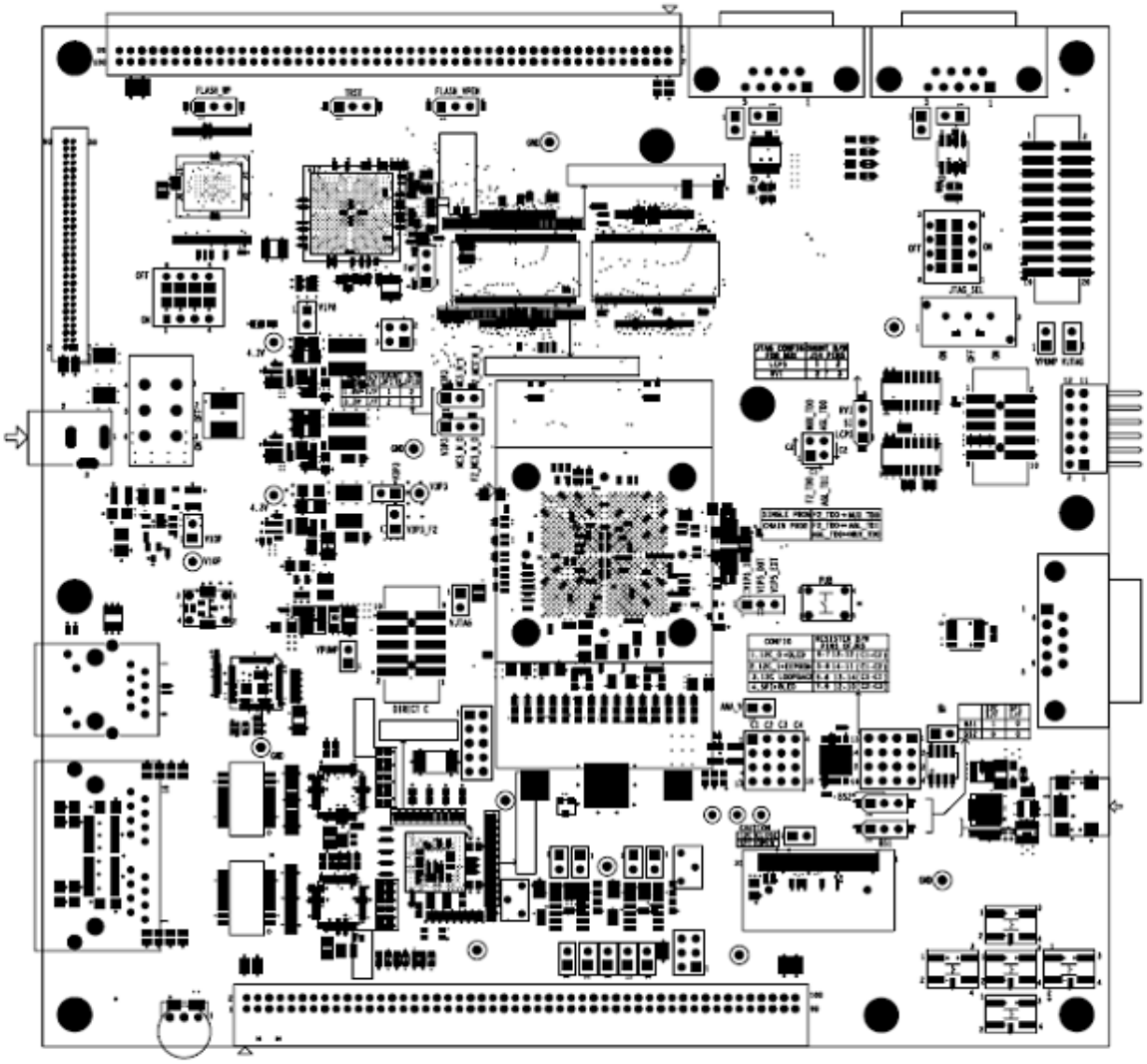
The following figure shows the stack-up:

Figure 54 • **PCB Layer Stackup**



The following figure shows the silkscreen top view.

Figure 55 • **Board Silkscreen Top View**



8 Manufacturing Test

8.1 A2F500-DEV-KIT-2 Board Testing Procedures

This chapter defines and describes the specific A2F500-DEV-KIT-2 board testing procedures. Instructions for running the Microsemi A2F500-DEV-KIT-2 board tests are detailed. The steps needed to set up the test environment are also outlined. Associated files for this procedure can be downloaded from the Microsemi website at http://soc.microsemi.com/soc/download/rsc/?f=A2F500-DEV-KIT_Mfg_PF.

8.2 Jumper Settings for the Board Test

The following table lists all the jumpers that need to be set on the board for performing the tests. In case any of the tests in the following section do not work as expected, double-check.

Table 38 • **Manufacturing Test Jumper Settings**

Jumper	Pin From	Pin To
JP1	1	2
JP2	1	2
JP4	1	3
	7	9
JP5	1	2
	3	4
JP6	2	3
J7	2	3
	6	7
	10	11
	14	15
JP7	1	2
JP8	3	4
	7	8
	11	12
	15	16
JP11	1	2
JP12	1	2
JP13	1	2
JP14	1	2
JP15	1	2
JP16	2	3
JP17	2	3
JP18	1	2
JP19	2	3

Table 38 • **Manufacturing Test Jumper Settings *(continued)***

Jumper	Pin From	Pin To
JP20	1	2
JP21	1	2
JP22	2	3
JP23	1	2
JP24	1	2
JP27	1	2
JP28	1	2
J32	1	2
	3	4
	5	6

8.3 Installing the A2F500-DEV-KIT-2 Board USB Serial Driver

1. Use WinZip to extract all files stored in the CP210x_Drivers.zip archive.
2. Double-click CP210x_Drivers.exe.
3. Choose the Install option in the Install Wizard and select Yes for the licensing agreement.
4. Restart the computer on which the driver was installed. After restart, the driver can be used to communicate with A2F500-DEV-KIT-2 board.

8.4 Hooking up the Board and Programming Stick

Connect the Microsemi A2F500-DEV-KIT-2 board to the Microsemi programming stick. Connect the J15 pins on the board to the programmer, as shown in Figure 61, page 73.

Connect one end of USB mini B cables to the USB connections on the A2F500-DEV-KIT-2 board and the Microsemi programming stick. These connections are labeled in Figure 61, page 73. Connect the USB cables to the PC you will use for testing.

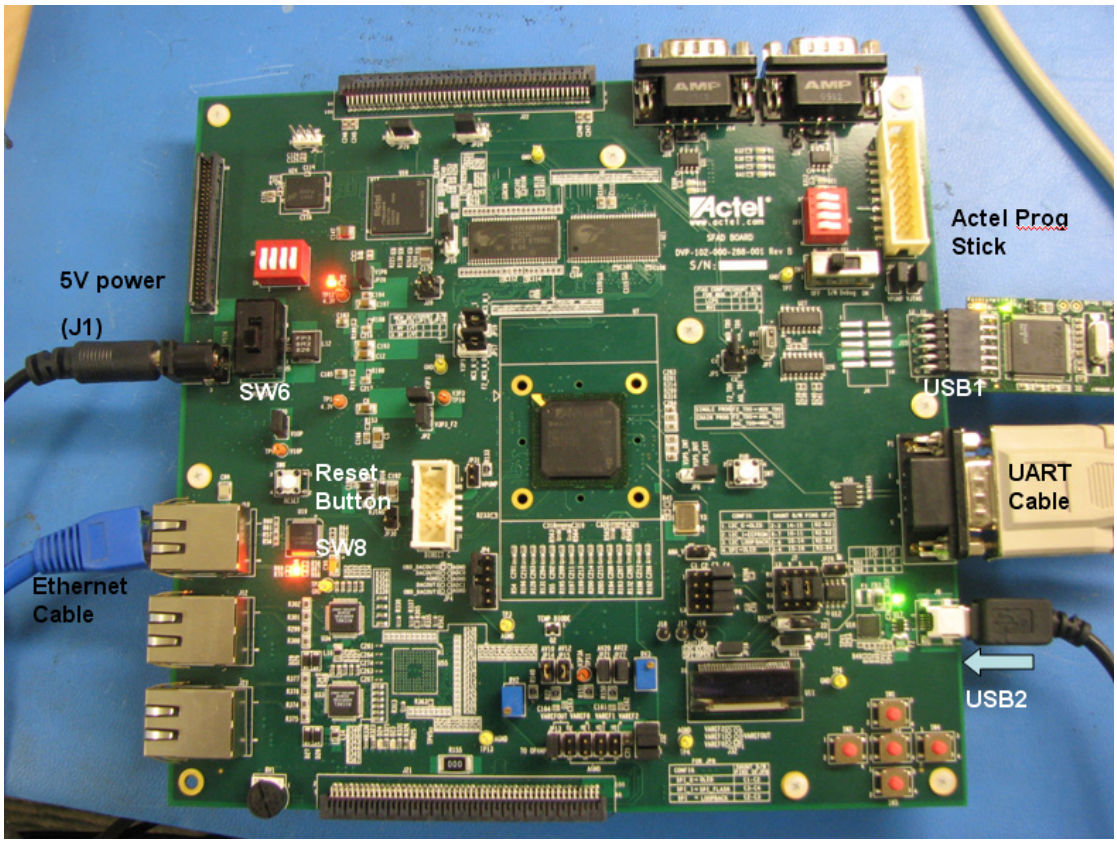
Connect one end of 5 V power supply to power input J1, on the A2F500-DEV-KIT-2 board (Figure 6-1 on page 81). Flip on the power switch SW6 on the board. LEDs labeled D5, D6, and D8 should light up. The LED labeled as ON in the programming stick should also be lighted.

8.4.1 Hooking Up the Board and Ethernet Cable

Connect an Ethernet cable from the local area network to J10, the A2F500-DEV-KIT-2 Ethernet jack.

Note: For the board Ethernet test to pass, the local network must be running a DHCP server that assigns an IP address to the web server on the board. Network firewalls must not block the board web server.

Figure 56 • **Board Manufacturing Test Setup**



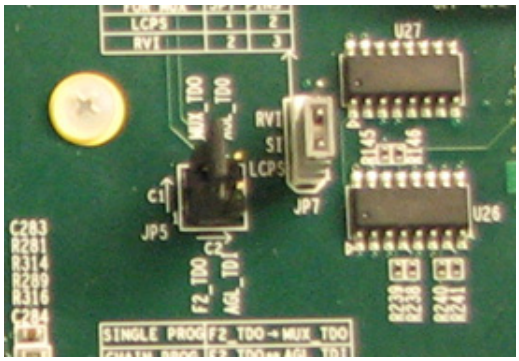
8.4.2 Hooking up the A2F500-DEV-KIT-2 Board and UART Cable

Connect a D9 UART cable from the PC (COM port 1) to the P1 UART connector on the board. Note: This cable is needed for the RS485 test.

8.5 Programming the A2F500-DEV-KIT-2 Board (SmartFusion cSoC Device)

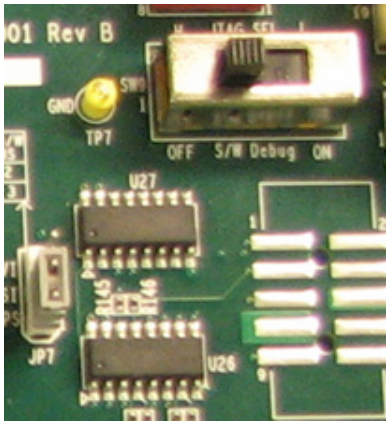
1. Ensure that Jumper JP5 is in 1-3 position and JP7 is in the 1-2 position, as shown in the following figure.

Figure 57 • **JTAG Chain Settings for A2F500 Programming**



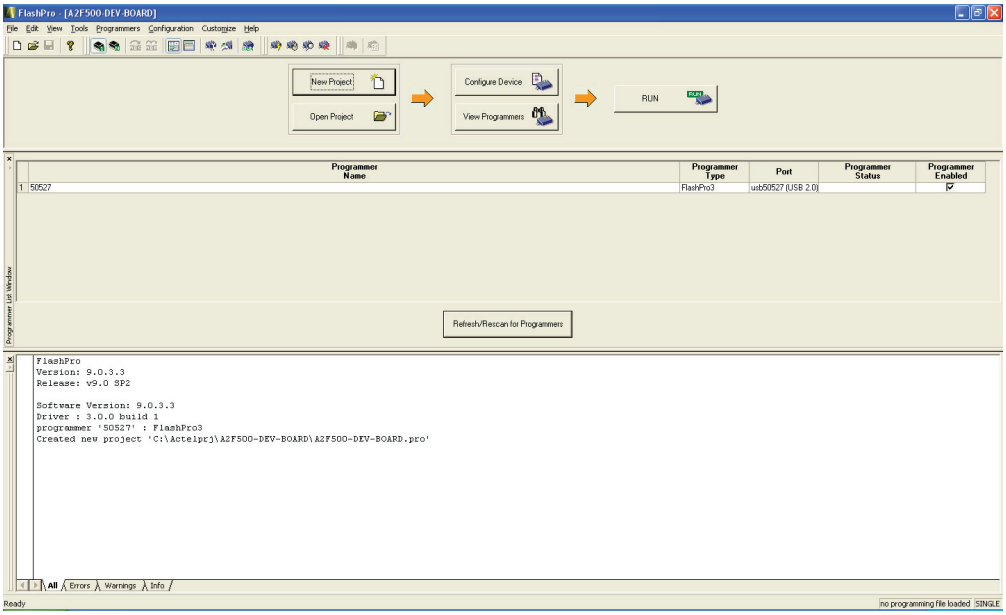
2. Set switch SW9 to the OFF position, as shown in the following figure.

Figure 58 • **JTAG SEL Setting for Programming**



3. Open the FlashPro programming software.

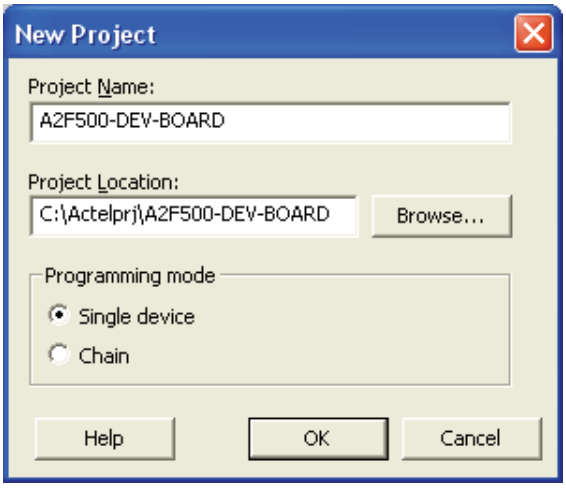
Figure 59 • **FlashPro New Project**



4. Create a new programming project.

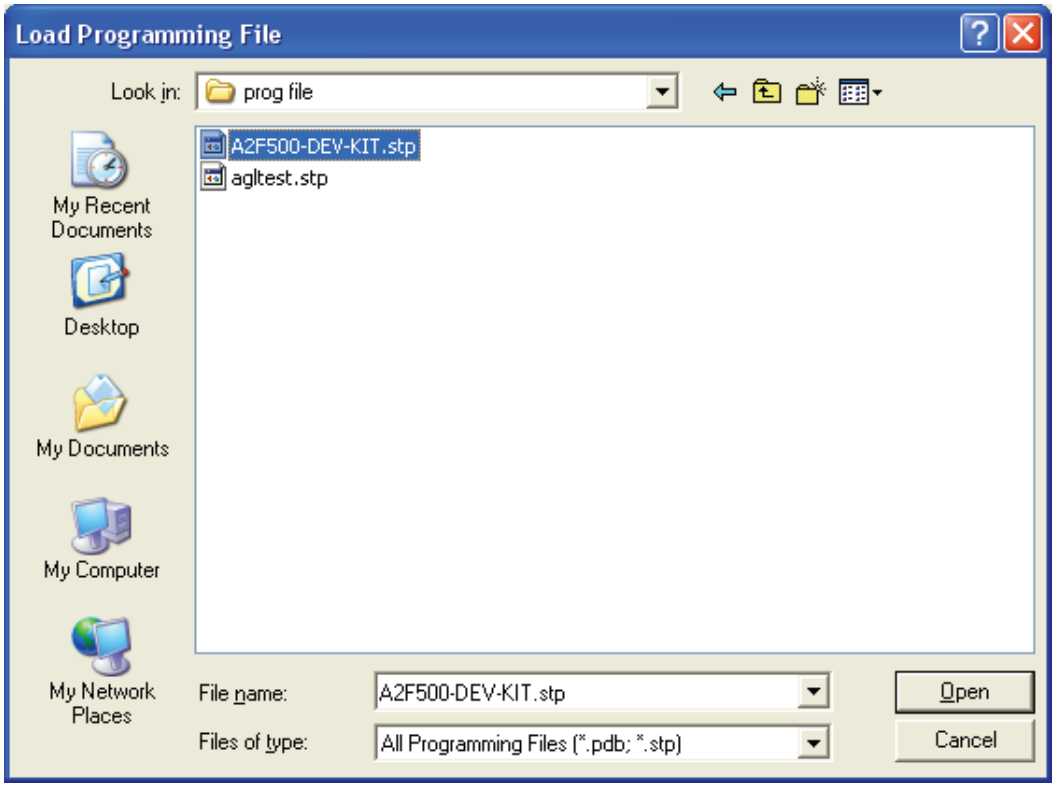
5. Select the option **Single device** when choosing the programming mode.

Figure 60 • **New Project Setup**



6. Click the **Configure Device** button. This opens the existing programming file button.
7. Browse the PC file system to find the A2F500-DEV-KIT.stp programming file. Click **Open** to select the A2F500-DEV-KIT.stp file.
8. Click the **Program** button to program the A2F500-DEV-KIT board.

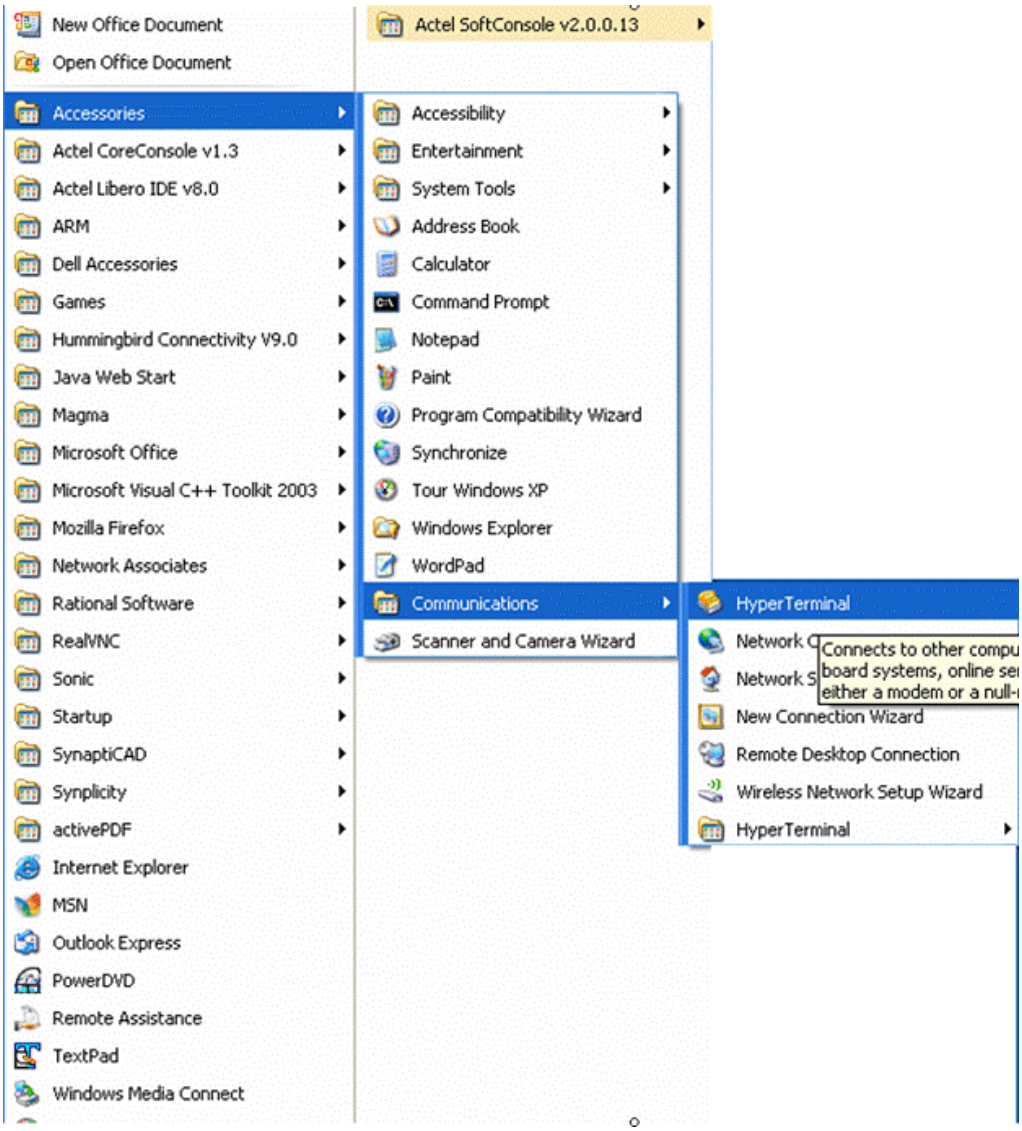
Figure 61 • **Manufacturing Test STAPL File Setup**



8.6 Setting Up the Test Terminal

1. Open the Windows start menu. Select **All** > **Programs** > **Accessories** > **Communications** and select the HyperTerminal program (Figure 62, page 74). This opens HyperTerminal. If your computer does not have the HyperTerminal program, use any free serial terminal emulation program such as PuTTY or Tera Term. Refer to the *Configuring Serial Terminal Emulation Programs* Tutorial for configuring HyperTerminal, Tera Term, and PuTTY.

Figure 62 • **HyperTerminal Program Setup**

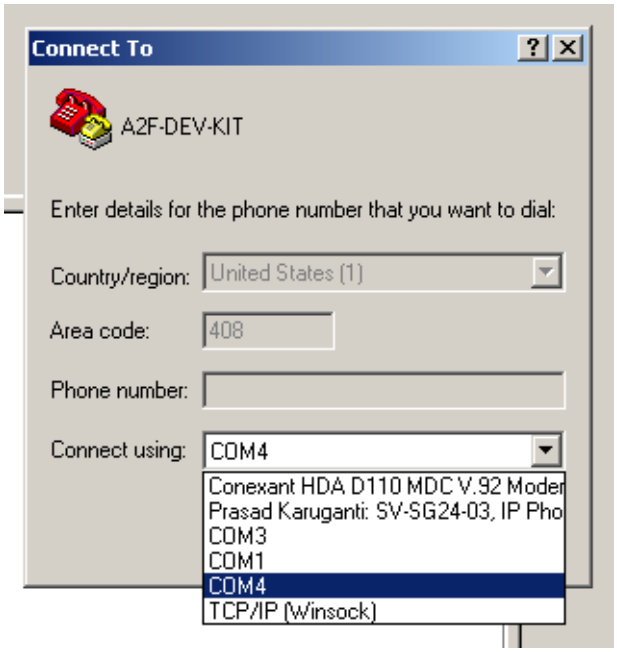


2. The Connection Description window is displayed. Type in **A2F500-DEV-KIT** as the name of the new HyperTerminal session and click **OK**.

Figure 63 • **HyperTerminal Connection Description**

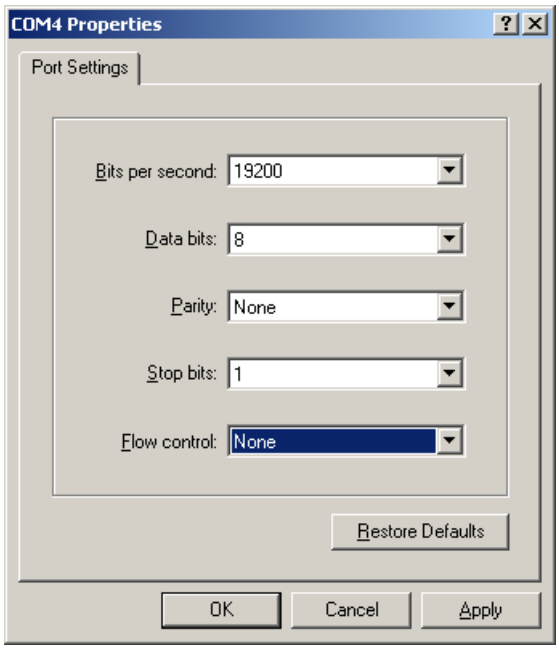
3. The Connect To window is displayed. Select the COM port for which A2F500-DEV-KIT is connected.

Figure 64 • **HyperTerminal Port Selection**



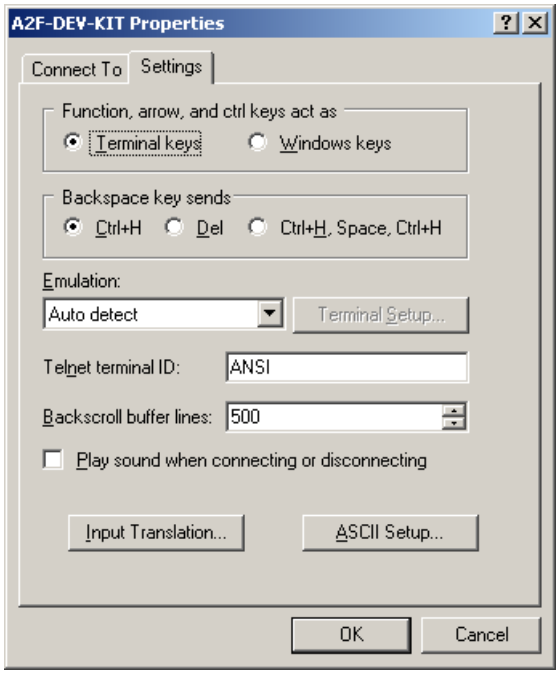
4. The COM4 Properties window is displayed. Select the following settings:
   Bits per second = 19200
   Data bits = 8
   Parity = None
   Stop bits = 1
   Flow Control = None

Figure 65 • **HyperTerminal Port Settings**



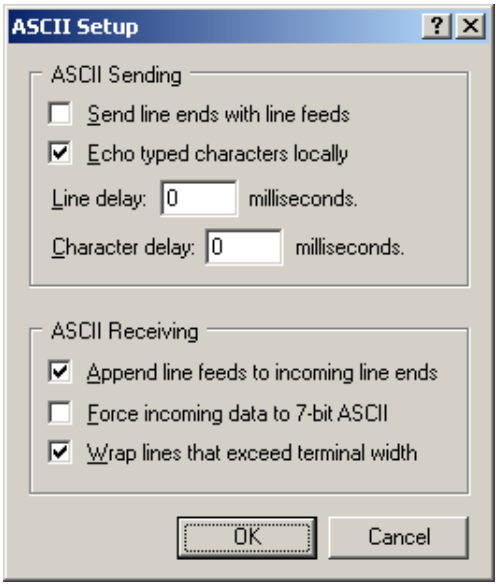
5. Select **File** > **Properties** in the HyperTerminal window. Choose the **Settings** tab.

Figure 66 • **HyperTerminal Properties**



6. Click the **ASCII Setup** button. Select the check box labeled *Append line feeds to incoming line ends*.

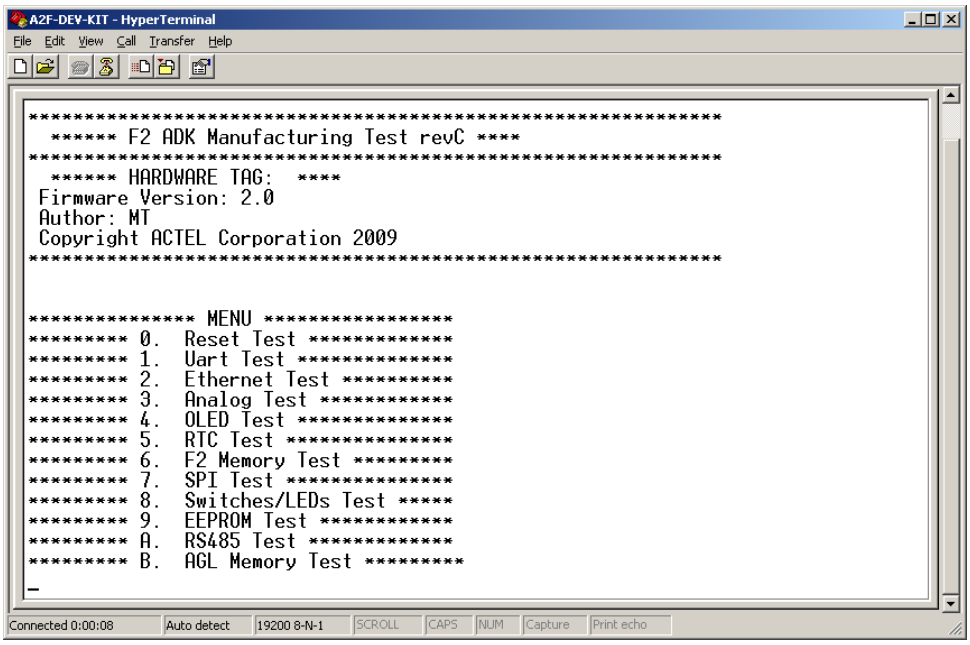
Figure 67 • **ASCII Character Settings**



8.7 Running the A2F500-DEV-KIT-2 Board Test

Press the button labeled **SW8** on the A2F500-DEV-KIT board to start the test program. The menu shown in the following figure is displayed on the terminal.

Figure 68 • **Manufacturing Test Menu**



Note: If this message does not appear, then try pressing button SW8 again. If the above message still does not appear, then refer to the Setting Up the Test Terminal, page 74 and check to see that the terminal has been set up correctly.

8.7.1 Reset Test

1. Enter 0 into the terminal to begin the reset test. The result should be similar to what is shown in the following figure.

Figure 69 • **Reset Test**

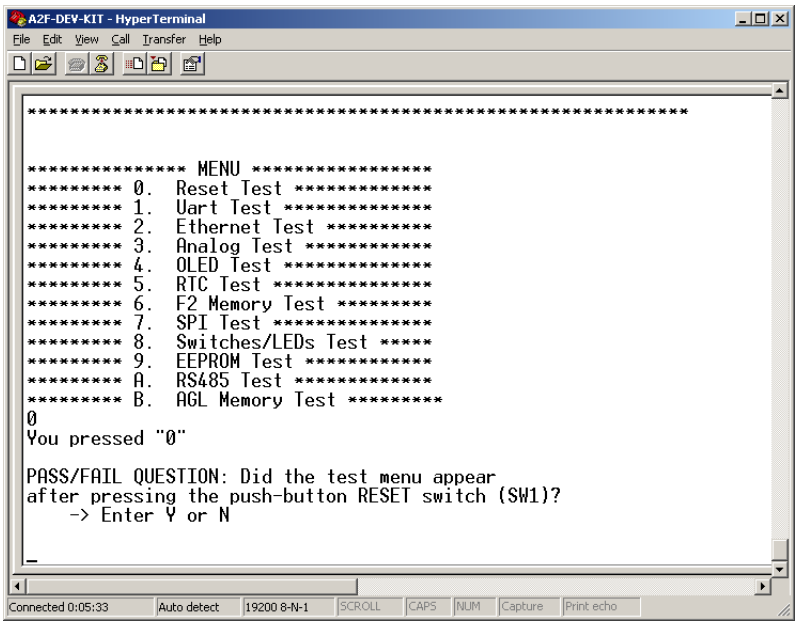
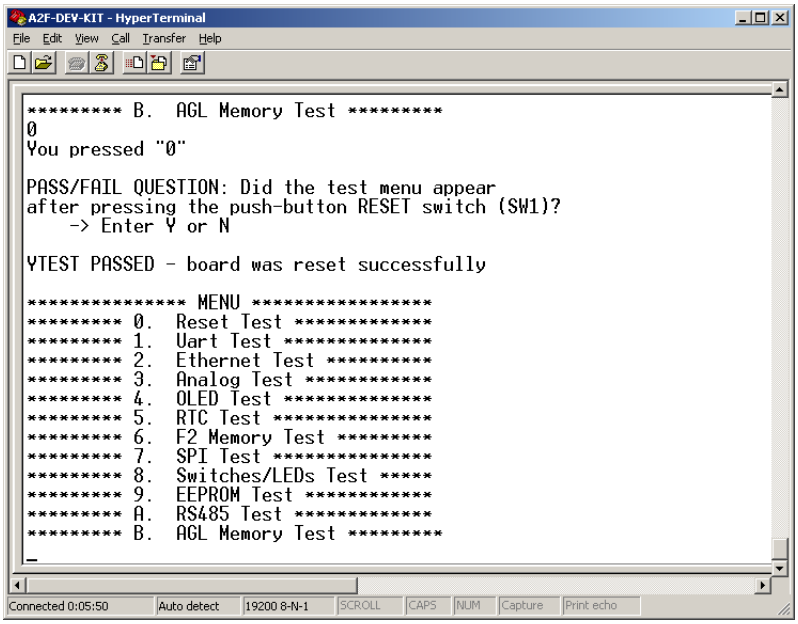


Figure 70 • **Reset Test Result**

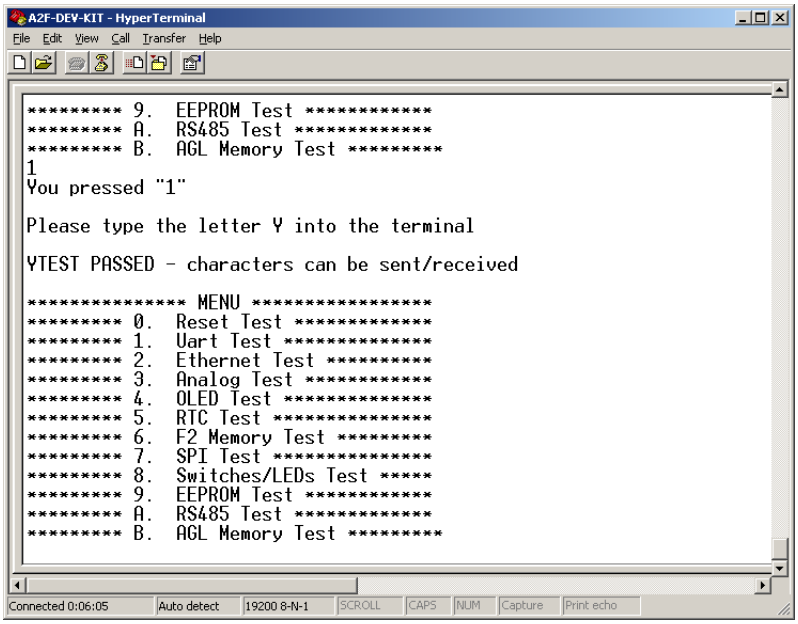


2. If the menu appears correct, enter the character **Y** into the terminal.

8.7.2 UART Test

Enter **1** into the terminal to begin the UART test. Type the character **Y** into the terminal. The result will be similar to the following figure.

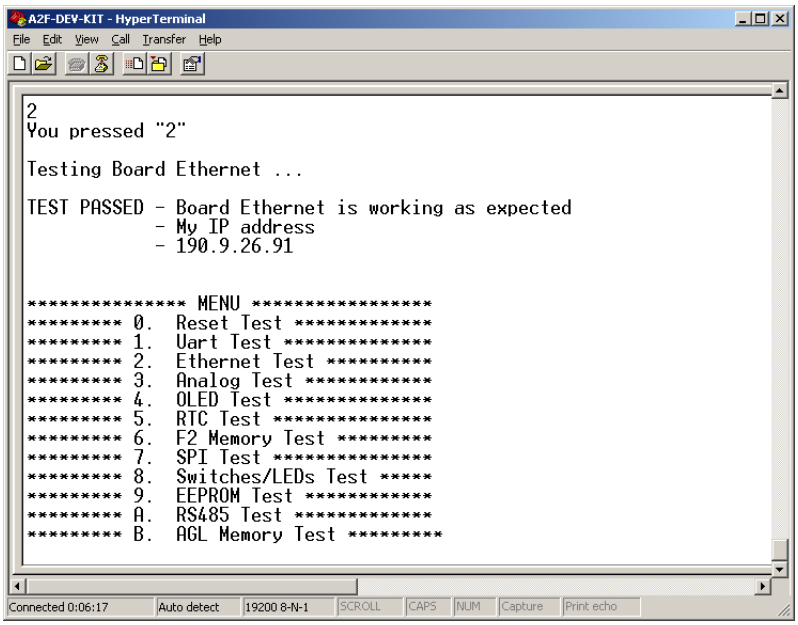
Figure 71 • **UART Test**



8.7.3 Ethernet Test

Enter **2** into the terminal to begin the Ethernet test. A screen similar to the following figure should appear.

Figure 72 • **Ethernet Test**

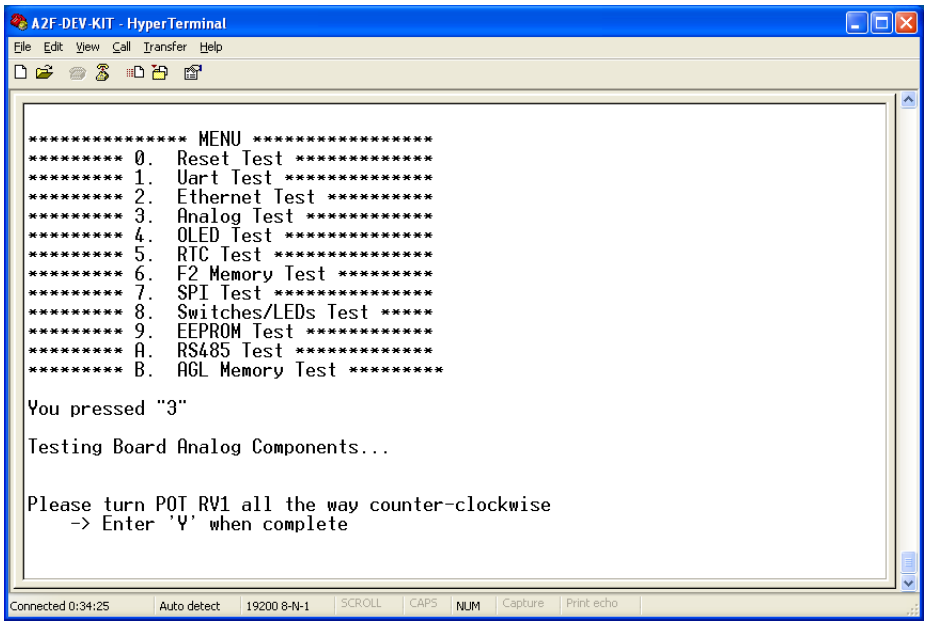


Note: The IP address may vary in the network setup.

8.7.4 Analog Test

1. Enter **3** into the terminal to begin the Analog test. A screen similar to the following figure should appear.

Figure 73 • **Analog Test**



2. Locate POT RV1 on bottom left hand corner of the board. Turn POT RV1 counter-clockwise all the way to the left, as shown in the following figure. A display similar to Figure 75, page 81 should appear on the terminal.

Figure 74 • **POT Selection**

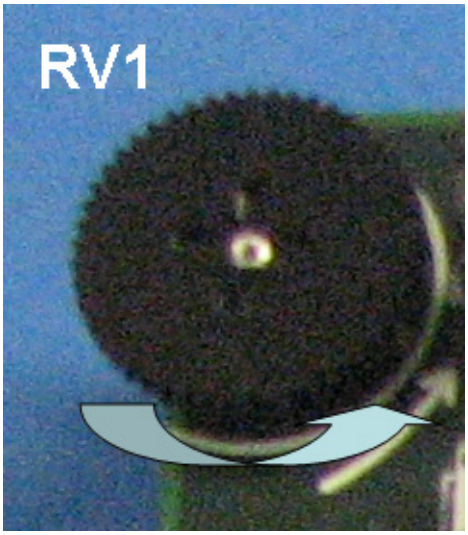
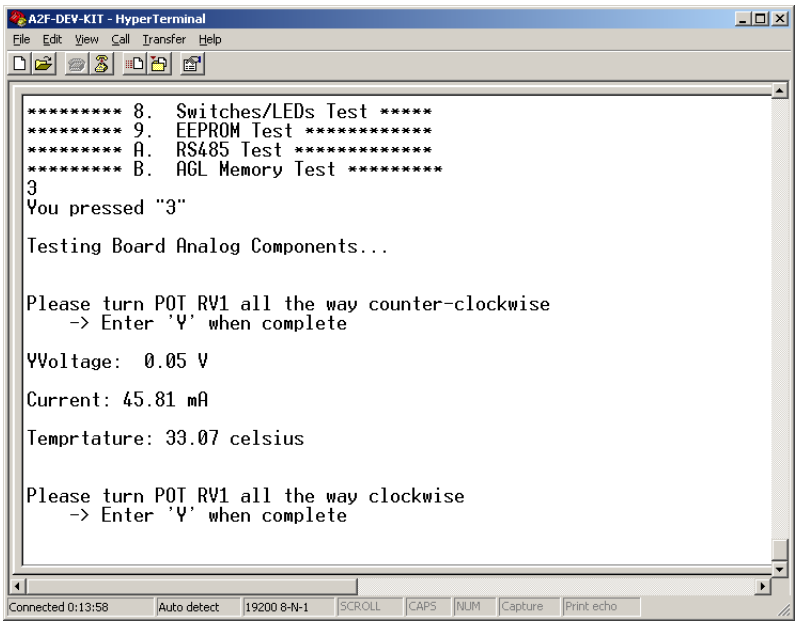
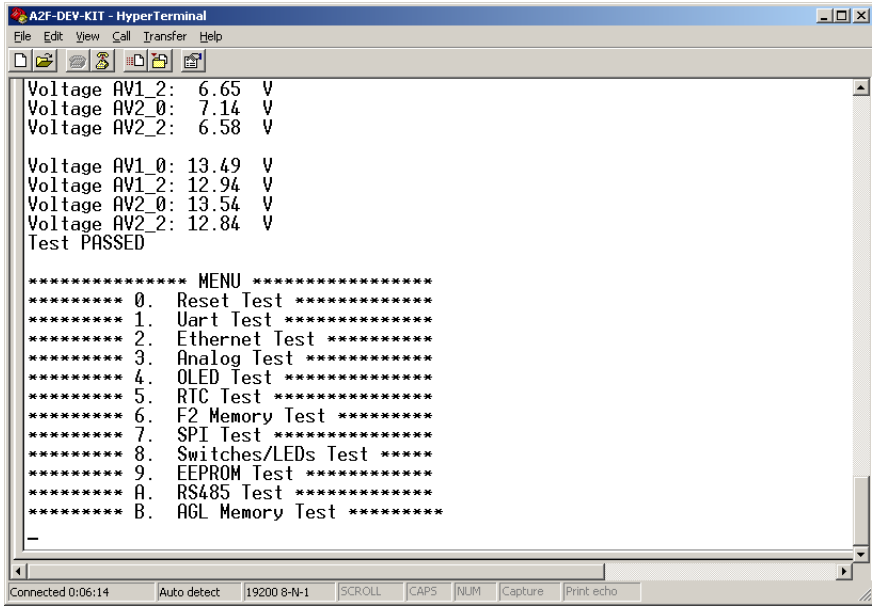


Figure 75 • **Analog Test**



3. Turn POT RV1 clockwise all the way clockwise all the way to the right. A display similar to the following figure should appear on the terminal.

Figure 76 • **Analog Test Results**

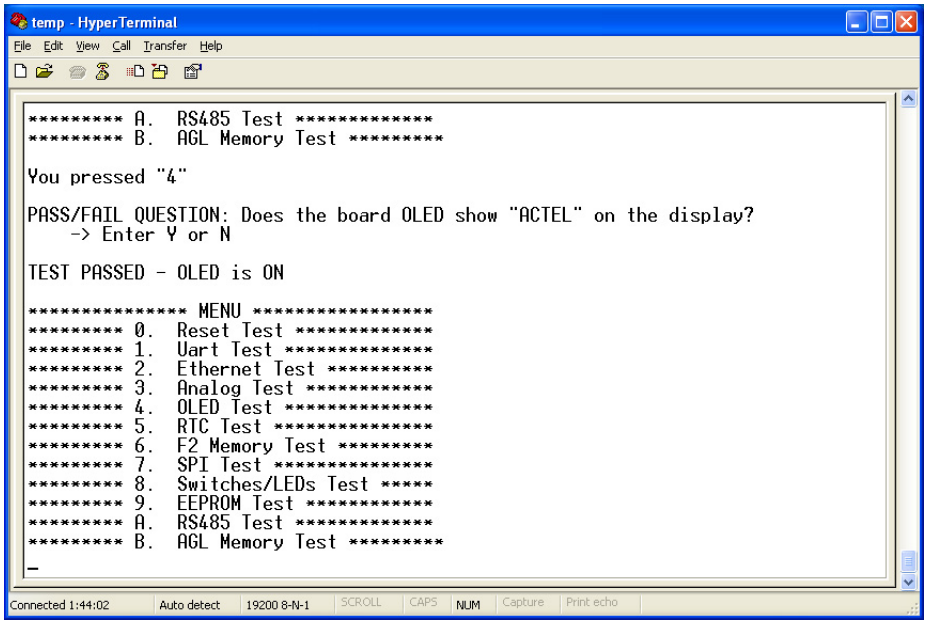


8.7.5 OLED Test

1. Enter **4** into the terminal to begin the OLED test.
2. Check the board OLED display. If the characters ACTEL MAN TEST are displayed in the OLED, then enter **Y** in the terminal; otherwise, enter **N**. If Y was entered, the screen shown in the following figure will be displayed:

Note: OLED is no longer populated on the latest revision of A2F500-DEV-KIT-2. For more information, see *PCN1502: Change in SmartFusion Development Kit (A2F500-DEV-KIT-2) hardware*..

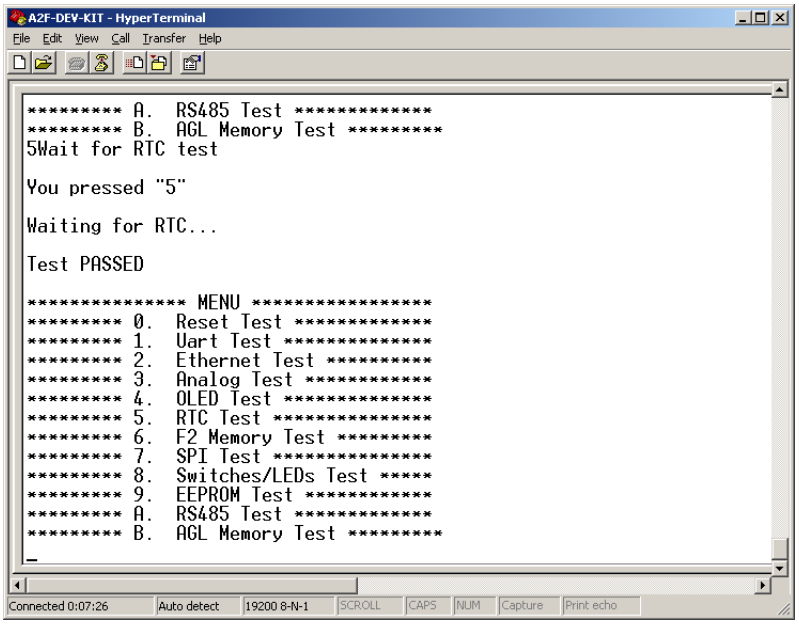
Figure 77 • **OLED Test**



8.7.6 RTC Test

Enter **5** into the terminal to begin the RTC test. After a few seconds, the screen shown in the following figure should appear.

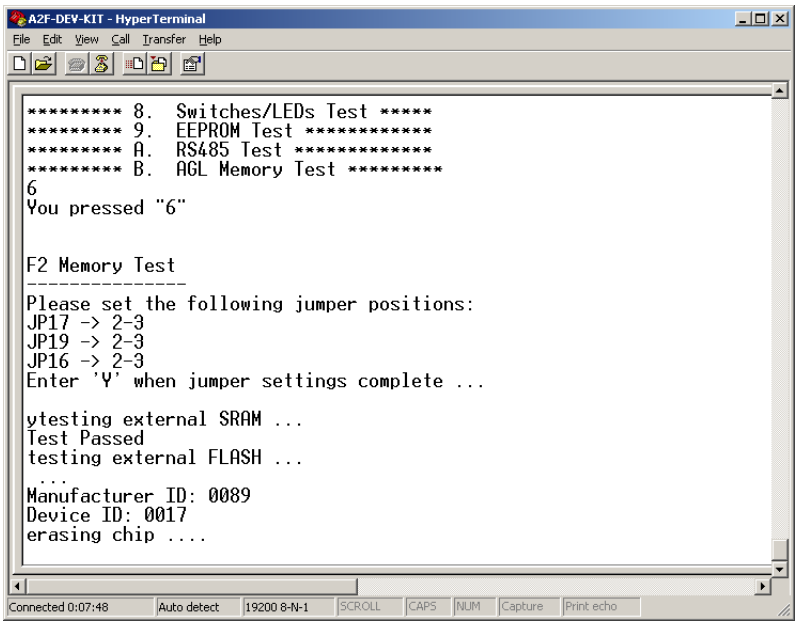
Figure 78 • **RTC Test**



8.7.7 Memory Test

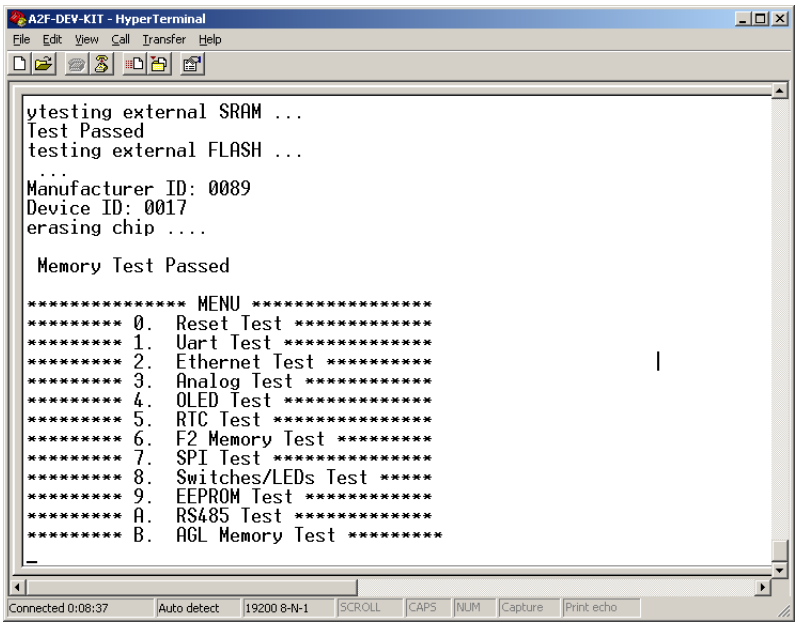
1. Enter **6** into the terminal to begin the SmartFusion Memory (EMC) test. After several seconds, the screen shown in the following figure should appear.

Figure 79 • **Memory Test**



2. Ensure jumpers JP17, JP19, and JP16 are set correctly and enter **Y** into the terminal. The display shown in the following figure should appear in the terminal.

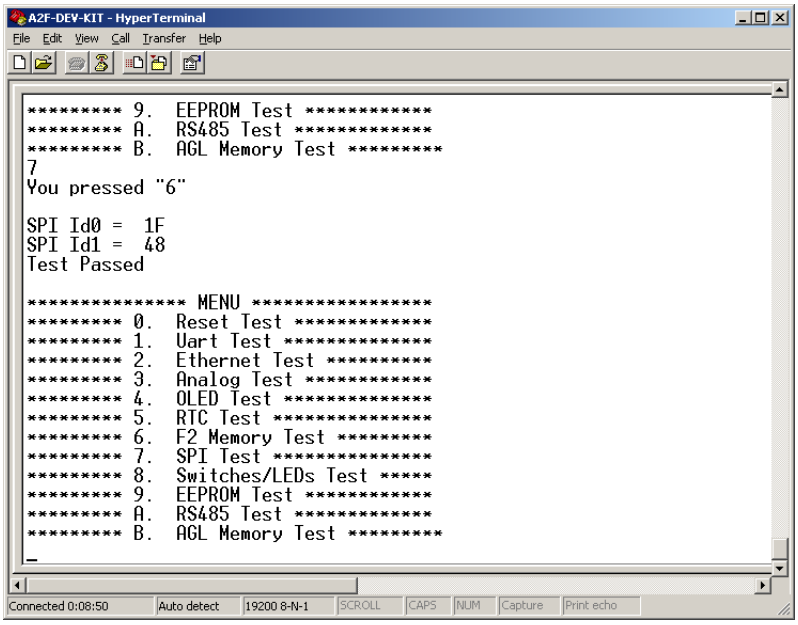
Figure 80 • **Memory Test Passed**



8.7.8 SPI Test

Enter **7** into the terminal to begin the SPI test. After several seconds, the screen shown in the following figure should appear.

Figure 81 • **SPI Test Results**



8.7.9 Switch/LED Test

1. Enter **8** into the terminal to begin the LEDs test. The screen shown in the following figure is displayed.

Figure 82 • **Switch/LEDs Test**

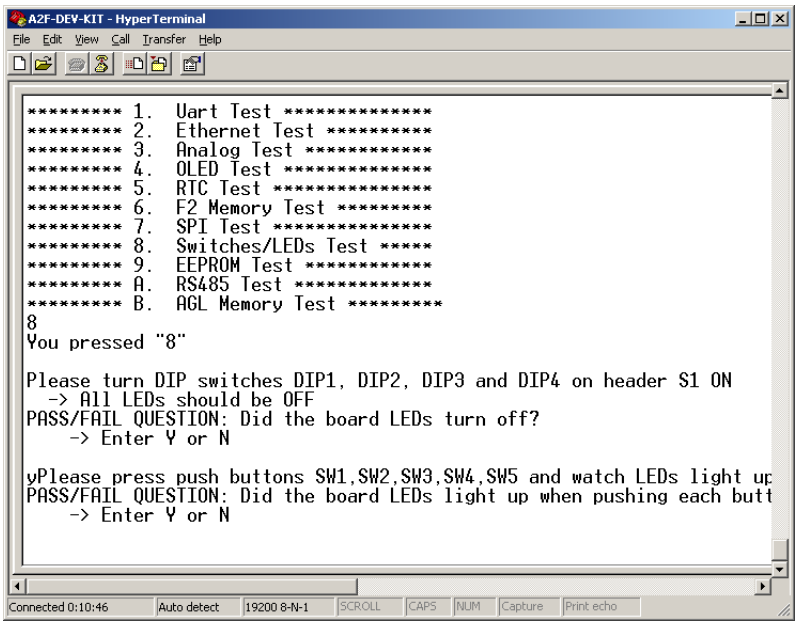
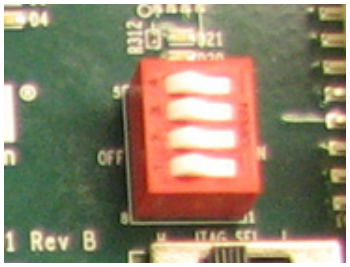


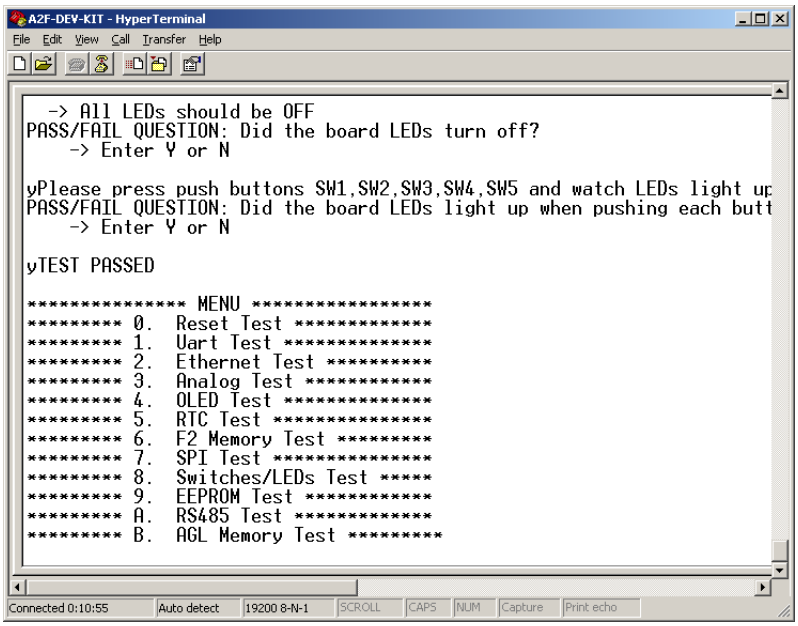
Figure 83 • **DIP Switch Settings**



2. Press push-buttons SW1, SW2, SW3, SW4 and SW5. When any of these buttons is pressed, the LEDs should light up.
3. Then press DIP1, DIP2, DIP3, DIP4. This should light up each of the 4 LEDs.

4. If you observed the LEDs light up, enter **Y** in the terminal. Otherwise enter **N**. If Y was entered, the screen shown in the following figure will be displayed.

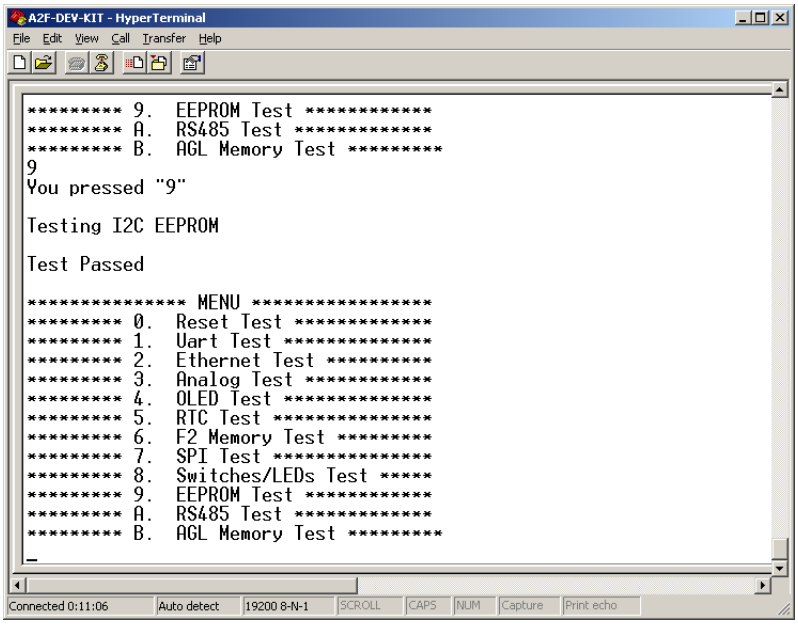
Figure 84 • **Switch Test**



8.7.10 I²C EEPROM

Enter **9** into the terminal to begin the I²C EEPROM test. The screen shown in the following figure is displayed after few seconds.

Figure 85 • **I²C EEPROM Test**



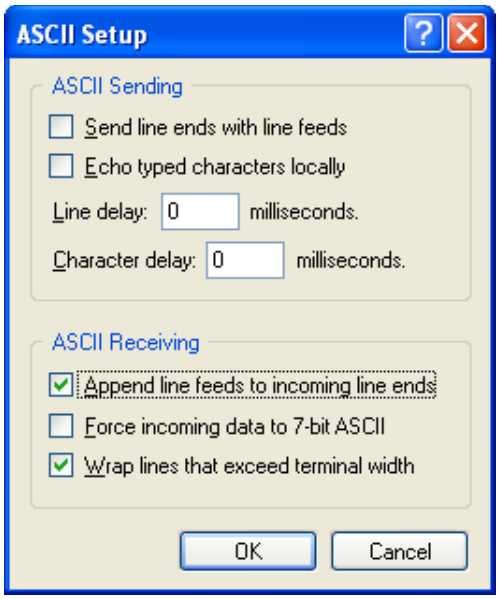
8.7.11 RS485 Test

1. Open another terminal window, this time set to COM. Configure as shown in Figure 86, page 87 through Figure 88, page 88.

Figure 86 • **COM1 Setting**

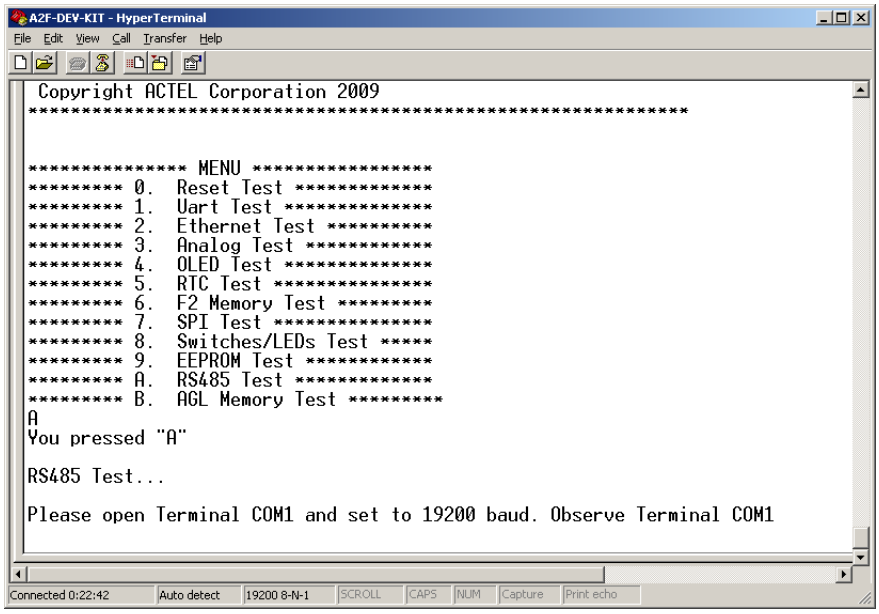
Figure 87 • **Connect To Dialog**

Figure 88 • **ASCII Setup**



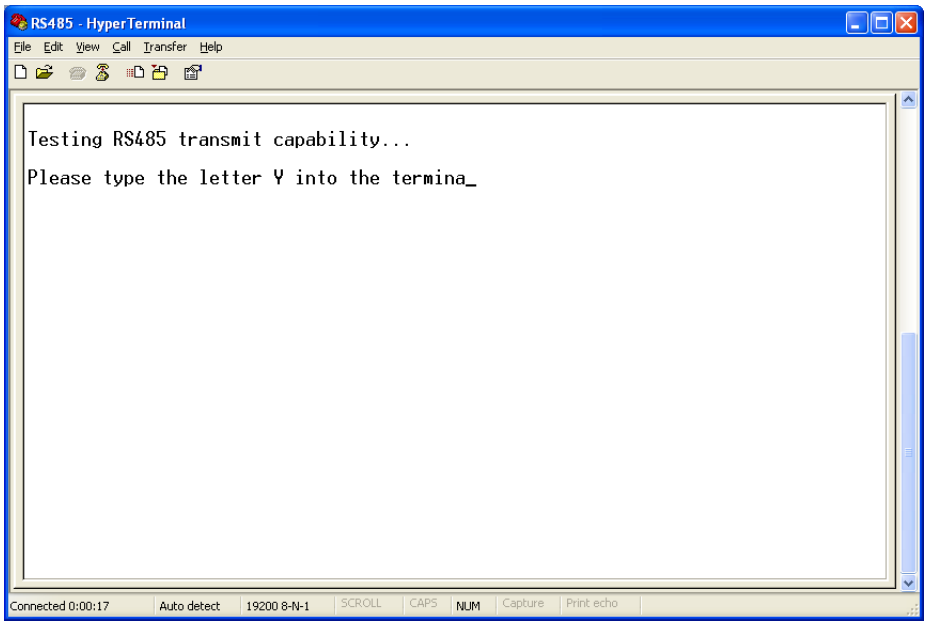
2. Enter **A** into the terminal to begin the RS485 test. The screen shown in the following figure is displayed.

Figure 89 • **RS485 Test**



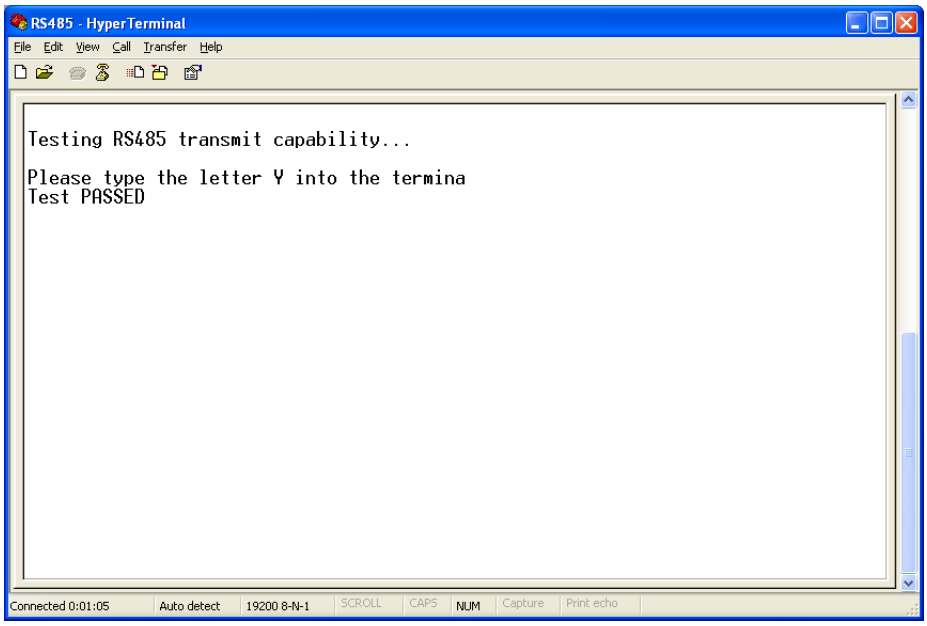
The display in the COM1 terminal window should be similar to the following figure.

Figure 90 • **RS485 Test Message**



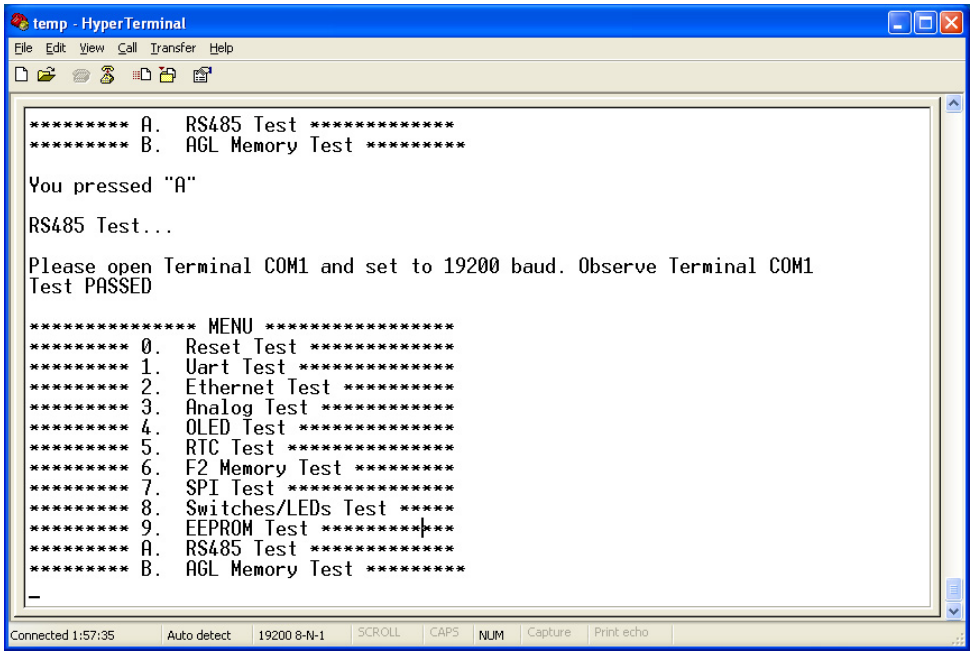
3. Enter the character **Y** into this terminal. The display on the COM1 terminal should be similar to the following figure

Figure 91 • **RS485 Test Message**



4. The display on the COM4 terminal should be as shown in the following figure

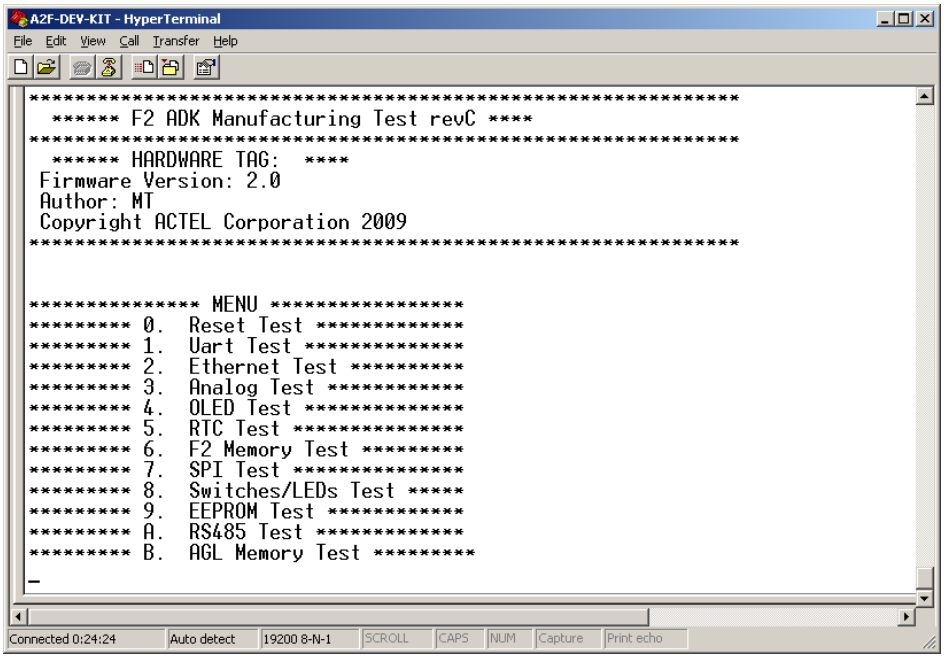
Figure 92 • **RS485 Test Passed**



8.7.12 AGL Memory Test

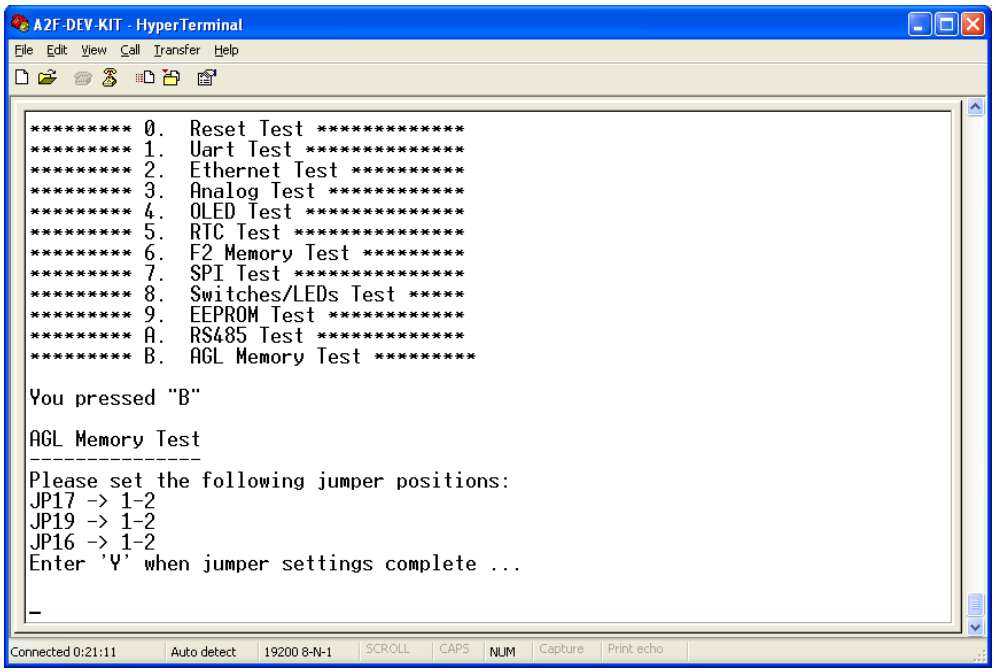
1. Turn off the board by flipping switch SW6 off.
2. Place board jumpers JP17, JP19, and JP16 in the following positions:
   JP17: 1–2
   JP19: 1–2
   JP16: 1–2
3. Turn on board power by flipping switch SW6. Press the reset button SW8. The screen shown in the following figure should appear.

Figure 93 • **Select AGL Memory Test**



4. Enter **B** into the terminal to begin the AGL memory test. The screen shown in the following figure is displayed.

Figure 94 • **AGL Memory Test**



5. When the jumpers are set, enter **Y** into the terminal. The display on the terminal should be similar to Figure 95, page 91, and eventually Figure 96, page 92.

Figure 95 • **AGL Test – Erasing Chip**

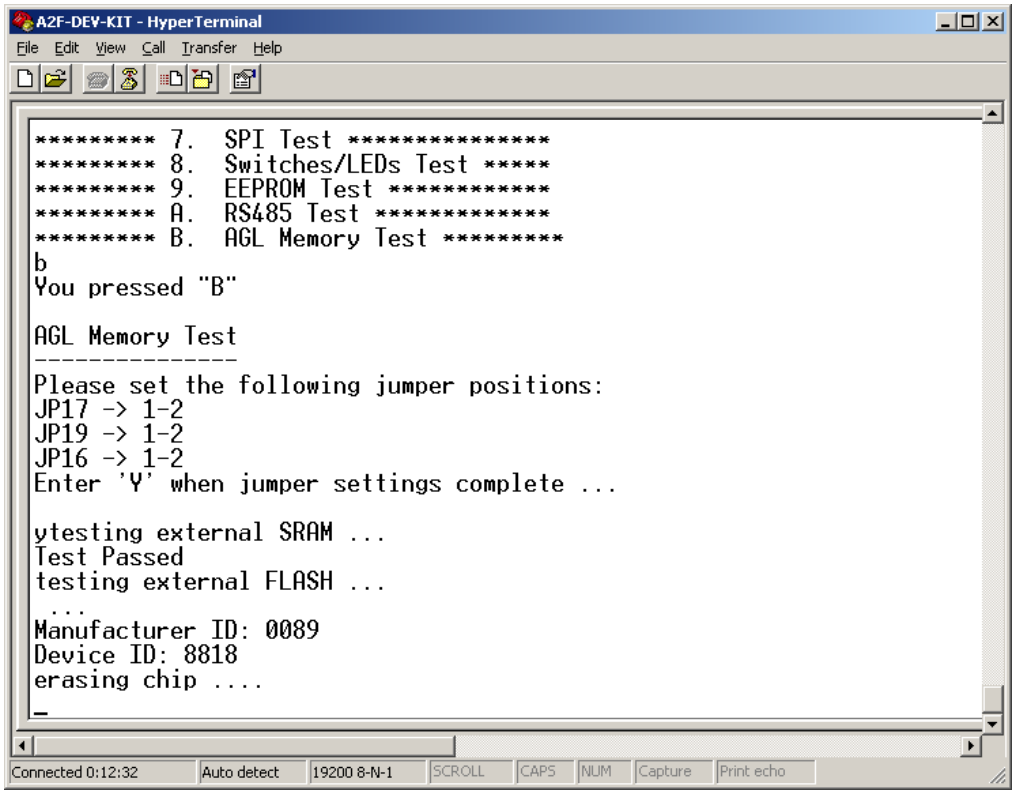
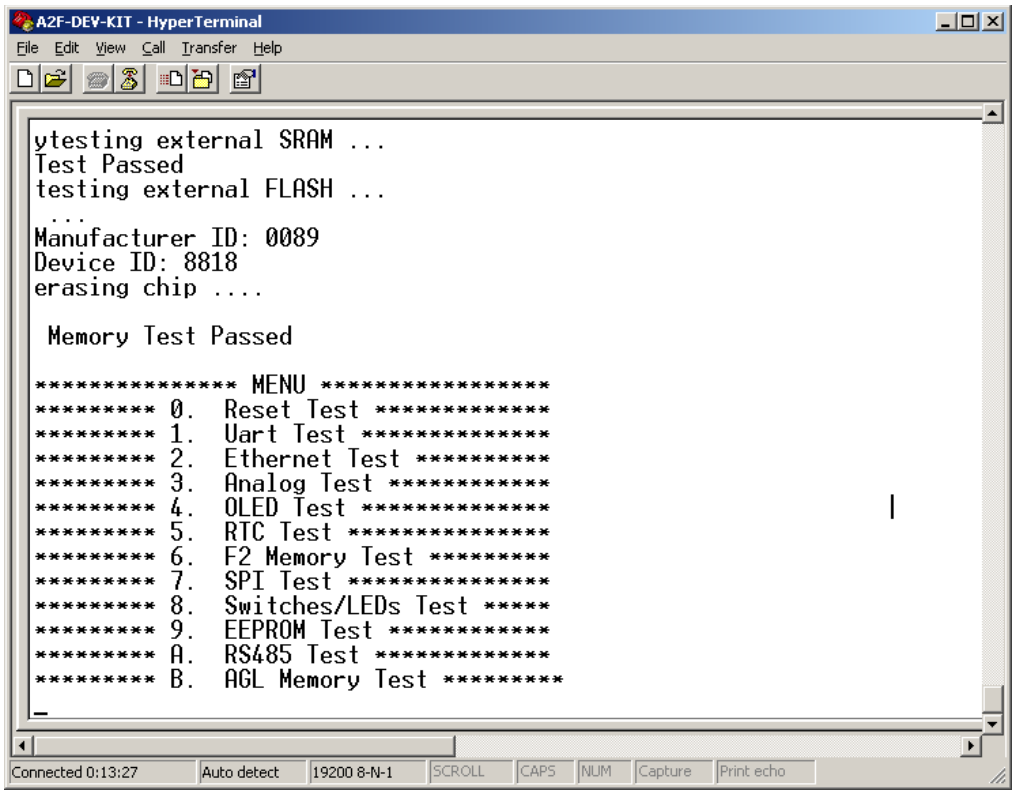


Figure 96 • **AGL Test Passed**



8.8 A2F500-DEV-KIT-2 Board Failures

All tests outlined in Running the A2F500-DEV-KIT-2 Board Test, page 77 should result in the words TEST PASSED being printed on the terminal. If this does not happen, or the words TEST FAILED are printed, the test has failed.