DirectC Frequently Asked Questions

Version 2.0

1. **What is DirectC programming?**

   DirectC is an Embedded In-System Programming (ISP) solution for Actel Flash FPGA devices

2. **What is required to enable DirectC Programming?**

   To perform In-System Programming (ISP) for the FPGA, the system must contain the following
   - Control logic (a microprocessor or a soft-core microprocessor implemented in another FPGA with at least 256 bytes of RAM)
   - JTAG interface to the target device
   - Access to the data file containing the programming data
   - Memory to store and run DirectC code

3. **What does the DirectC package contain?**

   DirectC package contains ANSI C compliant C code to support in-system programming along with sample project and documentation

4. **Do I have to make any changes to DirectC Code to work on my Setup?**

   Yes.

   Some minor modifications to the source code need to be done to address three major components of DirectC application. These components are JTAG interface functions, memory interface functions for the data file, and the delay function (dp_delay) defined in dpuser.c and dpcom.c. Once done, compile the source code to create a binary executable. This binary executable is downloaded into the system along with the programming data for execution

5. **What functions do I need to change in DirectC code?**

   You must modify the *dpuser.h* and *dpuser.c* files when using the DirectC source code. Please refer to the "Required Source Code Modifications" section in the **DirectC User's Guide** for specific details

6. **I am using a processor for DirectC. What type of I/O can I use to connect to JTAG signals?**

   DirectC supports discrete JTAG toggling. You can use a General Purpose I/O to connect to JTAG signals (TDI, TMS, TCK, TRSTN, TDO). JTAG port on Actel devices is LVTTL.

7. **What Microprocessors/Microcontrollers are supported?**

   Any Microprocessor/Microcontroller that comes with ANSI C-Compliant compiler is supported.

8. **Does DirectC code work on the 8051 Processor?**
   Yes

9. **Does DirectC run on a DSP processor?**
   Yes

10. What the memory requirements for DirectC?

The following applies to DirectC Version 2.0 and higher.
Microprocessor with a minimum of 256 Bytes RAM is required to run DirectC. There are two components of memory required

- Memory to store compiled DirectC code, the application code. While this varies based on the compiler switches selected, it does not vary much based on the device selected
- Memory to hold the programming data (*.dat). This depends on the device being programmed, plain text or encrypted programming

Refer to the latest DirectC User's Guide for updated information

ProASICPLUS uses STAPL files that require large amount of memory, so if you are using ProASICPLUS your memory requirements also depend on the size of the device.

11. What devices/families are supported by DirectC?

DirectC Version 1.3 solution supports the ProASICPLUS FPGA family of devices.
DirectC V2.0 and higher support Fusion, IGLOO and ProASIC3 Mixed-Signal FPGA devices and their derivatives.
Neither version of DirectC supports ProASIC devices.

12. Does the DirectC for ProASICPLUS support all flash devices?

No. Refer to question 11 for the list of supported families.

13. How long does it take to program with DirectC?

The time taken to program depends on the speed of the microprocessor, speed of the I/O driving the JTAG signals, device size and data access speed.

14. What is DatGen?

Datgen is a standalone program that is used to generate the "*.dat" file, which contains programming data extracted from the STAPL file. This was required before Libero IDE v8.5. With Libero IDE v8.5, the *.dat file can be generated from Designer similar to a STAPL or PDB file

15. What is a *.dat file?

The *.dat file contains programming data for the device to be programmed with DirectC. This is to reduce the run time memory and data storage requirement.

16. How do I generate a *.dat file?

This is not required for Libero IDE v8.5 or later. However if the design is created with an earlier version of Libero IDE and STAPL is available, the DATGEN executable which is available in DirectC package versions prior to Version 2.4 can be used to generate the *.dat file.

To generate the DAT file:

- Copy *datgen.exe* to a local directory
- Copy the STAPL files to the same directory as *datgen.exe*
- From the DOS prompt, type the following command:
  - DatGen <STAPL file>
- The output is a binary data file (**.dat*) with same name as input file

17. Does ProASICPLUS require a *.dat file?

ProASICPLUS uses a different version of DirectC compared with other flash devices. This version of DirectC (As of Q4-2008, the latest is v1.3), uses a STAPL file. It does not use a DAT file

18. Libero IDE version compatibility with DirectC?

While there is no direct link between these two, the way STAPL file and DAT files are generated evolved over time. The following table summarizes the evolution. This applies to flash families except ProASICPLUS.

DirectC Version	Libero IDE Version	DAT File Generation	Comment
Version 2.2	Libero IDE v8.4 and earlier	DATGEN (STAPL file)	Datgen must be used to generate the DAT file from the STAPL file
Version 2.3	Libero IDE v8.5	Designer	DAT file could be generated from Designer or from Datgen utility. Both files are identical. DAT file from Libero IDE v8.4 can be used
Version 2.4	Libero IDE v8.6	Designer	Datgen is no longer supported with this version of the software. Designer software must be used to generate the DAT file.

19. Is there a limit on the JTAG Clock (TCK) Frequency?

Not applicable. DirectC uses discrete JTAG Signal Toggling. So there is no frequency associated to TCK. However, Fusion, IGLOO and ProASIC3 devices have a limit of 20MHz.

20. What are the power supply requirements?

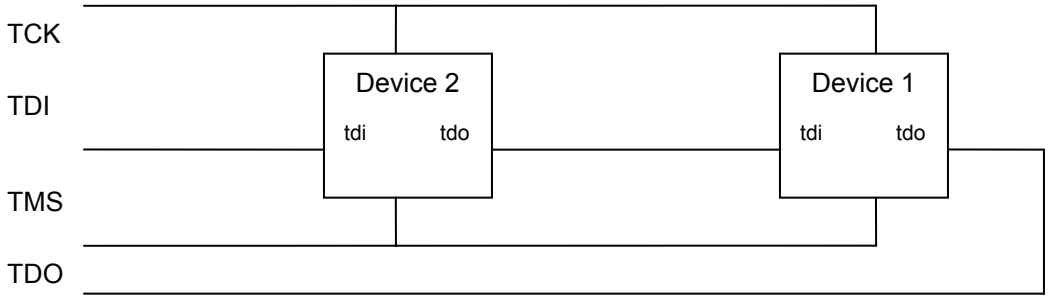
The VCC, VPUMP and VJTAG power supplies are required. Please refer to the datasheet for the FPGA family for power specifications.

21. Are there any bypass capacitor requirements for DirectC?

Yes. For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible. The bypass capacitor must be placed within 2.5 cm of the device pins

22. How do I enable Chain Programming with DirectC?

Please refer to the "Chain Programming Section" of the **DirectC User's Guide**.
In a setup which has two Actel Flash Devices in a chain, AGL600 for example



1. Chain setup:

To program Device 1, we need to set up the pre and post IR/DR to:

// START Actel Chain Configuration

#define PREIR_DATA_SIZE 1 // Byte

#define PREDR_DATA_SIZE 1 // Byte

#define POSTIR_DATA_SIZE 1 // Byte - dummy

#define POSTDR_DATA_SIZE 1 // Byte - dummy

#define PREIR_LENGTH_VALUE 0 // bits

#define PREDR_LENGTH_VALUE 0 // bits

#define POSTIR_LENGTH_VALUE 8 // bits

#define POSTDR_LENGTH_VALUE 1 // bits

// END Actel Chain Configuration

To program Device 2, we need to set up the pre and post IR/DR to:

// START Actel Chain Configuration

#define PREIR_DATA_SIZE 1 // Byte - dummy

#define PREDR_DATA_SIZE 1 // Byte - dummy

#define POSTIR_DATA_SIZE 1 // Byte

#define POSTDR_DATA_SIZE 1 // Byte

#define PREIR_LENGTH_VALUE 8 // bits

#define PREDR_LENGTH_VALUE 1 // bits

#define POSTIR_LENGTH_VALUE 0 // bits

#define POSTDR_LENGTH_VALUE 0 // bits

// END Actel Chain Configuration

23. How do I read Device ID using DirectC?

There is a standalone action called “read_idcode”. Assign the Action_code variable to DP_READ_IDCODE_ACTION_CODE prior to calling dp_top.

24. Can I select I/O-State during DirectC Programming?

You can specify individual I/Os to drive high, low, or tri-state during generating the DAT file from Designer.

Maintaining the last known state of the I/Os is possible. See question 25 for more details on how to do it. However, this setting must be applied to all I/Os.

25. How do I maintain the last known state of the I/Os?

To maintain the last known state of all I/Os, uncomment #define **BSR_SAMPLE** in dpuser.h. By doing this, DirectC ignores the BSR setting in the DAT file.

26. Can I use DirectC to program incremental UID to Flash ROM?

No. This feature is not supported

27. What action codes are supported in DirectC?

The following Action codes are supported as of DirectC v2.4

#define DP_DEVICE_INFO_ACTION_CODE 1
#define DP_READ_IDCODE_ACTION_CODE 2
#define DP_ERASE_ACTION_CODE 3
#define DP_ERASE_ALL_ACTION_CODE 4
#define DP_PROGRAM_ACTION_CODE 5
#define DP_VERIFY_ACTION_CODE 6
#define DP_ENC_DATA_AUTHENTICATION_ACTION_CODE 7
#define DP_ERASE_ARRAY_ACTION_CODE 8
#define DP_PROGRAM_ARRAY_ACTION_CODE 9
#define DP_VERIFY_ARRAY_ACTION_CODE 10
#define DP_ERASE_FROM_ACTION_CODE 11
#define DP_PROGRAM_FROM_ACTION_CODE 12
#define DP_VERIFY_FROM_ACTION_CODE 13
#define DP_ERASE_SECURITY_ACTION_CODE 14
#define DP_PROGRAM_SECURITY_ACTION_CODE 15
#define DP_PROGRAM_NVM_ACTION_CODE 16
#define DP_VERIFY_NVM_ACTION_CODE 17
#define DP_VERIFY_DEVICE_INFO_CODE 18

```
#define DP_READ_USERCODE_ACTION_CODE 19
#define DP_PROGRAM_NVM_ACTIVE_ARRAY_CODE 20
#define DP_VERIFY_NVM_ACTIVE_ARRAY_CODE 21
```

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