CoreMP7Bridge Datasheet

DirectCore

Product Summary

Intended Use

- Intended for Use with CoreMP7 in an AMBA-Based Subsystem Deployed through CoreConsole

Key Features

- Supplied in SysBASIC Core Bundle
- Synchronizes and Controls all Signals In and Out of the CoreMP7
- Provides Interrupt Synchronization
- Configurable for RealView, GDB, or No Debug
- Auto Stitching of Signals in CoreConsole

Benefits

- Allows Easy Connection of CoreMP7 to AHB
- Implements Recommended Practice Handling of Resets and Clocks
- Auto Stitch in CoreConsole for Rapid Development
- Compatible with AMBA and CoreMP7

ARM Supported Families

- ProASIC®3 (M7A3P)
- ProASIC3E (M7A3PE)
- Fusion (M7AFS)

Synthesis and Simulation Support

- Supported in the Actel Libero® Integrated Design Environment (IDE)

Verification and Compliance

- Compliant with AMBA

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General Description

CoreMP7Bridge has two functions. It converts the native signals from the CoreMP7 processor into an AMBA AHB master interface suitable for connection to an AHB bus, and it includes circuitry that deals with reset signals and the signals which connect to the ARM RealView ICE JTAG port. The incoming hardware reset signal is synchronized to the system clock and a provision is made for handling a watchdog-generated reset in the case where a watchdog component is included in the system. Circuitry to condition the RealView ICE signals is also included.

Connecting the CoreMP7Bridge

CoreMP7Bridge is normally auto stitched in CoreConsole and the required connections are made automatically. If Debug is selected as a configuration option, the Debug bus (RealView, UJTAG, or both) needs to be stitched out to the top level of the CoreConsole design (see Figure 1 on page 2). Since they are represented as busses in CoreConsole, it is a single connection for each. ALL signals going to the CoreMP7 now go through the CoreMP7Bridge, including Interrupts, Clocks, and Reset. The connection to the CoreMP7 is a single bus called the MP7_SysIf, which is auto stitched. This encapsulates all the relevant signals (this bus may be connected directly from CoreMP7 to the top level if the CoreMP7 is being instantiated on its own without a CoreMP7Bridge or other components).

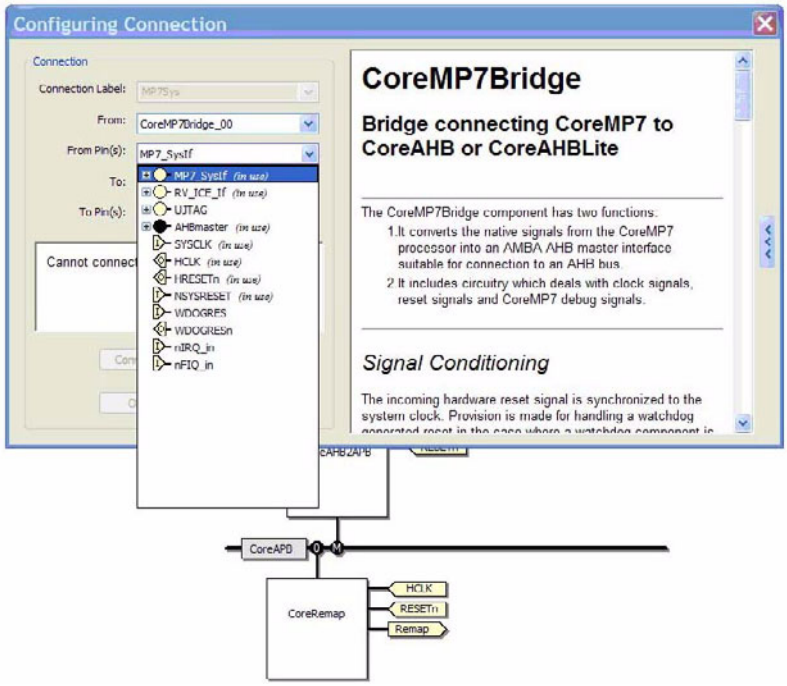

Figure 1 • **Configuring CoreMP7Bridge Connection**

The full set of connections is shown in Figure 2.

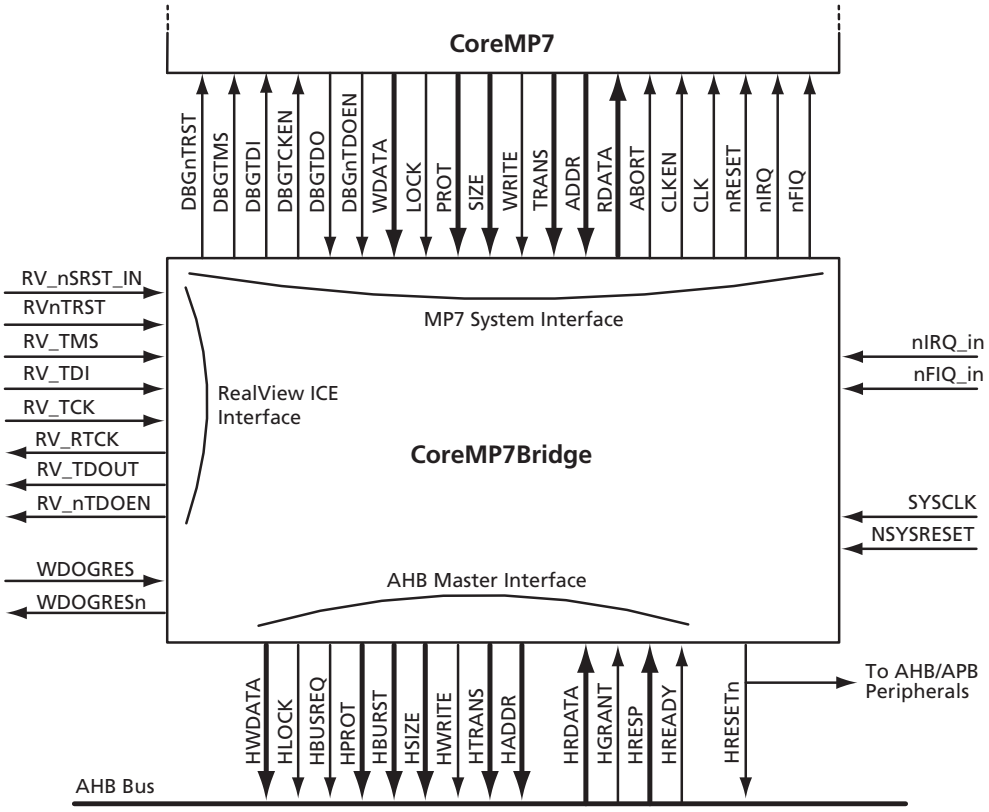

Figure 2 • **CoreMP7Bridge Connection**

Configuration

The standard approach to instantiating CoreMP7Bridge in your design is to add it to a design in CoreConsole and auto stitch it. You will be presented with four configuration items:

Synchronize nIRQ

Default: No

Synchronizes nIRQ_in to CLK if not already synchronized (e.g. from an external source).

Note that CoreInterrupt does NOT synchronize its interrupt sources.

Synchronize nFIQ

Default: No

Synchronizes nFIQ_in to CLK if not already synchronized (e.g. from an external source).

Note that CoreInterrupt does NOT synchronize its interrupt sources.

Debug

Default: RealView

There are 3 choices for Debug.

1. **Disabled**
   All interrupt logic is removed.
2. **RealView**
   The RealView ICE logic is enabled and the RV_ICE_If bus can be connected to the top level and mapped to pads.
3. **RealView or FlashPro3**
   Both the RealView ICE and GDB debug logic is enabled and instantiated and both the RV_ICE_If and UJTAG busses can be connected out. Note that these cannot be used simultaneously even if both sets of pins are available from the FPGA, but they can both be used.

Family

Default: Fusion

Choices: ProASIC3, ProASIC3/E, Fusion

Port List

Table 1 lists the ports present on the CoreMP7Bridge component and provides a brief description of each port.

Table 1 • **CoreMP7Bridge Port List**

Port Name	Width	Direction	Description
System Connections			
SYSCLK	1	Input	Raw system clock input from top level
NSYSRESET	1	Input	Raw hardware system reset input from top level. Will typically be controlled by a push-button switch.
AHB Connections			
HREADY	1	Input	AHB ready signal
HRESP	2	Input	AHB response signal
HGRANT	1	Input	AHB grant signal
HRDATA	32	Input	AHB read data

Table 1 • **CoreMP7Bridge Port List (Continued)**

Port Name	Width	Direction	Description
HRESETn	1	Output	AHB reset signal (active low). This reset may be asserted asynchronously but will always be negated synchronous to HCLK.
HADDR	32	Output	AHB address signal
HTRANS	2	Output	AHB transfer type signal
HWRITE	1	Output	AHB read/write indication
HSIZE	3	Output	AHB size (byte, word etc.) of transfer indication
HBURST	3	Output	AHB burst signal
HPROT	4	Output	AHB protection signal
HBUSREQ	1	Output	AHB bus request. In a single master system this port will typically be unconnected. Where there are multiple masters it will be connected to some form of arbitration component.
HLOCK	1	Output	AHB lock signal
HWDATA	32	Output	AHB write data
CoreMP7 Connections			
CLK	1	Output	Clock signal. Connect to CLK port of CoreMP7.
nRESET	1	Output	Reset signal. Connect to nRESET port of CoreMP7.
ADDR	32	Input	Address bus. Connect to ADDR port of CoreMP7.
LOCK	1	Input	Lock signal. Connect to LOCK port of CoreMP7.
SIZE	2	Input	Size signal. Connect to SIZE port of CoreMP7.
WRITE	1	Input	Write signal. Connect to WRITE port of CoreMP7.
PROT	2	Input	Protection signal. Connect to PROT port of CoreMP7.
TRANS	2	Input	Transfer signal. Connect to TRANS port of CoreMP7.
WDATA	32	Input	Write data. Connect to WRITE port of CoreMP7.
ABORT	1	Output	Abort signal. Connect to ABORT port of CoreMP7.
CLKEN	1	Output	Clock enable. Connect to CLKEN port of CoreMP7.
RDATA	32	Output	Read data. Connect to RDATA port of CoreMP7.
DBGnTRST	1	Output	Connect to DBGnTRST port of CoreMP7.
DBGTMS	1	Output	Connect to DBGTMS port of CoreMP7.
DBGTDI	1	Output	Connect to DBGTDI port of CoreMP7.
DBGTCKEN	1	Output	Connect to DBGTCKEN port of CoreMP7.
DBGTDO	1	Input	Connect to DBGTDO port of CoreMP7.
DBGnTDOEN	1	Input	Connect to DBGnTDOEN port of CoreMP7.
nIRQ	1	Output	Connect to nIRQ on CoreMP7.
nFIQ	1	Output	Connect to nFIQ on CoreMP7.
Watchdog Connections			
WDOGRES	1	Input	Watchdog reset input. If a watchdog is present in the system, this port should be connected to the "bark" port of the watchdog, which is the signal the watchdog asserts when it initiates a reset. This input is active high.

Table 1 • **CoreMP7Bridge Port List (Continued)**

Port Name	Width	Direction	Description
WDOGRESn	1	Output	Active low reset output to watchdog. Should be connected to the reset port of the watchdog (if present). This output is asserted when NSYSRESET is asserted, but not when WDOGRES is asserted. This allows the watchdog to reset the system without resetting itself.
RealView ICE JTAG Connections			
RV_nSRST_IN	1	Input	RealView ICE system reset input. Connect to top level if using RealView.
RV_nTRST	1	Input	RealView ICE Test Access Port (TAP) reset. Connect to top level if using RealView.
RV_TMS	1	Input	RealView ICE test mode select. Connect to top level if using RealView.
RV_TDI	1	Input	RealView ICE test data in. Connect to top level if using RealView.
RV_TCK	1	Input	RealView ICE test clock. Connect to top level if using RealView.
RV_RTCK	1	Output	RealView ICE return test clock. Connect to top level if using RealView.
RV_TDOUT	1	Output	RealView ICE test data out. Connect to top level if using RealView.
RV_nTDOEN	1	Output	RealView ICE test data out enable. Connect to top level if using RealView.
Other Connections			
nIRQ_in	1	Input	Connect the source IRQ interrupt that is intended for connection to the CoreMP7 IRQ input.
nFIQ_in	1	Input	Connect the source FIQ interrupt that is intended for connection to the CoreMP7 FIQ input.

Resource Requirements

The Utilization for CoreMP7Bridge is 440 tiles maximum (including RealView and GDB debug logic).

Ordering Information

CoreMP7Bridge is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreMP7Bridge cannot be ordered separately from the SysBASIC core bundle.

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version	Page
Advanced v0.1	Figure 2 was updated.	2
	Table 1 was updated to remove HCLK and change CLK and nRESET to Output from Input.	3
	The "Synchronize nIRQ" section and "Synchronize nFIQ" section were updated to change HCLK to CLK.	3

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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