Converting Triscend TE5 Designs to Actel Flash-Based FPGAs

Introduction: Core8051 and the Actel Flash-Based Family of FPGAs

Actel Flash-based FPGA families provide the ultimate way to implement a customizable microcontroller platform. With Core8051 Intellectual Property (IP), these versatile and high-performance Flash-based FPGAs become high-performance, industry-standard 8051/52-compatible microcontrollers with full debugging capabilities. Depending on the device selected, huge amounts of RAM and programmable logic are available to implement high-performance busses, memory interfaces, and any additional custom logic an application may require.

The Triscend® TE5 family of microcontrollers and programmable logic, a competing product, has been end-of-lifed. This application note highlights the key advantages of moving Triscend TE5 designs to Actel Flash-based FPGA devices using the Actel Core8051 microcontroller IP macrocell.

Actel ProASIC^{PLUS}® and ProASIC3 Flash-based FPGAs are discussed in this application note, but all recently released Actel FPGA families (Axcelerator®/RTAX-S, SX-A/RT54SX-S, ProASIC^{PLUS}, and ProASIC3) are excellent choices for implementing Core8051 designs.

8051 Microcontroller

Actel Core8051 IP Overview

The Core8051 macrocell is a high-performance, 8-bit microcontroller IP core. It is a fully functional 8-bit embedded controller that executes all ASM51 instructions and has the same instruction set as the 80C31 and other 8051 family microcontrollers. Unlike competitive MPU products, Core8051 is a true MCU and provides software and hardware interrupts, a serial port, and two timers.

The Core8051 architecture eliminates redundant bus states and implements a two-stage pipeline with parallel execution of fetch and execution phases. Cycles are aligned with memory fetch where possible, so most of the one-byte instructions are performed in a single cycle. This leads to an average performance increase of eight times with respect to the Intel device running at the same clock frequency. This is due to the drastically lower number of clock cycles required per instruction.

This core has been implemented in all of the most popular Actel FPGA devices (see the *Core8051 datasheet* for details). Actel Flash devices are a particularly good fit with their Flash-based programmable logic cells and abundant RAM, as described in this document.

Comparison to Triscend TE5 Microcontroller

- Both Core8051 and the TE5 are compatible with ASM51 and third party compilers and assemblers. Both feature dual data pointers, UARTs, timers, and multiple interrupt sources with selectable priority.
- Both Core8051 and the TE5 can be expanded by adding functionality to the SFR space or XDATA memory-mapped registers.
- The Triscend TE5 requires a minimum of 4 clock cycles to execute an instruction, with some instructions requiring as many as 8 to 12. The Actel Core8051 uses only one clock cycle to implement most instructions. Even for complex instructions, Core8051 requires only two or three clock cycles, which is one quarter the number of cycles used by the Triscend microcontroller.

- The Triscend TE5 operates at up to 10 millions of instructions per second (MIPS), while Core8051 operates at 15 MIPS to 45 MIPS depending on the Actel FPGA family used. The total performance improvement for Core8051 over the Triscend TE5 is more than 4 times in some Actel FPGA devices.

Former Triscend users will have no difficulty understanding and using Core8051 from a logical and functional point of view. Other than the significant performance increase of Core8051, the microcontrollers are almost indistinguishable in functionality.

Programmable Logic for Customer Logic Implementations

Actel Flash-Based FPGA Overview (ProASIC^{PLUS})

The ProASIC^{PLUS} family of devices, the second generation Actel Flash FPGAs, offers enhanced performance over the Actel ProASIC® family. ProASIC^{PLUS} combines the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC^{PLUS} family offers a unique clock conditioning circuit based on two on-board phase-locked loops (PLLs). The family offers up to one million system gates, supported with up to 198 kbits of two-port SRAM and up to 712 user I/Os, all providing PCI-compatible performance.

Comparison to Triscend TE5 FPGA Fabric

- Triscend offers a limited quantity of FPGA resources with a maximum of only 2,000 registers and/or 4-input LUTs, while the Actel ProASIC^{PLUS} family features up to 56,320 tiles (registers). Even after considering the number of tiles on the Actel device needed to implement Core8051, ProASIC^{PLUS} FPGAs will have up to 20 times more available FPGA resources than Triscend FPGAs.
- Actel FPGAs are live at power-up and do not require time to be configured, while the Triscend FPGA must be configured at power-up. A second, expensive non-volatile memory to hold the FPGA image is not needed with Actel FPGAs.
- Typical FPGA system speeds for the Triscend FPGA logic are limited to 25 to 40 Mhz, while Actel FPGAs support system speeds up to 150 MHz for ProASIC^{PLUS} FPGAs and more than 350 MHz for the Axcelerator (AX) FPGA family.
- Actel FPGAs make use of general purpose routing resources to implement all logic and have up to 88 low-skew clock segments. Triscend TE5 programmable logic requires the use of cumbersome, special purpose, bus-based routing resources that limit the flexibility of the design.
- Actel FPGAs are available with up to 712 usable I/Os. Triscend was limited by a PQ208 package to 150.

Converting custom FPGA logic designs from Triscend to Actel ProASIC^{PLUS} will dramatically increase performance and the amount of usable resources. Both systems rely on Synplicity® for Verilog or VHDL synthesis, and resynthesizing behavioral Verilog or VHDL will be extremely efficient. Only in cases where Triscend-specific primitives are instantiated in the source code will this process require design effort.

System Architecture

Triscend devices feature a large and complex system that takes up space and must be configured whether in use or not. Actel designs make use of FPGA technology to implement only the system hardware components that are required. This makes the Actel solution more flexible. However, some peripheral system components that exist in the Triscend TE5 chips may have to be recreated by the application designer if needed in an Actel system.

The large and versatile Actel FPGA logic and I/O circuitry have almost no limit to their capabilities. Actel customers are not limited by the Triscend least-common-denominator system architecture methodology.

With Triscend, the primary interface to the TE5 system is the CSI bus. This is an 8-bit synchronous data bus with single cycle access. Similarly, an Actel Core8051 has 2 separate 8-bit, synchronous data busses with which to interface to other logic (on or off the FPGA).

Actel Core8051 systems leave the definition and implementation of the memory interface and external peripheral bus to the application designer. The amount of work required to create these interfaces depends on the complexity of the application in terms of memory regions and memory mapped peripherals.

The Triscend TE5 8051, RAM, and CSI bus elements are part of the hardwired ASIC portion of the die. A small amount of FPGA is on the chip next to the 8051 system and connected to the CSI bus. This is illustrated in Figure 1.

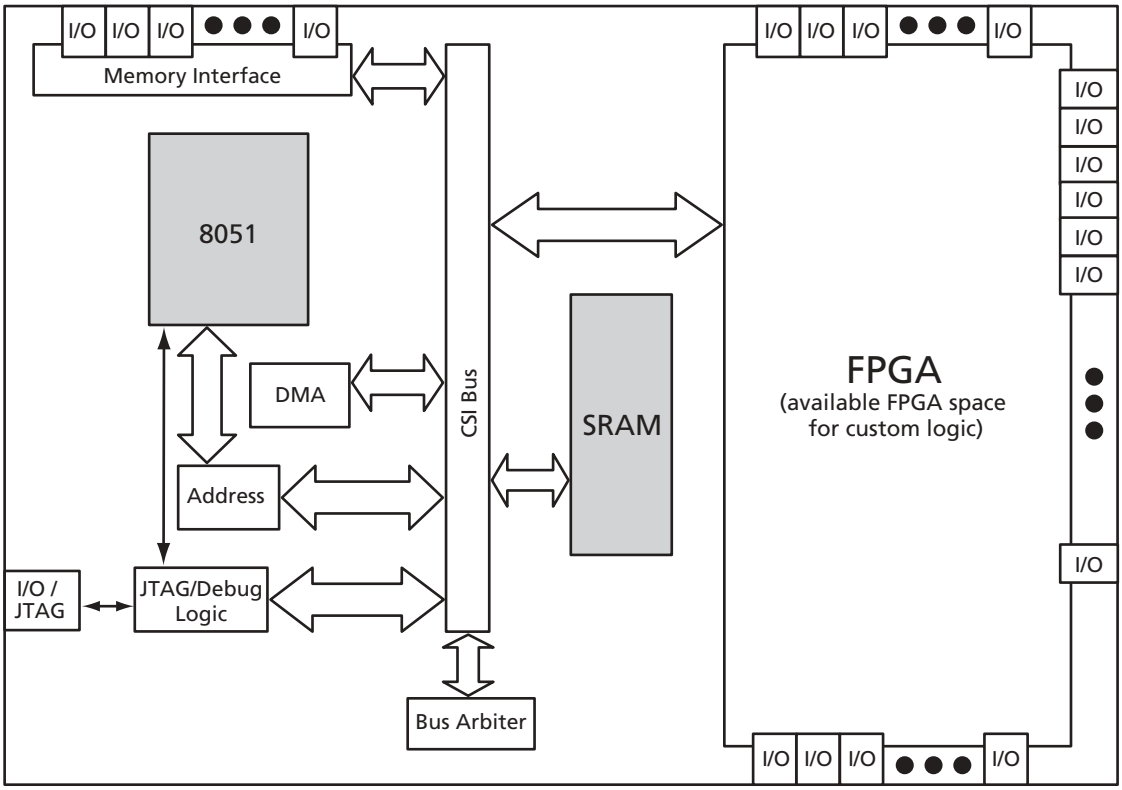

Figure 1 • **Triscend TE5 System Overview**

When working with Core8051, the SRAM and all bus components are constructed in FPGA resources. This is the fundamental difference in design methodology between Triscend and Actel 8051 systems. The Actel Core8051 system is illustrated in Figure 2.

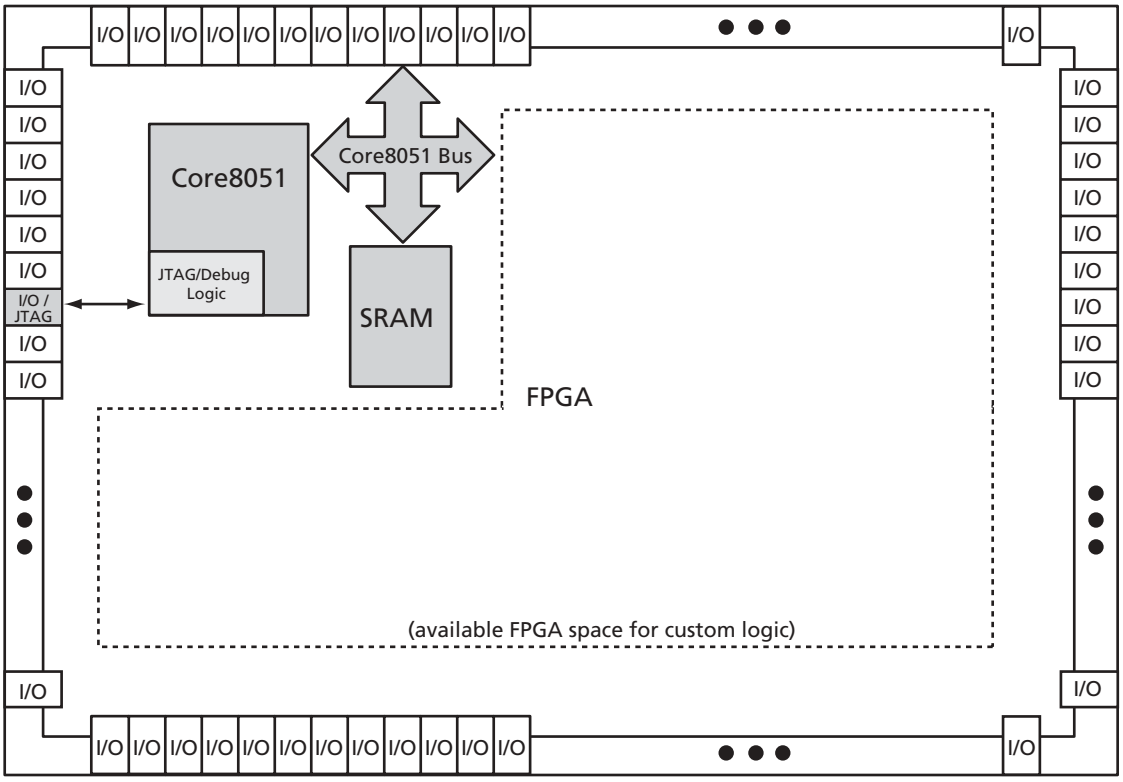

Figure 2 • **Actel Core8051 System Overview**

Software Tools for Hardware Design

Actel Libero IDE

Actel Libero® Integrated Design Environment (IDE) offers the latest and best-in-class tools from leading electronic design automation (EDA) vendors such as Mentor Graphics®, SynaptiCAD™, Synplicity, and our newest partner – Magma® Design Automation. These tools, combined with tools developed by Actel, are integrated into a single FPGA development platform. The Libero IDE flow offers true one-stop shopping for all Actel FPGA development tool needs, including a powerful design manager that guides you through the design process, keeps track of your design files, and seamlessly manages file exchanges between the various tools.

Actel Designer FPGA Implementation Tool

Designer is the premier Actel design implementation software tool suite. After completing design entry and functional verification using Libero IDE or any favorite front-end design tools, simply import the resulting netlist into Designer to complete physical implementation. Designer capabilities include constraints management, place-and-route, timing, power analysis, and programming.

Comparison to Triscend FastChip Tools

FastChip is the layout and design integration tool for the Triscend TE5 FPGA logic. Although FastChip performs the minimally necessary functions, it lacks the sophistication and advanced capabilities of the Actel Libero IDE / Designer tool suite, which includes physical placement and layout controls and sophisticated timing analysis tools. Triscend users must purchase their simulation and synthesis tools separately, while Libero IDE delivers all this and more in one package.

The Actel tools are pure logic design tools and do not have Triscend FastChip memory mapping and 8051 system integration features. This may add some work for very basic applications; however, for advanced applications, designers can take advantage of this freedom to create faster, smaller, cheaper, and/or more versatile designs.

Memory System Design Comparison

- 8 kbytes to 40 kbytes SRAM for Triscend. Up to 198 kbytes in Actel ProASIC^{PLUS} devices (other FPGA families may vary)
- Both the TE5 and Core8051 can run code from internal SRAM, RAM, or ROM in an external chip.

Supported External Memories

Triscend supplies parameters and algorithms to use a variety of memories from several vendors. In an Actel system, the memory interface design is up to the developer. Using powerful Actel software tools, IP, and FPGA fabric, there are virtually no limits to the memory types that can be used with Core8051.

Flash Programming

Flash programming for some vendors and types of Flash is automatically done by Triscend download tools. Actel tools leave Flash programming to the application (not the download tools). An example design on how to do this is available with the *Platform8051 Development Kit*.

Software Tools for 8051 Debug

Both Actel and Triscend systems are compatible with Keil and other common 8051 C compilers and debuggers. Keil tools must be purchased separately in either case. Licenses for the Actel Core8051 come with a free debugger from FS2 software. Both Core8051 and TE5 use standard JTAG hardware ports to connect to on-chip breakpoint and data access circuitry.

There is very little difference in the user interface and features when using the Keil C compiler and debugger with either Core8051 or TE5.

Integrating Custom Peripherals

Core8051 and the Triscend TE5 have very similar interfaces to connect custom FPGA logic to the microcontroller memory space. The primary differences are that Core8051 requires fewer special purpose bus access primitives. Also Core8051 has programmable multi-cycle operation (using the CKCON register) where the TE5 can only do this through hardware control.

A typical Triscend bus peripheral design is illustrated in Figure 3.

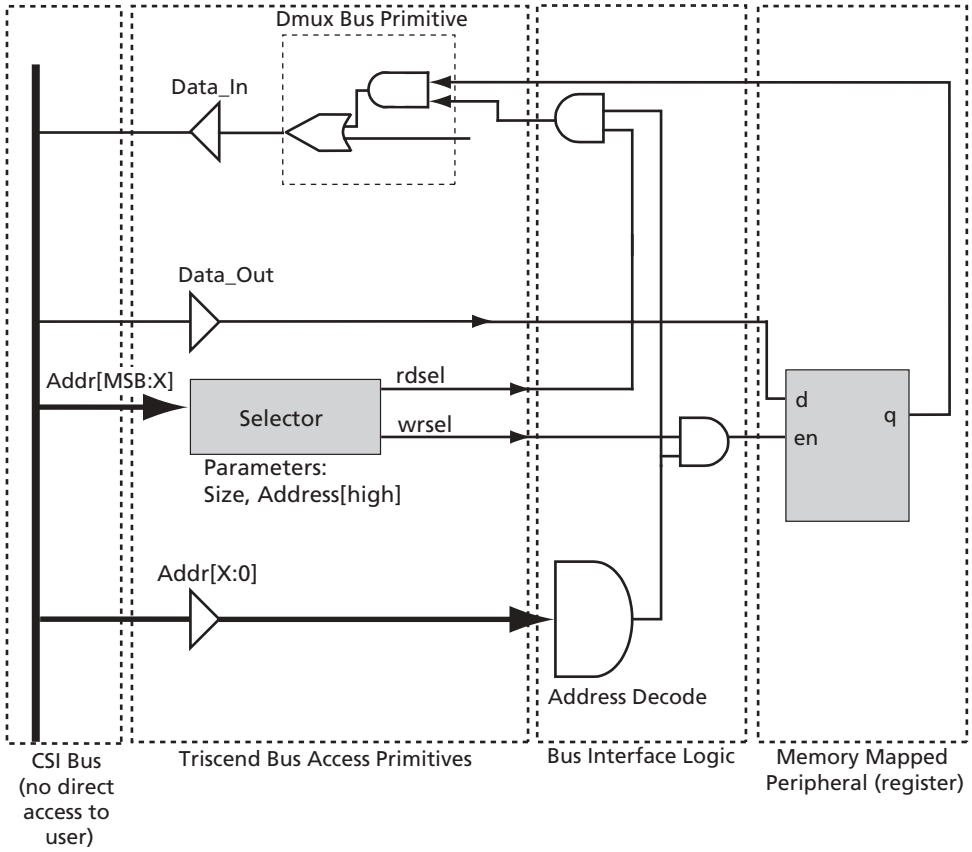

Figure 3 • **Typical Triscend TE5 Custom Logic Implementation**

- In a Triscend design, the bus is hidden from the designer and only the bus access primitives can be used to create a connection. These are not synthesizable and must be instantiated. A small amount of additional address decoding or other bus interface logic is normally needed. Waveforms for typical read and write operations are illustrated in Figure 4.

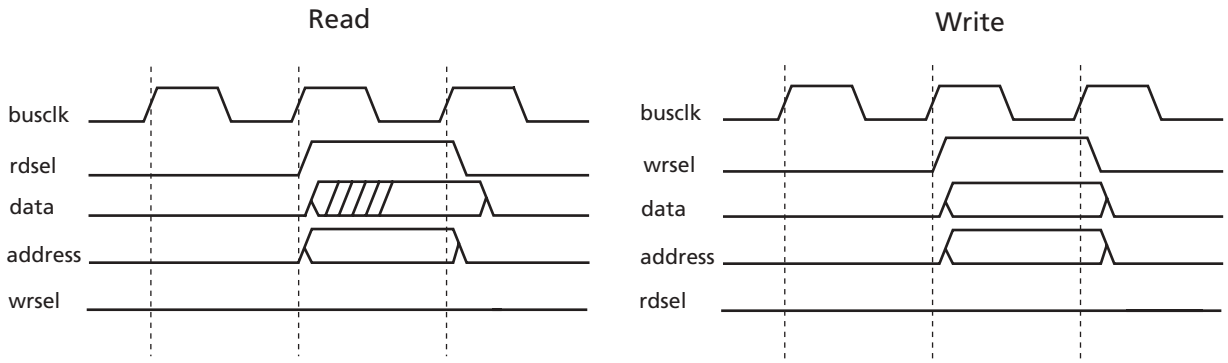

Figure 4 • **Triscend TE5 CSI Bus Read and Write Operations**

In an Actel system, all parts of the system are created from general purpose synthesizable logic components. No special purpose primitives are used. This is illustrated in Figure 5.

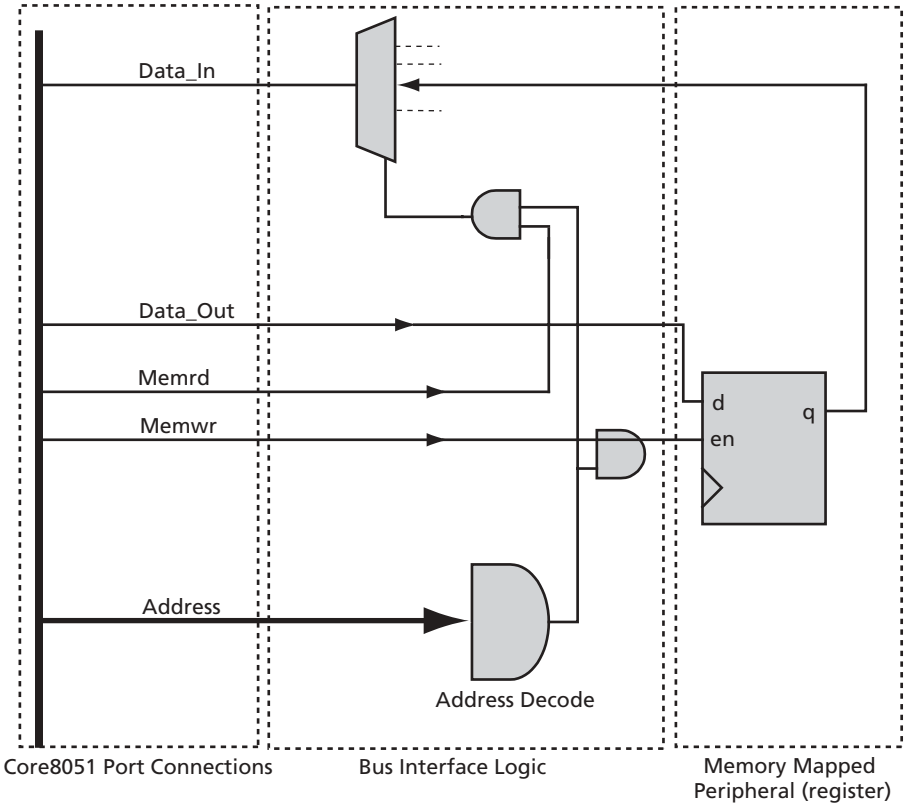

Figure 5 • **Typical Actel Core8051 Custom Logic Implementation**

Corresponding waveforms are shown in Figure 6.

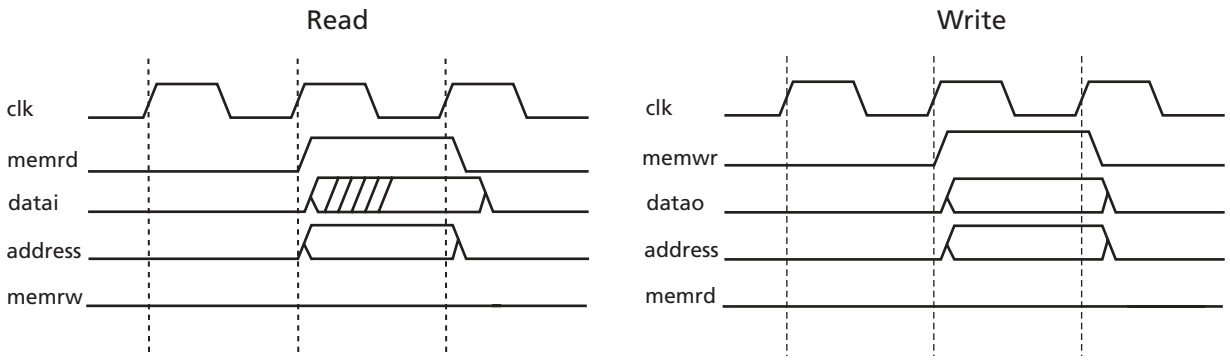

Figure 6 • **Actel Core8051 XDATA Read and Write Operation**

Summary

The Actel Core8051 used with Flash-based FPGA devices makes a very effective and efficient 8051 system. This Core8051 microcontroller solution can be used as a direct replacement for discontinued Triscend devices.

The Actel Core8051 plus Flash FPGA solution offers the following:

- Low cost
- High performance
- Versatility
- Compatibility with 8051 tools
- Cutting edge hardware design tools
- Support for hardware, tools, IP, and sales available

Designers should be aware that the Core8051 solution is not identical to the discontinued Triscend devices. Switching an existing design from Triscend to Actel will require some engineering time and resources. Using the Actel Core8051 may require greater system-level understanding than using the Triscend device. Core8051 has a simple memory bus interface, and it is up to the application designer to expand this interface if connection to complex memories or peripherals is desired.

The Actel Core8051 implemented in Flash-based FPGA devices is an effective replacement for the discontinued Triscend devices. Core8051 offers significant performance improvement, higher flexibility, and a much larger FPGA space with better FPGA tool support. It is an excellent replacement choice for a design that has been implemented with Triscend devices.

Actel Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a website, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Website

You can browse a variety of technical and non-technical information on the Actel home page, at www.actel.com. Actel Intellectual Property documents and information may be found at http://www.actel.com/products/ip/index.html.

Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/support/default.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel website.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call 650.318.4480

From Southeast and Southwest U.S.A., call 650.318.4480

From South Central U.S.A., call 650.318.4434

From Northwest U.S.A., call 650.318.4434

From Canada, call 650.318.4480

From Europe, call 650.318.4252 or +44 (0)1276 401 450

From Japan, call 650.318.4743

From the rest of the world, call 650.318.4743

Fax, from anywhere in the world 650.318.8044

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is likely that we have already answered your questions.

Contacting the Customer Technical Support Center

The highly skilled engineers of the Technical Support Center are available from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center forwards the information to a queue where the first available application engineer receives the data and returns your call. Technical support telephone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460

800.262.1060

Customers needing assistance outside US time zones can either contact technical support via email (tech@actel.com) or contact a local Actel sales office. Sales office listings can be found at www.actel.com/contact/offices/index.html.

Related Documents

Datasheets

Core8051

http://www.actel.com/ipdocs/Core8051_DS.pdf

www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan
www.jp.actel.com

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong
www.actel.com.cn

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488

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