Predicting the Power Dissipation of Actel FPGAs

Introduction

Calculating the power dissipation of field programmable gate arrays (FPGAs) is similar to using the calculations for other CMOS ASIC devices, such as gate arrays and standard cells. The power dissipation depends on such factors as utilization, average operating frequency, and load conditions. In contrast, most PALs and PLDs have a fixed power consumption.

This application note discusses power dissipation and the concept of equivalent power capacitance. The general approach to calculating power in an Actel device will be described using equivalent power capacitance values for the devices. This general equation is useful if internal switching frequencies can be accurately determined. Since this is often difficult to do, a set of approximation curves based on average frequency rules of thumb are provided. The graphs provide an upper limit estimate for active power sufficient for most designs.

General Power Equation

$$P = [I_{CC}\text{standby} + I_{CC}\text{active}] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M \quad (1)$$

Where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL} and I_{OH} are TTL sink/source currents.

V_{OL} and V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

Determining N and M depends on the design and the system I/O. An accurate determination of power dissipation comes from two components, static and active, which are considered separately.

Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. For an ACT 3 device, the standby power is specified as 5 mWatts, worst case.

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mWatts with all outputs driving low and 140 mWatts with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance to PC board traces and load device inputs. An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by the equation:

$$\text{Power } (\mu\text{Watts}) = C_{EQ} * V_{CC}^2 * F \quad (2)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. The results for ACT 1, ACT 2, 1200XL, and ACT 3 devices are given in Table 1.

Table 1 • CEQ Values for Actel FPGAs

	ACT 1	ACT 2	1200XL	ACT 3
Modules	6.3	7.7	7.7	8.2
Input Buffers	16.0	18.0	18.0	1.5
Output Buffers	25.0	25.0	25.0	2.3
Clock Buffer Loads	5.3	2.5	2.5	N/A
I/O Clock Buffer Loads	N/A	N/A	N/A	0.4
Dedicated Array Clock Buffer Loads	N/A	N/A	N/A	0.5
Routed Array Clock Buffer Loads	N/A	N/A	N/A	0.5 + fixed/ device

Finding the active power dissipated from the complete design requires solving Equation 2 for each component type. This requires the switching frequency of each part of the logic. The exact equation is a piecewise linear summation over all components as shown in Equation 3. For ACT 1, ACT 2, and 1200XL devices:

$$\text{Power} = [(m * C_{EQ} * f_m)_{modules} + (n * C_{EQ} * f_n)_{Inputs} + (p * (C_{EQ} + C_L) * f_p)_{Outputs} + (q * C_{EQ} * f_q)_{clk\_loads}] * V_{CC}^2 \quad (3)$$

Where:

m = Number of logic modules switching at frequency f_m

n = Number of input buffers switching at frequency f_n

p = Number of output buffers switching at frequency f_p

q = Number of clock loads on the global clock network

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_q = Frequency of global clock

C_L = Output load capacitance

For ACT 3 devices:

$$\text{Power } (\mu W) = [(m \times 8.2 \times f_1) + (n \times 1.5 \times f_2) + (p \times (2.3 + C_L) \times f_3) + (q \times 0.5 \times f_4) + ((r_1 + 0.5\, r_2) \times f_5) + (s \times 0.4 \times f_6)] \times V_{CC}^2 \quad (4)$$

Where:

m = Number of logic modules switching at f_1

n = Number of input buffers switching at f_2

p = Number of output buffers switching at f_3

q = Number of clock loads on the dedicated array clock network

A1415: q = 104

A1425: q = 160

A1440: q = 288

A1460: q = 432

A14100: q = 697

r_1 = Fixed capacitance due to routed array clock network

A1415: r_1 = 60

A1425: r_1 = 75

A1440: r_1 = 105

A1460: r_1 = 145

A14100: r_1 = 195

r_2 = Number of clock loads on the routed array clock network

s = Number of clock loads on the dedicated I/O clock network

A1415: s = 80

A1425: s = 100

A1440: s = 140

A1460: s = 168

A14100: s = 228

f_1 = Average logic module switching rate in MHz

f_2 = Average input buffer switching rate in MHz

f_3 = Average output buffer switching rate in MHz

f_4 = Average dedicated array clock rate in MHz

f_5 = Average routed array clock rate in MHz

f_6 = Average dedicated I/O clock rate in MHz

C_L = Output load capacitance in pF

Since all of the modules or inputs or outputs do not switch at the same frequency, a weighted average can be used. For example, a design consisting of 100 modules switching at 10 MHz and 200 modules switching at 5 MHz would have a weighted average frequency of:

$$f_{ave} = [(100 * 10) + (200 * 5)]/(100 + 200) = 6.67 \text{ MHz}$$

Determining Average Frequency

Determining the exact average frequency for a design requires a detailed understanding of the data input values to the circuit. Logic simulation can provide insight into average frequency, although simulation is limited by the percentage of real-time stimulus that can be applied. Fortunately, studies based on large numbers of ASIC designs have been made to determine rules of thumb for average switching frequency in logic circuits. These rules are meant to represent worst-case scenarios, hence their use for predicting the upper limits of power dissipation is generally acceptable. The rules given in Tables 2 and 3 are for ACT 1, ACT 2, and 1200XL devices. Table 4 gives the rules for ACT 3 devices. Using these rules, we can develop power estimates.

Table 2 • *Rules for Determining Average Frequency for ACT 1 Family*

1.	Module Utilization = 90%
2.	Average Module Frequency = F/10
3.	1/3 of I/Os are Inputs
4.	Average Input Frequency = F/5
5.	2/3 of I/Os are Outputs
6.	Average Output Frequency = F/10
7.	Clock Net Loading = 45%
8.	Clock Net Frequency = F

Table 3 • *Rules for Determining Average Frequency for ACT 2 and 1200XL Families*

1.	Module Utilization = 80% of combinatorial modules
2.	Average Module Frequency = F/10
3.	1/3 of I/Os are Inputs
4.	Average Input Frequency = F/5
5.	2/3 of I/Os are Outputs
6.	Average Output Frequency = F/10
7.	Clock Net 1 Loading = 40% of sequential modules
8.	Clock Net 1 Frequency = F
9.	Clock Net 2 Loading = 40% of sequential modules
10.	Clock Net 2 Frequency = F/2

Table 4 • *Rules for Determining Average Frequency for ACT 3 Family*

1.	Logic Modules (m)	= 80% of modules
2.	Average module switching rate (f_1)	= F/10
3.	Inputs switching (n)	= # I/Os used/12
4.	Average input switching rate (f_2)	= F
5.	Outputs switching (p)	= # I/Os used/15
6.	Output loading (C_L)	= 35
7.	Average output switching rate (f_3)	= F/2
8.	Dedicated array clock loads (q)	= fixed by device
9.	Average dedicated array switching rate (f_4)	= F
10.	Routed array fixed capacitance (r_1)	= fixed by device
11.	Routed array clock loads (r_2)	= 40% of sequential modules
12.	Average routed array switching rate (f_5)	= F/2
13.	I/O clock loads (s)	= # I/Os used
14.	Average I/O switching rate (f_6)	= F

Average Frequency Example

While some portions of a logic design switch at the system frequency, F, most of the logic switches at a reduced (or divided) frequency. Consider a 16-bit synchronous counter with a system input clock equal to F as shown in Figure 1.

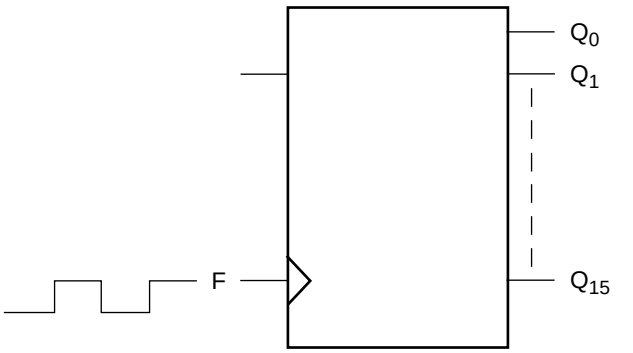

Figure 1 • *16-Bit Synchronous Counter*

Where:

The Q0 output is switching at F/2 (or $1/2^1$),

The Q1 output is switching at F/4 (or $1/2^2$),

The Q15 output is switching at F/65536 (or $1/2^{16}$).

The average frequency is:

$F_{ave} = 1/16 * (1/2^1 + 1/2^2 + \ldots\ldots\ldots 1/2^{16}) \cong F/16$

Thus, the average frequency of an n-bit synchronous counter switching at F MHz is F/n.

Estimated Power

The rules in Tables 2 and 3 are applied to ACT 1, ACT 2, and 1200XL devices. The resulting power components are detailed in Tables 5 and 6, and the total device power is shown in Figures 2 and 3. The graphs provide a simple guideline for estimating power. The tables may be interpolated when your application has different resource utilizations or frequencies. Table 4 details the rules applied to ACT 3 devices.

Table 5 • *Power Components for ACT 1 Family (Watts)*

F (MHz)	Module Power	Input Power	Output Power	Clock Power	Total Power (watts)
A1010					
1	0.005	0.002	0.009	0.019	0.035
2	0.010	0.004	0.017	0.038	0.069
5	0.025	0.009	0.043	0.096	0.173
10	0.051	0.018	0.085	0.192	0.347
15	0.076	0.027	0.128	0.289	0.520
20	0.101	0.036	0.171	0.385	0.693
25	0.126	0.046	0.213	0.481	0.866
A1020					
1	0.009	0.002	0.010	0.035	0.057
2	0.019	0.004	0.021	0.071	0.114
5	0.047	0.011	0.052	0.176	0.286
10	0.094	0.022	0.103	0.353	0.572
15	0.141	0.033	0.155	0.529	0.858
20	0.188	0.044	0.207	0.705	1.144
25	0.235	0.055	0.258	0.882	1.430

Table 6 • *Power Components for ACT 2 and 1200XL Families (Watts)*

F (MHz)	Module Power	Input Power	Output Power	Clock Power	Total Power (watts)
A1280/1280XL					
1	0.011	0.013	0.021	0.027	0.072
2	0.023	0.025	0.042	0.054	0.144
5	0.057	0.063	0.105	0.136	0.360
10	0.113	0.125	0.210	0.272	0.720
20	0.227	0.250	0.419	0.544	1.440
30	0.340	0.375	0.629	0.815	2.159
40	0.453	0.500	0.839	1.087	2.879
A1240/1240XL					
1	0.006	0.009	0.016	0.015	0.046
2	0.013	0.019	0.031	0.030	0.092
5	0.032	0.046	0.078	0.074	0.231
10	0.064	0.093	0156	0.149	0.461
20	0.127	0.186	0.311	0.298	0.923
30	0.191	0.279	0.467	0.447	1.384
40	0.255	0.372	0.623	0.596	1.845
A1225/1225XL					
1	0.004	0.007	0.012	0.009	0.033
2	0.008	0.015	0.025	0.019	0.066
5	0.020	0.037	0.062	0.047	0.166
10	0.040	0.074	0.124	0.094	0.332
20	0.080	0.148	0.249	0.187	0.664
30	0.120	0.222	0.373	0.281	0.996
40	0.160	0.297	0.497	0.375	1.329
50	0.200	0.371	0.621	0.468	1.661

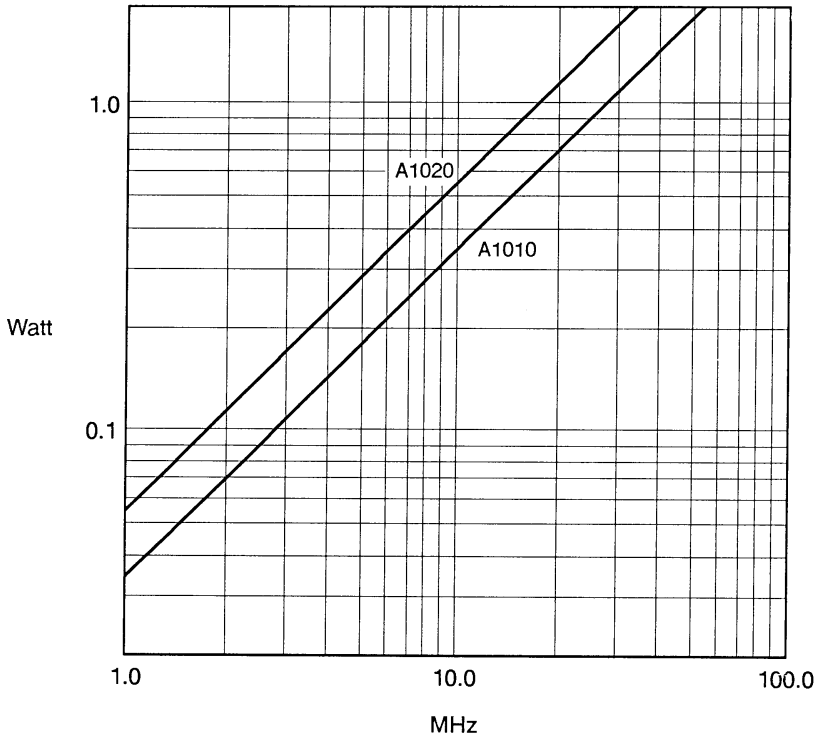

Figure 2 • *ACT 1 Family Power Estimates*

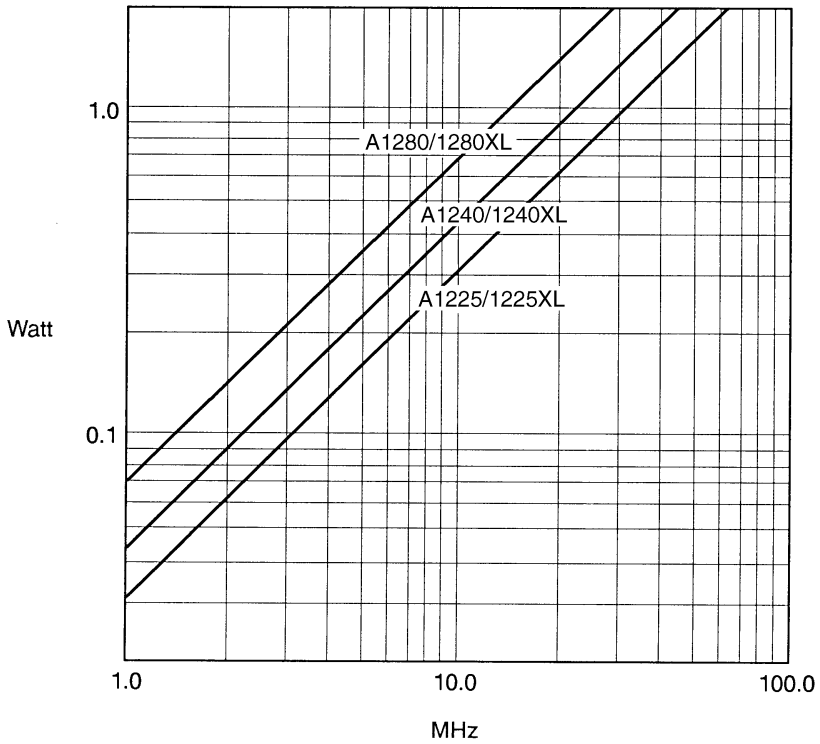

Figure 3 • *ACT 2 and 1200XL Families Power Estimates of Total Power (watts)*