
Internal Power-on Reset and Post Programming Reset Circuit for Flash-Based FPGAs

Table of Contents

Introduction	1
I/Os Behavior at Power-Up/-Down	2
I/Os Behavior During the Programming	2
Design Theory and the Implementation	3
Conclusion	5
Appendix A - Design Files	5
List of Changes	5

Introduction

The state of a system at startup is an important consideration in designing the most of the digital circuits. It is a good practice to provide a mechanism to reset the synchronous circuitry in a known state after the bring-up (power-up and reprogramming cycle). Otherwise, the system may initially operate in an unpredictable fashion because the flip-flops are not designed to power-on in any particular state. For example, in a microprocessor based system, as the potential exists for the processor to execute the runaway code prior to the completion of the initialization sequence. Further, the processors require that the RESET pin is held asserted for a minimum of prescribed clock cycles to fully reset the processor core logic. For example, the RESET pin should be set for a minimum of two clock cycles for Core8051s (Microsemi's high-performance 8-bit Processor IP core) processor to reset the core. Refer to the processor's datasheet for the requirements in relation to the reset circuitry. A power-on reset (POR) circuit insures that the device starts operating from a known state when the power is first applied. The device should be held in reset until the system power supplies are stabilized at the functional levels and the clock is settled. Most of the systems have a dedicated external power management device on the board to generate a reset pulse by monitoring the power supplies output voltage.

In the case of FPGAs, a reset pulse is required at the end of the FPGA in-system programming (ISP) to start the design in a known state and drive the outputs to a known logic state (1 or 0). The post programming reset (PPR) circuit ensures the generation of reset pulse at the end of the ISP.

Microsemi's customizable system-on-chip (cSoC) devices like SmartFusion[®] customizable system-on-chip (cSoC) have an internal reset controller circuit that can be used for generating the reset pulse at the system power-up and at the end of the ISP. However, this application note focuses on Microsemi's Flash-based FPGA system that does not have an internal or dedicated reset controller and implement a simple internal POR/PPR circuit using one FPGA I/O and a few logic tiles. This internal POR/PPR circuit is applicable to all the traditional Flash-based FPGAs like IGLOO, ProASIC3, and Fusion. The same circuit can be used with the SmartFusion cSoC devices, if you do not want to use the internal reset controller.

Note: The proposed POR/PPR circuit generates a reset pulse to the internal FPGA logic when an IGLOO or ProASIC3L device exits from the Flash*Freeze mode. The Flash*Freeze technology used in the IGLOO and ProASIC3L devices enables easy entry and exit from the ultra-low power mode, which consumes as little as 2 μ W, while retaining the SRAM and the register data. If the proposed POR/PPR circuit is used as reset to the whole design, then it resets all the registers data when the device exits from the Flash*Freeze mode. You should use the external POR/PPR circuit, if the application requires the Flash*Freeze mode.

I/Os Behavior at Power-Up/-Down

Microsemi's Flash-based FPGAs support Level 0 live at power-up (LAPU) due to their nonvolatile architecture. Microsemi's low power flash devices use the following main voltage pins during the normal operation:

- "VCC: Voltage supply to the FPGA core
- "VCCIBx: Supply voltage to the I/O bank output buffers and I/O logic. 'Bx' is the I/O bank number.
- "VMVx: Quiet supply voltage to the input buffers of each I/O bank. 'x' is the bank number.

Note: IGLOO nano, IGLOO PLUS, ProASIC3 nano, Fusion and SmartFusion devices do not have VMVx supply pins. On these devices, VMV pins are tied internally with the VCCI pins.

The bank VMVx pin must be tied to the VCCIBx pin of the same bank and therefore, the inputs and outputs are powered up/down at the same time. Therefore, the supplies that need to be powered up/down during the normal operation are VCC and VCCIBx. Unused I/O banks should have their corresponding VCCIBx pins tied to the GND. These power supplies can be powered up/down in any sequence during the normal operation of Flash-based FPGAs. Before the start of power-up, all the I/Os are tristated. The I/Os remain tristated during the power-up until the last supply (being either VCCIBx or VCC) is powered to its functional activation voltage level. After the last supply reaches the functional voltage level, the outputs of the active I/O bank exits the tristate mode and drive the logic at the input of the output buffer. Similarly, the input buffers of the active I/O bank passes the external logic into the FPGA fabric once the last supply reaches its functional voltage level. The behavior of user I/Os is independent of the VCC and VCCIBx power-up sequence or the state of other voltage supplies of the FPGA (VPUMP and VJTAG). Similarly, during the power-down, I/Os in each bank are tristated once the first supply reaches its brownout deactivation voltage. Refer to the respective device datasheet for the recommended functional activation voltages for these supply pins.

After the VCC and VCCIBx reach their minimum functional voltage levels, internally, the following power-up activation sequence takes place:

1. FPGA core gets activated
2. Input buffers get enabled
3. Output buffers are enabled after ~200 ns delay

Approximately, there is 200 ns delay between the input and output buffers activation after the power-up.

I/Os Behavior During the Programming

Microsemi's Flash-based FPGAs are reprogrammable via the JTAG interface either by an on-board resource, such as microprocessor, or by an off-board programmer like FlashPro4 through a header connection. Programming requires the recommended programming supply voltage (VPUMP) and JTAG supply voltage (VJTAG).

During the programming, all the I/O pins, except for JTAG interface pins are tristated and weakly pulled up to VCCI, by default. This isolates the part and prevents the signals from the floating. The default state of the I/O pins during the programming can be changed individually to low, high, last known state, or tristate by selecting the appropriate state in the FlashPro software. Refer to the *Specify I/O States During Programming Tutorial* section in the *FlashPro User's Guide* for more information on the customization of the I/O state during the programming.

With the VCCI and VCC supplies continuously powered up, during the device transitions from the programming to the operating mode, the following activation sequence takes place:

1. Programming sequence
2. Input buffers get enabled
3. Output buffers are enabled after ~1-3 ms delay

Approximately, there is 1-3 ms delay between the input and output buffers activation at the end of the programming.

Design Theory and the Implementation

The delay between the input and output buffers activation after the power-up and the programming prevents the bus contention and glitches on the outputs. The delay between the input and output buffers activation can be used to generate a pulse and it can also be used as reset to the FPGA logic after the device power-up and the programming. This delay provides ample time for the registers in the design to sample the reset signal. The implementation of this POR/PPR circuit requires a general purpose I/O pin configured as a bidirectional buffer and a few core logic tiles, as shown in the Figure 1. The FPGA I/O buffers power sequencing in the Flash-based FPGAs makes it possible to use a BIBUF I/O pad connected to an external weak pull-up resistor to implement an internal reset that triggers both after the power-up and device programming. The FPGA I/O used for generating the reset should be configured as either LVTTTL or LVCMOS standard. The output buffer of BIBUF is configured to always drive low by tying its D input to '0' and Enable (E) input to '1'. The output of input buffer (Y) generates a pulse due to the delay between input and output buffers activation. This POR/PPR circuit implementation generates an active low reset pulse to reset the rest of the design after the power-up and the programming. The Reset generation circuit should be designed depend upon the application specific reset requirements. It is recommended to implement a counter or shift register to increase the reset pulse width.

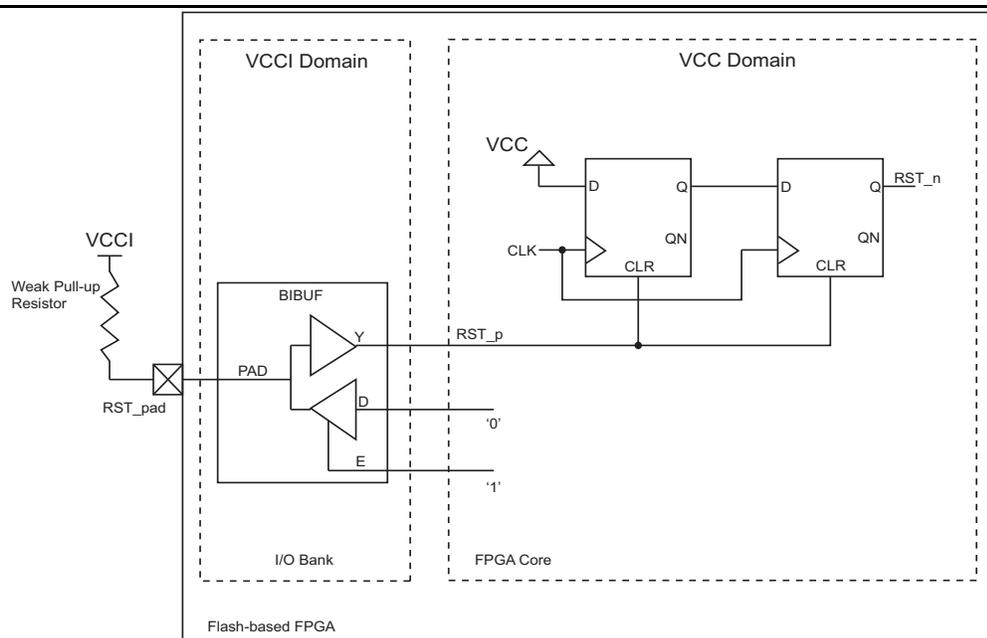


Figure 1 • POR/PPR Circuit Using the BIBUF and External Pull-up Resistor

If the VCC reaches its functional voltage level before the VCCI, then the core first turns on and both the input and output buffers are off. The I/Os are tristated and the core logic detects '1' on the inputs from the boundary scan register (BSR). The RST_p signal is asserted ('1') when the VCC reaches the minimum threshold and the VCCI is lower than the minimum threshold. In this case, the DFFs asynchronous CLEAR input is activated and asserts the RST_n ('0') to reset the internal user logic. When both the VCC and VCCI reaches the min threshold, after the core, the input buffers get turned on first, the pull-up resistor drives the logic high on the RST_p signal. In this case also, the DFFs CLEAR input is high and keeps the internal user logic at reset. About 200 ns later, the output buffers get turned on which then drives the RST_p signal low, releases the system from the reset by de-asserting the RST_n ('1'). This RST_n pulse acts as a power on reset.

Similarly, after the programming, there is a delay of about 1-3 ms between the input and output buffers activation. So after the programming, the same circuit drives the RST_n signal to low (active) for 1-3 ms and then to high (de-active), acts as PPR.

The reset pulse (RST_n) duration can be increased by placing a counter. Figure 2 shows a pulse generated for the duration of 64 μs using a counter that starts counting from a known state set by the reset generated from the POR/PPR circuit. The generated pulse can be used as reset pulse for the rest of the logic in the fabric. Refer to "Appendix A - Design Files" on page 5 for more information on the design used for the POR/PPR circuit validation. The value of the external weak pull-up resistor must be in the range of 10 $\text{k}\Omega$ to 100 $\text{k}\Omega$ depending on the noise on the board. There is some static current flowing from V_{CCI} after POR/PPR occurred and it is equal to $V_{CCI}/R_{\text{pull-up}}$.



Figure 2 • Pulse Generated Due to Reset from the POR or PPR Circuit

As shown in Figure 3, the reset pulse generated by the proposed POR/PPR circuit can be taken on an I/O pad to reset the board components after the power-up and the programming. An external pull-down resistor should be connected on this I/O pad to avoid the glitch during the power-up time. The I/O state during the programming should be set to low to keep external components in reset during the programming.

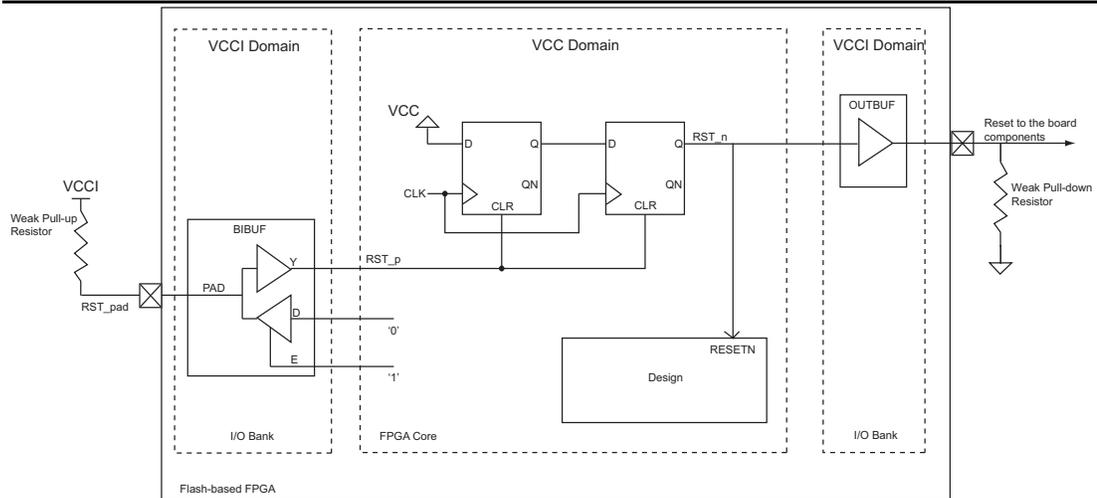


Figure 3 • POR/PPR Signal to Board Components

Conclusion

This application note shows an implementation of an internal POR and PPR circuit using one FPGA I/O and a few core logic tiles. For Microsemi's Flash FPGA-based systems that include a soft microprocessor without any dedicated reset management circuitry, the POR/PPR circuit described in this application note is sufficient to prevent the execution of runaway code or other system initialization issues after the power-up and the programming.

Appendix A - Design Files

You can download the design files for the POR/PPR circuit validation from the Microsemi SoC Products Group website:

www.microsemi.com/soc/download/rsc/?f=LPF_AC380_DF.

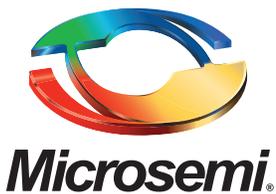
The design file consists of Libero SoC project for IGLOO AGL1000 device. It can be modified for any other Microsemi Flash-based FPGAs. Refer to the *Libero SoC Quick Start Guide* for more information on the Microsemi SoC Products Group SoC development flow using the Libero SoC design software.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 1 (February 2012)	Removed ".zip" extension in the link (SAR 36763).	5

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*



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