ProASIC and ProASIC^PLUS Design-Flow Migration to Designer v5.0

Introduction

In Designer v5.0, existing Flash users see slightly different default behavior than previous Designer releases.

The affected flows for Flash users in Designer v5.0, which are highlighted below, include:

These infrastructure changes provide a more stable base for Actel Flash device software support.

Import Source Files Dialog

There has been no change in the types of source files that you can bring into Designer software. Source files include your netlist and constraint files.

Table 1 • **Types of Source Files That You Can Import**

Source Files	File Type Extension
EDIF Files	*.ed*
Verilog Files	*.v*
VHDL Files	*.vhd*
ProASIC Constraint Files	*.gcf

There is a new check box in the "Import Source Files" GUI that you can select to keep existing physical constraints (i.e. fixed and initial placement, routing, region assignments and other placement constraints). See Figure 1 on page 2.

The "Keep existing physical constraints" check box is checked by default. Selecting this box preserves all existing physical constraints that you have previously entered using the GCF file or the MultiView Navigator tools—PinEditor, ChipPlanner, or the I/O Attribute Editor. If you re-import a GCF file with this check box selected, Designer tries to merge existing physical constraints already in the design database with the physical constraints in the user-defined GCF file. If you do not wish to merge the constraints, uncheck this box. Designer then flushes all existing physical constraints once source files are imported again.

For more information and details on this "Keep existing physical constraints" check box and user flows, please refer to the document *Keeping Existing Physical Constraints*.

Opening Existing Designs

Reopening existing ADB files generated with previous versions of Designer software triggers a convert process. This convert process can take some time (up to a few minutes). It is depicted by the turning hourglass icon in the bottom right-hand corner of Designer GUI. Once the ADB has been saved in Designer v5.0, files will open more quickly.

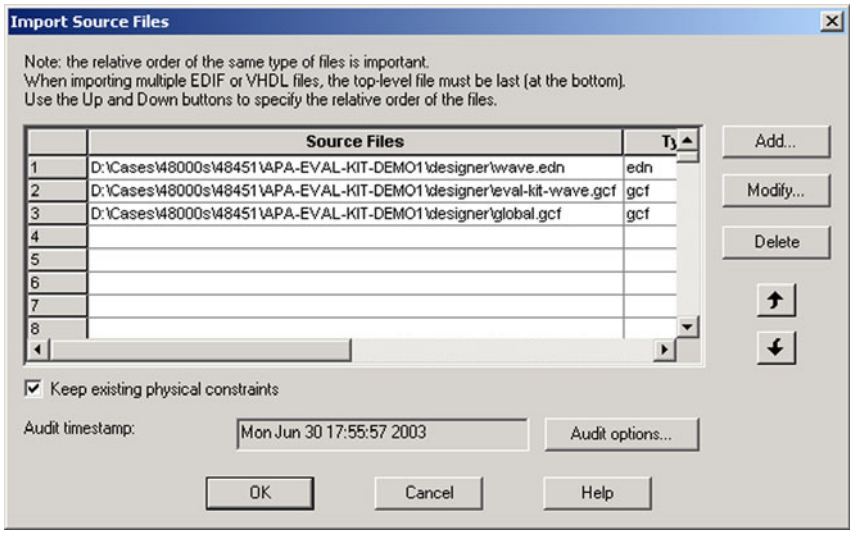

Figure 1 • **Import Source Files Dialog Box**

Incremental Design Flow Support (ECO Mode)

Designer v5.0 now supports incremental or ECO design flow (i.e. modifying the netlist or adding some new constraints). This is supported by the check box in the "Import Source Files" dialog box for "Keep existing physical constraints" (see "Import Source Files Dialog" on page 1).

NMAT (Netlist Name Matching)

To support incremental design flow/ECO mode, Designer v5.0 uses the netlist name matching (NMAT) method of preserving user data (such as constraints, I/O attributes, placement information, etc.) when a user recompiles with a modified netlist. Any user data that applies to both netlist is preserved, while any constraints referring to non-existing instances are ignored.

New Checks In Compile

Compile has implemented stricter design rules. As a result, you can expect new failures if you have any conflicting "set_io" constraints. Previously, if there was a conflict between two fixed placements for the same I/O, Designer used the last placement listed in the constraints file. In Designer v5.0, the same condition results in an error message, and you must modify the constraints file manually to remove any duplicate fixed assignments.

Designer uses the following rules to handle conflicting constraints:

1. A conflict between two fixed (i.e. "set") placements results in an error, except when a core instance is moved from one fixed location to a new fixed location. In this case, the previous fixed location stored in the database prevails and Designer generates a warning.
2. A fixed (i.e. "set") constraint always overrides an initial (i.e. "set_initial") constraint on the same instance. Designer returns a warning every time this conflict is encountered for I/O instances, but no warnings are returned for core instances and RAMs.
3. An existing initial (i.e. "set_initial") placement that is preserved in the design database is not overwritten by a new initial placement entered in a user-defined GCF. Instead, to give a new initial placement, use ChipPlanner, or flush the existing physical constraints when you import a GCF by de-selecting the "Keep existing physical constraints" box in the Import Source Files Dialog.

The Compile component generates an internal database for Flash families to communicate with Designer auxiliary tools. At the end of Compile, this internal database is synchronized. Some warnings may be displayed during this internal update, although Compile succeeded without warnings and errors. The Layout tool ignores all the constraint warnings during this internal update.

Layout / Timing / SmartPower

There have been no flow changes to these tools.

MultiView Navigator – ChipPlanner (new graphical floorplanning tool)

MultiView Navigator is Actel's new graphical floorplanning tool for the Flash (ProASIC and ProASIC^{PLUS}) families. ChipPlanner replaces the previous ChipView; it is a new chip design viewing and editing tool.

ChipPlanner support and limitations are:

- You can VIEW and EDIT the following placement constraints
  - I/O placements
  - Core placements
  - Region assignments (excluding RAM and global I/Os)
  - Empty region assignments (excluding RAM and global I/Os)
- You can VIEW, but not edit
  - Spine assignments
- You cannot VIEW or EDIT
  - Timing constraints
  - Optimization constraints
  - Control of globals

In addition, there are certain limitations in region creation for A500K/APA in the MultiView Navigator tool:

- Regions created in ChipPlanner cannot extend over RAMs and global I/Os
- You cannot create exclusive regions
- You cannot create an empty region over RAMs or globals

To enable routing display (as in the previous version of ChipView):

1. Invoke ChipPlanner for post-Layout design
2. Navigate to the Nets tab. Check that the "Nets" toolbar is shown (or menu View > Toolbars > Nets). Check that the "Show Routes" selection is on (Figure 2).

Figure 2 • **"Nets" Toolbar in MultiView Navigator**

3. In the "Hierarchy" window, click any net.
4. To display routing, press Control-A to select all (or Menu > Edit > Select All).

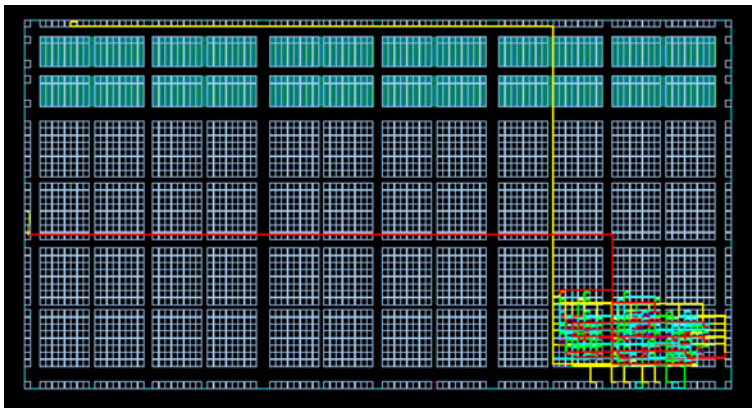

Figure 3 • **Routing Display in ChipPlanner**

Floorplan.gcf

In Designer v5.0, there is a new internal file called floorplan.gcf that takes the place of the last_placement.gcf file in previous versions of Designer. The layout of this file and its various sections is same as the exported GCF. To fix the layout of a design, do not use floorplan.gcf. Instead, follow the "Manual Placement Flow" on page 5 in this document.

Export GCF File Options

In Designer v5.0, there are now three options available to users when exporting constraint files. To export a constraint file, go to menu File > Export > Constraint Files. If the GCF files option is selected, a new window appears and asks for the type of constraints that should be exported. There are three options available to you when exporting GCF files:

1. Pin locations (This replaces the old option of exporting a pin-map GCF file)

   This option exports the set_io, set_initial_io and set_empty_io constraints.

2. Placement constraints

   This option exports all the layout constraints that are saved in the internal database. This includes the initial and fixed placements for I/O, location and region.

3. All GCF constraints

   This option exports all the GCF constraints. This includes the layout constraints saved in the internal database plus those constraints provided by the user that are not saved in the internal database. This includes initial and fixed placements for I/O, location, and region, as well as user-defined timing and optimization constraints (Figure 4).

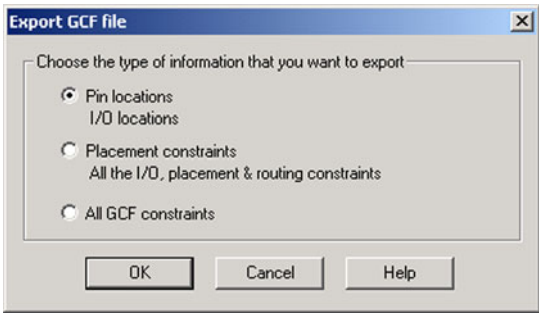

Figure 4 • **Export GCF File Dialog Box**

Note that the content of the exported GCF file varies according to the design state. For example, in the post-compile state, the exported GCF file only includes user-defined constraints. Post-layout, the GCF file includes all the layout information (if you select the appropriate option in the Export GCF file dialog box).

The exported GCF file contains four sections:

1. I/O constraints
2. Core cell constraints
3. Region constraints
4. Empty constraints

Script Options

The new export GCF options are supported in TCL scripts via the "-gcf_option" parameter. The following TCL commands are available for exporting GCF files from a TCL script:

1. Pin Locations

   ```
   export -format "GCF" -gcf_option "ios"{filename.gcf}
   ```

2. Placement Constraints

   ```
   export -format "GCF" -gcf_option "placement"{filename.gcf}
   ```

3. All GCF Constraints

   ```
   export -format "GCF" -gcf_option "all"{filename.gcf}
   ```

   ```
   If no -gcf_option parameter is provided, Designer exports the Pin Locations. This is backward compatible with the export GCF command in Designer R1-2003 and earlier releases.
   ```

Manual Placement Flow

In Designer v5.0, instead of using last_placement.gcf for manually fixing your layout for iterative design changes, export a GCF file and select the second option—Placement constraints: All the I/O, placement-and-routing constraints. Using this exported GCF file, you can globally replace all "set_initial" constraints to "set" and re-import this file as a source file along with your netlist in a new design session.

Reference Material

- *Designer Online Help*: Can be invoked from Designer software
- *Designer User's Guide*: *http://www.actel.com/documents/designer_UG.pdf*

http://www.actel.com

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