I/O Features in Axcelerator® Family Devices

Introduction and Feature Summary

The Axcelerator family offers I/O features to support a very wide variety of user designs. An outline of the features is as follows:

- Support for multiple I/O specifications
- Mixed-voltage operation – 1.5 V, 1.8 V, 2.5 V, 3.3 V
- Bank-Selectable I/Os – 8 banks per chip
- Registered I/O
- Double Data Rate (DDR) Operation
- Hot-Swap Compliant I/Os
- Programmable Slew Rate, Output Drive, and Input Delay
- Integrated Pull-Up and Pull-Down Circuits
- Boundary-Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)

A separate *Axcelerator I/O Selection Guide* gives an overview of the supported standards and features as well as performance information. This document provides details on configuration of the various basic I/O options.

Selecting Axcelerator I/Os

The following three steps summarize the configuration of Axcelerator I/O structures:

1. Select the **Default I/O Standard** in Actel's Designer software Device Selection Wizard (Figure 1).
2. Use SmartGen to configure I/Os by generating specific library cores.
3. Use Designer's I/O Attribute Editor to change characteristics of individual I/Os.

The options available in choices 2 and 3 are described in greater detail in the next section.

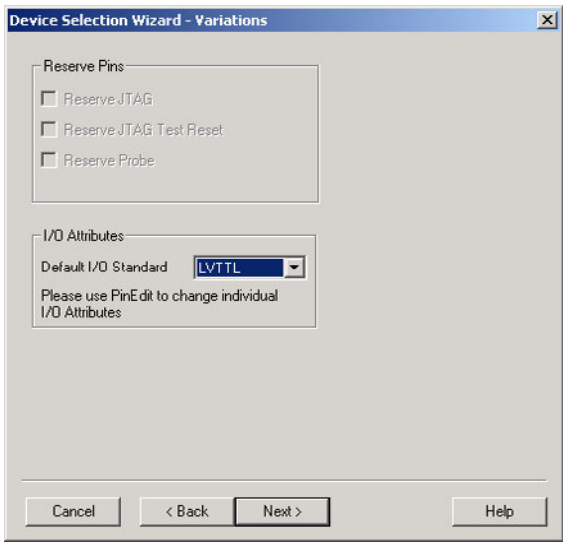

Figure 1 • **Default I/O Standard Selection in Designer**

Using SmartGen for I/O Configuration

The SmartGen tool in the Actel Libero® Integrated Design Environment (IDE) and Designer tool suites provides a GUI-based method of configuring I/Os. The first step is configuring SmartGen. You must create a workspace to generate a core in SmartGen.

A workspace defines your family and the default directory in which you save your configured cores. You can also save your workspace in a different directory. The workspace is a logical grouping for your cores; each workspace contains cores for a specific product family.

To create a workspace:

1. Start **SmartGen**. Then choose to **Create a Workspace** or **Open an Existing Workspace**, as shown in Figure 2.

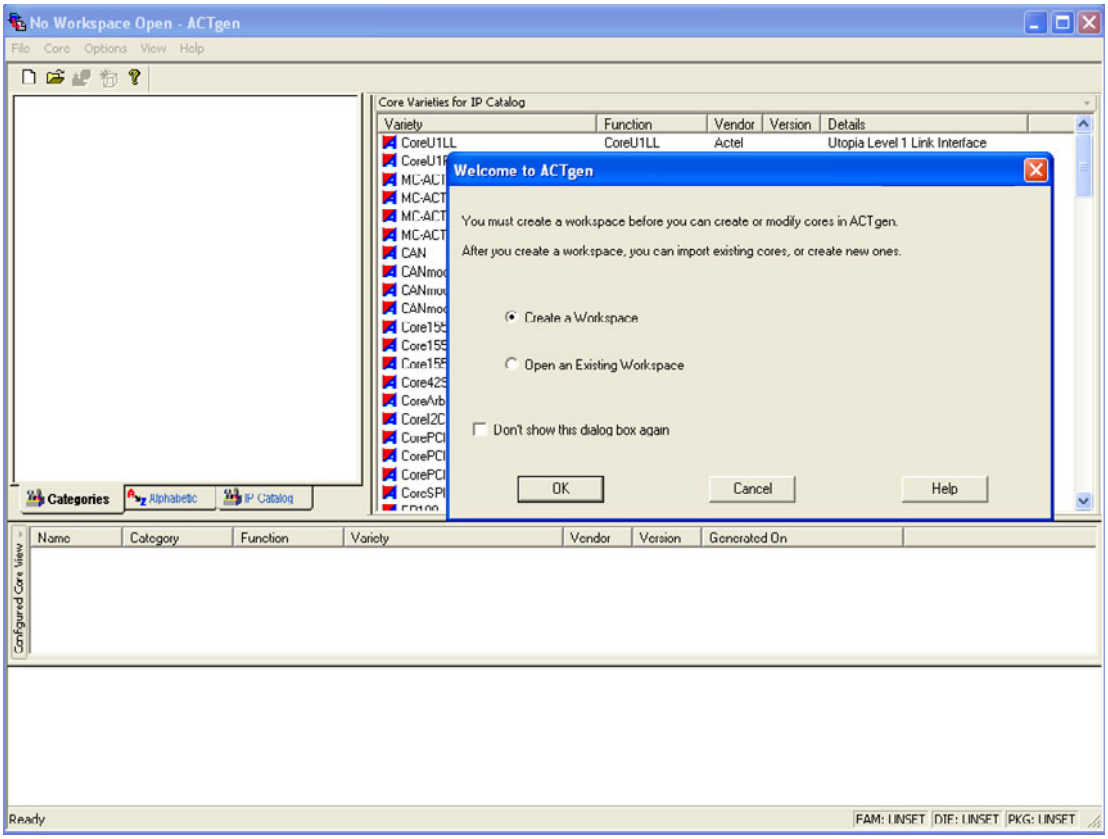

Figure 2 • **Invoking SmartGen**

2. Select **Create a Workspace**, and click **OK**.
3. Specify the **Workspace Name**, **Workspace Location** (click the **Browse** button to navigate to an existing directory or create a directory), **Family** as Axcelerator, and **Netlist** format.
4. Click the **I/O** icon in the **Categories** tab and expand it.

   Now there are five configuration options (Figure 3): Double-Data Rate (DDR), Input Buffers, Output Buffers, Bidirectional Buffers, and Tristate Buffers.
5. Select any of the options. The Variety View Window displays the list of configurable cores.

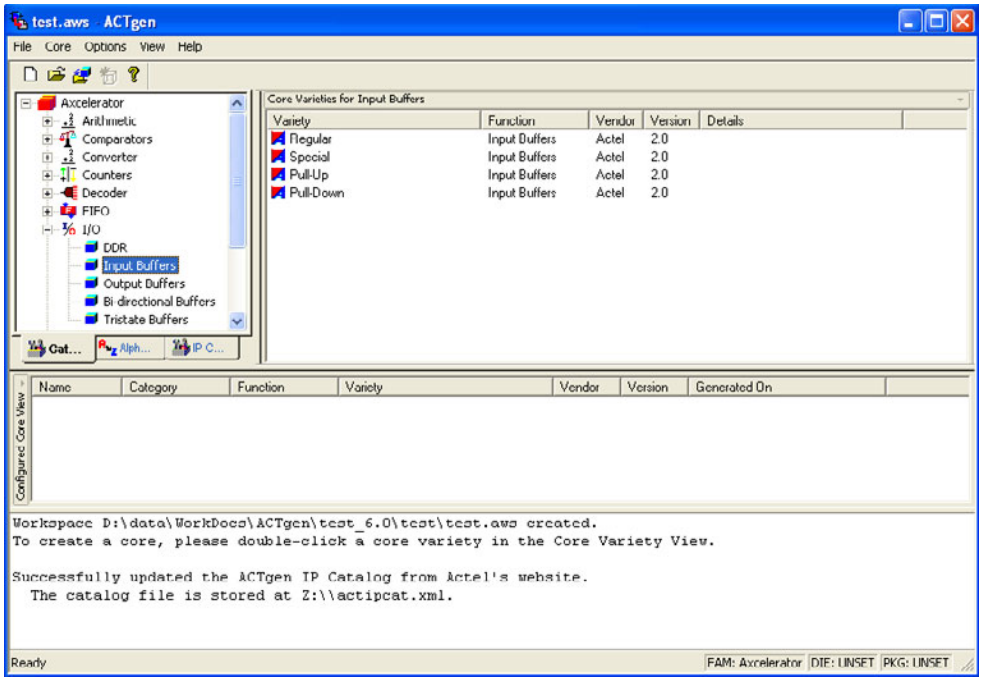

Figure 3 • **Selecting the I/O Macro**

Input Buffers

The Input Buffer is configured using the following options:

1. Double click any of the core varieties for Input Buffers from the Variety View Window (Figure 4). The I/O: Create Core dialog box opens with the Input Buffers tab selected (Figure 5).

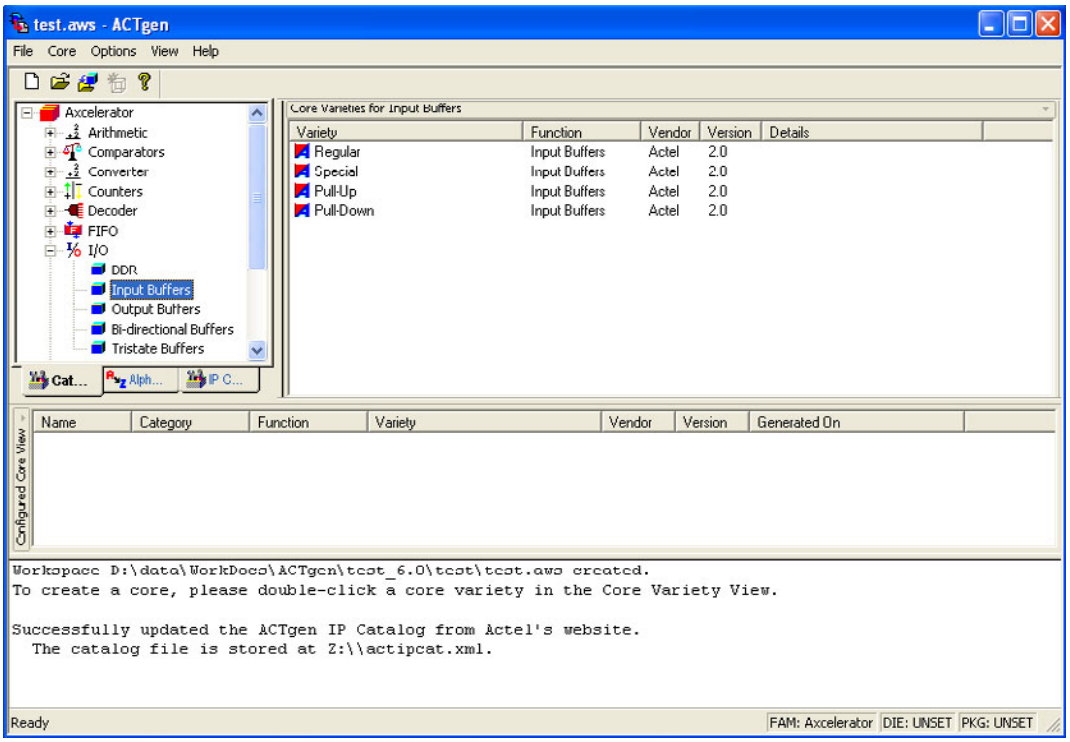

Figure 4 • **I/O Options**

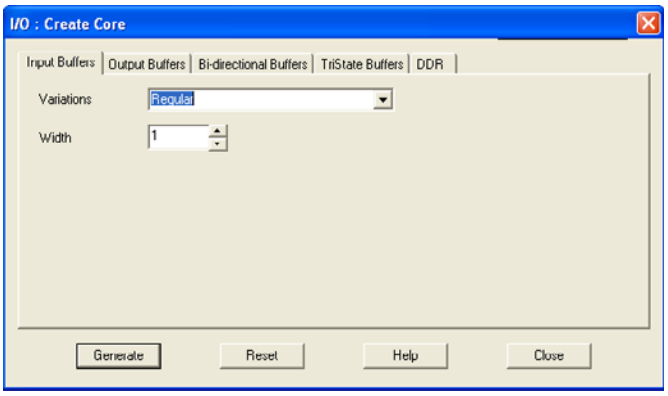

Figure 5 • **I/O: Create Core Dialog Box**

2. Choose one of the Variations: **Regular** or **Special**.
   The Regular variation has only one option (choosing width 1 (default) to 99).
   The Special variation has following additional options (Figure 6):
   – Technology LVCMOS15 (1.5 V LVCMO default), LVCMOS18 (1.8 V LVCMOS), LVCMOS25 (2.5 V LVCMOS), PCI, PCI-X, GTLP25 (GTL+ 2.5 V), GTLP33 (GTL+ 3.3 V), HSTL_I, HSTL_II, SSTL3_I, SSTL3_II, SSTL2_I, SSTL2_II
   – Voltage level: Various voltage levels are available with respect to different I/O technologies.
   – Resistor: Includes weak pull-up and pull-down resistor options.
3. Click **Generate**. You must enter a file name and select the file format: EDIF, VHDL, VERILOG, or ADL.

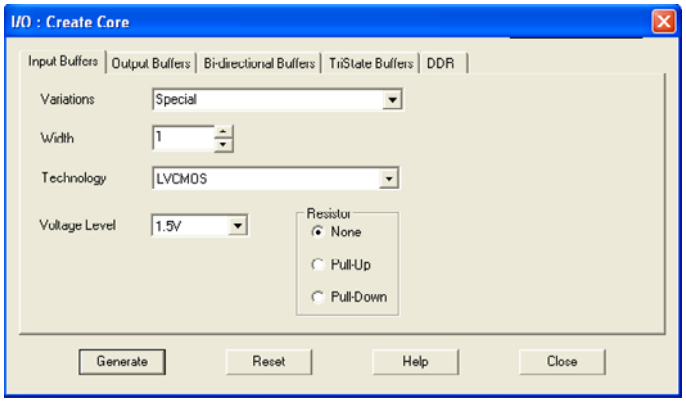

Figure 6 • **Output Buffer Selection**

Output Buffers

Configuring the Output Buffer is very similar to the Input Buffer:

1. Select the **Output Buffers** tab (Figure 7).

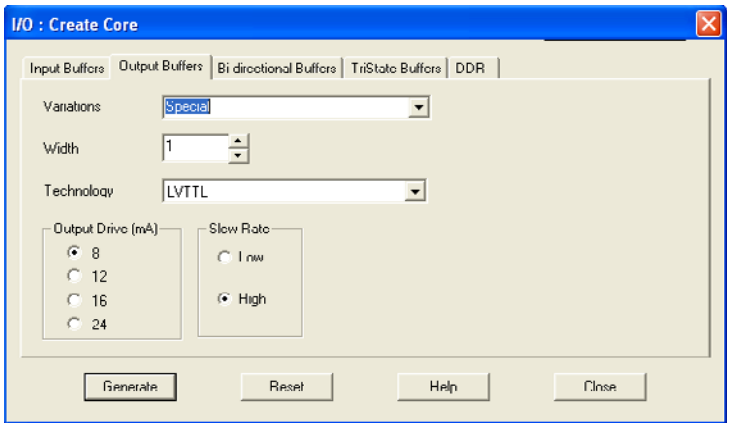

Figure 7 • **Output Buffer Selection**

2. Choose one of the Variations – **Regular** or **Special**.
3. Choose Width – 1 (default) to 99.
4. If the Special Variation is selected, the following options will be available depending on the technology (Figure 8):
   – Select the Output Drive – 8 mA (default), 12 mA, 16 mA, 24 mA
   – Select the Slew Rate – Low or High (default)
5. Select **Generate**. You must enter a file name and select the file format: EDIF, VHDL, VERILOG, or ADL.

Bidirectional Buffers and Tristate Buffers

The Bidirectional and Tristate Buffers have identical configuration options.

1. Select the **Bidirectional Buffers** or **Tristate Buffers** tab (Figure 8).

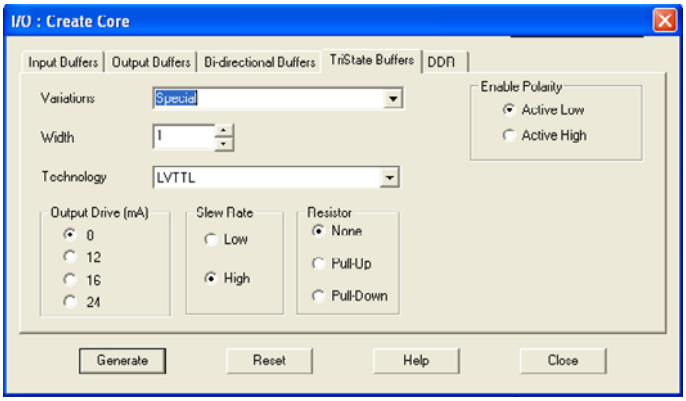

Figure 8 • **Tristate Buffer Selection**

2. Choose one of the Variations (see below).
3. Choose **Width** – 1 (default) to 99.
4. Select **Enable Polarity** – Active Low (default) or Active High.
5. If the Special variation is selected, the following options will be available depending on the technology:
   – Select Output Drive – 8 mA, 12 mA, 16 mA, 24 mA (default)
   – Select Slew Rate – Low or High (default)
6. Select **Generate**. You must enter a file name and select the file format: EDIF, VHDL, VERILOG, or ADL.

Double Data Rate (DDR) Input

For DDR inputs, two variations are available: DDR with regular Input Buffers and DDR with special Input Buffers. Select either of them and generate the DDR Input Buffer core.

Using I/O Attribute Editor for I/O Configuration

Even though it is very efficient to select I/O characteristics for a bus using SmartGen, many of the I/O options can also be selected in a GUI-based fashion using the I/O Attribute Editor. Click **I/O Attribute Editor** under MultiView Navigator to open the tool (Figure 9). Figure 10 on page 8 shows the I/O Attribute Editor. The I/O configuration options are given below:

- Pin number
- Locked (lock and unlock assigned attribute)
- I/O standard
- Output drive mA
- Slew
- Resistor pull
- Input delay
- Output load
- Use the I/O register
- Hot-swappable

The choices for each option are given in the following subsections.

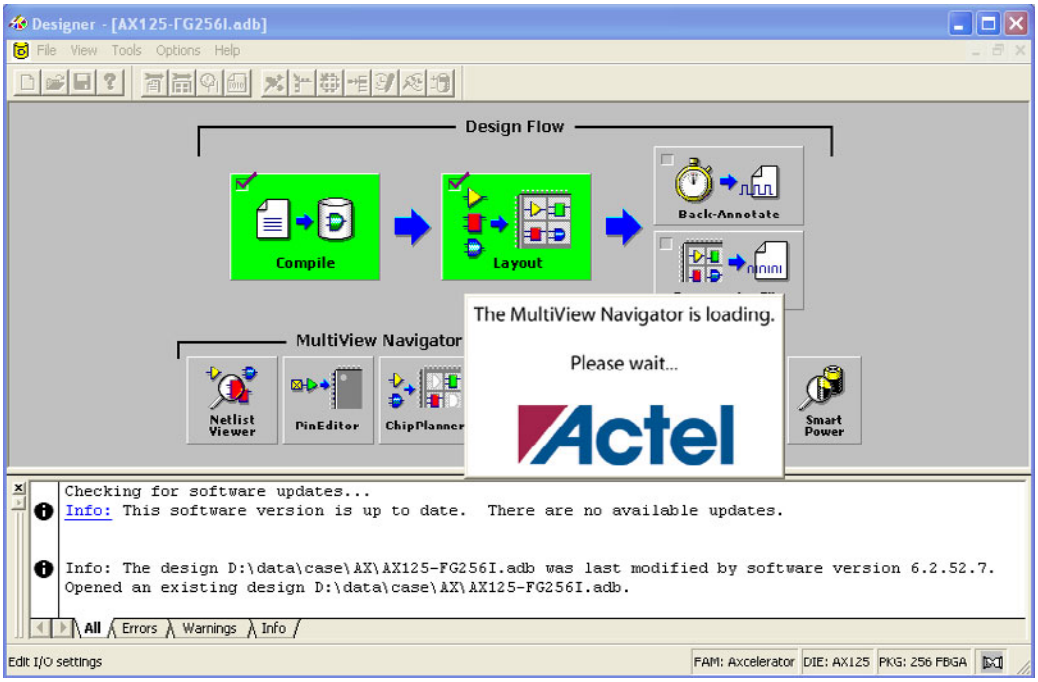

Figure 9 • **I/O Attribute Editor**

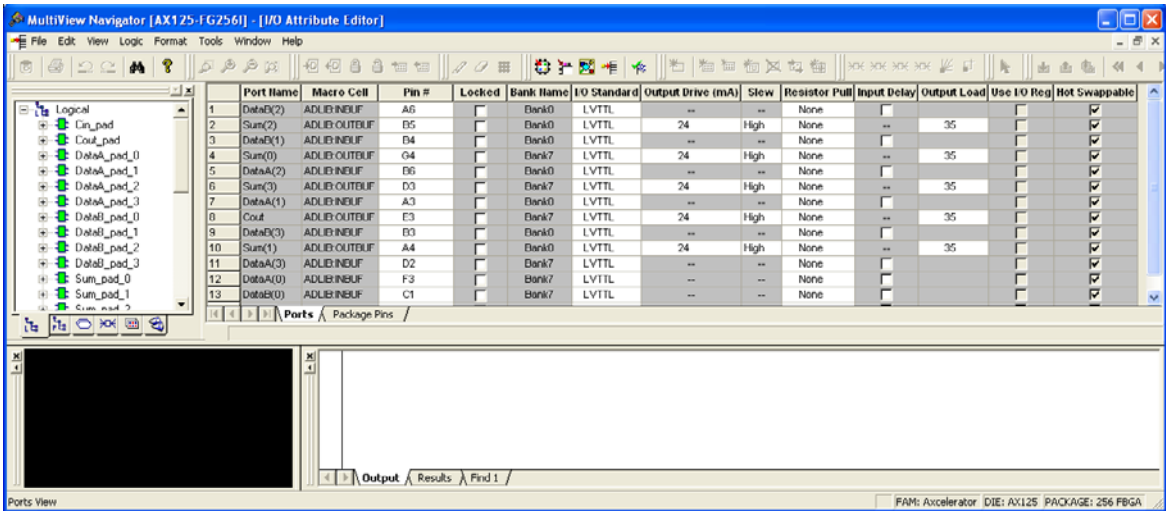

Figure 10 • **I/O Attribute Editor**

Pin Number

You can assign the pin number to your signal from a drop-down list. If there is no conflict, your pin number selection is implemented.

Locked

This option is to lock and unlock and assign attributes for a pin.

I/O Standard

The choices depend on compatibility of I/O standards within a given bank. If SmartGen has generated cores associated with several pins in a bank, the pins must be compatible types. Note that only single-ended standards are acceptable here. In addition, SmartGen's choices for compatibility are only those which are independent of V_{REF} (Table 1). Choices dependent upon V_{REF} are omitted.

Table 1 • **Single-Ended I/O Compatibility Matrix**

	LVTTL 3.3 V	LVCMOS 2.5 V	LVCMOS 1.8 V	LVMCOS 1.5 V	3.3 V PCI/PCI-X	GTL+ 3.3 V	GTL+ 2.5 V	HSTL I	SSTL2 I and II	SSTL3 I and II
LVTTL 3.3 V	✓				✓					
LVCMOS 2.5 V		✓								
LVCMOS 1.8 V			✓							
LVCMOS 1.5 V				✓				✓		
3.3 V PCI/PCI-X	✓				✓					
GTL+ 3.3 V	✓				✓	✓				
GTL+ 2.5 V		✓					✓			
HSTL I				✓				✓		
SSTL2 I and II		✓							✓	
SSTL3 I and II	✓				✓					✓

Output Drive mA

Here the choices correspond to selections in SmartGen although the nomenclature is different. The choice list is as follows:

- 8 mA (x1 in SmartGen)
- 12 mA (x2)
- 16 mA (x3)
- 24 mA (x4)

Slew

Choices are High and Low, as in SmartGen.

Resistor Pull

This option allows inclusion of a weak resistor for either pull-up or pull-down of the input buffer. The choices are None, Up (Pull-Up), or Down (Pull-Down). Again, these choices are all available in SmartGen.

Input Delay

A programmable input delay element is associated with each I/O bank. The delay is programmable in steps from approximately 0.54 ns to 3.41 ns. The delay can be switched in and out for each input buffer in I/O Attribute Editor by checking the associated box. If the input register is selected (refer to the "Use Register" section below), the delay element is activated (i.e., the box is checked) by default. You can override this default setting. The input delay selection is not included in SmartGen.

Use Register

The input and output registers for each individual I/O can be activated by checking the box associated with an I/O. The I/O registers are NOT selected by default.

Output Load

The user can enter a capacitive load as an integral number of picofarads. 35 pF is the default. This option is not available in SmartGen.

Hot Swappable

This box indicates whether or not the I/O is hot swappable. If checked (all standards except PCI and PCI-X), a clamp diode is NOT included to allow proper hot-swap behavior. If not checked (PCI and PCI-X only), the clamp diode is included as required by those specifications, but the I/O is NOT hot swappable.

Assigning Technologies and V_{REF} to I/O Banks

The Axcelerator family offers a wide variety of I/O standards, including voltage-referenced standards. These voltage-referenced standards require the use of a reference voltage (V_{REF}).

V_{REF} Usage Rules

V_{REF} must have a common voltage for an entire I/O bank; its location is user-selectable within the bank. When deciding on the location of the V_{REF} pin, the following information must be taken into account:

- Any pin that is assigned as a V_{REF} can control a maximum of eight user I/O pad locations in each direction (16 total maximum) within the same I/O bank.
- I/O package locations listed as No Connects (NC) are counted as part of the 16 maximum.
- Dedicated I/O pins (GND, V_{CCI}) are not counted as part of the 16.
- The two user I/O pads immediately adjacent on either side of the V_{REF} pin (total of four pads) may only be used as inputs. This means outputs, BIBUF, and TRIBUF I/Os, cannot be placed at these four locations. The exception is when there is a V_{CCI}/GND pair separating the V_{REF} pin and the user I/O pad location.

Manually Assigning Technologies to I/O Banks

1. Select an I/O bank in either ChipPlanner or PinEditor (from GUI).
2. From the **Edit** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select the technologies, and click **Apply**.

   Selecting a standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same V_{CCI}. Further, selecting GTLP (3.3V) disables SSTL3 as an option because the V_{REF} of the two are not the same. After you click **Apply**, the I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank, which are no longer compatible with the standards applied, are unassigned.
4. Click **More Attributes** to set the low-power mode and input delay (as shown in Figure 11 on page 11). (These attributes are not supported in RTAX-S).
5. Assign I/O standards to other banks by selecting the banks from the list and assigning standards. Any banks not assigned I/O standards use the default standard selected in the Device Selection Wizard.
6. Leave the **Use default pins for V_{REF}** option selected to set default V_{REF} pins and unset nondefault V_{REF} pins. If you unselect this option when setting a new V_{REF} technology, no V_{REF} pins are set. If you unselect this option when default V_{REF} pins are already set, it unsets them.

   If the **Use default pins for V_{REF}** option is selected when you click **OK** or **Apply**, the software will:
   - Determine if setting default V_{REF} pins causes any I/O cores to become unassigned, and if so, displays a warning message enabling you to cancel this operation.
   - Determine if unsetting non-default V_{REF} pins causes any I/O cores to become unassigned, and if so, displays a warning message enabling you to cancel this operation.
   - Set default V_{REF} pins and unset non-default V_{REF} pins.

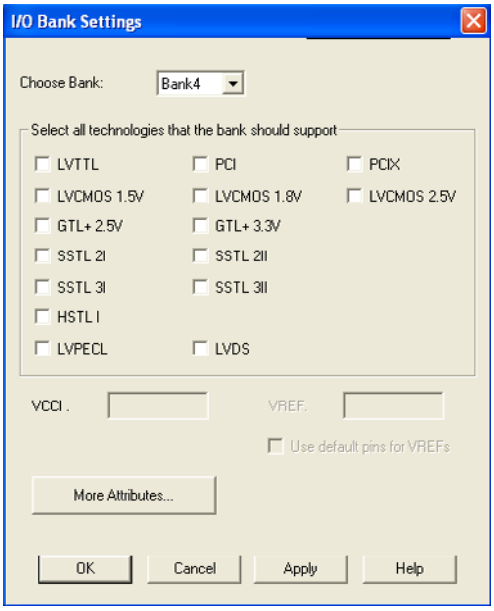

Figure 11 • **I/O Bank Settings Dialog Box for Axcelerator Devices**

If V_{REF} pins can be assigned, you must assign at least one V_{REF} pin before running Layout.

Note: If you use I/O standards that need reference voltage, make sure to assign V_{REF} pins. Actel strongly recommends you use the defaults. V_{REF} pins appear in red in ChipPlanner and are labeled V_{REF} in PinEditor.

To set the low-power mode and input delay:

1. Click **More Attributes** in the **I/O Bank Settings** dialog box.
2. Drag the slider bar to the desired delay. The delay is bank specific.
3. Click **View All Delays** to see all the delay values (Best, Worst, Typical, Rise-Rise, Fall-Fall) for the input delay selected. You must select a technology to see the input delays.
4. Click **OK** (Figure 12).

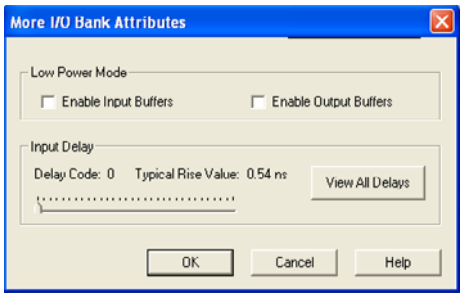

Figure 12 • **Other I/O Bank Attributes Dialog Box**

Note: Low Power Mode and Input Delay are not supported in RTAX-S devices.

Manually Assigning V_{REF} Pins

Voltage referenced I/O inputs require an input referenced voltage (V_{REF}). You must assign V_{REF} pins before running Layout.

Before assigning a V_{REF} pin, you must set a V_{REF} technology for the bank to which the pin belongs.

To set a V_{REF} technology for a bank:

1. Select a bank in ChipPlanner.
2. From the **Edit** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select a technology such as GTL+ 3.3 V so the V_{REF} field displays a non-zero value (uncheck Use default pins for V_{REF} box).
4. Click **Apply** and then **OK**. Now, when you right-click on pins in this I/O bank, the V_{REF} commands on the menu are enabled.

In either the PinEditor or ChipPlanner window, you can change a regular pin into a V_{REF} pin from the right-click menu.

To assign a pin as a V_{REF} pin:

1. In either PinEditor or ChipPlanner, select the pin to set as a V_{REF} pin.
2. Right-click and choose **Use Pin for V_{REF}** (Figure 13).

   A check mark appears next to the Use Pin for V_{REF} command in the right-click menu (Figure 13).

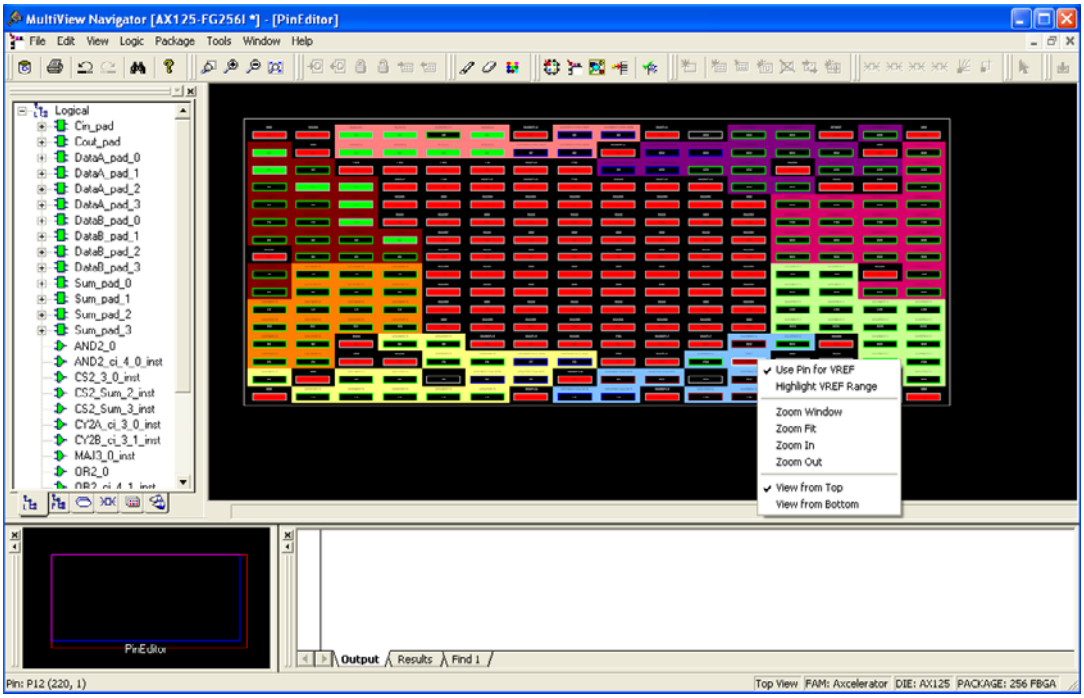

Figure 13 • **Manually Assigning V_{REF} Pins**

Note: The Use Pin for V_{REF} command appears on the right-click menu only if you selected a pin in an I/O bank that supports V_{REF} pins and for package pins or I/O modules that can become V_{REF} pins.

Setting a pin as a V_{REF} may result in I/O cores becoming unassigned, even if they are locked. In this case, a warning message appears so you can cancel this operation.

To unassign a V_{REF} pin:

1. Select the pin to unassign.
2. Right-click and choose **Use Pin for V_{REF}**. The check mark next to the command disappears. The V_{REF} pin is now a regular pin.

Resetting the pin may result in unassigning I/O cores, even if they are locked. In this case, a warning message appears so you can cancel this operation.

After you assign the V_{REF} pins, right-click a V_{REF} pin and choose Highlight V_{REF} Range to see how many I/Os are covered by this pin. To unhighlight the range, choose **Unhighlight All** from the **Edit** menu.

Automatically Assigning Technologies to I/O Banks

The I/O Bank Assigner (IOBA) tool runs automatically when you run Layout. You can also use this tool from within the MultiView Navigator (Figure 14). The IOBA tool automatically assigns technologies and V_{REF} pins (if required) to every I/O bank that does not currently have any technologies assigned to it. This tool is available when at least one I/O bank is unassigned.

To automatically assign technologies to I/O banks:

From the Tools menu, choose **I/O Bank Assigner**. Alternatively, you can click the IOBA toolbar button.

Messages appear in the Output window informing you when the automatic I/O bank assignment begins and ends. If the assignment is successful, the message, **I/O Bank Assigner completed successfully**, appears in the Output window as shown in Figure 14.

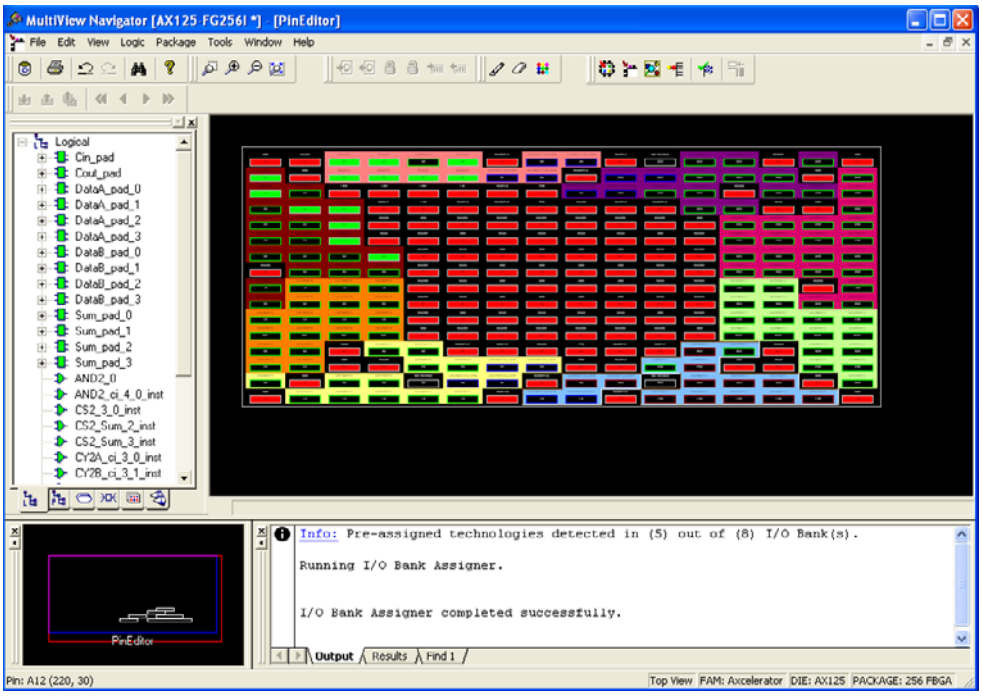

Figure 14 • **I/O Bank Assigner Displays Messages in Output Window**

If the assignment is not successful, an error message appears in the Output window.

To undo the I/O bank assignments, choose **Undo** from the **Edit** menu. Undo removes the I/O technologies assigned by the I/O Bank Assigner. It does not remove the I/O technologies previously assigned.

To redo the changes undone by the Undo command, choose **Redo** from the **Edit** menu.

If you need to clear I/O bank assignments made before using the Undo command, you can manually unassign or reassign I/O technologies to banks. To do so, choose **I/O Bank Settings** from the **Edit** menu to display the I/O Bank Settings dialog box.

Pin Listing

The V_{REF} rules are applied to die pads, not package pins. The pin listing in the datasheet does not reflect the package pins. A ball map listing spreadsheet has been created to reflect the package pins. The ball map listing shows the pin listing and each pin's relative position within the bank. Figure 15 shows a portion of the ball map listing for an AX125-FG256. The column, Relative I/O Pad Location, should be used to determine which I/O pins are controlled by a particular V_{REF} pin. The values of the locations take into account the V_{CC} and GND pins, and hence they are not in sequential order. When using V_{REF} I/Os, you should employ them to determine the V_{REF} locations. The ball map listing is available to download at http://www.actel.com/techdocs/appnotes/products.aspx#ax.

	A	B	C	D	E
1	AX125 FG256				
2					
3	Function	Ball #	Relative I/O pad location		
4					
5	Bank 0				
6	IO01NB0F0	B4	3		
7	IO01PB0F0	B3	1		
8	IO03NB0F0	A4	9		
9	IO03PB0F0	A3	7		
10	IO04NB0F0	B6	13		
11	IO04PB0F0	B5	12		
12	IO06NB0F0	A6	17		
13	IO06PB0F0	A5	15		
14	IO07NB0F0/HCLKAN	B0	21		
15	IO07PB0F0/HCLKAP	B7	20		
16	IO08NB0F0/HCLKBN	A9	27		
17	IO08PB0F0/HCLKBP	A8	26		

Figure 15 • **Ball Map Listing**

Example

In Figure 15, an AX125-FG256 design with pin B6 is assigned as V_{REF}, and B6 is pin #13 in bank 0. The V_{REF} rule states that each V_{REF} can control eight I/O pads in each direction, which means B6 can control pins 5 to 21 within bank 0 (13 – 8 = 5 and 13 + 8 = 21). The final result is pins A3, A4, B5, A6, B7, and B8 are controlled by this particular V_{REF}, as shown in Figure 16.

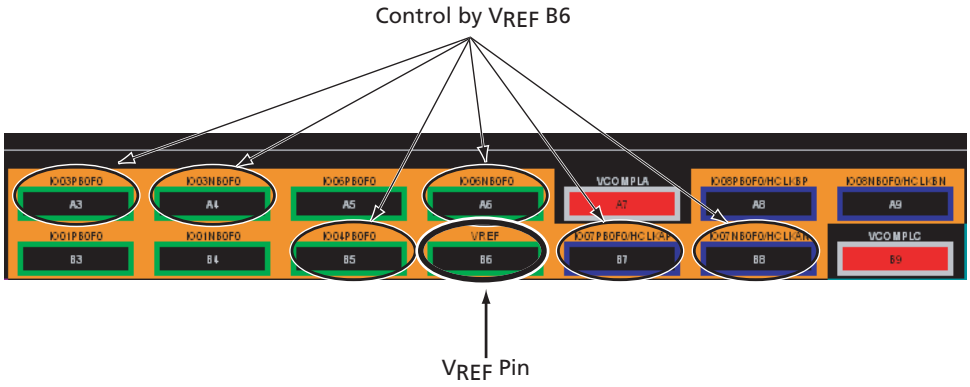

Figure 16 • **Example Results**

Conclusion

Actel Axcelerator devices were designed to meet various design needs. Flexible I/O features, combined with high-speed LVPECL and LVDS I/Os, simplify board-level design and enhance overall performance. Support of voltage-referenced I/O Standards also makes Axcelerator devices suitable for low voltage, high speed applications.

Related Documents

Application Notes

Axcelerator I/O Selection Guide

http://www.actel.com/documents/AX_IOSelection_AN.pdf

List of Changes

Previous Version	Changes in Current Version (5192715-3/1.06*)	Page
5192715-2/11.04	All figures have been updated with the latest software release.	N/A
	The "Using SmartGen for I/O Configuration" section was updated with new steps.	page 2
	The "Input Buffers" section was updated.	page 4
	The "Bidirectional Buffers and Tristate Buffers" section was updated.	page 6
	The bullets in the "Using I/O Attribute Editor for I/O Configuration" section were updated.	page 7
	The "Manually Assigning Technologies to I/O Banks" section is new.	page 10
5192715-1/8.03*	The "Assigning Technologies and VREF to I/O Banks" and "VREF Usage Rules" sections are new.	page 10
	The "Assigning VREF Pins" section is new.	page 10
	The "Pin Listing" section is new.	page 14
	The "Example" is new.	page 14

Note: **This is the part number located on the last page of the document.*

www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan
www.jp.actel.com

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong
www.actel.com.cn

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488

5192715-3/1.06