
Board-Level Considerations

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Introduction

Simulating and debugging individual components is the first step in verifying a board design. Despite all the best design efforts to produce a working design, in some cases, the devices do not operate as anticipated after they are integrated into the system. Many factors, such as power, airflow, and transmission lines can introduce undesirable results in a system and ultimately impair system performance. This application note explains how these factors should be treated while integrating Microsemi® SoC Products Group field programmable gate arrays (FPGAs) in board-level designs.

Power Supply Requirements

In order to operate the device successfully, power supplies must be free from unregulated spikes. All over and undershoots must be well within the absolute maximum ratings given in Microsemi FPGA datasheets. Microsemi recommends that all printed circuit boards (PCBs) should contain the suggested capacitors discussed in the [“Selecting Board Capacitors”](#) section on page 8.

Power-Up Behavior

Microsemi antifuse FPGAs have an internal charge pump which is used to control isolation transistors located on the input and output of every logic module. During power-up, this charge pump turns on the isolation transistors, allowing the logic array and I/Os to function according to the design. The exact behavior is a function of both power-up sequence and ramp rate. SoC Products Group devices have been characterized with two VCCA rise time conditions (i.e. ramp rate): faster ramp rate of approximately 0.5 V/us and slower ramp rate of approximately 0.2 V/ms. During power-up, there is typically a period of in-rush current when the pump is enabled and all of the logic modules are simultaneously connected to the routing tracks. The duration of in-rush current depends on the VCCA ramp rate and usually has a pulse width of approximately 500 ns.

[Table 1 on page 2](#) summarizes I/O behavior, power-up sequencing requirements and transient current during power-up for various Microsemi FPGA families. Refer to the application note and datasheet sections on Microsemi website for specific device information.

I/Os

Driving Capabilities

All Microsemi FPGAs have sufficient current drive capabilities to meet the logic levels defined in JEDEC specifications.

Microsemi provides IBIS models for almost all devices. Source and sink currents can be calculated from this model. These values are taken from a sample group of devices under particular operating conditions. IBIS values are not guaranteed for every device under worst-case conditions.¹ These models should not be used to find out overall drive capability of a device. They give an estimate of source and sink currents per I/O basis. I_{OH} and I_{OL} are specified in the datasheets. Only those values are guaranteed for operation.

The device will not necessarily sustain in a condition where it is forced to source or sink through multiple I/Os at the rate of the maximum value. For example, the maximum source current (from IBIS model) of an SX-A device is 50.9 mA, which means 50.9 mA can be supplied through one output. It does not mean 20 outputs can be forced to source 20 times that current simultaneously. There is a power dissipation limit of every device. The datasheets contain maximum power dissipation limit per package (refer to package thermal characteristics section of the datasheets).

However, sometimes outputs may be tied together externally to increase drive capability provided the device does not exceed maximum allowable power dissipation. Although this is a relatively common design practice, FPGA fabric designers must be diligent in their timing analysis to ensure that the delays from the common source to the multiple output pins are as closely matched as possible to avoid contention in the outputs. This may require manual placement of the driving source cells and the I/O cells.

Table 1 • Power-Up/Down Behavior of Microsemi Devices

| Device | I/O behavior during Power-Up | | Power-Up Sequencing Requirements | Power-Down Sequencing Requirements | Maximum In-Rush during Power-Up (mA) |
|-----------------------------|---|--------------------------------|--|--|--------------------------------------|
| | Slow Power-Up (0.2 V/ms) | Fast Power-Up (0.5 V/ μ s) | | | |
| ACT1/RH1020 | Behave as outputs driving either high or low for up to 5 ms | Tristate | None | None | 10-60 |
| ACT2/RH1280, 1200XL, 3200DX | Behave as outputs driving high for less than 1 ms | Tristate | None | None | 10-50 |
| ACT3 | Tristate | Tristate | None | None | 10-60 |
| SX/RTSX | Behave as outputs driving low | Behave as outputs driving low | VCCR must be greater than or equal to VCCI at all times. (VCCR first, VCCI second) | VCCI first, VCCR second. Complete power down (VCCA=0V) is required for 54SX16, A54SX16P, RT54SX16 and RT54SX32 | 400 |
| MX | Tristate | Tristate | None ¹ | None | 90-539 |

Note:

1. Mixed Voltage power-up of A42MX09, A42MX16, A42MX24, and A42MX36 requires $VCCA \geq VCCI$ throughout the power-up sequence.
2. Depends on ramp rate and power-up sequence. Refer to the application note, [Power-Up Behavior of ProASIC^{PLUS} Devices](#), for detail information.

1. Not all models are based on lab measurement, some models are based on SPICE simulation. Please check the header information in the individual model.

Table 1 • Power-Up/Down Behavior of Microsemi Devices (continued)

| Device | I/O behavior during Power-Up | | Power-Up Sequencing Requirements | Power-Down Sequencing Requirements | Maximum In-Rush during Power-Up (mA) |
|-------------------------|---|---|--|--|--------------------------------------|
| | Slow Power-Up (0.2 V/ms) | Fast Power-Up (0.5 V/ μ s) | | | |
| SX-A | Tristate | Tristate | None | None | 45-557 |
| RTSX-SU | Tristate | Tristate | None | None | 144-790 |
| eX | Tristate | Tristate | None | None | 162 |
| Axcelerator | Tristate | Tristate | VCCDA first, or simultaneously with, VCCA and VCCI | VCCA and VCCI first, or simultaneously with, VCCDA | 100 |
| ProASIC 500K | Tristate | Tristate | VDDP first, VDDL second | None | 38 |
| ProASIC ^{PLUS} | Please refer to the Power-Up Behavior of ProASIC^{PLUS} Devices application note. | Please refer to the Power-Up Behavior of ProASIC^{PLUS} Devices application note. | VDD first, then VDDP (or simultaneously). | None | 50-110 ² |
| ProASIC3/E | Tristate | Tristate | None | None | None |

Note:

1. Mixed Voltage power-up of A42MX09. A42MX16, A42MX24, and A42MX36 requires $VCCA \geq VCCI$ throughout the power-up sequence.
2. Depends on ramp rate and power-up sequence. Refer to the application note, [Power-Up Behavior of ProASIC^{PLUS} Devices](#), for detail information.

Unused I/O Configuration

For all of Microsemi antifuse based FPGAs, I/O modules have the basic architecture as shown in [Figure 1](#). As new families have been introduced, Microsemi has enhanced the design by incorporating latches and flip-flops, but the basic bidirectional buffer functionality has remained the same.

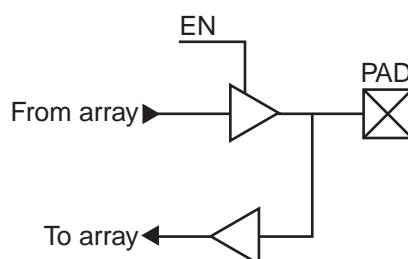


Figure 1 • Basic Architecture of SoC Products Group I/O Modules

This generic architecture is configured to implement the specific I/O macros instantiated in the design netlist. For example, when an INBUF macro is used to bring a signal into the FPGA fabric, the I/O module is configured as an input buffer. When an OUTBUF macro is used to take a signal off-chip, the I/O module will be configured as an output buffer.

When an I/O module is unused, (i.e., not implementing a specific macro) its configuration depends on the device family.

Unused CLKs in the SX, SX-A, RTSX-SU, eX, ProASIC and ProASIC^{PLUS} Families

For eX, SX, SX-A, and RT54SX32S parts, the CLKA/B and HCLK pins are only clock inputs. Unused CLKA/B and HCLK pins must not be left floating.

For RT54SX72S and A54SX72A, both the CLKA/B pins and the QCLKA/B/C/D pins are Clock-I/O pins (can be clock and/or I/O). When these pins are not used, they should be tied "high" or "low" on the board to avoid power dissipation due to a "floating" clock input buffer. The right recommendation is to not leave them floating if unused.

In the case of ProASIC and ProASIC^{PLUS} devices, both GL and GLMX pins can be configured as any normal I/O when they are not connected to the global network or the clock conditioning circuit. If the GL and GLMX are not used, they will be configured as an input with pull-up resistors.

Unused I/Os in the SX, SX-A, RTSX-SU, eX and Axcelerator Families

In the SX, SX-A, RTSX-SU, eX, and Axcelerator families, unused I/Os are configured as a TRIBUF with the enable permanently tied off to GND (disabled) by Microsemi Designer software (Figure 2).

Although tying off unused pins is not required, Microsemi recommends that they be tied to ground.

Driving unused I/Os is acceptable. For SX-A/RTSX-SU, if the clamping diode is disabled in the designer software, the unused I/Os are 5 V tolerant. Otherwise, the unused I/Os are tolerant to VCCI.

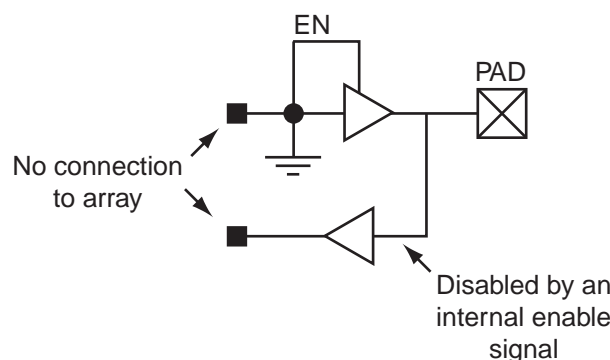


Figure 2 • Configuration of I/O Modules of SX, SX-A, RTSX-SU, eX, and Axcelerator

Unused I/Os in 3200DX, ACT 3, A42MX24, and A42MX36

Unused I/Os in these devices are also tristated. As Figure 3 illustrates, the input buffer is disabled by Microsemi Designer software; therefore, it does not burn power. Although tying off unused pins is not required, SoC Products Group recommends that they be tied to ground. Driving unused I/Os is acceptable.

Unused I/Os in ACT1, ACT2, 1200XL, A40MX02, A40MX04, A42MX09 and A42MX16

By default, unused I/Os in these devices are configured as low drivers as shown in Figure 4 on page 5. Unused I/Os should be tied to GND or left floating. Do not drive an unused I/O to any value other than GND. To configure unused I/Os any other way, you must manually instantiate the desired I/O macro.

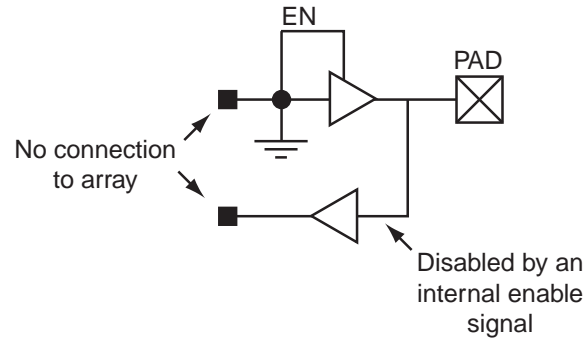


Figure 3 • Configuration of Unused I/Os in 3200DX, ACT3, A42MX24, and A42MX36

For example, to tristate unused pins, you must instantiate one TRIBUFF macro for each unused pin and connect the TRIBUFF as shown in [Figure 5](#) (with the enable and input pins tied to ground). Make sure to assign each TRIBUFF to the appropriate pin using Designer's PinEditor tool.

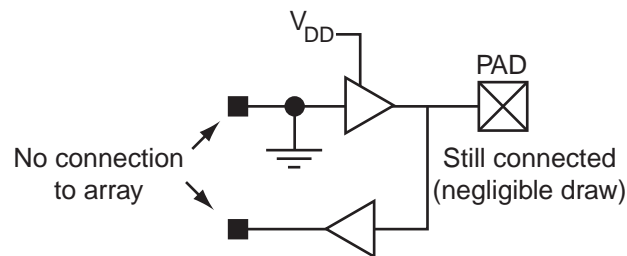


Figure 4 • Default Configuration for Unused I/Os in ACT1, ACT2, 1200XL, A40MX02, A40MX04, A42MX09, and A42MX16

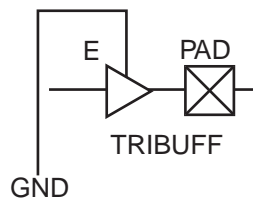


Figure 5 • Suggested User-Defined Configuration for Unused I/Os in ACT1, ACT2, A40MX02, A40MX04, A42MX09, and A42MX16

Unused I/Os in the ProASIC, ProASIC^{PLUS}, ProASIC3/E, IGLOO[®], IGLOO PLUS and IGLOO Families

Designer software configures unused I/Os of the ProASIC, ProASIC^{PLUS}, and ProASIC3/E families as IB33U or IB25LPU macros with a weak pull-up resistor. You can leave these I/Os floating, or terminate them to either VDDP or GND. Similarly, unused I/Os in ProASIC3/E devices are configured as tristate with weak pull-up.

Similarly, unused I/Os in ProASIC3/E, IGLOO, IGLOO PLUS and IGLOO devices are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

So, you can leave these I/Os floating.

Floating Input Behavior for All Antifuse Devices

Microsemi does not recommend floating input pins (including clock pins). Any floating input can cause the input buffer to go into an unpredictable state. It can float to an intermediate state where both transistors of the input buffer may activate and draw high current. Due to the fact that the I/O circuitry differs from family to family, the floating behavior cannot be generalized. Microsemi strongly recommends that any unused input pins should be terminated to a known state in the board.

Special I/Os

Microsemi MX, DX, SX, SX-A, eX, Axcelerator, ProASIC, ProASIC^{PLUS}, and ProASIC3/E devices are equipped with special pins for Boundary-Scan testing. These pins are TMS, TCK, TDI, TDO and TRST (no TRST pin on DX and MX). If these pins are not used they should be properly configured.

A description of their configurations as follows:

1. In dedicated mode an internal pull-up resistor is enabled on the TDI and TMS pins of MX, DX, SX, SX-A and eX devices. Therefore, a termination is not needed on those pins. In flexible mode the internal resistors on TMS and TDI pins of SX, SX-A, and eX devices are disabled, so these pins should be tied to VCC or GND. The TCK, TDI, TMS pins of DX and MX devices can be used as user I/Os in flexible mode. If not used, they will be configured as tristated outputs. In Axcelerator, ProASIC, and ProASIC^{PLUS} devices, TDI and TMS pins are equipped with on-chip 10 k Ω pull-up resistors, and hence termination is not required if the pins are unused. The TCK pin in SX, SX-A, eX, Axcelerator, ProASIC, and ProASIC^{PLUS} devices must always be terminated if not used.
2. In SX-A, eX devices, the TRST pin functions as a dedicated Boundary-Scan Reset pin when the "Reserve JTAG Test Reset" option is selected (in Designer software). An internal pull-up resistor is enabled in this mode. During normal operation this pin should be tied to GND to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or be driven high.
3. When the "Reserve JTAG Test Reset" option is not selected, the TRST pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.
4. TRST pin in SX, RTSX, RTSX-SU, Axcelerator, ProASIC and ProASIC^{PLUS} devices is always reserved for JTAG Test Reset. Please refer to [IEEE Standard 1149.1 \(JTAG\) in the SX/RTSX/SX-A/eX/RT54SX-S Families](#) application note for detailed information.
5. TRST pin should be grounded in flight boards for normal operation.
6. The SDI and DCLK pins in ACT1 and MX devices become user-defined inputs if the program fuse is not blown, so these pins must be terminated if not used.

Slew Rate Effects

Designers must pay close attention to slew rate when selecting parts for digital designs. Input signals must meet the input transition time (t_R , t_F) requirements given in the datasheet. If an input signal becomes too slow, then the noise around the FPGA's input threshold can cause multiple state changes (Figure 6).

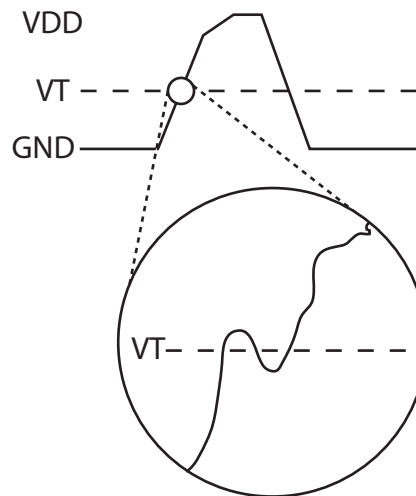


Figure 6 • Multiple State Changes at the Input Threshold Level

During the transition time, both input buffer transistors could potentially turn on at the same time. This could result in unpredictable output buffer oscillations.

In this situation the input buffer could still pass signals. However, these short, unpredictable oscillations would likely cause the device to malfunction. One way to eliminate problems with slow input signals is with external Schmitt triggers. A Schmitt trigger is a buffer used to convert a slow or noisy signal into a clean one before passing it to the FPGA fabric. This is a simple, low-cost solution for a user working with low-slew-rate signals.

In the case of output slew rate, a high number of applications need high-slew-rate signals. In those cases, there are possibilities of unwanted effects such as increased peak current, capacitive coupling, and ground bounce.

If too many outputs are switching at the same time, the output signals can produce ground bounce (refer to [Simultaneous Switching Noise and Signal Integrity](#) application note for more information).

By selecting the low slew-rate option, ground bounce can be minimized. Output slew rate can be selected in the Designer software for some devices. Consult the datasheet for the availability of that option.

Clock Network

Termination

For proper functionality of the device, it is essential that all the signals must meet signal integrity needs. Since clocks are the control signals, special focus is needed to configure them. If the edge rate of the clock signal is slower than the specification, the logic of the circuit driven by the clock signal may be incorrect. Another important parameter affecting the external clock signal's shape is reflection. For example, improper line termination of the clock path can result in uncontrolled reflections (similar to wave reflection in a wave guide).

These uncontrolled reflections of the clock signal on the termination points might result in unwanted spikes on the clock. These spikes might be incorrectly interpreted by FPGA logic as active clock edges, which will result in the design not functioning as expected.

Microsemi recommends AC termination of the clock line with a resistor and capacitor pulled down to ground at the clock input of the device as shown in Figure 7. This RC filter will stop unwanted spikes from propagating into the FPGA fabric.

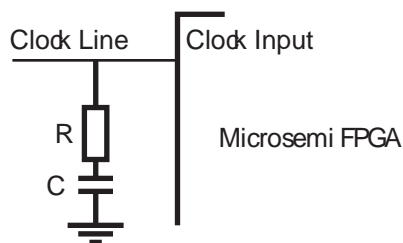


Figure 7 • AC Termination at the Clock Input

The R and C values follow a general rule:

R should be equal to Z_0 , where Z_0 is the impedance of the clock line. By selecting the proper value for R, the reflection coefficient of the line will cancel the reflected signals.

In other words, the reflections of the clock signal will be absorbed at the termination. The C value should be chosen so that the RC time constant is approximately 1/3 of the clock period. By doing this, the clock edges will be fast enough and acceptably noise free.

Another effective way to deal with reflection is to add series termination. The resistor value should be chosen so that the sum of it and the driver IC's impedance equals the effective trace impedance.

$$Z_0 = R_s + Z_d \quad (1)$$

Z_0 = trace impedance, R_s = series termination, Z_d = driver's impedance. The resistor should be placed as close as the driver.

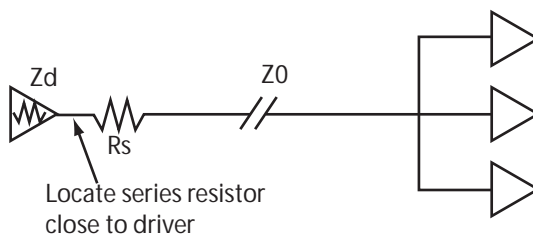


Figure 8 • Series Termination

Selecting Board Capacitors

In high-performance digital systems, when a large number of I/Os of the FPGA fabric are dynamically switching, a sudden change in the amount of current drawn by them can cause a momentary drop (or surge) in the voltage that change in the amount of current drawn (known as delta-I) on the power distribution bus. This delta-I can be sufficiently large enough to interrupt normal operation of the device. Reliable, noise-free circuit operation needs care in choosing the board capacitor types and sizes. There are usually two types of capacitors: decoupling capacitors and plane capacitors. Decoupling capacitors help to stabilize the power distribution bus by supplying current that opposes any change in the bus voltage. Decoupling capacitors network on the board has to be designed to ensure a low power supply impedance over a very wide range of frequencies. Microsemi recommends that the impedance is kept below $0.1 \, \Omega$ between 100 kHz and 1 GHz. This can be achieved with a group of parallel capacitors resonating at frequencies that are one decade away from one another. Also, the number of capacitors should increase as their value decrease.

For example, a decoupling network could be composed of 8 ceramic 0.01 μF X7R capacitors, 4 ceramic 0.1 μF X7R capacitors, 2 ceramic 1 μF X7R capacitors, and 1 electrolytic low frequency 1,000 μF capacitor.

The quality of decoupling the network can be tested in the finalized board by using a spectrum analyzer, which will show frequencies where there might still be insufficient decoupling. Depending on the design, there might be a requirement for more or fewer capacitors, and the spectrum analyzer used in a real board design is the best instrument to test the decoupling network. Below the resonance frequency (since the system contains capacitive and inductive elements), the decoupling capacitor works fine. The typical frequency limit is up to 100 MHz. Since addition of these capacitors needs extra space, sometimes it becomes a challenge for the PCB designers to pick and place right size appropriately. Moreover, above resonant frequency decoupling capacitor cannot supply high ΔI . Above 100 MHz, the extra charge has to come from inter-plane capacitors (plane fills). Specially, at higher frequency 150 MHz and above the capacitance formed by the parallel plates of the power plane provides all switching currents.

Concept of Signal Plane Fills

In the practice of PCB designs most PCBs are not left with sufficient power plane area to create a capacitor large enough to supply the switching currents. It will generate excessive high frequency ripple on the power planes and increase EMI. However, most PCBs have sufficient unused spaces on signal planes, which can be filled with copper to provide additional plate area to increase the size of the capacitors.

Figure 9 on page 10 is an example of high speed 14-layer PCB cross section with plane fills.

To determine how much plane capacitor is needed, following formula can be used:

$$\Delta V/V = C_{swl} / C_{plane} \quad (2)$$

ΔV is maximum allowance ripple, V is power supply voltage, C_{swl} is sum of parasitic capacitance in switching loads, and C_{plane} is plane capacitance needed.

Additionally, Microsemi recommends placing ground planes under SSI and SSO busses, since ground planes are more effective in isolating the noise than power planes. The ground plane layer below SSI and SSO busses needs to be as continuous as possible. Slots, splits, and holes should be avoided in the ground plane below these busses. As mentioned earlier, power planes should be placed on layer adjacent to ground plane, which ensures a high quality RF and VHF decoupling between power and ground.

Sample Calculation of Decoupling Capacitor Size

At below 100 MHz the decoupling capacitor is effective to provide the sufficient switching currents. Following is an example calculation of capacitor size.

A 5 V eX64-TQ64 device has 12 outputs each driving a 70 Ω transmission line, so the total current required is $12 \times 5 \text{ V} / 70 \Omega = 857 \text{ mA}$. Assuming some voltage droop from the power bus (50 mV) and the time required for the capacitor to charge the line is 2 ns, the minimum capacitor value will be:

$$C = I \, dt/dV = 34.28 \text{ nF} \cong 0.035 \mu\text{F} \quad (3)$$

A good practice is to place them in parallel (each 0.01 μF), in order to help reduce capacitive electrical series resistance (ESR).

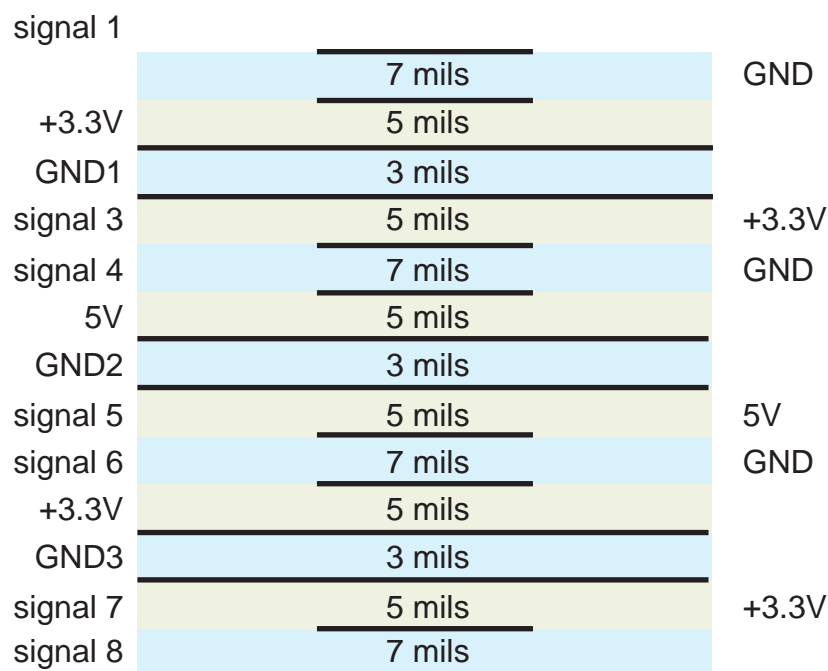
The above calculation is a guideline only, the values of decoupling capacitors are dictated by the switching activity in a design and how much droops in the supply the customer is prepared to tolerate.

Capacitor Placement

Sometimes PCBs are not located near by the power supply unit and hence power distribution inductances (typically in the order of 0.05 nH/cm in a multilayer board) will cause a significant drop in the supply voltage. A bulk decoupling capacitor (example, 10 μF 35 V Tantalum) on the board near the power input can help alleviate this problem. Also this bulk capacitor can be viewed as low-impedance power source. Smaller supply impedance stabilizes the voltage at the board input by providing more current for a given change in the voltage.

The inductance of the traces connecting different components and package lead inductance (sometimes as high as 20 nH) will create same type of voltage fluctuations.

14-Layer Cross Section Plane Fill



Prepreg Material
Laminate Material

Trace
width = 5 mils,
 $Z_0 = 50\Omega$
All internal layers 1.0-ounce copper
Overall thickness 93 mils
3.3 V capacitance = 910 pF/sq in

Figure 9 • Example of Signal Plane Fills

To take care of this situation a local decoupling capacitor (0.1 μ F, 0.01 μ F, or 0.001 μ F) is needed between power and ground pins of every switching component (refer to the Equation 2 for size and quantity guidelines). Microsemi recommends distributing the capacitors around the FPGA fabric as close as possible and not further than one inch away from the FPGA fabric.

If the board contains both inter-plane and decoupling capacitors, then the location is not critical at a frequency ≥ 100 MHz. However, to lower down the trace inductance capacitors can be mounted on the underside of the PCB underneath the FPGA fabric. BGA packages have less lead inductance (as low as 0.2 nH) and can be used to reduce resulting inductance. This will allow the capacitor to operate more efficiently and avoid noise on the power planes.

Furthermore, the decoupling capacitors should connect to ground and power plane vias through wide and very short traces.

Capacitor Dielectric

The capacitor dielectric material is an important factor when selecting capacitors.

The dielectric materials that have high dielectric constants also have the worst temperature coefficients. For example, the Z5U dielectric type has a higher dielectric constant than the X7R type but worse temperature and aging properties. Its temperature variation of capacitance is within +22% to –56% from 10°C to 85°C. Despite their capacitance instability, Z5U formulations are very popular because of their small size, low ESR and excellent frequency response. These features are particularly important for decoupling the application where only a minimum capacitance value is required.

Y5V formulations are for general-purpose use in a limited temperature range. They have a wide temperature characteristic of +22% to –82% capacitance change over the operating temperature range of –30°C to +85°C. Y5Vs high dielectric constant allows the manufacture of very high capacitance value (up to 22 MF) in small physical sizes and hence it can be used as a bulk capacitor.

Voltage Ratings and Lifetime

It is not wise to always operate at the rated voltage. A 50% voltage derating may significantly improve a capacitor's expected lifetime. For example, if the voltage rating of a capacitor is 34 V, it should be restricted to a 17 V or lower system.

Output Loading

Increasing capacitive loading of device outputs results in larger transient currents and oscillation in the power planes. If the decoupling capacitor is not capable of supplying the needed charge, the power planes may start to ring and eventually oscillate up to 2 V to 3 V peak-to-peak amplitude. By limiting capacitive loads, this effect can be reduced.

Some Useful Signal Integrity Tips

The biggest challenge for PCB designers is signal-integrity issues. The subject itself requires a separate application note so it will not be addressed in this document. Here are some basic recommendations:

1. If the FPGA fabric is driving clock for multiple receivers, it is important that the clock should be fanned out in multiple pins. In this way every receiver will get its own clock.
2. Keep the clock trace at least 40 mils from adjacent trace to avoid cross-talk (adjacent trace should be routed at a distance of four times the trace width). The low dielectric material also plays an important role in reducing the cross-talk.
3. Always use GND VIAS every time the signal makes a layer change.
4. If the line or loop has signal energy at a frequency high enough that the line or loop represents at least a tenth of a wavelength, there will be a measurable amount of electromagnetic radiation ("radio waves"). For example, a 100 MHz signal may radiate with a 12-inch trace length. Shortening the traces on the board, having GND plane beneath the traces and reducing other signal integrity problems may help to minimize EMI.
5. Minimize stub lengths.
6. Also please study the [*Simultaneous Switching Noise and Signal Integrity*](#) application note.

Operating Environment

Microsemi FPGAs must not be operated outside of the recommended operating conditions as described in the Absolute Maximum Ratings section of the datasheets. Exposure to maximum rated conditions for prolonged periods may result in irreparable damage to the device. As can be seen in the timing derating section of the datasheets, variations in voltage, temperature, and process will affect device performance. The designer must be careful to design systems so that the effects of these variables, from best to worst case, will not cause timing problems during inter-chip communications.

Thermal Considerations

Ambient temperature can also affect FPGA fabric performance. Microsemi's Designer software reports timing which is derated by thermal junction temperature. This is the temperature found at the junction of the die and the package casing. Additional derating must be applied for ambient-to-junction temperature effects (θ_{ja}). The units for θ_{ja} are °C/W. This implies that the device power dissipation must first be calculated to determine the value for θ_{ja} . (Please refer to the Power Dissipation section in SoC Products Group's datasheets.) Note that the value for θ_{ja} will vary from package to package. Because θ_{ja} is a function of ambient temperature, the use of a fan can decrease the θ_{ja} value. This can be seen by observing the difference between the θ_{ja} value in still air and at 300 ft./min., as shown in the [Package Thermal Characteristic](#) application note.

ESD Precautions

Electrostatic discharge (ESD) is defined as a transfer of an electrical charge between objects at different potentials, caused either by direct contact or induced by an electrical field. All types of electronic devices need to be handled correctly in compliance with ESD precaution guidelines. A simple shock from a doorknob can be as high as 35,000 volts. Due to ESD, devices can be either catastrophically damaged or degraded. All Microsemi packaged devices are delivered with a sealed static shield bag. When the customer receives the devices, any handling must be in accordance with ESD protection guidelines.

Conclusion

The guidelines described above are not consequences of using Microsemi devices but are rather good design practices that can be applied to any system. It is impossible to cover all device configurations and recommend board-level design tips. Each user needs to make decisions on what type and how many components to use based on cost, performance, and board space. The above guidelines are useful to facilitate making those decisions.

Related Documents

Application Notes

Power-Up Behavior of ProASIC^{PLUS} Devices

www.microsemi.com/soc/documents/APA_PowerUp_AN.pdf

IEEE Standard 1149.1 (JTAG) in the SX/RTSX/SX-A/eX/RT54SX-S Families

www.microsemi.com/soc/documents/SX_SXAJTAG_AN.pdf

Simultaneous Switching Noise and Signal Integrity

www.microsemi.com/soc/documents/SSO_AN.pdf

Package Thermal Characteristic

www.microsemi.com/soc/documents/Pack_Therm_AN.pdf

List of Changes

The following table lists critical changes that were made in each revision of the document.

| Revision* | Changes | Page |
|-------------------------------|---|------|
| Revision 4 (February 2012) | Corrected the Figure 2 title and updated "Unused I/Os in ACT1, ACT2, 1200XL, A40MX02, A40MX04, A42MX09 and A42MX16" section (SAR 36146). | 4 |
| Revision 3 (January 2012) | Under "Unused CLKs in the SX, SX-A, RTSX-SU, eX, ProASIC and ProASICPLUS Families" section on page 4 third paragraph removed the last sentence and incorporated a new sentence (SAR 30831). | 4 |
| | The "Unused I/Os in the ProASIC, ProASICPLUS, ProASIC3/E, IGLOO®, IGLOO PLUS and IGLOO Families" section was updated (SAR 27414). | 6 |
| | Updated the last part of "Unused I/Os in the ProASIC, ProASICPLUS, ProASIC3/E, IGLOO®, IGLOO PLUS and IGLOO Families" section (SAR 32625). | 6 |
| Revision 2 (July 2006) | Table 1 was updated to include ProASIC3/E information. | 2 |
| | "Selecting Board Capacitors" was updated with capacitor information and Microsemi SoC Products Group recommendations. | 8 |
| | Microsemi SoC Products Group recommendations were added to the "Concept of Signal Plane Fills" section. | 9 |
| | Microsemi SoC Products Group recommendations were added to the "Capacitor Placement" section. | 9 |
| Revision 1 | The "Driving Capabilities" section on page 2 was updated. | 2 |
| | Table 1 on page 2 was updated. | 2 |
| | The "Slew Rate Effects" section on page 7 was updated. | 7 |
| | The "Selecting Board Capacitors" section on page 8 was updated. | 8 |
| | The "ESD Precautions" section on page 12 was updated. | 12 |

Note: * The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.



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