SmartFusion: FPGA Fabric Synthesis Guidelines

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Introduction

SmartFusion™ intelligent mixed signal FPGAs integrate an FPGA fabric, hard ARM® Cortex™-M3 processor, and programmable analog for a wide variety of embedded system applications. SmartFusion FPGAs contain a hard embedded microcontroller subsystem (MSS), consisting of a 100 MHz ARM Cortex-M3 processor, communications matrix, system registers, Ethernet MAC, peripheral DMA engine, real-time counter (RTC), embedded nonvolatile memory (eNVM), and embedded SRAM (eSRAM) and fabric interface controller (FIC) that are interconnected via a multi-layer AHB bus matrix (ABM).

The MSS can be connected to the FPGA fabric through a configurable FIC that allows an AHB-to-AHB or AHB-to-APB3 bridging function between the AHB bus matrix and an AHB or APB3 bus implemented in the FPGA fabric. It provides two bus interfaces between the MSS and fabric. The first is mastered by the MSS and has slaves in the fabric and the second has a master in the FPGA fabric and slaves in the MSS.

User logic implementing the master or slave in FPGA fabric communicates with the MSS through the FIC. This involves paths crossing the interface between the MSS, which is a hardened block, and the user logic in FPGA fabric, which is in soft gates. To meet timing requirements of the design, certain guidelines must be followed. This application note covers guidelines on creating proper synthesis constraints to arrive at an optimum design.

The constraints generated in Synplify_Pro should only be used during synthesis. They must not be passed to the Designer as SmartTime timing constraints tool derives the appropriate constraints automatically based on the MSS configuration.

This application note covers the following topics pertaining to synthesis:

- Explanation of clocks that affect the inter-clock domain between the MSS and FPGA fabric: FCLK, FAB_CLK, and their relationship
- Overview of paths that cross the boundary between the MSS and FPGA fabric
- Timing shells generated and passed to Synplify Pro for AHB, APB, and AHB bypass mode configurations
- Creating clocks for synthesis for deriving constraints on paths originating in the MSS (source in MSS and sink in FPGA fabric) and paths originating in the FPGA fabric (source in FPGA fabric and sink in the MSS) for synthesis only
- Observing the effect of constraints during synthesis on a sample AHB design and APB design

Relationship Between MSS FCLK and FPGA Fabric FAB_CLK

Configure the clock requirements for the design using the MSS CCC configurator. The SmartFusion MSS is clocked by FCLK; and FPGA fabric is clocked by FAB_CLK. FAB_CLK is related to FCLK and can have a relationship of 1:1, 1:2, or 1:4 with FCLK; that is, when FCLK is set to 100 MHz, FAB_CLK can be configured as 100 MHz, 50 MHz, or 25 MHz.

FCLK uses the GLA0 output of the MSS CCC. FAB_CLK uses the GLA1 output of the MSS CCC for the FAB_CLK:FCLK ratio of 1:1. When the ratio is 1:2 or 1:4, then FAB_CLK uses the GLB output of the MSS_CCC. Refer to the *MSS Clock Configuration User's Guide* for further details.

Regardless of the ratio of FCLK:FAB_CLK, the specific registers inside FIC that interact with the FPGA fabric are synchronized to FAB_CLK. This is accomplished by using FAB_CLK as sort of Enable to the registers. Because of this even though these registers are clocked by FCLK they can be treated as equivalent to registers clocked by FAB_CLK for all timing purposes (Figure 1).

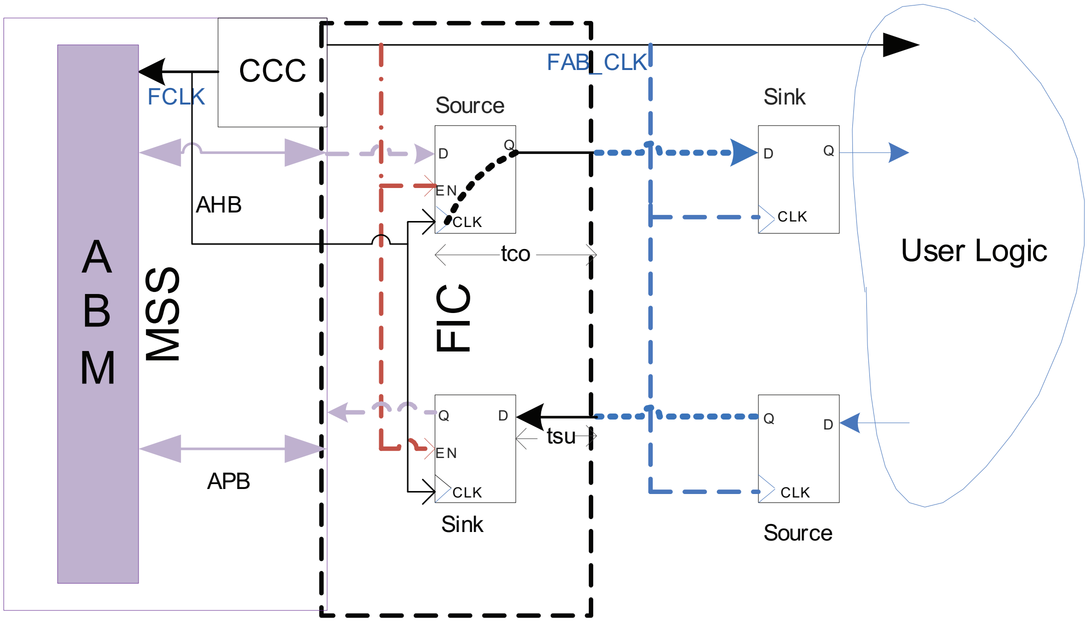


Figure 1 • **MSS, FIC, FPGA Fabric Data and Clock Paths**

SmartTime constraint generation and timing analysis tools have this knowledge and use it for proper timing analysis. The Synplify Pro synthesis tool is not aware of this and subsequent sections explain how to pass this information to the tool.

Overview of Register-to-Register Paths Between MSS and FPGA Fabric

Register-to-register paths crossing the FIC can be categorized into two types. The first type is those that have paths originating (source) in the MSS and destination (sink) in the FPGA fabric. For this type of path, part of the register-to-register path is hardwired and has a fixed value; specifically, the clock-to-out of the register in the FIC from where data is launched is fixed. This parameter is identified as **tco**. The remaining portion of this path is in the FPGA fabric. Synthesis can constrain and optimize this portion of the path.

Refer to Path1 in Figure 2.

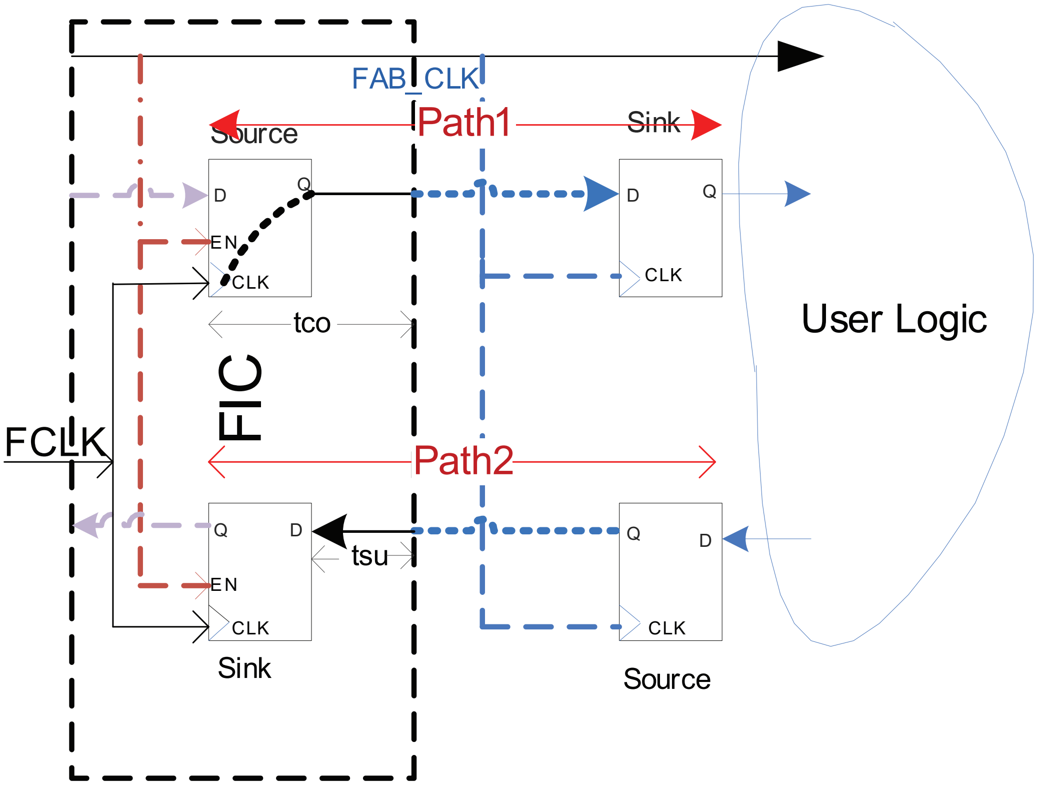


Figure 2 • **Types of Paths Between MSS and FPGA Fabric**

The second type is those that originate (source) in the FPGA fabric and have a destination (sink) in the MSS. For these types of paths, part of the register-to-register path is hardwired and has a fixed value; specifically the setup time of the register in the FIC where data is captured. This parameter is identified as **tsu**. The remaining portion of this path is in the FPGA fabric. Synthesis can constrain and optimize this portion of the path. Refer to Path 2 in Figure 2.

Starting with Microsemi SoC Products Group Libero® Integrated Design Environment (IDE) v9.1, using the MSS version 2.4.101 or later, this information is passed by SmartDesign to the Synplify Pro synthesis tool through a timing shell. This timing shell is generated based on the configuration of the FIC. The three possible timing shells that can be generated are AHB, APB, and AHB in bypass mode.

Timing Shell Overview for APB and AHB Interfaces

The timing shells generated for APB, AHB, and AHB in bypass mode contain the relevant paths for that mode. These include paths for both master and slave configurations. Also the values of clock-to-out (tco) and setup time (tsu) are provided in the timing shell.

This section will familiarize you with the paths for APB and AHB. For naming convention of AHB and APB signals, refer to the "Fabric Interface and IOMUX" chapter in the *Actel SmartFusion Microcontroller Subsystem (MSS) User's Guide*.

Note: As explained in the "Relationship Between MSS FCLK and FPGA Fabric FAB_CLK" section on page 2, FCLK in this context is the same as FAB_CLK.

Note: In addition to APB/AHB signals, the timing shell contains timing information fo Ethernet MAC signals and GPIO signals. These are not discussed in this application note. In case of Ethernet MAC, MAC_CLK and incase of GPIO, PCLK1 need to be created and constrained during synthesis. This is similar to the constraint generation on FAB_CLK discussed in the section "Creating Timing Constraints in Synplify Pro" on page 5.

Table 1 • **AHB Timing Shell Arcs**

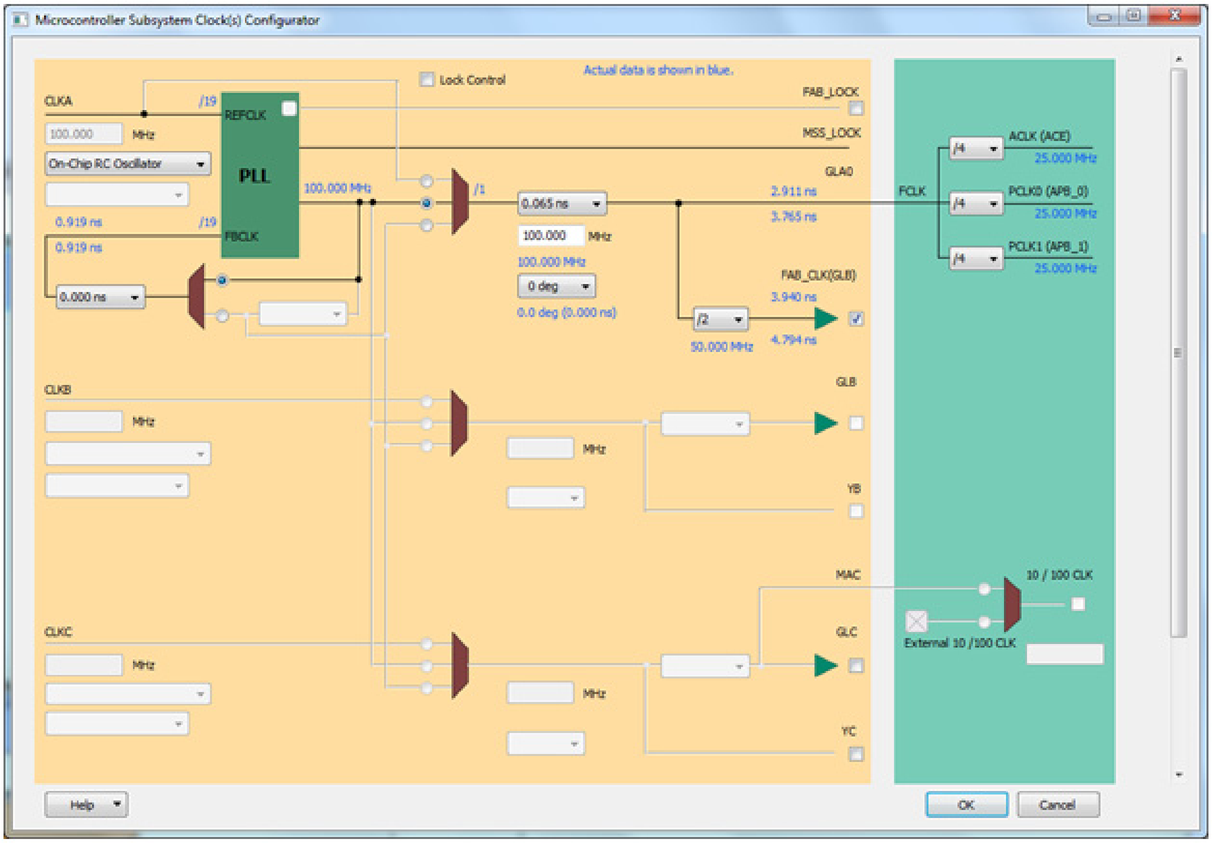
AHB Timing Shell (Master and Slave)				
MSS	**FPGA fabric**	**tco**	**tsu**	**Path**
Fabric AHB Slave				
Source	Destination	Yes	No	FCLK->MSSHADDR[19:0]
Source	Destination	Yes	No	FCLK->MSSHLOCK
Source	Destination	Yes	No	FCLK->MSSHSIZE[1:0]
Source	Destination	Yes	No	FCLK->MSSHTRANS[1:0]
Source	Destination	Yes	No	FCLK->MSSHWDATA[31:0]
Source	Destination	Yes	No	FCLK->MSSHWRITE
Destination	Source	No	Yes	MSSHRDATA[31:0]->FCLK
Destination	Source	No	Yes	MSSHREADY->FCLK
Destination	Source	No	Yes	MSSHRESP->FCLK
Fabric AHB Master				
Destination	Source	No	Yes	FABHADDR[31:0]->FCLK
Destination	Source	No	Yes	FABHMASTLOCK->FCLK
Destination	Source	No	Yes	FABHREADY->FCLK
Destination	Source	No	Yes	FABHSEL->FCLK
Destination	Source	No	Yes	FABHSIZE[1:0]->FCLK
Destination	Source	No	Yes	FABHTRANS[1:0]->FCLK
Destination	Source	No	Yes	FABHWDATA[31:0]->FCLK
Destination	Source	No	Yes	FABHWRITE->FCLK
Source	Destination	Yes	No	FCLK->FABHRDATA[31:0]
Source	Destination	Yes	No	FCLK->FABHREADYOUT
Source	Destination	Yes	No	FCLK->FABHRESP

Table 2 • **APB Timing Shell Arcs**

APB Timing Shell (Master and Slave)				
MSS	**FPGA fabric**	**tco**	**tsu**	**path**
Fabric APB Slave				
Source	Destination	Yes	No	FCLK->MSSPADDR[19:0]
Source	Destination	Yes	No	FCLK->MSSPENABLE
Source	Destination	Yes	No	FCLK->MSSPSEL
Source	Destination	Yes	No	FCLK->MSSPWDATA[31:0]
Source	Destination	Yes	No	FCLK->MSSPWRITE
Destination	Source	No	Yes	MSSPRDATA[31:0]->FCLK
Destination	Source	No	Yes	MSSPREADY->FCLK
Destination	Source	No	Yes	MSSPSELVERR->FCLK
Fabric APB Master				
Destination	Source	No	Yes	FABPADDR[31:0]->FCLK
Destination	Source	No	Yes	FABPENABLE->FCLK
Destination	Source	No	Yes	FABPSEL->FCLK
Destination	Source	No	Yes	FABPWDATA[31:0]->FCLK
Destination	Source	No	Yes	FABPWRITE->FCLK
Source	Destination	Yes	No	FCLK->FABPRDATA[31:0]
Source	Destination	Yes	No	FCLK->FABPREADY
Source	Destination	Yes	No	FCLK->FABPSELVERR

Creating Timing Constraints in Synplify Pro

The timing shell corresponding to AHB or APB is generated by SmartDesign. The file mss_tshell.v for Verilog flow and mss_tshell.vhd for VHDL flow is passed to Synplify Pro along with the design files. Synplify Pro reads these files and comes to know about the timing paths between the MSS and FPGA fabric. Figure 3 shows the MSS CCC configuration used in this example.



Microcontroller Subsystem Clock(s) Configurator

Actual data is shown in blue.

□ Lock Control

CLKA: 100.000 MHz, On-Chip RC Oscillator

PLL: REFCLK /19, FBCLK /19, 100.000 MHz

0.919 ns
0.919 ns
0.000 ns

GLA0: /1, 0.065 ns, 100.000 MHz, 100.000 MHz, 0 deg, 0.0 deg (0.000 ns), 2.911 ns, 3.765 ns

FAB_CLK(GLB): /2, 50.000 MHz, 3.940 ns, 4.794 ns ☑

FCLK:
ACLK (ACE): /4, 25.000 MHz
PCLK0 (APB_0): /4, 25.000 MHz
PCLK1 (APB_1): /4, 25.000 MHz

Figure 3 • **MSS CCC Configuration Used for the Design**

For Synplify Pro to understand the timing margin for the register-to-register path requirements, both the clocks, FAB_CLK and FCLK, must be generated for use by Synplify Pro. You can use the Synplify Timing Constraints file (.sdc) or use SCOPE constraints editor UI in Synplify Pro for entering constraints.

Figure 4 on page 6 shows an example of a Synplify Timing Constraints file. Make note of the fact that both FCLK and FAB_CLK are generated with 50 MHz clock frequency, which is the FAB_CLK frequency. This is only needed for Synthesis.

```
define_clock   {n:M3_PROC_ADC_DAC_0.MSS_CCC_0.FAB_CLK}
     -name {n: M3_PROC_ADC_DAC_0.MSS_CCC_0.FAB_CLK}
     -freq 50 -clockgroup default_clkgroup_0

define_clock   {n: M3_PROC_ADC_DAC_0.MSS_CCC_0.GLA0}
     -name {n: M3_PROC_ADC_DAC_0.MSS_CCC_0.GLA0}
     -freq 50 -clockgroup default_clkgroup_0
```

Notes:

1. *FCLK is always the GLA0 output of the MSS CCC.*
2. *M3_PROC_ADC_DAC_0 is the instance name of the MSS. This is design dependent.*
3. *50 MHz is the frequency of FAB_CLK as configured by user in MSS CCC.*

Figure 4 • **Synplify Timing Constraints File Example**

These generated clocks allow Synplify Pro to derive the timing margin for the non-hardwired portion of the register-to-register paths and constrain them to meet the timing requirements.

Performing Synthesis and Analyzing Timing Reports

After creating timing constraints, perform synthesis. To make sure that Synplify Pro used the timing shell information and constraints for optimal synthesis, review the synthesis log file (*.srr) worst path information. This section shows sample paths for one AHB master design and one APB master design to familiarize you with the analysis.

AHB master

In this design the AHB fabric master interfaces with the SmartFusion MSS. The worst path reported is from one of the HADDR pins to a register in the fabric master. Make note of the fact that the synthesis tool takes into account the tco of the HADDR pin from the timing shell (2.679 ns) while computing the worst path.

Worst Path Information

```
Path information for path number 1:
     Requested Period:                    20.000
     - Setup time:                        0.608
     + Clock delay at ending point:       0.000 (ideal)
     = Required time:                     19.392

     - Propagation time:                  23.621
     - Clock delay at starting point:     0.000 (ideal)
     = Slack (non-critical):              -4.229

Number of logic level(s):                 11
Starting point:                           M3_PROC_0.MSS_ADLIB_INST / MSSHADDR[17]
Ending point:                             COREAHBTOAPB3_0.CAHBtoAPB3oi0.CAHBtoAPB3oli[0] / E
The start point is clocked by             M3_PROC_0.MSS_CCC_0.GLA0 [rising] on pin FCLK
The end   point is clocked by             M3_PROC_0.MSS_CCC_0.FAB_CLK [rising] on pin CLK
```

Instance/Net Name	Type	Pin Name	Pin Dir.	Delay	Arrival Time	No. of Fanouts
M3_PROC_0.MSS_ADLIB_INST	MSS_AHB	MSSHADDR[17]	Out	2.679	2.679	
Z\\M3_PROC_0_MSS_MASTER_AHB_LITE_HADDR_\[17\]\\	Net	–	–	0.386	–	2
CoreAHBLite_1.CAHBLTLLO1LL.CAHBLTolllll.CAHBLTIl0l_RNIIQRE[17]	MX2	A	In	–	3.065	–
ICoreAHBLite_1.CAHBLTLLO1LL.CAHBLTolllll.CAHBLTIl0l_RNIIQRE[17]	MX2	Y	Out	0.579	3.643	–
COREAHBTOAPB3_0.CAHBtoAPB3LL0.HREADYOUT_RNI7CAHK	NOR3	Y	Out	0.751	16.485	–
hsel_0	Net	–	–	2.409	–	22
COREAHBTOAPB3_0.CAHBtoAPB3oi0.CAHBtoAPB3oli_1_sqmuxa	NOR2B	A	In	–	21.070	–
COREAHBTOAPB3_0.CAHBtoAPB3oi0.CAHBtoAPB3oli_1_sqmuxa	NOR2B	Y	Out	0.514	21.584	–
CAHBtoAPB3oli_1_sqmuxa	Net	–	–	2.037	–	13
COREAHBTOAPB3_0.CAHBtoAPB3oi0.CAHBtoAPB3oli[0]	DFN1E0C0	E	In	–	23.621	–

Total path delay (propagation time + setup) of 24.229 is 9.496 (39.2%) logic and 14.733 (60.8%) route.

Path delay is compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value.

APB master

In this design the APB fabric master interfaces with the SmartFusion MSS. The worst path reported is shown below, which is from one of the pins to a register in the fabric master. The synthesis tool takes into account tco of the FABPREADY pin from the timing shell (2.712 ns) while computing the worst path.

```
Path information for path number 4:
        Requested Period:              20.000
        - Setup time:                  0.539
        + Clock delay at ending point: 0.000 (ideal)
        = Required time:               19.461

        - Propagation time:            16.261
        - Clock delay at starting point: 0.000 (ideal)
        = Slack (non-critical):        3.201
Number of logic level(s):              11
Starting point:                        M3_PROC_0.MSS_ADLIB_INST / FABPREADY
Ending point:                          APB_MASTER_BLOCK_0.PADDR_1[15] / D
The start point is clocked by          M3_PROC_0.MSS_CCC_0.GLA0 [rising] on pin FCLK
The end   point is clocked by          M3_PROC_0.MSS_CCC_0.FAB_CLK [rising] on pin CLK
```

Instance/Net Name	Type	Pin Name	Pin Dir.	Delay	Arrival Time	No. of Fanouts
M3_PROC_0.MSS_ADLIB_INST	MSS_APB	FABPREADY	Out	2.712	2.712	–
CoreAPB3_0_APBmslave0_PREADY	Net	–	–	0.386	–	2
APB_MASTER_BLOCK_0.current_state_RNIARG8[6]	OA1B	C	In	–	3.098	–
APB_MASTER_BLOCK_0.current_state_RNIARG8[6]	OA1B	Y	Out	0.525	3.623	–
un1_current_state_m2_e_2	Net	–	–	0.322	–	1
...						
...						
APB_MASTER_BLOCK_0.PADDR_1_RNO[15]	MX2	B	In	–	15.353	–
APB_MASTER_BLOCK_0.PADDR_1_RNO[15]	MX2	Y	Out	0.586	15.939	–
PADDR_6[15]	Net	–	–	0.322	–	1
APB_MASTER_BLOCK_0.PADDR_1[15]	DFN1C0	D	In	–	16.261	–

Total path delay (propagation time + setup) of 16.799 is 9.538 (56.8%) logic and 7.261 (43.2%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value.

Conclusion

This application note has provided guidelines for generating synthesis timing constraints so the synthesis tool can effectively use timing arc information passed to it. Following these guidelines ensures the synthesis tool generates an optimal netlist for the designs that use the SmartFusion FPGA fabric.

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