SmartFusion cSoC Board Design Guidelines

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Objective

The successful design of printed circuit boards (PCBs) incorporating the SmartFusion® customizable system-on-chip (cSoC) devices requires a good understanding of the mixed signal nature of the SmartFusion chips. Good board design practices are required to achieve the expected performance from the PCB and SmartFusion cSoC devices. These are essential to achieve high quality and reliable results, such as minimal noise levels and adequate isolation between digital and analog domain.

This document presents guidelines for board-level design specific applications using SmartFusion cSoC devices. These guidelines should be treated as a supplement to standard board-level design practices.

This document assumes that the readers are experienced in digital and analog board layout and knowledgeable in the electrical characteristics of mixed signal systems. Background information on the key theories and concepts of mixed signal board-level design is available in *High Speed Digital Design: A Handbook of Black Magic*[1], as well as in many reference text books and literature.

Analog and Digital Plane Isolation

Since SmartFusion cSoC device is a mixed signal product in which both analog and digital components exist, it requires both analog and digital supply and ground planes. In addition, there are several voltage supply and ground pins on the device to power different components on the die. This section discusses the layout of the different analog or digital planes and recommends schemes to efficiently isolate different digital and analog domains from each other. This section also describes all ground and supply pins of the SmartFusion cSoC device required to operate the chip, and explains how to connect them to the existing digital or analog supply or ground planes.

1. *Johnson, Howard, and Martin Graham, High Speed Digital Design: A Handbook of Black Magic. Prentice Hall PTR, 1993. ISBN-10 0133957241 or ISBN-13: 978-0133957242*

Placement of SmartFusion cSoC Device and Isolation of Ground Planes

In applications using SmartFusion cSoC devices, two separate grounds to the device should be provided: GND (digital ground) and GNDA (analog ground). The ground pins of the device are to be connected to one of the ground planes appropriately, as discussed in the "Isolation of Ground Planes" on page 3. GND is the digital ground plane that connects to all GND pins of a SmartFusion cSoC device, while GNDA is the analog ground plane that connects to all GNDA pins of a SmartFusion cSoC device.

To avoid noise propagation from one plane to another (for example, from digital to analog ground), the ground planes should be well isolated from each other. Correct layout of the ground planes on the board for current and return paths in the board will prevent the noise in one plane to affect others. For example, if the return path of a digital signal trace on the board passes through the ground analog plane, the GNDA will be vulnerable to noise induced by the digital signal. Therefore, it is critical for digital traces and components on the board to be routed and placed only in the area of their corresponding layer that is covered by GND in the ground plane. Similar regulation should be applied to analog traces and components with respect to the GNDA as well. Figure 1 illustrates the aforementioned regulation.

In Figure 1, the digital component C and the traces that connect to it overlap with the GNDA layout in the ground plane. This may cause some of the digital signaling current and return paths to pass through the analog domain and induce noise in this noise-sensitive domain.

Figure 1 describes how a mixed signal device, such as a SmartFusion cSoC device, should be placed on the board.

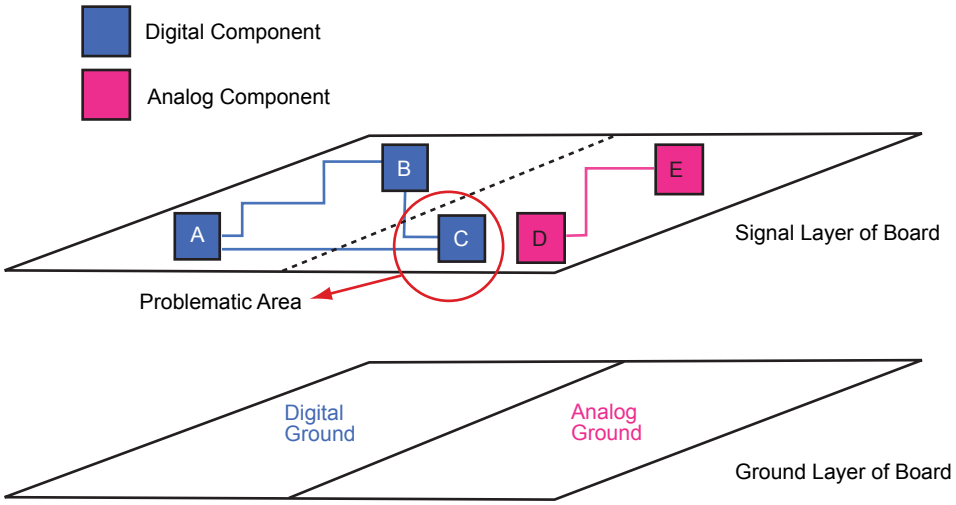

Figure 1 • **Illustration of Analog and Digital Components Placement on Board**

Placement of SmartFusion cSoC Device on Board

SmartFusion cSoC devices contain both analog and digital components and can interface with other digital and analog components on the board.

A SmartFusion cSoC device should be placed on board such that the analog signaling of the system falls within the boundaries of the analog ground and supply domain. Similarly, digital signaling of the system should fall within the boundaries of the digital domain. Figure 2 on page 3 shows a simple illustration of the placement of a SmartFusion cSoC device on the board.

As shown in Figure 2, the SmartFusion chip is placed on the boundary of analog and digital domains, so that the analog pins of the Fusion device are within the analog ground domain and the digital portion of the chip is placed within the digital ground domain.

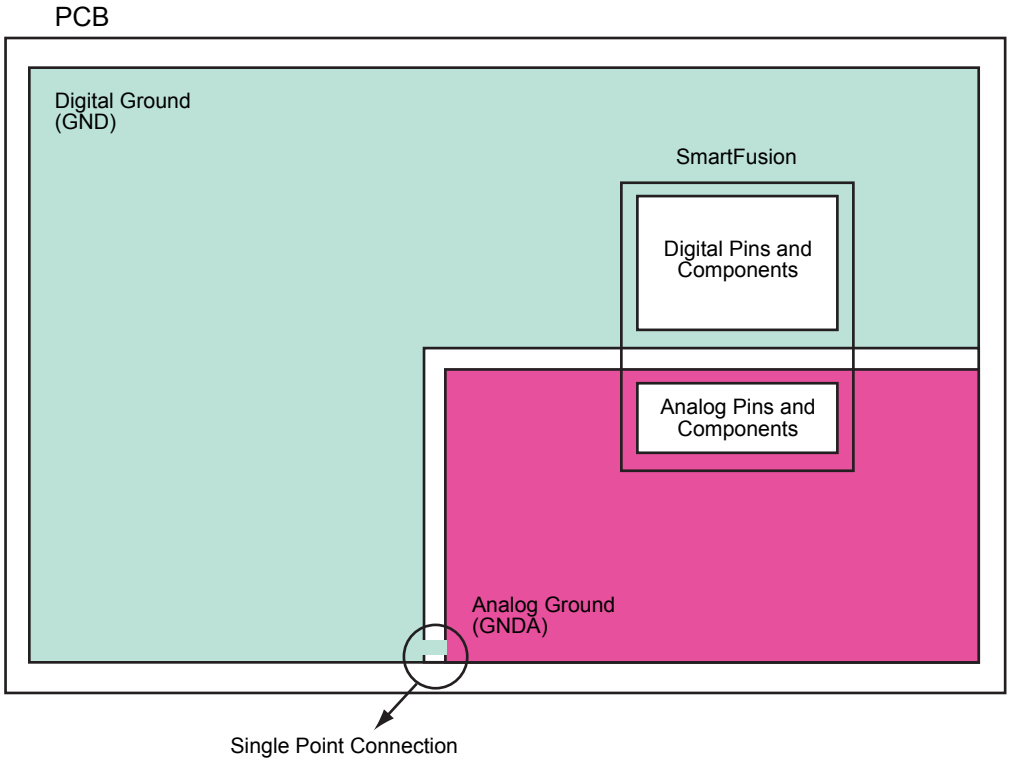

Figure 2 • **Simple Illustration of SmartFusion cSoC Device Placement on Boards**

In complicated system designs and more complicated device packages, the placement of a SmartFusion cSoC device may not be as straight forward as shown in the simplified diagram of Figure 2. However, in any board layout, it is critical to keep digital signals and their return paths well isolated from the analog domain. The "Isolation of Ground Planes" section discusses an example of SmartFusion cSoC device placement and ground plane layout in a real-world mixed signal system design.

Figure 2 also shows that the GND and GNDA are to be connected to each other at a single point. The layout of the ground planes, as well as the power supply planes, plays a key role in reducing the noise and hence enhances the performance and accuracy of the system.

Isolation of Ground Planes

As mentioned in the "Placement of SmartFusion cSoC Device and Isolation of Ground Planes" section on page 2, the ground and supply planes should be divided in two main domains: GND and GNDA. Though there is no technical limitation in implementing more ground and supply domains for other necessary ground and supply pins of a SmartFusion cSoC device, the rest of the ground and supply pins can be connected to one of the aforementioned domains.

The components and signaling in each of the two domains should remain within the boundaries of each ground as discussed in the "Placement of SmartFusion cSoC Device and Isolation of Ground Planes" section on page 2, and Figure 1 on page 2 describes how a mixed signal device, such as a SmartFusion cSoC device, should be placed on the board. However, since data and control signals usually exchange between different domains, a common connection between GND and GNDA is needed to ensure that the two planes are at the same potential. Connection between two grounds should be made only through a single point as shown in Figure 2. More than a single connection point between two grounds can result in inter-domain current paths that can induce noise from one domain to another. Furthermore, the single point connection should be as far as possible from the SmartFusion cSoC device.

Figure 3 shows a real-world example of a ground plane layout and the relative placement of the SmartFusion chip. Refer to the "Analog and Digital Plane Isolation" section on page 1 for board layout recommendations.

Figure 3 • **Example of Ground Plane Layout and SmartFusion cSoC Device Placement**

Note: Blue = GND; Yellow = VCCI; and Green = GNDA.

Other ground pins of the SmartFusion cSoC device can connect to one of the two grounds using traces on the board if necessary. However, the length of the traces should be kept as short as possible to reduce the trace inductance between ground pins and the ground plane. Table 1 lists all the ground pins of a SmartFusion cSoC device and the ground plane that they connect to.

Table 1 • **Ground Pin Connections to Ground Plate on Board**

Ground Pin Name	Ground Domain
GND	Digital
GNDQ	Digital
GNDENVM	Digital
GNDRCOSC	Digital
VCOMPLAx	Analog*
GNDA	Analog
GNDAQ	Analog
GND15ADC	Analog
GND33ADC	Analog
GNDLPXTAL	Analog
GNDMAINXTAL	Analog
GNDSDD	Analog
GNDVAREF	Analog

**If VCOMPLAx is not used it should still be grounded.*

Analog and Digital Voltage Supply Isolation

Digital and analog voltage supplies should be isolated from each other similar to the grounds as discussed in the "Placement of SmartFusion cSoC Device and Isolation of Ground Planes" section on page 2. There are four main power supplies to SmartFusion cSoC devices: VCC33A (3.3 V analog supply), VCC15A (1.5 V analog supply), VCC (1.5 V digital core supply), and VCCI (digital I/O supply). There may be multiple VCCI levels (for digital I/Os) since SmartFusion cSoC devices offer multiple I/O banks. Regardless of the number of power supply voltage levels, the layout of the board's power plans should conform to the same specifications as recommended for the ground plane in the "Placement of SmartFusion cSoC Device and Isolation of Ground Planes" section on page 2.

None of the digital power domains should overlap with the analog power supply domains (VCC33A and VCC15A). This ensures that digital signaling and its return paths are well isolated from the analog power supply, minimizing noise in the analog domain. Figure 4 shows a simple illustration of mixed signal board layers and relative layout of the digital and analog domains.

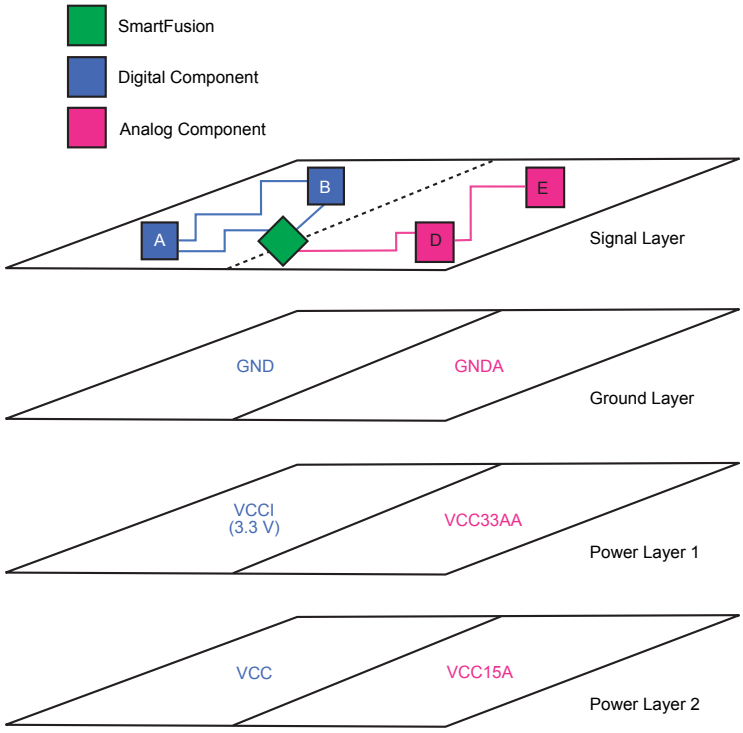

Figure 4 • **Simplified Illustration of a Mixed Signal Board Stack Up**

As shown in Figure 4, no digital grounds or digital voltage supplies overlap with the analog domain. The power planes in the Figure 4 board stack up follow the same layout as the ground plane. The SmartFusion cSoC device is placed on the boundary of the digital and analog domains as recommended in the "Placement of SmartFusion cSoC Device and Isolation of Ground Planes" section on page 2. Digital planes may be split if needed to accommodate additional supplies. For example, the VCCI plane can be split into 3.3 V and 2.5 V planes. The addition of another plane just to support the additional supply is typically not needed. Additionally, Figure 4 emphasizes the layout of the signal traces in the signal layers of the board stack up. The digital signal traces are laid out within the digital domain and the analog traces are contained within the analog area of the layer.

Other power pins of the SmartFusion cSoC device can connect to one of the two domains using traces on the board. However, the length of the traces should be kept as short as possible to reduce the trace inductance between power pins and the power plane, induced by board traces, to a minimum. Figure 2 on page 3 shows that the GND and GNDA are to be connected to each other at a single point. The same technique should be applied to digital and analog supplies.

Table 2 lists all the power pins of a SmartFusion cSoC device and the power plane that they connect to.

Table 2 • **Power Pin Connections to Power Plane on Board**

Supply Pin Name	Supply Domain	Supply Voltage Level	Handling When Unused
VCC	Digital	1.5 V	Powered all the time
VCCENVM	Digital	1.5 V	Powered all the time
VCCRCOSC[1]	Digital	3.3 V	Powered all the time
VCCMSSIOBx[1]	Digital	3.3 V	Grounded if IO Bank x is unused
VCCFPGAIOBx[2]	Digital	1.5 V	Grounded if IO Bank x is unused
VCCPLLx	Analog (connect recommended capacitors)	1.5 V	Powered all the time
VCC15A	Analog	1.5 V	Powered all the time
VCC15ADC	Analog	1.5 V	Powered all the time
VCC33A	Analog	3.3 V	Powered all the time
VCC33ADC	Analog	3.3 V	Microsemi® recommends that you connect to a 3.3 V supply.[3]
VCC33AP	Analog	3.3 V	Can be left floating or connect to VCC33A
VCC33SDD0	Analog	3.3 V	Floating or connect to VCC33A if DAC0 is unused
VCC33SDD1	Analog	3.3 V	Floating or connect to VCC33A if DAC1 and DAC2 are unused
VCCLPXTAL	Analog	3.3 V	Powered all the time
VCCMAINXTAL	Analog	3.3 V	Grounded if unused

Notes:

1. *Can be tied to any digital 3.3 V rail available in the application board (for example, VCCFPGAIOBx if the bank requires a 3.3 V supply).*
2. *If multiple banks are powered with different supply levels, different VCCI planes are needed for each voltage level.*
3. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*

Similar to any other board-level designs, decoupling/bypass capacitors or other power supply filtering techniques should be used between power supply pins and the ground to reduce any potential fluctuation on the supply lines. The SoC Products Group recommends that a 33nH inductor can be placed between the supply source and a 0.1 uF capacitor to filter out any low-/medium- and high-frequency noise for the VCCRCOSC supply input. For additional recommendations in using decoupling capacitors, refer to the *Board-Level Considerations* application note. There are numerous other industry publications and guidelines available on the subject.

PLL Power Supply Decoupling Scheme

The phase-locked loop (PLL) core is designed to tolerate noise levels on the PLL power supply as specified in the datasheets. When operated within the noise limits, the PLL will meet the output peak-to-peak jitter specifications specified in the datasheets. User applications should always ensure that the PLL power supply is powered from a noise-free or low-noise power source.

However, if the PLL power supply noise level is higher than the tolerable limits, various decoupling schemes can be designed to suppress noise to the PLL power supply. An example is provided in Figure 5. The VCCPLx and VCOMPLx pins correspond to the PLL analog power supply and ground.

Microsemi recommends that two ceramic capacitors (10 nF in parallel with 100 nF) be placed close to the power pins (less than 1 inch away). A third generic 10 µF electrolytic capacitor is recommended for low-frequency noise and should be placed farther away due to its large physical size.

Microsemi recommends that a 6.8 µH inductor be placed between the supply source and the capacitors to filter out any low-/medium- and high-frequency noise. In addition, the printed circuit board (PCB) layers should be controlled so the VCCPLx and VCOMPLx planes have the minimum separation possible, thus generating a good quality radio frequency (RF) capacitor.

For more recommendations, refer to the Board-Level Considerations application note.

Recommended 100 nF capacitor:

- Ceramic 100 nF, 16 V, 10%, X7R, 0603

Recommended 10 nF capacitor:

- Ceramic 10 nF, 50 V, 10%, X7R, 0603

Recommended 6.8 µH Inductor:

- Unshielded surface mount inductor, maximum saturation current, 30 MHz resonant frequency

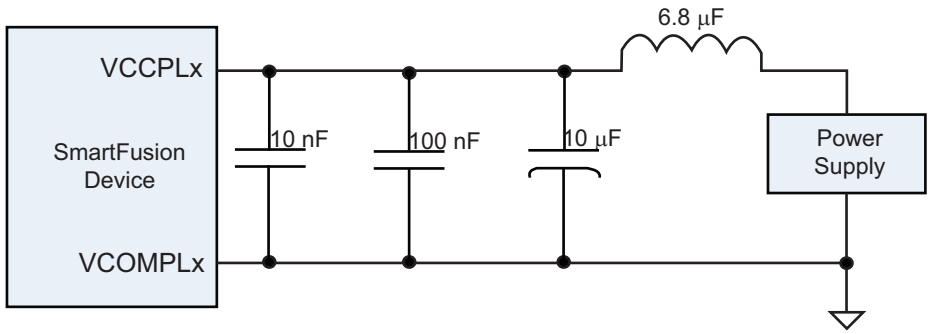

Figure 5 • **The VCCPLx and VCOMPLx pins Correspond to the PLL Analog Power Supply and Ground**

Other Special Function Pins

In addition to the general power and ground pins discussed in the "Analog and Digital Plane Isolation" section on page 1, there are a few other special pins that require special board considerations to ensure proper functionality of the SmartFusion cSoC device. This section of the document lists these pins and describes their connectivity in the board-level design.

VAREFx

There are up to three pins: VAREF0, VAREF1, and VAREF2 that provide the voltage reference for SmartFusion's analog-to-digital converter (ADC). VAREF2 is available only in the A2F500 device. The SmartFusion cSoC device can be configured to generate a 2.56 V internal reference that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREFOUT pin for use as a system reference.

When VAREF0 is internally generated, a bypass capacitor must be connected from this pin to GNDA. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual design. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. The choice of the capacitor value has an impact on the settling time of the VAREF0 signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF0 to achieve 2.56 V will be shorter than when selecting the larger capacitor value.

Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. The choice of capacitor values also depends on the total amount of noise existing on the user's board. Boards with relatively higher noise levels may need to have capacitor values close to 22 µF. On the other hand, the VAREF pin may not perform as expected if the capacitor values are close to 3.3 µF. Refer to the ADC section in the *SmartFusion Programmable Analog User's Guide* for more information.

The SoC Products Group recommends using 10 µF as the value of the bypass capacitor. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input on the PCB. For example, VAREFOUT can be connected to VAREF0 only, if ADC0 alone is used. VAREFOUT can be connected to VAREF1 only, if ADC1 alone is used. VAREFOUT can be connected to VAREF2 only, if ADC2 alone is used. VAREFOUT can be connected to VAREF0, VAREF1, and VAREF2 together, if ADC0, ADC1, and ADC2 all are used.

If a different reference voltage is required, it can be supplied using an external source between the corresponding VAREFx pin and GNDVAREF pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. Designers choosing to use an external VAREFx need to ensure that a stable and clean VAREFx source is supplied to the VAREFx pin before initiating conversions by the ADCx.

Since VAREF is the reference voltage for the ADC, it is critical for VAREF (either internal or external) to be very clean. Noise on VAREF affects the accuracy of the ADC and may cause the analog system to operate outside the specification listed in the *SmartFusion Customizable System-on-Chip (cSoC)* devices datasheet. For internal VAREF use model, the SoC Products Group recommends the external capacitor to be placed between VAREF and the analog ground, as close as possible to the VAREF pin. If these VAREF and VAREFOUT pins are not used, then these can be left floating.

VCC33N, PCAP, and NCAP

These three pins are associated with the -3.3 V charge pump. This charge pump uses two external capacitors in order to generate the -3.3 V supply. One capacitor is connected between the NCAP and PCAP pins, while the other is connected between VCC33N and the analog ground. The impulse charging of the capacitors, while the charge pump is in operation, is a source of electromagnetic interference (EMI). To reduce EMI, each of these capacitors consists of a 0.1 µF ceramic capacitor in parallel with a tantalum capacitor. The ceramic capacitors should be mounted as close as possible to the pins, using capacitors of small physical size. For the BGA package, these capacitors are to be mounted on the bottom layer, directly underneath the respective pins. The tantalum capacitors can be mounted a little further off, but you should try to minimize the distance. Ceramic capacitors are also available in higher values such as 2.2 µF. If such a capacitor is used, the 0.1 µF capacitor might not be needed. If the analog block is not used, then these pins can be left floating.

MAINXIN and MAINXOUT

MAINXIN is an input from an external crystal, ceramic resonator, or RC network, while MAINXOUT is an output to the same crystal. When using an external crystal or ceramic resonator, external capacitors are recommended, which will depend on the crystal oscillator manufacturer. If using an external RC network or clock input, MAINXIN should be used and MAINXOUT should be left unconnected.

For the layout and connection of the external crystal and the associated capacitors, keep stray capacitance and inductance to a minimum. It is very important to keep any noise from coupling to the on-chip crystal oscillator by way of power supply, the crystal, the two load capacitors, or the copper traces used to connect these components. It is also important to prevent noise from coupling from the oscillator into the analog power supply, thus affecting the performance and accuracy of other analog circuitry.

The following guidelines help achieve these objectives:

- The crystal should be placed as close as possible to the MAINXIN and MAINXOUT pins.
- The spacing between traces connecting crystal to MAINXIN and MAINXOUT pins and nearby traces should be increased beyond the minimum spacing dictated by the PCB design rules to prevent any noise from coupling into these traces. In addition, copper traces carrying high speed digital signals should not be routed in parallel to the copper traces connected to the MAINXIN and MAINXOUT pins, either on the same layer or on the other layers.
- To reduce electromagnetic emissions and provide good mechanical stability to the crystal, a copper pad slightly larger than the crystal and grounded to GNDMAINXTAL should be placed on the top layer of the PCB. The metal package of the crystal should be grounded to this pad with a suitable clip. Copper traces connected to this grounded pad and extending around the copper traces leading from the crystal to MAINXIN and MAINXOUT pins shield these pins and further increase noise immunity of the oscillator. The shields add a very small amount of stray capacitance and this can be accounted in the selection of the load capacitors.

The main crystal oscillator can be connected in two ways:

- RC-oscillator mode
- External crystal or ceramic resonator mode

In both the modes, VCCMAINXTAL is connected to 3.3 V and GNDMAINXTAL is connected to the ground. If the main crystal oscillator is not used, then both these pins can be grounded. In RC network mode, the oscillator is configured to work with an external RC network. The RC components are connected to the MAINXIN pin, with MAINXOUT left floating, as shown in Figure 6.

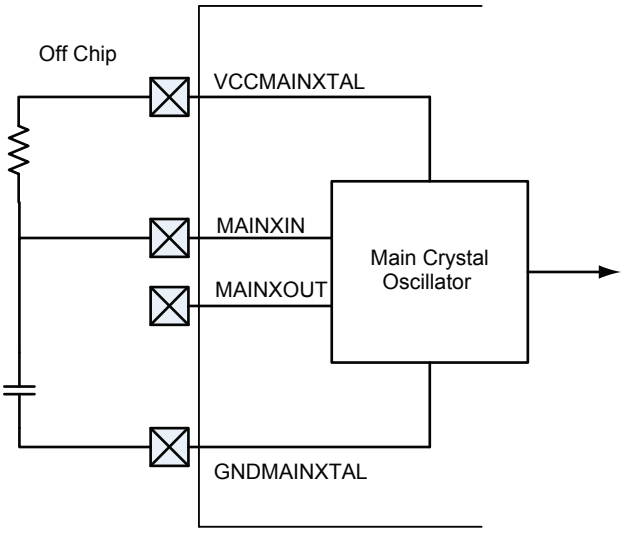

Figure 6 • **Main Crystal Oscillator in RC Network Mode**

The frequency generated by the circuit in RC Network mode is determined by the RC time constant of the selected components, as shown in Figure 7.

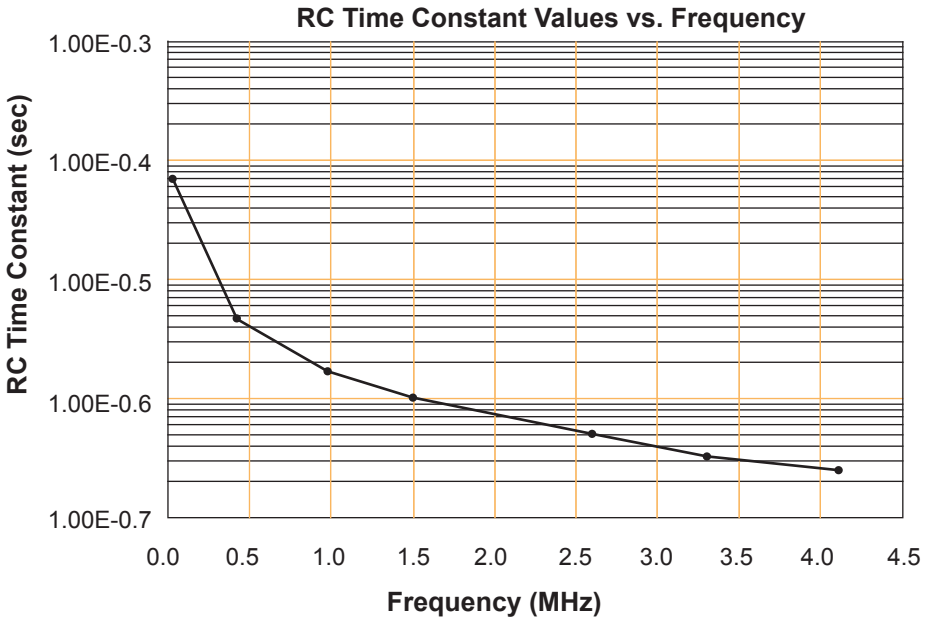

Figure 7 • **Main Crystal Oscillator RC Time Constant Versus Frequency**

The external crystal or ceramic resonator mode can be further classified into low, medium, and high gain modes based on the crystal oscillator frequency supported. The crystal or resonator is connected to the MAINXIN and MAINXOUT pins. Additionally, a capacitor is required on both MAINXIN and MAINXOUT pins to ground, as shown in Figure 8. The recommended input capacitance is 18 pF for ABM3 crystal. This capacitance value varies based on the crystal used in the design.

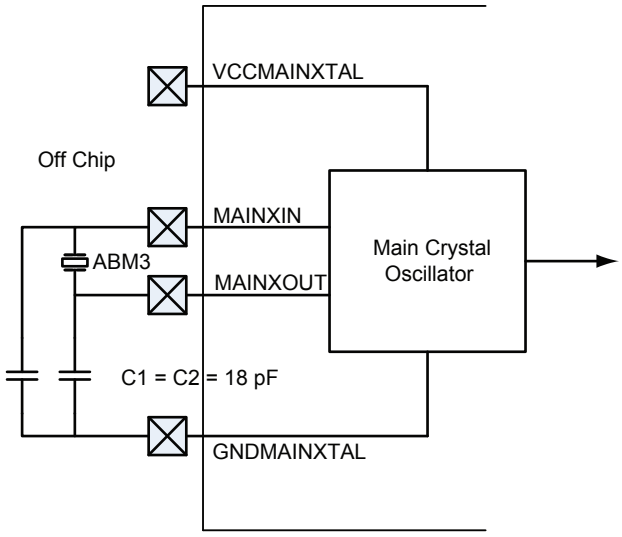

Figure 8 • **Main Crystal Oscillator in Ceramic Resonator or External Crystal Mode**

LPXIN and LPXOUT

The LPXIN is an input from a low power 32 KHz watch crystal while LPXOUT is an output to the same crystal. If not being used in the end user application, the LPXIN and LPXOUT pins can be left floating. Additionally, a capacitor is required on both LPXIN and LPXOUT pins to ground, as shown in Figure 9. The recommended input capacitance is 30 pF for a CM519 crystal. This capacitance value varies based on the crystal used in the design.

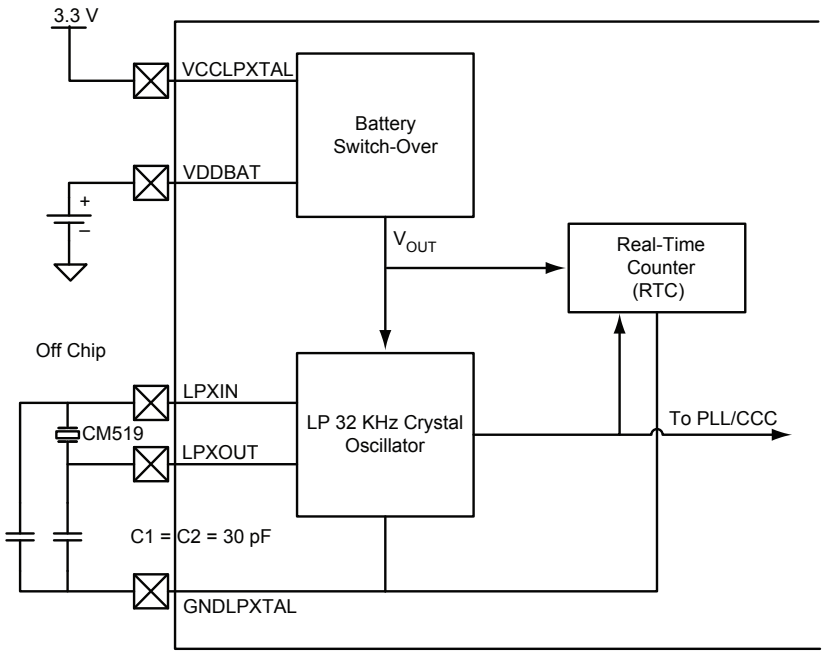

Figure 9 • **Low Power 32 KHz Oscillator with Battery Switch and RTC**

VCCLPXTAL is connected to 3.3 V and GNDLPXTAL is connected to ground in this mode. VCCLPXTAL supplies power to VRPSM block. Hence it must not be grounded, even if the low-power crystal oscillator is not used. The 32 KHz low-power crystal oscillator and the real-time counter (RTC) can be powered externally by a CR2032 type of lithium coin cell. As seen in Figure 9, a battery switch-over circuit is integrated into the SmartFusion cSoC device to switch between the main power and the battery. More information on this battery switch-over circuit can be obtained from the *SmartFusion Microcontroller Subsystem User's Guide*. Just like in the main crystal oscillator, the low-power crystal oscillator also should be placed such that noise is not coupled into the analog power supply. The three guidelines shown for MAINXIN and MAINXOUT can be applied for LPXIN and LPXOUT as well.

PTBASE and PTEM

PTBASE is the control signal of the 1.5 V internal voltage regulator. This pin should be connected to the base of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used. This output can source up to 20 mA into the pass transistors base. The output current of the circuit depends on the current gain of the NPN pass transistor connected externally.

PTEM is the feedback input of the voltage regulator. This pin should be connected to the emitter of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used. Microsemi SoC Products Group recommends using the transistors listed below with the internal voltage regulator. The collector and emitter of the pass transistor must be treated as power pins which have a current handling capacity of up to 500 mA. The pass transistor connection to the PTBASE and PTEM pins are depicted in Figure 10 on page 12.

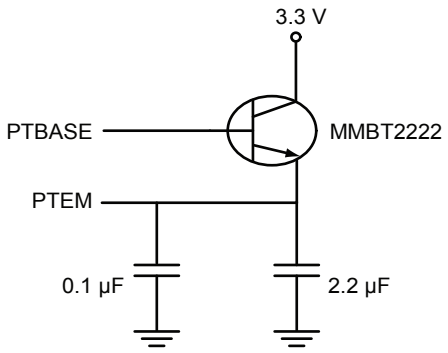

Figure 10 • **Pass Transistor Connection to PTBASE and PTEM**

External Pass Transistor Selection

The external pass transistor is selected based on the parameters as package and thermal resistance. Typical thermal resistance values are considered as per Table 3 from part datasheet.

Typical Thermal Resistance Value

Table 3 • **Typical Thermal Resistance Value**

Part	Package	Thermal Resistance	Unit
BCP55	SOT-23	θJ_A = 83.3	°C/W
MMBT222A	SOT-223	θJ_A = 357.1	°C/W
PZT2222A	SOT-223	θJ_A = 83.3	°C/W

Thermal resistance (θ) is a degree of heat radiation mentioned in the following equation:

θ = (T1-T2)/P (°C/W), where P(W) is the heat producing quantity, T1(°C) is the maximum junction temperature of the die, and T2(°C) is the ambient temperature.

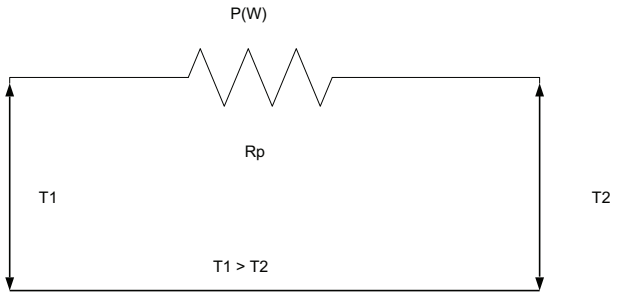

Figure 11 • **Thermal Resistance**

θJ_A is the thermal resistance between IC chip (junction point) and ambience.

Thermal Considerations

The factors that determine the temperature of the die are total power dissipation, package thermal resistance, ambient temperature, and airflow. These factors must be managed to stay below the maximum junction temperature of the die.

The total power dissipation of the pass transistor (P) can be calculated if the thermal resistance (θJ_A) value of the package is provided.

The equation below shows the maximum power dissipation (P) that can be achieved by a given package. Exceeding this power budget would result in reliability issues on the part of the die of the package, as per equation:

$P = (Tj - Ta)/ \theta J_A$

As an example of the thermal analysis procedure in design, transistor PZT2222AT1 is considered.

- Thermal resistance of SOT-223 θJA = 83.3 °C/W
- Junction Temperature = 150 °C
- Ambient temperature = 85 °C

The maximum power dissipation, Pd = (150 °C - 85 °C) / (83.3 °C/W) = 780 mW.

Redundant Information

From the above equations calculated for pass transistor power dissipation, one can calculate the total current of A2F 1.5 V current (Ipass) as per the equation:

Maximum Id current = Pd / Vce

- Pd: Maximum power dissipation for a given package
- Vce: Max Pass Transistor Collector-to-Emitter Voltage

Based on the above:

Ipass = 780 mW / (3.45-1.5) V = 400 mA

Based on the above calculation, you can conclude that a maximum current of 400 mA can be sourced using the PZ2222A device in the SOT-223 package. If the required current is greater than 400 mA, then either a heat sink should be used or a different package/device with a lower thermal resistance should be identified.

Recommendations

You are advised to select appropriate packages based on the thermal calculations shown above, so that the maximum junction temperature does not exceed absolute maximum rating or add provision for adding a heat sink on the device.

PU_N

PU_N is the connection for the external momentary switch that can be used to turn on the 1.5 V voltage regulator. This pin can be left floating if it is not used. The PU_N connection to the external switch is depicted in Figure 12.

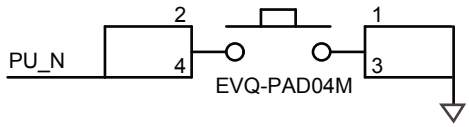

Figure 12 • **PU_N Connection to External Switch**

GNDTM[m]

The GNDTM[m] pins are the return path for the TM[n] pins that are used in temperature monitor applications. Each GNDTM pin acts as a return path for one or two TM pins. The GNDTM[m] should not be connected to ground since there are chances that the temperature monitor accuracy could be sensitive to board level noise. There are three different scenarios in which this pin can be used. The below scenarios make use of TM0 and TM1 pins with GNDTM0 as their common return path. Similar connections can be made for the other temperature monitor pins TM2, TM3, and TM4.

Scenario 1: When either TM0 or TM1 is used for temperature measurement while the other is used for direct current measurement or not used at all. In this case, the connections are done as shown in Figure 13.

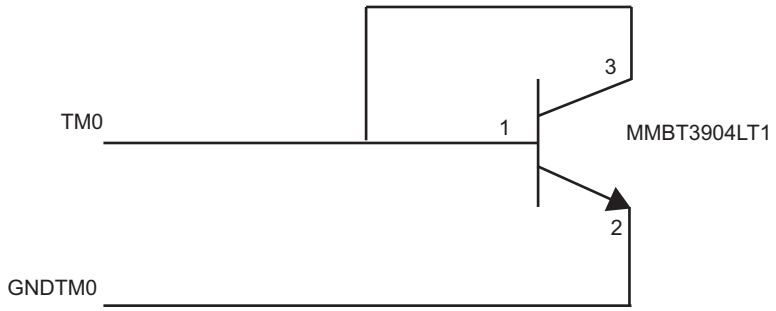

Figure 13 • **TM0 is used for Temperature Measurement**

Scenario 2: When both TM0 and TM1 are used for temperature measurement. In this case, the connections are done with the GNDTM0 being connected as a common return path for both TM0 and TM1 as shown in Figure 14.

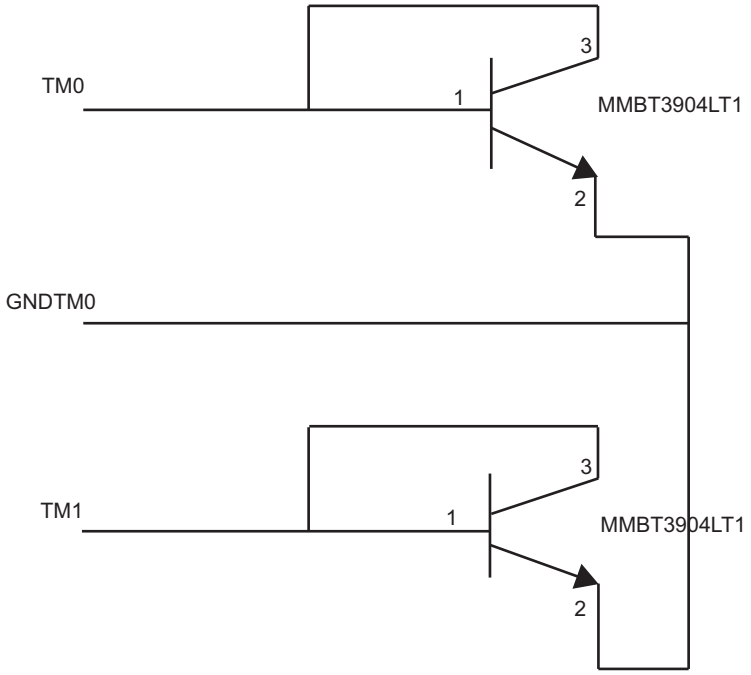

Figure 14 • **TM0 and TM1 are used for Temperature Measurement**

Scenario 3: When both TM0 and TM1 are used for direct current measurement or not used at all. In either case the GNDTMx pin can be left floating. If temperature monitor is not used, the ADC multiplexer (MUX) will not select the internal temperature monitor output (the internal TM[n] opamp output) to the input of the ADC. For this reason, whatever the TM input be, it will not be sampled by the ADC, but will only sample what the TM pin is configured to.

Application-Specific Recommendations

This section of the document discusses some recommendations that are specific to temperature, voltage, or current monitoring applications. These recommendations are merely for improving the accuracy of the applications.

Temperature Monitor

The temperature monitor generates a voltage of about 2.5 mV/K (per degree Kelvin), as seen by the ADC. However, the voltage change that appears across the external discreet bipolar transistor may be much smaller. Such low levels mean that precautions should be taken to avoid coupling noisy signals to the conductors connecting the transistor to the temperature monitor pins.

If the temperature sensing diode/transistor is connected to a SmartFusion cSoC device through cables, the SoC Products Group recommends using a twin lead shielded cable to carry the TM[n] and GNDTM[m] traces with the shield of the cable grounded at the board. If the connections are made by copper traces on the PCB, TM[n] and GNDTM[m] traces should be routed in such a way that traces carrying digital signal are not parallel to them above, below, or on the sides. To achieve this, lay the TM[n] and GNDTM[m] traces on the top layer, so that the next adjacent layer in the PCB stack is the ground layer. This provides for shielding against digital signals that can couple to the signals on the copper traces connected to the TM[n] and GNDTM[m] pins.

If the digital signal carrying traces cannot be avoided in the vicinity of the traces connecting to the transistor, sufficient distance is to be created between the offending trace and the TM[n] and GNDTM[m] traces. It is important to minimize the resistance of the conductors connecting the external discrete bipolar transistor to the TM[n] and GNDTM[m] pins of the SmartFusion chip. If PCB copper traces are used as the interconnecting conductors, they should be of such a width that, taking into account their length, they contribute only a negligible voltage drop compared to 200 µV. The current through the bipolar transistor used for sensing the temperature changes by 90 µA during the measurement process. This current, multiplied by the total resistance of the copper trace from the TM[n] pin to the transistor and from the transistor back to the GNDTM[m] pin, should be negligible compared to 200 µV. If a shielded cable is used, the wire gauge of its conductors should be appropriately selected. If the system using the SmartFusion cSoC devices is to be operated at other than room temperature, the effect of temperature on the resistance of the wire or copper traces should also be taken into account.

Voltage and Current Monitor

If any of the AV channels are used in the direct mode that is directly connecting to the ADC without prescalers, it is recommend that a ceramic capacitor of the NPO or COG variety, or better yet, a polyester capacitor of 2200 pF be placed from the corresponding AV channel pin to the analog ground, and as close as possible to the AV pin. A resistor of 100 O should then be connected between the AV pin and whatever point is being monitored by the particular AV channel. If the accuracy requirements are not stringent, one may be able to get by without using the above mentioned resistor/capacitor combination. However, it is good practice to at least make provisions for these components on the prototype PCB. Also note that if the prescalers are not used then 2.56 V is the maximum that can be seen at the AV, AC, and AT pins. The ADC is a switched capacitor design and needs to be driven from low impedance. It draws a charging current every time a channel is sampled, and the capacitor helps to maintain the voltage steady at the particular AV pin during such intervals. All copper traces connecting to the AV, AT, or the AC pins should stay within the area covered by the analog ground plane. The power for the ADC, voltage and current monitors, and the internal voltage reference is provided from the same pins. These pins are to be adequately decoupled with 0.1 µF ceramic X7R dielectric capacitors in parallel with a tantalum capacitor of 22 µF capacity.

In applications using current monitor, it is important to route the AT and AC signals of each channel in parallel and keep the two traces matched as much as possible. Large differences in the nets bringing AT and AC signals to the device may cause significant inaccuracy in differential voltage across the AT and AC pin. While measuring current, the current flow should be from AC to AT as shown in Figure 15.

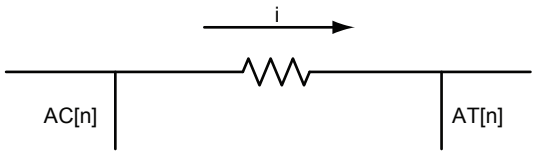

Figure 15 • **Current Flow Direction while Measuring Current**

In current monitor applications, the current sense resistor should be chosen carefully so that optimal accuracy and resolution can be achieved. The *SmartFusion Programmable Analog User's Guide* describes the recommended resistor values for various current ranges.

Connection to PLL

Table 1 on page 4 and Table 2 on page 6 describe the connections of the VCCPLA/B and VCOMPLA/B pins of the SmartFusion cSoC device to the power and ground planes. This section of the document discusses how these pins and the dedicated clock pins of the SmartFusion cSoC device connect to the PLLs on the chip.

Connecting external signals into PLL and powering them up should be done considering that A2F060 and A2F200 devices contain only one PLL, while A2F500 FG484 package device contain two PLL blocks. Note that A2F500 FG256 package does not have the FAB PLL and hence has only one PLL. In A2F060, A2F200, and A2F500 FG256 package devices, the PLL is located on the west side of the die. In devices with two PLLs, the second PLL is placed on east side of the die. Table 4 shows the corresponding power and ground pins for each PLL block.

Table 4 • **Power and Ground Pin Names for SmartFusion cSoC Device PLLs**

PLL/Device	A2F060	A2F200	A2F500 - FG256	A2F500-CS288/-FG484
West PLL	VCCPLA/VCOMPLA	VCCPLA/VCOMPLA	VCCPLL0/VCOMPLA0	VCCPLL0/VCOMPLA0
East PLL	–	–	–	VCCPLL1/VCOMPLA1

In addition to hardwired clock pins, SmartFusion cSoC device PLLs can be driven by any internal net or external I/O pins. Although the hardwired I/Os can be used as any user I/O, if designers are required to minimize the propagation from external clock to the PLL, hardwired clock pins of the PLL provide the shortest paths from board to PLL clock input. Table 5 lists the hardwired clock pins for each PLL on the device.

Table 5 • **Hardwired Clock Pin Connections to PLL**

PLL/Device	A2F060	A2F200	A2F500 - FG256	A2F500-CS288/-FG484
West PLL	GFA0/GFA1/GFA2*	GFA0/GFA1/GFA2*	GFA2	GFA0/GFA1/GFA2
East PLL	–	–	–	GCA0/GCA1/GCA2
*Note: *Depending on the selected package, not all three hardware clock I/Os may be available.*				

Cold Sparing

The ABPS inputs of SmartFusion supports Cold sparing feature. However, if the ABPS inputs are powered with voltages greater than 5 V when the device is not powered, the ESD circuitry on the ABPS input pin can potentially be damaged and can cause a short and permanent silicon damage. If voltages greater than 5 V are applied to the ABPS inputs when the device is not powered, to prevent possible damage to the device, Microsemi recommends adding a >1K Ohm series resistor to limit the current flowing into the ESD circuitry.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 9 (July 2014)	Added "Cold Sparing" section (SAR 47611).	16
Revision 8 (June 2014)	Modified "VAREFx" section (SAR 49718).	8
Revision 7 (December 2012)	Table 1 is updated (SAR 42924).	4
	Table 2 is updated (SAR 42924).	6
Revision 6 (October 2012)	Table 2 is updated (SAR 42182).	6
	The "PLL Power Supply Decoupling Scheme" section is new (SAR 42182).	7
Revision 5 (September 2012)	In Table 2 • Power Pin Connections to Power Plane on Board, the "handling when unused" instructions for VCC3ADC were changed to the following: "Microsemi recommends that you connect to a 3.3 V supply." A table note was added regarding connecting 3.3 V supplies together (SAR 41139).	6
Revision4 (April 2012)	The hyperlink for the *Board Level Considerations* application note (in the text beneath Table 2 • Power Pin Connections to Power Plane on Board) was corrected (SAR 38044).	6
Revision 3 (April 2011)	The first two lines of the "LPXIN and LPXOUT" section, below Figure 9 • Low Power 32 KHz Oscillator with Battery Switch and RTC, were rewritten (SAR 31447).	11
Revision 2 (February 2011)	The "PTBASE and PTEM" section was rewritten.	11
	The "External Pass Transistor Selection" section, "Thermal Considerations" section, and "Thermal Considerations" section are new.	12 to 13
Revision 1 (December 2010)	Table 2 • Power Pin Connections to Power Plane on Board was revised. (SAR 24510)	6

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

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