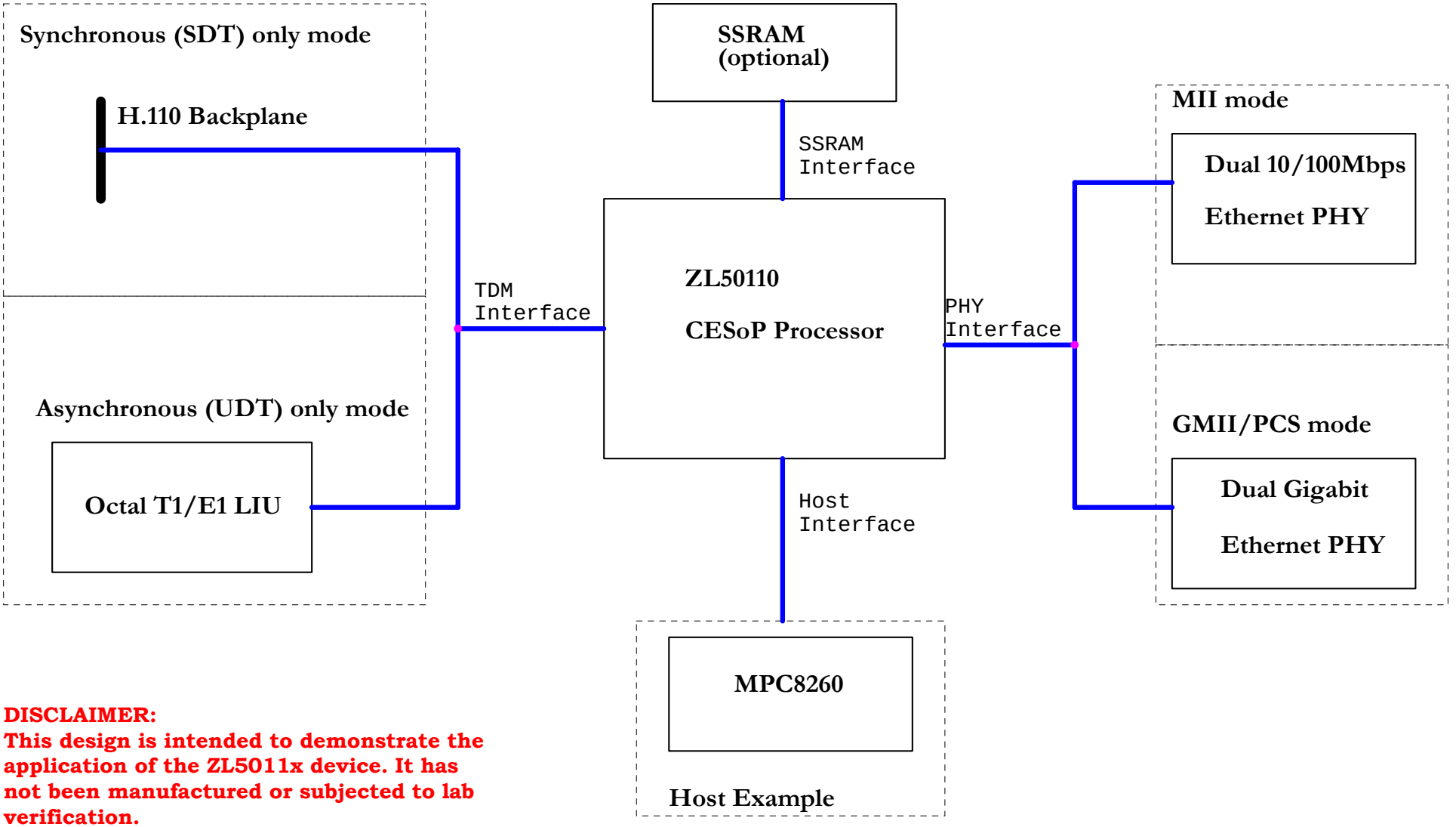

DISCLAIMER:
This design is intended to demonstrate the application of the ZL5011x device. It has not been manufactured or subjected to lab verification.

Notes:
1. Two designs are shown on TDM interface and PHY interface catering for different applications. However, at any time only one circuit should be connected.

2. The same design is applicable to the ZL50111 and the ZL50114.

ZARLINK SEMICONDUCTOR

Applications Engineering, Network Access

ZL50110 Reference Design - Block Diagram

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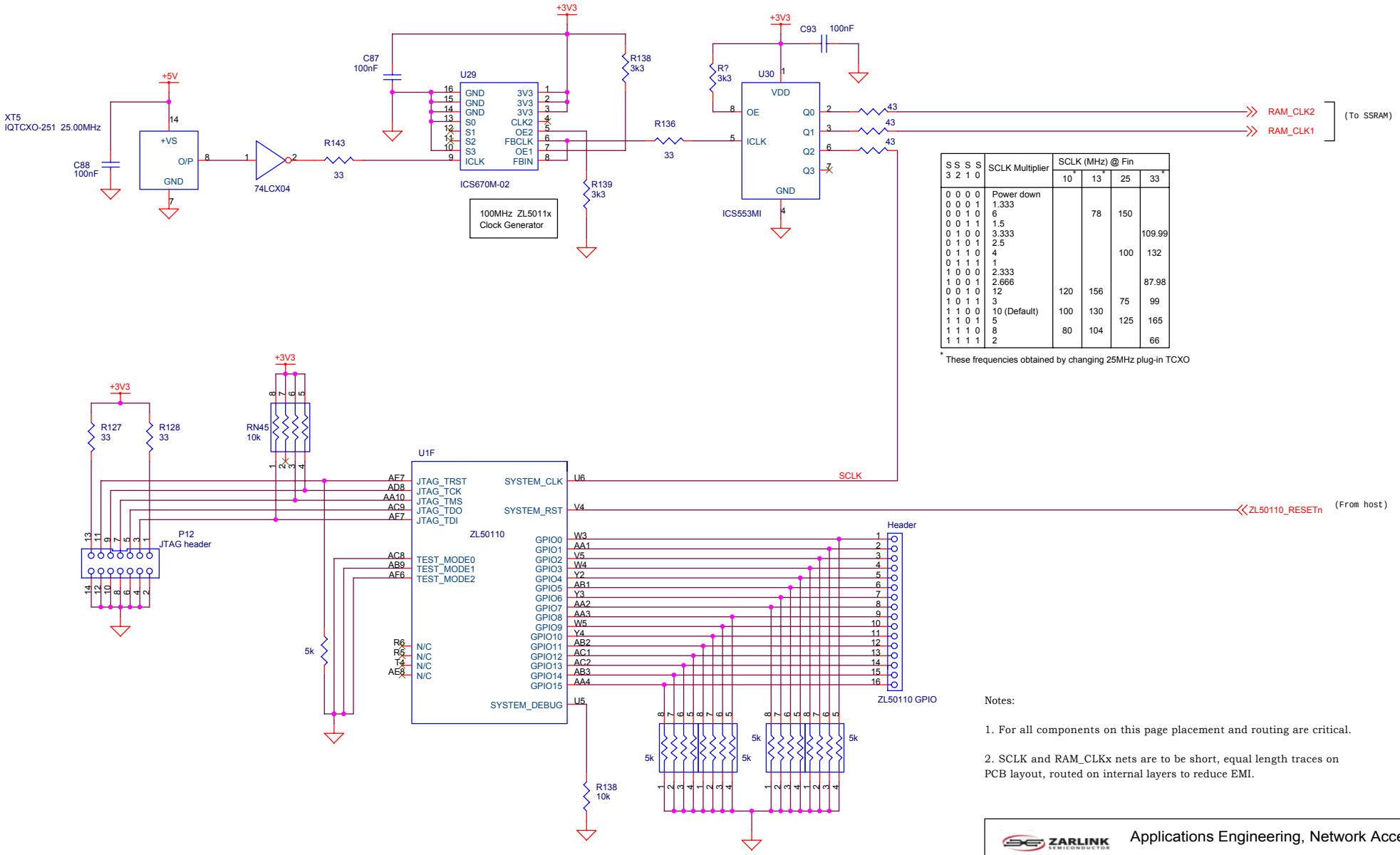

S3	S2	S1	S0	SCLK Multiplier	SCLK (MHz) @ Fin 10*	13*	25	33*
0	0	0	0	Power down				
0	0	0	1	1.333				
0	0	1	0	6		78	150	
0	0	1	1	1.5				
0	1	0	0	3.333				109.99
0	1	0	1	2.5				
0	1	1	0	4			100	132
0	1	1	1	1				
1	0	0	0	2.333				
1	0	0	1	2.666				87.98
0	0	1	0	12	120	156		
1	0	1	1	3			75	99
1	1	0	0	10 (Default)	100	130		
1	1	0	1	5			125	165
1	1	1	0	8	80	104		
1	1	1	1	2				66

* These frequencies obtained by changing 25MHz plug-in TCXO

Notes:

1. For all components on this page placement and routing are critical.

2. SCLK and RAM_CLKx nets are to be short, equal length traces on PCB layout, routed on internal layers to reduce EMI.

ZARLINK SEMICONDUCTOR

Applications Engineering, Network Access

ZL50110 Reference Design - ZL50110 Clock, GPIO and JTAG

Size: B			Revision 1.0
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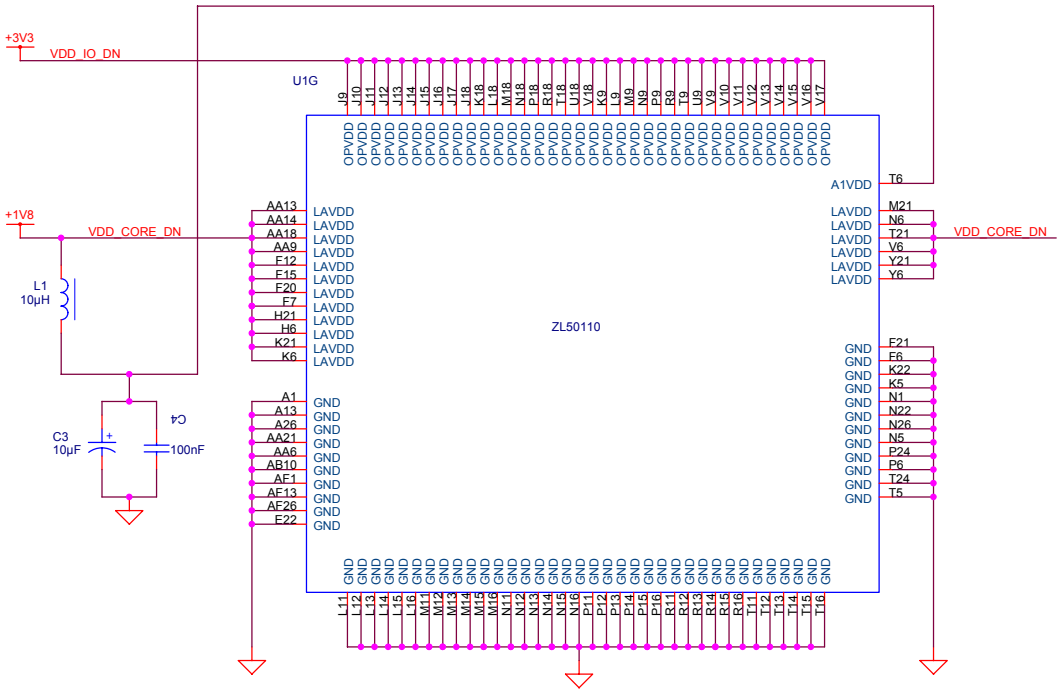
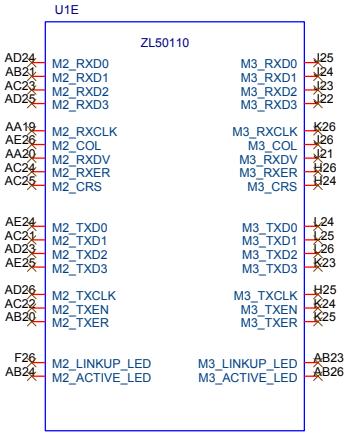
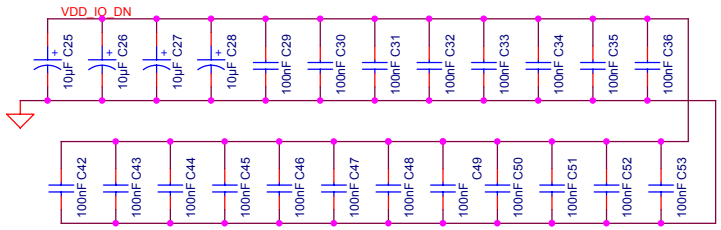
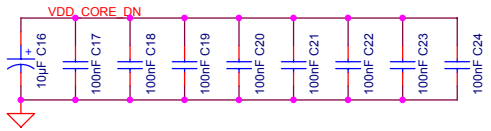




Note:
MII port 2 and port 3 are only available on the ZL50111.





ZARLINK SEMICONDUCTOR

Applications Engineering, Network Access

ZL50110 Reference Design - ZL50110 Power Supply

Size: B		Revision 1.0
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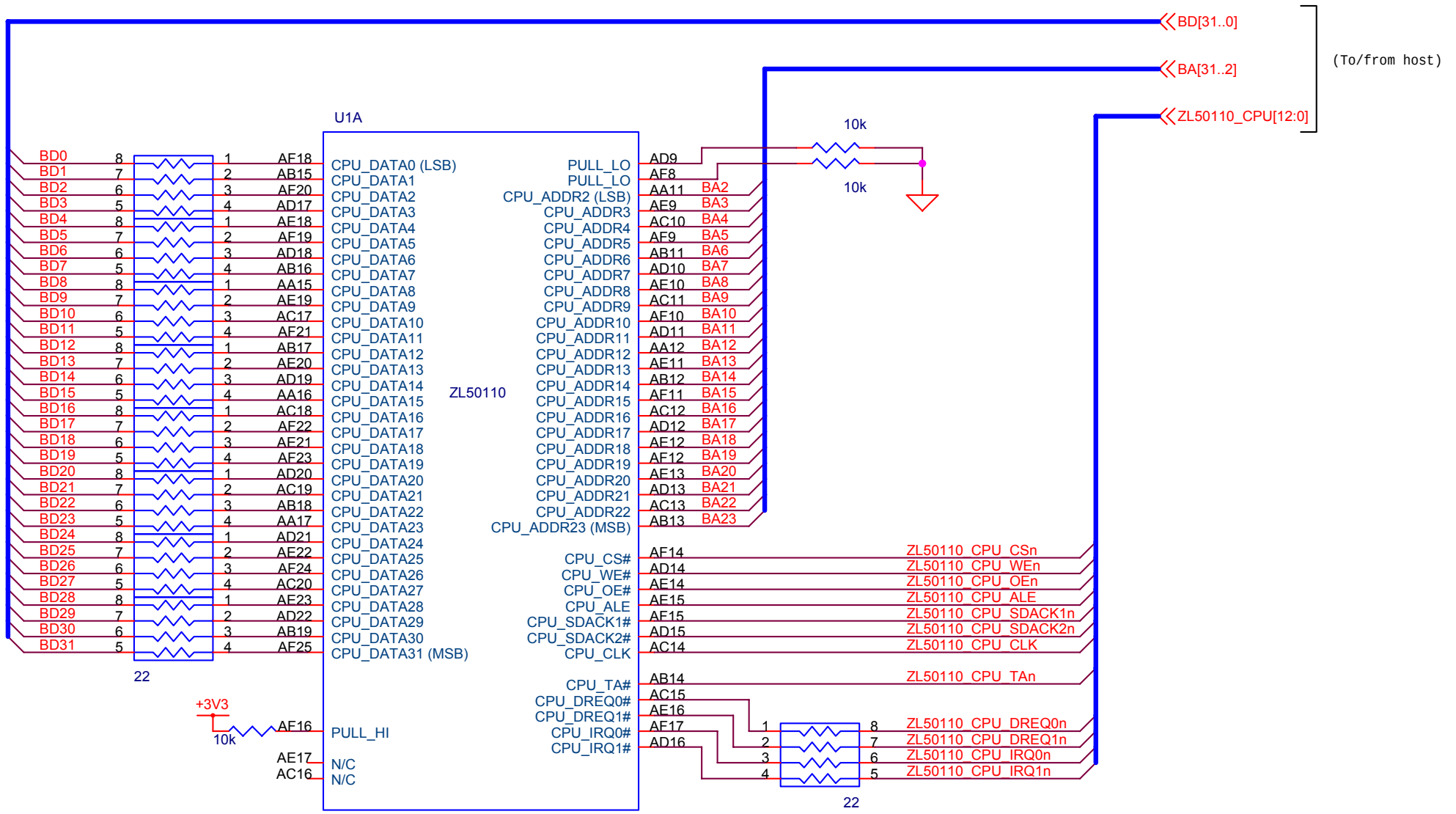

ZARLINK SEMICONDUCTOR

Applications Engineering, Network Access

ZL50110 Reference Design - ZL50110 Host Interface

Size: A		Revision 1.0
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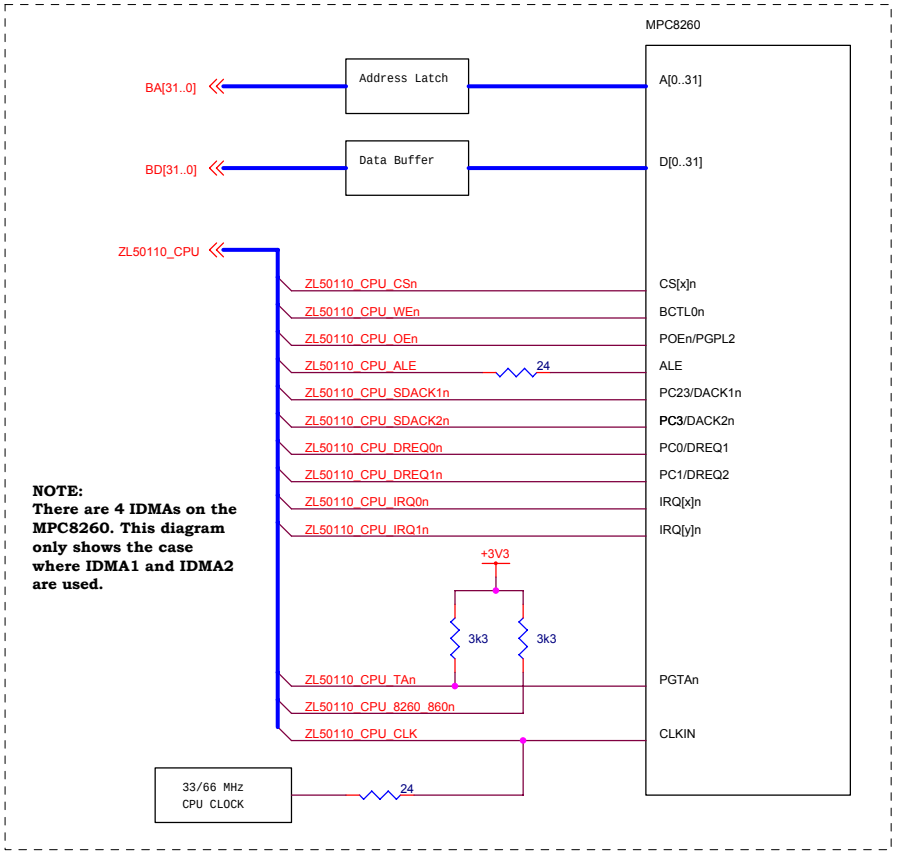

NOTES:

1. The ZL50110 can be connected to most processors as a SRAM device. Only the MPC8260 is shown here as an example.

2. The implementation of address latch, data buffer, CPU clock and CPLD control logic are application/design specific, therefore are not shown here.

ZARLINK SEMICONDUCTOR

Applications Engineering, Network Access

ZL50110 Reference Design - Host Examples

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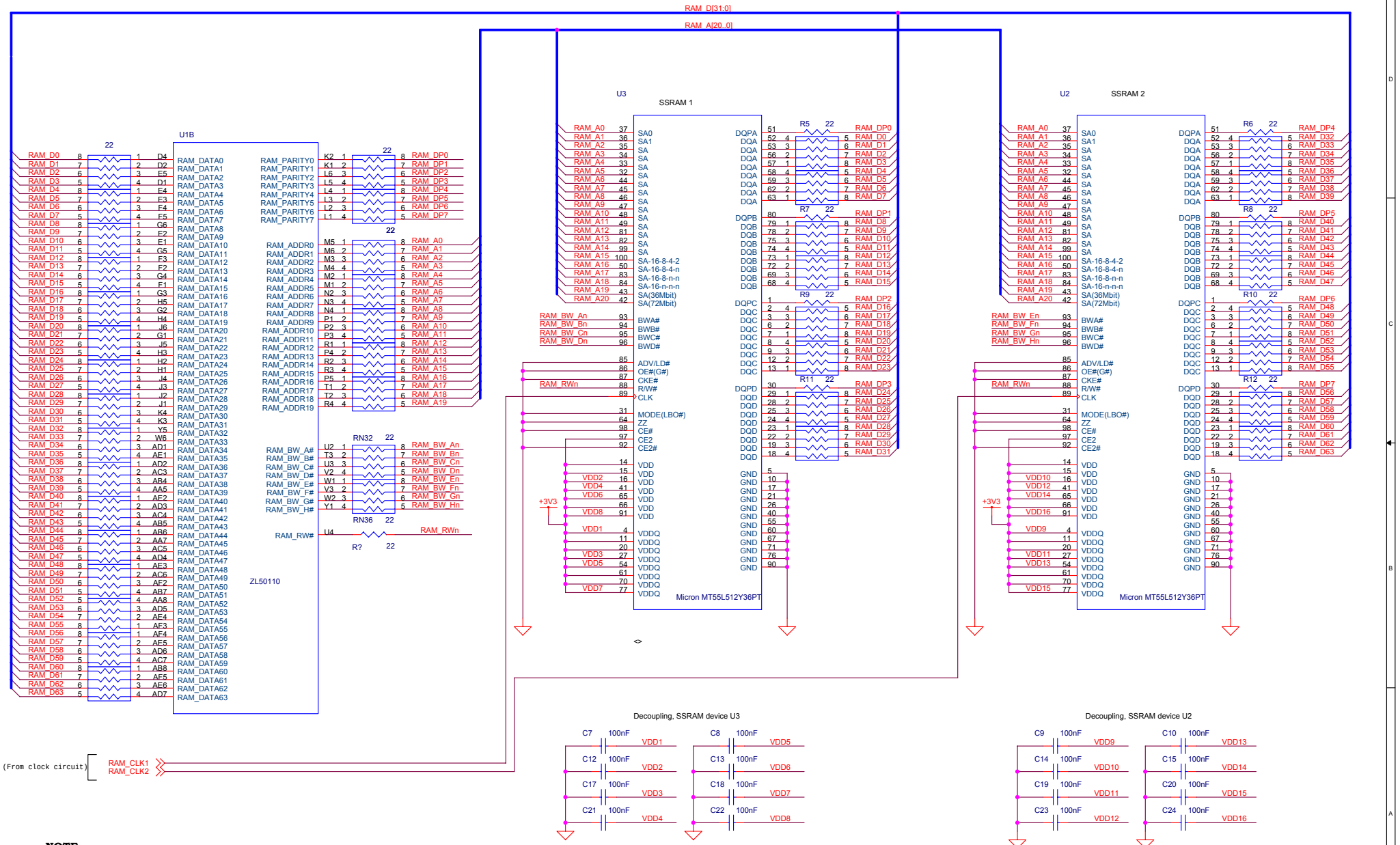

NOTE:

1. The use of SSRAM and its size are optional and application specific.

2. RAM_CLKx traces are to be matched length.

ZARLINK SEMICONDUCTOR	Applications Engineering, Network Access	
ZL50110 Reference Design - Memory Interface		
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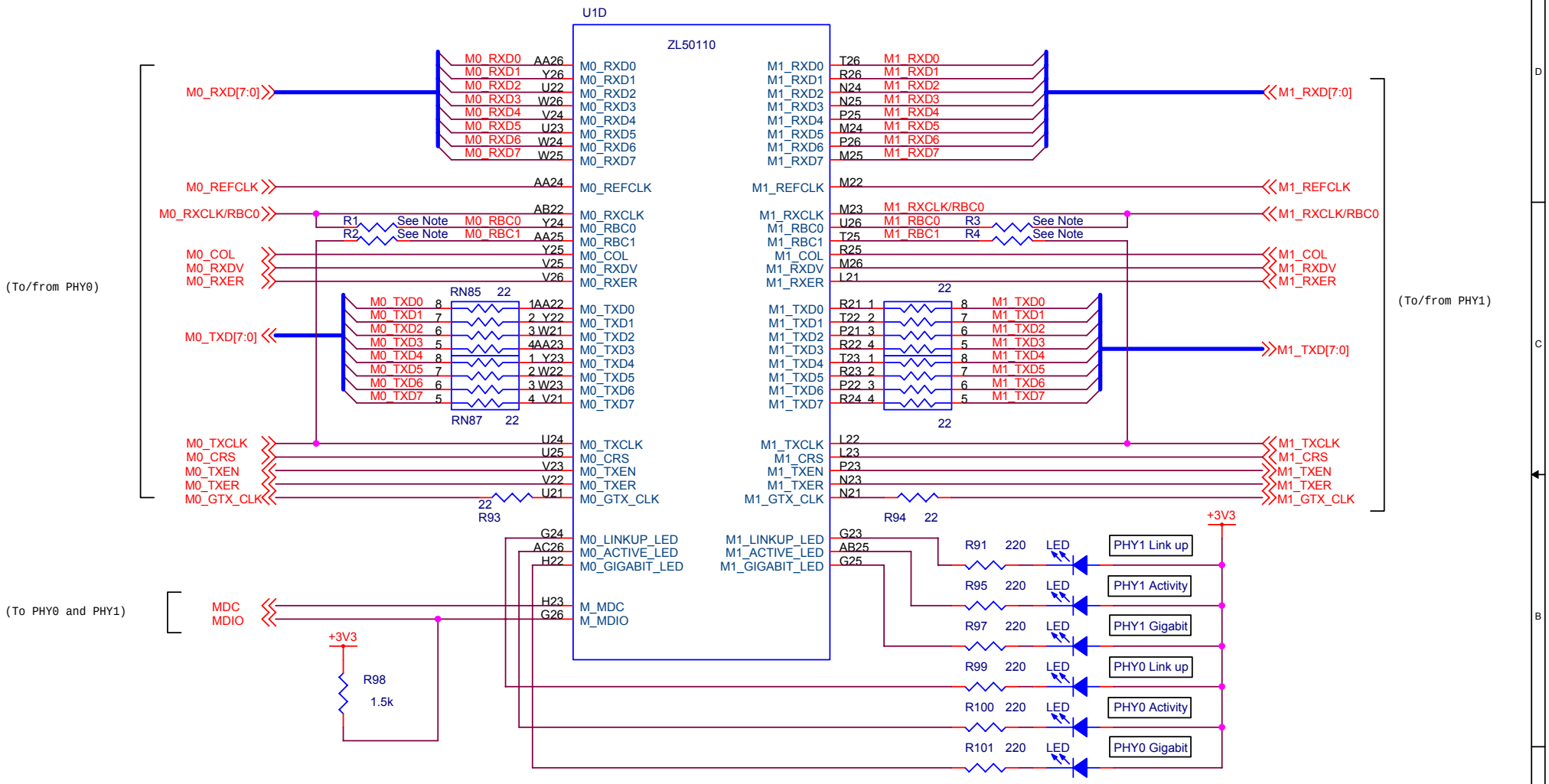

NOTE:
R1, R2, R3, R4 are populated in PCS mode only. They are not populated in MII or GMII modes.

ZARLINK SEMICONDUCTOR Applications Engineering, Network Access

ZL50110 Reference Design - ZL50110 PHY Interface

Size: A		Revision 1.0
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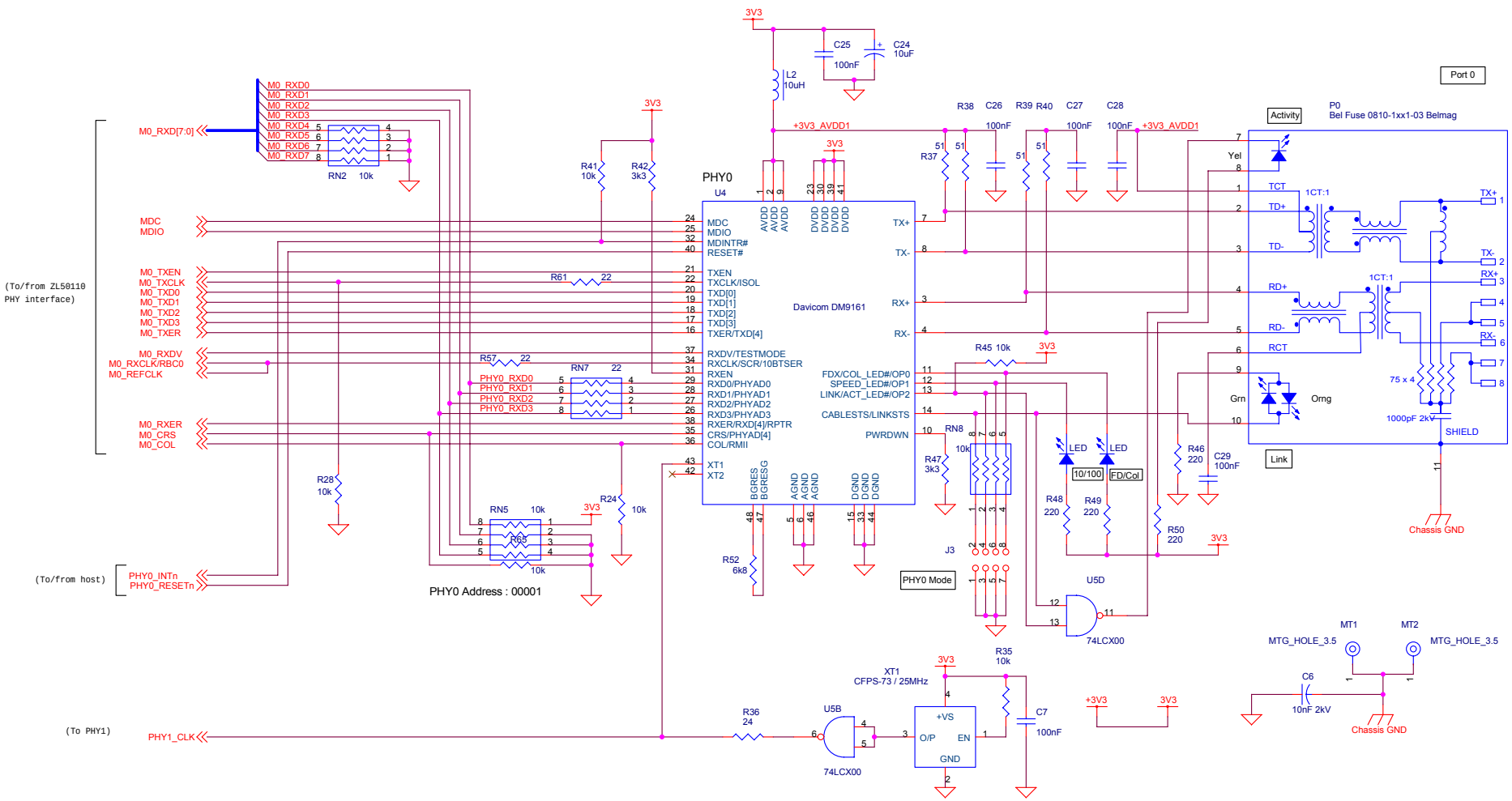
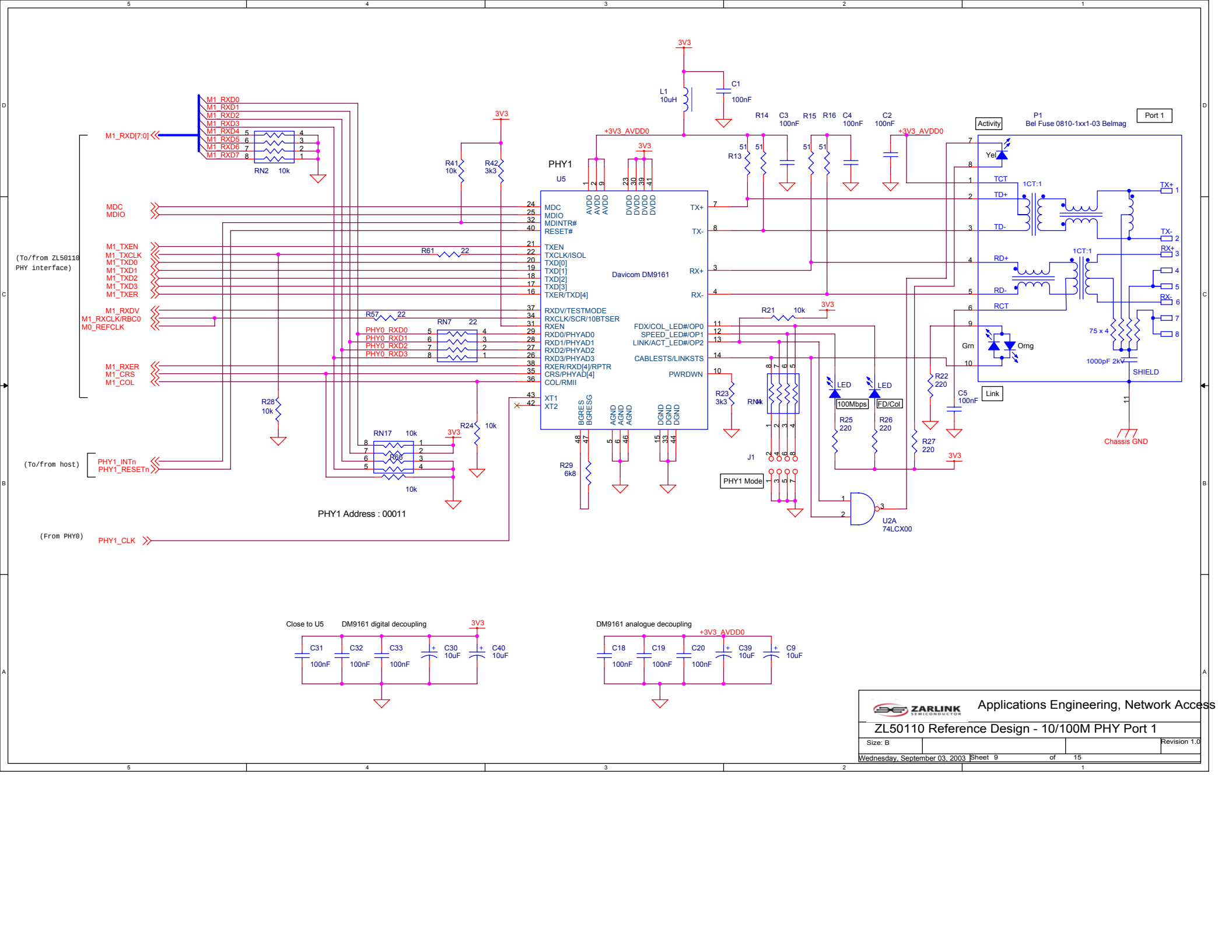

PHY0
U4
Davicom DM9161
PHY0 Address : 00001
PHY0 Mode
Port 0
P0
Bel Fuse 0810-1xx1-03 Belmag
Activity
Link
Yel
Grn
Orng
1CT:1
75 x 4
1000pF 2kV
SHIELD
Chassis GND
10/100
FD/Col
LED
74LCX00
CFPS-73 / 25MHz
MTG_HOLE_3.5
Close to U4
DM9161 digital decoupling
DM9161 analogue decoupling
(To/from ZL50110 PHY interface)
(To/from host)
(To PHY1)
ZARLINK SEMICONDUCTOR
Applications Engineering, Network Access
ZL50110 Reference Design - 10/100M PHY Port 0
Size: C
Revision 1.0
Wednesday, September 03, 2003
Sheet 8 of 15


M1_RXD[7:0]
M1_RXD0
M1_RXD1
M1_RXD2
M1_RXD3
M1_RXD4
M1_RXD5
M1_RXD6
M1_RXD7
RN2 10k
MDC
MDIO
(To/from ZL50110 PHY interface)
M1_TXEN
M1_TXCLK
M1_TXD0
M1_TXD1
M1_TXD2
M1_TXD3
M1_TXER
M1_RXDV
M1_RXCLK/RBC0
M0_REFCLK
M1_RXER
M1_CRS
M1_COL
(To/from host)
PHY1_INTn
PHY1_RESETn
(From PHY0)
PHY1_CLK
R28 10k
R24 10k
RN17 10k
R60 10k
R57 22
RN7 22
R61 22
R41 10k
R42 3k3
3V3
L1 10uH
C1 100nF
+3V3_AVDD0
PHY1
U5
Davicom DM9161
PHY0_RXD0
PHY0_RXD1
PHY0_RXD2
PHY0_RXD3
R14 C3 100nF R15 R16 C4 100nF C2 100nF
R13 51
R21 10k
R23 3k3
RN1 4k
R29 6k8
J1
PHY1 Mode
LED 100Mbps
LED FD/Col
R25 220
R26 220
R27 220
R22 220
C5 100nF
U2A 74LCX00
P1 Bel Fuse 0810-1xx1-03 Belmag
Port 1
Activity
Link
Yel
Grn
Orng
TCT
TD+
TD-
RD+
RD-
RCT
1CT:1
75 x 4
1000pF 2kV
SHIELD
Chassis GND
TX+
TX-
RX+
RX-
PHY1 Address : 00011
Close to U5
DM9161 digital decoupling
C31 100nF
C32 100nF
C33 100nF
C30 10uF
C40 10uF
DM9161 analogue decoupling
C18 100nF
C19 100nF
C20 100nF
C39 10uF
C9 10uF
ZARLINK SEMICONDUCTOR
Applications Engineering, Network Access
ZL50110 Reference Design - 10/100M PHY Port 1
Size: B
Revision 1.0
Wednesday, September 03, 2003
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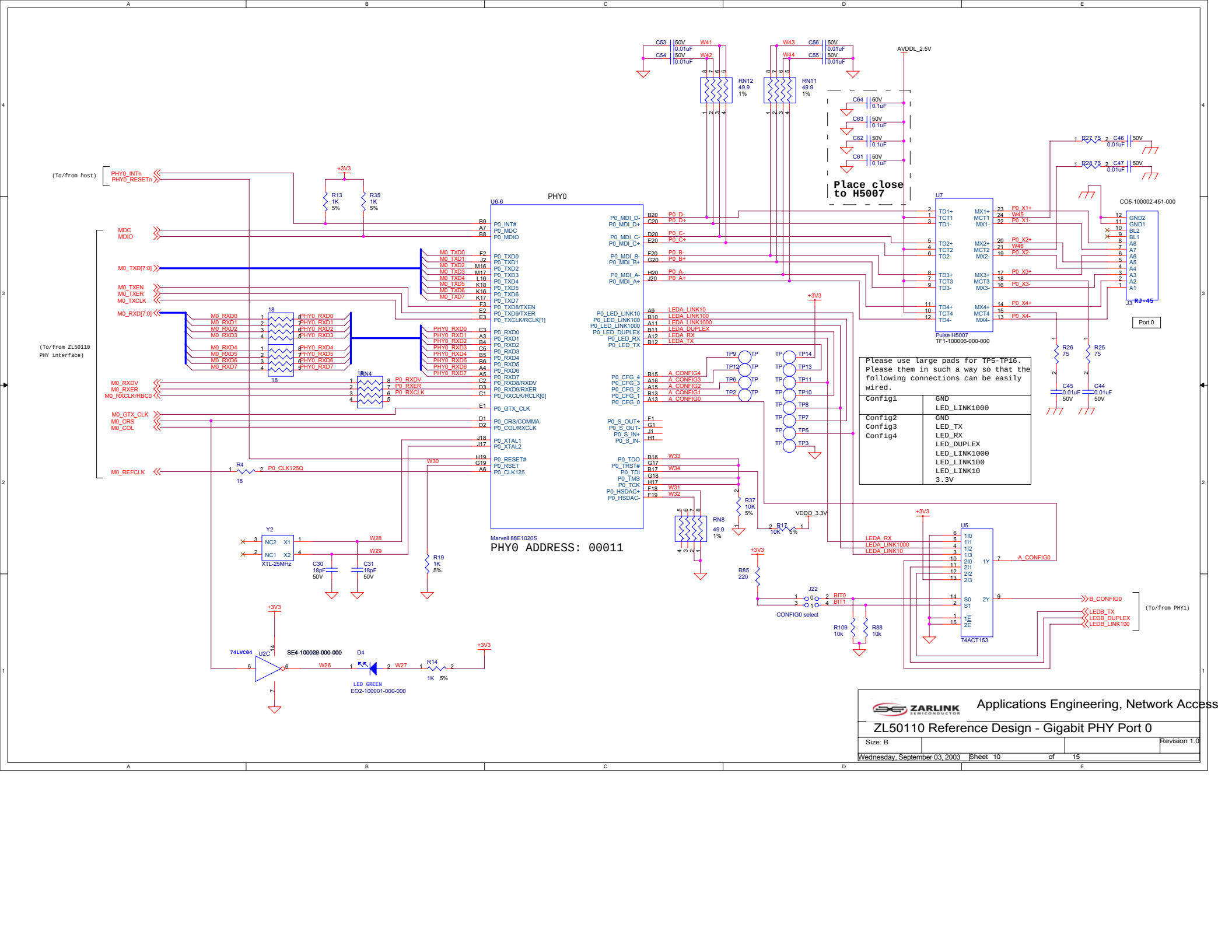
PHY0
U6-6
Marvell 88E1020S
PHY0 ADDRESS: 00011
Place close to H5007
Pulse H5007
TF1-100006-000-000
U7
U5
74ACT153
Y2
XTL-25MHz
J22
CONFIG0 select
J3
R3-45
CO5-100002-451-000
Port 0
D4
LED_GREEN
EO2-100001-000-000
U2C
74LVC04
SE4-100029-000-000
(To/from host)
(To/from ZL50110 PHY interface)
(To/from PHY1)
AVDDL_2.5V
VDDO_3.3V
+3V3
Please use large pads for TP5-TP16. Please them in such a way so that the following connections can be easily wired.
Config1 GND LED_LINK1000
Config2 Config3 Config4 GND LED_TX LED_RX LED_DUPLEX LED_LINK1000 LED_LINK100 LED_LINK10 3.3V
ZARLINK SEMICONDUCTOR
Applications Engineering, Network Access
ZL50110 Reference Design - Gigabit PHY Port 0
Size: B
Revision 1.0
Wednesday, September 03, 2003
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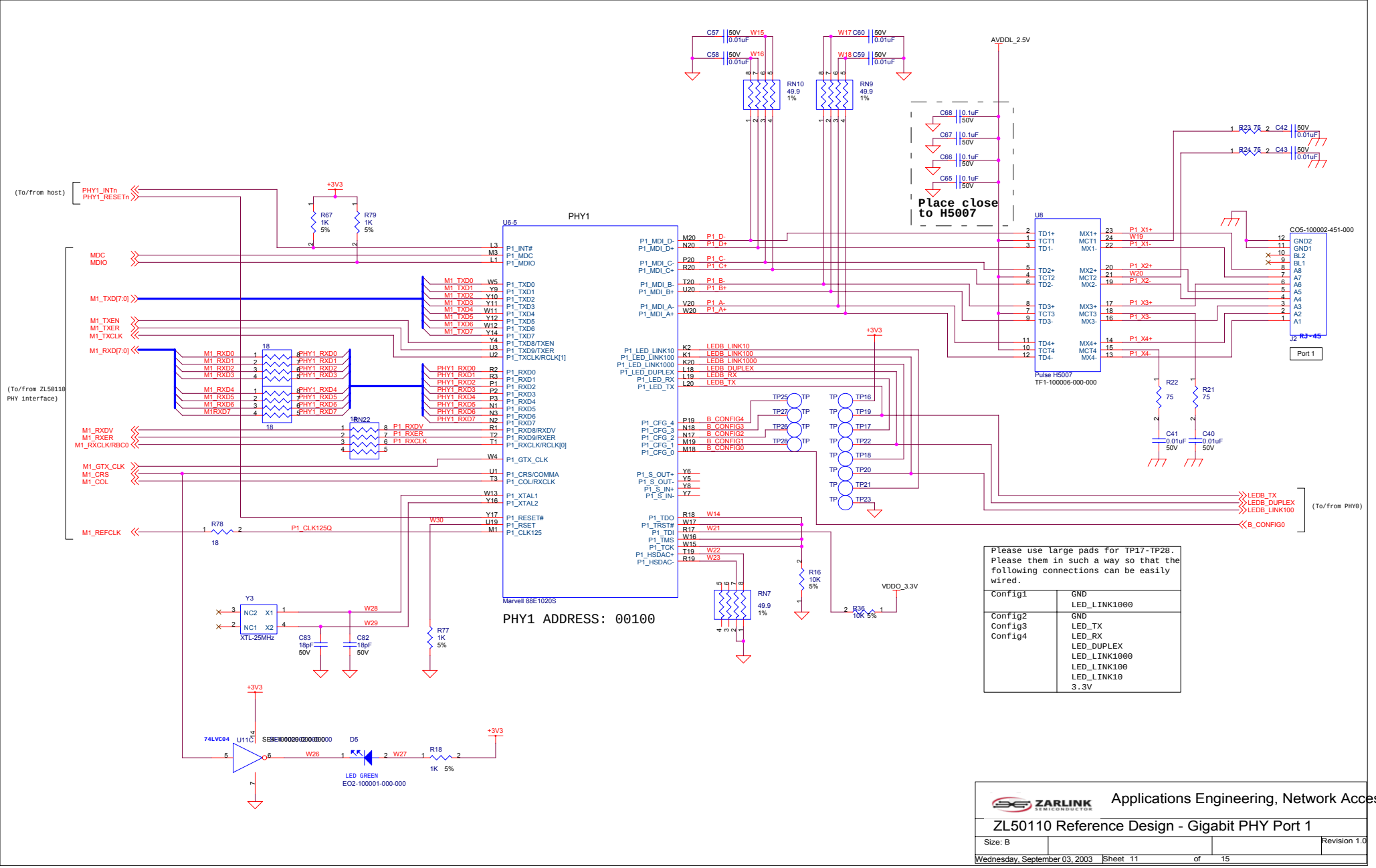
PHY1
PHY1 ADDRESS: 00100
Marvell 88E1020S
Place close to H5007
Pulse H5007
TF1-100006-000-000
CO5-100002-451-000
Port 1
XTL-25MHz
LED GREEN
EO2-100001-000-000
Please use large pads for TP17-TP28. Please them in such a way so that the following connections can be easily wired.
Config1 GND LED_LINK1000
Config2 GND
Config3 LED_TX
Config4 LED_RX
LED_DUPLEX
LED_LINK1000
LED_LINK100
LED_LINK10
3.3V
ZARLINK SEMICONDUCTOR
Applications Engineering, Network Access
ZL50110 Reference Design - Gigabit PHY Port 1
Size: B
Revision 1.0
Wednesday, September 03, 2003
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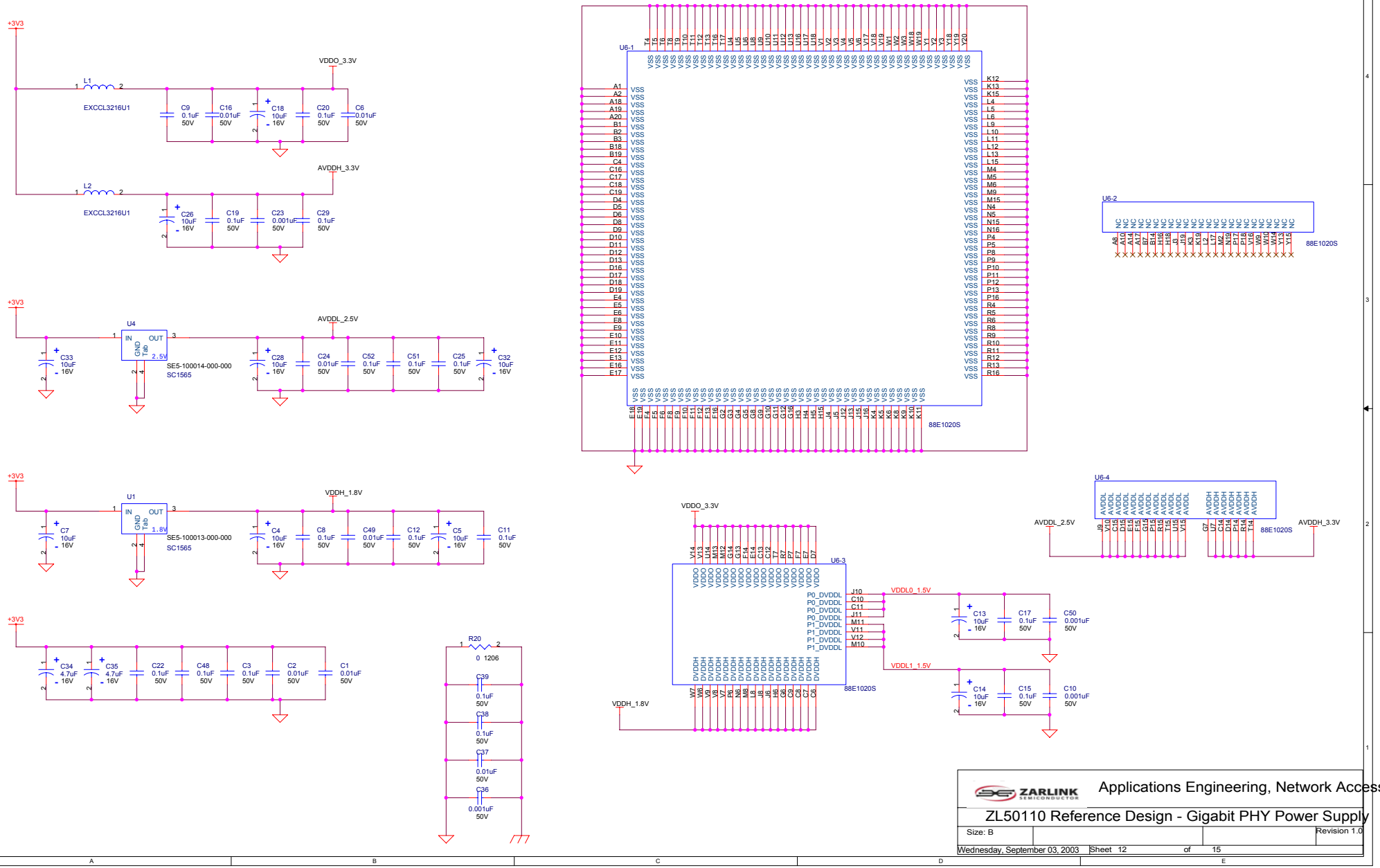

ZARLINK SEMICONDUCTOR

Applications Engineering, Network Access

ZL50110 Reference Design - Gigabit PHY Power Supply

Size: B			Revision 1.0
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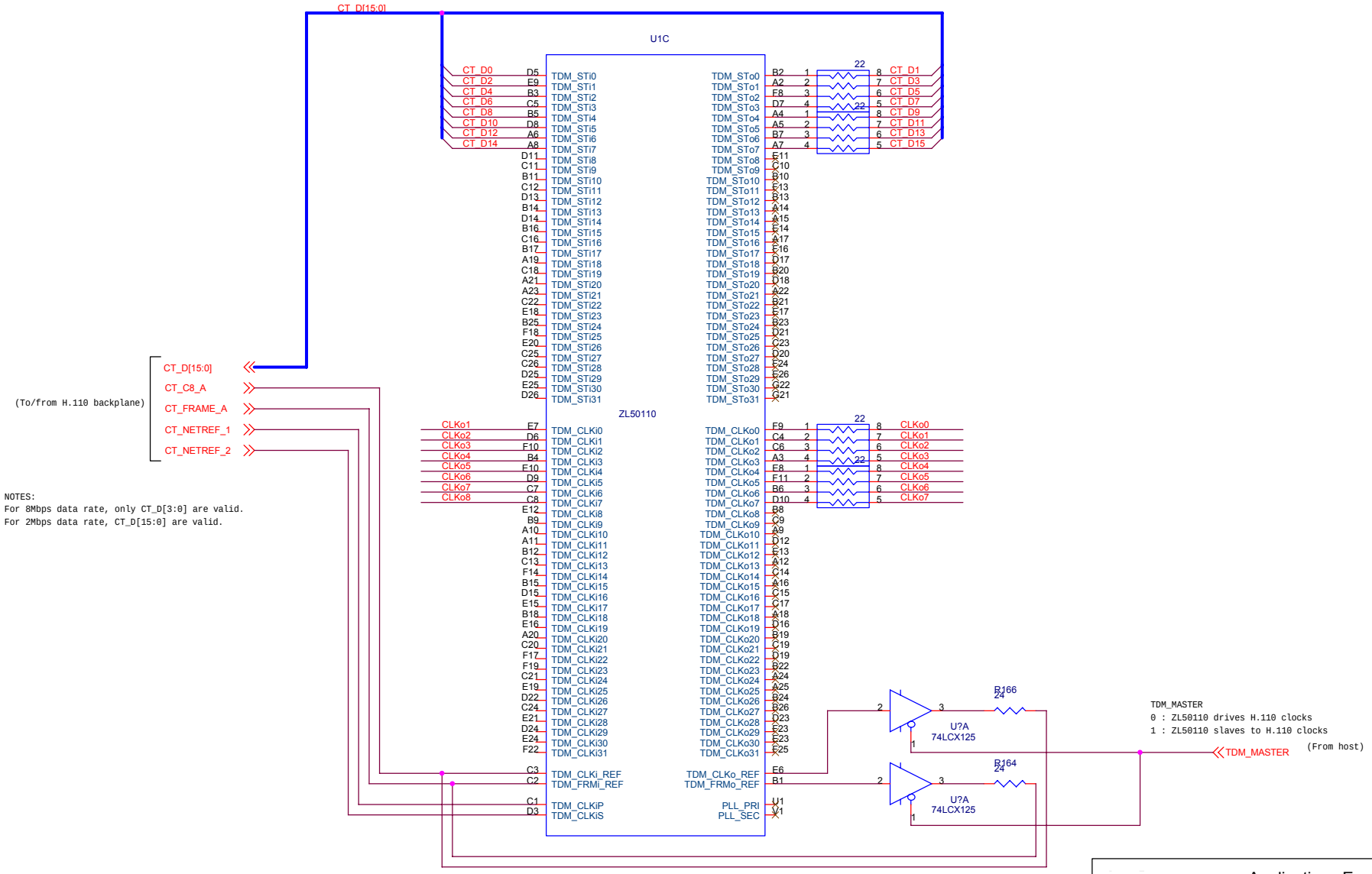
CT_D[15:0]
U1C
ZL50110
CT_D0
CT_D2
CT_D4
CT_D6
CT_D8
CT_D10
CT_D12
CT_D14
CT_D1
CT_D3
CT_D5
CT_D7
CT_D9
CT_D11
CT_D13
CT_D15
22
TDM_STi0
TDM_STi1
TDM_STi2
TDM_STi3
TDM_STi4
TDM_STi5
TDM_STi6
TDM_STi7
TDM_STi8
TDM_STi9
TDM_STi10
TDM_STi11
TDM_STi12
TDM_STi13
TDM_STi14
TDM_STi15
TDM_STi16
TDM_STi17
TDM_STi18
TDM_STi19
TDM_STi20
TDM_STi21
TDM_STi22
TDM_STi23
TDM_STi24
TDM_STi25
TDM_STi26
TDM_STi27
TDM_STi28
TDM_STi29
TDM_STi30
TDM_STi31
TDM_STo0
TDM_STo1
TDM_STo2
TDM_STo3
TDM_STo4
TDM_STo5
TDM_STo6
TDM_STo7
TDM_STo8
TDM_STo9
TDM_STo10
TDM_STo11
TDM_STo12
TDM_STo13
TDM_STo14
TDM_STo15
TDM_STo16
TDM_STo17
TDM_STo18
TDM_STo19
TDM_STo20
TDM_STo21
TDM_STo22
TDM_STo23
TDM_STo24
TDM_STo25
TDM_STo26
TDM_STo27
TDM_STo28
TDM_STo29
TDM_STo30
TDM_STo31
CT_D[15:0]
CT_C8_A
CT_FRAME_A
CT_NETREF_1
CT_NETREF_2
(To/from H.110 backplane)
CLKo1
CLKo2
CLKo3
CLKo4
CLKo5
CLKo6
CLKo7
CLKo8
CLKo0
CLKo1
CLKo2
CLKo3
CLKo4
CLKo5
CLKo6
CLKo7
TDM_CLKi0
TDM_CLKi1
TDM_CLKi2
TDM_CLKi3
TDM_CLKi4
TDM_CLKi5
TDM_CLKi6
TDM_CLKi7
TDM_CLKi8
TDM_CLKi9
TDM_CLKi10
TDM_CLKi11
TDM_CLKi12
TDM_CLKi13
TDM_CLKi14
TDM_CLKi15
TDM_CLKi16
TDM_CLKi17
TDM_CLKi18
TDM_CLKi19
TDM_CLKi20
TDM_CLKi21
TDM_CLKi22
TDM_CLKi23
TDM_CLKi24
TDM_CLKi25
TDM_CLKi26
TDM_CLKi27
TDM_CLKi28
TDM_CLKi29
TDM_CLKi30
TDM_CLKi31
TDM_CLKo0
TDM_CLKo1
TDM_CLKo2
TDM_CLKo3
TDM_CLKo4
TDM_CLKo5
TDM_CLKo6
TDM_CLKo7
TDM_CLKo8
TDM_CLKo9
TDM_CLKo10
TDM_CLKo11
TDM_CLKo12
TDM_CLKo13
TDM_CLKo14
TDM_CLKo15
TDM_CLKo16
TDM_CLKo17
TDM_CLKo18
TDM_CLKo19
TDM_CLKo20
TDM_CLKo21
TDM_CLKo22
TDM_CLKo23
TDM_CLKo24
TDM_CLKo25
TDM_CLKo26
TDM_CLKo27
TDM_CLKo28
TDM_CLKo29
TDM_CLKo30
TDM_CLKo31
TDM_CLKi_REF
TDM_FRMi_REF
TDM_CLKiP
TDM_CLKiS
TDM_CLKo_REF
TDM_FRMo_REF
PLL_PRI
PLL_SEC
NOTES:
For 8Mbps data rate, only CT_D[3:0] are valid.
For 2Mbps data rate, CT_D[15:0] are valid.
U?A
74LCX125
R166
24
R164
24
TDM_MASTER
0 : ZL50110 drives H.110 clocks
1 : ZL50110 slaves to H.110 clocks
(From host)
TDM_MASTER
ZARLINK SEMICONDUCTOR
Applications Engineering, Network Access
ZL50110 Reference Design - Synchronous TDM Interface
Size: B
Revision 1.0
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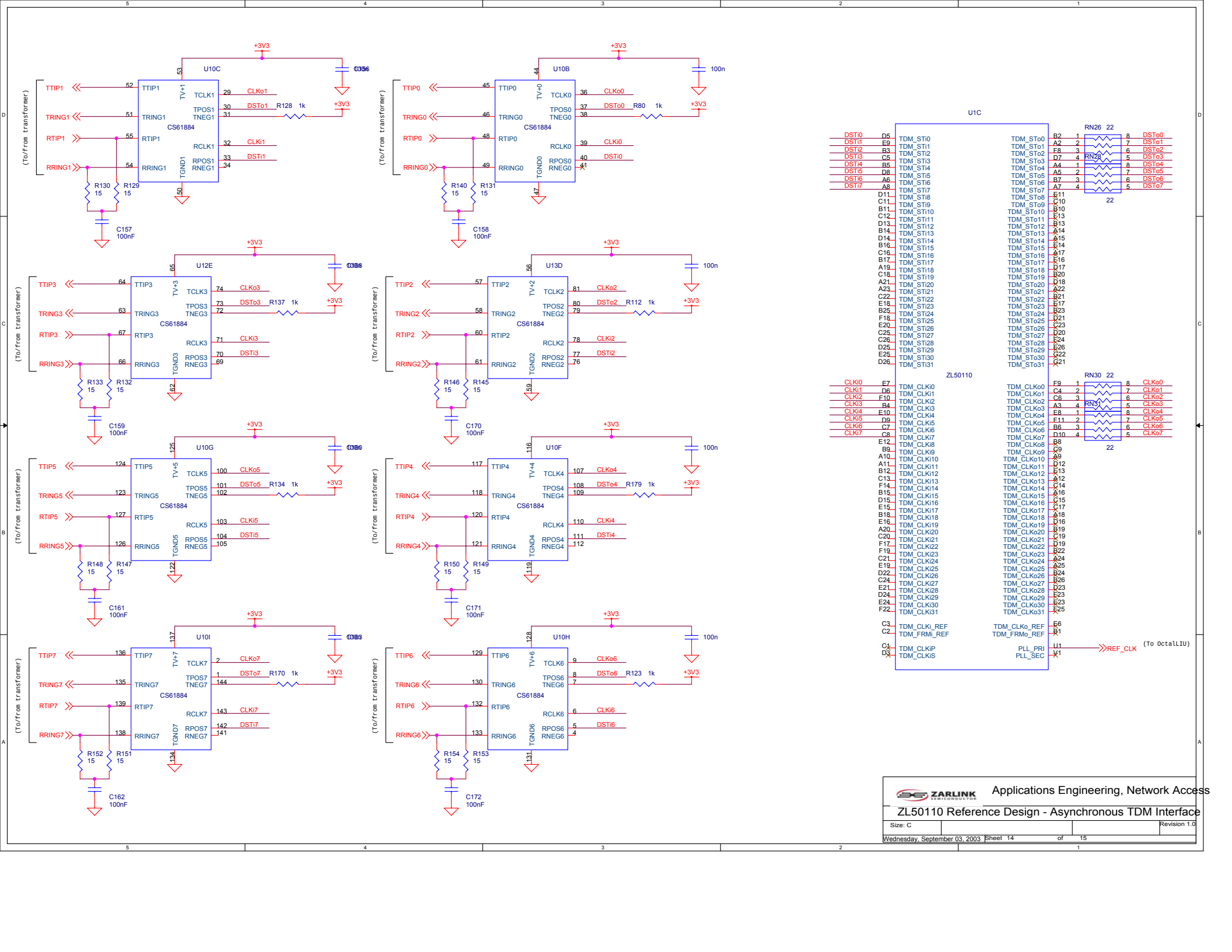
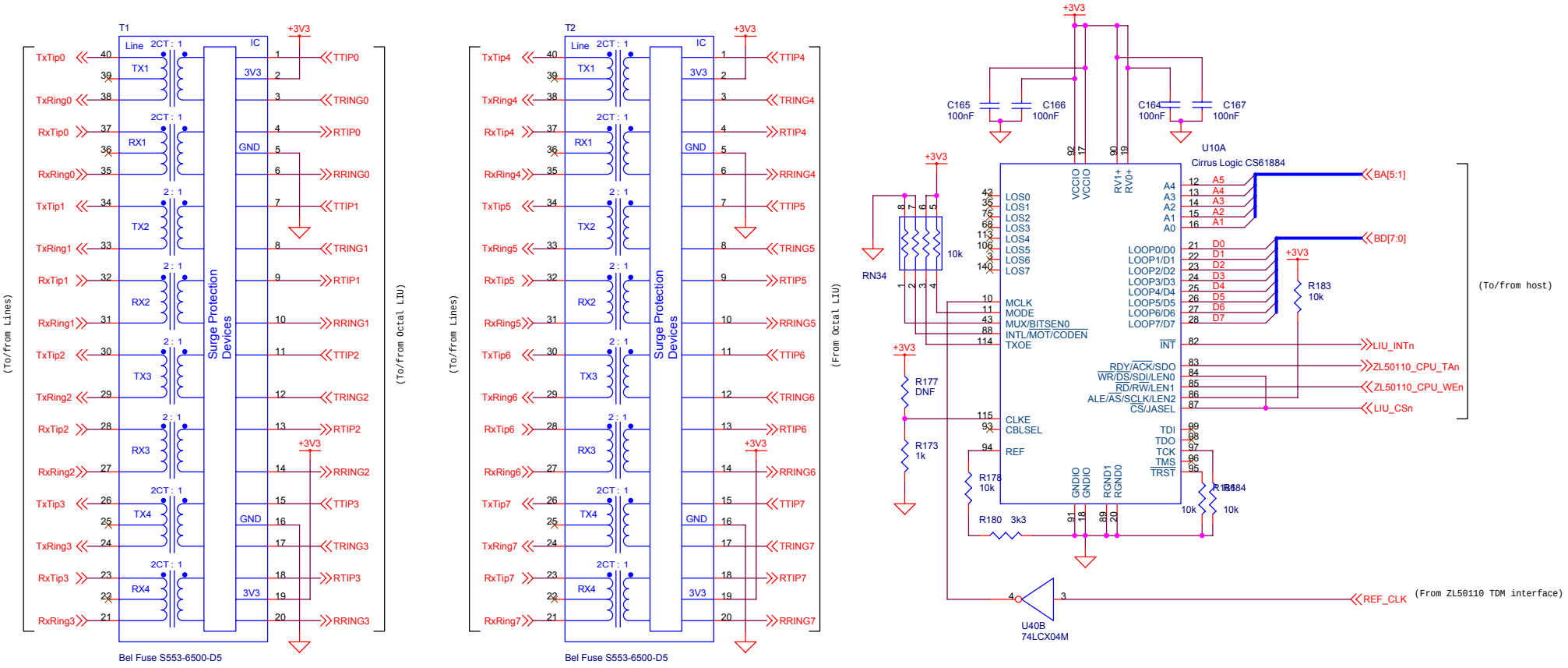

U10C
U10B
U12E
U13D
U10G
U10F
U10I
U10H
CS61884
TTIP1
TRING1
RTIP1
RRING1
TTIP0
TRING0
RTIP0
RRING0
TTIP3
TRING3
RTIP3
RRING3
TTIP2
TRING2
RTIP2
RRING2
TTIP5
TRING5
RTIP5
RRING5
TTIP4
TRING4
RTIP4
RRING4
TTIP7
TRING7
RTIP7
RRING7
TTIP6
TRING6
RTIP6
RRING6
(To/from transformer)
+3V3
100n
R130 15
R129 15
R140 15
R131 15
R133 15
R132 15
R146 15
R145 15
R148 15
R147 15
R150 15
R149 15
R152 15
R151 15
R154 15
R153 15
C157 100nF
C158 100nF
C159 100nF
C170 100nF
C161 100nF
C171 100nF
C162 100nF
C172 100nF
U1C
ZL50110
RN26 22
RN28 22
RN30 22
RN31 22
(To OctalLIU)
REF_CLK
ZARLINK SEMICONDUCTOR
Applications Engineering, Network Access
ZL50110 Reference Design - Asynchronous TDM Interface
Size: C
Revision 1.0
Wednesday, September 03, 2003
Sheet 14 of 15



ZARLINK SEMICONDUCTOR

Applications Engineering, Network Access

ZL50110 Reference Design - Octal LIU and Transformers

Size: B		Revision 1.0
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