



# CESoP PROCESSORS ZL50110/1/2/4

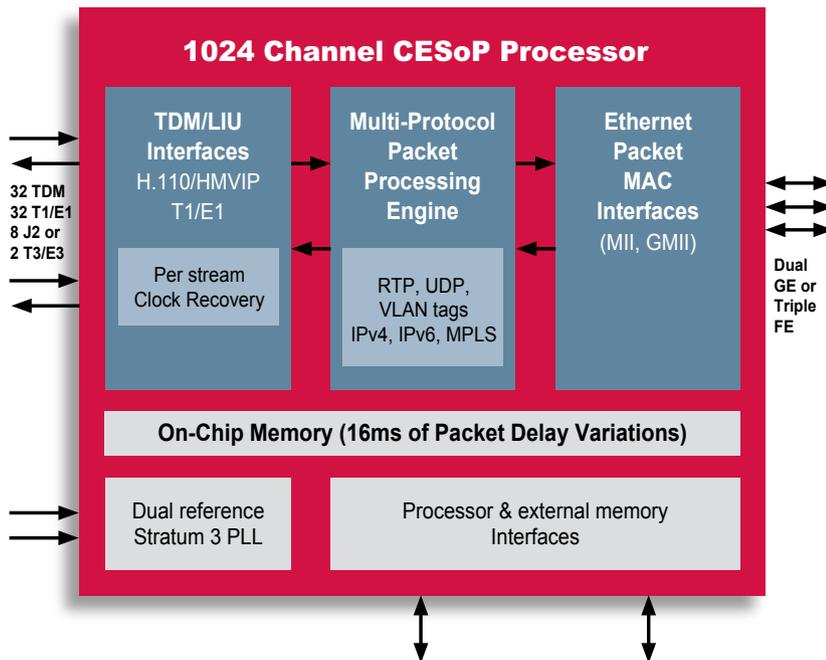
## PRODUCT PREVIEW

The ZL50110/1/2/4 are Zarlink's second generation of TDM-to-Packet processors. Designed specifically for T1/E1 voice and data services emulation over packet switched networks, they optimize performance and cost efficiency of metro Ethernet applications.

The ZL50111 features the industry's highest density dedicated processor for structured and unstructured circuit emulation services over packet (CESoP), able to support up to 32 T1, 32 E1, 8 J2, 2 T3 or 2 E3 streams. The high density is required to drive carrierclass voice and data services between the circuit-switched TDM and Ethernet networks.

With the industry's highest density, integrated memory and embedded timing solution, the single-chip design substantially reduces CES equipment cost, form factor and design complexity.

**ZL50111 Simplified Block Diagram**



	TDM Interfaces	Package	Availability
ZL50110	8 T1/E1 (256Ch.) or 2 J2	552 PBGA	Now
ZL50111	32 T1/E1 (1024Ch.), 2 T3/E3 or 8 J2	552 PBGA	Now
ZL50112	16 T1/E1 (512Ch.) or 4 J2	552 PBGA	Now
ZL50114	4 T1/E1 (128Ch.) or 1 J2	552 PBGA	Now

### Applications

- ➔ Leased line support over packet network
- ➔ Multi-tenant unit access concentration
- ➔ Transport over WiFi & WiMAX systems
- ➔ Cell site backhaul
- ➔ EPON, GPON, GEAPON
- ➔ Metro Ethernet switches
- ➔ Legacy traffic over packet switched networks
- ➔ Retrofit existing TDM systems

### Industry's Highest Density

- ➔ TDM access interfaces support up to 32 T1, 32 E1, 8 J2, 2 T3 or 2 E3 streams
- ➔ Supports up to 1024 bi-directional 64 kbps channel trunking
- ➔ Up to 3 x 100 Mbps MII or Dual 1000 Mbps GMII packet interfaces

### Supports High QoS Carrier-Class Voice

- ➔ Programmable multi-protocol packet encapsulation supports RTP, UDP, Ethernet VLANs, IPv4, IPv6 and evolving MPLS, PWE3 and MEF circuit emulation standards
- ➔ Dedicated Packet processing engine provides low latency (less than 500 μs), which contribute to superior QoS
- ➔ Four classes of service with programmable priority mechanisms
- ➔ Packet sequencing allows lost packet detection and resequencing

### Embedded Timing

- ➔ Embedded timing solution recovers clocks across packet switched networks providing network-wide synchronization
- ➔ Provides per-stream T1/E1 clock recovery in unstructured CES mode
- ➔ Dual reference stratum 3/4/4E DPLL supports TDM (H.110/HMVIP) master and slave timing operation

### Flexible

- ➔ Flexible 32-bit CPU interface compatible to Motorola's PowerQUICC II™
- ➔ On-chip packet memory with buffer depths from 16 to 128 ms supports most application requirements
- ➔ Up to 8 Mbytes of off-chip packet memory, supporting buffer depths of over 128 ms when required

### Complementary Products

- ➔ MT9072/6 Framers
- ➔ ZL50115-ZL50120 CESoP processors

### Standards Compliant

- ➔ IETF PWE3 Draft for native TDM circuit emulation
- ➔ RFC 4553
- ➔ ITU-T G.823 and G.824 traffic interface timing requirements
- ➔ ITU-T G.8261 for standard E1 circuits
- ➔ ANSI T1.403
- ➔ MFA 8.0.0, ITU Y.1413, Y.1453

### Customer Support

Evaluation boards and API are available for the CESoP Processors, supported by Zarlink's network of application engineers.



## APPLICATION

Circuit emulation services over packet (CESoP) are accelerating the deployment of metro Ethernet/IP networks by allowing equipment to transport high volumes of TDM services with carrier grade quality.

Zarlink's CESoP processors can be used at every point in the system where equipment bridges the TDM circuit-switched infrastructure to the Ethernet/IP network. As shown, the ZL50111 is easily implemented in a CES card that supports up to 32 T1, 32 E1, 8 J2, 2 T3 or 2 E3 streams on one side, and an Ethernet/IP backplane on the other side. In this system, the ZL50111 receives data from the TDM stream, assembles user-defined packets of TDM traffic, and transmits them over packet-switched networks using RTP, UDP, Ethernet VLANs, IPv4, IPv6, MPLS or user defined protocols. The packet engine is programmable and can support changing requirements.

The ZL50111 ensures high QoS, able to support four classes of service on packet egress for priority treatment of time-sensitive traffic. When packets are received from the Ethernet network, they are parsed to determine the egress destination, queued

based on sequence number, and lost packets are filled in to maintain timing integrity.

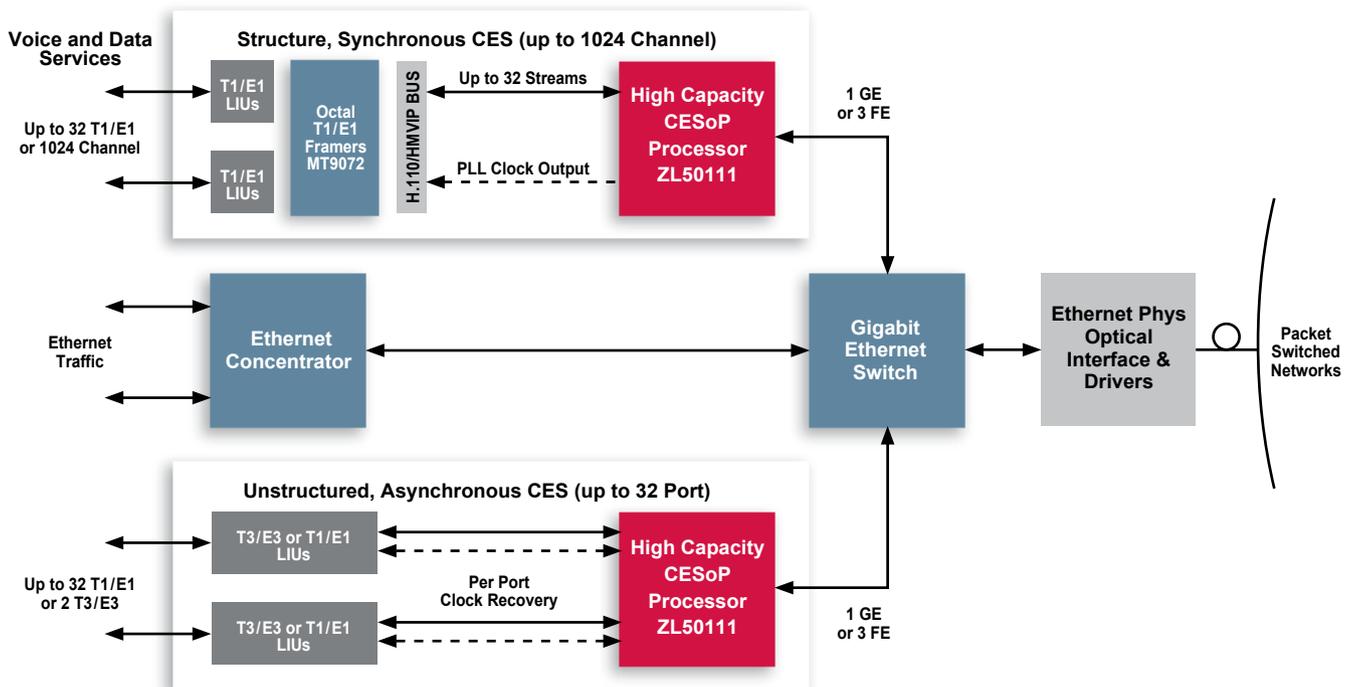
In further support of high QoS, on-chip per-stream Digitally Controlled Oscillator (DCO) ensures precise synchronization across the Ethernet network. Patent-pending software technology supports adaptive or differential timing so the best scheme can be used for a given application.

For added flexibility, the ZL50111 can be configured to act as the master or slave timing source using the embedded Stratum 3/4/4E DPPLL.

In addition to the embedded timing solution, the ZL50111 is equipped with on-board memory that compensates for up to 16 ms of packet delay variations (PDV) in the network with external support for up to 128 ms.

Zarlink's single-chip approach eliminates external circuitry, enabling a system-level solution with at least 80% saving in board area compared to equivalent discrete designs using communication processors.

### Circuit Emulation Services over Metro Ethernet



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