ZL30102/5

Product Preview

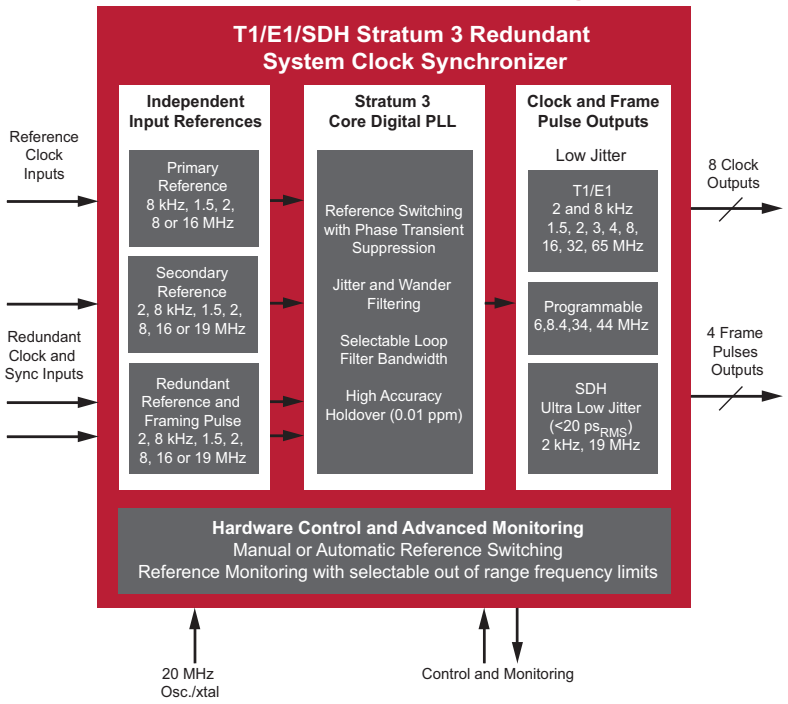
REDUNDANT SYSTEM CLOCK SYNCHRONIZER DPLLs

The ZL™30102 and ZL30105 are high-performance digital phase-locked loops (DPLLs) designed for synchronization and timing control of redundant system clocks requiring Stratum 4/4E and Stratum 3 or SDH timing specifications, respectively.

The ZL30102/5 are based on an enhanced DPLL architecture that ensures an easy and cost-effective route to compliance, with industry-standard synchronization clock interfaces. Featuring clock redundancy, low jitter generation, and excellent holdover accuracy, the ZL30102/5 provide the critical synchronization and sourcing functions in access and enterprise premises equipment to carrier-class levels.

The ZL30102/5 provide timing solutions meeting Telcordia requirements for enterprise equipment using T1/E1 interfaces and high-performance H.110 buses. In addition, the ZL30105 is suited for PDH/SDH network equipment that requires a redundant ultra-low jitter 19.44 MHz timing backplane such as Advanced TCA™ (Telecommunications Computing Architecture).

ZL30105 Simplified Block Diagram



Applications

- Clock and frame pulse source for Advanced[1] TCA, H.110, CT-BUS, ST-BUS, GCI, and other TDM buses
- Synchronization and timing control for multi-trunk T1/E1 and SDH systems, such as DSLAMs, media gateways, wireless base stations, and IP-PBXs
- 8 kHz clock multiplier

1. ZL30105 only

Enhanced Features for PDH and SDH Redundant Clock Interface

- Accepts three reference clocks that synchronize to any combination of 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz and 19.441[1] MHz
- Reference clock and synchronization pair inputs provides redundancy switching with close phase alignment between primary and secondary system clocks
- Advanced reference monitoring with selectable clock frequency range provides lock, holdover, and out-of range indications
- Simple hardware control interface offers manual or automatic hitless reference switching
- ZL30105 high performance DPLL features:
  - Ultra-low jitter of less than 20 ps_{RMS} on the 19.44 MHz clock exceeding GR-253- CORE OC-3 and G.813 STM-1 specifications
  - Less than 600 ps_{p-p} intrinsic jitter on all the other clock and frame pulse outputs
  - Accurate holdover performance of 0.01 ppm
  - Generates a wide range of fixed and programmable clock and frame pulse outputs for PDH and SDH systems

Standards Compliant

- ANSI T1.403 and ETSI ETS 300 011 for ISDN primary rate interfaces
- ITU-T G.823 for 2048 kbps and G.824 for 1544 kbps interfaces, G.813[1] option 1
- Telcordia GR-1244-CORE Stratum 4/4E and Stratum 3[1]

Complementary Microsemi Products

- APLL and DPLL for SONET/SDH
- TDM/TSI switches and T1/E1 transceivers

Customer Support

The ZL30102/5 are supported by a customer evaluation board and the network of in-house field application and design engineers of Microsemi.

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ZL30102/5

Applications

Networking equipment deployed in central offices and customer premises must meet strict international standards for timing and synchronization to ensure accurate and reliable system performance. The ZL30102/5 DPLLs provide a complete off-the-shelf timing solution for networking equipment carrying circuit-switched and packet-based traffic.

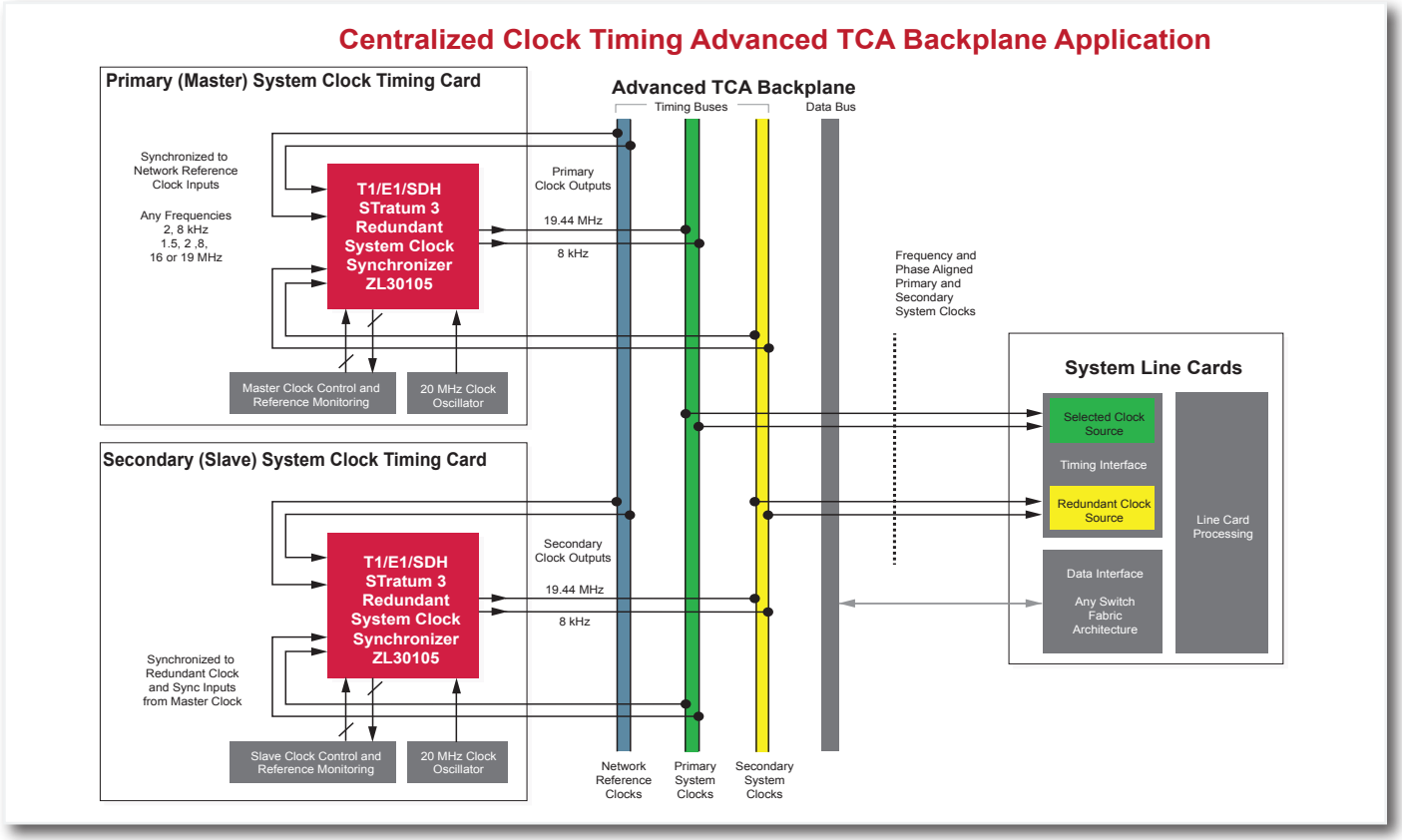
The following diagram describes an Advanced TCA™ centralized timing configuration that can be used with any backplane data bus or switch fabric configuration. The ZL30105 on the primary and secondary timing card each provide reliable, phase-aligned, low jitter 8 kHz, and 19.44 MHz system clocks to all the line cards connected to the backplane.

The primary timing card is usually synchronized to a BITS, SSU clock, or an extracted network timing reference signal from the line cards. The ZL30105 accepts a wide range of standard reference clock and frame pulse frequencies. Each reference input is monitored within its specific frequency range and maximum frequency deviation limits. When the network frequencies are outside the programmable frequency range, the ZL30105 provides automatic reference switching between reference inputs without any disruption to the primary system clock outputs. When both network references are down, the ZL30105's holdover mode keeps the primary system output clocks accurate within 0.01 ppm of the previous valid reference.

On the secondary timing card, the ZL30105 is synchronized to the primary system clock using the reference clock and synchronization pair inputs to provide redundancy switching. Precise phase alignment of the primary and secondary timing cards clock outputs is achieved under all jitter and wander conditions. This enables the line cards to switch at any time between primary and secondary system clocks without disruption or loss of synchronization.

The ZL30102 and ZL30105 DPLLs enable designers to easily and costeffectively built redundant timing systems that meet Telcordia and SDH timing requirements for Advanced TCA and H.110 backplanes.

Centralized Clock Timing Advanced TCA Backplane Application



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