*Sanjaya Maniktala, 2013*

# ACTIVE RESET IN FORWARD CONVERTERS

## Introduction

There is a steady build-up of current (and stored energy), every cycle, within the magnetization inductance of any transformer, just as in any inductor. It is this energy which gets delivered to the Secondary side in a Flyback topology. In a Forward converter, because of the winding polarities, that does not happen. We have to do something about it. Unfortunately, the magnetization energy is much larger than the leakage energy of a Flyback. Typically, leakage inductance is only 1% of the magnetizing inductance in a transformer. We can try RCD clamps or zener clamps for a Forward converter too, but clearly the impact on efficiency will be unacceptable.

The conventional way to handle this is to use a third "energy recovery" winding. This thin "tertiary" or "third' or "reset" winding is tightly coupled to the Primary winding (usually wound together, i.e. "bifilar"), to minimize leakage between the Primary winding and the energy-recovery winding, so that the energy recovery winding can take up all the ampere × turns relinquished by the Primary winding whenever the switch turns OFF. The diode direction and polarity of the winding is such that the winding conducts just like a (very tightly coupled), Flyback winding. Since this new winding typically connects through a diode into the input cap (of the input rail), therefore, during the OFF-time, it places exactly $V_{IN}$ across the Primary winding, but as expected, this voltage in an opposite direction to the $V_{IN}$ impressed across the same winding during the ON-time. So the magnetization current component of the Primary-side current, ramps up with a slope of $V_{IN}/L_{MAG}$ during the ON-time, and ramps down with exactly $-V_{IN}/L_{MAG}$ slope during the OFF-time. To ensure it can complete the ramp down to zero (and thus get "reset") we have to allocate enough time. Suppose, the ON-time is 60% of the time period ("T"), and the OFF-time is only 40%, there will be a bigger ΔI (increase) during the ON-time and a smaller ΔI (decrease) during the OFF-time. So we will end the cycle with a net *increment* in current. The core would not be "reset" and there will be staircasing every cycle till destruction occurs. Therefore we must allocate at least 50% of the time period as $T_{OFF}$, just to ensure reset. This time symmetry is purely because of the equal slopes mentioned above. It is for this reason that all controller ICs intended for single-ended Forward converters are limited to 50% duty cycle (to leave margin, they may actually be set to a nominal of 0.47 ±0.3 duty cycle, i.e. 0.44 to 0.5 duty cycle. So the min of the duty cycle limit should be taken as 44% for all such design purposes. That is the case for the LX7309. In particular, we must ensure this max duty cycle limit (brickwall) is not "hit" at the lowest input voltage which we want to have a regulated output at. Otherwise the output will start to droop. In both the Forward and Flyback converter, since we do not usually have any control of the max duty cycle of the converter, we need to adjust our turns ration very carefully for this very reason. ***Turns ratio is invariably determined by the duty cycle limit of the controller and the lowest input voltage under consideration.*** This "50% duty cycle limit" is conducive to also eliminating subharmonic instability in current-mode control (with continuous conduction mode), and therefore turns out to be useful even in Flyback controllers (using current mode control).

Another option is to use an ***Active Clamp.***

# ACTIVE RESET IN FORWARD CONVERTERS

## ACTIVE CLAMP RESET

Before we discuss this, we may need to understand synchronous topologies a little better.

1) They are always in Forced Continuous Conduction mode (FCCM) since the current is allowed to reverse direction in the inductor. The average of the inductor current waveform (its center of ramp value), equals the load current. So if the load current is zero, the converter continues passing current back and forth, charging up the output cap, then discharging it back into the input cap, and so on. This is constantly circulating energy.

2) The Boost and the Buck-Boost are not much different actually as shown in Figure 1. The difference is, one uses a cap on the low-side, one on the high-side. This leads to the oft-quoted difference in their DC transfer functions

$$V_{O\_BOOST} = V_{IN} \times \frac{1}{1 - D_{BOOST}}$$

$$V_{O\_BUCK-BOOST} = V_{IN} \times \frac{D_{BUCK-BOOST}}{1 - D_{BUCK-BOOST}}$$

Now looking at Figure 2, we see that the "high-side" active clamp is just a *parasitic synchronous Buck-Boost*. From Figure 3, we see that the "low-side" active clamp is just a *parasitic synchronous Boost*. In both cases, these are not "regulated" converters, but are instead slaved at the duty cycle determined by $V_{IN}$ and $V_O$ (by the main switching stage). So the voltage on the clamp capacitors can vary significantly, and it is obvious that we will get the following steady voltages on the clamping caps ("cap")

$$V_{CLAMP\_LO} = V_{IN} \times \frac{1}{1 - D}$$

$$V_{CLAMP\_HI} = V_{IN} \times \frac{D}{1 - D}$$

The detailed calculations and waveforms for the high-side active clamp are shown in Figure 4 as an example. The design table (derivations are tedious but obvious), is presented in Table 2. Note our terminology here

***a) "LAC" stands for low-side active clamp***

***b) "HAC" stands for high-side active clamp***

***c) "ERW" stands for energy recovery winding case***

# ACTIVE RESET IN FORWARD CONVERTERS

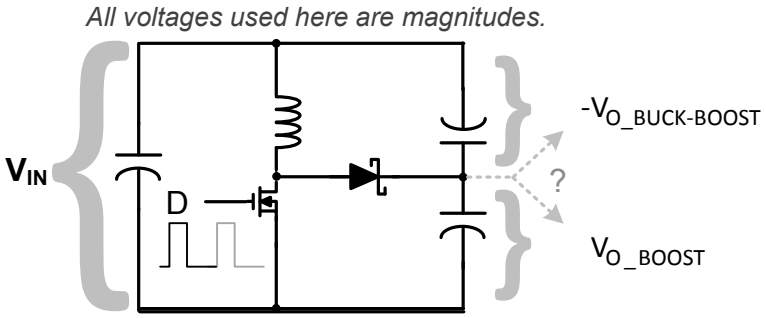
| **Design Table for Active Clamp** (and comparison to conventional "third winding" case): several alternative forms shown | | |
|---|---|---|
| **Low- side clamp** | **High-side clamp** | **Tertiary (Energy-Recovery) Winding 1:1** |
| $$D = \frac{V_O}{V_{IN}} \times n \quad (\text{where } n = N_P/N_S)$$ $$V_{IN} = V_O nD$$ | | |
| $$V_{CLAMP\_LO} = V_{IN} \times \frac{1}{1-D}$$ $$= \frac{V_O nD}{(1-D)}$$ $$= \frac{V_{IN}^{\ 2}}{V_{IN} - nV_O}$$ (clamp cap average, add typ. 10% for ripple component) | $$V_{CLAMP\_HI} = V_{IN} \times \frac{D}{1-D}$$ $$= \frac{V_O nD^2}{(1-D)}$$ $$= \frac{nV_O V_{IN}}{V_{IN} - nV_O}$$ (clamp cap average, add typ. 10% for ripple component) | NA |
| $$V_{DS} = V_{CLAMP\_LO}$$ $$V_{DS} = \frac{V_O nD}{(1-D)} \equiv \frac{V_{IN}}{1-D}$$ $$V_{DS} = \frac{V_{IN}}{1 - \frac{nV_O}{V_{IN}}} = \frac{V_{IN}^{\ 2}}{V_{IN} - nV_O}$$ (Drain-Source FET voltage, same as minimum voltage rating of active clamp FET) | $$V_{DS} = V_{CLAMP\_HI} + V_{IN}$$ $$= \frac{V_O nD}{D(1-D)} + \frac{V_O n}{D}$$ $$V_{DS} = \frac{V_O nD}{(1-D)} \equiv \frac{V_{IN}}{1-D}$$ $$V_{DS} = \frac{V_{IN}}{1 - \frac{nV_O}{V_{IN}}} = \frac{V_{IN}^{\ 2}}{V_{IN} - nV_O}$$ (Drain-Source FET voltage, same as minimum voltage rating of active clamp FET) | $$V_{DS} = 2V_{IN}$$ $$V_{DS} = 2V_O nD$$ (Drain-Source FET voltage) |
| $$V_{DS} = \frac{V_{IN}}{1-D}$$ $$V_{DS} = \frac{V_O nD}{1-D}$$ $$V_{DS} = \frac{V_{IN}^{\ 2}}{V_{IN} - nV_O}$$ (Drain-Source FET voltage) | | $$V_{DS} = 2V_{IN}$$ $$V_{DS} = 2V_O nD$$ |

| | | |
|---|---|---|
| $V_{RESET} = V_{CLAMP\_LO} - V_{IN}$<br>(voltage across Primary during OFF-time | $V_{RESET} = V_{CLAMP\_HI}$<br>(voltage across Primary during OFF-time | $V_{RESET} = V_{IN}$<br>(voltage across Primary during OFF-time |
| $V_{RESET} = \frac{V_O V_{IN} n}{V_{IN} - nV_O}$<br>(voltage across Primary during OFF-time) | | $V_{RESET} = V_{IN}$<br>(voltage across Primary during OFF-time) |
| $V_D = \frac{V_{RESET}}{n} + V_O$<br>$= \frac{V_O}{1-D}$<br>(diode rating: check at max $V_{IN}$) | $V_D = \frac{V_{RESET}}{n} + V_O$<br>$= \frac{V_O}{1-D} \times \left(D^2 - D + 1\right)$<br>(diode rating: check at max $V_{IN}$) | $V_D = \frac{V_{RESET}}{n} + V_O$<br>$= V_O(1+D)$<br>$= \frac{V_{IN} + nV_O}{n}$<br>(diode rating: check at max $V_{IN}$) |
| $V_D = \frac{V_O\left(2V_{IN} - nV_O\right)}{\left(V_{IN} - nV_O\right)}$<br>(diode rating: check at max $V_{IN}$) | | |

**Table 1:** Active Clamp Design Table

# ACTIVE RESET IN FORWARD CONVERTERS

## Positive to Positive Boost OR Negative to Positive Buck-Boost




Start with DC transfer function of a Boost Topology:

$$\frac{V_{O\_BOOST}}{V_{IN}} = \frac{1}{1-D}$$

Using $V_{O\_BOOST} - V_{IN} = V_{O\_BUCK-BOOST}$ (from above schematic)

$$V_{O\_BUCK-BOOST} + V_{IN} = \frac{V_{IN}}{1-D}$$

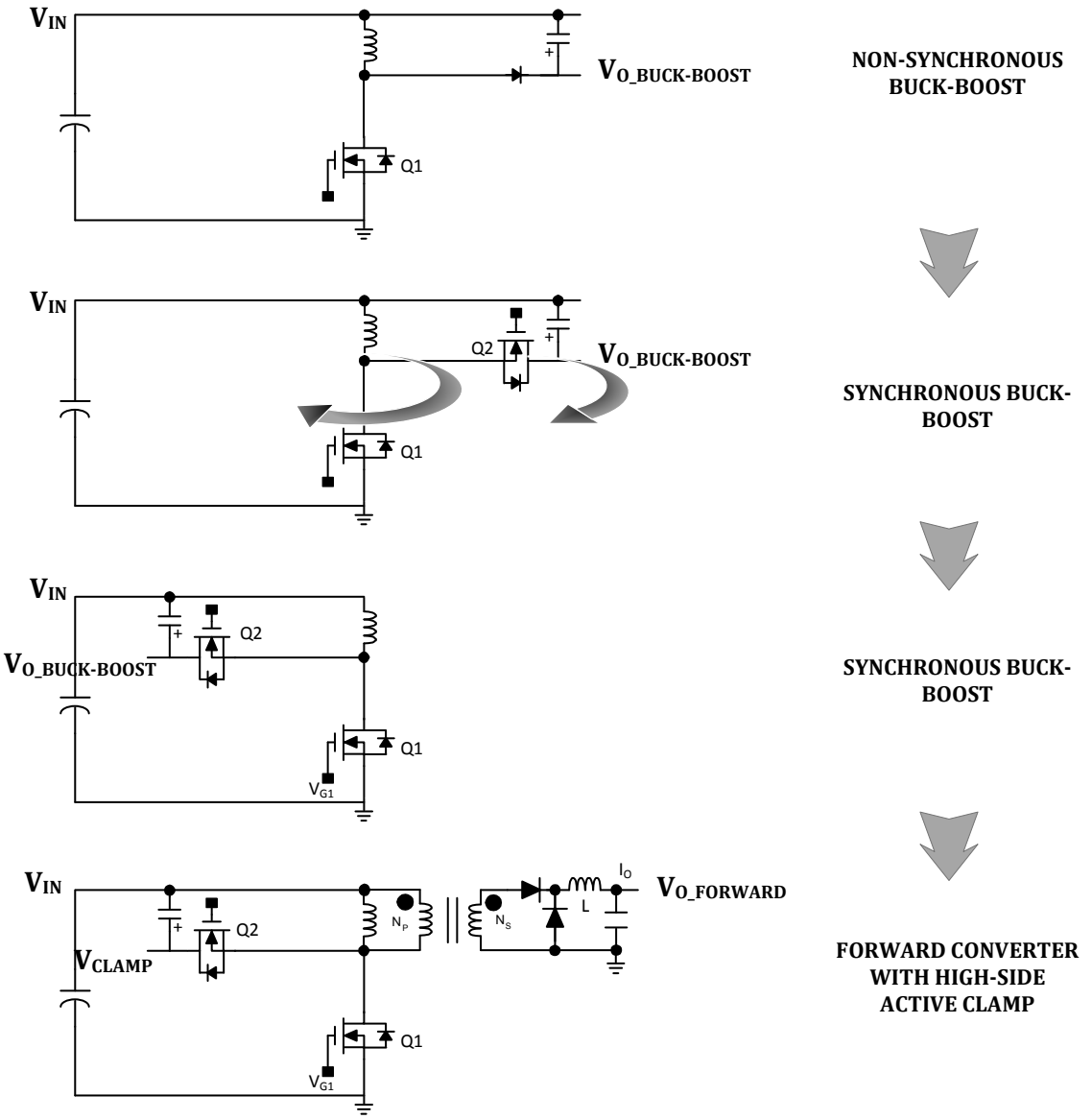
Simplifying,

$$\frac{V_{O\_BUCK-BOOST}}{V_{IN}} = \frac{D}{1-D}$$

We get the DC transfer function of a Buck-Boost Topology, starting from a Boost topology! This is by just drawing power from either of the two caps shown above.

**Figure 1:** Boost and Buck-Boost are very similar

# ACTIVE RESET IN FORWARD CONVERTERS

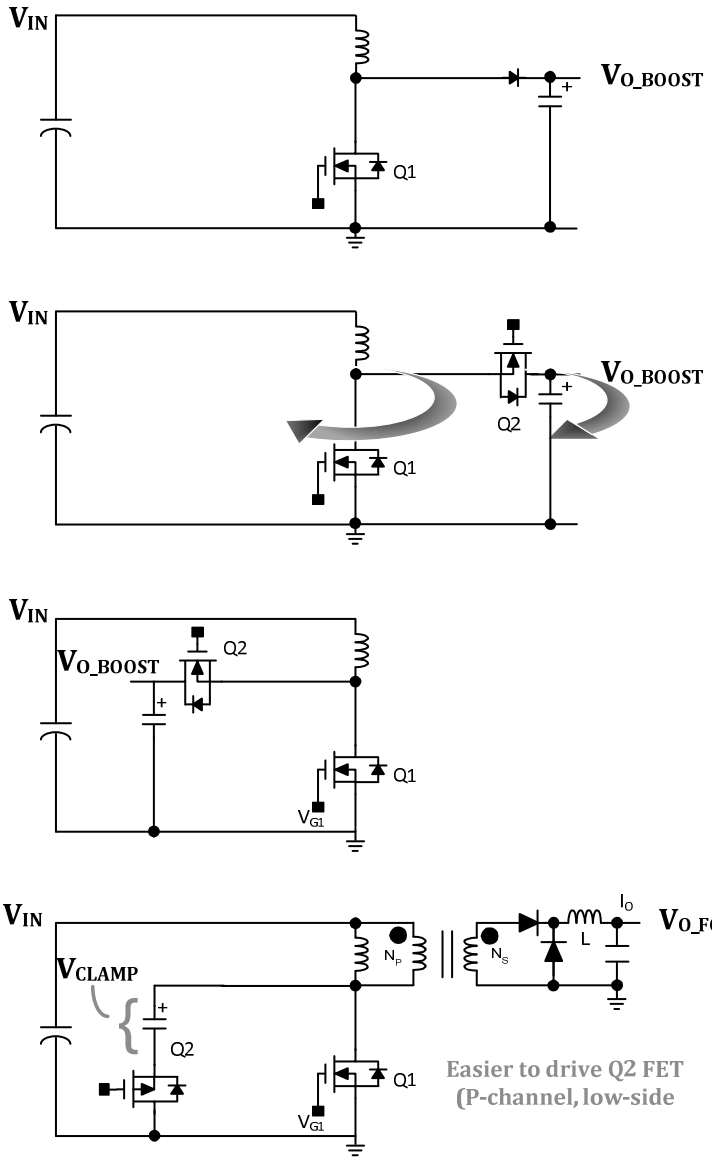



**Clamp Cap Voltage is the output voltage of a synchronous Buck-Boost. So** $V_{CLAMP} = V_{IN} \times \frac{D}{1-D}$

**The high-side active clamp is in effect, simply a synchronous Buck-Boost, operating at almost zero average load current (since no "load" is connected across the clamp capacitor, which is the Buck-Boost stage's "output cap"). So cycles energy back and forth between the clamp capacitor and the input rail. The output of this Buck-Boost is not being regulated, instead it is slaved to the duty cycle of the Forward: D= $V_O/V_{IN}$**

**Figure 2:** The "high-side" active clamp is just a parasitic synchronous Buck-Boost

# ACTIVE RESET IN FORWARD CONVERTERS




NON-SYNCHRONOUS BOOST

SYNCHRONOUS BOOST

SYNCHRONOUS BOOST

FORWARD CONVERTER WITH LOW-SIDE ACTIVE CLAMP

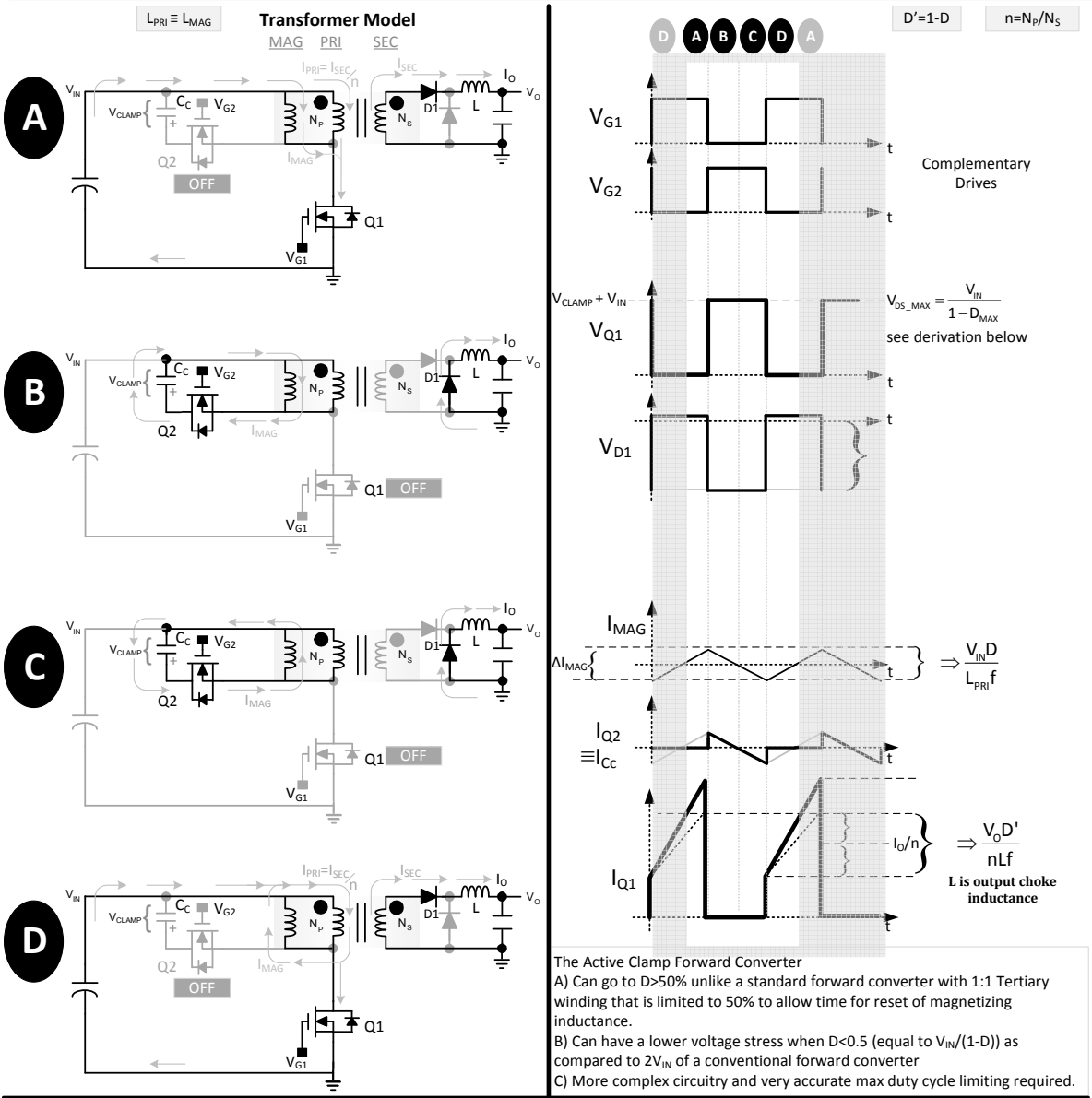
**Clamp Cap Voltage is the output voltage of a synchronous Boost. So**

$$V_{CLAMP} = V_{IN} \times \frac{1}{1-D}$$

**The low-side active clamp is in effect, simply a synchronous Buck-Boost, operating at almost zero average load current (since no "load" is connected across the clamp capacitor, which is the Boost stage's "output cap"). So cycles energy back and forth between the clamp capacitor and the input rail. The output of this Buck-Boost is not being regulated, instead it is slaved to the duty cycle of the Forward: D= $V_O/V_{IN}$**

**Figure 3:** The "low-side" active clamp is just a parasitic synchronous Boost

# ACTIVE RESET IN FORWARD CONVERTERS




For all practical purposes, on the Primary side, we have a synchronous Buck-boost converter with input $V_{IN}$ and output $V_{CLAMP}$ (and net load current of zero). Its inductor is the magnetizing inductance "MAG". The duty cycle and max voltage on the switch are determined just an in any Buck-boost.

In a Buck-boost: $\Rightarrow V_O = V_{IN} \times \frac{D}{1-D}$

So for the clamp circuit effective Buck-boost: $\Rightarrow V_{CLAMP} = V_{IN} \times \frac{D}{1-D}$ (Voltage across Clamp Cap)

Max $V_{DS}$ in a Buck-boost: $\Rightarrow V_{DS\_MAX} = V_O + V_{IN} = V_{IN} \frac{D}{1-D} + V_{IN} = \frac{V_{IN}}{1-D}$

Max $V_{DS}$ for the clamp circuit effective Buck-boost: $\Rightarrow V_{DS\_MAX} = \frac{V_{IN}}{1-D}$

**Figure 4:** Detailed Current and Voltage waveforms of a high-side active clamp

## Analysis and Conclusions (Figures 5 to 7)

Note that for a given turns ratio "n", the curve for active clamp (high-side or low-side, "HAC" or "LAC") intersects the energy recovery winding ("ERW") case at exactly D=0.5 (at this point duty cycle is the for active clamp or energy recovery winding cases). The ERW curve does not go to lower inputs because the duty cycle limit of the controller is 50%.

It is commonly stated in literature that the advantage of the active clamp is it "allows" us to go to duty cycles greater than 50%. It certainly does, but as we see in Figure 5, there is no point in doing that. The FET voltage stress goes up significantly above D=0.5. So does the diode stress as per Figure 6. The reason is obvious: if we apply $V_{IN}$ across the Primary winding for larger $T_{ON}$, the voltage across the Primary during the OFF-time (its so-called reset voltage) must go up, as also indicated in Figure 7. This is because *for any winding on a transformer the voltseconds law must be satisfied (in steady state)*. There is no escaping Physics here again.

So though the active clamp enables us to go to D>0.5, we should not. In fact it is advisable to firmly clamp the duty cycle to 50%, just as in the case of the conventional Forward converter with 1:1 energy recovery winding.

So how do we benefit? Assuming the turns ratio is still the same, we see from Figure 5 that at duty cycles less than 50% (higher input voltages than their intersection, and corresponding to the shaded area), the ERW curve and the HAC/LAC curve diverge, so the active clamp helps lower the voltage stress. This is because the clamp voltage is determined no longer by us or the Forward converter per se, by whatever output voltage the (parasitic) Boost, or Buck-Boost develops, when slaved to the master duty cycle (based on the Buck stage of the Forward converter). It just so happens that that output rail (clamping capacitor voltage) is less than $V_{IN}$ or $2\times V_{IN}$ (in the case of the parasitic Buck-Boost, i.e., high-side active clamp, or the parasitic Boost, i.e., low-side active clamp, respectively).

The active clamp therefore reduces the voltage stresses (FET and diode) as compared to the energy recovery winding, for D<0.5. The down-side is that since the active clamp is sloshing current back and forth continuously, as in the case of any synchronous topology at almost zero load, the circulating current is relatively higher in an active clamp case, compared to the energy recovery winding case.

Figure 5 and Figure 6 also tell us that if for a given input and output voltage, and for duty cycles less than 50%, a further reduction in voltage stress occurs if we lower the turns ratio (not increase it as sometimes stated in literature). The physical reason for that is easy to understand. Because by lowering the turns ratio, we are making the reflected input voltage $V_{INR}/n$ bigger. So the duty cycle $D= V_O/V_{INR}$ will decrease. Then, since $T_{ON}$ of the main FET is now less, the input voltage $V_{IN}$ applied across the Primary, is present for a smaller time. Then by the voltseconds law, the voltage on the winding during the OFF-time (the reset voltage) will be less. This is what gets reflected to the output diodes as $V_{RESET}/n + V_O$. So it tends to decrease. Though, if n had decreased faster than $V_{RESET}$ had decreased, the diode stress would go up! We see from Figure 10 that that does not happen. So we can conclude that lowering the turns ratio would benefit us from the viewpoint of diode ad FET stresses. The down-side is that because of smaller duty cycle, we will tend to run into discontinuous conduction mode (DCM) in the Buck stage for higher than light loads, and we may therefore need to increase the inductance of the output choke for example. Also, as we lower the input, we may more readily hit the $D_{MIN}$ limit of controller IC, especially at lighter loads.

## Which is Better: High-Side or Low-Side Active Clamp?

Note that from Figure 6, we see that the low-side active clamp has much higher voltage stresses. In contrast, the high-side clamp has lower stresses. Other than that, the voltage and diode stresses on the Forward converter components and the transformer windings, are all identical. High-side or low-side does not matter.

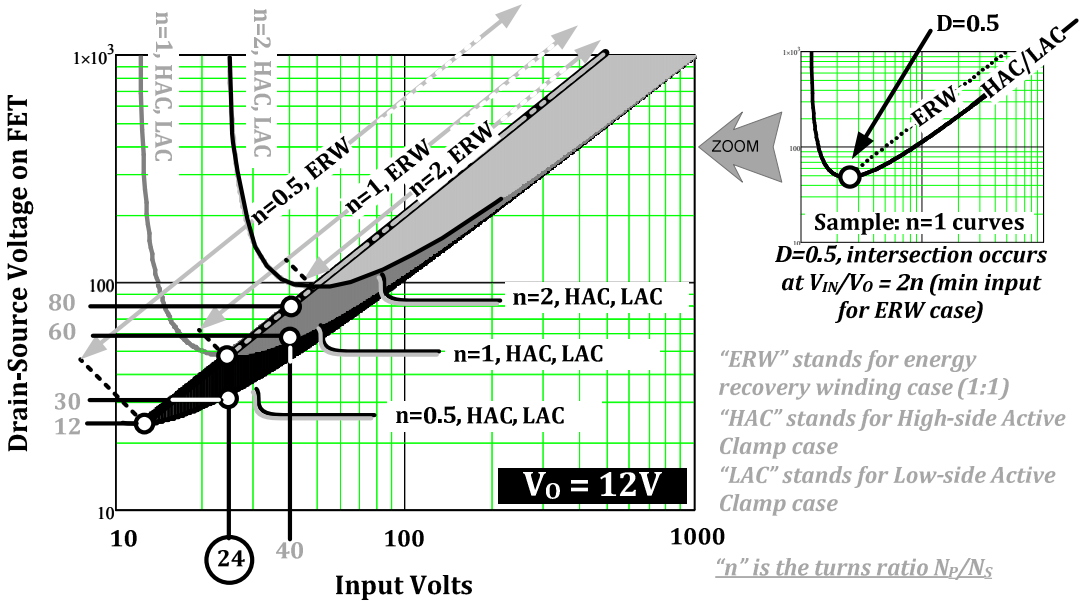
One problem this can lead to, especially in high-voltage applications is that the low-side clamp position is most suited to using a P-channel FET. And this is also the position we are getting highest voltage stresses. It may be difficult to even find P-channel FETs with ratings greater than 400V.

The high-side clamp is suited for an N-channel FET, but we will need a Gate driver transformer to translate the voltage to its Source (its Gate reference level). On the other hand, the low-side clamp is a P-channel FET, and can be driven with a simple capacitor coupling circuit from the controller IC. This translates the signal to provide negative pulses to turn ON the P-channel FET.

The polarity of the voltages must be kept in mind. To turn ON a P-channel FET, we need the controller IC to produce a LOW level when the Gate of the main FET goes LOW. Whereas to drive the N-channel FET, it needs to produce a HIGH pulse when the Gate of the main FET goes low. Simple buffer or inverting circuits, derived from the main Gate pin signal do not work well, because we need a certain deadtime before we turn on any active clamp FET after the main FET turns OFF, and similarly turn it OFF, a little before the main FET turns ON. So for example, a simple complementary signal from the main FET drive pin is not enough to drive the N-channel FET of the high-side clamp: we definitely need deadtime. So a dedicated pin is usually provided on a control IC for that. It may also feature an inverted (but similarly deadtime gated) signal for driving the P-channel FET of a low-side active clamp. Fir the high-side active clamp, do not use a Floating driver IC! This usually has 100's of nanoseconds of propagation delay, and that will annihilate any deadtime planning, and will cause shoot-through in the main FET and active clamp FET, destroying either or both (if one goes, the other will very shortly!).

Microsemi

# ACTIVE RESET IN FORWARD CONVERTERS




*D=0.5, intersection occurs at $V_{IN}/V_O = 2n$ (min input for ERW case)*

*"ERW" stands for energy recovery winding case (1:1)*
*"HAC" stands for High-side Active Clamp case*
*"LAC" stands for Low-side Active Clamp case*

*"n" is the turns ratio $N_P/N_S$*

**For example ($V_O$=12V), graphically:**

**General case, mathematically:**

A) With turns ratio 1, the energy recovery winding case will work down to only 24V.

$$V_{IN} = V_O nD, so V_{INMIN} = 12 \times 1 \times 0.5 = 24V$$

B) The active clamp with same turns ratio, does go to lower voltages than that, but the voltage on the FET rises steeply (which is not good, so it is NOT a region we want to go into, and shouldn't --- by means of a good max duty cycle clamp!).

C) However above 24V, the active clamp case FET voltage does dip compared to energy recovery winding case. So fpr example, at $V_{IN}$=40V, the FET voltage with active clamp is ~60V (57V, see on right) as compared to 80V with the energy recovery winding.

$$V_{DS} = \frac{V_{IN}^2}{V_{IN} - nV_O} = \frac{40^2}{40 - 1 \times 12} = 57.14V$$

D) We can lower the FET voltage further, down to ~30V (say at 24V input), by **lowering** the turns ratio to 0.5 (the transformer is stepping up now, to force a smaller duty cycle for the Buck).

$$V_{DS} = \frac{V_{IN}^2}{V_{IN} - nV_O} = \frac{24^2}{24 - 2 \times 12} = 32V$$

E) By lowering the turns ratio to n = 0.5, we can now also go down to 12V input (with duty cycle still less than 50%).

$$V_{IN} = V_O nD, so V_{INMIN} = 12 \times 2 \times 0.5 = 12V$$

**1) Though the active clamp does allow you to go to duty cycles greater than 0.5, the FET voltage stress increases dramatically for D >0.5. So we do <u>not</u> want to operate in that region ayway.**
**2) The biggest advantage in stresses is for duty cycles less than 0.5 (using active clamp).**
**3) Lowering the duty cycle further, i.e., by decreasing (not increasing) the turns ratio, will help sgnificantly lower FET voltage stress (though waveforms are more peaky in switch, so RMS will be higher --- it is a compromise to find the "ideal spot" and optimum turns ratio).**

## Lowering (not increasing) the turns ratio, reducing (not increasing) the duty cycle, helps reduce FET voltage stress.

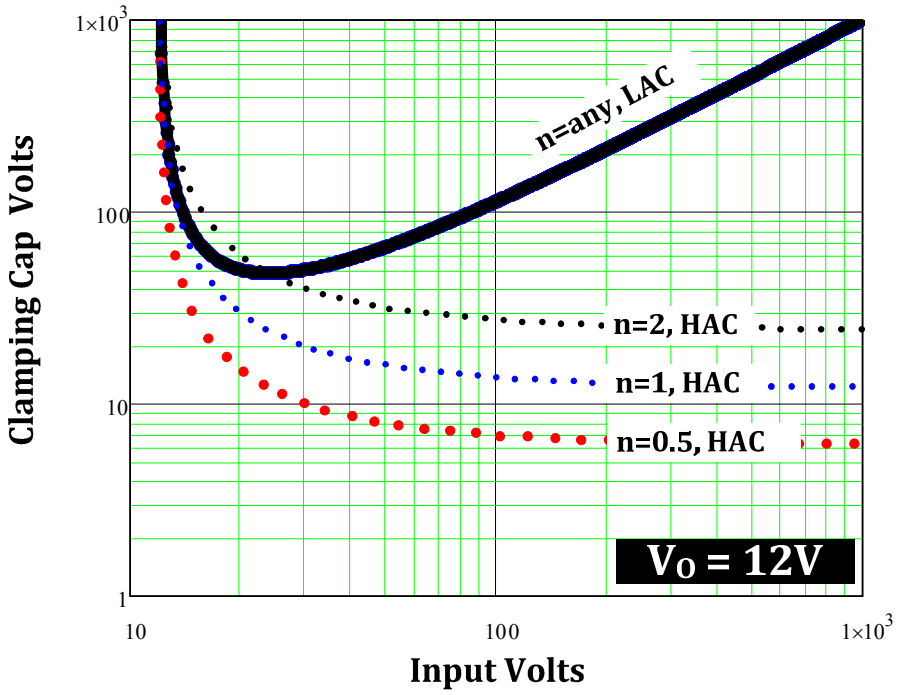
**Figure 5:** Drain-Source Voltage on Main FET, comparing Active Clamps and Energy Recovery winding cases. Also a graphical and mathematical analysis based on these graphs and equations in Table 1.

# ACTIVE RESET IN FORWARD CONVERTERS

*"LAC" stands for Low-side Active Clamp case*

*"ERW" stands for energy recovery winding case (1:1)*

*"HAC" stands for High-side Active Clamp case*



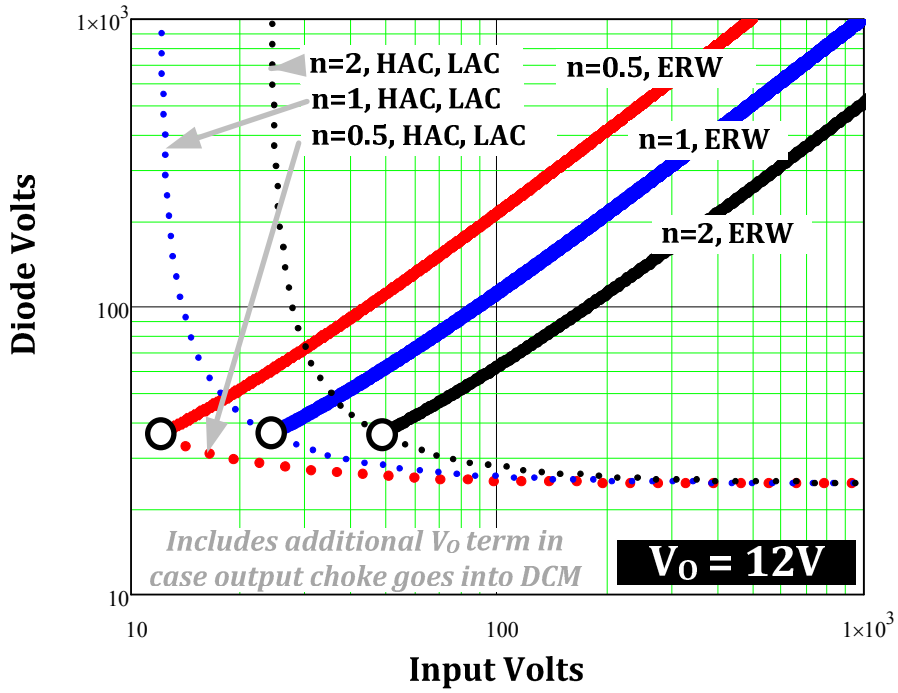




**Figure 6:** Clamping and Diode Voltage stresses compared

*"LAC" stands for Low-side Active Clamp case*

*"ERW" stands for energy recovery winding case (1:1)*

*"HAC" stands for High-side Active Clamp case*

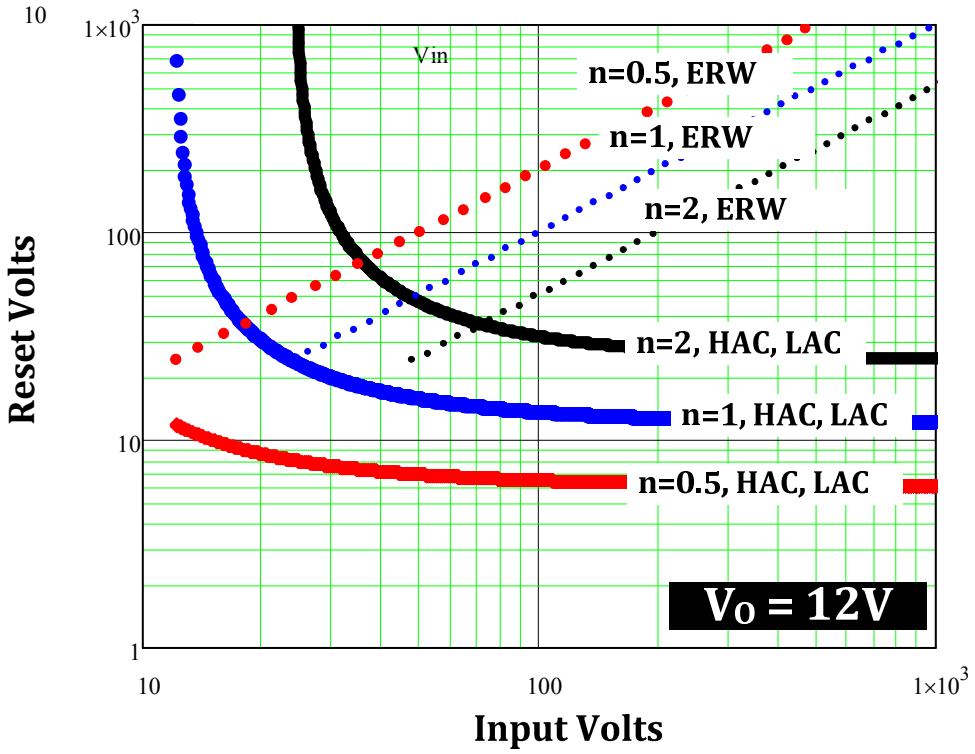



**Figure 7:** Reset Voltages compared



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