

APPLICATION NOTE

Introduction

This application note provides detailed layout guidelines for the implementation of a POE PD device DCDC PD system, based on Microsemi's PD70101AILQ and PD70201ILQ combined PD and PWM controller devices.

Applicable Documents

- PD70101A/PD70201 datasheet, catalog number DS_PD70101A_PD70201
- PD70201EVB60F12 evaluation board user guide

Background

Microsemi's PD70101AILQ and PD70201ILQ devices are part of a device family; these devices are targeted for realizing the 802.3at standard PD interface.

The PD interface device family includes the following:

Device type	Power capability	Integrates PWM controller
PD70100/A	IEEE 802.3at Type 1 (IEEE 802.3 af)	No
PD70101/A	IEEE 802.3at Type 1 (IEEE 802.3 af)	Yes
PD70200	IEEE 802.3at Type 2	No
PD70201	IEEE 802.3at Type 2	Yes

Due to its high power handling, it is very important to follow the guidelines specified in this application note in order to have noise robustness and a solution with good thermal behavior.

Layout Guidelines

PD70101ILQ / PD70201ILQ ICs comprises four ground types:

1. VPNI – VPNI is the negative side of the voltage received from the PSE side. It is connected to VPNO through the isolation switch. This switch is ON as long as the voltage is a valid PSE voltage.
2. VPNO – VPNO is the negative side voltage which is the output of the PD device front end. It is connected to VPNI through the isolation switch.
3. PWM controller Power Ground (PGND) – DC/DC power circuitry should be referenced to this ground. The DV/DT FETs gate driving signals are returned through this ground pin.
4. Quiet ground (GND) – PWM controller quiet ground used for the return path of the low power control signals.

GND and PGND are connected in a single point to the PCB to eliminate the high currents signals affecting the control signals.

In order to realize IEEE802.3at standard, PD system usually has one more ground type which is the secondary ground of the DCDC converter. Secondary ground should obtain 1500VRMS isolation from all of the above ground types.

PD70101A/PD70201 structure:

- The device is comprised of dual Dies: PD front-end Die and PWM controller Die.
- 10 pins on the left hand side of the package belong to PD front-end Die. These are pins 31-32 and 1-8. In addition the thermal Pad – pin 33 in the schematics – is also referenced to PD front-end and is internally connected to VPNI signal.
- All the rest of the pins belong to PWM controller Die.



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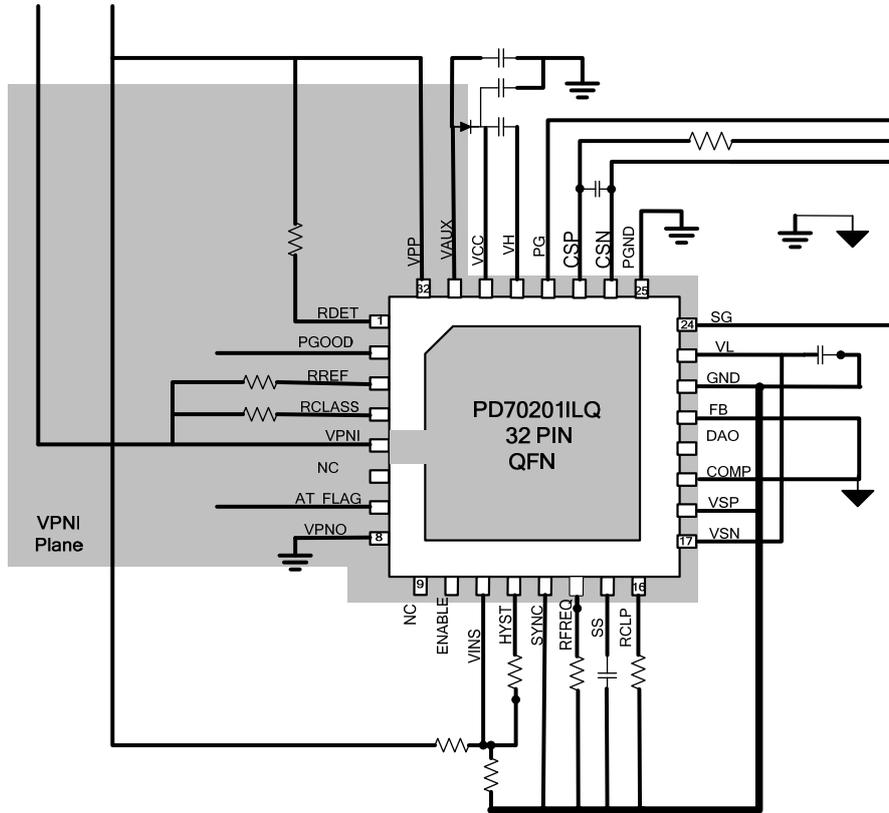


Figure 1: System Based on PD70201ILQ

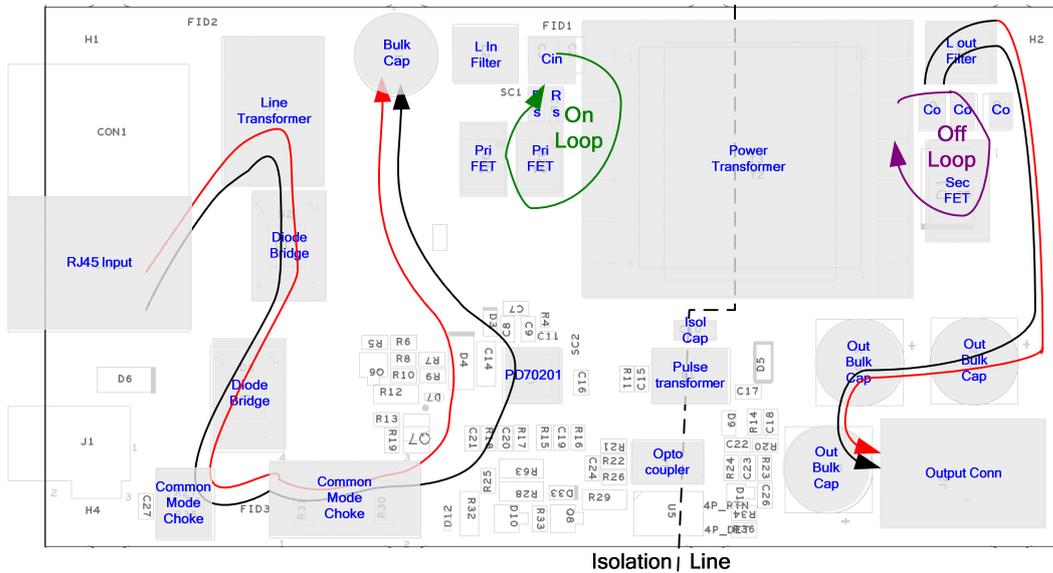


Figure 2: PD70201EVB60F12 EVB power loops and power flow

PD is comprised of some generic parts.

- Input stage.
- DCDC converter stage
- Output stage.

Figure 3 shows the current flow through these stages for the PD70201EVB60F12 evaluation board.

Input Stage

Input stage includes the following elements:

- Input RJ45 connectors
- Line transformer
- Diode bridge
- Common mode choke
- PD70101A/PD70201 device
- Bulk capacitor for DCDC input filter.

In this set of elements, the current is floating in continuous form (non-switched).

The first 4 elements should be placed next to each other in order to enable the common mode choke to filter the noise close to RJ45 connector.

To have low radiation design, the layout of the positive input and of the negative input should be in a differential form. This means that the positive rail is always as tight as possible to the negative one. See blue and RED lines in Figure 3.

Among the above elements the diode bridges and PD device are the only elements that dissipate high power and get heated. Therefore copper land for heat sinking should be maintained for them.

PD70101A/ PD70201

- PD70101A/PD70201 power dissipation is mainly a function of the device's switching FET resistance and system Current.

$$P=SW_RDSon \times \text{Max current}$$

- Place both the PD70101A/PD70201 device and its peripheral on the top side so that the bottom layer will be used as a Power dissipation layer. Keep it in as solid as possible VPNI potential.
- For the layout, use the pattern land shown in Figure 10. Vias under the device are used for heat transfer between layers.
- If there are inner layers, use them for extended copper land under the device to improve heat dissipation.
- Place VPNI/Vpp capacitors as close as possible to PD70101A/PD70201, between pins 5 and 32.
- Place PD70101A/PD70201 bypass capacitors as close as possible to the device.

Note: although the PD device is the controller of the DCDC converter its location should be determined by its Conducting features. A proper layout will allow control from a distance.

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DCDC Converter Stage.

Figure 3 depict two current pathways of driver's power section. When Primary FET is on, current flows through input On loop. When Primary FET is off, current flows through output Off loop.

Locating components close to each other within a loop, allows a shorter current loop. As a result, high currents remain in the driver's power block (and out of ground return path of quiet components). For the On Loop place CIN, power transformer, sense resistors, and Primary FET as close as possible to each other. For the Off Loop, place power XFMR, Sync FET and COUT as close as possible to each other.

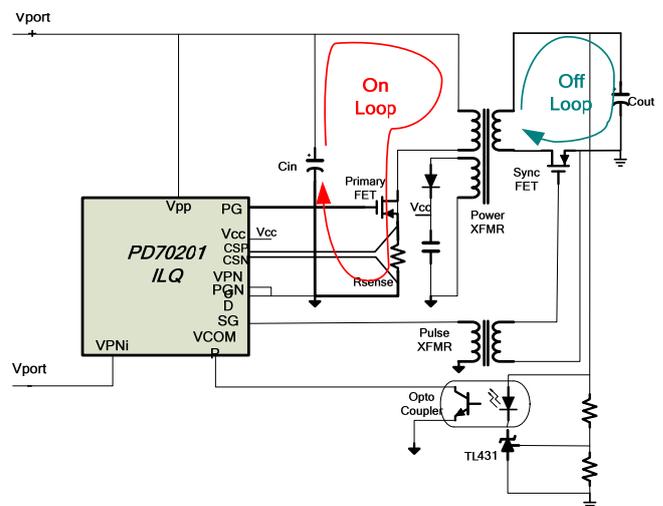


Figure 3: Current Path During ON/Off Times

Traces

Figure 4 depicts the high current traces. It is marked in RED and highlighted by a yellow background.

Make all high current traces as short and direct as possible. The trace thickness should withstand its current values with low temperature rise.

Note: Power is flowing out of VPNo signal, and not PGND.

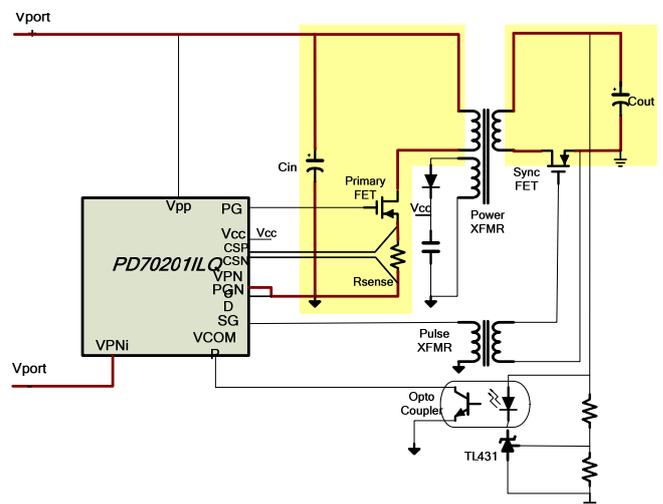


Figure 4: High current traces Layout

Sense Resistors:

Sensing of the primary loop current is done using 1% +/-100ppm low resistance resistors connected as a shunt.

Figure 5 depicts the right way to layout the power supply sense resistors.

Calculate sense resistor power dissipation. Choose resistor size and number of resistors according to calculation result.

The sense resistors' voltage is in the range of 0 to 200mV and exists in an environment of fast transitions of up to 160V. The form of the current sense signal is very important and its integrity must be maintained. Thus the sense voltage traces layout should be maintained carefully.

In order to simplify the integrity challenge, PD70101A/PD70201 has a differential sampling mechanism built of pins CSP & CSN.

Route differential traces from sense resistor terminals to CSN and CSP input pins. They should be connected as a Kelvin connection, as close as possible to the resistors pads, and should not be part of the high current path to the resistors. This way, voltage measurement is not influenced by voltage drop on the high power traces.

The two lines should be routed together close to each other in order to maintain good noise immunity. For the resistor high current trace, use a Wide trace or copper planes to decrease trace voltage drop.

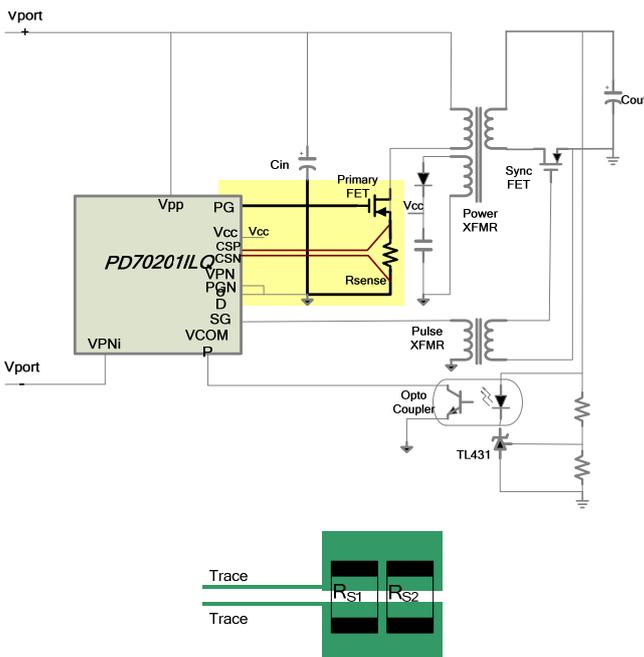


Figure 5: Sense Resistor Layout

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Primary and Secondary FETs

Primary and secondary FETs are high power devices. A FET should have copper land to enable power dissipation from it to the environment.

Copper land is a function of the FET package power consumption and the system requirements.

Figure 6 depicts DCDC converter MOSFET layout.

Calculate DCDC converter FET power dissipation to Choose MOSFET's package and thermal pad size according to calculation results. If you use two MOSFETs, connect them in parallel.

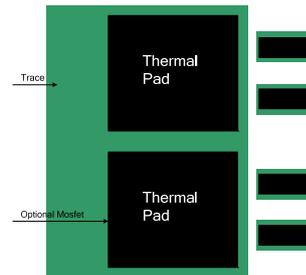


Figure 6: MOSFET Layout

MOSFET Design Example:

System Specifications:

$T_{ja_abs_max} = 150^{\circ}C$ (absolute maximum taken from data sheet)

$T_{ja_max} = 120^{\circ}C$ (design margin from data sheet absolute maximum value)

$T_{MAX} = 70^{\circ}C$ (maximum ambient temperature)

$\Delta T = T_{ja_max} - T_{MAX} = 50^{\circ}C$ (maximum required temperature rise on MOSFET case)

PMOSFET = 1.3W (Maximum FET power based on static and dynamic losses calculation)

Due to MOSFET high power dissipation, chosen MOSFET package is D2PAK with pad size of 1x1inch (25.4x25.4 mm).

$\Theta_{ja} = 35^{\circ}C/W$ (see figure 9)

$\Delta T_{ja} = 35 \times 1.3 = 45.5^{\circ}C$

Temperature rise is within system specification.

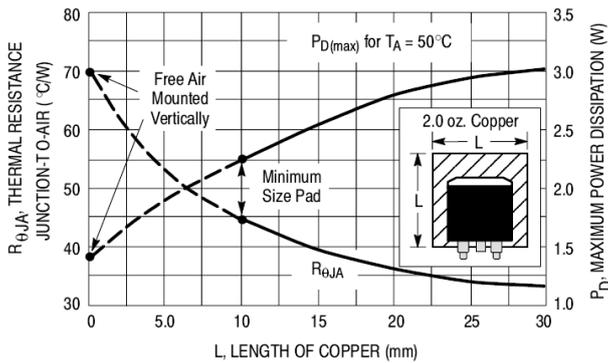


Figure 7: Thermal Resistance versus Drain Pad Area for D2PAK Package

Isolation

For an isolated DCDC design such as Flyback, Isolation level is based on IEEE 802.3AT standard.

IEEE 802.3AT standard defines 1500V_{rms} isolation to be obtained between all accessible external conductors including frame ground (if any), RJ45 connector leads, and all internal leads of the PD such as secondary side traces.

So isolation should be maintained between Flyback converter primary and secondary sides and between Frame ground and secondary side.

1500V_{rms} isolation is obtained by having a gap of 60mil between the traces of the primary domain and the secondary domain.

The isolation line of separation should include power transformer, secondary gate pulse transformer, opto-couplers, and Primary/secondary 2000V capacitor.

The Capacitor should be located close to the power transformer to help fighting conducted emission issues if raised.

Do not mix the two isolated sides. Mixing the sides may cause signals to mix and thus difficulty in maintaining the isolation.

Use a physical Isolation line as presented in Figure 8.

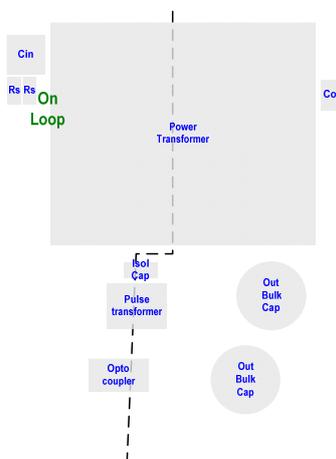


Figure 8: Isolation Line

There should not be a plane layout under the primary and secondary sides of the power transformer.

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Driving

Gate drive pulses are supplied to the primary and secondary gates and are generated by the PWM controller section of the PD70x01 devices.

In order to increase efficiency and still decrease the temperature rise of the FETs, a fast slew rate pulses should be obtained.

PD70x01 device drivers have internal serial output resistance. To overcome this internal resistance and also the distance of the controller from the FETs, extra driving components are used. For proper operation of the driving elements, pull up transistor, pull down transistor, and bypass capacitor should be as close as possible to the referenced FET.

Snubbers

Figure 9 depicts Snubbers location.

Snubbers are elements that are aimed to protect FETs from high voltage spikes that are produced due to system parasitic. For example, in the primary domain, the transformer inductance reaction to current switching creates high voltage spikes.

To overcome this issue, Snubber is placed in parallel to the transformer primary winding, and should be placed as close as possible to it. The proximity of those is very important in order to reduce the voltage spikes on the Drain-Source of the primary FET.

The location, in the bottom side under the transformer, yields a low inductance connection. The Snubber can be comprised of serial resistor and capacitor (RC Snubber), resistor capacitor and diode (RCD), or active Snubber that also uses inductor.

The Secondary side Snubber is usually an RC Snubber, and should be located very close to the secondary FET, between Drain and source.

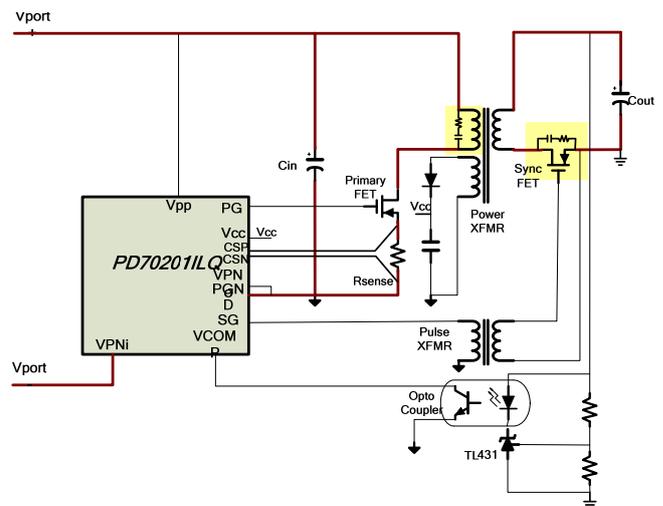


Figure 9: Snubbers Location



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Heat Sinking

The components that usually dissipate the major power portion and as a result heat up are:

- Primary FET
- Secondary FET
- Power Transformer
- PD70x01 device
- Primary Snubber components
- Secondary snubber components.

Board design should provide an adequate copper land for dissipating the heat of those components.

For PD70101A/PD70201 use the pattern land shown in Figure 10 for the layout. Vias under the device are used for heat transfer between layers. Use 25 mil Vias for effective heat transfer between layers. As a first priority use external layers for the heat dissipation; If can be done using the internal layers as well for good heat transfer.

Design example

On Figure 14 to Figure 18 you can see the layout of PD70201EVB60F12 evaluation board for reference. This board can be ordered from Microsemi.



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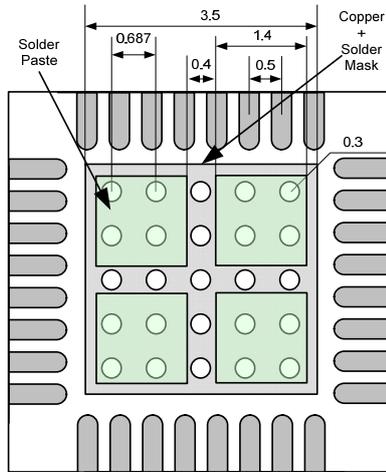


Figure 10: PD70201ILQ Recommended PCB Layout for Thermal Pad Array (mm)

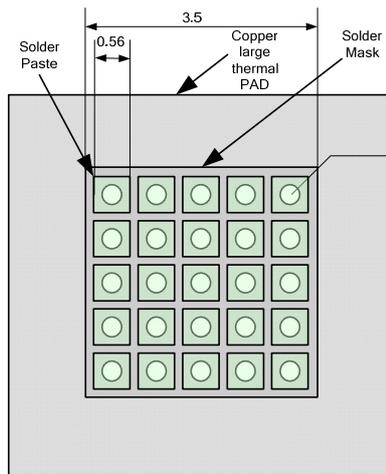


Figure 11: PD70201ILQ Bottom layer Recommended PCB Layout for Thermal Pad Array (mm)



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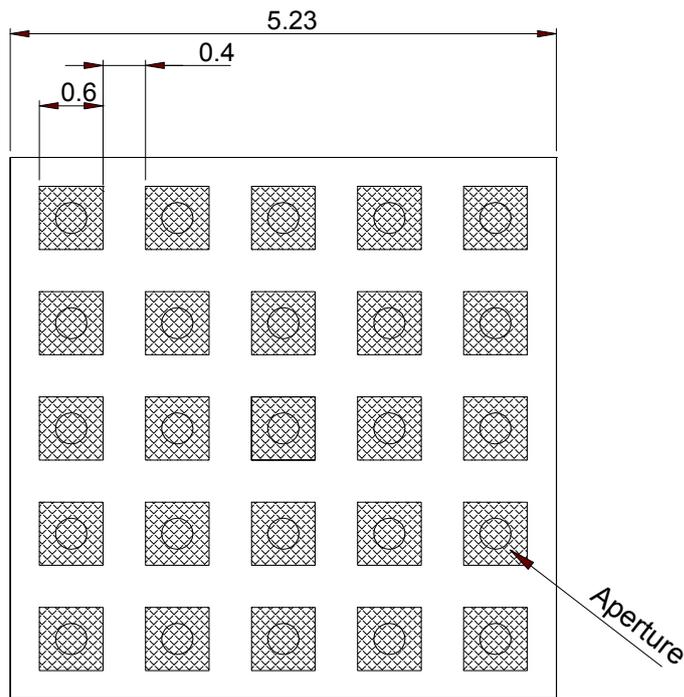


Figure 12: LX23214ILQ Recommended PCB Layout for Thermal Pad Array Footprint (PS)



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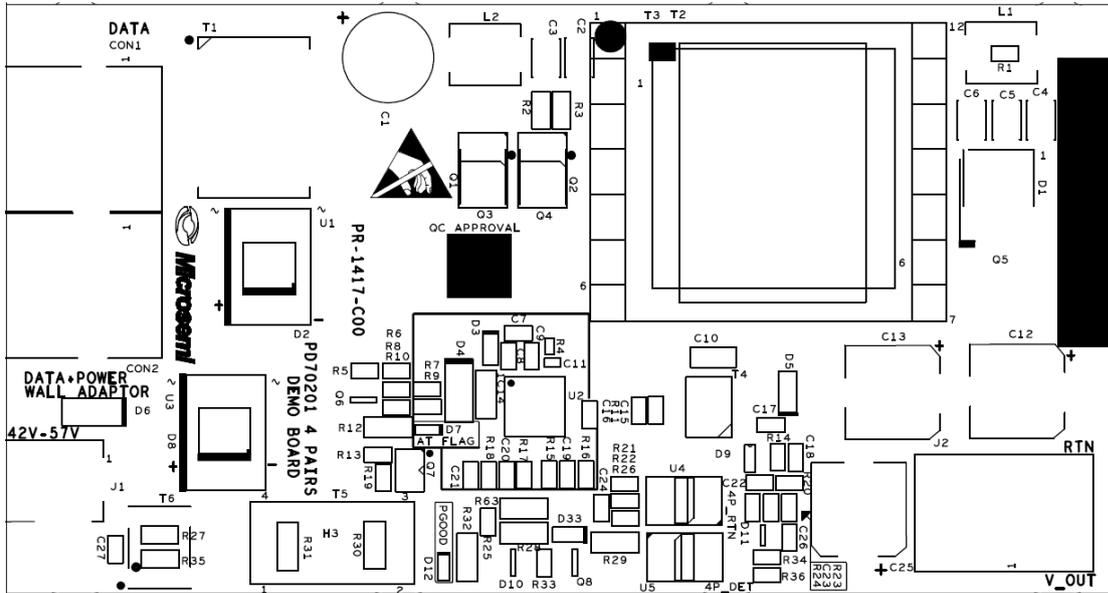


Figure 13: PD70201EVB60F12 EVB PCB Silk Top

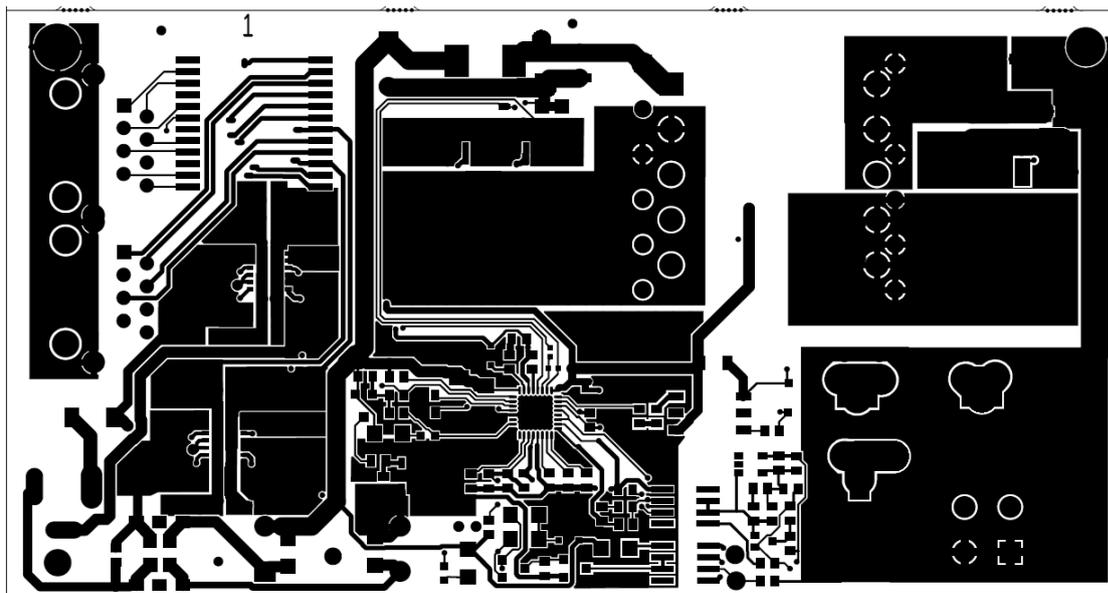


Figure 14: PD70201EVB60F12 EVB PCB Top



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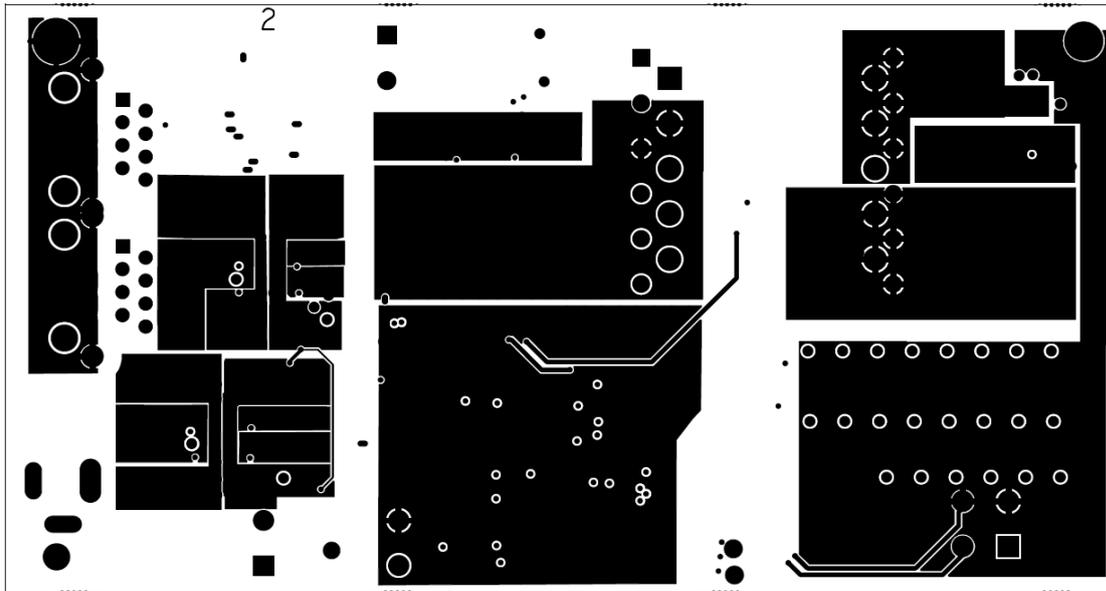


Figure 15: PD70201EVB60F12 EVB PCB Layer 2

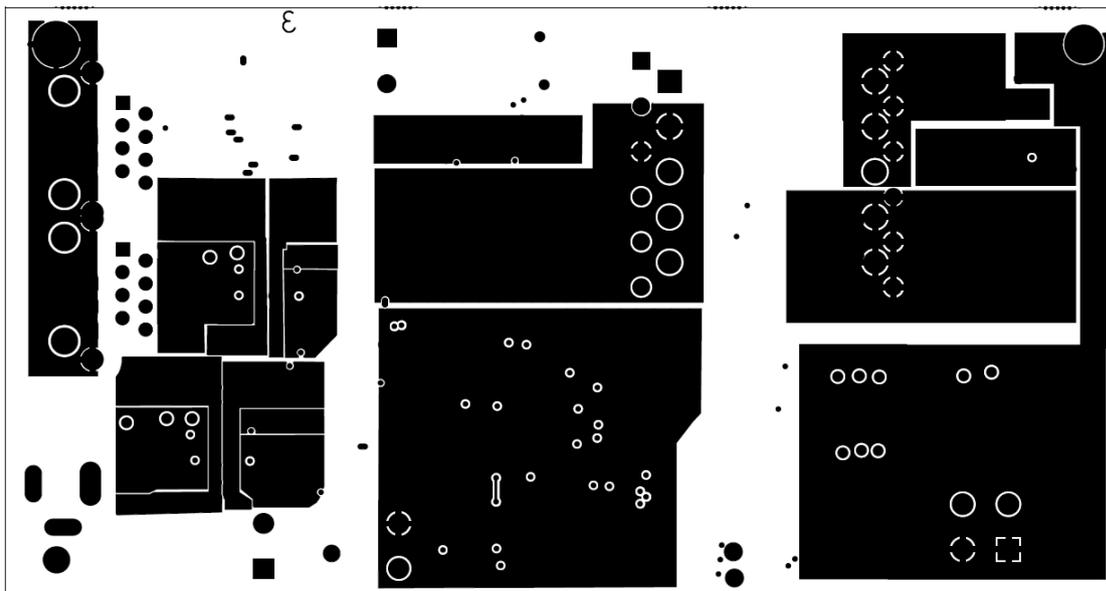


Figure 16: PD70201EVB60F12 EVB PCB Layer 3



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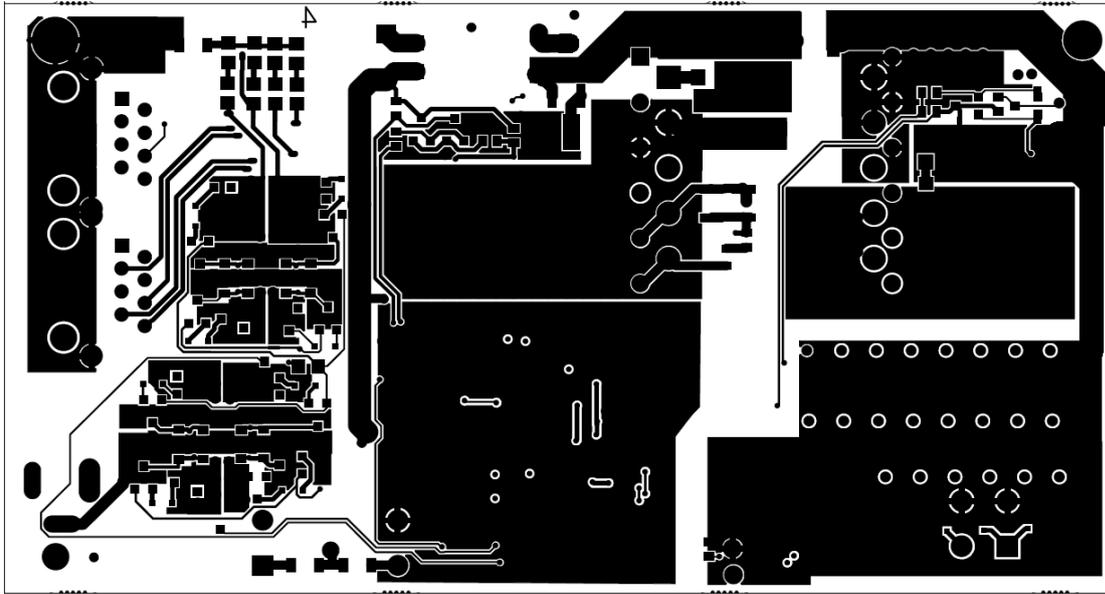


Figure 17: PD70201EVB60F12 EVB PCB Bottom (Layer 4)

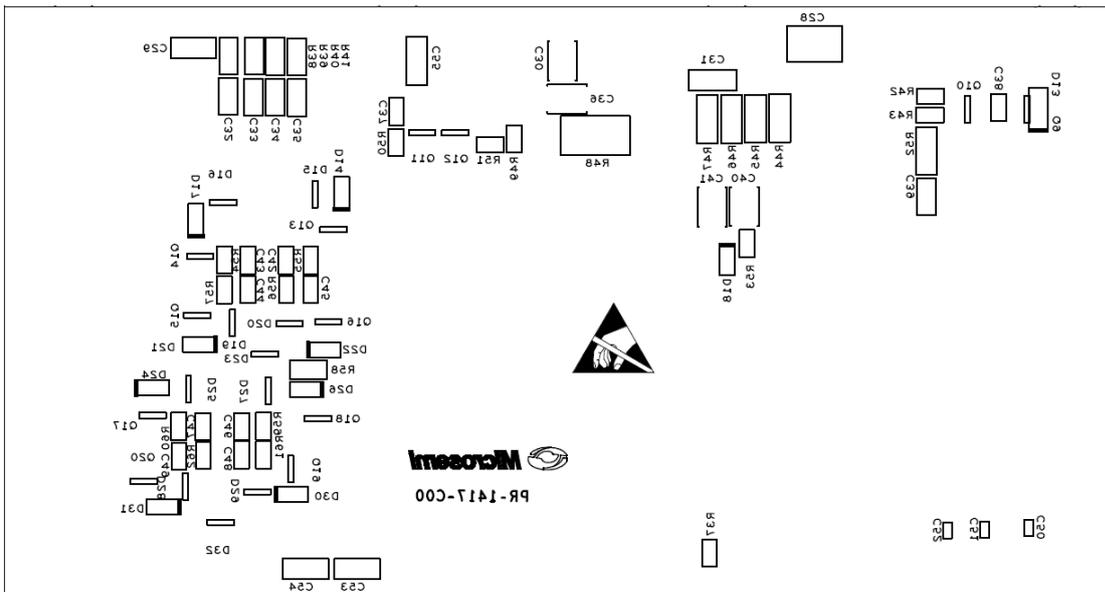


Figure 18: PD70201EVB60F12 EVB PCB Silk Bottom (Mirror)



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Revision History

Revision Level / Date	Para. Affected	Description
1.0 / 04 December. 12	-	Initial Release – preliminary version

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