Total Ionizing Dose Test Report

No. 22T-RT4G150-LG1657- K7WFH

February 3, 2022

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I. SUMMARY TABLE

Table. 1. Summary

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO_2)
2. Power Supply Current	Passed 125 krad(SiO_2)
3. Input Threshold (VIL/VIH)	Passed 125 krad(SiO_2)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO_2)
5. Propagation Delay	Passed 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters.

Table. 2. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	K7WFH
Quantity Tested	6
Serial Number (Dose)	06787 (125 krad), 06816 (125 krad), 06828 (125 krad), 06829 (125 krad), 06877 (125 krad), 06917 (125 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

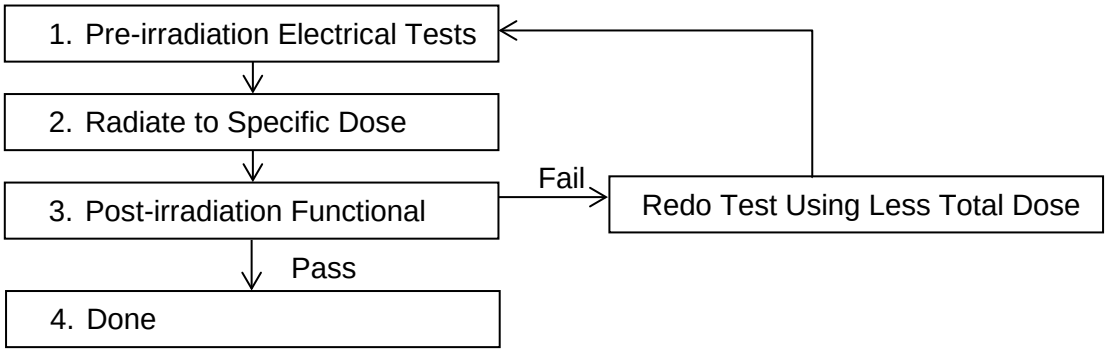

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 3. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump and PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-25 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL.

Table. 4. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
6787	125 krad	0.2852	0.297	4.14
6816	125 krad	0.2888	0.3036	5.12
6828	125 krad	0.3091	0.3219	4.14
6829	125 krad	0.3400	0.3614	6.29
6877	125 krad	0.3117	0.3286	5.42
6917	125 krad	0.2898	0.301	3.86

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
6787	125 krad	0.0157	0.0165	5.10
6816	125 krad	0.0136	0.0139	2.21
6828	125 krad	0.0129	0.0137	6.20
6829	125 krad	0.0116	0.0125	7.76
6877	125 krad	0.0118	0.0118	0.00
6917	125 krad	0.0125	0.0134	7.20

Table. 6. Pre-irradiation and Post-irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
6787	125 krad	0.0341	0.0389	14.1
6816	125 krad	0.0338	0.0383	13.3
6828	125 krad	0.0337	0.0369	9.5
6829	125 krad	0.0348	0.0382	9.8
6877	125 krad	0.0344	0.038	10.5
6917	125 krad	0.034	0.0373	9.7

Table. 7. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
6787	125 krad	0.0156	0.0156	0.00
6816	125 krad	0.0156	0.0159	1.92
6828	125 krad	0.0155	0.0164	5.81
6829	125 krad	0.0153	0.0157	2.61
6877	125 krad	0.0154	0.0157	1.95
6917	125 krad	0.0155	0.0156	0.65

The following figures (2-25) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

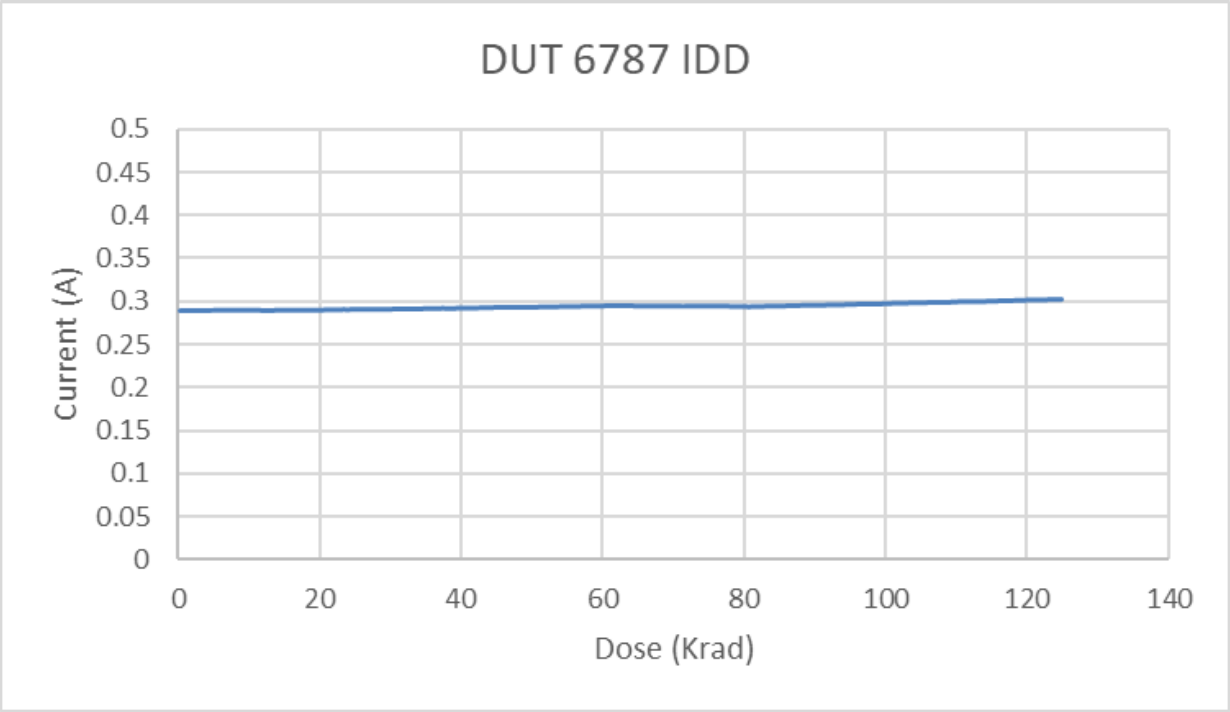

Fig. 2. DUT 06787 core power supply current (I_{DD}) versus TID

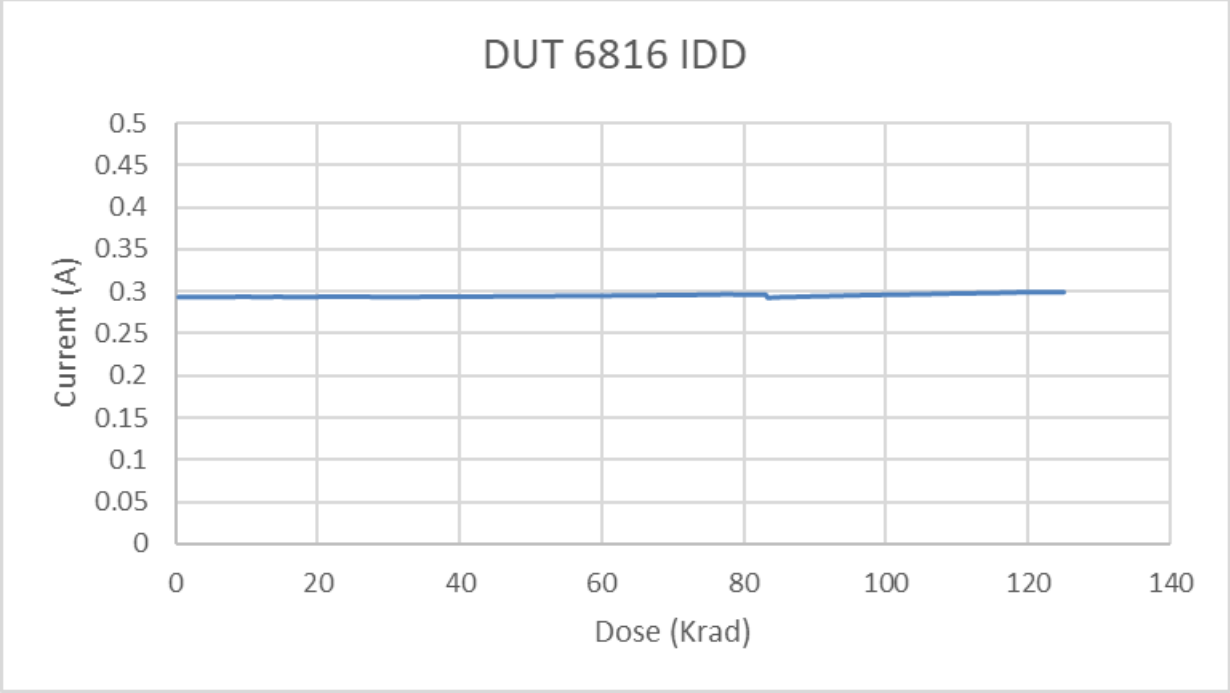

Fig. 3. DUT 06816 core power supply current (I_{DD}) versus TID

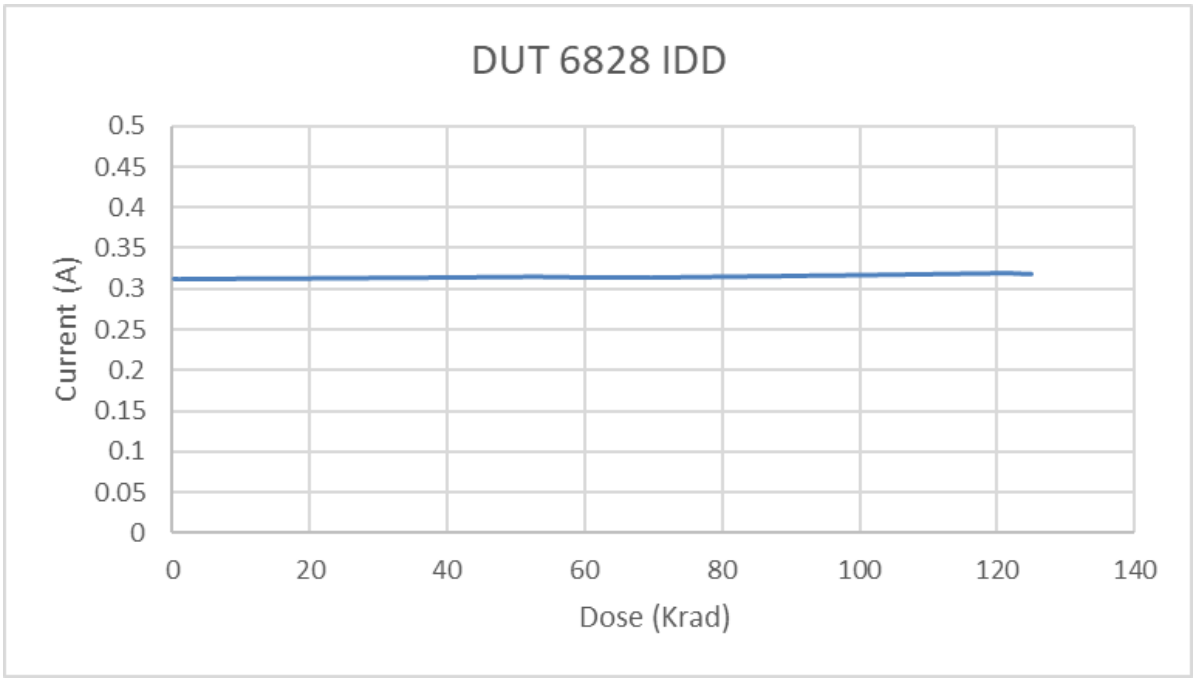

Fig. 4. DUT 06828 core power supply current (I_{DD}) versus TID

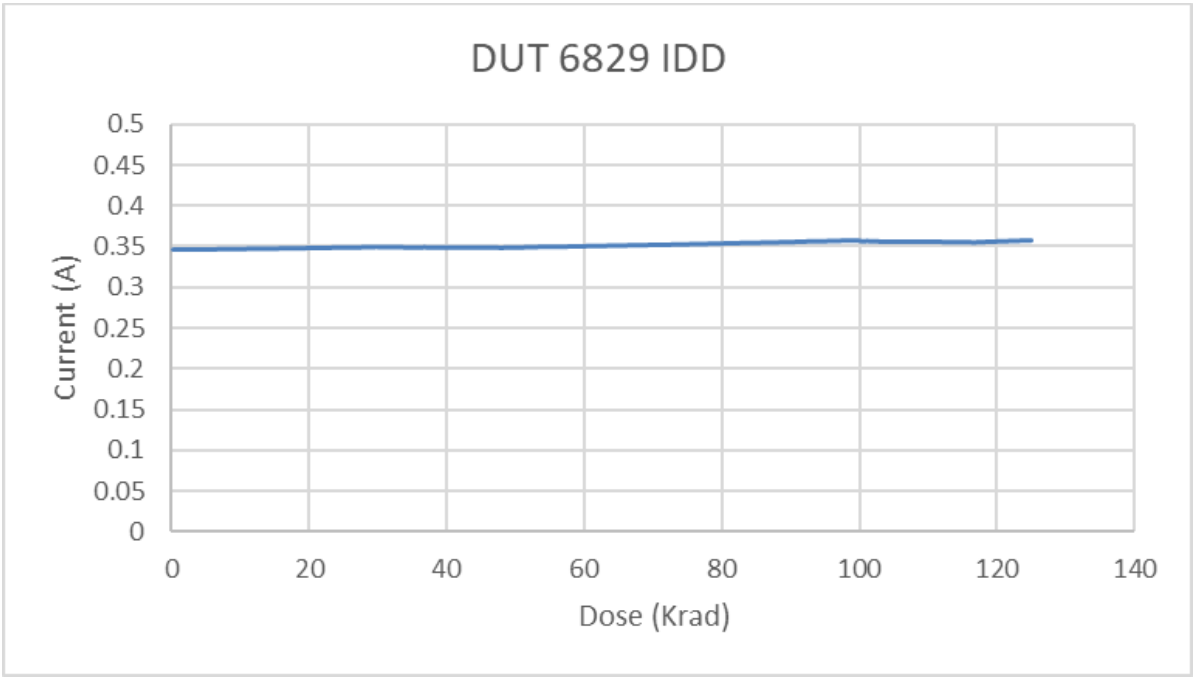

Fig. 5. DUT 06829 core power supply current (I_{DD}) versus TID

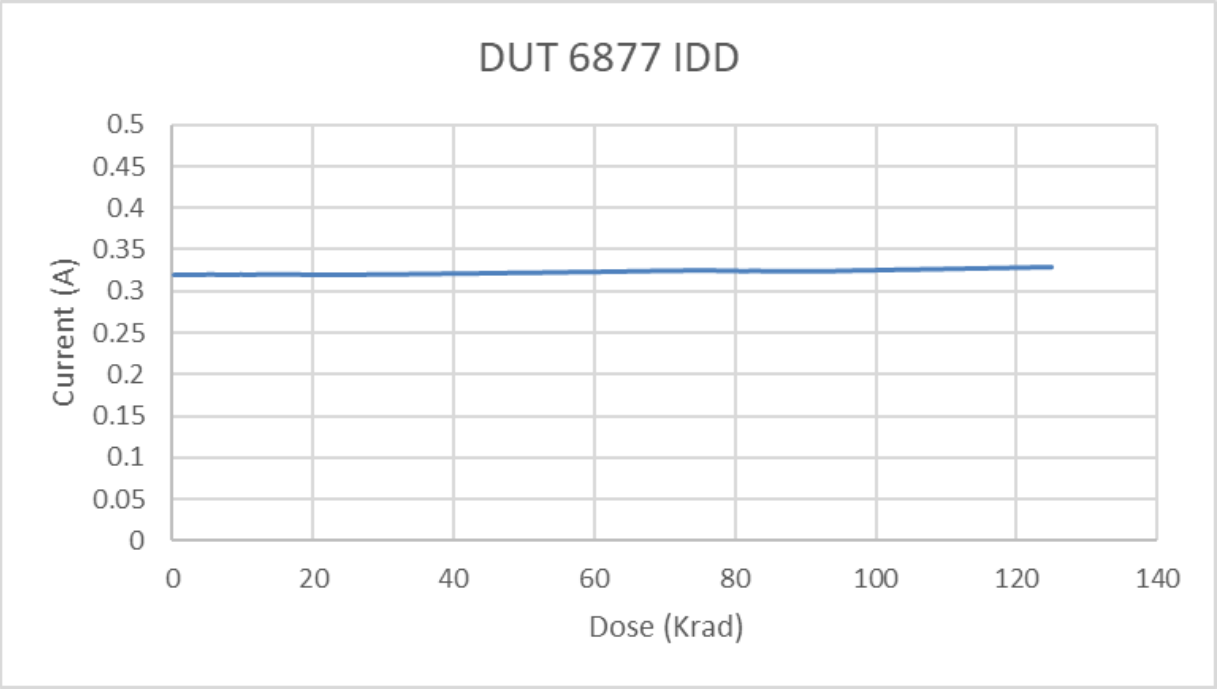

Fig. 6. DUT 06877 core power supply current (I_{DD}) versus TID

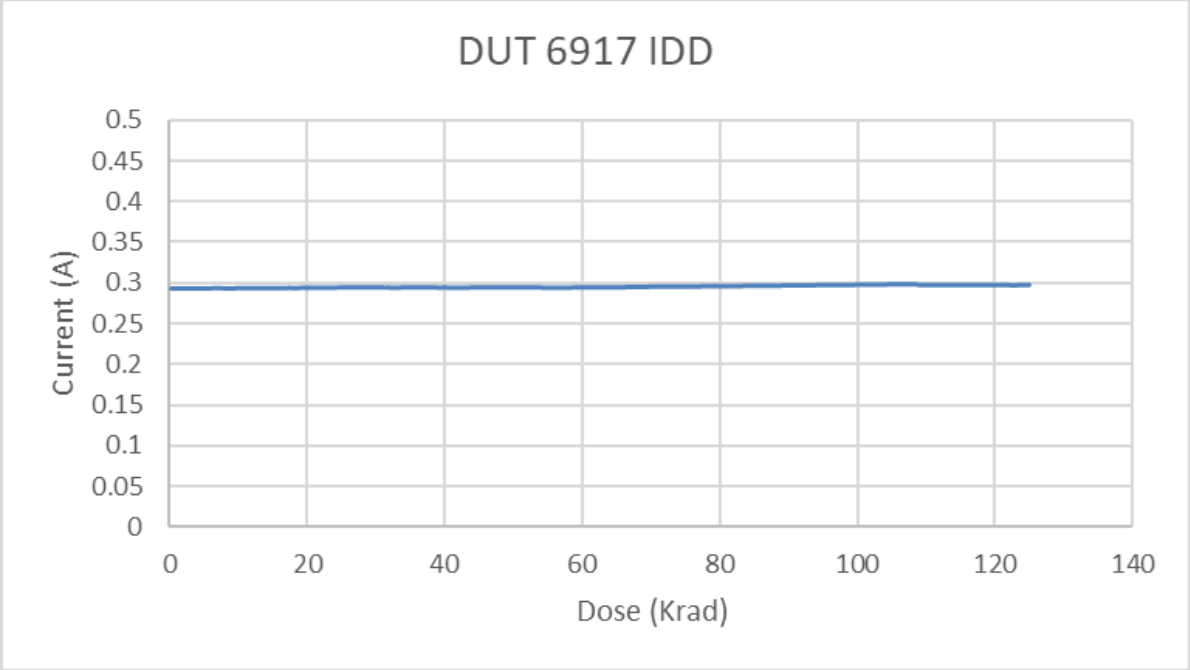

Fig. 7. DUT 06917 core power supply current (I_{DD}) versus TID

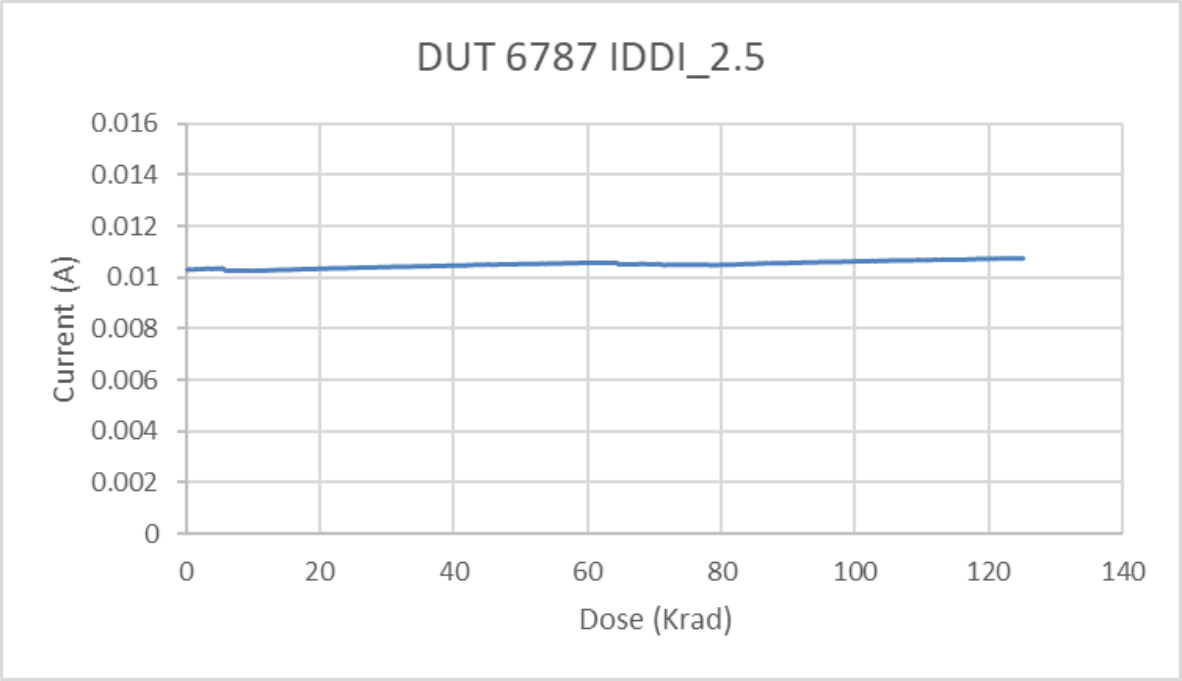

Fig. 8. DUT 06787 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

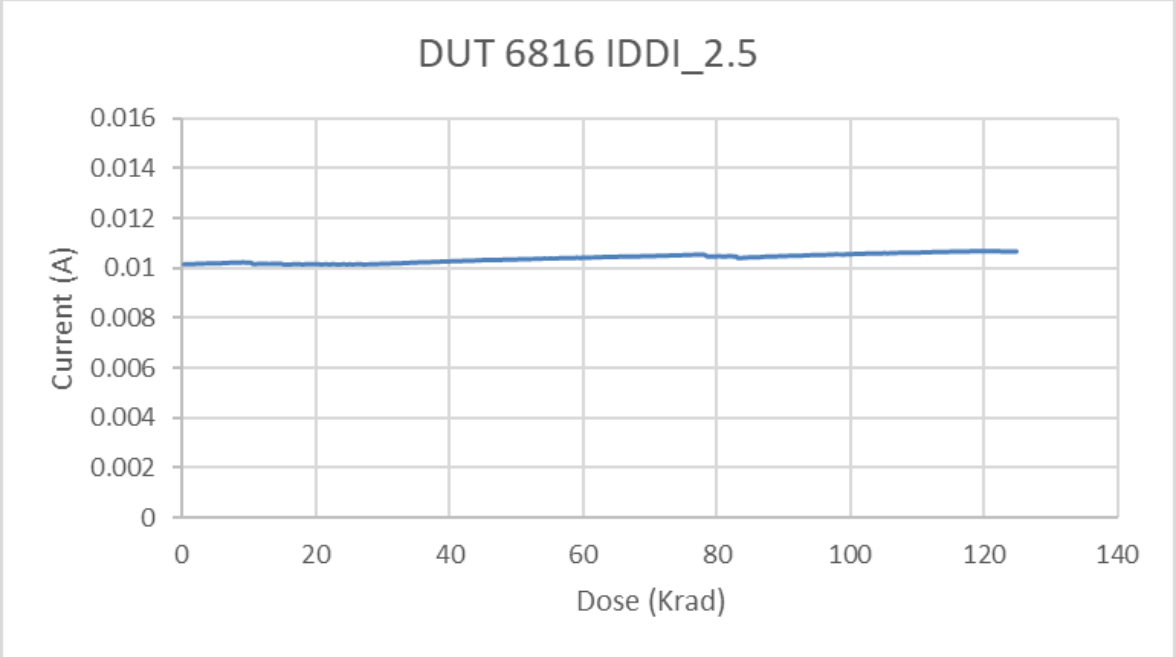

Fig. 9. DUT 06816 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

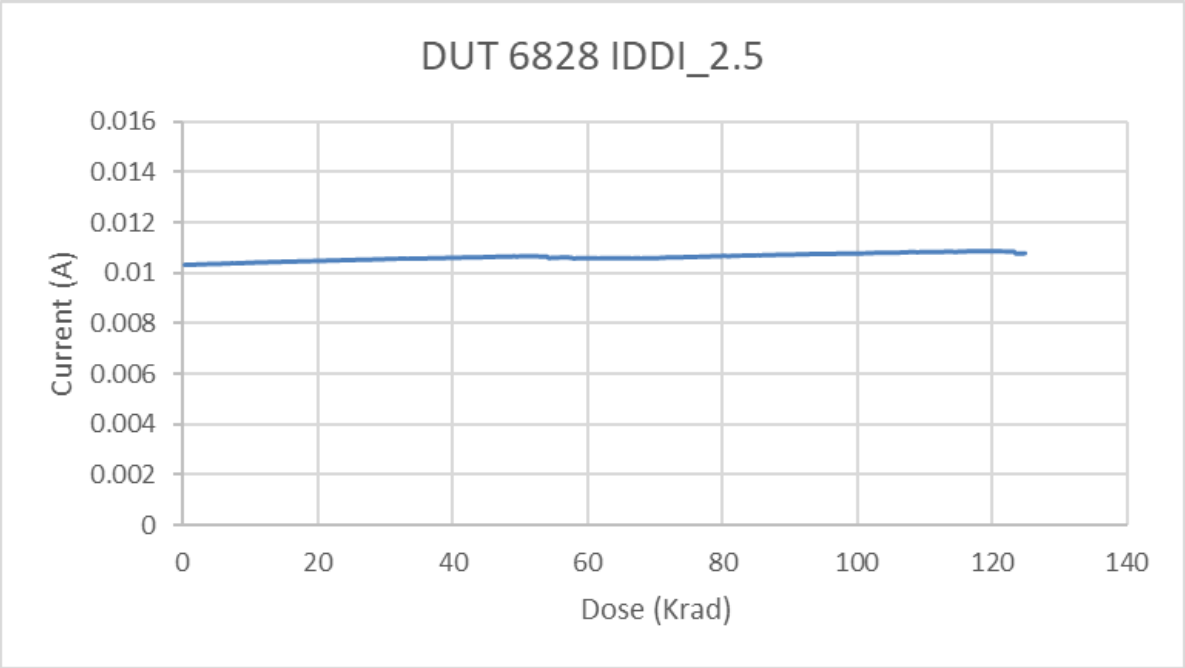

Fig. 10. DUT 06828 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

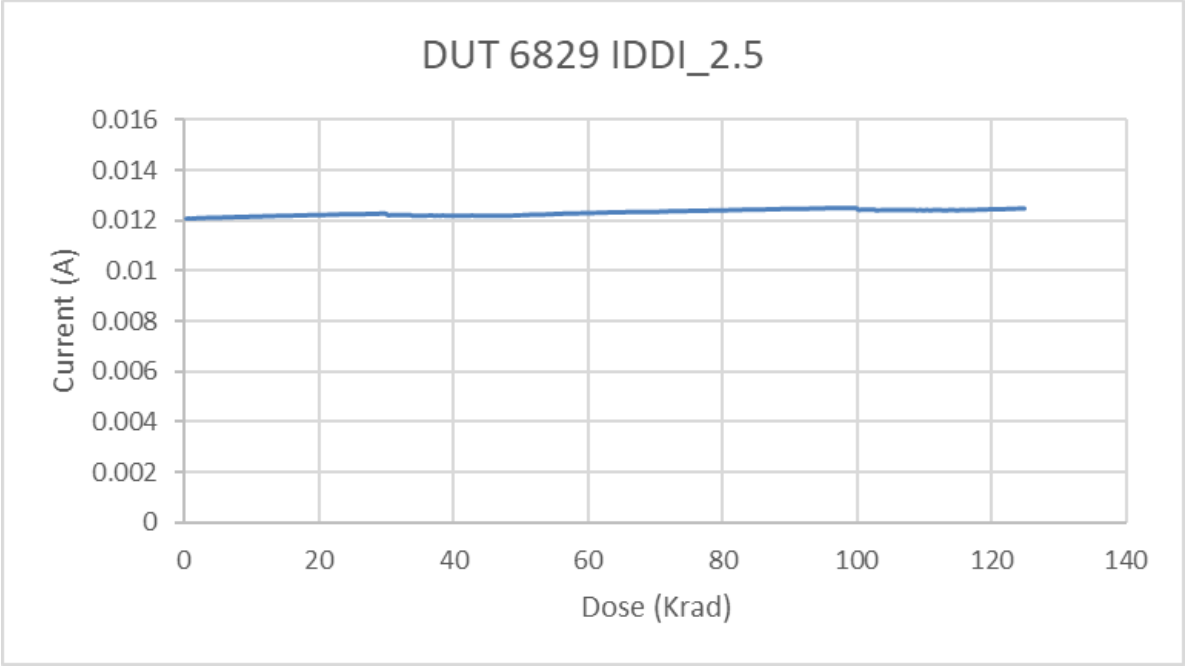

Fig. 11. DUT 06829 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

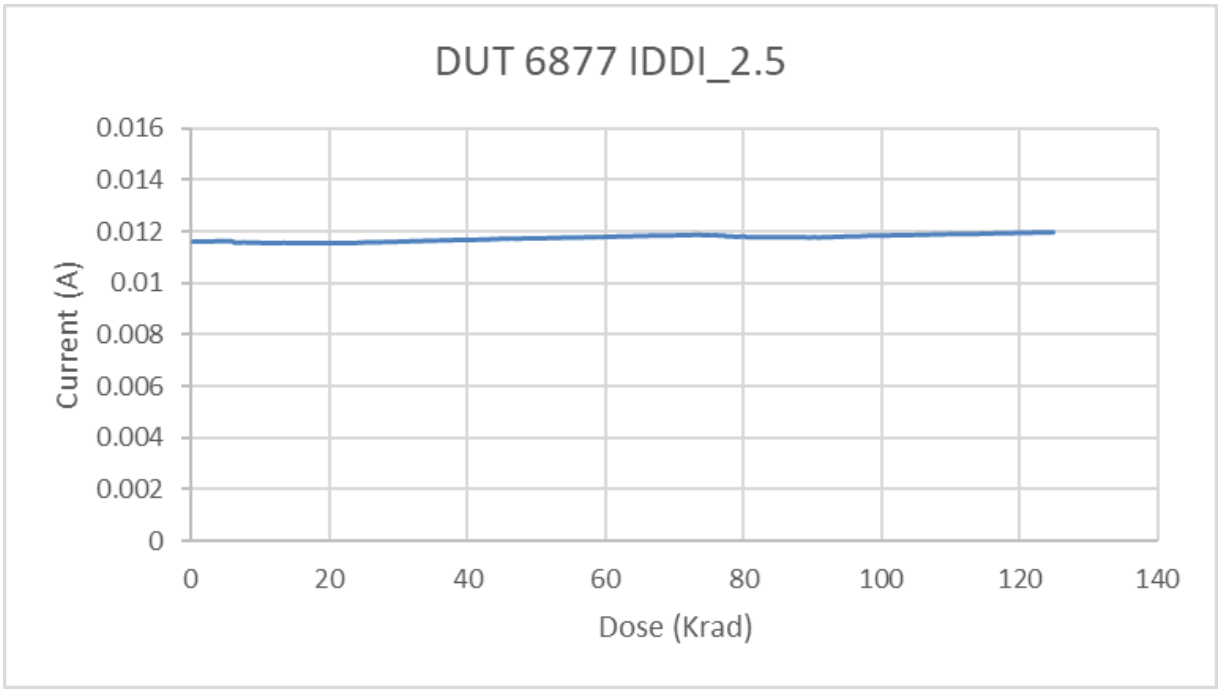

Fig. 12. DUT 06877 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

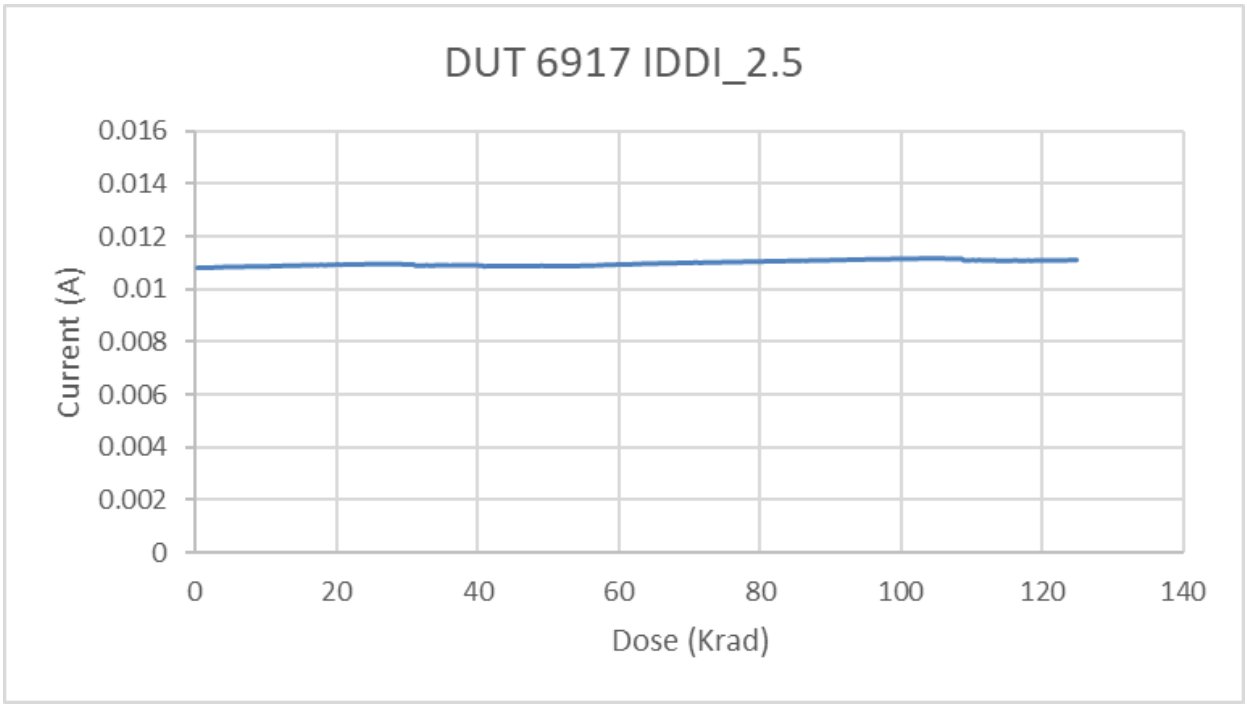

Fig. 13. DUT 06917 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

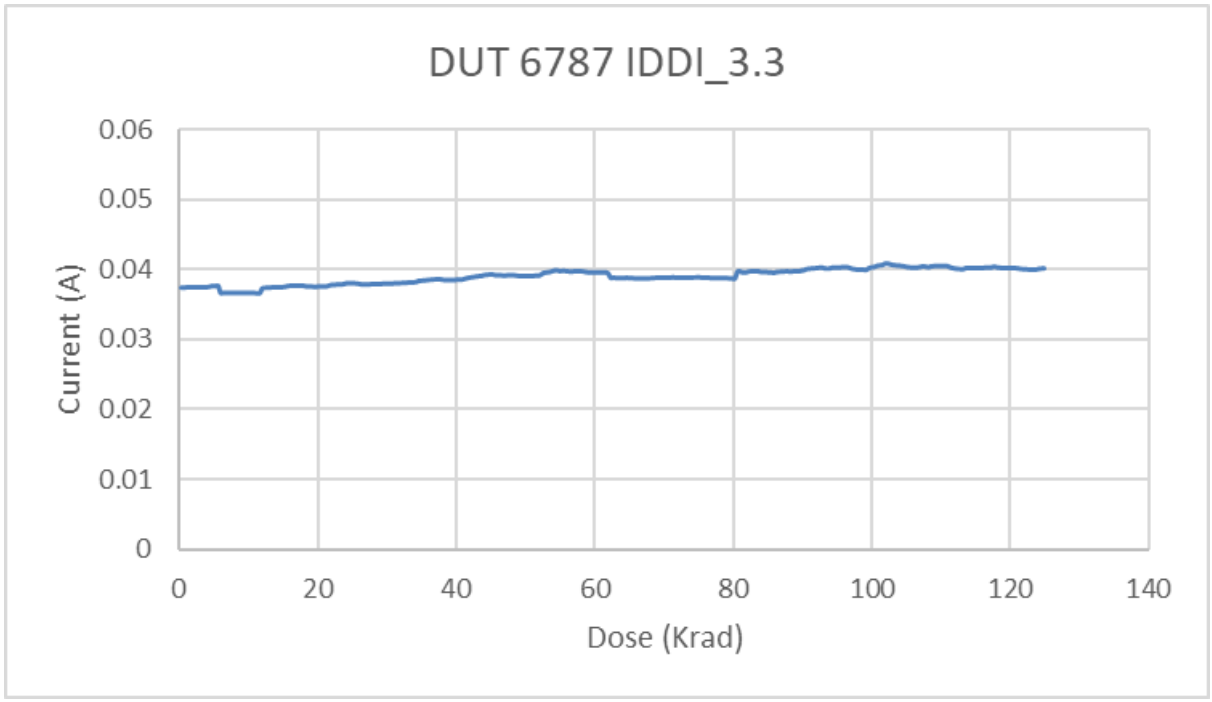

Fig. 14. DUT 06787 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

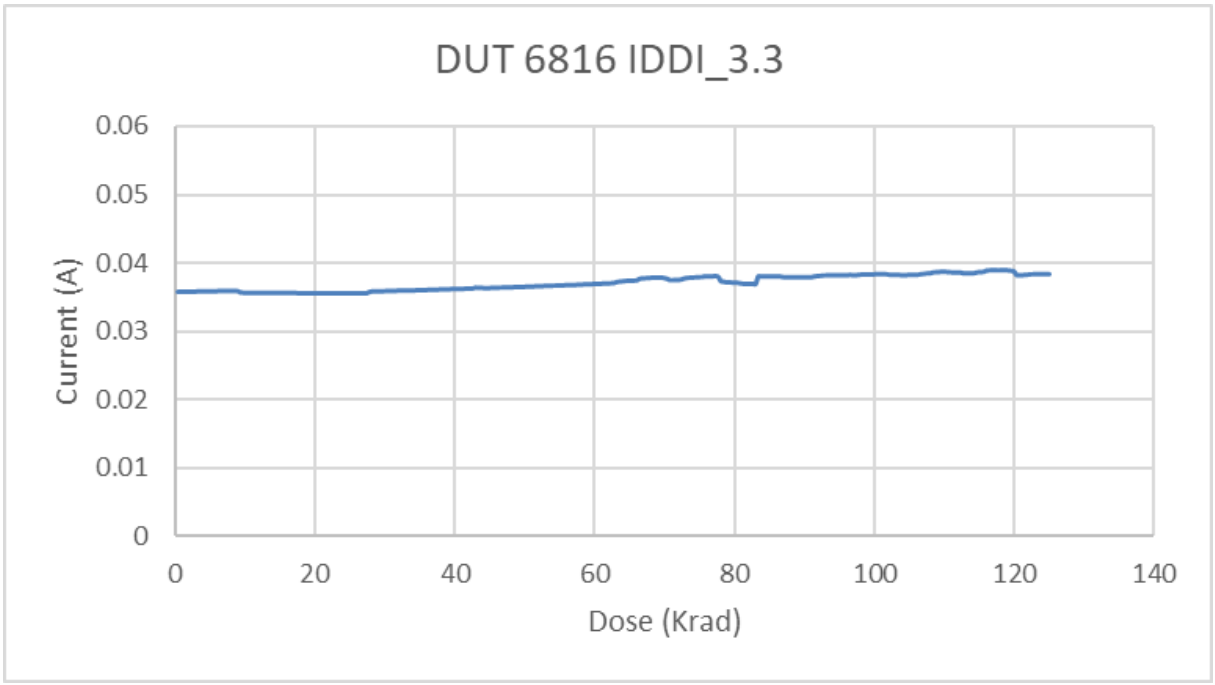

Fig. 15. DUT 06816 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

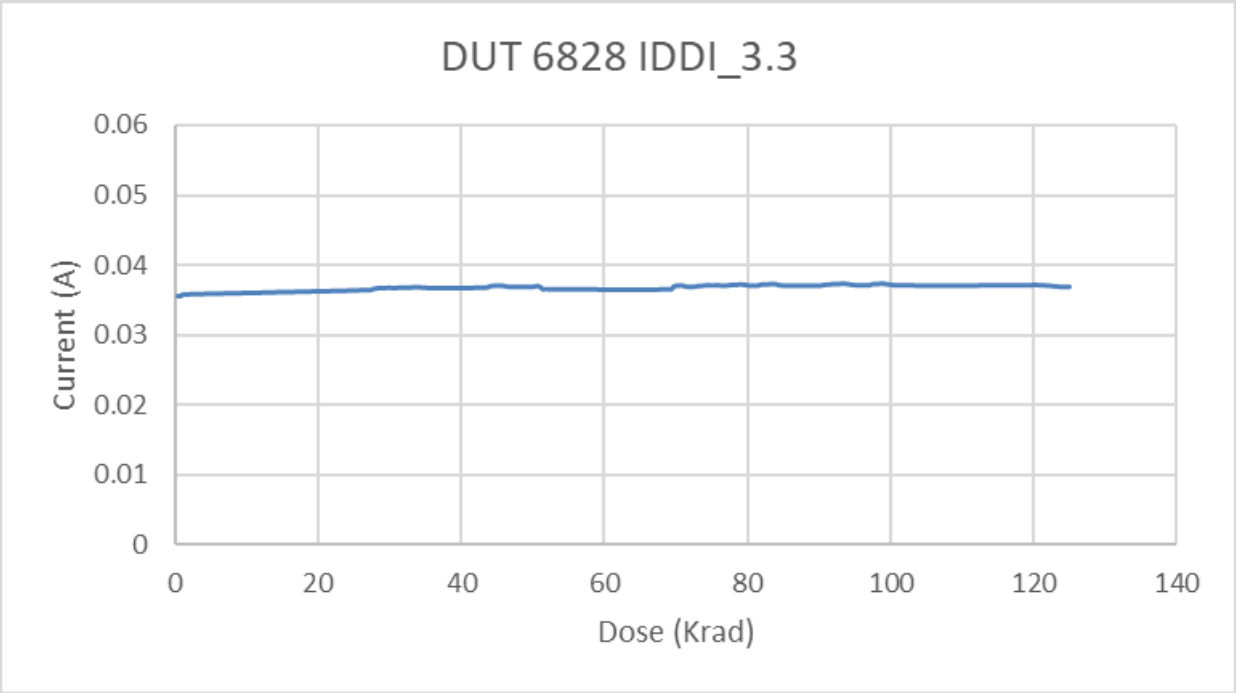

Fig. 16. DUT 06828 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

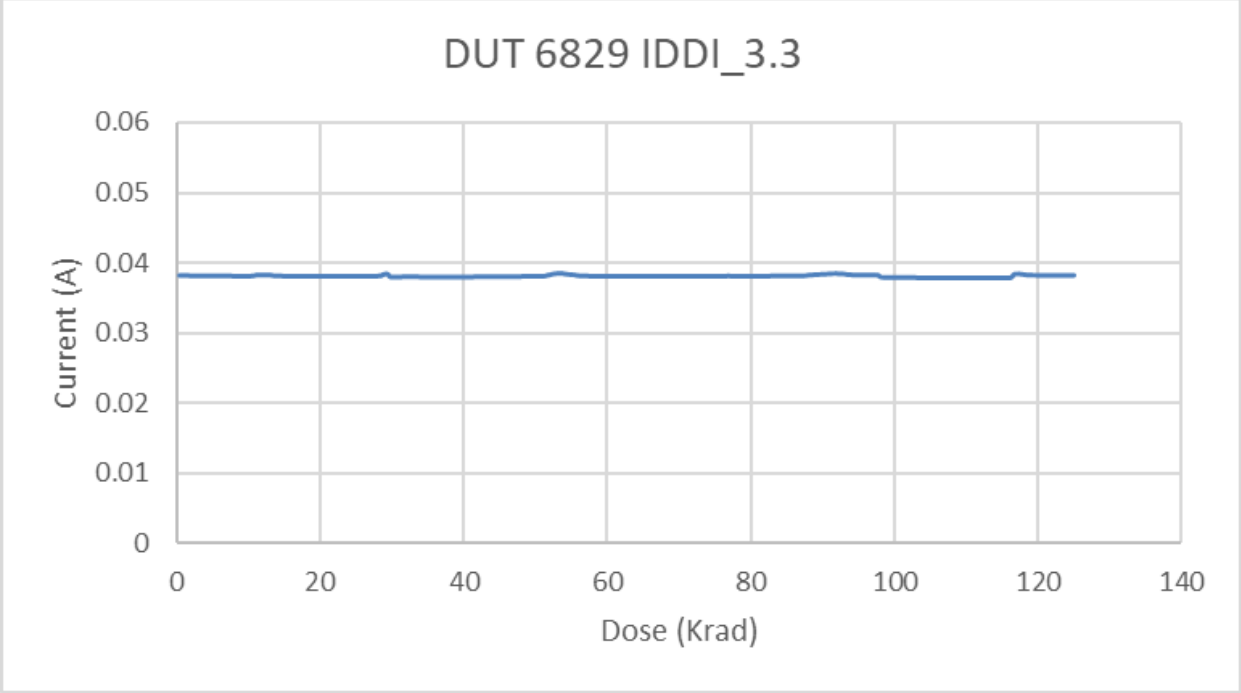

Fig. 17. DUT 06829 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

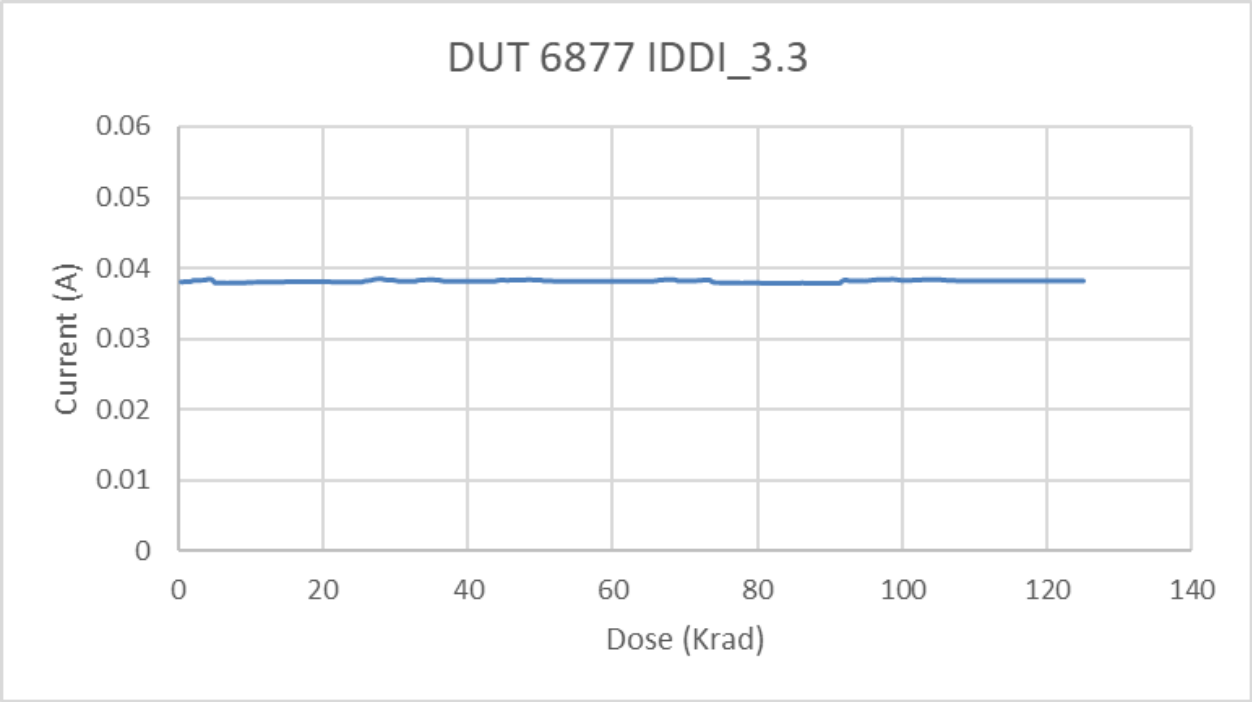

Fig. 18. DUT 06877 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

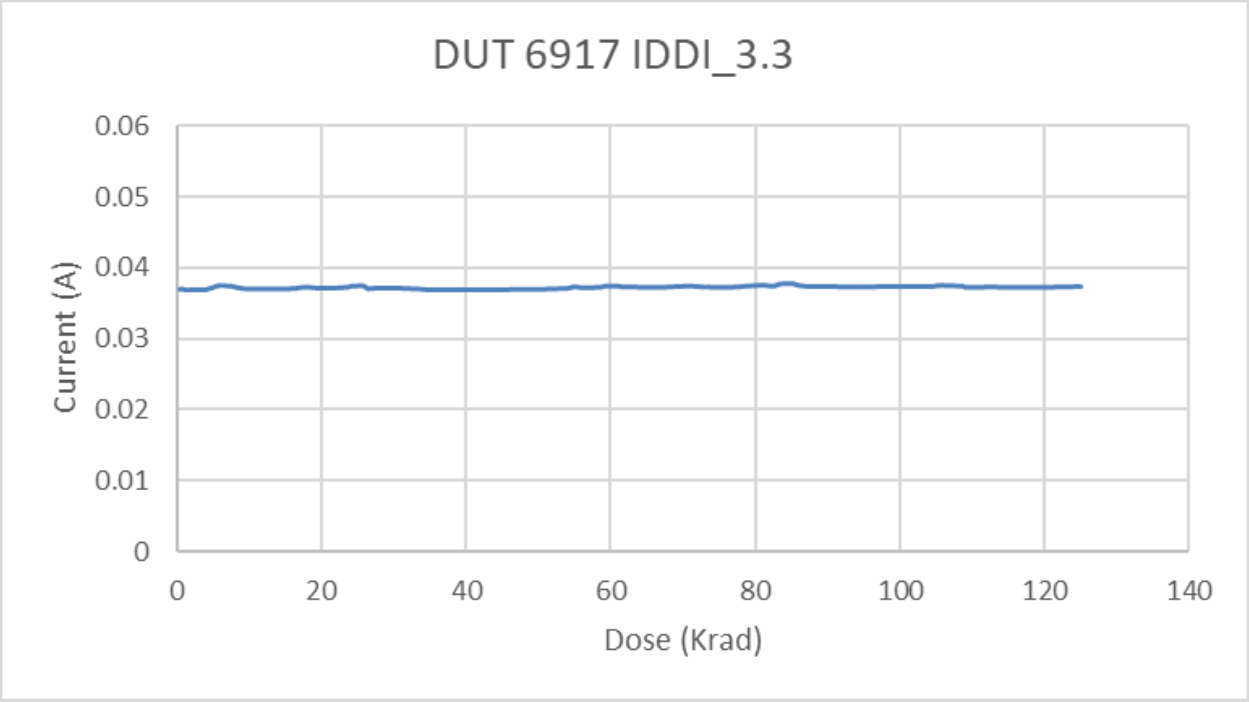

Fig. 19. DUT 06917 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

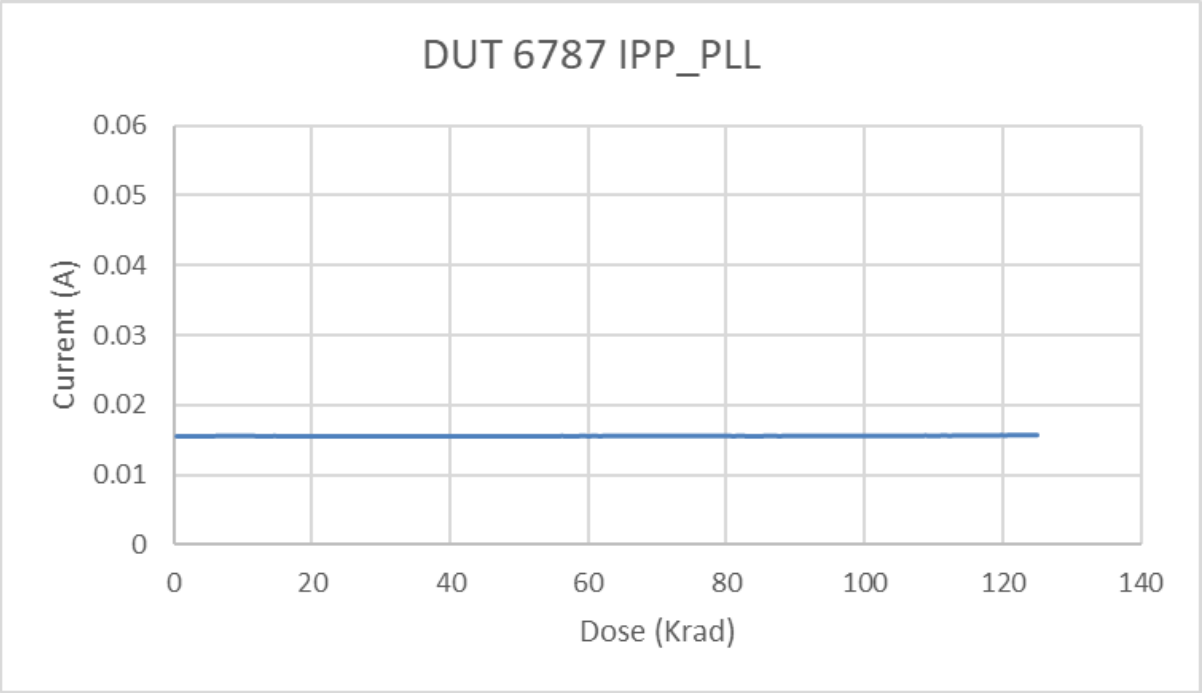

Fig. 20. DUT 06787 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

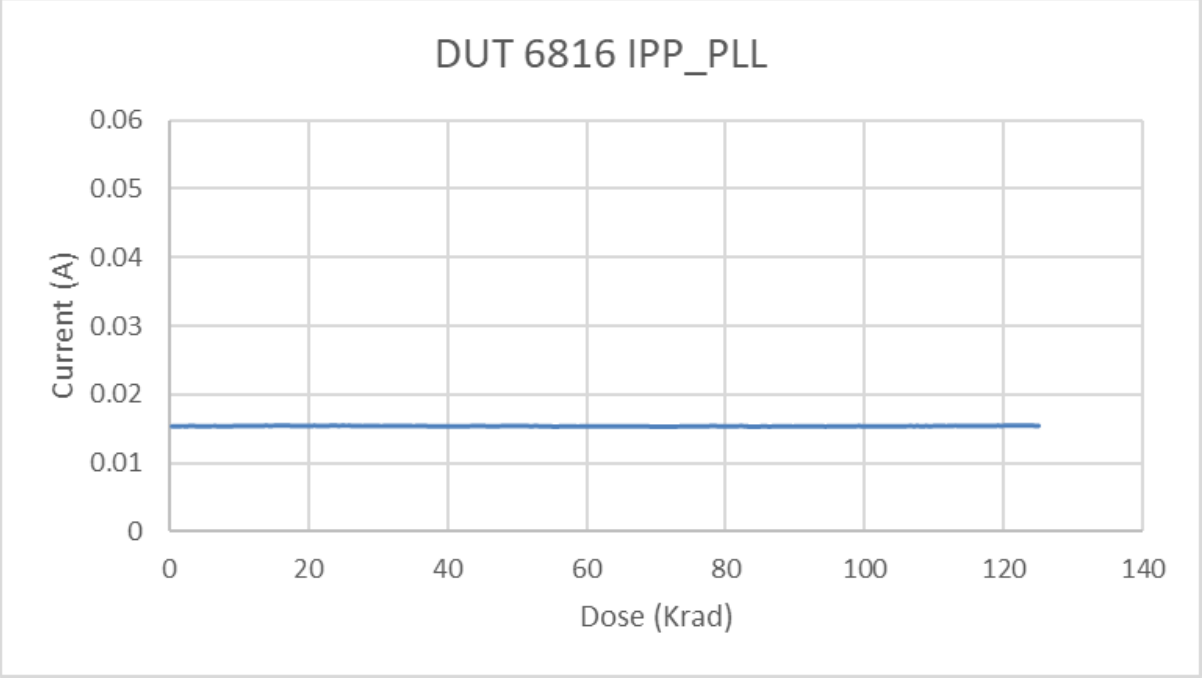

Fig. 21. DUT 06816 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

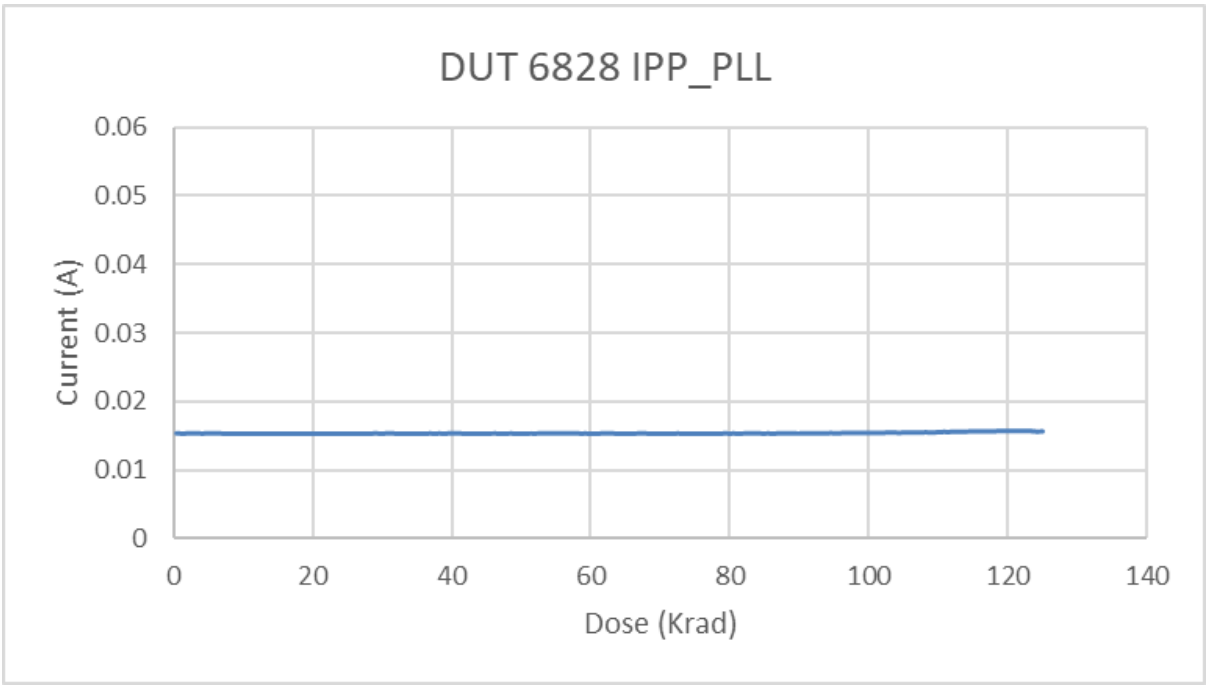

Fig. 22. DUT 06828 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

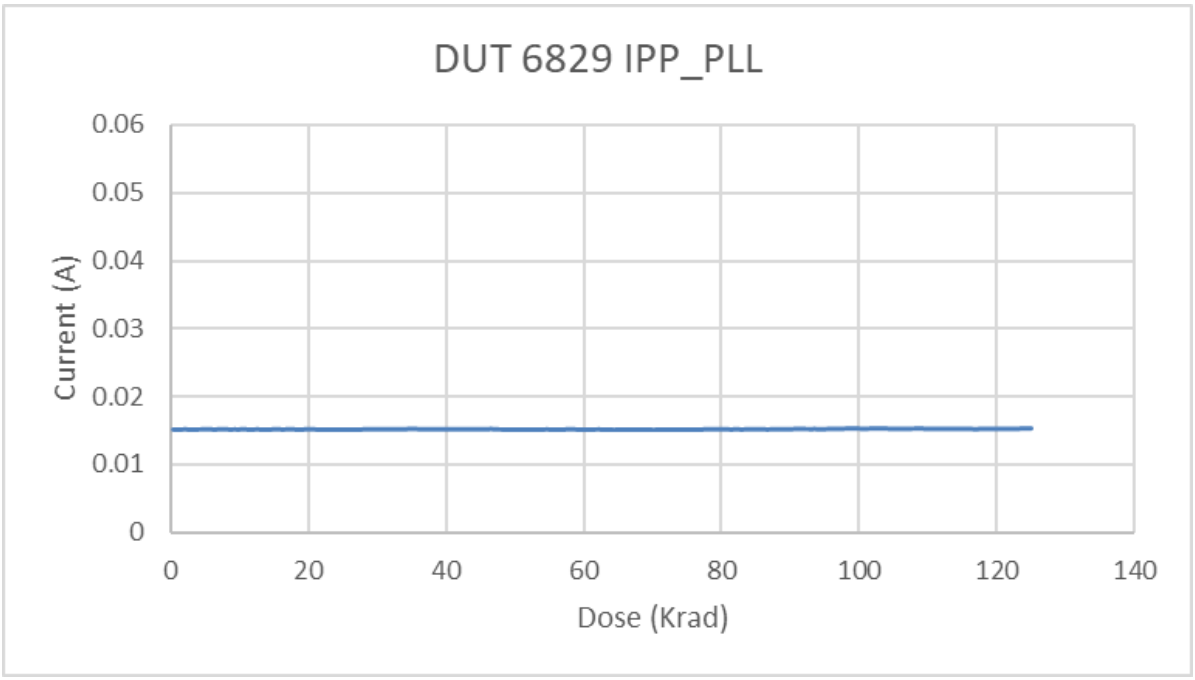

Fig. 23. DUT 06829 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

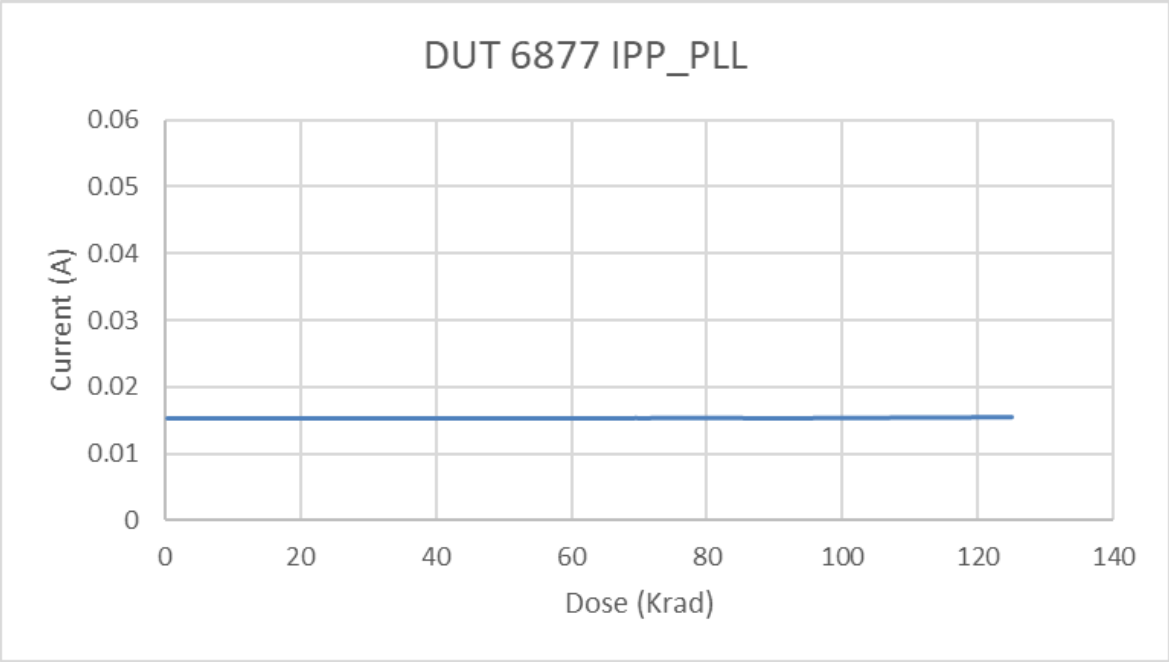

Fig. 24. DUT 06877 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

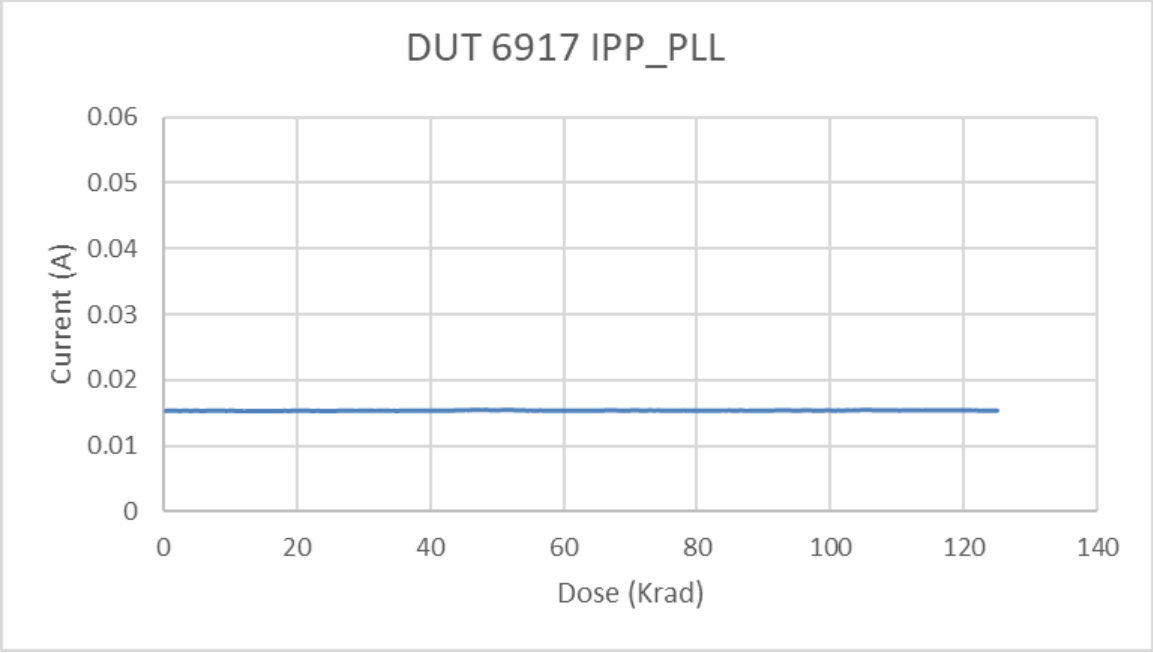

Fig. 25. DUT 06917 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 8. VIH Summary

DUT	Pre-irradiation	Post-irradiation
06787	Passed	Passed
06816	Passed	Passed
06828	Passed	Passed
06829	Passed	Passed
06877	Passed	Passed
06917	Passed	Passed

Table. 9. VIL Summary

DUT	Pre-irradiation	Post-irradiation
06787	Passed	Passed
06816	Passed	Passed
06828	Passed	Passed
06829	Passed	Passed
06877	Passed	Passed
06917	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 10 through 33 are sampled on several pins used in the burn in design.

Table. 10. LVCMOS 25 VOH – DUT 06787

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.131	2.131	2.201	2.201	2.171	2.172	2.152	2.154	2.119	2.120	2.104	2.107
EPCSRST_N_0	B31	2.129	2.132	2.194	2.201	2.161	2.171	2.138	2.152	2.097	2.118	2.079	2.104
EPCSRST_N_1	B32	2.134	2.134	2.203	2.203	2.175	2.175	2.155	2.155	2.124	2.124	2.110	2.111
EPCSRST_N_2	B34	2.132	2.132	2.202	2.201	2.172	2.172	2.152	2.152	2.119	2.120	2.105	2.106
EPCSRST_N_3	B35	2.133	2.133	2.203	2.203	2.174	2.175	2.154	2.155	2.123	2.124	2.110	2.111
EPCSRST_N_4	B36	2.132	2.132	2.201	2.201	2.172	2.172	2.151	2.151	2.118	2.118	2.104	2.104
EPCSRST_N_5	B37	2.132	2.133	2.200	2.202	2.171	2.174	2.150	2.154	2.116	2.122	2.102	2.109
MONITOR	K23	2.134	2.133	2.204	2.204	2.176	2.175	2.156	2.156	2.126	2.125	2.113	2.113
PLL_MON	L20	2.136	2.134	2.208	2.206	2.182	2.180	2.165	2.162	2.139	2.134	2.128	2.123
TOGGLE_MON	L22	2.134	2.133	2.205	2.205	2.178	2.178	2.159	2.160	2.130	2.131	2.118	2.119

Table. 11. LVCMOS 25 VOH – DUT 06816

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.132	2.132	2.201	2.202	2.172	2.172	2.153	2.154	2.119	2.121	2.104	2.107
EPCSRST_N_0	B31	2.129	2.133	2.194	2.201	2.160	2.172	2.137	2.152	2.095	2.118	2.077	2.104
EPCSRST_N_1	B32	2.134	2.134	2.204	2.204	2.175	2.175	2.155	2.156	2.123	2.124	2.110	2.111
EPCSRST_N_2	B34	2.134	2.134	2.202	2.202	2.173	2.174	2.152	2.153	2.119	2.120	2.105	2.107
EPCSRST_N_3	B35	2.135	2.135	2.204	2.204	2.176	2.176	2.156	2.157	2.124	2.126	2.111	2.112
EPCSRST_N_4	B36	2.134	2.134	2.203	2.202	2.173	2.173	2.152	2.153	2.119	2.120	2.105	2.106
EPCSRST_N_5	B37	2.134	2.135	2.202	2.204	2.172	2.175	2.151	2.156	2.118	2.124	2.103	2.111
MONITOR	K23	2.134	2.134	2.204	2.204	2.176	2.176	2.156	2.156	2.126	2.125	2.113	2.113
PLL_MON	L20	2.136	2.134	2.208	2.206	2.182	2.180	2.165	2.162	2.138	2.134	2.127	2.123
TOGGLE_MON	L22	2.134	2.133	2.205	2.205	2.178	2.178	2.159	2.159	2.130	2.131	2.118	2.119

Table. 12. LVCMOS 25 VOH – DUT 06828

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.132	2.131	2.201	2.201	2.171	2.172	2.152	2.153	2.119	2.119	2.104	2.106
EPCSRST_N_0	B31	2.129	2.132	2.194	2.201	2.160	2.171	2.137	2.152	2.096	2.117	2.077	2.103
EPCSRST_N_1	B32	2.134	2.133	2.203	2.203	2.174	2.174	2.154	2.154	2.122	2.123	2.109	2.110
EPCSRST_N_2	B34	2.132	2.132	2.201	2.201	2.171	2.172	2.150	2.151	2.117	2.118	2.103	2.104
EPCSRST_N_3	B35	2.133	2.133	2.202	2.203	2.174	2.174	2.154	2.154	2.122	2.123	2.109	2.110
EPCSRST_N_4	B36	2.133	2.132	2.201	2.201	2.172	2.172	2.151	2.151	2.118	2.118	2.104	2.104
EPCSRST_N_5	B37	2.132	2.133	2.200	2.203	2.170	2.174	2.148	2.154	2.114	2.123	2.099	2.109
MONITOR	K23	2.134	2.133	2.204	2.204	2.175	2.175	2.156	2.155	2.125	2.125	2.112	2.112
PLL_MON	L20	2.136	2.134	2.208	2.206	2.182	2.180	2.165	2.162	2.139	2.134	2.128	2.123
TOGGLE_MON	L22	2.134	2.134	2.205	2.205	2.178	2.178	2.158	2.159	2.129	2.130	2.117	2.119

Table. 13. LVCMOS 25 VOH – DUT 06829

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.132	2.131	2.201	2.201	2.172	2.172	2.153	2.153	2.120	2.120	2.106	2.106
EPCSRST_N_0	B31	2.127	2.131	2.190	2.200	2.155	2.171	2.130	2.152	2.085	2.118	2.065	2.103
EPCSRST_N_1	B32	2.133	2.133	2.203	2.203	2.175	2.175	2.155	2.155	2.123	2.123	2.110	2.110
EPCSRST_N_2	B34	2.132	2.131	2.201	2.201	2.172	2.172	2.151	2.152	2.118	2.120	2.105	2.106
EPCSRST_N_3	B35	2.133	2.133	2.203	2.203	2.174	2.174	2.154	2.155	2.123	2.124	2.110	2.111
EPCSRST_N_4	B36	2.131	2.131	2.201	2.200	2.171	2.171	2.150	2.151	2.118	2.118	2.104	2.104
EPCSRST_N_5	B37	2.131	2.132	2.199	2.202	2.169	2.174	2.147	2.154	2.112	2.122	2.097	2.109
MONITOR	K23	2.133	2.132	2.203	2.203	2.175	2.175	2.156	2.155	2.125	2.124	2.111	2.112
PLL_MON	L20	2.135	2.134	2.208	2.206	2.181	2.179	2.164	2.161	2.138	2.133	2.126	2.122
TOGGLE_MON	L22	2.133	2.133	2.205	2.205	2.177	2.178	2.158	2.159	2.129	2.130	2.117	2.118

Table. 14. LVCMOS 25 VOH – DUT 06877

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.130	2.130	2.201	2.200	2.171	2.171	2.153	2.153	2.120	2.119	2.106	2.106
EPCSRST_N_0	B31	2.127	2.130	2.193	2.200	2.159	2.170	2.137	2.151	2.095	2.117	2.078	2.103
EPCSRST_N_1	B32	2.131	2.132	2.202	2.202	2.173	2.174	2.153	2.154	2.122	2.123	2.108	2.110
EPCSRST_N_2	B34	2.130	2.131	2.200	2.201	2.171	2.172	2.150	2.152	2.118	2.119	2.103	2.105
EPCSRST_N_3	B35	2.131	2.132	2.201	2.202	2.173	2.174	2.153	2.154	2.122	2.123	2.108	2.111
EPCSRST_N_4	B36	2.130	2.131	2.200	2.200	2.170	2.171	2.149	2.150	2.116	2.117	2.102	2.103
EPCSRST_N_5	B37	2.129	2.131	2.198	2.201	2.168	2.173	2.146	2.153	2.111	2.121	2.096	2.108
MONITOR	K23	2.131	2.131	2.202	2.202	2.173	2.174	2.154	2.154	2.123	2.123	2.110	2.111
PLL_MON	L20	2.133	2.132	2.206	2.205	2.180	2.178	2.163	2.160	2.136	2.133	2.126	2.122
TOGGLE_MON	L22	2.131	2.132	2.203	2.204	2.176	2.177	2.156	2.158	2.127	2.129	2.115	2.118

Table. 15. LVCMOS 25 VOH – DUT 06917

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.131	2.131	2.201	2.201	2.172	2.172	2.153	2.153	2.120	2.120	2.106	2.106
EPCSRST_N_0	B31	2.128	2.131	2.193	2.200	2.160	2.171	2.137	2.151	2.096	2.118	2.078	2.103
EPCSRST_N_1	B32	2.133	2.133	2.203	2.203	2.174	2.174	2.154	2.155	2.123	2.123	2.110	2.110
EPCSRST_N_2	B34	2.132	2.132	2.201	2.201	2.172	2.172	2.151	2.152	2.118	2.119	2.104	2.105
EPCSRST_N_3	B35	2.133	2.132	2.203	2.203	2.174	2.174	2.154	2.155	2.123	2.124	2.110	2.111
EPCSRST_N_4	B36	2.131	2.131	2.201	2.200	2.171	2.171	2.151	2.151	2.118	2.118	2.104	2.104
EPCSRST_N_5	B37	2.131	2.132	2.200	2.202	2.170	2.174	2.149	2.154	2.115	2.122	2.101	2.109
MONITOR	K23	2.133	2.132	2.203	2.203	2.175	2.175	2.155	2.155	2.125	2.124	2.112	2.111
PLL_MON	L20	2.135	2.133	2.207	2.206	2.181	2.179	2.164	2.161	2.138	2.133	2.127	2.122
TOGGLE_MON	L22	2.133	2.132	2.204	2.204	2.177	2.177	2.158	2.158	2.129	2.130	2.117	2.118

Table. 16. LVCMOS 25 VOL – DUT 06787

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	238.2	237.7	169.9	168.8	198.5	197.1	222.1	220.2	254.1	251.1	267.9	264.7
EPCSRST_N_0	B31	239.8	236.1	176.7	169.2	209.0	197.8	236.6	221.5	276.3	253.6	294.0	267.7
EPCSRST_N_1	B32	235.2	235.2	167.0	166.9	194.7	194.5	214.7	215.0	245.4	245.3	258.8	258.4
EPCSRST_N_2	B34	237.6	237.7	169.3	169.0	197.5	197.2	218.5	218.3	250.3	249.7	264.1	263.2
EPCSRST_N_3	B35	236.8	236.8	168.2	167.7	196.1	195.3	216.4	215.9	247.2	246.2	260.4	258.9
EPCSRST_N_4	B36	237.5	237.8	169.6	169.7	198.3	198.2	219.6	219.8	251.6	251.6	265.6	265.4
EPCSRST_N_5	B37	237.7	236.9	170.3	168.3	199.4	196.1	220.8	217.1	253.6	247.6	267.9	260.6
MONITOR	K23	236.0	235.7	167.2	166.9	194.4	194.1	214.9	213.9	244.4	243.4	257.1	255.9
PLL_MON	L20	233.7	233.9	162.7	163.8	188.1	189.7	206.9	208.9	232.5	235.5	243.1	246.6
TOGGLE_MON	L22	235.2	234.9	165.7	165.1	192.1	191.3	212.1	211.0	240.4	238.9	252.4	250.6

Table. 17. LVCMOS 25 VOL – DUT 06816

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	236.2	235.2	168.8	167.6	197.4	195.8	220.9	219.0	252.8	250.0	266.7	263.8
EPCSRST_N_0	B31	239.2	234.7	176.4	168.1	209.2	196.8	237.2	220.7	277.5	252.7	295.6	267.0
EPCSRST_N_1	B32	233.9	233.6	166.4	165.9	194.0	193.6	214.6	214.3	245.4	244.7	258.8	257.8
EPCSRST_N_2	B34	234.7	234.4	167.9	167.3	196.3	195.5	217.3	216.6	249.4	248.4	263.5	262.0
EPCSRST_N_3	B35	234.1	233.8	166.3	165.8	194.0	193.1	214.4	213.7	245.4	244.2	258.7	257.1
EPCSRST_N_4	B36	235.2	235.0	168.1	167.7	196.5	196.0	217.5	217.4	249.8	249.5	263.8	263.1
EPCSRST_N_5	B37	235.1	234.0	168.5	166.3	197.4	194.1	218.9	214.9	251.6	245.3	266.1	258.4
MONITOR	K23	235.4	234.3	166.7	166.0	194.1	193.2	214.3	213.0	244.2	242.6	256.8	255.2
PLL_MON	L20	233.6	233.3	162.8	163.4	188.1	189.4	206.8	208.3	232.4	235.1	242.8	246.3
TOGGLE_MON	L22	235.0	234.3	165.5	164.7	192.1	191.1	211.8	210.6	240.2	238.2	252.2	249.9

Table. 18. LVCMOS 25 VOL – DUT 06828

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	238.1	237.4	170.0	169.2	198.7	197.6	222.4	221.2	254.4	252.2	268.1	265.9
EPCSRST_N_0	B31	240.8	236.7	177.4	169.8	210.1	198.6	237.9	222.5	277.9	254.8	295.9	268.9
EPCSRST_N_1	B32	236.0	235.7	167.6	167.4	195.6	195.2	216.2	216.0	247.2	246.8	260.6	259.9
EPCSRST_N_2	B34	238.1	237.9	170.4	169.8	199.1	198.2	220.3	219.6	252.9	251.5	267.1	265.4
EPCSRST_N_3	B35	237.5	237.2	168.9	168.5	197.0	196.3	217.5	217.1	248.5	247.8	261.9	260.7
EPCSRST_N_4	B36	237.6	237.5	170.0	169.8	198.7	198.5	219.9	220.0	252.2	252.0	266.2	265.8
EPCSRST_N_5	B37	238.8	237.2	171.4	168.4	200.8	196.3	222.6	217.0	256.4	247.6	271.0	260.6
MONITOR	K23	236.7	236.0	167.9	167.1	195.2	194.4	215.6	214.3	245.3	243.8	258.1	256.5
PLL_MON	L20	233.8	233.9	163.0	163.9	188.4	189.9	207.2	209.0	232.8	235.9	243.3	247.0
TOGGLE_MON	L22	235.3	234.6	165.9	165.2	192.7	191.7	212.6	211.4	241.3	239.4	253.4	251.1

Table. 19. LVCMOS 25 VOL – DUT 06829

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	237.4	237.3	169.3	169.1	197.8	197.4	221.0	220.6	252.2	251.5	265.8	264.9
EPCSRST_N_0	B31	242.1	236.4	180.6	169.4	214.7	198.2	244.1	221.9	287.5	253.8	307.2	268.1
EPCSRST_N_1	B32	235.2	235.2	167.2	167.1	194.9	194.6	215.2	215.3	245.8	245.6	258.9	258.7
EPCSRST_N_2	B34	237.6	238.0	169.4	169.2	197.7	197.4	218.7	218.8	250.6	250.1	264.5	263.6
EPCSRST_N_3	B35	237.1	237.0	168.1	167.8	196.0	195.5	216.5	216.3	247.0	246.2	260.1	259.1
EPCSRST_N_4	B36	238.3	238.4	169.9	169.9	198.6	198.5	219.7	220.2	251.9	252.0	265.9	265.8
EPCSRST_N_5	B37	238.9	237.4	171.6	168.3	201.2	196.2	223.1	217.3	257.3	247.7	272.1	260.7
MONITOR	K23	236.5	236.0	167.7	167.4	195.0	194.7	215.4	214.4	245.3	244.3	258.1	257.0
PLL_MON	L20	234.2	234.5	163.4	164.3	188.9	190.4	207.7	209.5	233.6	236.6	244.2	247.8
TOGGLE_MON	L22	235.1	234.8	165.9	165.4	192.6	191.9	212.5	211.6	241.1	239.6	253.2	251.4

Table. 20. LVCMOS 25 VOL – DUT 06877

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	239.7	238.8	170.1	169.6	198.4	197.9	221.4	221.2	252.3	252.0	265.5	265.4
EPCSRST_N_0	B31	242.4	237.8	178.1	170.2	210.6	199.0	238.3	222.8	277.7	254.8	295.3	268.7
EPCSRST_N_1	B32	237.8	236.9	168.6	167.8	196.5	195.4	216.8	216.1	247.7	246.3	260.9	259.4
EPCSRST_N_2	B34	239.5	238.8	170.7	169.8	199.2	197.9	220.3	219.1	252.2	250.5	266.1	263.9
EPCSRST_N_3	B35	239.1	238.2	169.6	168.6	197.5	196.4	217.9	216.9	248.5	246.9	261.6	259.6
EPCSRST_N_4	B36	239.6	238.9	171.3	170.6	200.2	199.3	221.4	220.8	254.0	252.8	267.8	266.6
EPCSRST_N_5	B37	241.0	238.8	172.9	169.0	202.5	197.0	224.7	218.0	258.7	248.7	273.5	261.7
MONITOR	K23	239.2	237.7	169.3	168.1	197.0	195.6	217.6	215.4	247.6	245.1	260.5	257.6
PLL_MON	L20	236.5	235.9	164.6	165.0	190.2	191.1	209.0	210.2	234.5	236.9	245.2	248.0
TOGGLE_MON	L22	237.3	236.1	167.3	166.0	194.2	192.7	214.4	212.4	243.0	240.4	255.3	252.0

Table. 21. LVCMOS 25 VOL – DUT 06917

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	238.1	237.9	169.5	169.2	197.8	197.5	221.1	220.7	252.2	251.6	265.7	265.2
EPCSRST_N_0	B31	240.7	237.0	177.3	169.8	209.7	198.6	237.4	222.3	277.0	254.3	294.7	268.5
EPCSRST_N_1	B32	235.7	235.7	167.4	167.2	195.0	194.9	215.4	215.5	246.2	246.1	259.4	259.1
EPCSRST_N_2	B34	237.3	237.5	169.5	169.2	198.0	197.6	218.9	218.8	250.8	250.0	264.6	263.7
EPCSRST_N_3	B35	237.1	237.0	168.3	167.9	196.1	195.7	216.5	216.3	247.1	246.5	260.4	259.3
EPCSRST_N_4	B36	238.4	238.6	170.3	170.2	198.7	198.6	219.8	220.0	252.1	252.0	265.9	265.6
EPCSRST_N_5	B37	238.4	237.2	170.8	168.4	199.9	196.1	221.5	217.0	254.8	247.5	269.3	260.5
MONITOR	K23	236.9	236.5	167.8	167.4	195.2	194.8	215.6	214.7	245.4	244.2	258.0	256.9
PLL_MON	L20	234.8	235.1	163.5	164.5	188.9	190.5	207.7	209.7	233.4	236.5	244.0	247.6
TOGGLE_MON	L22	235.8	235.5	166.3	165.7	193.0	192.2	212.9	211.8	241.3	239.6	253.3	251.3

Table. 22. LVTTL VOH – DUT 06787

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.918	2.918	2.909	2.909	2.890	2.891	2.870	2.872	2.852	2.855
EPCSRST_N_0	B31	2.916	2.919	2.902	2.909	2.875	2.889	2.848	2.870	2.822	2.851
EPCSRST_N_1	B32	2.921	2.921	2.912	2.912	2.894	2.894	2.876	2.877	2.859	2.860
EPCSRST_N_2	B34	2.919	2.919	2.909	2.910	2.890	2.891	2.872	2.872	2.853	2.854
EPCSRST_N_3	B35	2.920	2.920	2.911	2.911	2.893	2.894	2.875	2.876	2.858	2.860
EPCSRST_N_4	B36	2.920	2.919	2.910	2.909	2.890	2.890	2.871	2.871	2.852	2.852
EPCSRST_N_5	B37	2.919	2.920	2.909	2.911	2.889	2.893	2.869	2.875	2.849	2.858
MONITOR	K23	2.921	2.921	2.912	2.912	2.896	2.895	2.879	2.878	2.862	2.862
PLL_MON	L20	2.923	2.922	2.917	2.915	2.904	2.901	2.891	2.887	2.879	2.874
TOGGLE_MON	L22	2.921	2.921	2.914	2.913	2.898	2.899	2.883	2.884	2.868	2.869

Table. 23. LVTTL VOH – DUT 06816

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.920	2.921	2.910	2.911	2.891	2.892	2.871	2.873	2.853	2.855
EPCSRST_N_0	B31	2.917	2.921	2.903	2.911	2.875	2.891	2.847	2.870	2.820	2.852
EPCSRST_N_1	B32	2.922	2.922	2.913	2.913	2.895	2.895	2.877	2.877	2.859	2.860
EPCSRST_N_2	B34	2.922	2.922	2.912	2.912	2.892	2.893	2.872	2.874	2.853	2.855
EPCSRST_N_3	B35	2.923	2.923	2.913	2.914	2.896	2.897	2.878	2.879	2.860	2.862
EPCSRST_N_4	B36	2.922	2.922	2.912	2.912	2.892	2.892	2.873	2.873	2.854	2.854
EPCSRST_N_5	B37	2.922	2.923	2.911	2.913	2.891	2.895	2.871	2.877	2.851	2.860
MONITOR	K23	2.922	2.922	2.913	2.913	2.897	2.896	2.879	2.879	2.862	2.863
PLL_MON	L20	2.924	2.922	2.917	2.915	2.904	2.901	2.891	2.887	2.879	2.874
TOGGLE_MON	L22	2.921	2.921	2.914	2.914	2.899	2.899	2.883	2.884	2.868	2.870

Table. 24. LVTTL VOH – DUT 06828

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.919	2.919	2.909	2.909	2.889	2.890	2.869	2.871	2.851	2.853
EPCSRST_N_0	B31	2.916	2.919	2.902	2.909	2.875	2.889	2.847	2.869	2.821	2.850
EPCSRST_N_1	B32	2.920	2.921	2.911	2.911	2.893	2.893	2.875	2.875	2.857	2.858
EPCSRST_N_2	B34	2.919	2.919	2.909	2.909	2.889	2.890	2.869	2.871	2.850	2.852
EPCSRST_N_3	B35	2.920	2.920	2.911	2.911	2.892	2.893	2.874	2.875	2.857	2.858
EPCSRST_N_4	B36	2.920	2.920	2.909	2.909	2.890	2.890	2.870	2.871	2.852	2.852
EPCSRST_N_5	B37	2.919	2.920	2.908	2.911	2.887	2.893	2.866	2.875	2.846	2.858
MONITOR	K23	2.921	2.920	2.912	2.911	2.895	2.895	2.878	2.878	2.861	2.862
PLL_MON	L20	2.923	2.922	2.917	2.915	2.904	2.901	2.891	2.887	2.879	2.873
TOGGLE_MON	L22	2.921	2.921	2.913	2.913	2.898	2.899	2.882	2.884	2.867	2.868

Table. 25. LVTTL VOH – DUT 06829

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.919	2.918	2.909	2.909	2.890	2.890	2.871	2.872	2.853	2.854
EPCSRST_N_0	B31	2.913	2.918	2.898	2.908	2.868	2.889	2.837	2.869	2.807	2.850
EPCSRST_N_1	B32	2.920	2.920	2.911	2.911	2.893	2.893	2.876	2.876	2.858	2.859
EPCSRST_N_2	B34	2.918	2.918	2.909	2.909	2.890	2.890	2.871	2.872	2.852	2.853
EPCSRST_N_3	B35	2.920	2.920	2.910	2.911	2.893	2.893	2.875	2.876	2.858	2.859
EPCSRST_N_4	B36	2.918	2.918	2.909	2.909	2.889	2.889	2.870	2.870	2.851	2.851
EPCSRST_N_5	B37	2.918	2.919	2.907	2.910	2.886	2.892	2.865	2.874	2.845	2.857
MONITOR	K23	2.921	2.920	2.912	2.911	2.895	2.894	2.877	2.877	2.861	2.861
PLL_MON	L20	2.923	2.921	2.916	2.914	2.903	2.900	2.890	2.886	2.877	2.872
TOGGLE_MON	L22	2.921	2.920	2.913	2.913	2.897	2.898	2.882	2.883	2.866	2.868

Table. 26. LVTTL VOH – DUT 06877

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.917	2.917	2.908	2.908	2.890	2.890	2.872	2.871	2.854	2.854
EPCSRST_N_0	B31	2.914	2.918	2.900	2.907	2.873	2.888	2.846	2.868	2.821	2.850
EPCSRST_N_1	B32	2.918	2.919	2.909	2.910	2.892	2.893	2.874	2.875	2.857	2.858
EPCSRST_N_2	B34	2.917	2.918	2.908	2.909	2.889	2.890	2.870	2.871	2.851	2.853
EPCSRST_N_3	B35	2.918	2.919	2.909	2.910	2.892	2.893	2.874	2.875	2.857	2.859
EPCSRST_N_4	B36	2.917	2.918	2.907	2.908	2.888	2.889	2.868	2.869	2.849	2.851
EPCSRST_N_5	B37	2.916	2.918	2.906	2.909	2.885	2.892	2.864	2.874	2.843	2.856
MONITOR	K23	2.918	2.918	2.909	2.910	2.892	2.893	2.875	2.877	2.859	2.860
PLL_MON	L20	2.920	2.920	2.914	2.913	2.901	2.899	2.889	2.885	2.877	2.872
TOGGLE_MON	L22	2.919	2.920	2.911	2.912	2.895	2.897	2.880	2.882	2.864	2.867

Table. 27. LVTTL VOH – DUT 06917

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.918	2.918	2.909	2.909	2.890	2.890	2.872	2.871	2.854	2.854
EPCSRST_N_0	B31	2.915	2.918	2.901	2.908	2.874	2.888	2.847	2.869	2.821	2.850
EPCSRST_N_1	B32	2.920	2.920	2.911	2.911	2.893	2.893	2.875	2.875	2.858	2.858
EPCSRST_N_2	B34	2.919	2.919	2.909	2.909	2.890	2.890	2.871	2.872	2.852	2.853
EPCSRST_N_3	B35	2.920	2.920	2.911	2.911	2.893	2.893	2.875	2.876	2.858	2.859
EPCSRST_N_4	B36	2.918	2.918	2.909	2.909	2.889	2.889	2.870	2.870	2.851	2.851
EPCSRST_N_5	B37	2.918	2.919	2.908	2.911	2.888	2.893	2.867	2.874	2.848	2.857
MONITOR	K23	2.920	2.920	2.912	2.911	2.895	2.894	2.877	2.877	2.861	2.861
PLL_MON	L20	2.922	2.921	2.916	2.914	2.903	2.900	2.890	2.886	2.878	2.872
TOGGLE_MON	L22	2.920	2.920	2.913	2.913	2.897	2.898	2.882	2.883	2.866	2.868

Table. 28. LVTTL VOL – DUT 06787

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	217.9	217.3	232.0	230.6	245.7	243.9	265.0	262.4	286.1	282.8
EPCSRST_N_0	B31	220.0	216.2	238.9	230.8	260.0	245.0	287.5	264.6	316.7	286.5
EPCSRST_N_1	B32	215.1	215.2	224.4	224.8	240.7	240.5	258.4	257.9	276.5	275.9
EPCSRST_N_2	B34	217.3	217.5	226.9	227.1	244.7	244.0	263.3	262.3	282.5	281.5
EPCSRST_N_3	B35	216.3	216.2	225.6	225.9	242.4	241.6	260.0	258.7	278.2	276.7
EPCSRST_N_4	B36	217.3	217.3	227.4	227.6	245.5	245.1	264.7	264.4	284.3	284.0
EPCSRST_N_5	B37	217.5	216.6	228.0	226.4	246.9	242.4	266.9	260.2	286.8	278.5
MONITOR	K23	215.4	215.4	224.7	223.9	240.1	239.7	256.6	256.5	274.3	273.4
PLL_MON	L20	213.5	213.5	221.9	221.7	231.9	234.1	244.6	248.1	258.5	262.5
TOGGLE_MON	L22	214.9	214.7	224.0	223.1	237.0	236.1	252.8	250.9	269.1	266.9

Table. 29. LVTTL VOL – DUT 06816

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	215.3	214.5	230.0	228.6	243.9	241.9	263.4	260.6	284.9	281.4
EPCSRST_N_0	B31	218.8	214.2	237.7	228.5	260.0	243.6	288.1	263.5	318.2	285.3
EPCSRST_N_1	B32	213.6	213.1	222.8	222.7	239.8	238.8	257.5	256.7	276.2	275.2
EPCSRST_N_2	B34	214.1	214.0	224.2	224.3	242.4	241.5	261.9	260.3	281.5	279.9
EPCSRST_N_3	B35	213.4	212.9	222.7	222.4	239.6	238.4	257.4	256.1	275.8	274.2
EPCSRST_N_4	B36	214.5	214.2	224.5	224.8	242.7	242.1	262.1	261.2	281.9	281.2
EPCSRST_N_5	B37	214.6	213.4	225.0	223.3	244.1	239.5	264.1	257.2	284.4	275.7
MONITOR	K23	214.2	213.8	223.8	221.9	239.1	238.3	255.8	254.9	273.8	272.1
PLL_MON	L20	212.7	212.7	221.4	220.8	231.4	233.3	244.1	247.2	257.8	261.7
TOGGLE_MON	L22	214.0	213.5	223.2	222.1	236.7	235.2	252.1	250.0	268.5	266.0

Table. 30. LVTTL VOL – DUT 06828

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	217.8	217.3	232.7	231.1	246.6	244.6	266.0	263.4	287.4	284.2
EPCSRST_N_0	B31	220.8	216.6	240.0	231.5	261.5	246.2	288.9	266.0	318.6	288.1
EPCSRST_N_1	B32	215.9	215.7	225.1	225.4	242.2	241.5	259.9	259.4	278.6	277.9
EPCSRST_N_2	B34	217.8	217.5	227.9	228.0	246.5	245.2	266.0	264.4	286.0	284.0
EPCSRST_N_3	B35	216.9	216.9	226.5	226.5	243.6	242.8	261.5	260.5	279.9	278.6
EPCSRST_N_4	B36	217.4	217.3	227.6	227.9	245.9	245.4	265.3	264.9	284.8	284.6
EPCSRST_N_5	B37	218.4	216.7	228.9	226.4	248.8	242.8	269.5	260.4	290.5	278.8
MONITOR	K23	215.9	215.8	225.7	224.4	241.0	240.3	257.6	256.8	275.6	273.9
PLL_MON	L20	213.8	213.9	222.3	222.3	232.3	234.4	244.9	248.4	258.5	262.9
TOGGLE_MON	L22	214.9	214.4	224.4	223.0	238.0	236.6	253.5	251.8	270.1	267.6

Table. 31. LVTTL VOL – DUT 06829

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	217.4	217.3	232.1	231.4	245.0	244.4	263.8	262.9	284.4	283.5
EPCSRST_N_0	B31	222.4	216.7	242.8	231.4	267.9	245.7	298.5	265.2	331.6	287.1
EPCSRST_N_1	B32	215.5	215.3	224.7	225.2	241.4	240.9	258.9	258.3	277.0	276.8
EPCSRST_N_2	B34	217.6	217.7	227.6	228.1	245.1	244.7	264.0	262.7	283.3	282.3
EPCSRST_N_3	B35	217.0	217.0	226.0	226.4	242.7	241.9	260.4	259.3	278.1	277.1
EPCSRST_N_4	B36	218.2	218.3	228.1	228.7	246.2	245.9	265.1	264.9	284.8	284.7
EPCSRST_N_5	B37	218.7	217.1	229.4	227.0	249.2	243.0	270.0	260.5	291.1	278.9
MONITOR	K23	216.1	216.2	225.6	224.5	241.0	240.7	258.0	257.5	275.8	274.6
PLL_MON	L20	214.5	214.5	222.7	222.9	233.3	235.4	245.9	249.2	260.0	264.0
TOGGLE_MON	L22	215.3	214.6	224.6	223.5	238.1	237.3	253.7	252.3	270.2	268.1

Table. 32. LVTTL VOL – DUT 06877

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	219.4	218.3	233.0	232.1	245.4	245.0	263.4	263.4	283.7	283.8
EPCSRST_N_0	B31	222.2	217.7	240.8	232.3	262.0	246.7	289.0	266.1	317.9	287.6
EPCSRST_N_1	B32	217.7	216.8	226.7	226.4	243.1	241.9	260.5	259.1	278.8	277.3
EPCSRST_N_2	B34	219.0	218.2	228.9	228.6	246.5	245.0	265.4	263.3	284.6	282.4
EPCSRST_N_3	B35	218.8	217.7	227.7	227.4	244.3	242.8	261.5	259.7	279.4	277.5
EPCSRST_N_4	B36	219.0	218.7	229.7	229.3	247.6	246.7	266.8	265.6	286.6	285.5
EPCSRST_N_5	B37	220.5	218.4	231.0	227.8	250.9	243.6	271.8	261.7	293.0	279.9
MONITOR	K23	218.4	217.3	227.8	225.6	243.1	241.7	260.1	258.3	278.0	275.3
PLL_MON	L20	216.0	215.6	224.7	223.9	234.3	236.1	247.1	249.7	260.6	264.2
TOGGLE_MON	L22	216.8	215.7	226.2	224.4	239.7	237.8	255.3	252.7	272.0	268.8

Table. 33. LVTTL VOL – DUT 06917

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	217.7	217.6	232.0	231.2	244.9	244.2	263.3	262.9	283.8	283.4
EPCSRST_N_0	B31	220.8	216.9	240.0	231.8	260.8	246.0	288.2	265.5	317.4	287.3
EPCSRST_N_1	B32	215.6	215.5	224.9	225.3	241.4	241.1	259.1	258.7	277.2	276.9
EPCSRST_N_2	B34	217.0	217.2	227.2	227.2	245.0	244.6	263.8	262.9	283.0	282.1
EPCSRST_N_3	B35	216.8	216.6	225.6	226.2	242.6	241.8	260.1	259.1	277.9	276.9
EPCSRST_N_4	B36	218.1	218.0	228.0	228.4	245.9	245.7	265.2	264.8	284.5	284.3
EPCSRST_N_5	B37	218.0	216.9	228.6	226.7	247.4	242.6	267.6	260.3	288.3	278.4
MONITOR	K23	216.3	216.0	225.5	224.5	240.9	240.7	257.6	257.3	275.5	274.4
PLL_MON	L20	214.8	214.7	223.1	223.2	233.0	235.2	245.6	249.1	259.3	263.6
TOGGLE_MON	L22	215.4	215.0	224.7	223.8	238.4	237.2	253.7	252.3	270.1	267.8

E. Propagation Delay

Table 34 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 34. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
06787	125 krad	0.48	0.483	0.63
06816	125 krad	0.481	0.483	0.42
06828	125 krad	0.471	0.473	0.42
06829	125 krad	0.471	0.477	1.27
06877	125 krad	0.475	0.479	0.84
06917	125 krad	0.484	0.486	0.41

F. Transition Time

The figures below show the pre-irradiation and post-irradiation transitions edges. In each case the radiation induced transition degradation is not observable.

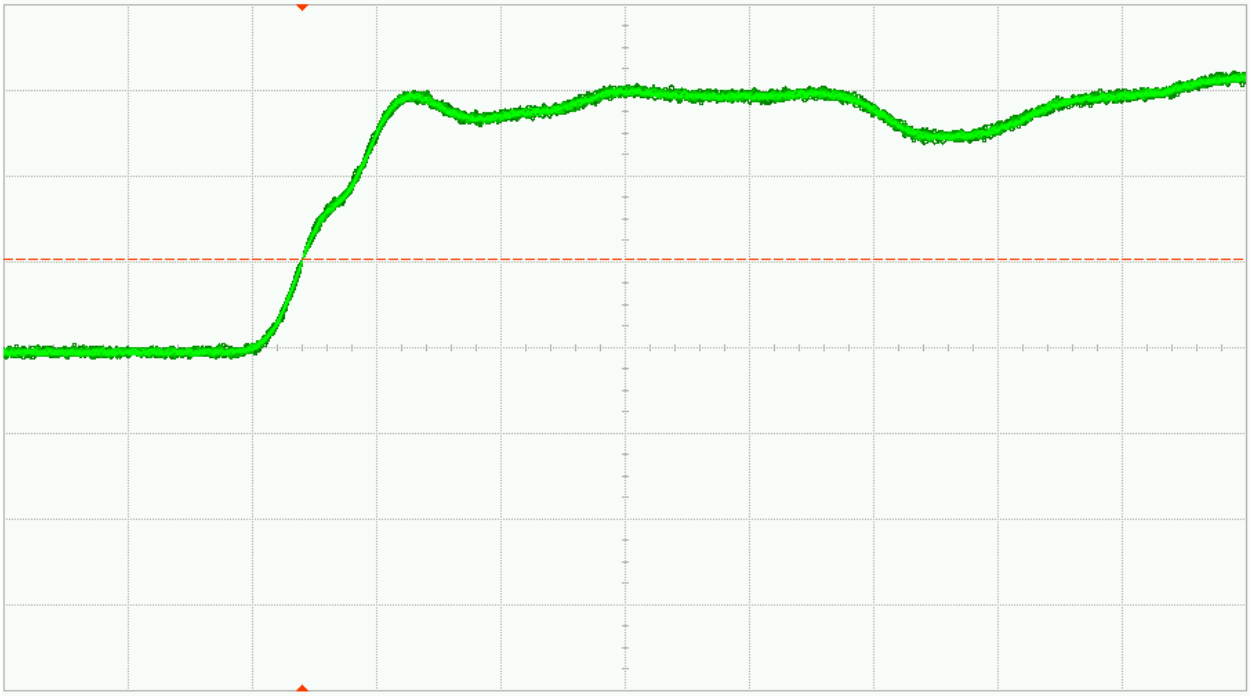

Fig. 26 (a). DUT 06787 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

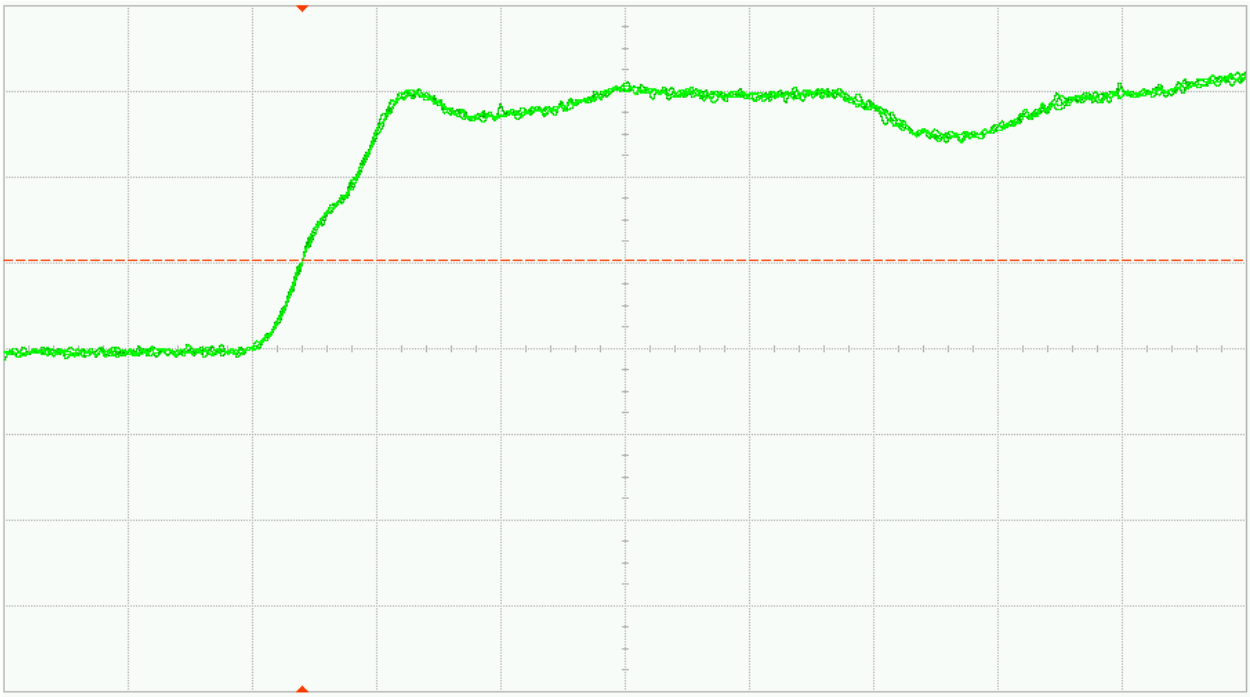

Fig. 26 (b). DUT 06787 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

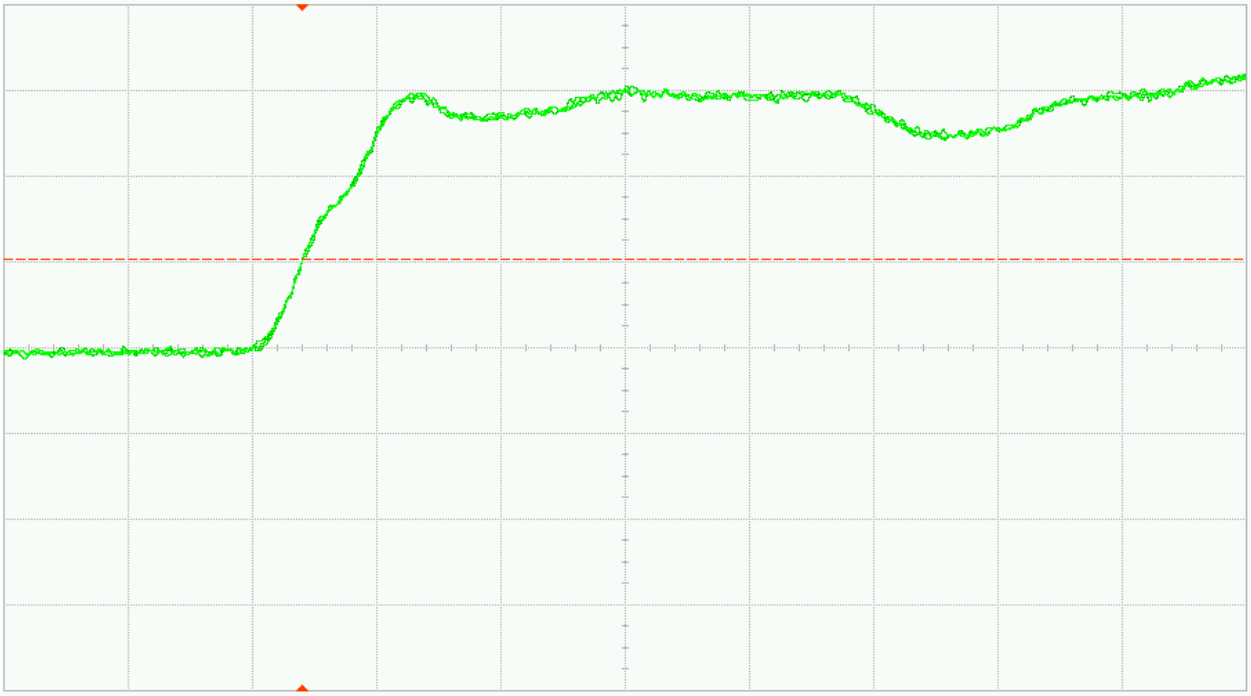

Fig. 27 (a). DUT 06816 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

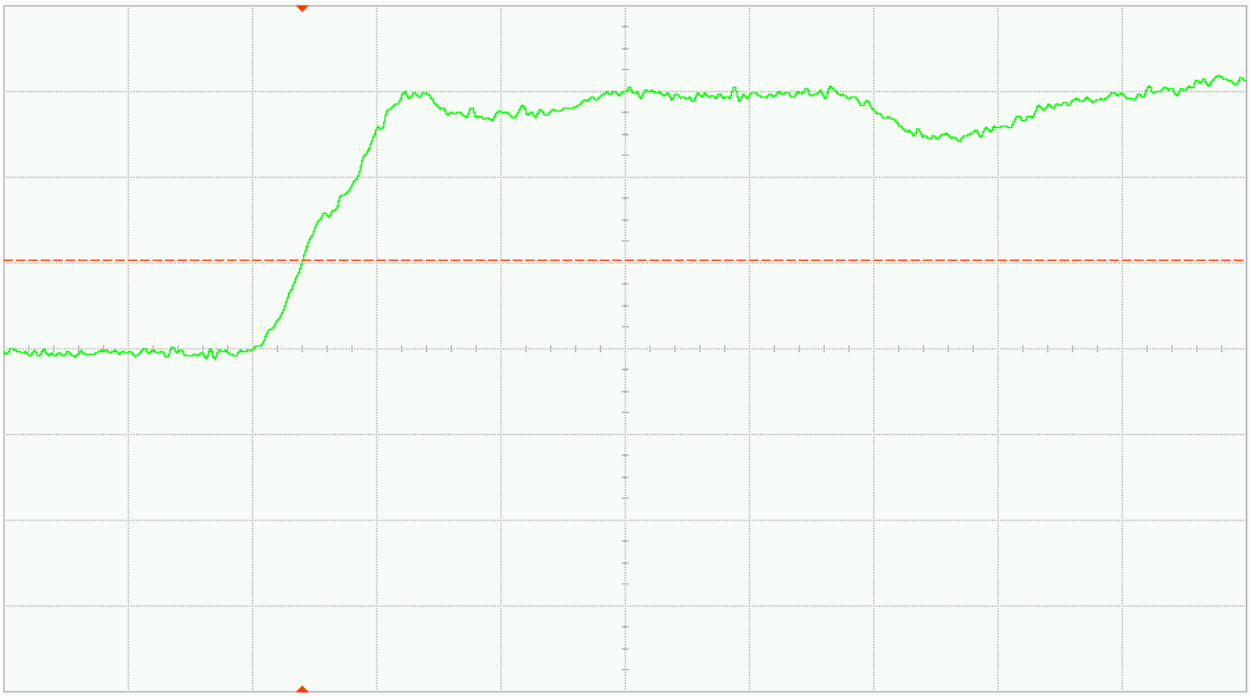

Fig. 27 (b). DUT 06816 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

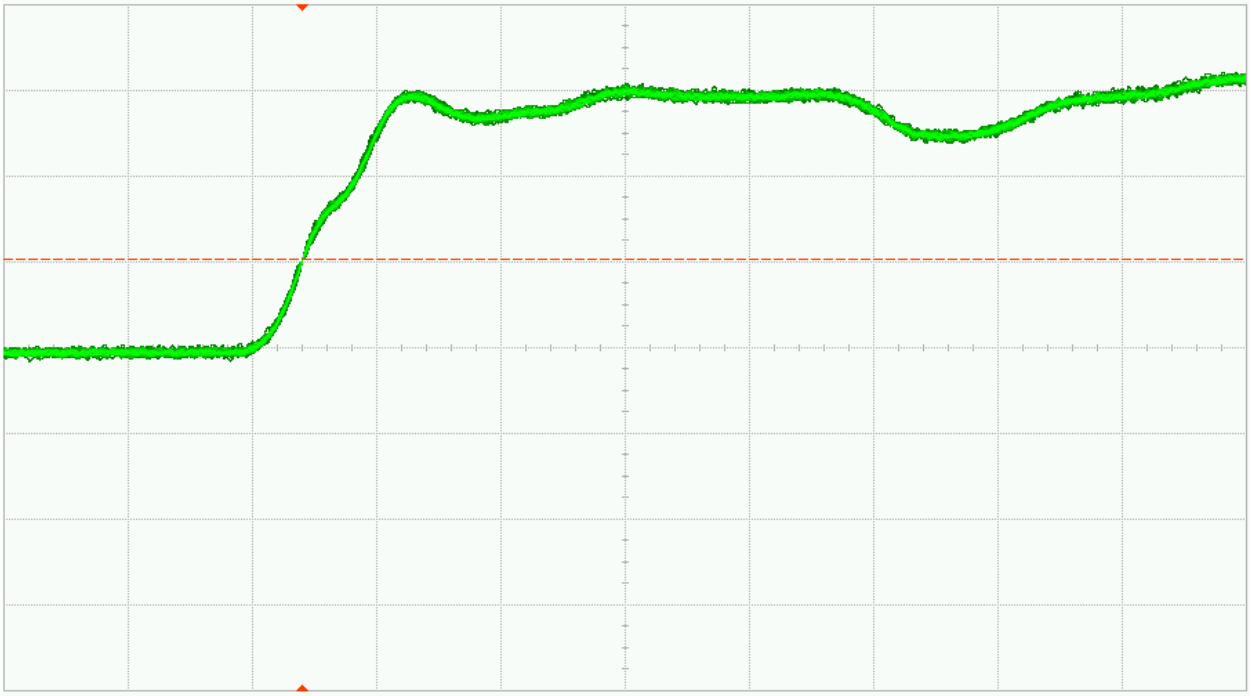

Fig. 28 (a). DUT 06828 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

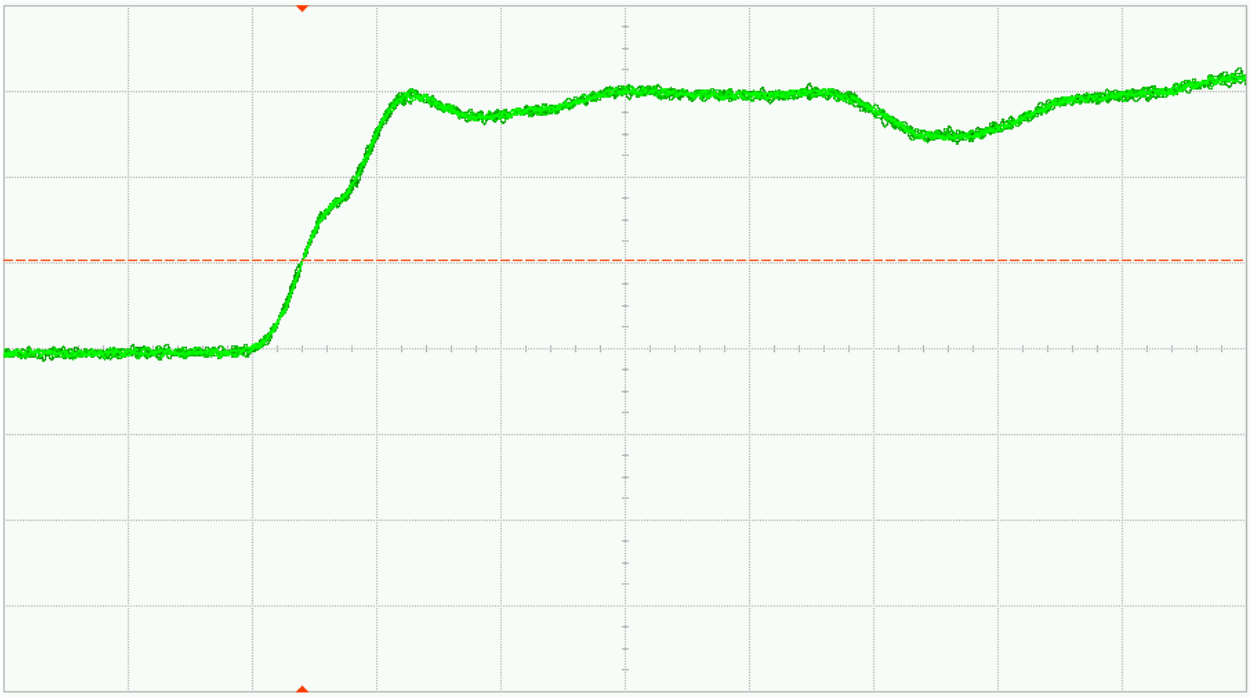

Fig. 28 (b). DUT 06828 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

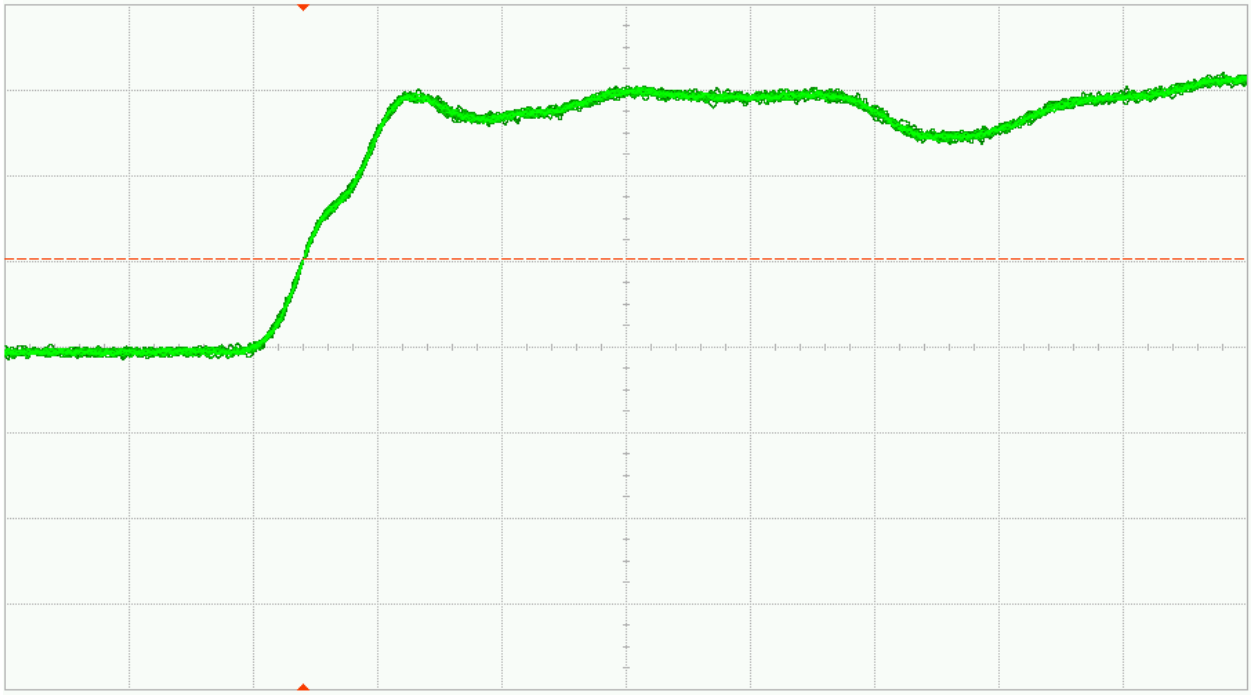

Fig. 29 (a). DUT 06829 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

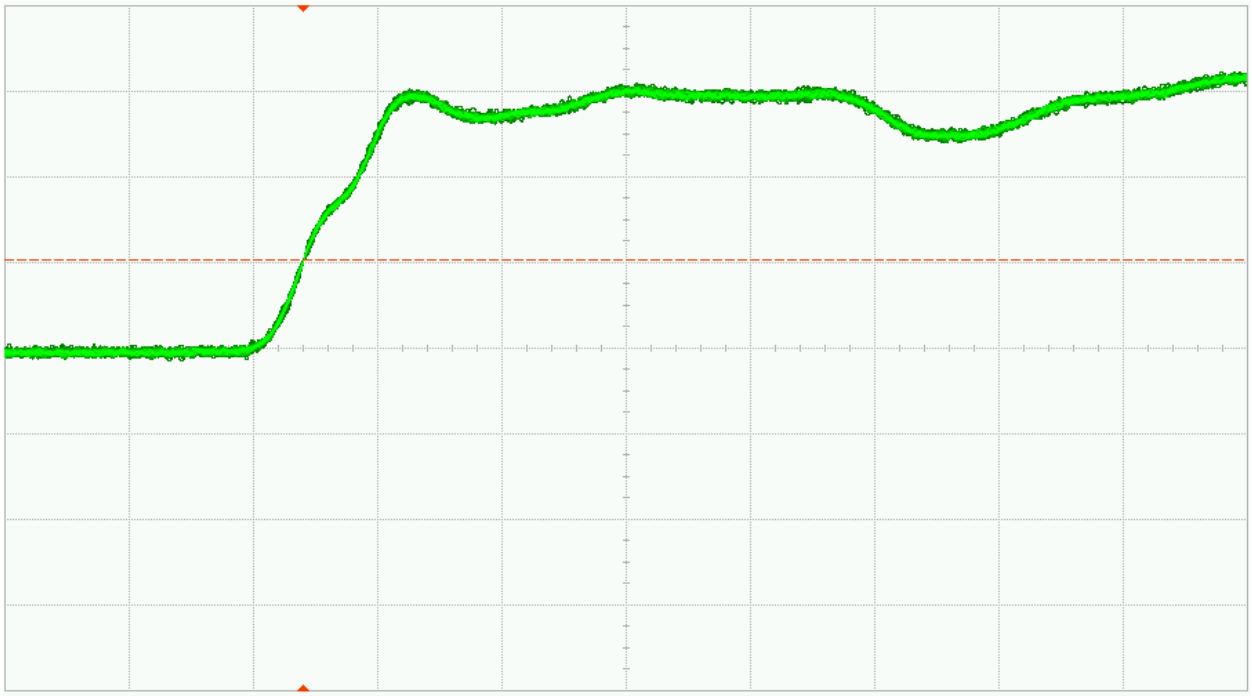

Fig. 29 (b). DUT 06829 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

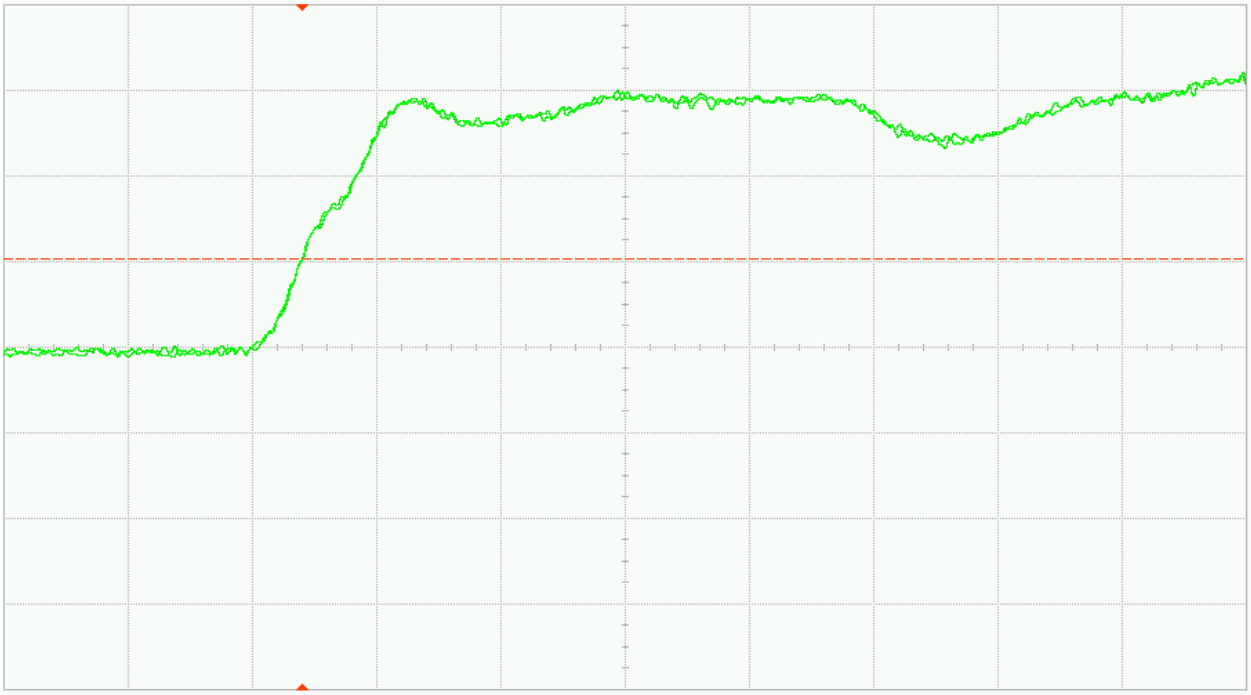

Fig. 30 (a). DUT 06877 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

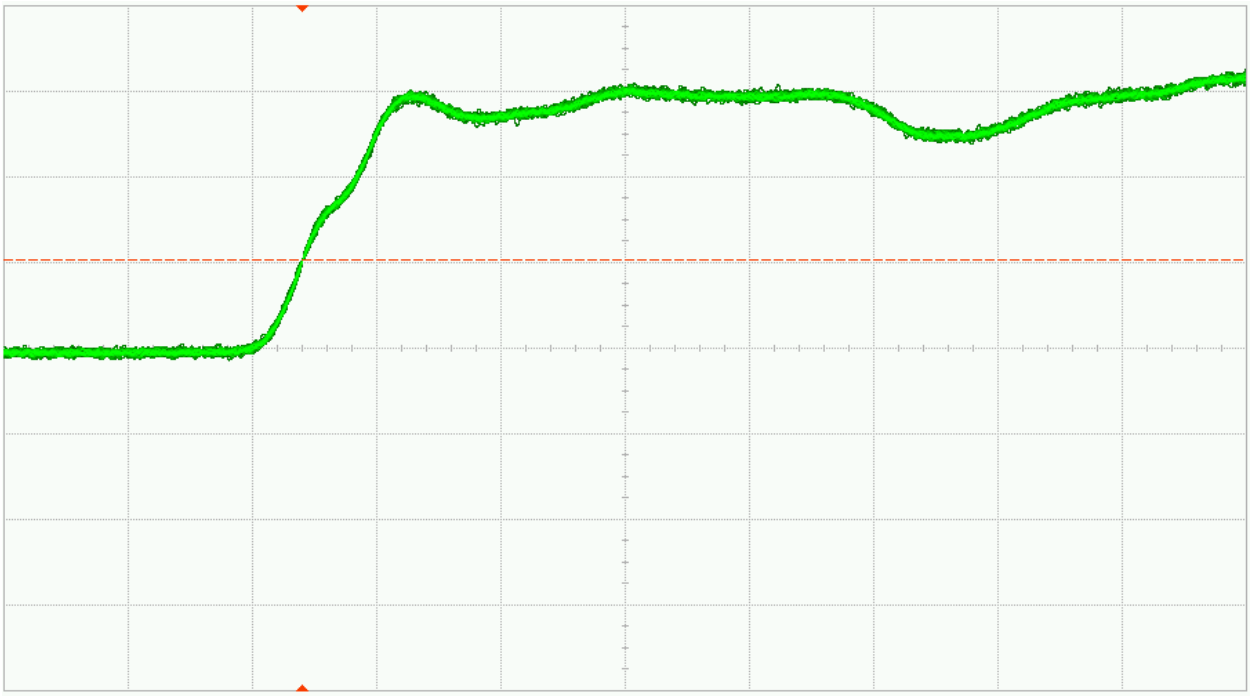

Fig. 30 (b). DUT 06877 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

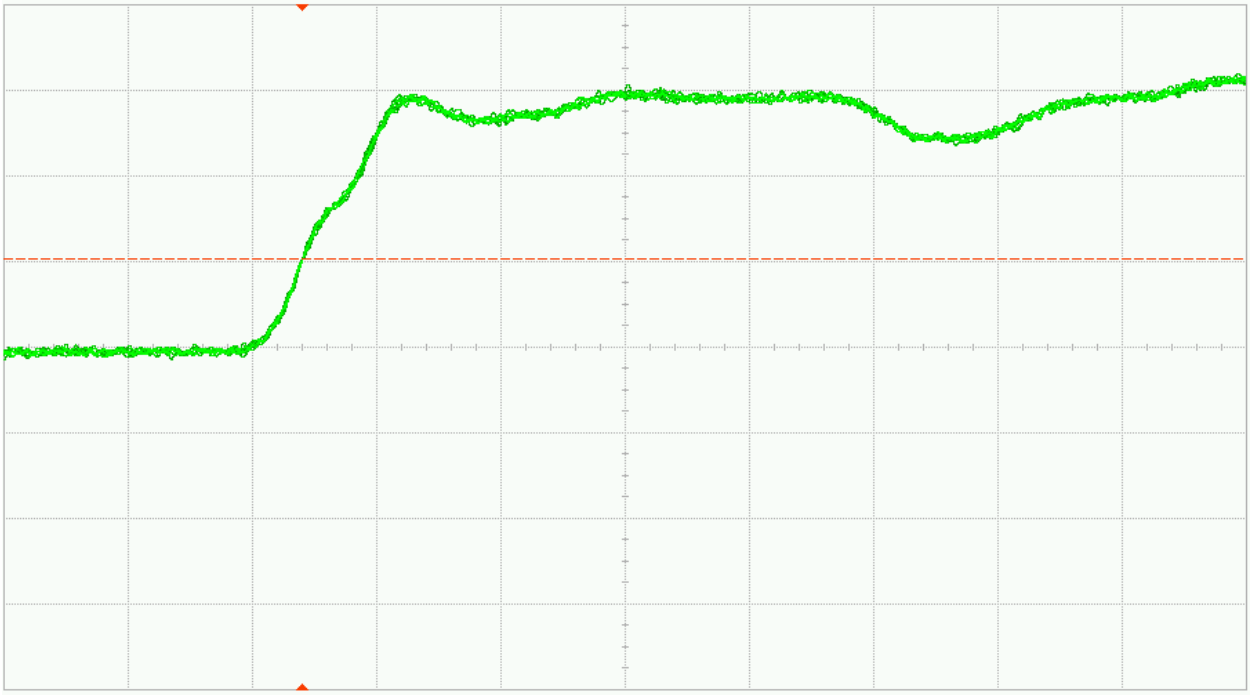

Fig. 31 (a). DUT 06917 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

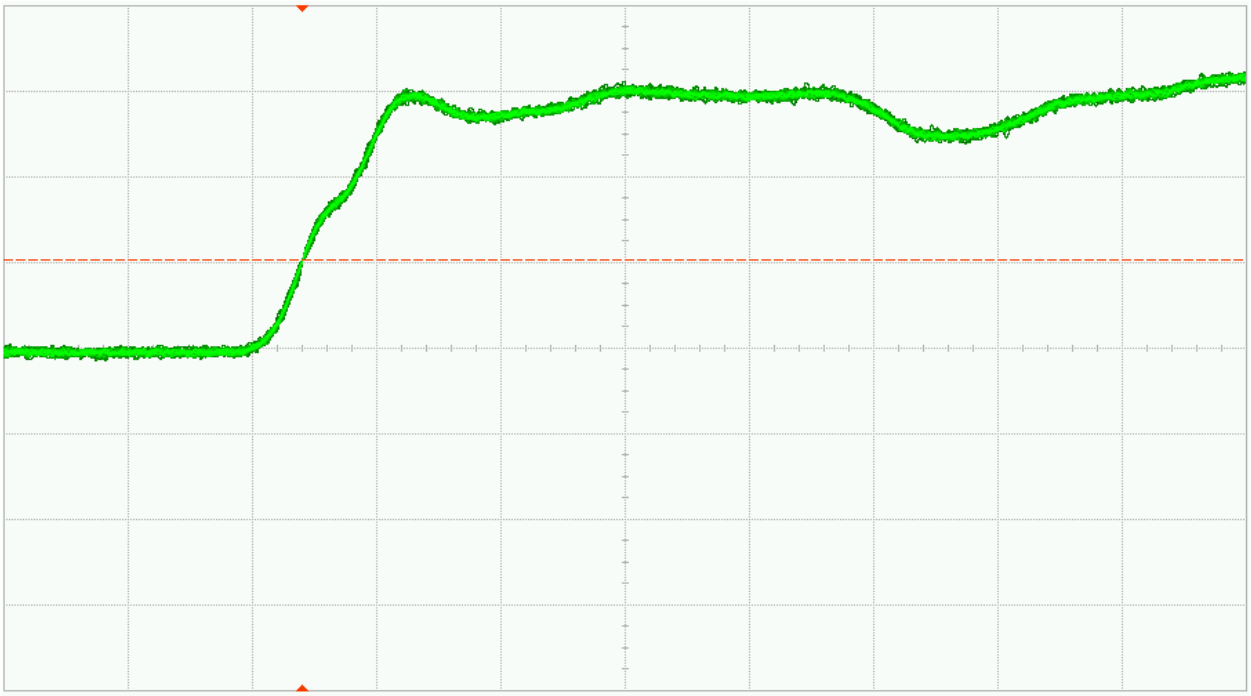

Fig. 31 (b). DUT 06917 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

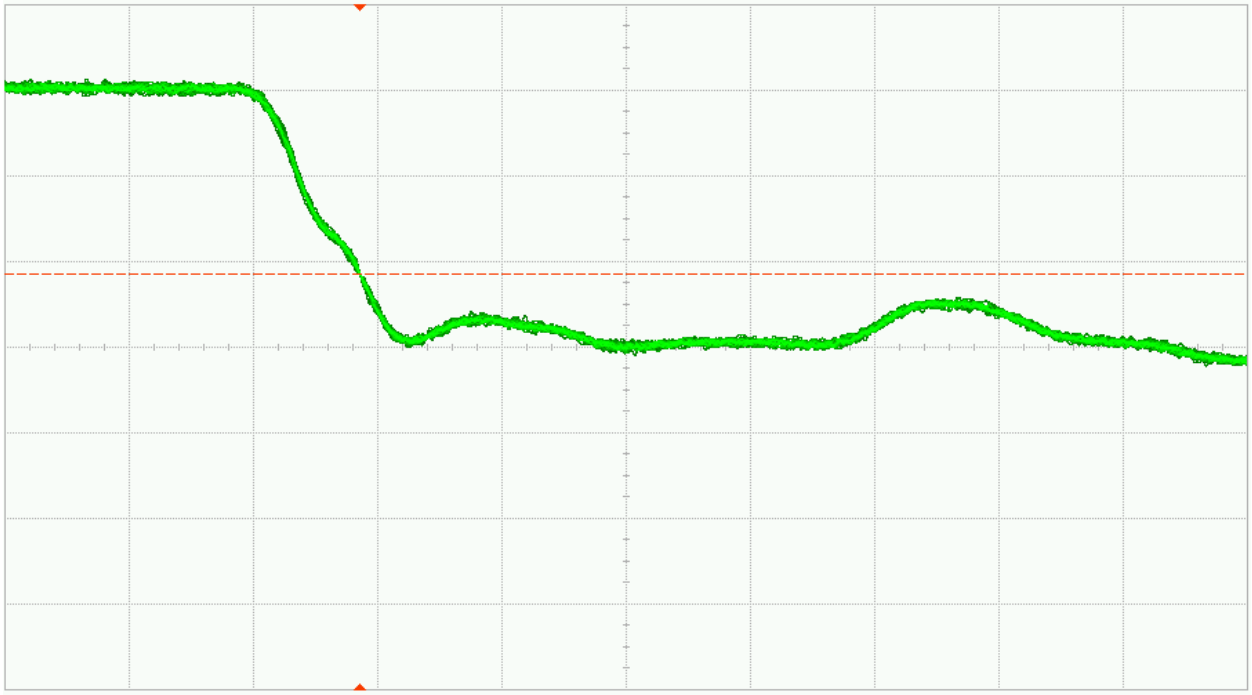

Fig. 32 (a). DUT 06787 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

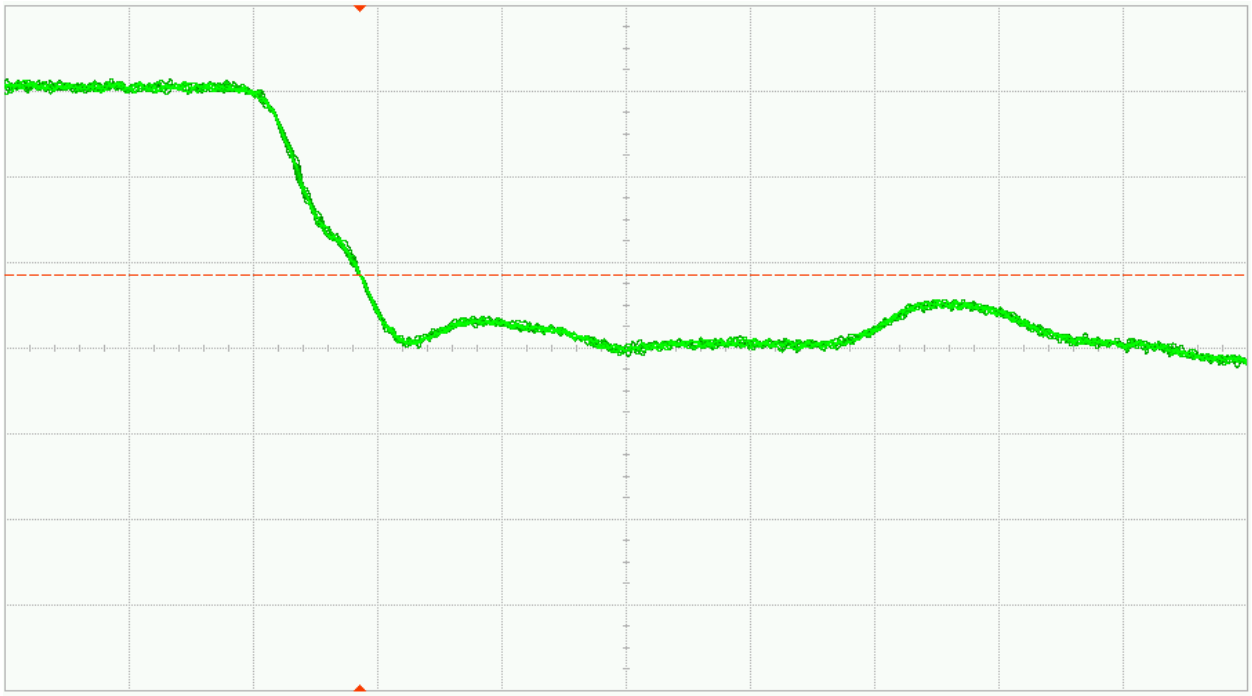

Fig. 32 (b). DUT 06787 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

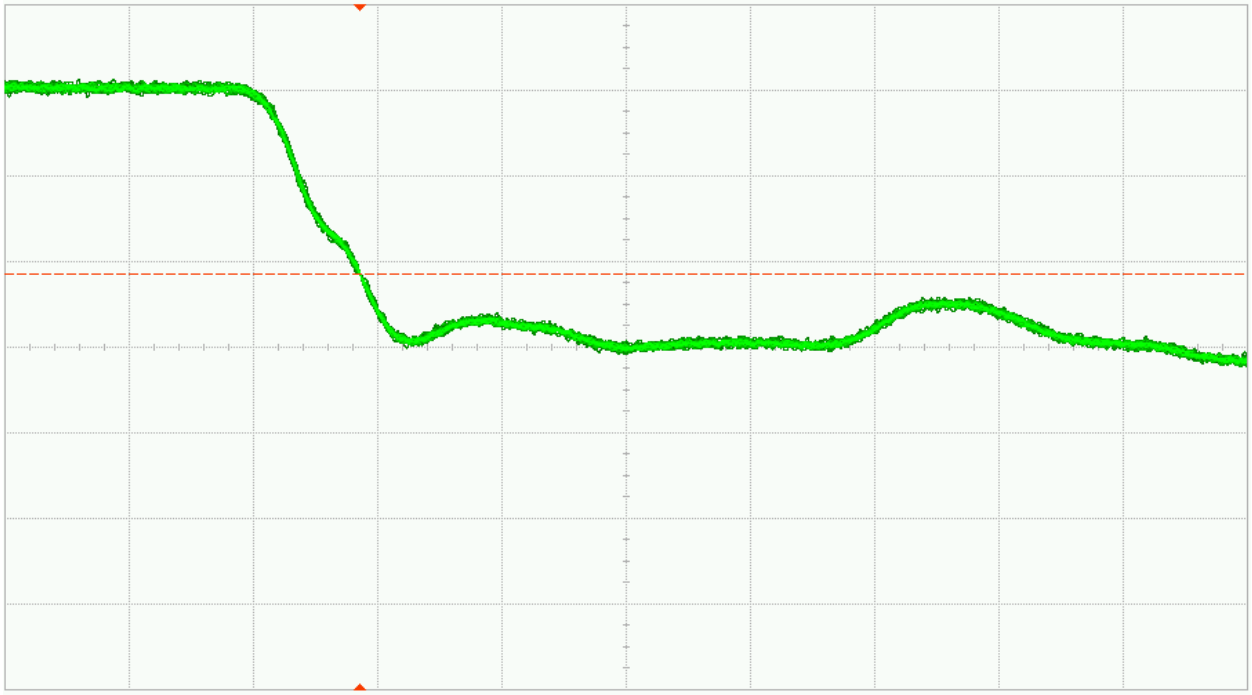

Fig. 33 (a). DUT 06816 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

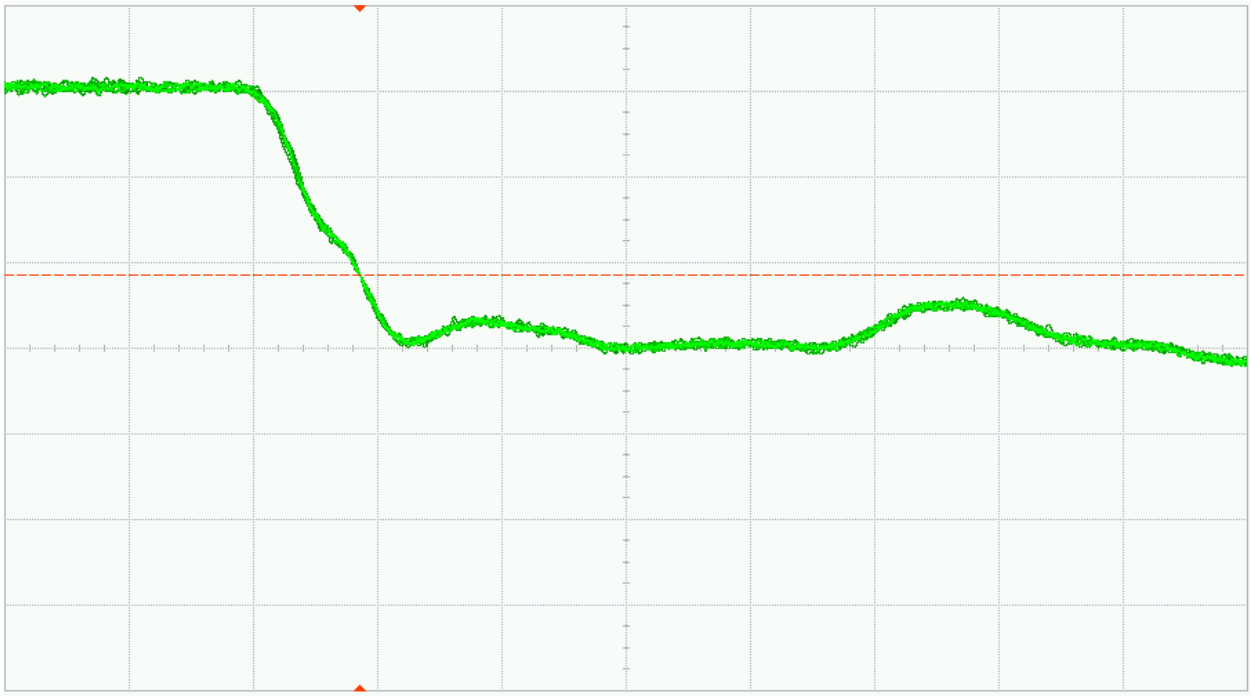

Fig. 33 (b). DUT 06816 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

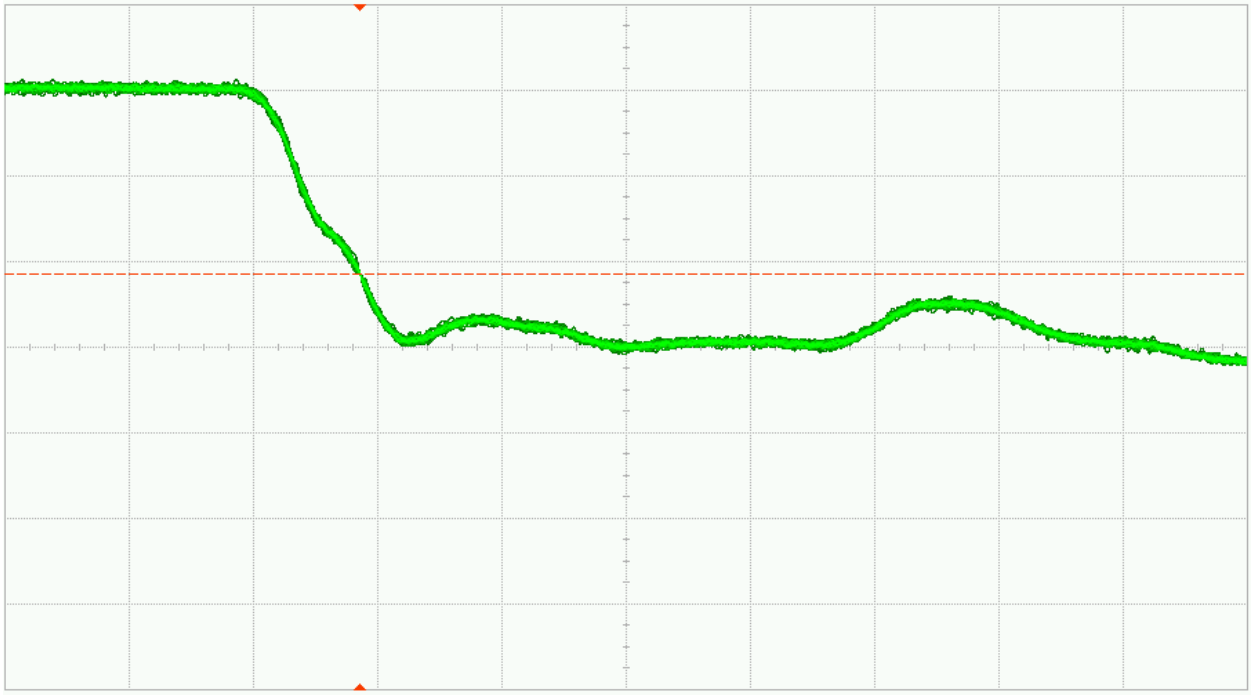

Fig. 34 (a). DUT 06828 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

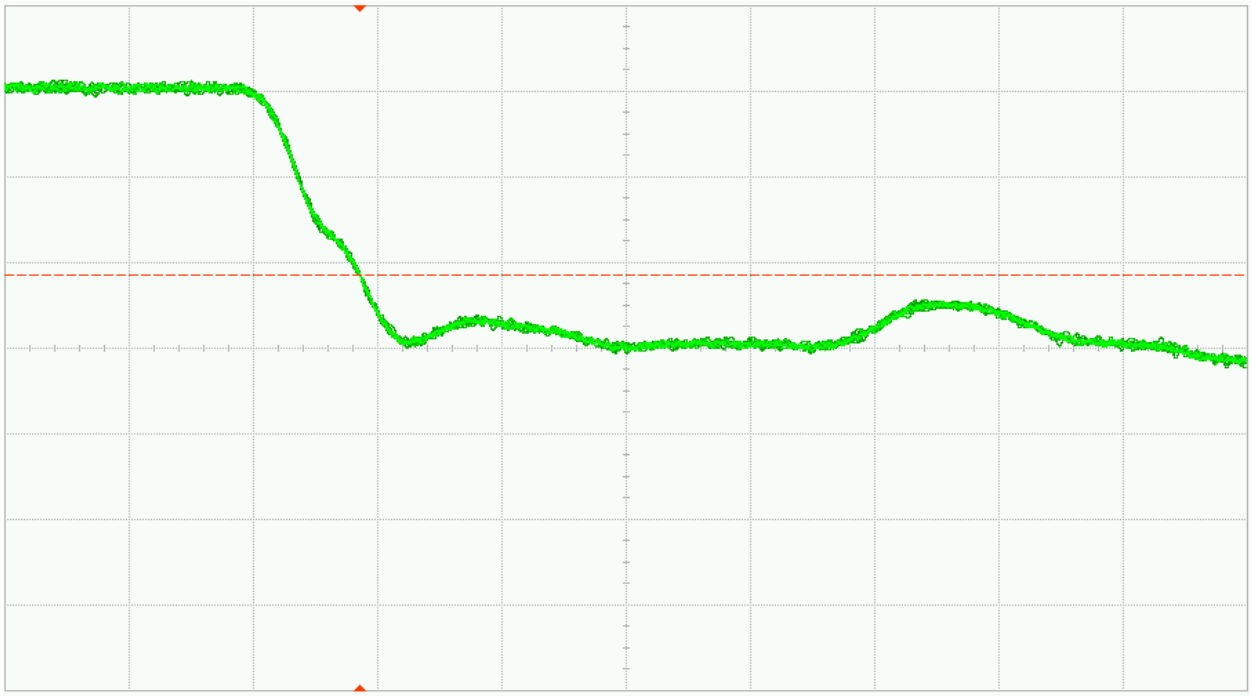

Fig. 34 (b). DUT 06828 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

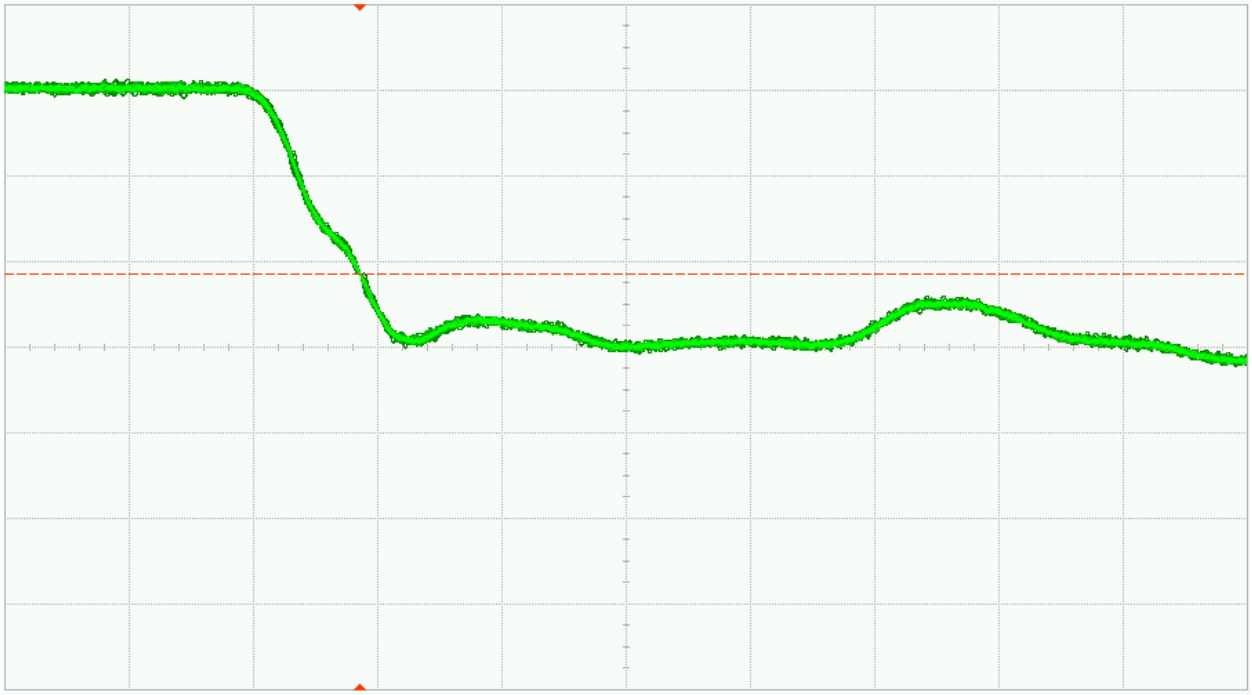

Fig. 35 (a). DUT 06829 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

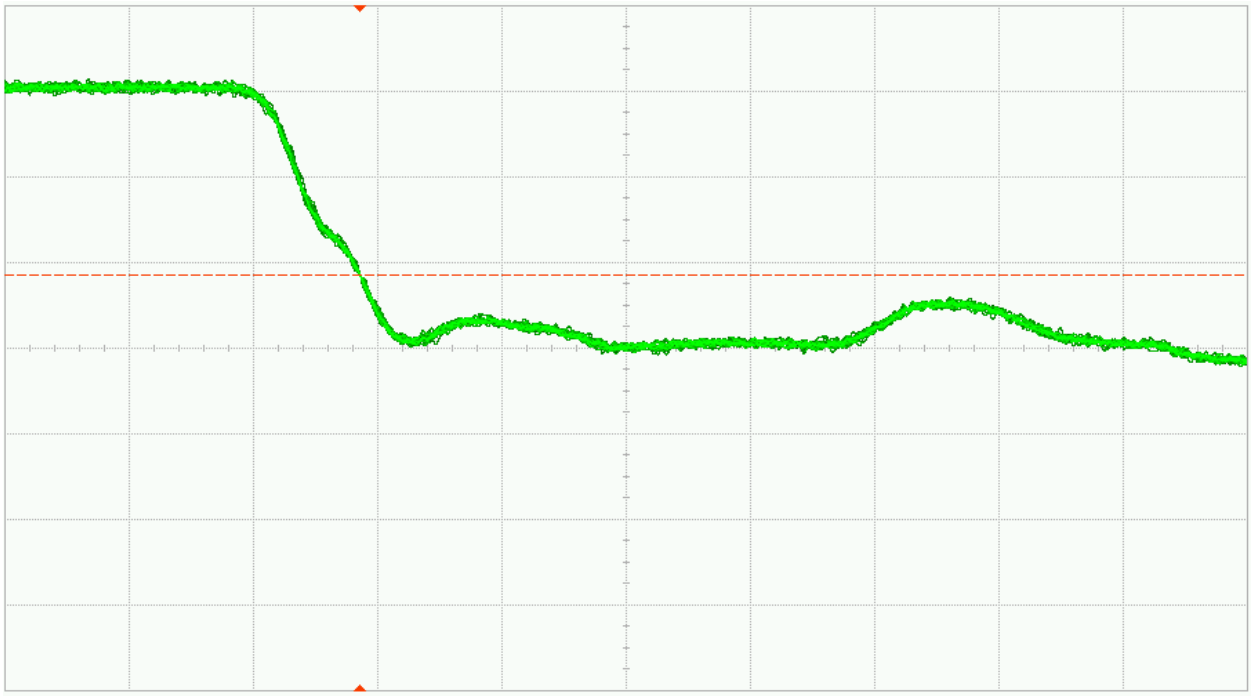

Fig. 35 (b). DUT 06829 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

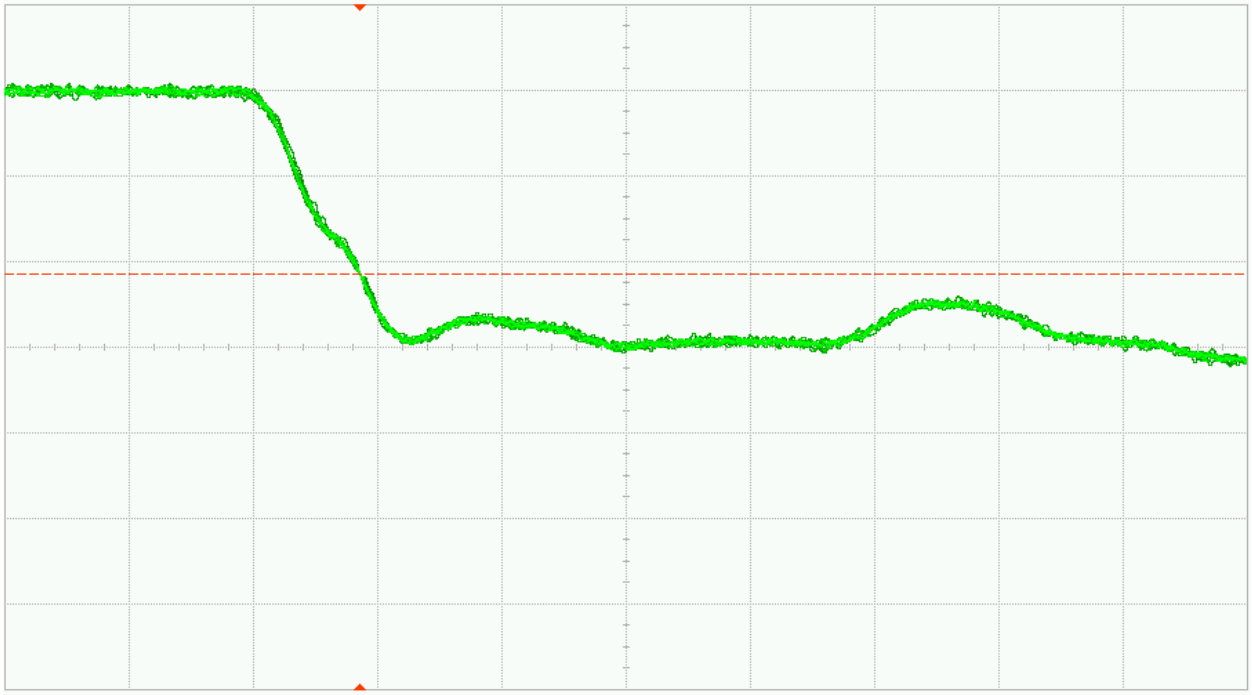

Fig. 36 (a). DUT 06877 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

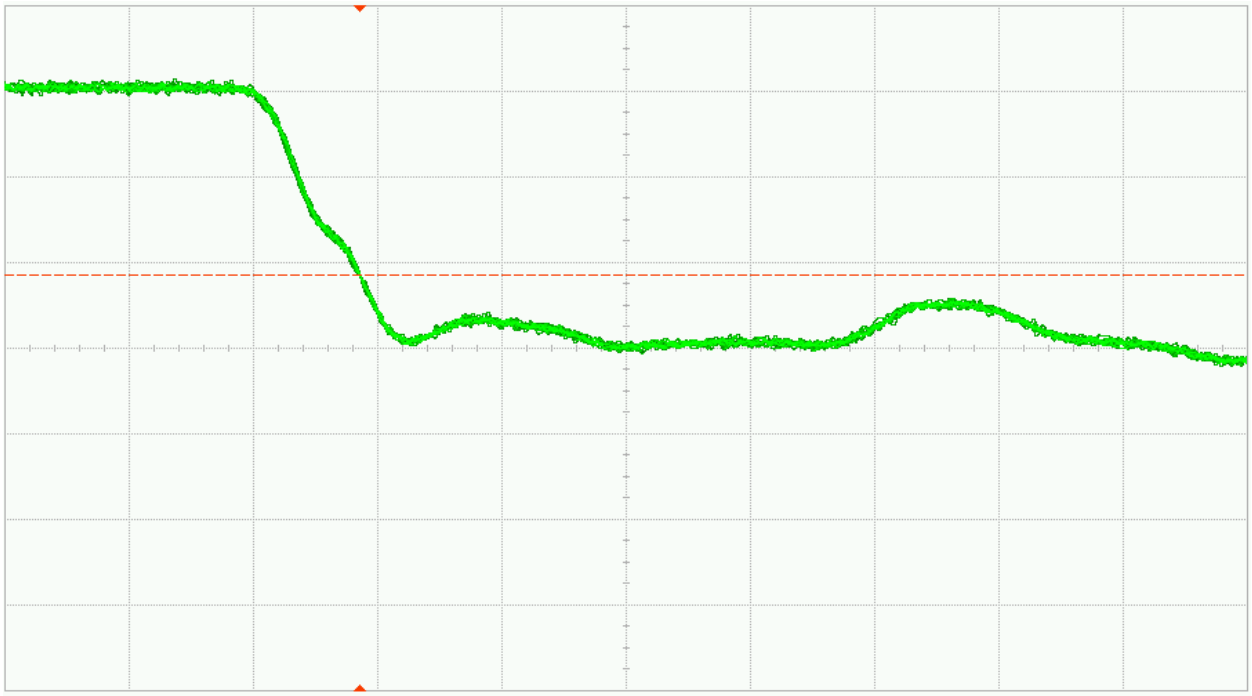

Fig. 36 (b). DUT 06877 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

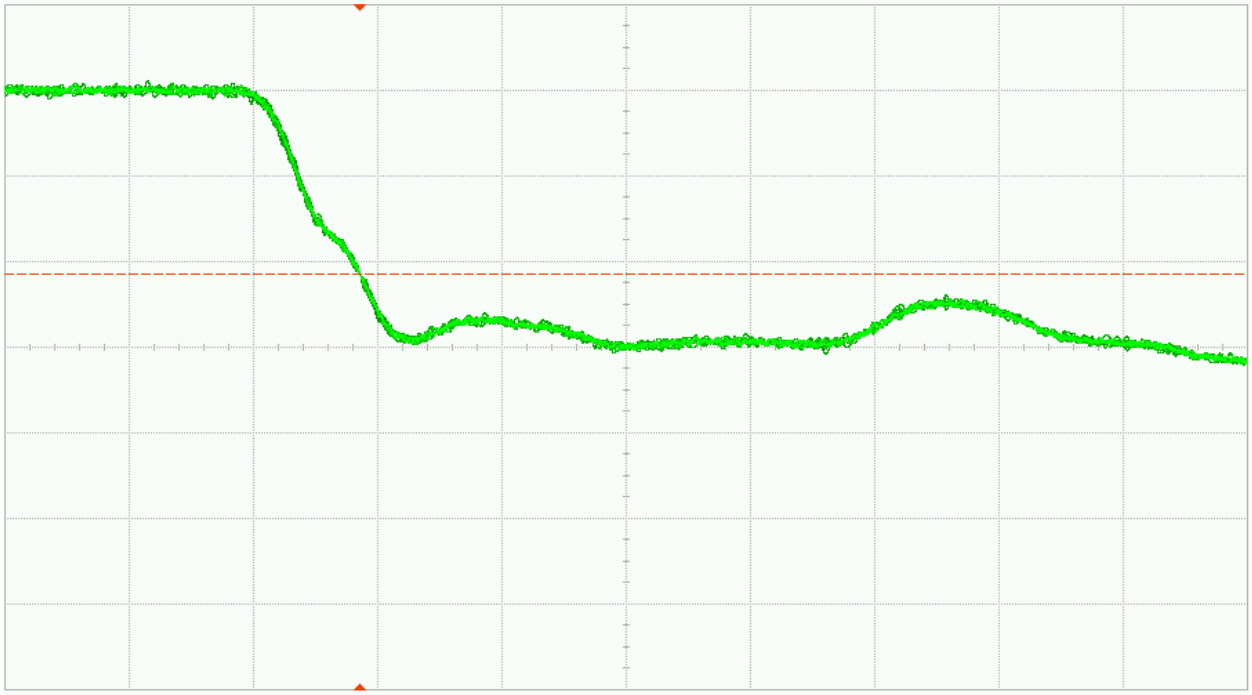

Fig. 37 (a). DUT 06917 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

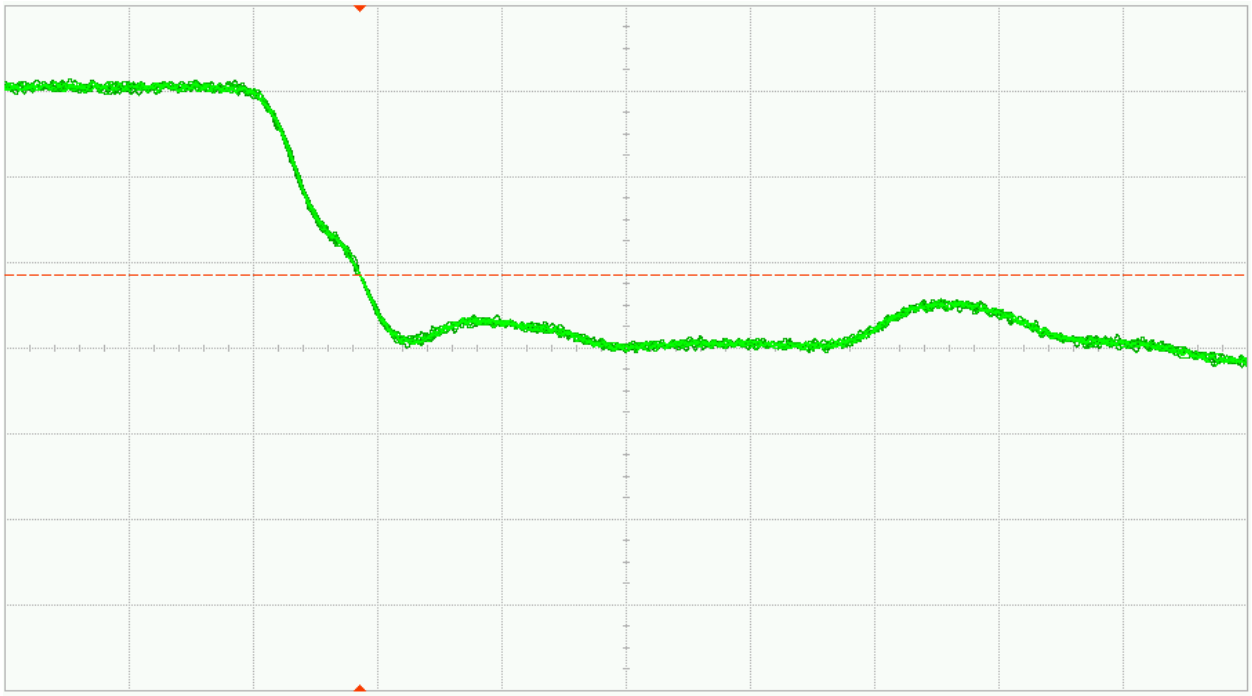

Fig. 37 (b). DUT 06917 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 35. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

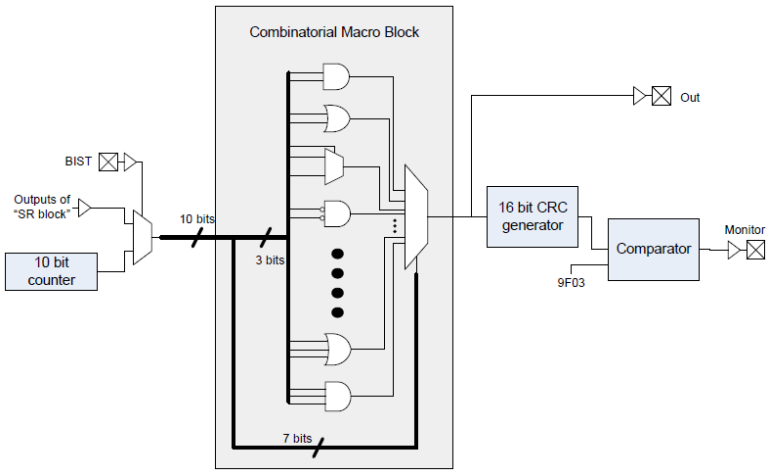

Fig. 38. Combo Block

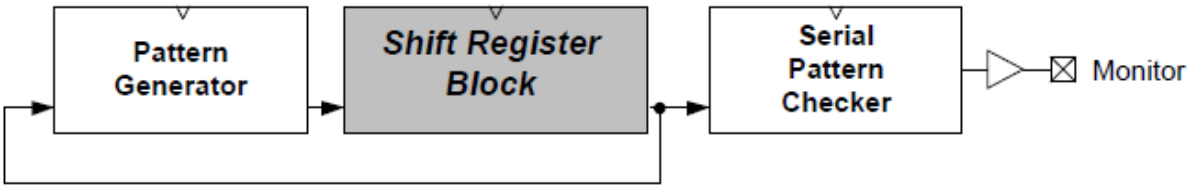

Fig. 39. Shift Register Block

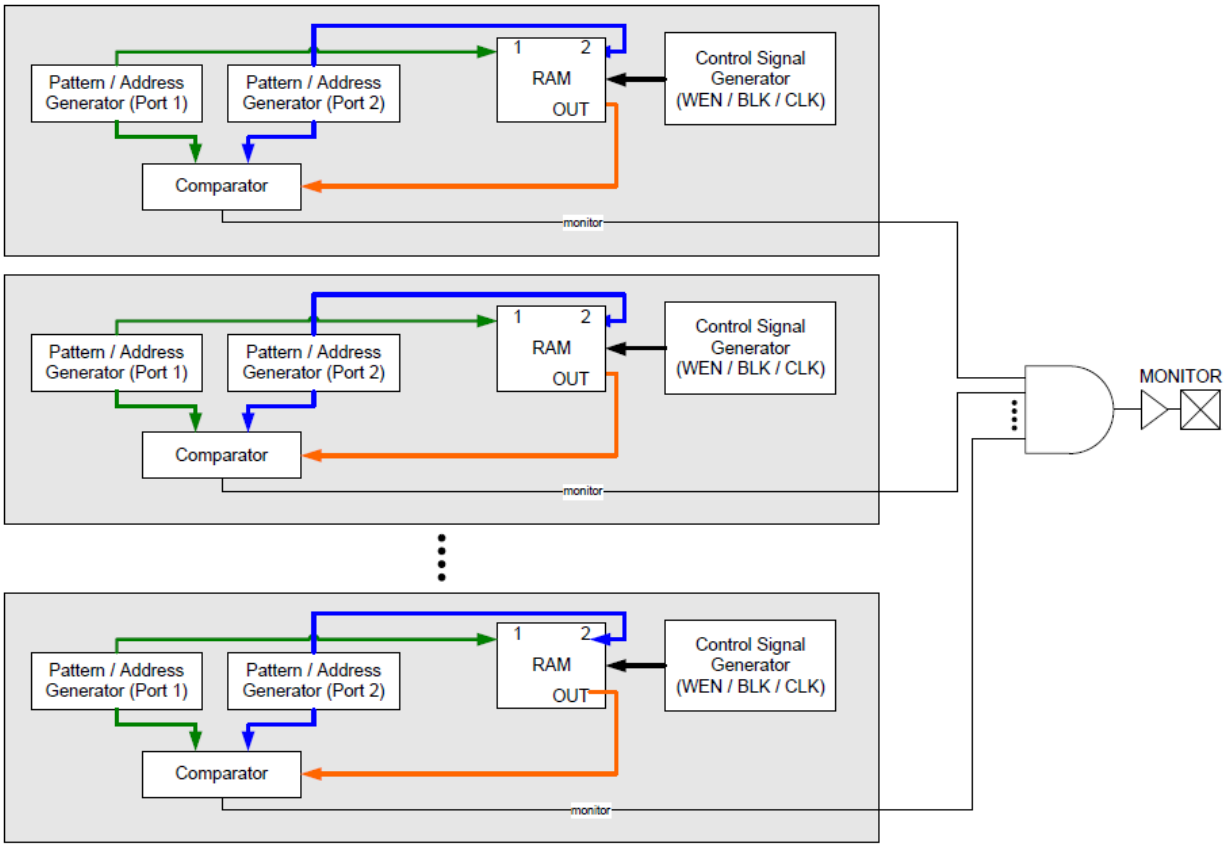

Fig. 40. Embedded Ram Blocks

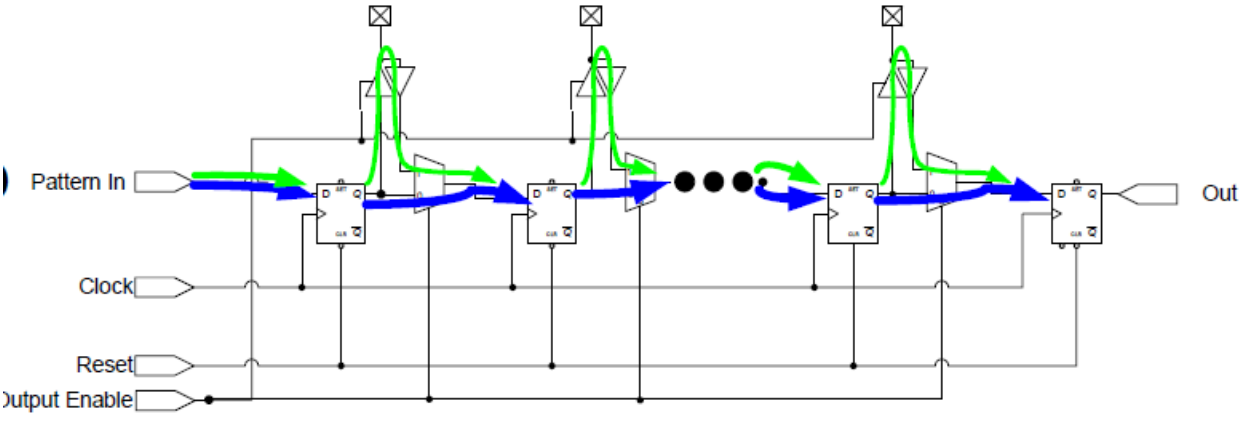

Fig. 41. IO Block

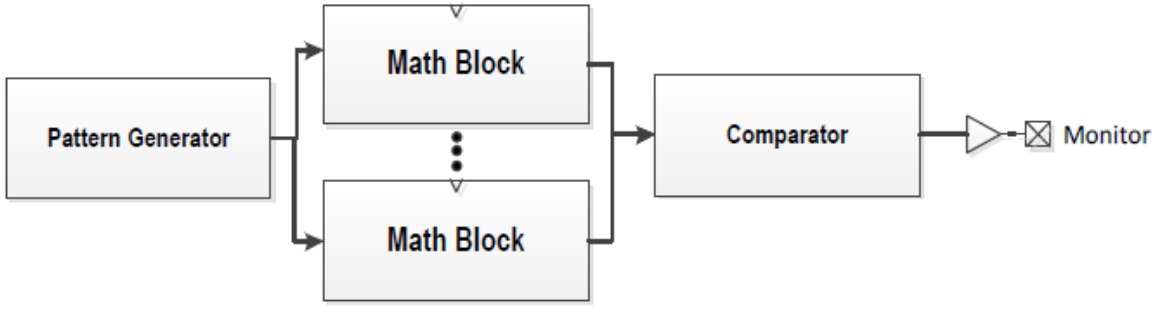

Fig. 42. Math Block

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